DESIGN-IN REFERENCE MANUAL

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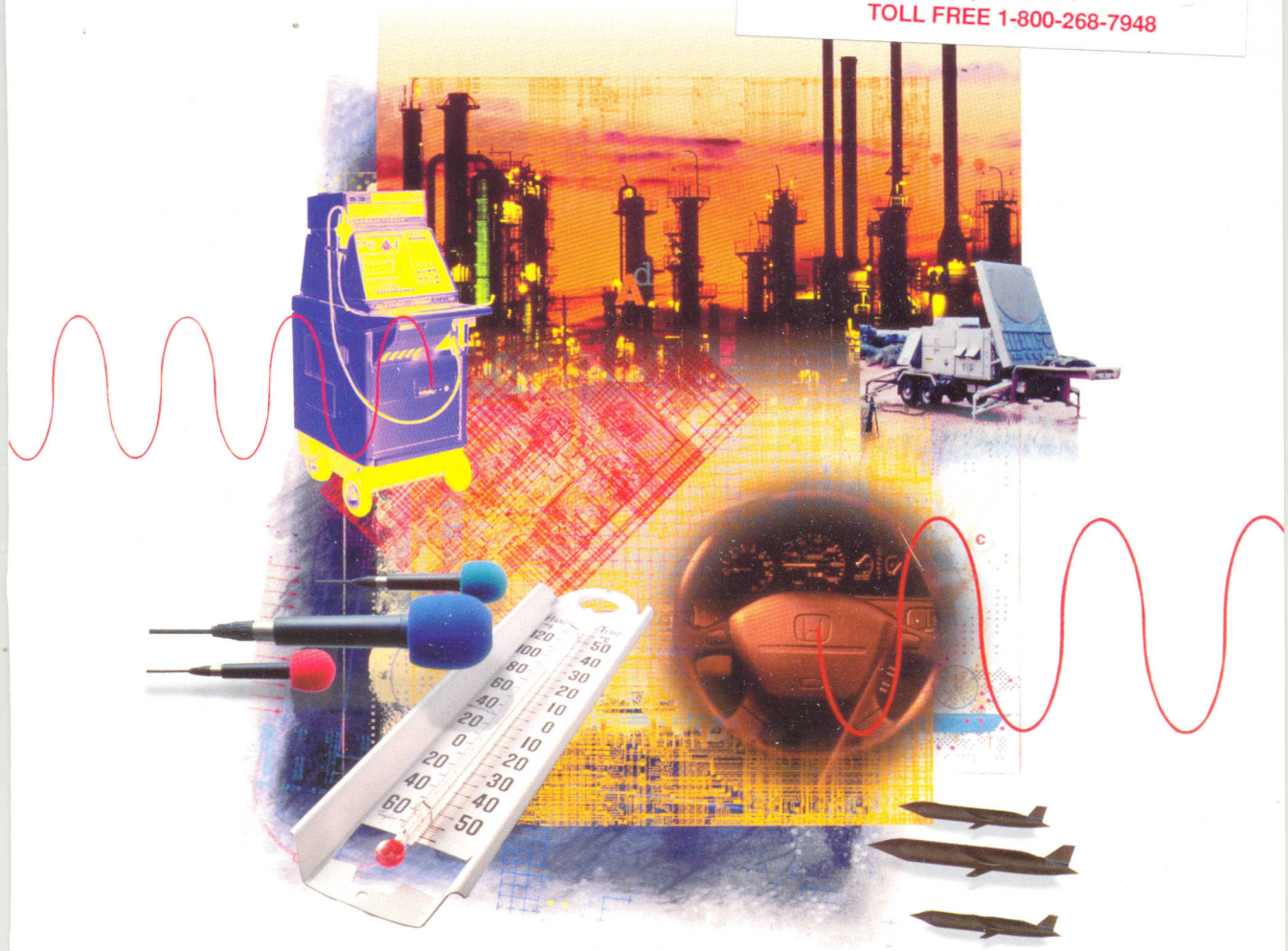

DATA CONVERTERS

AMPLIFIERS

SPECIAL LINEAR PRODUCTS

SUPPORT COMPONENTS

ANALOG DEVICES

How to Find Product Data in This Reference Manual

THIS VOLUME*

Contains Data Sheets, Selection Guides and a wealth of background information on state-of-the-art products that are suitable for new equipment design.

This volume is one member of a six-volume set of reference manuals describing and specifying Special Linear, Amplifier, Converter and Military/Aerospace products from Analog Devices, Inc.

IF YOU KNOW THE MODEL NUMBER

Turn to the product index at the back of the book and look up the model number. You will find the Section-Page location of any data sheet in this volume. You will find additional references for all other Analog Devices products currently available.

If you're looking for a form-and-function-compatible version of a product originally brought to market by some other manufacturer (second source), you may find it by adding our "AD" prefix and looking it up in the index. Or call our nearest sales office.

IF YOU DON'T KNOW THE MODEL NUMBER

Find your functional group in the list on the opposite page. Turn directly to the appropriate Section. You will find a functional Selection Tree and Selection Guide at the beginning of the Section. The Selection Tree and Selection Guide will help you find the products that are the closest to satisfying your need. Use them to compare all products in the category by salient criteria. A comprehensive Table of Contents is provided for your convenience on page 1–5 through 1–15.

IF YOU CAN'T FIND IT HERE . . . ASK

If you can't find the product you are looking for in this databook, please contact your local Analog Devices sales officer or phone our Applications Department at 617-937-1428 or 1-800-262-5643 (U.S.A. only).

See the Worldwide Sales Directory on pages 24-16 and 24-17 at the back of this volume for our sales office phone numbers.

*The fax retrieval system number shown on abridged and preliminary data sheets applies to U.S.A. and Canada only.

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- Signal Compression Components
- Switches & Multiplexers
- V/F & F/V Converters
- Voltage References

If you don't already own these volumes, you can have them FREE by getting in touch with Analog Devices or the nearest sales office or phoning 1-800-262-5643 (U.S.A. only) or 617-461-3392.

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Analog Devices, a *Fortune* 500 Industrials company, designs, manufactures and sells worldwide sophisticated electronic components and subsystems for use in real-world signal processing. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including several embodiments of CMOS, BiMOS, bipolar and hybrid integrated circuits, each optimized for specific attributes—and assembled products in the form of potted modules, printed-circuit boards and instrument packages.

State-of-the-art technologies (including surface micromachining) have been utilized (and in many cases invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Our popular IC products are available in both conventional and surface-mount packages (SOIC, LCC, PLCC), and many of our assembled products employ surface-mount technology to reduce manufacturing costs and overall size. A quarter-century of successful applications experience and continuing vertical integration ensure that these products are oriented to user needs. The ongoing application of today's state-of-the-art and the invention of tomorrow's state-of-the-art processes strengthen the leadership position of Analog Devices in standard data-acquisition and signal-processing products and make us a strong contender in high performance mixed-signal ASICs.

MAJOR PROGRESS

Since publication of the selection guides in the current set of Reference Manuals, Analog Devices has introduced more than 200 significant new products; they run the gamut from brand new product and market categories and technologies to standard products (with improvements in price, performance, or design) to augmented second source products. All of the newest products in the area of standard data converter, amplifier, and special purpose linear are included in this volume, with our latest offerings in DSP and special function products for audio, communications, and computer peripherals to be published in our forthcoming *DSP Reference Manual.*

Examples of the variety, performance, and innovation content of outstanding new linear and data converter products to be found in this volume include:

- **AD8001/AD8002** 800 MHz single and dual current feedback operational amplifiers that use only 50 mW from ± 5 volt supplies—first amplifiers from the XFCB process
- **ADXL05** second generation surface-micromachined accelerometer with ±5 g full scale and better than 1 milli-g useful resolution
- **AD7716** 22-bit quad-input sigma-delta ADC with 105 dB dynamic range at 146 Hz bandwidth on 50 mW from ±5 volt supplies
- **AD420** 16-bit complete digital-to-4-20 mA current loop driver with serial interface and 3 MHz update rate
- **AD720/AD721** RGB to NTSC/PAL encoders needing no external filters or delay lines
- **AD878** 14-bit 2.2 Msps ADC complete with SHA and reference using only 500 mW
- **AD607** complete receiver IF subsystem with mixer/AGC/RSSI from 3 volt supply
- **AD9101** 125 MHz sample-hold amplifier with 350 MHz signal bandwidth
- **OP291/OP491** rail-to-rail input/output dual and quad op amps that work down to a 2.7 volt single supply
- **AD7853/AD7858** single/octal input 12-bit 200 Msps sampling ADCs using only 5.5 mW from a 3 volt supply
- **REF190 Series** precision references with 0.5 volt dropout voltage, ±2 mV accuracy, and 45 µA supply current.

Many more could be added to this list.

DESIGN-IN REFERENCE MANUAL

This volume provides comprehensive technical data on the latest Analog Devices standard linear and data conversion products for all of the electronic industries we serve, with particular focus on the industrial, instrumentation, and military markets. This *Design-In Reference Manual* contains technical information on all of the standard linear products that we recommend for new designs. This is a companion volume and update to the series of Reference Manuals we began publishing in 1992. These manuals include the two-volume *Data Converter Reference Manual, Amplifier Reference Manual, Special Linear Reference Manual, and the Applications Reference Manual.* While this volume provides up-to-date information on our products, products which have appeared in a Reference Manual previously may have an abbreviated data sheet, so it is important to retain the entire set of Reference Manuals to have complete applications information about all of our products. If you need one of the previously printed Manuals, you can order it from our Literature Center.

In the approximately 2400 pages of this volume you will find:

- Recently released products with a complete data sheet containing all application and packaging information required to design in the product.
- Design-in products appearing in a previous Reference Manual which may have an abbreviated data sheet containing only specifications, packaging, pinout, and block diagram information, sufficient to make a design choice, but possibly not sufficient to complete a design; the full data sheets on these products are in the previously printed Reference Manuals.
- Advance technical information on upcoming new products which may prompt you to seek more up-to-date information on the product.
- Selection guides and product function trees for finding products rapidly.
- A representative list of available Analog Devices technical publications on real-world analog and digital signal processing.
- Our Worldwide Sales Directory.
- The complete Product Index to all Analog Devices products currently available or soon to be released which are covered in any of our Reference Manuals or the upcoming *DSP Reference Manual.*

The product data in this book are intended primarily for the majority of users who are concerned with new designs. For this reason, existing and available products that offer little if any unique advantage over newer products in future designs are listed in the Index, and data sheets may be available separately—but they are not published in this book.

TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for real-world signal processing. Besides tutorial material and comprehensive data sheets, including a large number in our reference manuals, we offer application notes, application guides, technical handbooks (at reasonable prices), and several free serial publications. For example, *Analog Briefings*® provides current information about products for military/avionics, and *Analog Dialogue*, our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, signal processing, control, and test. *DSPatch*® is a quarterly newsletter that brings its readers up-to-date applications information on our DSP products and the general field of digital signal processing. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to these reference manual catalogs—and general short-form selection guides—we also publish several short-form catalogs on specific product families. You will find typical publications described on pages 24–11 to 24–15 at the back of the book.

SALES AND SERVICE

Backing up our design and manufacturing capabilities and our extensive array of publications, is a network of distributors, plus sales offices and representatives throughout the United States and most of the world, staffed by experienced sales and applications engineers. Our Worldwide Sales Directory, as of the publication date, appears on pages 24–16 and 24–17 at the back of the book.

RELIABILITY

The manufacture of reliable products is a key objective at Analog Devices. The primary focus is a companywide Total Quality Management (TQM) Program. In addition, we maintain facilities that have been qualified under such standards as MIL-M-38510 (Class B and Class S) for ICs in the U.S., MIL-STD-1772 for hybrids, and ISO9000 (required by many European customers). Many of our products—both proprietary and second-source—have qualified for JAN part numbers; others are in the process. A larger number of products—including many of the newer ones just starting the JAN qualification process—are specifically characterized on Standard Military Drawings (SMDs). Most of our ICs are available in versions that comply with MIL-STD-883C Class B, and many also comply with Class S. We publish a *Military/Aerospace Reference Manual* for designers who specify ICs and hybrids for military contracts. The 1994 issue contains data on 379 product families. It also contains Mil/Aero Product Cross Reference Guides, radiation information and space qualified products information. Our newsletter *Analog Briefings* provides current information about the status of reliability at ADI.

Our PLUS program makes available standard devices (commercial and industrial grades, plastic or ceramic packaging) for *any* user with demanding application environments, at a small premium. Subjected to stringent screening, similar to MIL-STD-883 test methods, these devices are suffixed "/+" and are available from stock.

PRODUCTS NOT FOUND IN THE SELECTION GUIDES

For maximum usefulness to designers of new equipment, we have limited the contents of selection guides to standard products most likely to be used for the design of new circuits and systems with the exception of digital signal processing products. For DSP products to be included in our forthcoming *Digital Signal Processing Reference Manual*, please turn to page 24–6 at the back of this volume, Otherwise, if the model number of a product you are interested in is not in the Table of Contents, turn to page 24–4 where you will find a list of older products for which data sheets are available upon request. On page 24–7 you will find a guide to substitutions (where possible) for products no longer available.

ICs embodying combinations of functions that you need but cannot find among our standard offerings may be available to meet your specific requirements as custom designs. For more information, get in touch with Analog Devices. A complete Worldwide Sales Directory is included on pages 24–16 and 24–17.

PRICES

Accurate, up-to-date prices are an important consideration in making a choice among the many available product families. Since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices and distributors.

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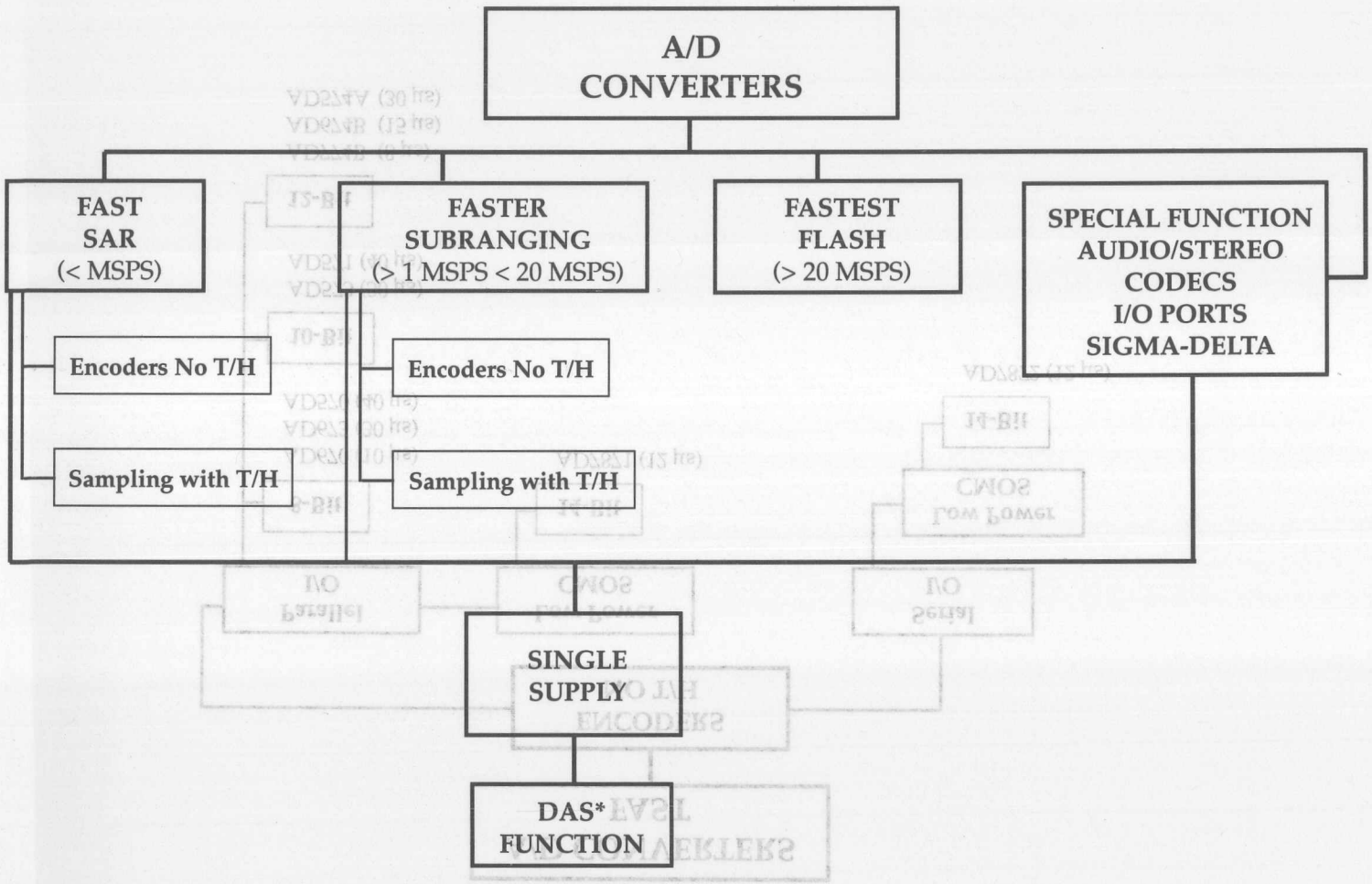
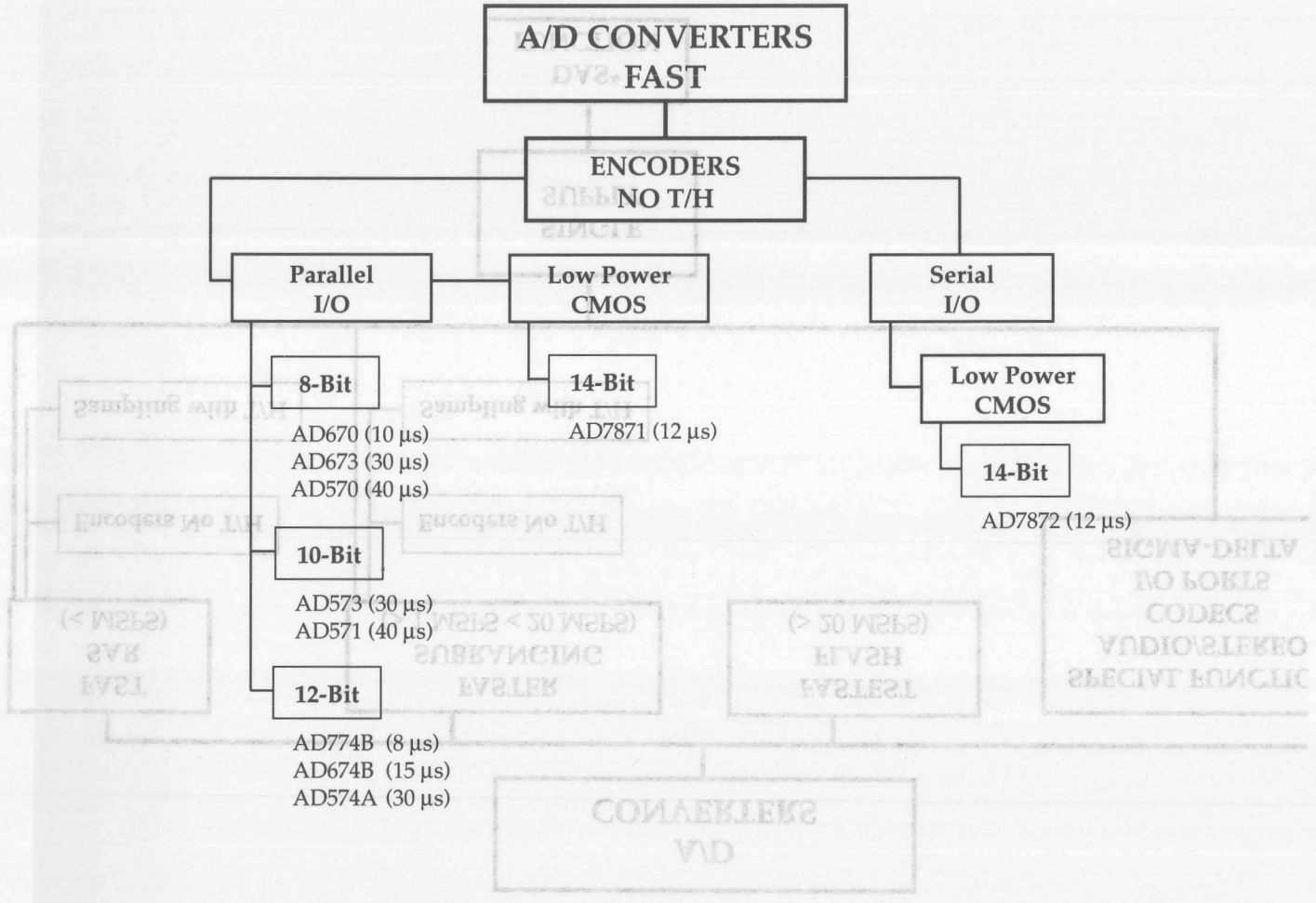
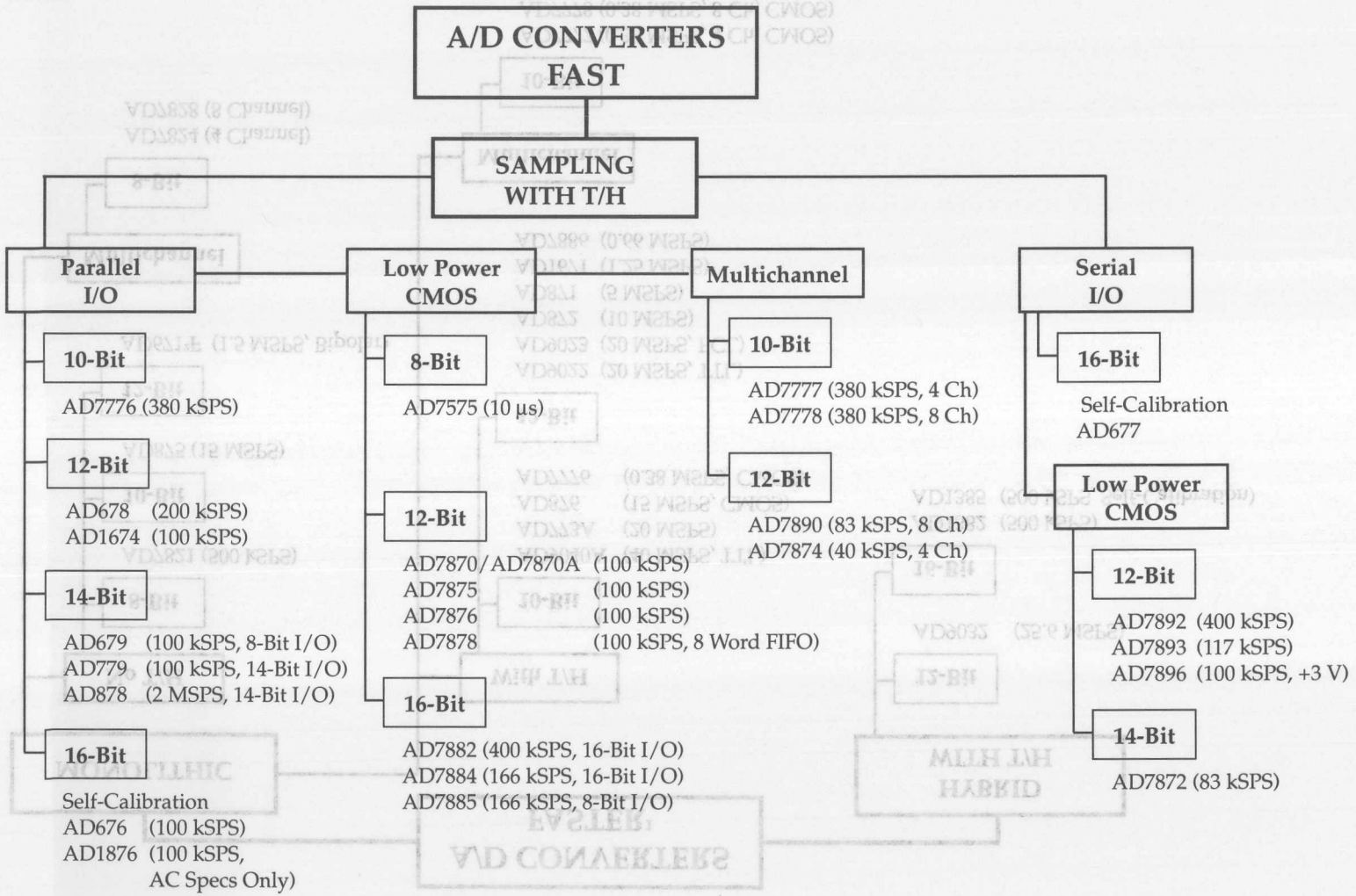


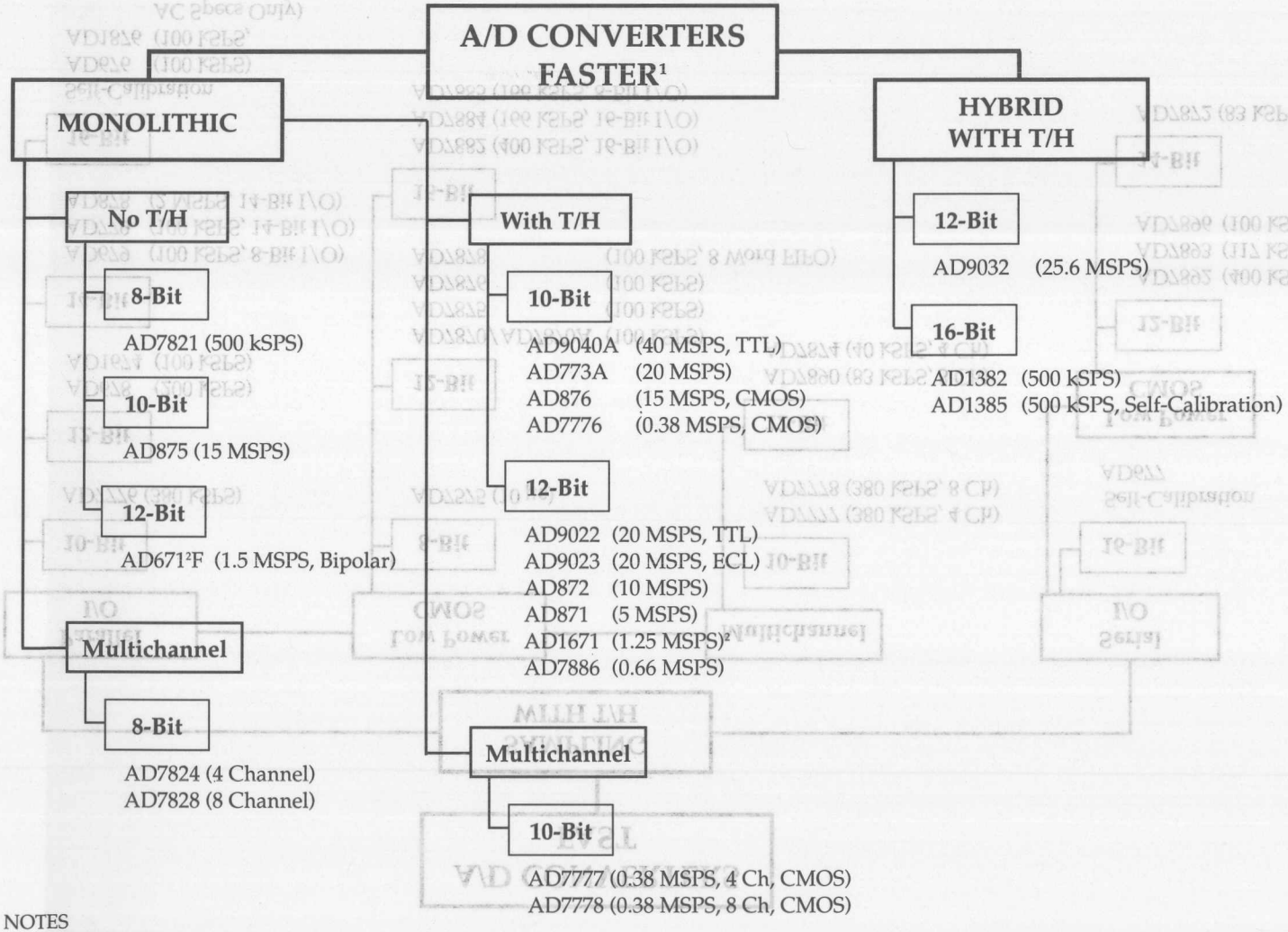
* DAS = Data Acquisition System: MUX, T/H & A/D

Selection Trees — Analog-to-Digital Converters

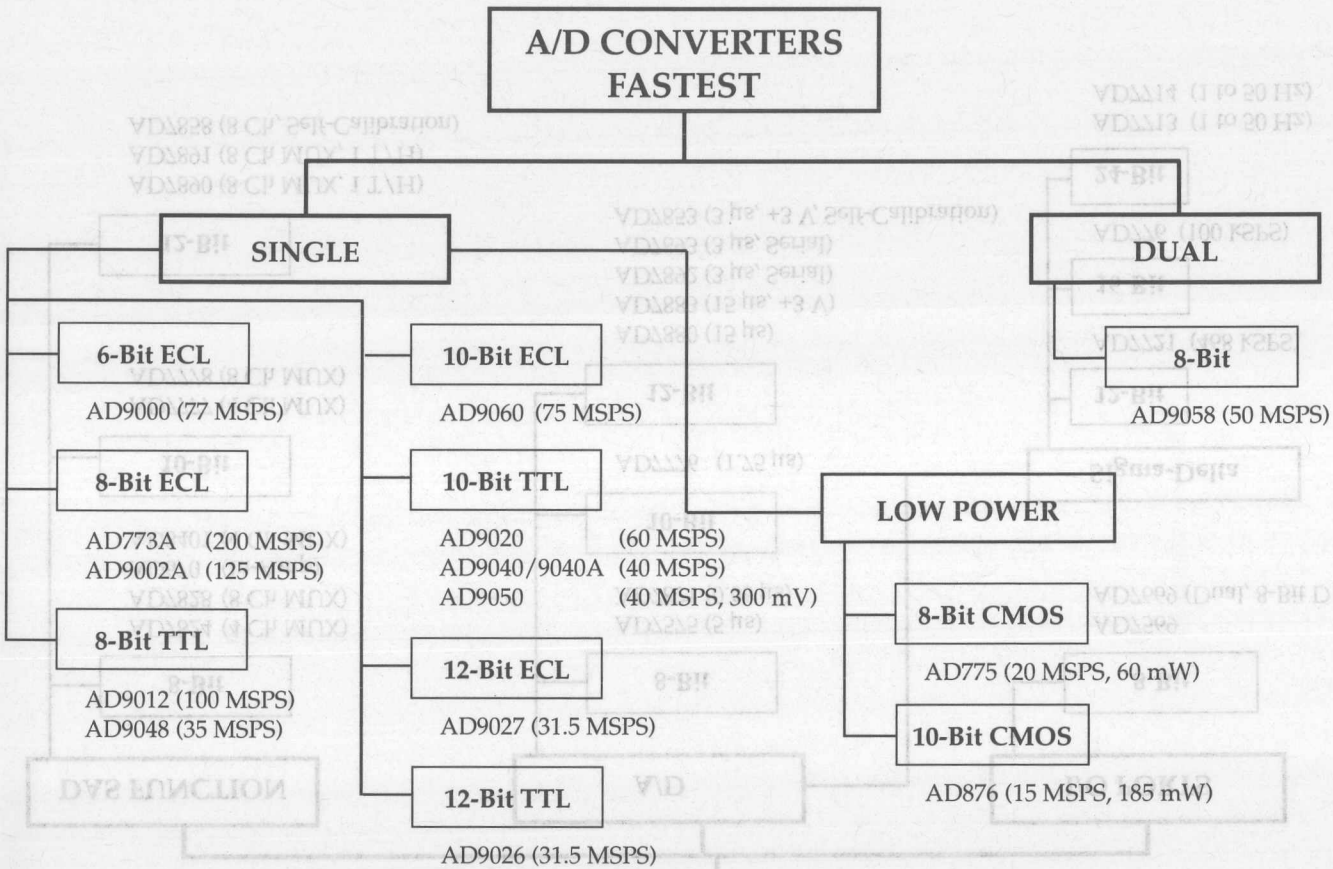



A/D CONVERTERS
FAST
SAMPLING
WITH T/H
Parallel
I/O
10-Bit
AD7776 (380 kSPS)
12-Bit
AD678 (200 kSPS)
AD1674 (100 kSPS)
14-Bit
AD679 (100 kSPS, 8-Bit I/O)
AD779 (100 kSPS, 14-Bit I/O)
AD878 (2 MSPS, 14-Bit I/O)
16-Bit
Self-Calibration
AD676 (100 kSPS)
AD1876 (100 kSPS,
AC Specs Only)
Low Power
CMOS
8-Bit
AD7575 (10 µs)
12-Bit
AD7870/AD7870A (100 kSPS)
AD7875 (100 kSPS)
AD7876 (100 kSPS)
AD7878 (100 kSPS, 8 Word FIFO)
16-Bit
AD7882 (400 kSPS, 16-Bit I/O)
AD7884 (166 kSPS, 16-Bit I/O)
AD7885 (166 kSPS, 8-Bit I/O)
Multichannel
10-Bit
AD7777 (380 kSPS, 4 Ch)
AD7778 (380 kSPS, 8 Ch)
12-Bit
AD7890 (83 kSPS, 8 Ch)
AD7874 (40 kSPS, 4 Ch)
Serial
I/O
16-Bit
Self-Calibration
AD677
Low Power
CMOS
12-Bit
AD7892 (400 kSPS)
AD7893 (117 kSPS)
AD7896 (100 kSPS, +3 V)
14-Bit
AD7872 (83 kSPS)

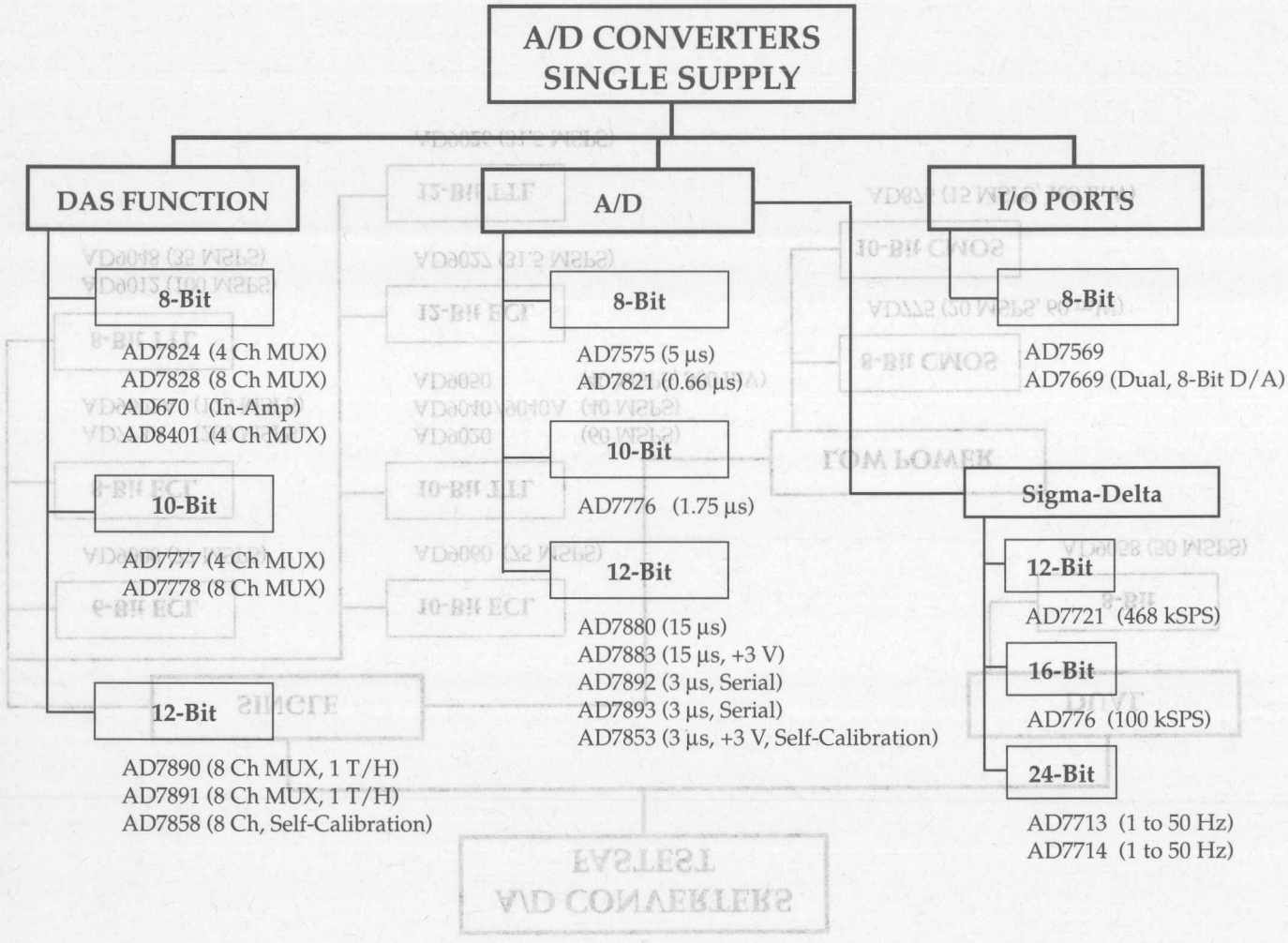
Selection Trees — Analog-to-Digital Converters

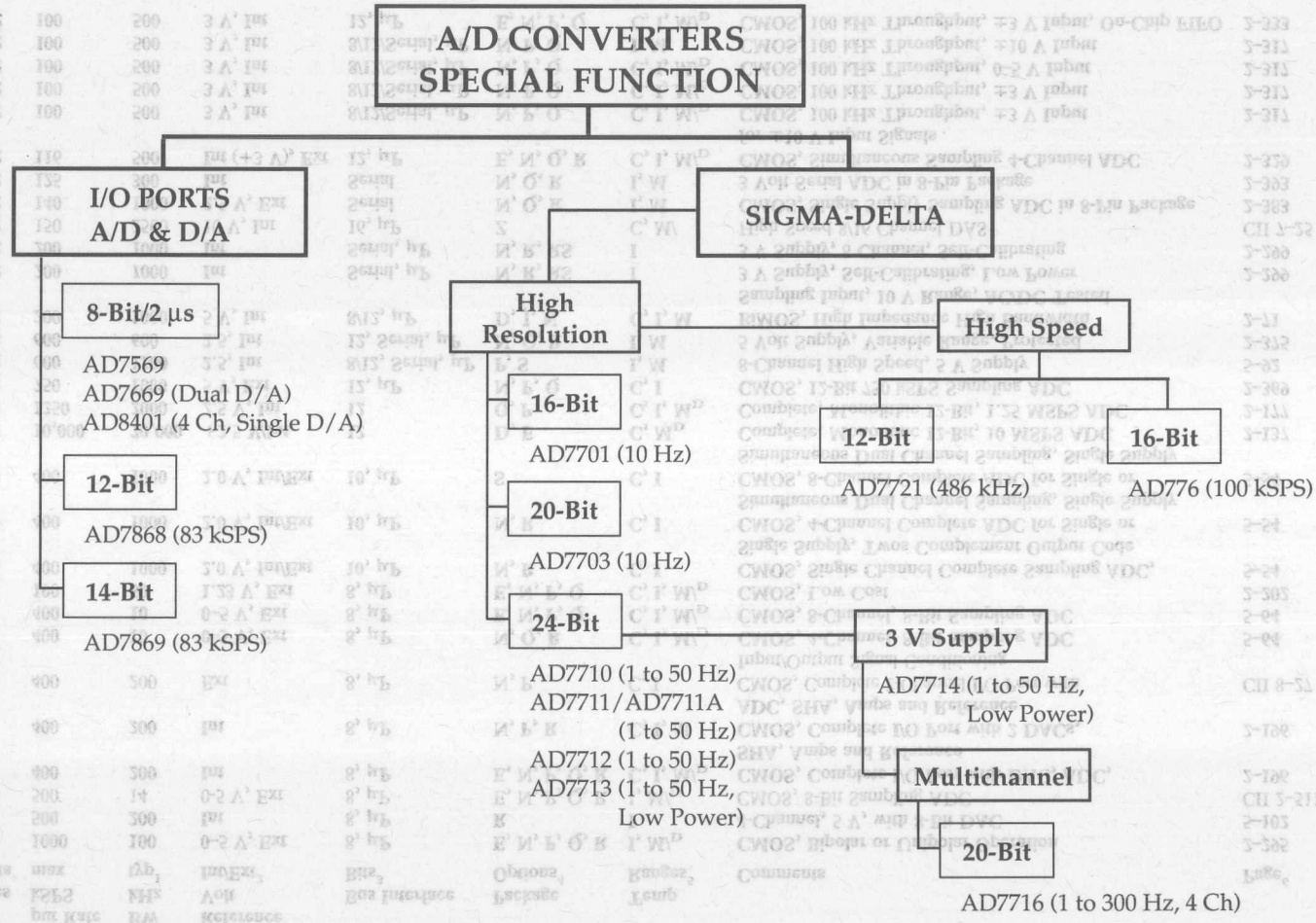


NOTES
[1] Subranging or 1/2 Flash
[2] Contact Factory For Versions Up to 2 MHz


A/D CONVERTERS
FASTEST
SINGLE
DUAL
6-Bit ECL
AD9000 (77 MSPS)
8-Bit ECL
AD773A (200 MSPS)
AD9002A (125 MSPS)
8-Bit TTL
AD9012 (100 MSPS)
AD9048 (35 MSPS)
10-Bit ECL
AD9060 (75 MSPS)
10-Bit TTL
AD9020 (60 MSPS)
AD9040/9040A (40 MSPS)
AD9050 (40 MSPS, 300 mV)
12-Bit ECL
AD9027 (31.5 MSPS)
12-Bit TTL
AD9026 (31.5 MSPS)
LOW POWER
8-Bit CMOS
AD775 (20 MSPS, 60 mW)
10-Bit CMOS
AD876 (15 MSPS, 185 mW)
8-Bit
AD9058 (50 MSPS)

Selection Trees — Analog-to-Digital Converters




A/D CONVERTERS
SPECIAL FUNCTION
I/O PORTS
A/D & D/A
8-Bit/2 µs
AD7569
AD7669 (Dual D/A)
AD8401 (4 Ch, Single D/A)
12-Bit
AD7868 (83 kSPS)
14-Bit
AD7869 (83 kSPS)
SIGMA-DELTA
High Resolution
16-Bit
AD7701 (10 Hz)
20-Bit
AD7703 (10 Hz)
24-Bit
AD7710 (1 to 50 Hz)
AD7711/AD7711A (1 to 50 Hz)
AD7712 (1 to 50 Hz)
AD7713 (1 to 50 Hz, Low Power)
High Speed
12-Bit
AD7721 (486 kHz)
16-Bit
AD776 (100 kSPS)
3 V Supply
AD7714 (1 to 50 Hz, Low Power)
Multichannel
20-Bit
AD7716 (1 to 300 Hz, 4 Ch)

Selection Guides—Analog-to-Digital Converters

Sampling ADCs

Model	Res Bits	Through-put Rate kSPS max	SHA BW kHz typ[1]	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Ranges[5]	Comments	Pag
AD7821	**8**	**1000**	**100**	**0–5 V, Ext**	**8, µP**	**E, N, P, Q, R**	**I, $M/_D$**	**CMOS, Bipolar or Unipolar Operation**	**2–2**
AD8401	**8**	**500**	**200**	**Int**	**8, µP**	**R**	**I**	**4-Channel, 5 V, with 8-Bit DAC**	**5–1**
AD7820	8	500	14	0-5 V, Ext	8, µP	E, N, P, Q, R	I, $M/_D$	CMOS, 8-Bit Sampling ADC	CII
AD7569	**8**	**400**	**200**	**Int**	**8, µP**	**E, N, P, Q, R**	**C, I, $M/_D$**	**CMOS, Complete I/O Port with DAC, ADC, SHA, Amps and Reference**	**2–1**
AD7669	**8**	**400**	**200**	**Int**	**8, µP**	**N, P, R**	**C, I, M**	**CMOS, Complete I/O Port with 2 DACs, ADC, SHA, Amps and Reference**	**2–1**
AD7769	8	400	200	Ext	8, µP	N, P	C, I	CMOS, Complete 2-Channel I/O Port with Input/Output Signal Conditioning	CII
AD7824	**8**	**400**	**10**	**0–5 V, Ext**	**8, µP**	**N, Q, R**	**C, I, $M/_D$**	**CMOS, 4-Channel, 8-Bit Sampling ADC**	**5–6**
AD7828	**8**	**400**	**10**	**0–5 V, Ext**	**8, µP**	**E, N, P, Q**	**C, I, $M/_D$**	**CMOS, 8-Channel, 8-Bit Sampling ADC**	**5–6**
AD7575	**8**	**190**	**50**	**1.23 V, Ext**	**8, µP**	**E, N, P, Q**	**C, I, $M/_D$**	**CMOS, Low Cost**	**2–2**
AD7776	**10**	**400**	**1000**	**2.0 V, Int/Ext**	**10, µP**	**N, R**	**C, I**	**CMOS, Single Channel Complete Sampling ADC, Single Supply, Twos Complement Output Code**	**5–5**
AD7777	**10**	**400**	**1000**	**2.0 V, Int/Ext**	**10, µP**	**N, R**	**C, I**	**CMOS, 4-Channel Complete ADC for Single or Simultaneous Dual Channel Sampling, Single Supply**	**5–5**
AD7778	**10**	**400**	**1000**	**2.0 V, Int/Ext**	**10, µP**	**S**	**C, I**	**CMOS, 8-Channel Complete ADC for Single or Simultaneous Dual Channel Sampling, Single Supply**	**5–5**
AD872	**12**	**10,000**	**70,000**	**+2.5 V/Int**	**12**	**D, E**	**C, M_D**	**Complete, Monolithic 12-Bit, 10 MSPS ADC**	**2–1**
AD1671	**12**	**1250**	**2000**	**2.5 V, Int**	**12**	**Q, P**	**C, I, M_D**	**Complete, Monolithic 12-Bit, 1.25 MSPS ADC**	**2–1**
AD7886	**12**	**750**	**1000**	**5 V, Ext**	**12, µP**	**N, P, Q**	**C, I**	**CMOS, 12-Bit 750 kSPS Sampling ADC**	**2–3**
AD7891	**12**	**600**	**1200**	**2.5, Int**	**8/12, Serial, µP**	**P, S**	**I, M**	**8-Channel High Speed, 5 V Supply**	**5–9**
AD7892	**12**	**600**	**600**	**2.5, Int**	**12, Serial, µP**	**N, Q, R**	**I, M**	**5 Volt Supply, Variable Range, Protected**	**2–3**
AD678	**12**	**200**	**1000**	**5 V, Int**	**8/12, µP**	**D, J, N**	**C, I, M**	**BiMOS, High Impedance High Bandwidth Sampling Input, 10 V Range, AC/DC Tested**	**2–7**
AD7853	**12**	**200**	**1000**	**Int**	**Serial, µP**	**N, R, RS**	**I**	**3 V Supply, Self-Calibrating, Low Power**	**2–2**
AD7858	**12**	**200**	**1000**	**Int**	**Serial, µP**	**N, R, RS**	**I**	**3 V Supply, 8 Channel, Self-Calibrating**	**2–2**
AD1341	12	150	2500	10 V, Int	16, µP	Z	C, M/	High Speed 8/16 Channel DAS	CII
AD7893	**12**	**140**	**1000**	**2.5 V, Ext**	**Serial**	**N, Q, R**	**I, M**	**CMOS, Single Supply Sampling ADC in 8-Pin Package**	**2–3**
AD7896	**12**	**125**	**300**	**Int**	**Serial**	**N, Q, R**	**I, M**	**3 Volt Serial ADC in 8-Pin Package**	**2–3**
AD7874	**12**	**116**	**500**	**Int (+3 V), Ext**	**12, µP**	**E, N, Q, R**	**C, I, $M/_D$**	**CMOS, Simultaneous Sampling 4-Channel ADC for ±10 V Input Signals**	**2–3**
AD7870	**12**	**100**	**500**	**3 V, Int**	**8/12/Serial, µP**	**N, P, Q**	**C, I, $M/_D$**	**CMOS, 100 kHz Throughput, ±3 V Input**	**2–3**
AD7870A	**12**	**100**	**500**	**3 V, Int**	**8/12/Serial, µP**	**N, P, Q**	**C, I, $M/_D$**	**CMOS, 100 kHz Throughput, ±3 V Input**	**2–3**
AD7875	**12**	**100**	**500**	**3 V, Int**	**8/12/Serial, µP**	**N, P, Q**	**C, I, $M/_D$**	**CMOS, 100 kHz Throughput, 0–5 V Input**	**2–3**
AD7876	**12**	**100**	**500**	**3 V, Int**	**8/12/Serial, µP**	**N, P, Q**	**I, M**	**CMOS, 100 kHz Throughput, ±10 V Input**	**2–3**
AD7878	**12**	**100**	**500**	**3 V, Int**	**12, µP**	**E, N, P, Q**	**C, I, $M/_D$**	**CMOS, 100 kHz Throughput, ±3 V Input, On-Chip FIFO**	**2–3**

Model	Res Bits	Through-put Rate kSPS max	SHA BW kHz typ[1]	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Ranges[5]	Comments	Page[6]
AD1674	**12**	**100**	**500**	**10 V, Int**	**8/12, µP**	**D, N, R**	**C, I, M**	**Complete AD574A Pinout Compatible, Sampling Input, AC/DC Tested**	**2–188**
AD7890	**12**	**100**	**1000**	**2.5 V, Ext**	**Serial**	**N, Q, R**	**I, M**	**8-Channel Single Supply Sampling ADC**	**5–76**
AD7868	**12**	**83**	**500**	**3 V, Int**	**Serial, µP**	**N, Q, R**	**I, $M/_D$**	**CMOS, Complete I/O Port with 12-Bit ADC and 12-Bit DAC**	**5–68**
AD7880	**12**	**66**	**33**	**5 V, Ext**	**12, µP**	**N, Q, R**	**I**	**Single +5 V Supply, Low Power Shutdown**	**2–337**
AD7883	**12**	**50**	**25**	**3.0, Ext**	**12, µP**	**N, R**	**I**	**3 Volt, 8 mW, Complete**	**2–353**
AD679	**14**	**128**	**1000**	**5 V, Int**	**8, µP**	**D, N, J**	**C, I, M**	**BiMOS, High Impedance, High Bandwidth Sampling Input, 10 V Input Range, AC/DC Tested**	**2–76**
AD779	**14**	**128**	**1000**	**5 V, Int**	**14, µP**	**D, N, J**	**C, I, M**	**BiMOS, High Impedance, High Bandwidth Sampling Input, 10 V Input Range, AC/DC Tested**	**2–115**
AD7869	**14**	**83**	**500**	**3 V, Int**	**Serial**	**N, Q, R**	**C, I**	**CMOS, Complete I/O Port with 14-Bit DAC and 14-Bit ADC**	**5–72**
AD7871	**14**	**83**	**500**	**3 V, Int**	**8/14/Serial, µP**	**N, Q, P**	**C, I, M**	**CMOS, Complete Sampling ADC, ±3 V Input**	**2–323**
AD7872	**14**	**83**	**500**	**3 V, Int**	**Serial, µP**	**N, Q, R**	**C, I, M**	**CMOS, Complete, Serial Interface, 16-Pin DIP/SOIC**	**2–323**
AD1382	**16**	**500**	**2200**	**10 V, Int**	**8, µP**	**D**	**C**	**High Speed, Guaranteed Dynamic Performance**	**5–20**
AD1385	**16**	**500**	**2200**	**10 V, Int**	**8, µP**	**D**	**C, $M/_D$**	**Similar to AD1382 with Autocalibration Ability, Guaranteed Dynamic Performance**	**5–24**
AD7882	**16**	**400**	**400**	**2.5 V, Ext**	**16, µP**	**S, Q**	**I, $M/_D$**	**16-Bit Self-Calibrating ADC**	**2–341**
AD7884	**16**	**166**	**83**	**3 V, Ext**	**16, µP**	**N, Q, P**	**I**	**CMOS, Low Power (250 mW), 5.3 µs Conversion**	**2–357**
AD7885	**16**	**166**	**83**	**3 V, Ext**	**8, µP**	**N, Q, P**	**I**	**Similar to AD7884, 28-Pin Package, Byte Output**	**2–357**
AD1876	**16**	**100**	**1000**	**3–7 V, Ext**	**Serial**	**N**	**C**	**Autocalibrating, 16-Pin DIP ADC, AC Tested**	**2–193**
AD676	**16**	**100**	**1000**	**3–10 V, Ext**	**16**	**D, N**	**C, I, M**	**Autocalibrating, 28-Pin DIP, Parallel Output**	**2–43**
AD677	**16**	**100**	**1000**	**3–10 V, Ext**	**Serial**	**D, N, R**	**C, I, $M/_{DS}$**	**Autocalibrating, 16-Pin Narrow DIP, Serial Output**	**2–57**

[1]X indicates that the internal SHA bandwidth is not specified in kHz.
[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[3]This column lists the data format for the bus with "µP" indicating microprocessor capability—e.g., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
[4]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[5]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[6]CII = *Data Converter Reference Manual, Volume II*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Selection Guides—Analog-to-Digital Converters

Nonsampling ADCs

Model	Res Bits	Conv Rate µs max	Reference Voltage Int/Ext[1]	Bus Interface Bits[2]	Package Options[3]	Temp Ranges[4]	Comments	Page[5]
ADC-908	8	6.0	−10 V, Ext	8, µP	N, Q, E, R	C, I, M/$_D$	CMOS, +5 V Operation, Fast	D
AD670	**8**	**10**	**Int**	**8, µP**	**D, N, E, P**	**C, I, M/$_D$**	**Single +5 V Supply, Including In-Amp and Reference**	**2–28**
AD7576	8	10	1.23 V, Ext	8, µP	N, Q, E, P	C, I, M/	CMOS, Low Cost, Single Supply	CII 2–509
AD7574	8	15	−10 V, Ext	8, µP	N, Q	C, I, M/$_D$	CMOS, +5 V Operation	CII 8–63
AD570	**8**	**25**	**Int**	**8**	**D**	**C, M/$_D$**		**2–17**
AD673	**8**	**30**	**Int**	**8, µP**	**D, N, P**	**C, M/$_D$**		**2–37**
AD7581	8	66.7	−5 V to (−15 V), Ext	8, µP	N, Q, P	C, I	CMOS 8-Bit ADC	CII 2–363
AD579	10	1.8	10 V, Int	10/Serial	D	SM/	High Speed with Low Power	CII 2–61
AD875	**10**	**0.067**	**2.4 V, +4 V, Ext**	**10**	**S**	**C**	**CMOS, 165 mW, 10-Bit, 15 MHz ADC**	**2–156**
ADC-910	10	6.0	2.5 V, Int	8, 10, µP	Q	C, I, M/	Bipolar, Fast with Byte Output	CII 2–819
AD571	**10**	**25**	**Int**	**10**	**D**	**C, M/$_D$**	**Complete 10-Bit ADC**	**2–17**
AD573	**10**	**30**	**Int**	**8/10, µP**	**D, N, P**	**C, M/$_D$**	**Complete 10-Bit ADC, Byte or Parallel Interface**	**2–21**
AD671	**12**	**0.5**	**5 V, Ext**	**12**	**D**	**C, M/**	**12-Bit 500 ns Monolithic ADC**	**2–32**
AD7586	12	1	−4 V, Ext	12, µP	N, Q, P	C, I, M	CMOS 12-Bit, 1 MHz ADC	CII 2–383
AD578	12	3	10 V, Int	12	D	C, M/$_D$	Complete, 3 µs, 12-Bit ADC	CII 2–61
AD7572A	12	3	Int	8/12, µP	N, Q, R	C, I	Improved Version of Industry Standard	CII 2–303
AD7572	12	5	Int	8/12, µP	N, Q, E, P	C, I, M/$_D$	Industry Standard, 12-Bit ADC	CII 2–299
ADC-170	12	5.6	−5.25 V, Ext	Serial	N, Q, R	I, M	Complete, 3 µs, 12-Bit ADC in 8-Pin Mini-DIP	CII 2–817
AD774B	12	8	10 V, Int	8/12, µP	D, N, R	C, I, M/	Faster Version of AD674B, Industry Standard	CII 2–109
AD ADC84	12	10	6.3 V, Int	12	D	C, I, M	Industry Standard	CII 2–809
AD ADC85	12	10	6.3 V, Int	12	D	C, I, M/	Industry Standard	CII 2–809
ADC-912A	12	10	−5 V, Ext	12, µP	N, Q, R	I, M/	CMOS, Improved Version of ADC-912	CII 2–831
AD5210	12	13	−10 V, Int/Ext	12	D	I, M/	Industry Standard (AD5211/12/14/15)	D
AD674B	**12**	**15**	**10 V, Int**	**8/12, µP**	**D, N, R**	**C, I, M/$_D$**	**Improved Version of AD674A/AD574A, Industry Standard**	**2–39**
AD572	12	25	10 V, Int	12	D	I, M/	12-Bit Successive Approximation ADC	CII 2–31
AD ADC80	12	30	6.3 V, Int	12	D	I	Industry Standard	CII 2–803
AD574A	**12**	**35**	**10 V, Int**	**8/12, µP**	**D, N, E, P**	**C, M/$_{DJ}$**	**Complete ADC with Reference and Clock; Industry Standard**	**2–24**
AD5200	12	50	−10 V, Int/Ext	12	D	I, M/	Industry Standard (AD5201/02/04/05)	D
AD7578	12	100	5 V, Ext	8, µP	D, N, Q	C, I, M/	CMOS, 1 LSB Total Unadjusted Error	CII 2–335

Model	Res Bits	Conv Rate µs max	Reference Voltage Int/Ext[1]	Bus Interface Bits[2]	Package Options[3]	Temp Ranges[4]	Comments	Page[5]
AD7582	12	100	5 V, Ext	8, µP	D, N, P, Q	C, I, M/	CMOS, 4 Channel, 1 LSB Total Unadjusted Error	CII 2–371
AD1377	16	10	Int	16, Serial	D	C	Complete, High Speed 16-Bit ADC	CII 2–215
							Operation over −25°C to +85°C	
AD1376	16	17	Int	16, Serial	D	C	Complete 16-Bit Converter; Industry Standard Pinout	CII 2–215
AD ADC71	16	50	6.3 V, Int	16	D	C	Industry Standard	CII 2–801
AD ADC72	16	50	6.3 V, Int	16	D	C, I	Industry Standard	CII 2–801
AD1170	18	1000	5 V, Int	8	N	C	7 to 22-Bit Programmable Integrating ADC	CII 2–203

[1]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.

[2]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 13-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.

[3]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.

[4]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

[5]CII = *Data Converter Reference Manual, Volume II*; D = Data Sheet. All other entries pertain to this volume.

Boldface Type: Datasheet information in this volume.

Selection Guides—Analog-to-Digital Converters

High Speed ADCs

Model	Res Bits	Through-put Rate MSPS min	Full Power BW MHz typ	Bus Interface Bits[1]	Reference Voltage Int/Ext[2]	Package Options[3]	Temp Range[4]	Page[5]	Comments
AD9000	**6**	**77**	**20**	**6**	**0.5–2 V, Ext**	**D, Q**	**C, M/**	**2–399**	**MIL-STD-883, Rev. C, Devices Availa Low Error Rate**
AD9002	**8**	**150**	**160**	**8**	**0.1–(−2.1) Ext**	**D, E, J**	**I, M/$_D$**	**2–402**	**Single Supply, Low Power, Low Input Capacitance, MIL-STD-883, Rev. C Device Available**
AD9012	**8**	**100**	**160**	**8**	**−2 V, Ext**	**E, J, Q**	**I, M/$_D$**	**2–406**	**TTL Outputs, Low Power, Low Input**
AD9058	**8**	**50**	**175**	**8**	**+2 V, Int**	**D, J**	**C, M/**	**2–461**	**Dual 8-Bit, TTL Output**
AD9048	**8**	**35**	**15**	**8**	**−2 V, Ext**	**E, J, Q**	**C, M/$_D$**	**2–455**	**35 MSPS, 8-Bit Video ADC, 16 pF Inp Capacitance**
AD775	**8**	**20**	**—**	**8**	**2.8, 0.6 V, Ext**	**N, R**	**C**	**2–95**	**Single Supply, Low Power, Low Input**
AD9060	**10**	**75**	**175**	**10**	**±1.75 V, Ext**	**E, Z**	**C, M/**	**2–465**	**Fastest 10-Bit ECL Monolithic ADC**
AD9020	**10**	**60**	**175**	**10**	**±1.75 V, Ext**	**E, Z**	**C, M/**	**2–410**	**Fastest 10-Bit TTL Monolithic ADC**
AD9040A	10	**40**	**48**	**10**	**+2.5 V, Int**	**N, R**	**C**	**2–444**	**SNR = 53 dB with 10.3 MHz Input @**
AD9050	**10**	**40**	**40**	**10**	**2.5 V, Int**	**R**	**C**	**2–458**	**Single Supply, Wide Range, Low Powe**
AD873	**10**	**30**	**200**	**10**	**3.0, 1.5 V, Ext**	**N, R**	**C**	**2–152**	**Single Supply, CMOS, Low Noise**
AD876	**10**	**20**	**250**	**10**	**4.0, 2.0 V, Ext**	**R, ST**	**C**	**2–169**	**Single Supply, 140 mW, 3.3 V Interfac**
AD773A	**10**	**20**	**100**	**10**	**+2.5, Ext**	**D**	**C**	**2–81**	**Low Power, 10-Bit 20 MSPS with On-C**
AD875	**10**	**15**	**—**	**10**	**+2 V, +4 V/Ext**	**S**	**C**	**2–156**	**CMOS, 165 mW, 10-Bit, 15 MHz ADC**
AD9027	**12**	**31**	**200**	**12**	**Int**	**D**	**I**	**2–429**	**Direct IF to Digital, Wideband, ECL**
AD9032	**12**	**25**	**220**	**12**	**Int**	**D, Z**	**I, M**	**2–437**	**World's Fastest Complete 12-Bit ADC**
AD9034	12	20	150	12	Int	D, Z	I, M	D	20 MSPS
AD9023	**12**	**20**	**115**	**12**	**Int**	**Q, Z**	**I, M**	**2–422**	**ECL Compatible Logic, with THA and**
AD9022	**12**	**20**	**115**	**12**	**Int**	**Q, Z**	**I, M**	**2–414**	**TTL Compatible Logic, with THA and**
AD872	**12**	**10**	**70**	**12**	**+2.5 V/Int**	**D, E**	**C, M/$_D$**	**2–137**	**Complete, Monolithic 12-Bit 10 MSPS**
AD9005A	12	10	38	12	Int	M	C, M/	CII 2–697	Complete 12-Bit ADC with T/H, Refere and Timing Circuitry
AD9007	12	10	38	12	Int	M	C	D	±5 V Only Version of AD9005A
AD871	**12**	**5**	**15**	**12**	**2.5, Int**	**D, E**	**C, M**	**2–121**	**Low Noise, High Accuracy, Wide Dyn**
AD1671	**12**	**1.25**	**2**	**12**	**2.5 V, Int**	**P, Q**	**C, I, M/$_D$**	**2–177**	**Complete, Monolithic 12-Bit, 1.25 MSI**
AD9014	14	10	60	14	Int	Board	C	CII 2–729	Wide Spurious Free Dynamic Range
AD878	**14**	**2.2**	**2**	**14**	**2.5, Int**	**P**	**C, I**	**2–173**	**Low Power, Wide Dynamic Range, Lo**

[1]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can l (12 bits) and is microprocessor compatible.

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[4]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade o temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.

[5]CII = *Data Converter Reference Manual, Volume II*; D = Data Sheet. All other entries refer to this volume.

Boldface Type: Data sheet information in this volume.

Sigma-Delta ADCs

Model	Res Bits	Input BW kHz	Through-put Rate kHz	Reference Voltage Int/Ext[1]	Bus Interface Bits[2]	Package Options[3]	Temp Ranges[4]	Page[5]	Comments
AD776	**16**	**50**	**100 to 400**	**2 V, Int**	**Serial**	**D**	**I**	**2–103**	**16-Bit 100 kSPS Oversampling ADC, Single Supply**
AD1878	16	24	2.5 to 50	3 V, Int	Serial	N	C	C II 2–295	Dual Channel, High Performance Stereo 16-Bit Oversampled ADC
AD7701	**16**	**10 Hz**	**4**	**2.5 V, Ext**	**Serial, µP**	**N, Q, R**	**I, M**	**2–206**	**16-Bit Sigma-Delta ADC, 0.1–10 Hz Input Bandwidth**
AD28msp02	16	4	8	2.5, Ext	Serial, µP	R, N	C	C I 4–25	Complete Voice Band Linear Codec with On-Chip Filtering
AD28msp01	16	3.4	7.2/8.0/9.6	2.5, Int	Serial, µP	R, P, N	C	C I 4–9	Complete Analog Front End for High Performance, DSP-Based Modems
AD1879	18	24	2.5 to 50	3 V, Int	Serial	N	C	C II 2–297	Dual Channel, High Performance Stereo 18-Bit Oversampled ADC
AD7703	**20**	**10 Hz**	**4**	**2.5 V, Ext**	**Serial, µP**	**N, Q, R**	**I, M**	**2–212**	**20-Bit Sigma-Delta ADC, 0.1–10 Hz Input Bandwidth**
AD7710	**24**	**2.62 to 262 Hz**	**0.01 to 1.0**	**2.5 V, Int**	**Serial, µP**	**N, Q, R**	**I, M**	**2–218**	**24-Bit Sigma-Delta Signal Conditioning ADC with 2 Differential Input Channels**
AD7714	**24**	**2.62 to 262 Hz**	**0.01 to 1.0**	**2.5 V, Ext**	**Serial, µP**	**N, Q, R, RS**	**I, M**	**2–271**	**3 Volt Supply, PGA, 5 Channels**
AD7711A	**24**	**2.62 to 262 Hz**	**0.01 to 1.0**	**2.5 V, Int**	**Serial, µP**	**N, Q, R**	**I, M**	**2–265**	**AD7711 Function—24 Bits, No Missing Codes**
AD7711	**21**	**2.62 to 262 Hz**	**0.01 to 1.0**	**2.5 V, Int**	**Serial, µP**	**N, Q, R**	**I, M**	**2–244**	**Similar to AD7710 but 24-Bit Sigma-Delta ADC with 1 Differential, 1 Single-Ended Input and RTD Current Sources**
AD7712	**21**	**2.62 to 262 Hz**	**0.01 to 1.0**	**2.5 V, Int**	**Serial, µP**	**N, Q, R**	**I, M**	**2–218**	**24-Bit ADC with 1 Differential Input Channel and 1 High Voltage Input Channel**
AD7713	**21**	**0.52 to 52.4 Hz**	**2.0 to 200 Hz**	**2.5 V, Ext**	**Serial, µP**	**N, Q, R**	**I, M**	**2–244**	**Loop Powered 24-Bit Sigma-Delta Signal Conditioning ADC**
AD7716	**22**	**36.5 to 584 Hz**	**1 (max)**	**2.5 V, Ext**	**Serial**	**S, P**		**5–40**	**22-Bit Data Acquisition System with with 4 Independent Channels**
AD1848	16	8 to 48 kHz	8 to 48 kHz	2.25 V, Int	8	P, S	C	D	16-Bit Parallel SoundPort® Stereo Codec. Stereo ADCs and Stereo DACs, PGA, Attenuator and All Filters
AD1849	16	8 to 48 kHz	8 to 48 kHz	2.25 V, Int	Serial	P	C	D	16-Bit Serial SoundPort® Stereo Codec. Stereo ADCs and Stereo DACs, PGA, Attenuator and All Filters. Operates on +5 V Supplies
AD7715	**16**	**5 to 131 Hz**	**20 to 500 Hz**	**2.5 V, Ext**	**Serial, µP**	**N, R**	**I**	**5–28**	**3 Volt, PGA, Low Power, 3-Wire**
AD7721	**12**	**210**	**468**	**2.5 V, Ext**	**12/Serial, µP**	**N, Q, R**	**I, M**	**2–287**	**5 Volt Supply, FIR Filter, 16-Bit Resolution**

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Selection Guides—Analog-to-Digital Converters

Multiplexed ADCs

Model	Res Bits	# Chan	Conv Time µs	SHA BW kHz	Reference Volt Int/Ext[1]	Bus Interface Bits[2]	Package Options[3]	Temp Ranges[4]	Comments	Page[5]
AD7769	8	2	2.5	200	Ext	8, µP	N, P	C, I	CMOS, Complete 2-Channel I/O Port with Input/Output Signal Conditioning	CII 8–27
AD7824	**8**	**4**	**2.5**	**10**	**0–5 V, Ext**	**8, µP**	**N, Q, R**	**C, I, M/$_D$**	**CMOS, On-Chip Track-Hold**	**5–64**
AD8401	**8**	**4**	**2**	**200**	**Int**	**8, µP**	**R**	**I**	**5 Volt Supply, DAC Out, High Speed**	**5–102**
AD7828	**8**	**8**	**2.5**	**10**	**0–5 V, Ext**	**8, µP**	**N, Q, E, P**	**C, I, M/$_D$**	**CMOS, On-Chip Track-Hold**	**5–64**
AD7777	**10**	**4**	**2.5**	**1000**	**2.0 V, Int**	**10, µP**	**N, R**	**I**	**Dual SHA, Offset Adjust, CMOS**	**5–54**
AD7778	**10**	**8**	**2.5**	**1000**	**2.0 V, Int**	**10, µP**	**S**	**I**	**Dual SHA, Offset Adjust, CMOS**	**5–54**
AD1341	12	8/16	6.67	2500	10 V, Int	16, µP	Z	C, M	High Speed, 16-Channel Programmable 12-Bit DAS with 25 ns Bus Interface	CII 7–25
AD7874	**12**	**4**	**32.5 (for 4 Channels)**	**500**	**3 V Int**	**12, µP**	**N, Q, R**	**C, I, M/$_D$**	**CMOS, Simultaneous Sampling Four-Channel 29 kHz ADC for ±10 V Input Signals**	**2–329**
AD363R	12	8/16	40	2000	10 V, Int	12, µP	D	C, M	High Speed, 16-Channel, 12-Bit DAS	CII 7–5
AD364R	12	8/16	50	2000	10 V, Int	12, µP	D	C, M	16-Channel, 12-Bit DAS with Three-State Buffers	CII 7–5
AD7582	12	4	100	—	4 V–6 V, Ext	12, µP	D, N, P, Q	C, I, M/	CMOS, 1 LSB Total Unadjusted Error	CII 2–371
AD7890	**12**	**8**	**5**	**1000**	**2.5 V, Ext**	**Serial, µP**	**N, Q, R**	**I, M**	**CMOS, 8-Channel Multiplexed ADC**	**5–76**
AD7858	**12**	**8**	**4.5**	**1000**	**Int**	**Serial, µP**	**N, R, RS**	**I**	**3 Volt Supply, Low Power, 3-Wire**	**2–299**
AD7891	**12**	**8**	**1.6**	**1200**	**2.5 V, Int**	**12, Serial, µP**	**P, S**	**I**	**5 Volt, Input Protected, Range Selectable**	**5–92**
AD7714	**24**	**5**	**1–100 ms**	**—**	**2.5 V, Ext**	**Serial, µP**	**N, Q, R, RS**	**I, M**	**3 Volt Supply, PGA, Prog. Filter**	**2–271**

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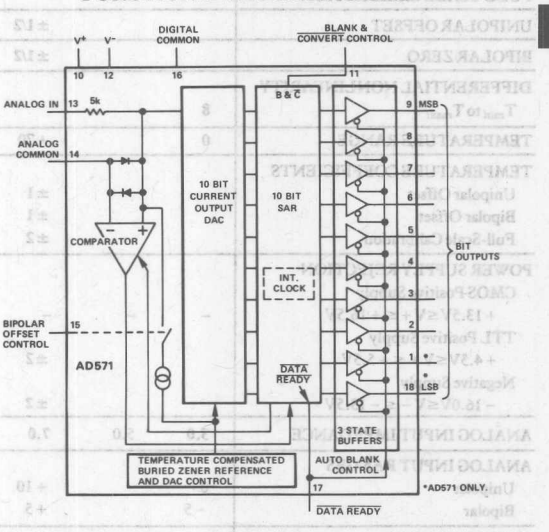
8- and 10-Bit Analog-to-Digital Converters

AD570/AD571*

FEATURES

Complete A/D Converters with Reference and Clock
AD570: 8 Bit
AD571: 10 Bit
Fast Successive Approximation Conversion – 25μs
No Missing Codes Over Temperature
Digital Multiplexing – 3 State Outputs
18-Pin Ceramic DIP
Low Cost Monolithic Construction
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTIONS

The AD570/AD571 are successive approximation A/D converters consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform full accuracy conversions in 25μs.

The AD570/AD571 incorporate advanced integrated circuit design and processing technologies. They employ I^2L (integrated logic) processing in the fabrication of the SAR function. Laser trimming of the high stability SiCr thin-film resistor ladder network insures high accuracy, which is maintained with a temperature compensated, subsurface Zener reference.

Operating on supplies of +5V to +15V and −15V, the AD570/AD571 will accept analog inputs of 0 to +10V, unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three-state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ high blanks the outputs and readies the device for the next conversion.

The devices are available in two versions: the "J" and "K" specified for the 0 to +70°C temperature range. The "S" guarantees the specified accuracy and no missing codes from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD571 is a complete 10-bit A/D converter. The AD570 is an 8-bit version which employs the same architecture. No external components are required to perform a conversion.
2. The AD570/AD571 are single chip devices employing advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The converters accept either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
4. Each device offers the specified accuracy with no missing codes over its entire operating temperature range.
5. Operation is guaranteed with −15V and +5V to +15V supplies. The devices will also operate with a −12V supply.
6. The AD570 and AD571 are available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current /883B data sheet for detailed specifications.

*Covered by Patent Nos. 3,940,760; 4,213,806; 4,136,349.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD570/AD571 SPECIFICATIONS (T_A = +25°C, V+ = +5V, V− = −12V or −15V, all voltages mea-

RELATIVE ACCURACY							
T_{min} to T_{max}			**±1/2**			**±1/2**	LSB
FULL-SCALE CALIBRATION		±2			±2		LSB
UNIPOLAR OFFSET			**±1/2**			**±1/2**	LSB
BIPOLAR ZERO			**±1/2**			**±1/2**	LSB
DIFFERENTIAL NONLINEARITY							
T_{min} to T_{max}	**8**			**8**			Bits
TEMPERATURE RANGE	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS							
Unipolar Offset			**±1**			**±1**	LSB
Bipolar Offset			**±1**			**±1**	LSB
Full-Scale Calibration			**±2**			**±2**	LSB
POWER SUPPLY REJECTION							
CMOS Positive Supply							
+13.5V≤V+≤+16.5V	–	–	–	–	–	–	LSB
TTL Positive Supply							
+4.5V≤V+≤+5.5V			**±2**			**±2**	LSB
Negative Supply							
−16.0V≤V−≤−13.5V			**±2**			**±2**	LSB
ANALOG INPUT IMPEDANCE	**3.0**	5.0	**7.0**	**3.0**	5.0	**7.0**	kΩ
ANALOG INPUT RANGES							
Unipolar	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	V
OUTPUT CODING							
Unipolar	Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT							
Output Sink Current							
(V_{OUT} = 0.4V max, T_{min} to T_{max})	**3.2**			**3.2**			mA
Output Source Current							
(V_{OUT} = 2.4V max, T_{min} to T_{max})	**0.5**			**0.5**			mA
Output Leakage			**±40**			**±40**	µA
LOGIC INPUTS							
Input Current			**±100**			**±100**	µA
Logic "1"	**2.0**			**2.0**			V
Logic "0"			**0.8**			**0.8**	V
CONVERSION TIME							
T_{min} to T_{max}	**15**	25	**40**	**15**	25	**40**	µs
POWER SUPPLY							
V+	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	V
V−	**−12.0**	−15	**−16.5**	**−12.0**	−15	**−16.5**	V
OPERATING CURRENT							
V+		7	**10**		7	**10**	mA
V−		9	**15**		9	**15**	mA
PACKAGE OPTION[2,3]							
Ceramic (D-18)	AD570JD			AD570SD			

NOTES

[1]The AD570 is a selected version of the AD571 10-bit A-to-D converter. Only TTL logic inputs should be connected to Pins 1 and 18 (or no connection made) or damage may result.

[2]D = Ceramic DIP. For outline information see Package Information section.

[3]For details on grade and package offerings for SD-grade in accordance with MIL-STD-883, refer to Analog Devices Military Products databook or current /883B data sheet.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

T_{min} to T_{max}			±1			±1/2			±1	LSB
FULL-SCALE CALIBRATION		±2			±2			±2		LSB
UNIPOLAR OFFSET			±1			±1/2			±1	LSB
BIPOLAR ZERO			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY, T_A	10			10			10			Bits
T_{min} to T_{max}	9			10			10			Bits
TEMPERATURE RANGE	0		+70	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS										
Unipolar Offset			±2			±1			±2	LSB
Bipolar Offset			±2			±1			±2	LSB
Full-Scale Calibration			±4			±2			±5	LSB
POWER SUPPLY REJECTION										
CMOS Positive Supply										
+13.5V≤V+≤+16.5V	–	–	–			±1	–	–	–	LSB
TTL Positive Supply										
+4.5V≤V+≤+5.5V			±2			±1			±2	LSB
Negative Supply										
−16.0V≤V−≤−13.5V			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	−5		+5	V
OUTPUT CODING										
Unipolar	Positive True Binary			Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT										
Output Sink Current										
(V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2			3.2			3.2			mA
Output Source Current[1]										
(V_{OUT} = 2.4V max, T_{min} to T_{max})	0.5			0.5			0.5			mA
Output Leakage			±40			±40			±40	µA
LOGIC INPUTS										
Input Current			±100			±100			±100	µA
Logic "1"	2.0			2.0			2.0			V
Logic "0"			0.8			0.8			0.8	V
CONVERSION TIME										
T_{min} to T_{max}	15	25	40	15	25	40	15	25	40	µs
POWER SUPPLY										
V+	+4.5	+5.0	+7.0	+4.5	+5.0	+16.5	+4.5	+5.0	+7.0	V
V−	−12.0	−15	−16.5	−12.0	−15	−16.5	−12.0	−15	−16.5	V
OPERATING CURRENT										
V+		7	10		7	10		7	10	mA
V−		9	15		9	15		9	15	mA
PACKAGE OPTION[2,3]										
Ceramic (D-18)		AD571JD			AD571KD			AD571SD		

NOTES

[1]The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

[2]D = Ceramic DIP. For outline information see Package Information section.

[3]For details on grade and package offerings for SD-grade in accordance with MIL-STD-883, refer to Analog Devices Military Products databook or current /883B data sheet.

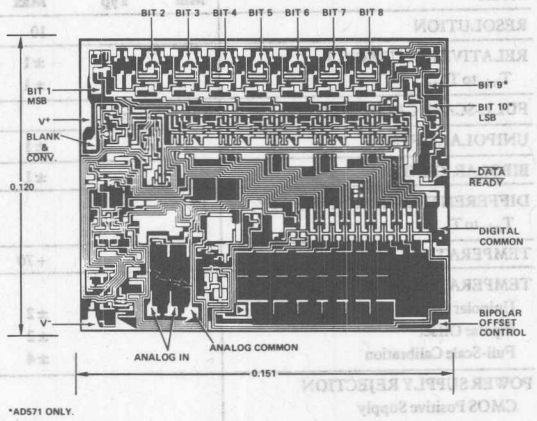
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common AD570J, S/AD571J, S	0 to +7V
AD571K	0 to +16.5V
V− to Digital Common	0 to −16.0V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (Blank Mode)	0 to V+
Power Dissipation	800mW

CHIP BONDING DIAGRAM



CIRCUIT DESCRIPTION

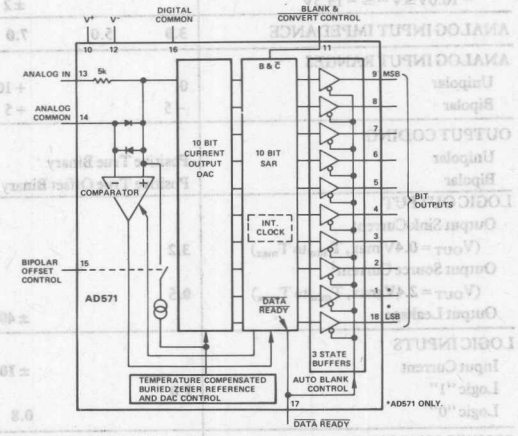
The AD571 is a complete 10-bit A/D converter which requires no external components to provide the complete successive approximation analog-to-digital conversion function. The AD570 is an 8-bit version. A functional block diagram of the AD570/AD571 is shown below. Upon receipt of the CONVERT command, the internal 10-bit (AD571) current output DAC is sequenced by the I^2L successive approximation register (SAR) from its most-significant bit (MSB) to least-significiant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ input resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current. If the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ±1/2LSB (0.05%).

Upon completion of the sequences, the SAR sends out a DATA READY signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and CONVERT line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle. Details of the timing are given further on.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows a positive bipolar offset current to be injected into the summing (+) node of the comparator to offset the DAC output. The nominal 0 to +10V unipolar input range now becomes a −5V to +5V range. The 5kΩ thin-film input resistor is trimmed so that with a full-scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

POWER SUPPLY SELECTION

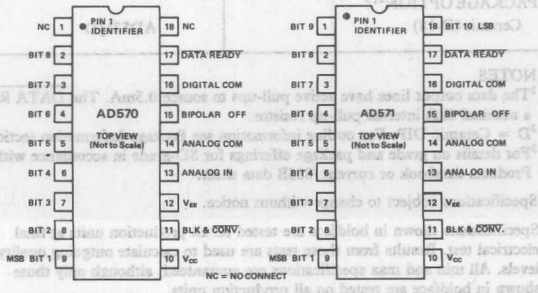
The AD570/AD571 are designed for optimum performance using a +5V and −15V supply, for which the J and S grades are specified. AD571K will also operate with up to a +15V supply, which allows direct interface to CMOS logic.



AD570/AD571 Functional Block Diagram

CONNECTING THE AD570/AD571 FOR STANDARD OPERATION

The AD570/AD571 contain all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and −15), the analog input, and the conversion start pulse. The functional pin outs are shown below.



AD570 Pin Connections *AD571 Pin Connections*

ANALOG DEVICES

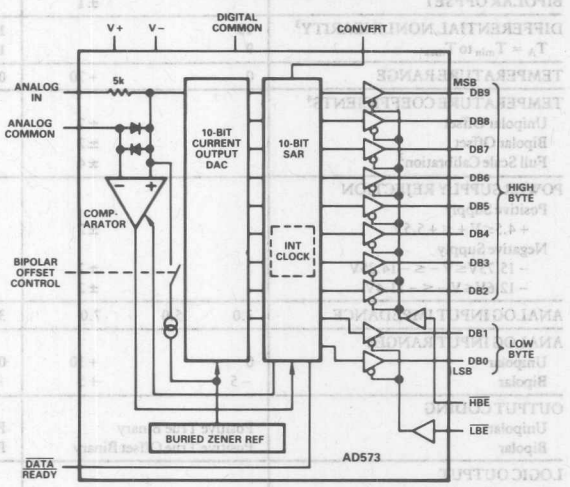
10-Bit A/D Converter

AD573*

FEATURES

- **Complete 10-Bit A/D Converter with Reference, Clock and Comparator**
- **Full 8- or 16-Bit Microprocessor Bus Interface**
- **Fast Successive Approximation Conversion – 20μs typ**
- **No Missing Codes Over Temperature**
- **Operates on +5V and −12V to −15V Supplies**
- **Low Cost Monolithic Construction**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD573 is a complete 10-bit successive approximation analog to digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and 3 state output buffers–all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 20μs.

The AD573 incorporates advanced integrated circuit design and processing technologies. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin film resistor ladder network insures high accuracy, which is maintained with a temperature compensated sub-surface Zener reference.

Operating on supplies of +5V and −12V to −15V, the AD573 will accept analog inputs of 0 to +10V or −5V to +5V. The trailing edge of a positive pulse on the CONVERT line initiates the 20μs conversion cycle. DATA READY indicates completion of the conversion. HIGH BYTE ENABLE (HBE) and LOW BYTE ENABLE (LBE) control the 8-bit and 2-bit three state output buffers.

The AD573 is available in two versions for the 0 to +70°C temperature range, the AD573J and AD573K. The AD573S guarantees ±1LSB relative accuracy and no missing codes from −55°C to +125°C.

Three package configurations are offered. All versions are offered in a 20-pin hermetically sealed ceramic DIP. The AD573J and AD573K are also available in a 20-pin plastic DIP or 20-pin leaded chip carrier.

PRODUCT HIGHLIGHTS

1. The AD573 is a complete 10-bit A/D converter. No external components are required to perform a conversion.
2. The AD573 interfaces to many popular microprocessors without external buffers or peripheral interface adapters. The 10 bits of output data can be read as a 10-bit word or as 8- and 2-bit words.
3. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD573 adapts to either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.
6. The AD573 is available in a version compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current /883B datasheet for detailed specifications.

***Protected by U.S. Patent Nos. 3,940,760; 4,213,806; 4,136,349; 4,400,689; and 4,400,690**

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD573—SPECIFICATIONS (T_A = 25V, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated.)

Model	AD573J Min	AD573J Typ	AD573J Max	AD573K Min	AD573K Typ	AD573K Max	AD573S Min	AD573S Typ	AD573S Max	Units
RESOLUTION		10			10			10		Bits
RELATIVE ACCURACY[1]			±1			±1/2			±1	LSB
$T_A = T_{min}$ to T_{max}			±1			±1/2			±1	LSB
FULL SCALE CALIBRATION[2]		±2			±2				±2	LSB
UNIPOLAR OFFSET			±1			±1/2			±1	LSB
BIPOLAR OFFSET			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY[3]	**10**			**10**			**10**			Bits
$T_A = T_{min}$ to T_{max}	**9**			**10**			**10**			Bits
TEMPERATURE RANGE	0		+70	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS[4]										
Unipolar Offset			±2			±1			±2	LSB
Bipolar Offset			±2			±1			±2	LSB
Full Scale Calibration[2]			±4			±2			±5	LSB
POWER SUPPLY REJECTION										
Positive Supply										
+4.5≤V+≤+5.5V			±2			±1			±2	LSB
Negative Supply										
−15.75V≤V−≤−14.25V			±2			±1			±2	LSB
−12.6V≤V−≤−11.4V			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	−5		+5	V
OUTPUT CODING										
Unipolar	Positive True Binary			Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT										
Output Sink Current										
(V_{OUT} = 0.4V max, T_{min} to T_{max})	**3.2**			**3.2**			**3.2**			mA
Output Source Current[5]										
(V_{OUT} = 2.4V min, T_{min} to T_{max})	**0.5**			**0.5**			**0.5**			mA
Output Leakage			±40			±40			±40	μA
LOGIC INPUTS										
Input Current			±100			±100			±100	μA
Logic "1"	**2.0**			**2.0**			**2.0**			V
Logic "0"			**0.8**			**0.8**			**0.8**	V
CONVERSION TIME										
$T_A = T_{min}$ to T_{max}	**10**	20	**30**	**10**	20	**30**	**10**	20	**30**	μs
POWER SUPPLY										
V+	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	V
V−	**−11.4**	−15	**−16.5**	**+11.4**	−15	**−16.5**	**−11.4**	−15	**−16.5**	V
OPERATING CURRENT										
V+		15	**20**		15	**20**		15	**20**	mA
V−		9	**15**		9	**15**		9	**15**	mA

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full-scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

[3]Defined as the resolution for which no missing codes will occur.

[4]Change from +25°C value from +25°C to T_{min} or T_{max}.

[5]The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V− to Digital Common	0 to −16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (High Impedance State)	0 to V+
Power Dissipation	800mW

ORDERING GUIDE[1]

Model	Package Option[2]	Temperature Range	Relative Accuracy
AD573JN	20-Pin Plastic DIP (N-20)	0 to +70°C	±1LSB max
AD573KN	20-Pin Plastic DIP (N-20)	0 to +70°C	±1/2LSB max
AD573JP	20-Pin Leaded Chip Carrier (P-20A)	0 to +70°C	±1LSB max
AD573KP	20-Pin Leaded Chip Carrier (P-20A)	0 to +70°C	±1/2LSB max
AD573JD	20-Pin Ceramic DIP (D-20)	0 to +70°C	±1LSB max
AD573KD	20-Pin Ceramic DIP (D-20)	0 to +70°C	±1/2LSB max
AD573SD	20-Pin Ceramic DIP (D-20)	−55°C to +125°C	±1LSB max

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices Military Products Databook.
[2]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

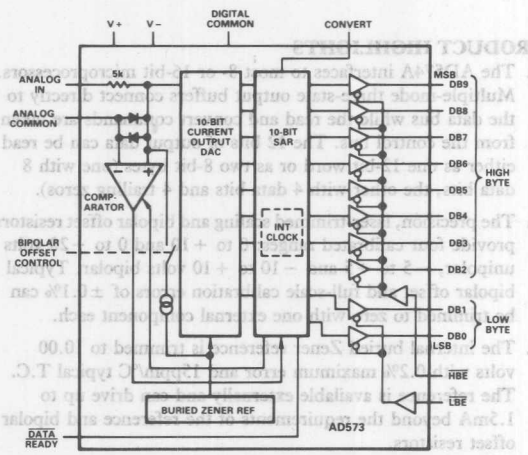


Figure 1. AD573 Functional Block Diagram

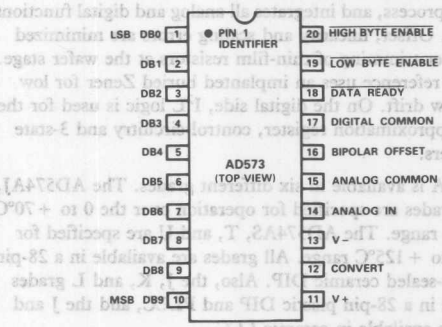
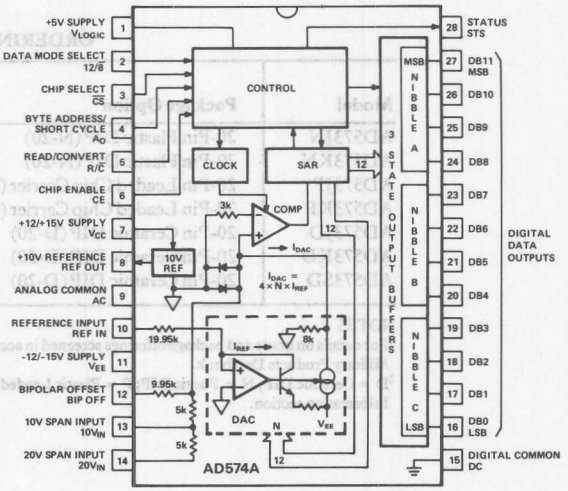


Figure 2. AD573 Pin Connections

FEATURES

- Complete 12-Bit A/D Converter with Reference and Clock
- 8- and 16-Bit Microprocessor Bus Interface
- Guaranteed Linearity Over Temperature
  - 0 to +70°C – AD574AJ, K, L
  - −55°C to +125°C – AD574AS, T, U
- No Missing Codes Over Temperature
- 35µs Maximum Conversion Time
- Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10ppm/°C max AD574AL, 12.5ppm/°C max AD574AU
- Ceramic DIP, Plastic DIP or PLCC Package
- Available in Higher Speed, Pinout-Compatible Versions (15µs AD674B, 8µs AD774B; 10µs (with SHA) AD1674)
- Available in Versions Compliant with MIL-STD-883 and JAN QPL.

BLOCK DIAGRAM AND PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8- or 16-bit microprocessor bus. A high-precision voltage reference and clock are included on-chip, and the circuit guarantees full-rated performance without external circuitry or clock signals.

The AD574A design is implemented using Analog Devices' Bipolar/I^2L process, and integrates all analog and digital functions on one chip. Offset, linearity and scaling errors are minimized by active laser-trimming of thin-film resistors at the wafer stage. The voltage reference uses an implanted buried Zener for low noise and low drift. On the digital side, I^2L logic is used for the successive-approximation register, control circuitry and 3-state output buffers.

The AD574A is available in six different grades. The AD574AJ, K, and L grades are specified for operation over the 0 to +70°C temperature range. The AD574AS, T, and U are specified for the −55°C to +125°C range. All grades are available in a 28-pin hermetically-sealed ceramic DIP. Also, the J, K, and L grades are available in a 28-pin plastic DIP and PLCC, and the J and K grades are available in ceramic LCC.

The S, T, and U grades in ceramic DIP or LCC are available with optional processing to MIL-STD-883C Class B; the T and U grades are available as JAN QPL. The Analog Devices' Military Products Databook should be consulted for details on /883B testing of the AD574A.

PRODUCT HIGHLIGHTS

1. The AD574A interfaces to most 8- or 16-bit microprocessors. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 and 0 to +20 volts unipolar, −5 to +5 and −10 to +10 volts bipolar. Typical bipolar offset and full-scale calibration errors of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried Zener reference is trimmed to 10.00 volts with 0.2% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 1.5mA beyond the requirements of the reference and bipolar offset resistors.
4. AD674B (15µs) and AD774B (8µs) provide higher speed, pin compatibility; AD1674 (10µs) includes on-chip Sample-Hold Amplifier (SHA).

*Protected by U.S. Patent Nos. 3,803,590; 4,213,806; 4,511,413; RE 28,633.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise noted)

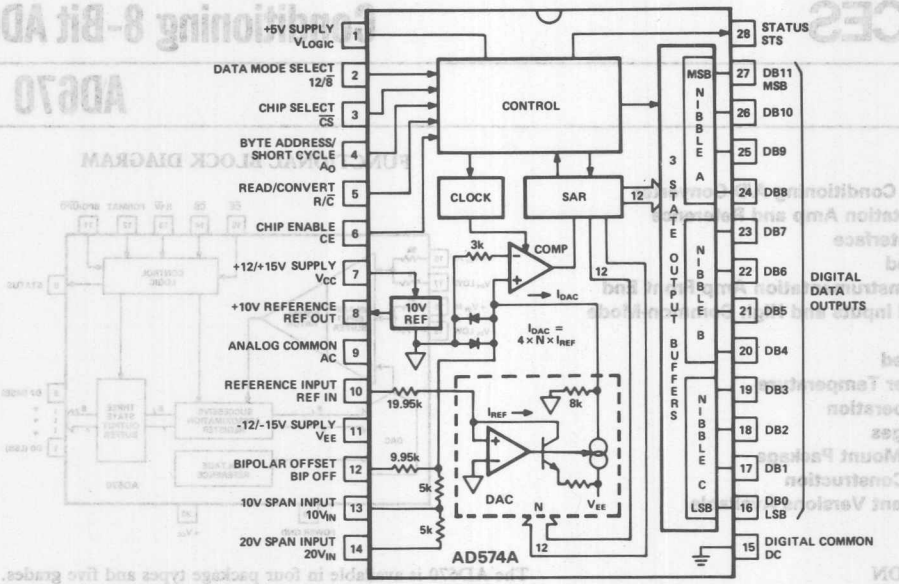
T_{min} to T_{max}			±1			±1/2			±1/2	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed) T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to zero)			±2			±1			±1	LSB
BIPOLAR OFFSET (Adjustable to zero)			±4			±4			±2	LSB
FULL-SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero)			0.25			0.25			0.125	% of F.S.
TEMPERATURE RANGE	0		+70	0		+70	0		+70	°C
TEMPERATURE COEFFICIENTS (Using internal reference) T_{min} to T_{max}										
Unipolar Offset			±2(10)			±1(5)			±1(5)	LSB (ppm/°C)
Bipolar Offset			±2(10)			±1(5)			±1(5)	LSB (ppm/°C)
Full-Scale Calibration			±9(50)			±5(27)			±2(10)	LSB (ppm/°C)
POWER SUPPLY REJECTION Max change in Full Scale Calibration										
V_{CC} = 15V ±1.5V or 12V ±0.6V			±2			±1			±1	LSB
V_{LOGIC} = 5V ±0.5V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15V ±1.5V or −12V ±0.6V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS[1] (T_{min}–T_{max})										
Inputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0)										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−20		+20	−20		+20	−20		+20	µA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage (I_{SOURCE}≤500µA)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage (I_{SINK}≤1.6mA)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	µA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.98	10.0	10.02	9.98	10.0	10.02	9.99	10.0	10.01	Volts
Output current (available for external loads)[3] (External load should not change during conversion)			1.5			1.5			1.5	mA
PACKAGE OPTIONS[4]										
Ceramic (D-28)		AD574ASD			AD574AKD			AD574ALD		
Plastic (N-28)		AD574AJN			AD574AKN			AD574ALN		
PLCC (P-28A)		AD574AJP			AD574AKP			AD574ALP		
LCC (E-28A)		AD574AJE			AD574AKE					

NOTES
[1]Detailed Timing Specifications appear in the Timing Section.
[2]12/$\overline{8}$ Input is not TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.
[3]The reference should be buffered for operation on ±12V supplies.
[4]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

Specifications subject to change without notice.

Model	AD574AS Min	AD574AS Typ	AD574AS Max	AD574AT Min	AD574AT Typ	AD574AT Max	AD574AU Min	AD574AU Typ	AD574AU Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR @ +25°C			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1			±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)										
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to zero)			±2			±1			±1	LSB
BIPOLAR OFFSET (Adjustable to zero)			±4			±4			±2	LSB
FULL-SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero)			0.25			0.25			0.125	% of F.S.
TEMPERATURE RANGE	−55		+125	−55		+125	−55		+125	°C
TEMPERATURE COEFFICIENTS (Using internal reference)										
T_{min} to T_{max}										
Unipolar Offset			±2 (5)			±1 (2.5)			±1 (2.5)	LSB (ppm/°C)
Bipolar Offset			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full-Scale Calibration			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
POWER SUPPLY REJECTION										
Max change in Full Scale Calibration										
V_{CC} = 15V ±1.5V or 12V ±0.6V			±2			±1			±1	LSB
V_{LOGIC} = 5V ±0.5V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15V ±1.5V or −12V ±0.6V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS[1] (T_{min}–T_{max})										
Inputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0)										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage (I_{SOURCE}≤500μA)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage (I_{SINK}≤1.6mA)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.98	10.0	10.02	9.98	10.0	10.02	9.99	10.0	10.01	Volts
Output current (available for external loads)[3]			1.5			1.5			1.5	mA
(External load should not change during conversion)										
PACKAGE OPTIONS[4]										
Ceramic (D-28)		AD574ASD			AD574ATD			AD574AUD		

NOTES
[1]Detailed Timing Specifications appear in the Timing Section.
[2]12/8 Input is not TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.
[3]The reference should be buffered for operation on ±12V supplies.
[4]D = Ceramic DIP. For outline information see Package Information section.
Specifications subject to change without notice.



AD574A Block Diagram and Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common . . . . . 0 to +16.5V
V_{EE} to Digital Common . . . . . 0 to −16.5V
V_{LOGIC} to Digital Common . . . . . 0 to +7V
Analog Common to Digital Common . . . . . ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common . . . −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to
Analog Common . . . . . V_{EE} to V_{CC}
$20V_{IN}$ to Analog Common . . . . . ±24V
REF OUT . . . . . Indefinite short to common
Momentary short to V_{CC}

Chip Temperature . . . . . 175°C
Power Dissipation 825mW
Lead Temperature, Soldering . . . . . +300°C, 10 sec.
Storage Temperature (Ceramic) . . . . . −65°C to +150°C
(Plastic) . . . . . −25°C to +100°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

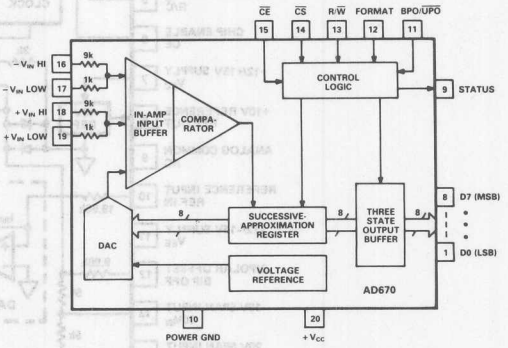
Model[1]	Temperature Range	Linearity Error Max (T_{min} to T_{max})	Resolution No Missing Codes (T_{min} to T_{max})	Max Full Scale T.C. (ppm/°C)
AD574AJ(X)	0 to +70°C	±1LSB	11 Bits	50.0
AD574AK(X)	0 to +70°C	±1/2LSB	12 Bits	27.0
AD574AL(X)	0 to +70°C	±1/2LSB	12 Bits	10.0
AD574AS(X)[2]	−55°C to +125°C	±1LSB	11 Bits	50.0
AD574AT(X)[2]	−55°C to +125°C	±1LSB	12 Bits	25.0
AD574AU(X)[2]	−55°C to +125°C	±1LSB	12 Bits	12.5

NOTES
[1]X = Package designator. Available packages are:
D (D-28) for all grades.
E (E-28A) for J and K grades and /883B processed S, T and U grades.
N (N-28) for J, K, and L grades.
P (P-28A)for PLCC in J, K grades.
Example: AD574AKN is K grade in plastic DIP.
[2]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices Military Products Databook.

FEATURES

- Complete 8-Bit Signal Conditioning A/D Converter Including Instrumentation Amp and Reference
- Microprocessor Bus Interface
- 10μs Conversion Speed
- Flexible Input Stage: Instrumentation Amp Front End Provides Differential Inputs and High Common-Mode Rejection
- No User Trims Required
- No Missing Codes Over Temperature
- Single +5V Supply Operation
- Convenient Input Ranges
- 20-Pin DIP or Surface-Mount Package
- Low Cost Monolithic Construction
- MIL-STD-883B Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD670 is a complete 8-bit signal conditioning analog-to-digital converter. It consists of an instrumentation amplifier front end along with a DAC, comparator, successive approximation register (SAR), precision voltage reference, and a three-state output buffer on a single monolithic chip. No external components or user trims are required to interface, with full accuracy, an analog system to an 8-bit data bus. The AD670 will operate on the +5V system supply. The input stage provides differential inputs with excellent common-mode rejection and allows direct interface to a variety of transducers.

The device is configured with input scaling resistors to permit two input ranges: 0 to 255mV (1mV/LSB) and 0 to 2.55V (10mV/LSB). The AD670 can be configured for both unipolar and bipolar inputs over these ranges. The differential inputs and common-mode rejection of this front end are useful in applications such as conversion of transducer signals superimposed on common-mode voltages.

The AD670 incorporates advanced circuit design and proven processing technology. The successive approximation function is implemented with I^2L (integrated injection logic). Thin-film SiCr resistors provide the stability required to prevent missing codes over the entire operating temperature range while laser wafer trimming of the resistor ladder permits calibration of the device to within ±1LSB. Thus, no user trims for gain or offset are required. Conversion time of the device is 10μs.

The AD670 is available in four package types and five grades. The J and K grades are specified over 0 to +70°C and come in 20-pin plastic DIP packages or 20-terminal PLCC packages. The A and B grades (−40°C to +85°C) and the S grade (−55°C to +125°C) come in 20-pin ceramic DIP packages.

The S grade is also available with optional processing to MIL-STD-883 in 20-pin ceramic DIP or 20-terminal LCC packages. The Analog Devices Military Products Databook should be consulted for detailed specifications.

PRODUCT HIGHLIGHTS

1. The AD670 is a complete 8-bit A/D including three-state outputs and microprocessor control for direct connection to 8-bit data buses. No external components are required to perform a conversion.
2. The flexible input stage features a differential instrumentation amp input with excellent common-mode rejection. This allows direct interface to a variety of transducers without preamplification.
3. No user trims are required for 8-bit accurate performance.
4. Operation from a single +5V supply allows the AD670 to run off of the microprocessor's supply.
5. Four convenient input ranges (two unipolar and two bipolar) are available through internal scaling resistors: 0 to 255mV (1mV/LSB) and 0 to 2.55V (10mV/LSB).
6. Software control of the output mode is provided. The user can easily select unipolar or bipolar inputs and binary or 2's complement output codes.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

RESOLUTION	8		8		Bit
CONVERSION TIME		**10**		**10**	µs
RELATIVE ACCURACY		**±1/2**		**±1/4**	LSB
T_{min} to T_{max}		**±1/2**		**±1/2**	LSB
DIFFERENTIAL LINEARITY ERROR[1]					
T_{min} to T_{max}	**GUARANTEED NO MISSING CODES ALL GRADES**				
GAIN ACCURACY					
@ +25°C		**±1.5**		**±0.75**	LSB
T_{min} to T_{max}		**±2.0**		**±1.0**	LSB
UNIPOLAR ZERO ERROR					
@ +25°C		**±1.5**		**±0.75**	LSB
T_{min} to T_{max}		**±2.0**		**±1.0**	LSB
BIPOLAR ZERO ERROR					
@ +25°C		**±1.5**		**±0.75**	LSB
T_{min} to T_{max}		**±2.0**		**±1.0**	LSB
ANALOG INPUT RANGES					
DIFFERENTIAL ($-V_{IN}$ to $+V_{IN}$)					
Low Range	0 to +255		0 to +255		mV
	−128 to +127		−128 to +127		mV
High Range	0 to +2.55		0 to +2.55		V
	−1.28 to +1.27		−1.28 to +1.27		V
ABSOLUTE (Inputs to Power Gnd)					
Low Range T_{min} to T_{max}	**−0.150**	**V_{CC} −3.4**	**−0.150**	**V_{CC} −3.4**	V
High Range T_{min} to T_{max}	−1.50	V_{CC}	−1.50	V_{CC}	V
BIAS CURRENT (255mV RANGE)					
T_{min} to T_{max}	200	**500**	200	**500**	nA
OFFSET CURRENT (255mV RANGE)					
T_{min} to T_{max}	40	**200**	40	**200**	nA
2.55V RANGE INPUT RESISTANCE	**8.0**	**12.0**	**8.0**	**12.0**	kΩ
2.55V RANGE FULL SCALE MATCH					
+ AND − INPUT	±1/2		±1/2		LSB
COMMON-MODE REJECTION					
RATIO (255mV RANGE)		**1**		**1**	LSB
COMMON-MODE REJECTION					
RATIO (2.55V RANGE)		1		1	LSB
POWER SUPPLY					
Operating Range	**4.5**	**5.5**	**4.5**	**5.5**	V
Current I_{CC}	30	**45**	30	**45**	mA
Rejection Ratio T_{min} to T_{max}		**0.015**		**0.015**	% of FS/%
DIGITAL OUTPUTS					
SINK CURRENT (V_{OUT} = 0.4V)					
T_{min} to T_{max}	**1.6**		**1.6**		mA
SOURCE CURRENT (V_{OUT} = 2.4V)					
T_{min} to T_{max}	**0.5**		**0.5**		mA
THREE-STATE LEAKAGE CURRENT		**±40**		**±40**	µA
OUTPUT CAPACITANCE	5		5		pF
DIGITAL INPUT VOLTAGE					
V_{INL}		**0.8**		**0.8**	V
V_{INH}	**2.0**		**2.0**		V
DIGITAL INPUT CURRENT					
(0≤V_{IN}≤+5V)					
I_{INL}	**−100**		**−100**		µA
I_{INH}		**+100**		**+100**	µA
INPUT CAPACITANCE	10		10		pF

NOTES
[1]Tested at V_{CC} = 4.5V, 5.0V and 5.5V.
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.
Specifications subject to change without notice.

Model	AD670A Min	AD670A Typ	AD670A Max	AD670B Min	AD670B Typ	AD670B Max	AD670S Min	AD670S Typ	AD670S Max	Units
OPERATING TEMPERATURE RANGE	−40		+85	−40		+85	−55		+125	°C
RESOLUTION	8			8			8			Bit
CONVERSION TIME			10			10			10	µs
RELATIVE ACCURACY			±1/2			±1/4			±1/2	LSB
T_{min} to T_{max}			±1/2			±1/2			±1	LSB
DIFFERENTIAL LINEARITY ERROR[1]										
T_{min} to T_{max}			GUARANTEED NO MISSING CODES ALL GRADES							
GAIN ACCURACY										
@ +25°C			±1.5			±0.75			±1.5	LSB
T_{min} to T_{max}			±2.5			±1.5			±2.5	LSB
UNIPOLAR ZERO ERROR										
@ +25°C			±1.0			±0.5			±1.0	LSB
T_{min} to T_{max}			±2.0			±1.0			±2.0	LSB
BIPOLAR ZERO ERROR										
@ +25°C			±1.0			±0.5			±1.0	LSB
T_{min} to T_{max}			±2.0			±1.0			±2.0	LSB
ANALOG INPUT RANGES										
DIFFERENTIAL ($-V_{IN}$ to $+V_{IN}$)										
Low Range		0 to +255			0 to +255			0 to +255		mV
		−128 to +127			−128 to +127			−128 to +127		mV
High Range		0 to +2.55			0 to +2.55			0 to +2.55		V
		−1.28 to +1.27			−1.28 to +1.27			−1.28 to +1.27		V
ABSOLUTE (Inputs to Power Gnd)										
Low Range T_{min} to T_{max}	−0.150		V_{CC} −3.5	−0.150		V_{CC} −3.5	−0.150		V_{CC} −3.5	V
High Range T_{min} to T_{max}	−1.50		V_{CC}	−1.50		V_{CC}	−1.50		V_{CC}	V
BIAS CURRENT (255mV RANGE)										
T_{min} to T_{max}		200	500		200	500		200	750	nA
OFFSET CURRENT (255mV RANGE)										
T_{min} to T_{max}		40	200		40	200		40	200	nA
2.55V RANGE INPUT RESISTANCE	8.0		12.0	8.0		12.0	8.0		12.0	kΩ
2.55V RANGE FULL SCALE MATCH + AND − INPUT		±1/2			±1/2			±1/2		LSB
COMMON-MODE REJECTION RATIO (255mV RANGE)			1			1			1	LSB
COMMON-MODE REJECTION RATIO (2.55V RANGE)			1			1			1	LSB
POWER SUPPLY										
Operating Range	4.5		5.5	4.5		5.5	4.75		5.5	V
Current I_{CC}		30	45		30	45		30	45	mA
Rejection Ratio T_{min} to T_{max}			0.015			0.015			0.015	% of FS/%
DIGITAL OUTPUTS										
SINK CURRENT (V_{OUT} = 0.4V)										
T_{min} to T_{max}	1.6			1.6			1.6			mA
SOURCE CURRENT (V_{OUT} = 2.4V)										
T_{min} to T_{max}	0.5			0.5			0.5			mA
THREE-STATE LEAKAGE CURRENT			±40			±40			±40	µA
OUTPUT CAPACITANCE		5			5			5		pF
DIGITAL INPUT VOLTAGE										
V_{INL}			0.8			0.8			0.7	V
V_{INH}	2.0			2.0			2.0			V
DIGITAL INPUT CURRENT ($0 \le V_{IN} \le +5V$)										
I_{INL}	−100			−100			−100			µA
I_{INH}			+100			+100			+100	µA
INPUT CAPACITANCE		10			10			10		pF

NOTES

[1]Tested at V_{CC} = 4.5V, 5.0V and 5.5V for A, B grades; 4.75V, 5.0V and 5.5V for S grade.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

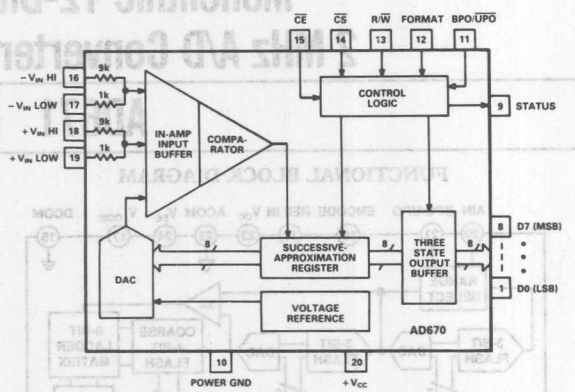


Figure 1. AD670 Block Diagram and Terminal Configuration (All Packages)

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Ground . . . . . 0V to +7.5V
Digital Inputs (Pins 11-15) . . . . . −0.5V to V_{CC} +0.5V
Digital Outputs (Pins 1-9) . Momentary Short to V_{CC} or Ground
Analog Inputs (Pins 16-19) . . . . . −30V to +30V
Power Dissipation 450mW
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

ORDERING GUIDE

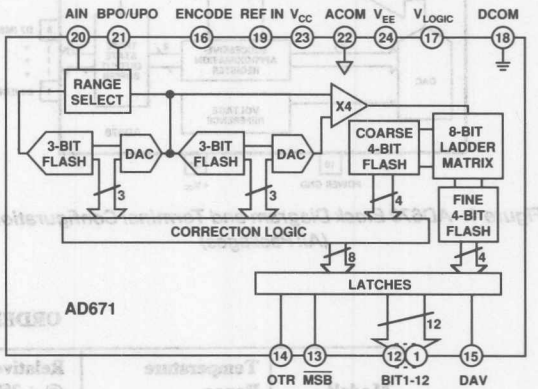
Model[1]	Temperature Range	Relative Accuracy @ +25°C	Gain Accuracy @ +25°C	Package Option[2]
AD670JN	0 to +70°C	±1/2LSB	±1.5LSB	Plastic DIP (N-20)
AD670JP	0 to +70°C	±1/2LSB	±1.5LSB	PLCC (P-20A)
AD670KN	0 to +70°C	±1/4LSB	±0.75LSB	Plastic DIP (N-20)
AD670KP	0 to +70°C	±1/4LSB	±0.75LSB	PLCC (P-20A)
AD670AD	−40°C to +85°C	±1/2LSB	±1.5LSB	Ceramic DIP (D-20)
AD670BD	−40°C to +85°C	±1/4LSB	±0.75LSB	Ceramic DIP (D-20)
AD670SD	−55°C to +125°C	±1/2LSB	±1.5LSB	Ceramic DIP (D-20)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883 refer to the Analog Devices Military Products Databook.
[2]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

AD671

FEATURES
12-Bit Resolution
24-Pin "Skinny DIP" Package
Conversion Time: 500 ns max – AD671J/K/S-500
750 ns max – AD671J/K/S-750
Low Power: 475 mW
Unipolar (0 to +5 V, 0 to +10 V) and Bipolar Input Ranges (±5 V)
Twos Complement or Offset Binary Output Data
Out of Range Indicator
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD671 is a high speed monolithic 12-bit A/D converter offering conversion rates of up to 2 MHz (500 ns conversion time). The combination of a merged high speed bipolar/CMOS process and a novel architecture results in a combination of speed and power consumption far superior to previously available hybrid implementations. Additionally, the greater reliability of monolithic construction offers improved system reliability and lower costs than hybrid designs.

The AD671 uses a subranging flash conversion technique, with digital error correction for possible errors introduced in the first part of the conversion cycle. An on-chip timing generator provides strobe pulses for each of the four internal flash cycles and assures adequate settling time for the interflash residue amplifier. A single ENCODE pulse is used to control the converter.

The performance of the AD671 is made possible by using high speed, low noise bipolar circuitry in the linear sections and low power CMOS for the logic sections. Analog Devices' ABCMOS-1 process provides both high speed bipolar and 2-micron CMOS devices on a single chip. Laser trimmed thin-film resistors are used to provide accuracy and temperature stability.

The AD671 is available in two conversion speeds and performance grades. The AD671J and K grades are specified for operation over the 0 to +70°C temperature range. The AD671S grades are specified for operation over the −55°C to +125°C temperature range. All grades are available in a 0.300 inch wide 24-pin ceramic DIP. The J and K grades are also available in a 24-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. The AD671 offers a single chip 2 MHz analog-to-digital conversion function in a space saving 24-pin DIP.
2. Input signal ranges are 0 to +5 V and 0 to +10 V unipolar, and −5 V to +5 V bipolar, selected by pin strapping. Input resistance is 1.5 kΩ. Power supplies are +5 V and −5 V, and typical power consumption is less than 500 mW.
3. The external +5 V reference can be chosen to suit the dc accuracy and temperature drift requirements of the application.
4. Output data is available in unipolar, bipolar offset or bipolar twos complement binary format.
5. An OUT OF RANGE output bit indicates when the input signal is beyond the AD671's input range.
6. The AD671 is available in versions compliant with the MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD671/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%, V_{REF} = +5.000 V, unless otherwise indicated)

Parameter	AD671J/S-500 Min	AD671J/S-500 Typ	AD671J/S-500 Max	AD671K-500 Min	AD671K-500 Typ	AD671K-500 Max	Units
RESOLUTION	12			12			Bits
ACCURACY (+25°C)							
Integral Nonlinearity (INL)							
T_{MIN} to T_{MAX}			±4			±2	LSB
Differential Nonlinearity (DNL)							
T_{MIN} to T_{MAX}	10			11			Bits
No Missing Codes		10 Bits Guaranteed			11 Bits Guaranteed		
Unipolar Offset[1]			±4			±4	LSB
Bipolar Zero[1]			±10			±10	LSB
Gain Error[2]		0.1	0.25		0.1	0.25	% FSR
TEMPERATURE COEFFICIENTS[3]							
Unipolar Offset			±10			±10	ppm/°C
Bipolar Zero			±15			±15	ppm/°C
Gain Error			±20			±20	ppm/°C
ANALOG INPUT							
Input Ranges							
Bipolar	−5		+5	−5		+5	Volts
Unipolar	0		+5	0		+5	Volts
	0		+10	0		+10	Volts
Input Resistance							
10 Volt Range	1.0	1.5	2.0	1.0	1.5	2.0	kΩ
5 Volt Range	0.5	0.75	1.0	0.5	0.75	1.0	kΩ
Input Capacitance		10			10		pF
Reference Input Resistance	2.4	3.5	4.7	2.4	3.5	4.7	kΩ
POWER SUPPLIES							
Power Supply Rejection[4]							
V_{CC} (+5 V ± 0.25 V)			±1			±1	LSB
V_{LOGIC} (+5 V ± 0.5 V)			±1			±1	LSB
V_{EE} (−5 V ± 0.25 V)			±1			±1	LSB
Operating Voltages							
V_{CC}	+4.75		+5.25	+4.75		+5.25	Volts
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	Volts
V_{EE}	−5.25		−4.75	−5.25		−4.75	Volts
Operating Current							
I_{CC}		46	56		46	56	mA
I_{LOGIC}[5]		3	6		3	6	mA
I_{EE}		46	56		46	56	mA
POWER CONSUMPTION		475	621		475	621	mW
TEMPERATURE RANGE							
Specified (J/K)	0		+70	0		+70	°C
(S)	−55		+125				°C

NOTES

[1]Adjustable to zero with external potentiometers. See Offset/Gain Calibration section for additional information.

[2]Full-scale range (FSR) is 5 V for the 0 V to 5 V range and 10 V for the 0 V to 10 V and −5 V to +5 V ranges.

[3]25°C to T_{MIN} and 25°C to T_{MAX}.

[4]Change in gain error as a function of the dc supply voltage.

[5]Tested under static conditions.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

AD671—SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5 %, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%, V_{REF} = +5.000 V, unless otherwise indicated)

Parameter	AD671J/S-750 Min	AD671J/S-750 Typ	AD671J/S-750 Max	AD671K-750 Min	AD671K-750 Typ	AD671K-750 Max	Units
RESOLUTION	12			12			Bits
ACCURACY (+25°C)							
Integral Nonlinearity (INL)							
T_{MIN} to T_{MAX} (J)			±2			±1.5	LSB
T_{MIN} to T_{MAX} (S)			±2.5				LSB
Differential Nonlinearity (DNL)							
T_{MIN} to T_{MAX}	11			12			Bits
No Missing Codes		11 Bits Guaranteed			12 Bits Guaranteed		
Unipolar Offset[1]			±4			±4	LSB
Bipolar Zero[1]			±10			±10	LSB
Gain Error[2]		0.1	0.25		0.1	0.25	% FSR
TEMPERATURE COEFFICIENTS[3]							
Unipolar Offset			±10			±10	ppm/°C
Bipolar Zero			±15			±15	ppm/°C
Gain Error			±20			±20	ppm/°C
ANALOG INPUT							
Input Ranges							
Bipolar	−5		+5	−5		+5	Volts
Unipolar	0		+5	0		+5	Volts
	0		+10	0		+10	Volts
Input Resistance							
10 Volt Range	1.0	1.5	2.0	1.0	1.5	2.0	kΩ
5 Volt Range	0.5	0.75	1.0	0.5	0.75	1.0	kΩ
Input Capacitance		10			10		pF
Reference Input Resistance	2.4	3.5	4.7	2.4	3.5	4.7	kΩ
POWER SUPPLIES							
Power Supply Rejection[4]							
V_{CC} (+5 V ± 0.25 V)			±1			±1	LSB
V_{LOGIC} (+5 V ± 0.5 V)			±1			±1	LSB
V_{EE} (−5 V ± 0.25 V)			±1			±1	LSB
Operating Voltages							
V_{CC}	+4.75		+5.25	+4.75		+5.25	Volts
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	Volts
V_{EE}	−5.25		−4.75	−5.25		−4.75	Volts
Operating Current							
I_{CC}		46	56		46	56	mA
I_{LOGIC}[5]		3	6		3	6	mA
I_{EE}		46	56		46	56	mA
POWER CONSUMPTION		475	621		475	621	mW
TEMPERATURE RANGE							
Specified (J/K)	0		+70	0		+70	°C
(S)	−55		+125				°C

NOTES

[1]Adjustable to zero with external potentiometers. See Offset/Gain Calibration section for further information.

[2]Full-scale range (FSR) is 5 V for the 0 V to 5 V range and 10 V for the 0 V to 10 V and −5 V to +5 V ranges.

[3]25°C to T_{MIN} and 25°C to T_{MAX}.

[4]Change in gain error as a function of the dc supply voltage.

[5]Tested under static conditions.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested.

DIGITAL SPECIFICATIONS

(For all grades T_{MIN} to T_{MAX}, with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%, V_{REF} = +5.000 V, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUT					
High Level Input Voltage	V_{IH}	+2.0			V
Low Level Input Voltage	V_{IL}			+0.8	V
High Level Input Current (V_{IN} = V_{LOGIC})	I_{IH}	−10		+10	μA
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	−10		+10	μA
Input Capacitance	C_{IN}		5		pF
LOGIC OUTPUTS					
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	+2.4			V
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}			+0.4	V
Output Capacitance	C_{OUT}		5		pF

Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS

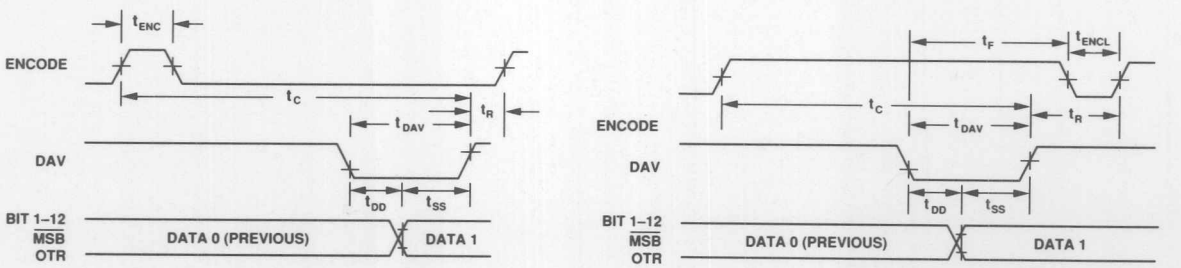
(For all grades T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%; V_{IL} = 0.8 V, V_{IH} = 2.0 V, V_{OL} = 0.4 V and V_{OH} = 2.4 V)

Parameter	Symbol	Min	Typ	Max	Units
Conversion Time					
(AD671-500)	t_C	475		500	ns
(AD671-750)	t_C	725		750	ns
ENCODE Pulse Width High					
(AD671-500)	t_{ENC}	20		30	ns
(AD671-750)	t_{ENC}	20		50	ns
ENCODE Pulse Width Low	t_{ENCL}	20			ns
DAV Pulse Width					
(AD671-500)	t_{DAV}	75		200	ns
(AD671-750)	t_{DAV}	75		300	ns
ENCODE Falling Edge Delay	t_F	0			ns
Start New Conversion Delay	t_R	0			ns
Data and OTR Delay from DAV Falling Edge	t_{DD} [1]	20	75		ns
Data and OTR Valid before DAV Rising Edge	t_{SS} [2]	20	75		ns

NOTES

[1] t_{DD} is measured from when the falling edge of DAV crosses 0.8 V to when the output crosses 0.4 V or 2.4 V with a 25 pF load capacitor on each output pin.

[2] t_{SS} is measured from when the outputs cross 0.4 V or 2.4 V to when the rising edge of DAV crosses 2.4 V with a 25 pF load capacitor on each output pin.



a. Encode Pulse HIGH

b. Encode Pulse LOW

Figure 1. AD671 Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
V_{CC}	ACOM	−0.5	+6.5	Volts
V_{EE}	ACOM	−6.5	+0.5	Volts
V_{LOGIC}	DCOM	−0.5	+6.5	Volts
ACOM	DCOM	−1.0	+1.0	Volts
V_{CC}	V_{LOGIC}	−6.5	+6.5	Volts
ENCODE	DCOM	−0.5	V_{LOGIC}+0.5	Volts
REF IN	ACOM	−0.5	V_{CC}+0.5	Volts
AIN, BPO/UPO	ACOM	−6.5	11.0	Volts
Junction Temperature			+175	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)		+300		°C
Power Dissipation			1000	mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model[1]	Linearity	Temperature Range	Package Options[2]
AD671JD-500	±4 LSB	0°C to +70°C	D-24A
AD671KD-500	±2 LSB	0°C to +70°C	D-24A
AD671JD-750	±2 LSB	0°C to +70°C	D-24A
AD671KD-750	±1.5 LSB	0°C to +70°C	D-24A
AD671SD-500	±4 LSB	−55°C to +125°C	D-24A
AD671SD-750	±2.5 LSB	−55°C to +125°C	D-24A

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD671/883 data sheet.
[2]D = Ceramic DIP. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ANALOG DEVICES

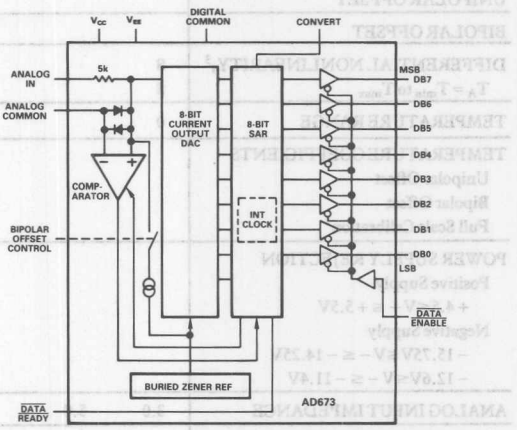
8-Bit A/D Converter

AD673*

FEATURES

Complete 8-Bit A/D Converter with Reference, Clock and Comparator
30μs Maximum Conversion Time
Full 8- or 16-Bit Microprocessor Bus Interface
Unipolar and Bipolar Inputs
No Missing Codes Over Temperature
Operates on +5V and −12V to −15V Supplies
MIL-STD-883 Compliant Version Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD673 is a complete 8-bit successive approximation analog-to-digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and 3 state output buffers–all fabricated on a single chip. No external components are required to perform a full accuracy 8-bit conversion in 20μs.

The AD673 incorporates advanced integrated circuit design and processing technologies. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin film resistor ladder network insures high accuracy, which is maintained with a temperature compensated sub-surface Zener reference.

Operating on supplies of +5V and −12V to −15V, the AD673 will accept analog inputs of 0 to +10V or −5V to +5V. The trailing edge of a positive pulse on the CONVERT line initiates the 20μs conversion cycle. $\overline{\text{DATA READY}}$ indicates completion of the conversion.

The AD673 is available in two versions. The AD673J as specified over the 0 to +70°C temperature range and the AD673S guarantees ±½LSB relative accuracy and no missing codes from −55°C to +125°C.

Two package configurations are offered. All versions are also offered in a 20-pin hermetically sealed ceramic DIP. The AD673J is also available in a 20-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. The AD673 is a complete 8-bit A/D converter. No external components are required to perform a conversion.
2. The AD673 interfaces to many popular microprocessors without external buffers or peripheral interface adapters.
3. The device offers true 8-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD673 adapts to either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.
6. The AD673 is available in a version compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD673/883B data sheet for detailed specifications.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option[1]
AD673JN	0 to +70°C	± 1/2LSB max	Plastic DIP (N-20)
AD673JD	0 to +70°C	± 1/2LSB max	Ceramic DIP (D-20)
AD673SD[2]	−55°C to +125°C	± 1/2LSB max	Ceramic DIP (D-20)
AD673JP	0 to +70°C	± 1/2LSB max	PLCC (P-20A)

NOTES
[1]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.
[2]For details on grade and package offering screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook.

*Protected by U.S. Patent Nos. 3,940,760; 4,213,806; 4,136,349; 4,400,689; and 4,400,690

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

RELATIVE ACCURACY,[1]			±1/2			±1/2	LSB
$T_A = T_{min}$ to T_{max}			±1/2			±1/2	LSB
FULL SCALE CALIBRATION[2]		±2			±2		LSB
UNIPOLAR OFFSET			±1/2			±1/2	LSB
BIPOLAR OFFSET			±1/2			±1/2	LSB
DIFFERENTIAL NONLINEARITY,[3]	8			8			Bits
$T_A = T_{min}$ to T_{max}	8			8			Bits
TEMPERATURE RANGE	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS							
Unipolar Offset			±1			±1	LSB
Bipolar Offset			±1			±1	LSB
Full Scale Calibration[2]			±2			±2	LSB
POWER SUPPLY REJECTION							
Positive Supply							
$+4.5 \le V+ \le +5.5V$			±2			±2	LSB
Negative Supply							
$-15.75V \le V- \le -14.25V$			±2			±2	LSB
$-12.6V \le V- \le -11.4V$			±2			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES							
Unipolar	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	V
OUTPUT CODING							
Unipolar	Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT							
Output Sink Current							
(V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2			3.2			mA
Output Source Current[4]							
(V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5			0.5			mA
Output Leakage			±40			±40	μA
LOGIC INPUTS							
Input Current			±100			±100	μA
Logic "1"	2.0			2.0			V
Logic "0"			0.8			0.8	V
CONVERSION TIME, T_A and							
T_{min} to T_{max}	10	20	30	10	20	30	μs
POWER SUPPLY							
V+	+4.5	+5.0	+7.0	+4.5	+5.0	+7.0	V
V−	−11.4	−15	−16.5	−11.4	−15	−16.5	V
OPERATING CURRENT							
V+		15	20		15	20	mA
V−		9	15		9	15	mA

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full scale calibration is guaranteed trimmable to zero with an external 200Ω potentiometer in place of the 15Ω fixed resistor.

Full scale is defined as 10 volts minus 1LSB, or 9.961 volts.

[3]Defined as the resolution for which no missing codes will occur.

[4]The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

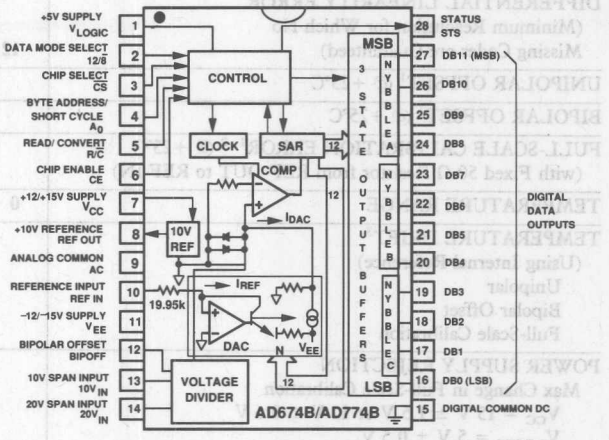
Complete 12-Bit A/D Converter

AD674B*/AD774B*

FEATURES

Complete Monolithic 12-Bit A/D Converters with Reference, Clock, and Three-State Output Buffers
Industry Standard Pinout
High Speed Upgrades for AD574A
8- and 16-Bit Microprocessor Interface
8 μs (max) Conversion Time (AD774B)
15 μs (max) Conversion Time (AD674B)
±5 V, ±10 V, 0–10 V, 0–20 V Input Ranges
Commercial, Industrial and Military Temperature Range Grades
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD674B and AD774B are complete 12-bit successive-approximation analog-to-digital converters with three-state output buffer circuitry for direct interface to 8- and 16-bit microprocessor busses. A high precision voltage reference and clock are included on chip, and the circuit requires only power supplies and control signals for operation.

The AD674B and AD774B are pin compatible with the industry-standard AD574A, but offer faster conversion time and bus-access speed than the AD574A and lower power consumption. The AD674B converts in 15 μs (maximum) and the AD774B converts in 8 μs (maximum).

The monolithic design is implemented using Analog Devices' BiMOS II process allowing high performance bipolar analog circuitry to be combined on the same die with digital CMOS logic. Offset, linearity and scaling errors are minimized by active laser-trimming of thin-film resistors.

Five different grades are available. The J and K grades are specified for operation over the 0°C to +70°C temperature range. The A and B grades are specified from −40°C to +85°C, the T grade is specified from −55°C to +125°C. The J and K grades are available in a 28-pin plastic DIP or 28-lead SOIC. All other grades are available in a 28-pin hermetically sealed ceramic DIP.

*Protected by U.S. Patent Nos. 4,250,445; 4,808,908; RE30586.

PRODUCT HIGHLIGHTS

1. Industry Standard Pinout: The AD674B and AD774B utilize the pinout established by the industry standard AD574A.
2. Analog Operation: The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 V and 0 to +20 V unipolar; −5 V to +5 V and −10 V to +10 V bipolar. The AD674B and AD774B operate on +5 V and ±12 V or ±15 V power supplies.
3. Flexible Digital Interface: On-chip multiple-mode three-state output buffers and interface logic allow direct connection to most microprocessors. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
4. The internal reference is trimmed to 10.00 volts with 1% maximum error and 10 ppm/°C typical temperature coefficient. The reference is available externally and can drive up to 2.0 mA beyond the requirements of the converter and bipolar offset resistors.
5. The AD674B and AD774B are available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD674B/AD774B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD674B/AD774B—SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −15 V ± 10% or −12 V ± 5% unless otherwise indicated)

Model (AD674B or AD774B)	J Grade Min	J Grade Typ	J Grade Max	K Grade Min	K Grade Typ	K Grade Max
RESOLUTION			12			12
LINEARITY ERROR @ +25°C			±1			±1/2
T_{MIN} to T_{MAX}			±1			±1/2
DIFFERENTIAL LINEARITY ERROR (Minimum Resolution for Which No Missing Codes are Guaranteed)	12			12		
UNIPOLAR OFFSET[1] @ +25°C			±2			±2
BIPOLAR OFFSET[1] @ +25°C			±6			±3
FULL-SCALE CALIBRATION ERROR[1, 2] @ +25°C (with Fixed 50 Ω Resistor from REF OUT to REF IN)		0.1	0.25		0.1	0.125
TEMPERATURE RANGE	0		+70	0		+70
TEMPERATURE DRIFT[3] (Using Internal Reference)						
Unipolar			±2			±1
Bipolar Offset			±2			±1
Full-Scale Calibration			±6			±2
POWER SUPPLY REJECTION Max Change in Full-Scale Calibration						
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2
V_{EE} = −15 V ± 1.5 V or −12 V ± 0.6 V			±2			±1
ANALOG INPUT						
Input Ranges						
Bipolar	−5		+5	−5		+5
	−10		+10	−10		+10
Unipolar	0		+10	0		+10
	0		+20	0		+20
Input Impedance						
10 Volt Span	3	5	7	3	5	7
20 Volt Span	6	10	14	6	10	14
POWER SUPPLIES						
Operating Range						
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5
V_{CC}	+11.4		+16.5	+11.4		+16.5
V_{EE}	−16.5		−11.4	−16.5		−11.4
Operating Current						
I_{LOGIC}		3.5	7		3.5	7
I_{CC}		3.5	7		3.5	7
I_{EE}		10	14		10	14
POWER CONSUMPTION		220	375		220	375
		175			175	
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1
Output Current (Available for External Loads) (External Load Should Not Change During the Conversion)			2.0			2.0

NOTES
[1]Adjustable to zero.
[2]Includes internal voltage reference error.
[3]Maximum change from +25°C value to the value at T_{MIN} or T_{MAX}.
[4]Tested with REF OUT tied to REF IN through 50 Ω resistor, V_{CC} = +16.5 V, V_{EE} = −16.5 V, V_{LOGIC} = +5.5 V, and outputs in high-Z mode.
[5]Tested with REF OUT tied to REF IN through 50 Ω resistor, V_{CC} = +12 V, V_{EE} = −12 V, V_{LOGIC} = +5 V, and outputs in high-Z mode.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test at T_{MIN}, +25°C, and T_{MAX}, and results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

2

A Grade			B Grade			T Grade			
Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
		12			12			12	Bits
		±1			±1/2			±1/2	LSB
		±1			±1/2			±1	LSB
12			12			12			Bits
		±2			±2			±2	LSB
		±6			±3			±3	LSB
	0.1	0.25		0.1	0.125		0.1	0.125	% of FS
−40		+85	−40		+85	−55		+125	°C
		±2			±1			±1	LSB
		±2			±1			±2	LSB
		±8			±5			±7	LSB
		±2			±1			±1	LSB
		±1/2			±1/2			±1/2	LSB
		±2			±1			±1	LSB
−5		+5	−5		+5	−5		+5	Volts
−10		+10	−10		+10	−10		+10	Volts
0		+10	0		+10	0		+10	Volts
0		+20	0		+20	0		+20	Volts
3	5	7	3	5	7	3	5	7	kΩ
6	10	14	6	10	14	6	10	14	kΩ
+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
−16.5		−11.4	−16.5		−11.4	−16.5		−11.4	Volts
	3.5	7		3.5	7		3.5	7	mA
	3.5	7		3.5	7		3.5	7	mA
	10	14		10	14		10	14	mA
	220	375		220	375		220	375	mW[4]
	175			175			175		mW[5]
9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
		2.0			2.0			2.0	mA

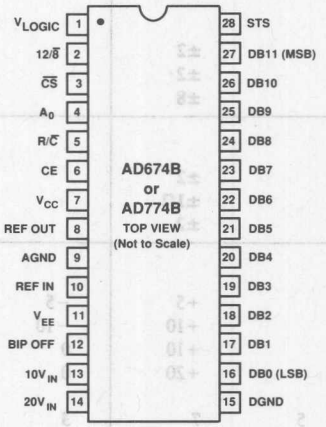
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		+2.0	V_{LOGIC} +0.5 V	V
V_{IL}	Low Level Input Voltage		−0.5	+0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{LOGIC}$	−10	+10	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V	−10	+10	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.5 mA	+2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		+0.4	V
I_{OZ}	High-Z Leakage Current	V_{IN} = 0 to V_{LOGIC}	−10	+10	μA
C_{OZ}	High-Z Output Capacitance			10	pF

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Digital Common . . . . . 0 to +16.5 V
V_{EE} to Digital Common . . . . . 0 to −16.5 V
V_{LOGIC} to Digital Common . . . . . 0 to +7 V
Analog Common to Digital Common . . . . . ±1 V
Digital Inputs to Digital Common . −0.5 V to V_{LOGIC} +0.5 V
Analog Inputs to Analog Common . . . . . V_{EE} to V_{CC}
20 V_{IN} to Analog Common . . . . . ±24 V
REF OUT . . . . . Indefinite Short to Common
. . . . . Momentary Short to V_{CC}
Junction Temperature . . . . . +175°C
Power Dissipation . . . . . 825 mW
Lead Temperature, Soldering . . . . . 300°C, 10 sec
Storage Temperature . . . . . −65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



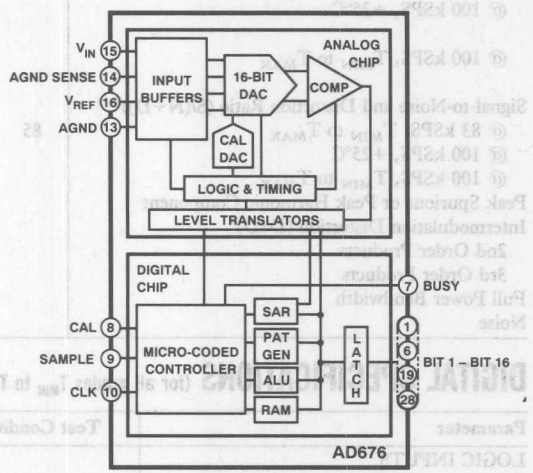
ORDERING GUIDE

Model[1]	Temperature	Conversion Time (max)	INL (T_{MIN} to T_{MAX})	Package Description	Package Option[2]
AD674BJN	0°C to +70°C	15 μs	±1 LSB	Plastic DIP	N-28
AD674BKN	0°C to +70°C	15 μs	±1/2 LSB	Plastic DIP	N-28
AD674BJR	0°C to +70°C	15 μs	±1 LSB	Plastic SOIC	R-28
AD674BKR	0°C to +70°C	15 μs	±1/2 LSB	Plastic SOIC	R-28
AD674BAD	−40°C to +85°C	15 μs	±1 LSB	Ceramic DIP	D-28
AD674BBD	−40°C to +85°C	15 μs	±1/2 LSB	Ceramic DIP	D-28
AD674BTD	−55°C to +125°C	15 μs	±1 LSB	Ceramic DIP	D-28
AD774BJN	0°C to +70°C	8 μs	±1 LSB	Plastic DIP	N-28
AD774BKN	0°C to +70°C	8 μs	±1/2 LSB	Plastic DIP	N-28
AD774BJR	0°C to +70°C	15 μs	±1 LSB	Plastic SOIC	R-28
AD774BKR	0°C to +70°C	15 μs	±1/2 LSB	Plastic SOIC	R-28
AD774BAD	−40°C to +85°C	8 μs	±1 LSB	Ceramic DIP	D-28
AD774BBD	−40°C to +85°C	8 μs	±1/2 LSB	Ceramic DIP	D-28
AD774BTD	−55°C to +125°C	8 μs	±1 LSB	Ceramic DIP	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD674B/AD774B/883B data sheet.
[2]N = Plastic DIP; D = Hermetic DIP; R = Plastic SOIC. For outline information see Package Information section.

FEATURES
Autocalibrating
On-Chip Sample-Hold Function
Parallel Output Format
16 Bits No Missing Codes
±1 LSB INL
−97 dB THD
90 dB S/(N+D)
1 MHz Full Power Bandwidth

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD676 is a multipurpose 16-bit parallel output analog-to-digital converter which utilizes a switched-capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 μs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The AD676 circuitry is segmented onto two monolithic chips—a digital control chip fabricated on Analog Devices DSP CMOS process and an analog ADC chip fabricated on our BiMOS II process. Both chips are contained in a single package.

The AD676 is specified for ac (or "dynamic") parameters such as S/(N+D) Ratio, THD and IMD which are important in signal processing applications. In addition, dc parameters are specified which are important in measurement applications.

The AD676 operates from +5 V and ±12 V supplies and typically consumes 360 mW during conversion. The digital supply (V_{DD}) is separated from the analog supplies (V_{CC}, V_{EE}) for reduced digital crosstalk. An analog ground sense is provided for the analog input. Separate analog and digital grounds are also provided.

The AD676 is available in a 28-pin plastic DIP or 28-pin side-brazed ceramic package. A serial-output version, the AD677, is available in a 16-pin 300 mil wide ceramic or plastic package.

AD676—SPECIFICATIONS

AC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD676J/A Min	AD676J/A Typ	AD676J/A Max	AD676K/B Min	AD676K/B Typ	AD676K/B Max	Units
Total Harmonic Distortion (THD)[2]							
@ 83 kSPS, T_{MIN} to T_{MAX}		−96	−88		−97	−90	dB
		0.0016	0.004		0.0014	0.003	%
@ 100 kSPS, +25°C		−96			−97		dB
		0.0016			0.0014		%
@ 100 kSPS, T_{MIN} to T_{MAX}		−92			−92		dB
		0.0025			0.0025		%
Signal-to-Noise and Distortion Ratio (S/(N+D))[2, 3]							
@ 83 kSPS, T_{MIN} to T_{MAX}	85	89		87	90		dB
@ 100 kSPS, +25°C		89			90		dB
@ 100 kSPS, T_{MIN} to T_{MAX}		86			86		dB
Peak Spurious or Peak Harmonic Component		−98			−98		dB
Intermodulation Distortion (IMD)[4]							
2nd Order Products		−102			−102		dB
3rd Order Products		−98			−98		dB
Full Power Bandwidth		1			1		MHz
Noise		160			160		μV rms

DIGITAL SPECIFICATIONS (for all grades T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High-Level Input Voltage		2.4		V_{DD} +0.3	V
V_{IL}	Low-Level Input Voltage		−0.3		0.8	V
I_{IH}	High-Level Input Current	$V_{IH} = V_{DD}$	−10		+10	μA
I_{IL}	Low-Level Input Current	$V_{IL} = 0$ V	−10		+10	μA
C_{IN}	Input Capacitance			10		pF
LOGIC OUTPUTS						
V_{OH}	High-Level Output Voltage	I_{OH} = 0.1 mA	V_{DD} − 1 V			V
		= 0.5 mA	2.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 1.6 mA			0.4	V

NOTES

[1]V_{REF} = 10.0 V, Conversion Rate (fs) = 83 kSPS, f_{IN} = 1.0 kHz, V_{IN} = −0.05 dB, Bandwidth = fs/2 unless otherwise indicated. All measurements referred to a 0 dB (20 V p-p) input signal. Values are post-calibration.

[2]For other input amplitudes, refer to Figure 13.

[3]For other input ranges/voltages reference values see Figure 12.

[4]fa = 1008 Hz, fb = 1055 Hz. See Definition of Specifications section and Figure 15.

Specifications subject to change without notice.

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD676J/A Min	AD676J/A Typ	AD676J/A Max	AD676K/B Min	AD676K/B Typ	AD676K/B Max	Units
TEMPERATURE RANGE							
J, K Grades	0		+70	0		+70	°C
A, B Grades	−40		+85	−40		+85	°C
ACCURACY							
Resolution	16			16			Bits
Integral Nonlinearity (INL)							
@ 83 kSPS, T_{MIN} to T_{MAX}		±1			±1	±1.5	LSB
@ 100 kSPS, +25°C		±1			±1		LSB
@ 100 kSPS, T_{MIN} to T_{MAX}		±2			±2		LSB
Differential Nonlinearity (DNL)—No Missing Codes		16		16			Bits
Bipolar Zero Error[2] (at Nominal Supplies)		0.005			0.005		% FSR
Gain Error (at Nominal Supplies)							
@ 83 kSPS[2]		0.005			0.005		% FSR
@ 100 kSPS, +25°C		0.005			0.005		% FSR
@ 100 kSPS[2]		0.01			0.01		% FSR
Temperature Drift, Bipolar Zero[3]							% FSR
J, K Grades		0.0015			0.0015		% FSR
A, B Grades		0.003			0.003		% FSR
Temperature Drift, Gain[3]							
J, K Grades		0.0015			0.0015		% FSR
A, B Grades		0.003			0.003		% FSR
VOLTAGE REFERENCE INPUT RANGE[4] (V_{REF})	5		10	5		10	V
ANALOG INPUT[5]							
Input Range (V_{IN})			$\pm V_{REF}$			$\pm V_{REF}$	V
Input Impedance		*			*		
Input Settling Time		2			2		µs
Input Capacitance During Sample			50*			50*	pF
Aperture Delay		6			6		ns
Aperture Jitter		100			100		ps
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = +12 V ± 5%		±1			±1		LSB
V_{EE} = −12 V ± 5%		±1			±1		LSB
V_{DD} = +5 V ± 10%		±1			±1		LSB
Operating Current							
I_{CC}		14.5	18		14.5	18	mA
I_{EE}		14.5	18		14.5	18	mA
I_{DD}		2	5		2	5	mA
Power Consumption		360	480		360	480	mW

NOTES

[1]V_{REF} = 5.0 V, Conversion Rate = 83 kSPS unless otherwise noted. Values are post-calibration.

[2]Values shown apply to any temperature from T_{MIN} to T_{MAX} after calibration at that temperature.

[3]Values shown are based upon calibration at +25°C with no additional calibration at temperature. Values shown are the worst case variation from the value at +25°C

[4]See "APPLICATIONS" section for recommended voltage reference circuit, and Figure 12 for dynamic performance with other reference voltage values.

[5]See "APPLICATIONS" section for recommended input buffer circuit.

*For explanation of input characteristics, see "ANALOG INPUT" section.

Specifications subject to change without notice.

Parameter	Symbol	Min	Typ	Max	Units
Conversion Time[2]	t_C	10		1000	µs
CLK Period[3]	t_{CLK}	480			ns
Calibration Time	t_{CT}			85,530	t_{CLK}
Sampling Time (Included in t_C)	t_S	2			µs
CAL to BUSY Delay	t_{CALB}		75	150	ns
BUSY to SAMPLE Delay	t_{BS}	2			µs
SAMPLE to BUSY Delay	t_{SB}		15	100	ns
CLK HIGH[4]	t_{CH}	50			ns
CLK LOW[4]	t_{CL}	50			ns
SAMPLE LOW to 1st CLK Delay	t_{SC}	50			ns
SAMPLE LOW	t_{SL}	100			ns
Output Delay	t_{OD}		125	200	ns
Status Delay	t_{SD}	50			ns
CAL HIGH Time	t_{CALH}	50			ns

NOTES
[1]See the "CONVERSION CONTROL" and "AUTOCALIBRATION" sections for detailed explanations of the above timing.
[2]Depends upon external clock frequency; includes acquisition time and conversion time. The maximum conversion time is specified to account for the droop of the internal sample/hold function. Longer conversion times may degrade performance. See "General Conversion Guidelines" for additional explanation of maximum conversion time.
[3]580 ns is recommended for optimal accuracy over temperature.
[4]$t_{CH} + t_{CL} = t_{CLK}$ and must be greater than 480 ns.

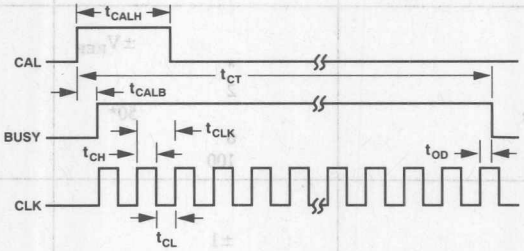


Figure 1. Calibration Timing

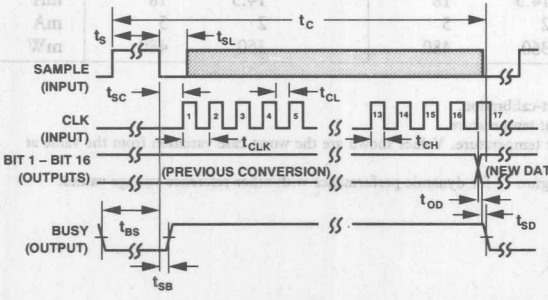


Figure 2a. General Conversion Timing

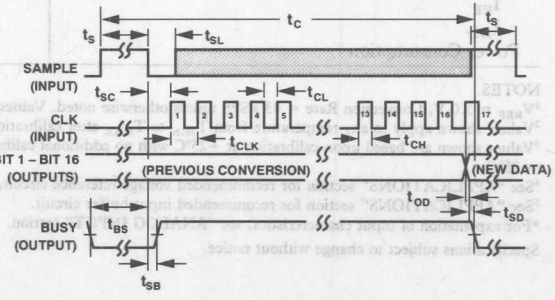


Figure 2b. Continuous Conversion Timing

Model	Temperature Range[1]	S/(N+D)	Max INL	Package Description	Option[2]
AD676JD	0°C to +70°C	85 dB		Ceramic 28-Pin DIP	D-28
AD676KD	0°C to +70°C	87 dB	±1.5 LSB	Ceramic 28-Pin DIP	D-28
AD676AD	−40°C to +85°C	85 dB		Ceramic 28-Pin DIP	D-28
AD676BD	−40°C to +85°C	87 dB	±1.5 LSB	Ceramic 28-Pin DIP	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the AD676/883 data sheet.
[2]D = Ceramic DIP. For outline information see Package Information section.

2

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to V_{EE} . . . . . −0.3 V to +26.4 V
V_{DD} to DGND . . . . . −0.3 V to +7 V
V_{CC} to AGND . . . . . −0.3 V to +18 V
V_{EE} to AGND . . . . . −18 V to +0.3 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . 0 to +5.5 V
Analog Inputs, V_{REF} to AGND
. . . . . (V_{CC} + 0.3 V) to (V_{EE} − 0.3 V)
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . −65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

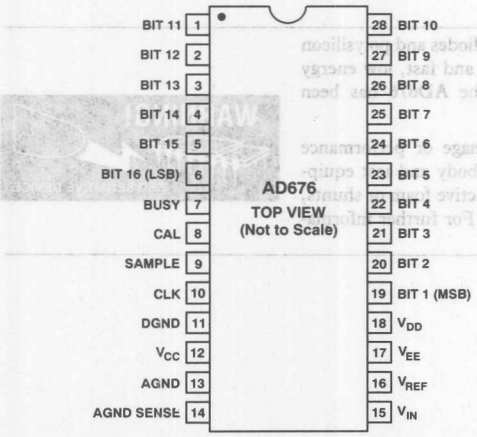
The AD676 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD676 has been classified as a Category 1 Device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment, and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam discharged to the destination socket before devices are removed. For further information on ESD precaution, refer to Analog Devices' *ESD Prevention Manual*.

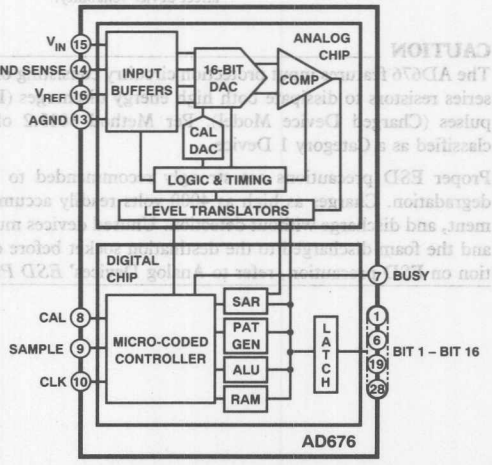
PIN DESCRIPTION

Pin	Name	Type	Description
1–6	BIT 11–BIT 16	DO	BIT 11–BIT 16 represent the six LSBs of data.
7	BUSY	DO	Status Line for Converter. Active HIGH, indicating a conversion or calibration in progress. BUSY should be buffered when capacitively loaded.
8	CAL	DI	Calibration Control Pin (Asynchronous).
9	SAMPLE	DI	V_{IN} Acquisition Control Pin. Active HIGH. During conversion, SAMPLE controls the state of the internal sample-hold amplifier and the falling edge initiates conversion (see "Conversion Control" paragraph). During calibration, SAMPLE should be held LOW. If HIGH during calibration, diagnostic information will appear on the two LSBs (Pins 5 and 6).
10	CLK	DI	Master Clock Input. The AD676 requires 17 clock cycles to execute a conversion.
11	DGND	P	Digital Ground.
12	V_{CC}	P	+12 V Analog Supply Voltage.
13	AGND	P/AI	Analog Ground.
14	AGND SENSE	AI	Analog Ground Sense.
15	V_{IN}	AI	Analog Input Voltage.
16	V_{REF}	AI	External Voltage Reference Input.
17	V_{EE}	P	−12 V Analog Supply Voltage. Note: the lid of the ceramic package is internally connected to V_{EE}.
18	V_{DD}	P	+5 V Logic Supply Voltage.
19–28	BIT 1–BIT 10	DO	BIT 1–BIT 10 represent the ten MSB of data.

Type: AI = Analog Input
DI = Digital Input
DO = Digital Output
P = Power



Package Pinout



Functional Block Diagram

NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist frequency" of a converter is that input frequency which is one half the sampling frequency of the converter.

TOTAL HARMONIC DISTORTION
Total harmonic distortion (THD) is the ratio of the rms sum of the harmonic components to the rms value of a full-scale input signal and is expressed in percent (%) or decibels (dB). For input signals or harmonics that are above the Nyquist frequency, the aliased components are used.

SIGNAL-TO-NOISE PLUS DISTORTION RATIO
Signal-to-noise plus distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

GAIN ERROR
The last transition should occur at an analog value 1.5 LSB below the nominal full scale (4.99977 volts for a ±5 V range). The gain error is the deviation of the actual difference between the first and last code transition from the ideal difference between the first and last code transition.

BIPOLAR ZERO ERROR
Bipolar zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are one LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

INTEGRAL NONLINEARITY (INL)
The ideal transfer function for an ADC is a straight line bisecting the center of each code drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the most negative code transition. "Full scale" is defined as a level 1.5 LSB beyond the most positive code transition. Integral nonlinearity is the worst-case deviation of a code center average from the straight line.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb), and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude, and the peak value of their sum is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

APERTURE DELAY
Aperture delay is the time required after SAMPLE pin is taken LOW for the internal sample-hold of the AD676 to open, thus holding the value of V_{IN}.

APERTURE JITTER
Aperture jitter is the variation in the aperture delay from sample to sample.

POWER SUPPLY REJECTION
DC variations in the power supply voltage will affect the overall transfer function of the ADC, resulting in zero error and gain error changes. Power supply rejection is the maximum change in either the bipolar zero error or gain error value. Additionally, there is another power supply variation to consider. AC ripple on the power supplies can couple noise into the ADC, resulting in degradation of dynamic performance. This is displayed in Figure 16.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

The AD676 is a multipurpose 16-bit analog-to-digital converter and includes circuitry which performs an input sample/hold function, ground sense, and autocalibration. These functions are segmented onto two monolithic chips—an analog signal processor and a digital controller. Both chips are contained within the AD676 package.

The AD676 employs a successive-approximation technique to determine the value of the analog input voltage. However, instead of the traditional laser-trimmed resistor-ladder approach, this device uses a capacitor-array, charge redistribution technique. Binary-weighted capacitors subdivide the input sample to perform the actual analog-to-digital conversion. The capacitor array eliminates variation in the linearity of the device due to temperature-induced mismatches of resistor values. Since a capacitor array is used to perform the data conversions, the sample/hold function is included without the need for additional external circuitry.

Initial errors in capacitor matching are eliminated by an autocalibration circuit within the AD676. This circuit employs an on-chip microcontroller and a calibration DAC to measure and compensate capacitor mismatch errors. As each error is determined, its value is stored in on-chip memory (RAM). Subsequent conversions use these RAM values to improve conversion accuracy. The autocalibration routine may be invoked at any time. Autocalibration insures high performance while eliminating the need for any user adjustments and is described in detail below.

The microcontroller controls all of the various functions within the AD676. These include the actual successive approximation algorithm, the autocalibration routine, the sample/hold operation, and the internal output data latch.

AUTOCALIBRATION

The AD676 achieves rated performance without the need for user trims or adjustments. This is accomplished through the use of on-chip autocalibration.

In the autocalibration sequence, sample/hold offset is nulled by internally connecting the input circuit to the ground sense circuit. The resulting offset voltage is measured and stored in RAM for later use. Next, the capacitor representing the most significant bit (MSB) is charged to the reference voltage. This charge is then transferred to a capacitor of equal size (composed of the sum of the remaining lower weight bits). The difference in the voltage that results and the reference voltage represents the amount of capacitor mismatch. A calibration digital-to-analog converter (DAC) adds an appropriate value of error correction voltage to cancel this mismatch. This correction factor is also stored in RAM. This process is repeated for each of the capacitors representing the remaining top eight bits. The accumulated values in RAM are then used during subsequent conversions to adjust conversion results accordingly.

As shown in Figure 1, when CAL is taken HIGH the AD676 internal circuitry is reset, the BUSY pin is driven HIGH, and the ADC prepares for calibration. This is an asynchronous hardware reset and will interrupt any conversion or calibration currently in progress. Actual calibration begins when CAL is taken going LOW. During calibration, it is preferable that SAMPLE be held LOW. If SAMPLE is HIGH, diagnostic data will appear on Pins 5 and 6. This data is of no value to the user.

The AD676 requires one clock cycle after BUSY goes LOW to complete the calibration cycle. If this clock cycle is not provided, it will be taken from the first conversion, likely resulting in first conversion error.

In most applications, it is sufficient to calibrate the AD676 only upon power-up, in which case care should be taken that the power supplies and voltage reference have stabilized first. If not calibrated, the AD676 accuracy may be as low as 10 bits.

CONVERSION CONTROL

The AD676 is controlled by two signals: SAMPLE and CLK, as shown in Figures 2a and 2b. It is assumed that the part has been calibrated and the digital I/O pins have the levels shown at the start of the timing diagram.

A conversion consists of an input acquisition followed by 17 clock pulses which execute the 16-bit internal successive approximation routine. The analog input is acquired by taking the SAMPLE line HIGH for a minimum sampling time of t_S. The actual sample taken is the voltage present on V_{IN} one aperture delay after the SAMPLE line is brought LOW, assuming the previous conversion has completed (signified by BUSY going LOW). Care should be taken to ensure that this negative edge is well defined and jitter free in ac applications to reduce the uncertainty (noise) in signal acquisition. With SAMPLE going LOW, the AD676 commits itself to the conversion—the input at V_{IN} is disconnected from the internal capacitor array, BUSY goes HIGH, and the SAMPLE input will be ignored until the conversion is completed (when BUSY goes LOW). SAMPLE must be held LOW for a minimum period of time t_{SL}. A period of time t_{SC} after bringing SAMPLE LOW, the 17 CLK cycles are applied; CLK pulses that start before this period of time are ignored. BUSY goes HIGH t_{SB} after SAMPLE goes LOW, signifying that a conversion is in process, and remains HIGH until the conversion is completed. BUSY goes LOW during the 17th CLK cycle at the point where the data outputs have changed and are valid. The AD676 will ignore CLK after BUSY has gone LOW and the output data will remain constant until a new conversion is completed. The data can, therefore, be read any time after BUSY goes LOW and before the 17th CLK of the next conversion (see Figures 2a and 2b). The section on Microprocessor Interfacing discusses how the AD676 can be interfaced to a 16-bit databus.

Typically BUSY would be used to latch the AD676 output data into buffers or to interrupt microprocessors or DSPs. It is recommended that the capacitive load on BUSY be minimized by driving no more than a single logic input. Higher capacitive loads such as cables or multiple gates may degrade conversion quality unless BUSY is buffered.

CONTINUOUS CONVERSION

For maximum throughput rate, the AD676 can be operated in a continuous convert mode (see Figure 2b). This is accomplished by utilizing the fact that SAMPLE will no longer be ignored after BUSY goes LOW, so an acquisition may be initiated even

circuitry. If SAMPLE is already HIGH when BUSY goes LOW at the end of a conversion, then an acquisition is immediately initiated and t_S and t_C start from that time. Data from the previous conversion may be latched up to t_{SD} before BUSY goes LOW or t_{OD} after the rising edge of the 17th clock pulse. However, it is preferred that latching occur on or after the falling edge of BUSY.

Care must be taken to adhere to the minimum/maximum timing requirements in order to preserve conversion accuracy.

GENERAL CONVERSION GUIDELINES

During signal acquisition and conversion, care should be taken with the logic inputs to avoid digital feedthrough noise. It is possible to run CLK continuously, even during the sample period. However, CLK edges during the sampling period, and especially when SAMPLE goes LOW, may inject noise into the sampling process. The AD676 is tested with no CLK cycles during the sampling period. The BUSY signal can be used to prevent the clock from running during acquisition, as illustrated in Figure 3. In this circuit BUSY is used to reset the circuitry which divides the system clock down to provide the AD676 CLK. This serves to interrupt the clock until after the input signal has been acquired, which has occurred when BUSY goes HIGH. When the conversion is completed and BUSY goes LOW, the circuit in Figure 3 truncates the 17th CLK pulse width which is tolerable because only its rising edge is critical.

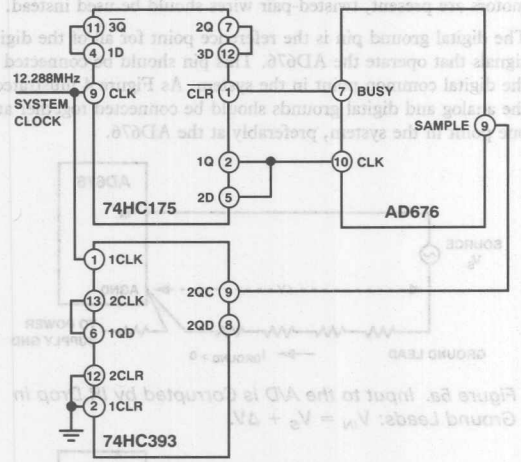


Figure 3.

Figure 3 also illustrates the use of a counter (74HC393) to derive the AD676 SAMPLE command from the system clock when a continuous convert mode is desirable. Pin 9 (2QC) provides a 96 kHz sample rate for the AD676 when used with a 12.288 MHz system clock. Alternately, Pin 8 (2QD) could be used for a 48 kHz rate.

If a continuous clock is used, then the user must avoid CLK edges at the instant of disconnecting V_{IN} which occurs at the falling edge of SAMPLE (see t_{SC} specification). The duty cycle of CLK may vary, but both the HIGH (t_{CH}) and LOW (t_{CL}) edge of CLK. To avoid a negative edge transition disturbing the comparator's settling, t_{CL} should be at least half the value of t_{CLK}. To also avoid transitions disturbing the internal comparator's settling, it is not recommended that the SAMPLE pin change state toward the end of a CLK cycle.

During a conversion, internal dc error terms such as comparator voltage offset are sampled, stored on internal capacitors and used to correct for their corresponding errors when needed. Because these voltages are stored on capacitors, they are subject to leakage decay and so require refreshing. For this reason there is a maximum conversion time t_C (1000 μs). From the time SAMPLE goes HIGH to the completion of the 17th CLK pulse, no more than 1000 μs should elapse for specified performance. However, there is no restriction to the maximum time between conversions.

Output coding for the AD676 is twos complement, as shown in Table I. By inverting the MSB, the coding can be converted to offset binary. The AD676 is designed to limit output coding in the event of out-of-range inputs.

Table 1. Output Coding

V_{IN}	Output Code
>Full Scale	011 . . . 11
Full Scale	011 . . . 11
Full Scale − 1 LSB	011 . . . 10
Midscale + 1 LSB	000 . . . 01
Midscale	000 . . . 00
Midscale − 1 LSB	111 . . . 11
−Full Scale + 1 LSB	100 . . . 01
−Full Scale	100 . . . 00
<−Full Scale	100 . . . 00

POWER SUPPLIES AND DECOUPLING

The AD676 has three power supply input pins. V_{CC} and V_{EE} provide the supply voltages to operate the analog portions of the AD676 including the ADC and sample-hold amplifier (SHA). V_{DD} provides the supply voltage which operates the digital portions of the AD676 including the data output buffers and the autocalibration controller.

As with most high performance linear circuits, changes in the power supplies can produce undesired changes in the performance of the circuit. Optimally, well regulated power supplies with less than 1% ripple should be selected. The ac output impedance of a power supply is a complex function of frequency, and in general will increase with frequency. In other words, high frequency switching such as that encountered with digital circuitry requires fast transient currents which most power supplies cannot adequately provide. This results in voltage spikes on the supplies. If these spikes exceed the ±5% tolerance of the ±12 V supplies or the ±10% limits of the +5 V supply, ADC performance will degrade. Additionally, spikes at frequencies higher than 100 kHz will also degrade performance. To compensate for the finite ac output impedance of the supplies, it is necessary to store "reserves" of charge in bypass capacitors. These capacitors can effectively lower the ac impedance presented to the AD676 power inputs which in turn will significantly reduce the magnitude of the voltage spikes. For

bypassing to be effective, certain guidelines should be followed. Decoupling capacitors, typically 0.1 μF, should be placed as closely as possible to each power supply pin of the AD676. It is essential that these capacitors be placed physically close to the IC to minimize the inductance of the PCB trace between the capacitor and the supply pin. The logic supply (V_{DD}) should be decoupled to digital common and the analog supplies (V_{CC} and V_{EE}) to analog common. The reference input is also considered as a power supply pin in this regard and the same decoupling procedures apply. These points are displayed in Figure 4.

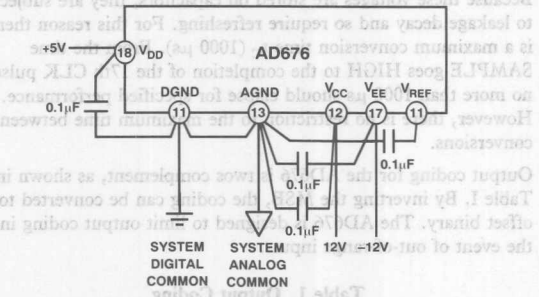


Figure 4. Grounding and Decoupling the AD676

Additionally, it is beneficial to have large capacitors (>47 μF) located at the point where the power connects to the PCB with 10 μF capacitors located in the vicinity of the ADC to further reduce low frequency ripple. In systems that will be subjected to particularly harsh environmental noise, additional decoupling may be necessary. RC-filtering on each power supply combined with dedicated voltage regulation can substantially decrease power supply ripple effects (this is further detailed in Figure 7).

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 4 LSBs at the 16-bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals.

Analog and digital signals should not share a common return path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point at the AD676 to minimize interference between analog and digital circuitry. Analog signals should be routed as far as possible from digital signals and should cross them, if at all, only at right angles. A solid analog ground plane around the AD676 will isolate it from large switching ground currents. For these reasons, the use of wire wrap circuit construction will not provide adequate performance; careful printed circuit board construction is preferred.

GROUNDING

The AD676 has three grounding pins, designated ANALOG GROUND (AGND), DIGITAL GROUND (DGND) and ANALOG GROUND SENSE (AGND SENSE). The analog ground pin is the "high quality" ground reference point for the device, and should be connected to the analog common point in the system.

AGND SENSE is intended to be connected to the input signal ground reference point. This allows for slight differences in level between the analog ground point in the system and the input signal ground point. However no more than 100 mV is recommended between the AGND and the AGND SENSE pins for specified performance.

Using AGND SENSE to remotely sense the ground potential of the signal source can be useful if the signal has to be carried some distance to the A/D converter. Since all IC ground currents have to return to the power supply and no ground leads are free from resistance and inductance, there are always some voltage differences from one ground point in a system to another.

Over distance this voltage difference can easily amount to several LSBs (in a 10 V input span, 16-bit system each LSB is about 0.15 mV). This would directly corrupt the A/D input signal if the A/D measures its input with respect to power ground (AGND) as shown in Figure 5a. To solve this problem the AD676 offers an AGND SENSE pin. Figure 5b shows how the AGND SENSE can be used to eliminate the problem in Figure 5a. Figure 5b also shows how the signal wires should be shielded in a noisy environment to avoid capacitive coupling. If inductive (magnetic) coupling is expected to be dominant such as where motors are present, twisted-pair wires should be used instead.

The digital ground pin is the reference point for all of the digital signals that operate the AD676. This pin should be connected to the digital common point in the system. As Figure 4 illustrated, the analog and digital grounds should be connected together at one point in the system, preferably at the AD676.

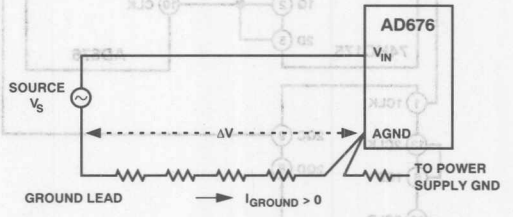


Figure 5a. Input to the A/D Is Corrupted by IR Drop in Ground Leads: $V_{IN} = V_S + \Delta V$.

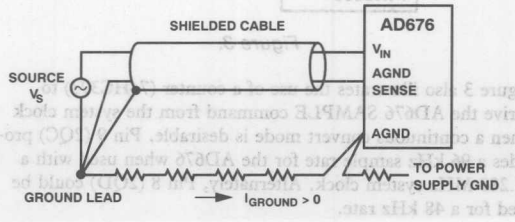


Figure 5b. AGND SENSE Eliminates the Problem in Figure 5a.

VOLTAGE REFERENCE

The AD676 requires the use of an external voltage reference. The input voltage range is determined by the value of the reference voltage; in general, a reference voltage of n volts allows an input range of ±n volts. The AD676 is specified for both 10 V and 5.0 V references. A 10 V reference will typically require support circuitry operated from ±15 V supplies; a 5.0 V reference may be used with ±12 V supplies. Signal-to-noise performance is increased proportionately with input signal range. In the presence of a fixed amount of system noise, increasing the LSB size (which results from increasing the reference voltage) will increase the effective S/(N+D) performance. Figure 12 illustrates S/(N+D) as a function of reference voltage. In contrast, INL will be optimal at lower reference voltage values (such as 5 V) due to capacitor nonlinearity at higher voltage values.

During a conversion, the switched capacitor array of the AD676 presents a dynamically changing current load at the voltage reference as the successive-approximation algorithm cycles through various choices of capacitor weighting. (See the following section "Analog Input" for a detailed discussion of the V_{REF} input characteristics.) The output impedance of the reference circuitry must be low so that the output voltage will remain sufficiently constant as the current drive changes. In some applications, this may require that the output of the voltage reference be buffered by an amplifier with low impedance at relatively high frequencies. In choosing a voltage reference, consideration should be made for selecting one with low noise. A capacitor connected between REF IN and AGND will reduce the demands on the reference by decreasing the magnitude of high frequency components required to be sourced by the reference.

Figures 6 and 7 represent typical design approaches.

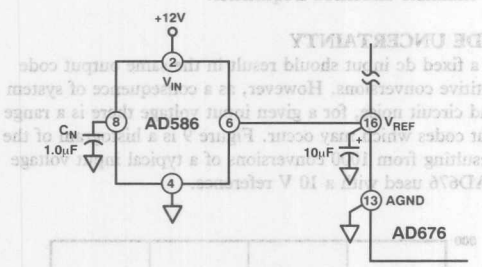


Figure 6.

Figure 6 shows a voltage reference circuit featuring the 5 V output AD586. The AD586 is a low cost reference which utilizes a buried Zener architecture to provide low noise and drift. Over the 0°C to +70°C range, the AD586L grade exhibits less than 2.25 mV output change from its initial value at +25°C. A noise-reduction capacitor, C_N, reduces the broadband noise of the AD586 output, thereby optimizing the overall performance of the AD676. It is recommended that a 10 μF to 47 μF high quality tantalum capacitor be tied between the V_{REF} input of the AD676 and ground to minimize the impedance on the reference.

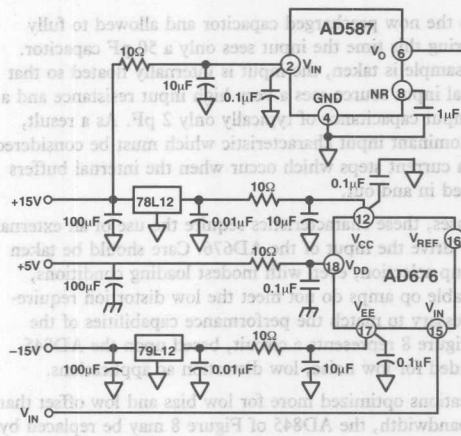


Figure 7.

Using the AD676 with ±10 V input range (V_{REF} = 10 V) typically requires ±15 V supplies to drive op amps and the voltage reference. If ±12 V is not available in the system, regulators such as 78L12 and 79L12 can be used to provide power for the AD676. This is also the recommended approach (for any input range) when the ADC system is subjected to harsh environments such as where the power supplies are noisy and where voltage spikes are present. Figure 7 shows an example of such a system based upon the 10 V AD587 reference, which provides a 300 μV LSB. Circuitry for additional protection against power supply disturbances has been shown. A 100 μF capacitor at each regulator prevents very large voltage spikes from entering the regulators. Any power line noise which the regulators cannot eliminate will be further filtered by an RC filter (10 Ω/10 μF) having a −3 dB point at 1.6 kHz. For best results the regulators should be within a few centimeters of the AD676.

ANALOG INPUT

As previously discussed, the analog input voltage range for the AD676 is ±V_{REF}. For purposes of ground drop and common mode rejection, the V_{IN} and V_{REF} inputs each have their own ground. V_{REF} is referred to the local analog system ground (AGND), and V_{IN} is referred to the analog ground sense pin (AGND SENSE) which allows a remote ground sense for the input signal.

The AD676 analog inputs (V_{IN}, V_{REF} and AGND SENSE) exhibit dynamic characteristics. When a conversion cycle begins, each analog input is connected to an internal, discharged 50 pF capacitor which then charges to the voltage present at the corresponding pin. The capacitor is disconnected when SAMPLE is taken LOW, and the stored charge is used in the subsequent conversion. In order to limit the demands placed on the external source by this high initial charging current, an internal buffer amplifier is employed between the input and this capacitance for a few hundred nanoseconds. During this time the input pin exhibits typically 20 kΩ input resistance, 10 pF input capacitance and ±40 μA bias current. Next, the input is switched

directly to the now precharged capacitor and allowed to fully settle. During this time the input sees only a 50 pF capacitor. Once the sample is taken, the input is internally floated so that the external input source sees a very high input resistance and a parasitic input capacitance of typically only 2 pF. As a result, the only dominant input characteristic which must be considered is the high current steps which occur when the internal buffers are switched in and out.

In most cases, these characteristics require the use of an external op amp to drive the input of the AD676. Care should be taken with op amp selection; even with modest loading conditions, most available op amps do not meet the low distortion requirements necessary to match the performance capabilities of the AD676. Figure 8 represents a circuit, based upon the AD845, recommended for low noise, low distortion ac applications.

For applications optimized more for low bias and low offset than speed or bandwidth, the AD845 of Figure 8 may be replaced by the OP-27.

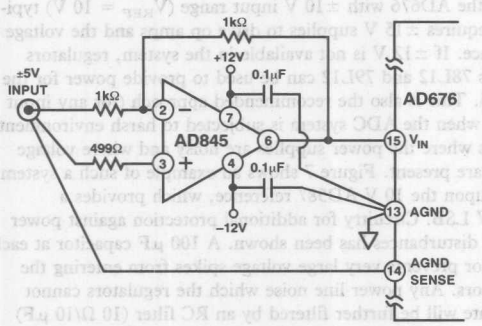


Figure 8.

AC PERFORMANCE

AC parameters, which include S/(N+D), THD, etc., reflect the AD676's effect on the spectral content of the analog input signal. Figures 12 through 16 provide information on the AD676's ac performance under a variety of conditions.

As a general rule, averaging the results from several conversions reduces the effects of noise, and therefore improves such parameters as S/(N+D). AD676 performance may be optimized by operating the device at its maximum sample rate of 100 kSPS and digitally filtering the resulting bit stream to the desired signal bandwidth. This succeeds in distributing noise over a wider frequency range, thus reducing the noise density in the frequency band of interest. This subject is discussed in the following section.

OVERSAMPLING AND NOISE FILTERING

The Nyquist rate for a converter is defined as one-half its sampling rate. This is established by the Nyquist theorem, which requires that a signal be sampled at a rate corresponding to at least twice its highest frequency component of interest in order to preserve the informational content. Oversampling is a conversion technique in which the sampling frequency is more than twice the frequency bandwidth of interest. In audio applications, the AD676 can operate at a $2 \times F_S$ oversampling rate, where F_S = 48 kHz.

In quantized systems, the informational content of the analog input is represented in the frequency spectrum from dc to the Nyquist rate of the converter. Within this same spectrum are higher frequency noise and signal components. Antialias, or low pass, filters are used at the input to the ADC to reduce these noise and signal components so that their aliased components do not corrupt the baseband spectrum. However, wideband noise contributed by the AD676 will not be reduced by the antialias filter. The AD676 quantization noise is evenly distributed from dc to the Nyquist rate, and this fact can be used to minimize its overall affect.

The AD676 quantization noise effects can be reduced by oversampling—sampling at a rate higher than that defined by the Nyquist theorem. This spreads the noise energy over a bandwidth wider than the frequency band of interest. By judicious selection of a digital decimation filter, noise frequencies outside the bandwidth of interest may be eliminated.

The process of analog to digital conversion inherently produces noise, known as quantization noise. The magnitude of this noise is a function of the resolution of the converter, and manifests itself as a limit to the theoretical signal-to-noise ratio achievable. This limit is described by $S/(N+D) = (6.02n + 1.76 + 10 \log F_S/2F_A)$ dB, where n is the resolution of the converter in bits, F_S is the sampling frequency, and Fa is the signal bandwidth of interest. For audio bandwidth applications, the AD676 is capable of operating at a 2 × oversample rate (96 kSPS), which typically produces an improvement in S/(N+D) of 3 dB compared with operating at the Nyquist conversion rate of 48 kSPS. Oversampling has another advantage as well; the demands on the antialias filter are lessened. In summary, system performance is optimized by running the AD676 at or near its maximum sampling rate of 100 kHz and digitally filtering the resulting spectrum to eliminate undesired frequencies.

DC CODE UNCERTAINTY

Ideally, a fixed dc input should result in the same output code for repetitive conversions. However, as a consequence of system noise and circuit noise, for a given input voltage there is a range of output codes which may occur. Figure 9 is a histogram of the codes resulting from 1000 conversions of a typical input voltage by the AD676 used with a 10 V reference.

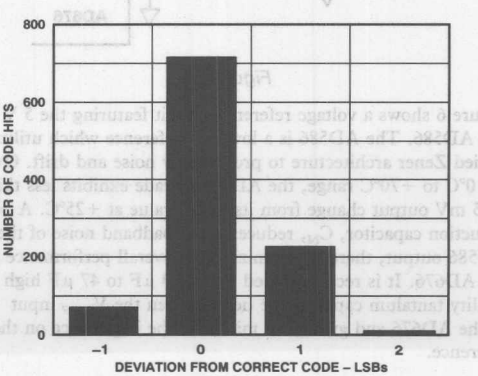


Figure 9. Distribution of Codes from 1000 Conversions, Relative to the Correct Code.

The standard deviation of this distribution is approximately 0.5 LSBs. If less uncertainty is desired, averaging multiple conversions will narrow this distribution by the inverse of the square root of the number of samples; i.e., the average of 4 conversions would have a standard deviation of 0.25 LSBs.

MICROPROCESSOR INTERFACE

The AD676 is ideally suited for use in both traditional dc measurement applications supporting a microprocessor, and in ac signal processing applications interfacing to a digital signal processor. The AD676 is designed to interface with a 16-bit data bus, providing all output data bits in a single read cycle. A variety of external buffers, such as 74HC541, can be used with the AD676 to provide 3-state outputs, high driving capability, and to prevent bus noise from coupling into the ADC. The following sections illustrate the use of the AD676 with a representative digital signal processor and microprocessor. These circuits provide general interface practices which are applicable to other processor choices.

ADSP-2101

Figure 10a shows the AD676 interfaced to the ADSP-2101 DSP processor. The AD676 buffers are mapped in the ADSP-2101's memory space, requiring one wait state when using a 12.5 MHz processor clock.

The falling edge of BUSY interrupts the processor, indicating that new data is ready. The ADSP-2101 automatically jumps to the appropriate service routine with minimal overhead. The interrupt routine then instructs the processor to read the new data using a memory read instruction.

Figure 10b shows circuitry which would be included by a typical address decoder for the output buffers. In this case, a data memory access to any address in the range 3000H to 37FFH will result in the output buffers being enabled.

The AD676 CLK and SAMPLE can be generated by dividing down the system clock as described earlier (Figure 3), or if the ADSP-2101 serial port clocks are not being used, they can be programmed to generate CLK and SAMPLE.

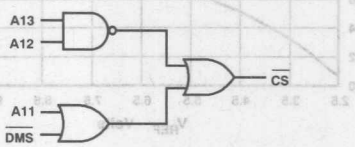


Figure 10b.

80286

The 80286 16-bit microprocessor can be interfaced to a buffered AD676 without any generation of wait states. As seen in Figure 11, BUSY can be used both to control the AD676 clock and to alert the processor when new data is ready. In the system shown, the 80286 should be configured in an edge triggered, direct interrupt mode (integrated controller provides the interrupt vector). Since the 80286 does not latch interrupt signals, the interrupt needs to be internally acknowledged before BUSY goes HIGH again during the next AD676 conversion (BUSY = 0). Depending on whether the AD676 buffers are mapped into memory or I/O space, the interrupt service routine will read the data by using either the MOV or the IN instruction. To be able to read all the 16 bits at once, and thereby increase the 80286's efficiency, the buffers should be located at an even address.

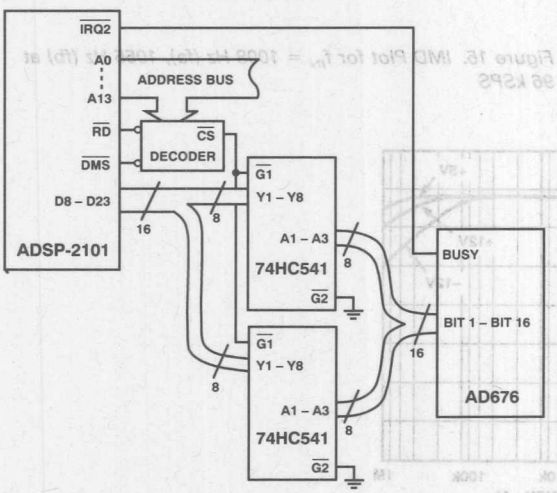


Figure 10a.

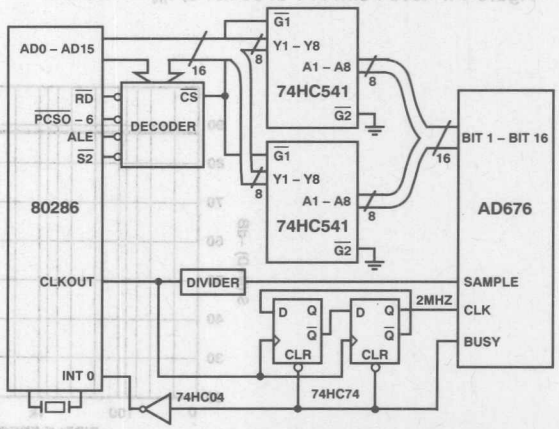


Figure 11.

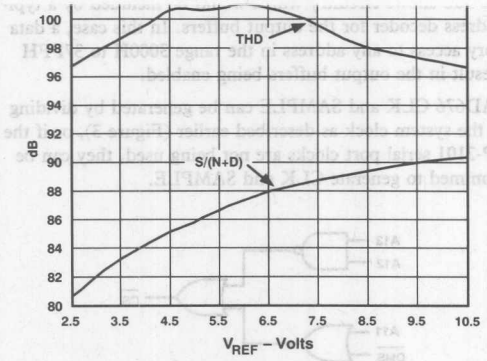


Figure 12. S/(N+D) and THD vs. V_{REF}

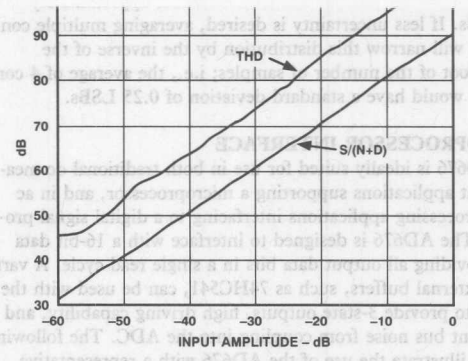


Figure 13. S/(N+D) and THD vs. Input Amplitude

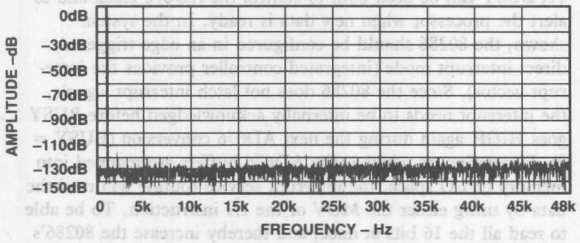


Figure 14. 4096 Point FFT at 96 kSPS, f_{IN} = 1.06 kHz

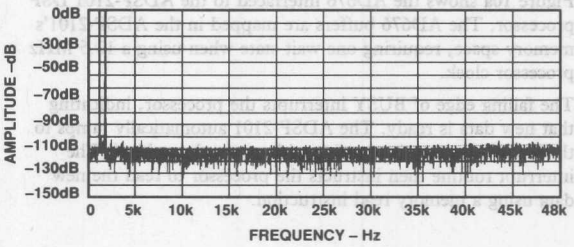


Figure 15. IMD Plot for f_{IN} = 1008 Hz (fa), 1055 Hz (fb) at 96 kSPS

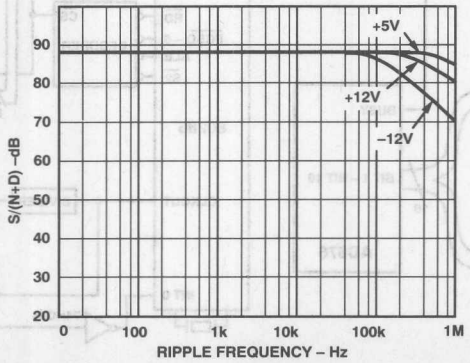


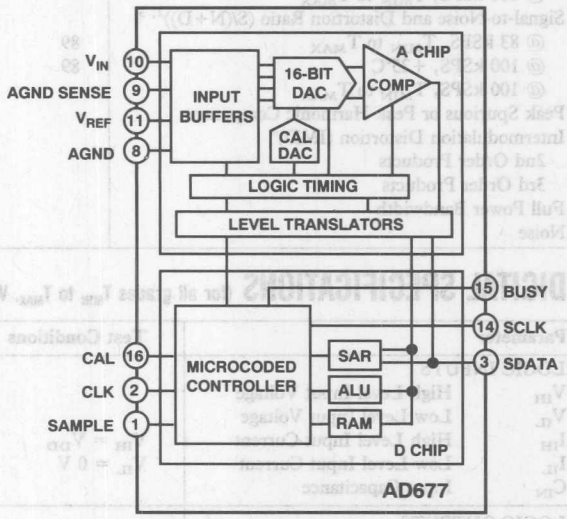
Figure 16. AC Power Supply Rejection (f_{IN} = 1.06 kHz)
f_{SAMPLE} = 96 kSPS, V_{RIPPLE} = 0.13 V p–p

16-Bit 100 kSPS Sampling ADC

AD677

FEATURES
Autocalibrating
On-Chip Sample-Hold Function
Serial Output
16 Bits No Missing Codes
±1 LSB INL
−99 dB THD
92 dB S/(N+D)
1 MHz Full Power Bandwidth

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD677 is a multipurpose 16-bit serial output analog-to-digital converter which utilizes a switched-capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 μs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The AD677 circuitry is segmented onto two monolithic chips—a digital control chip fabricated on Analog Devices DSP CMOS process and an analog ADC chip fabricated on our BiMOS II process. Both chips are contained in a single package.

The AD677 is specified for ac (or "dynamic") parameters such as S/(N+D) Ratio, THD and IMD which are important in signal processing applications. In addition, dc parameters are specified which are important in measurement applications.

The AD677 operates from +5 V and ±12 V supplies and typically consumes 450 mW using a 10 V reference (360 mW with 5 V reference) during conversion. The digital supply (V_{DD}) is separated from the analog supplies (V_{CC}, V_{EE}) for reduced digital crosstalk. An analog ground sense is provided to remotely sense the ground potential of the signal source. This can be useful if the signal has to be carried some distance to the A/D converter. Separate analog and digital grounds are also provided.

The AD677 is available in a 16-pin narrow plastic DIP, 16-pin narrow side-brazed ceramic package, or 28-lead SOIC. A parallel output version, the AD676, is available in a 28-pin ceramic or plastic DIP. All models operate over a commercial temperature range of 0°C to +70°C or an industrial range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Autocalibration provides excellent dc performance while eliminating the need for user adjustments or additional external circuitry.
2. ±5 V to ±10 V input range ($\pm V_{REF}$).
3. Available in 16-pin 0.3″ skinny DIP or 28-lead SOIC.
4. Easy serial interface to standard ADI DSPs.
5. TTL compatible inputs/outputs.
6. Excellent ac performance: −99 dB THD, 92 dB S/(N+D), peak spurious −101 dB.
7. Industry leading dc performance: 1.0 LSB INL, ±1 LSB full scale and offset.

AD677—SPECIFICATIONS

AC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD677J/A Min	AD677J/A Typ	AD677J/A Max	AD677K/B Min	AD677K/B Typ	AD677K/B Max	Units
Total Harmonic Distortion (THD)[2]							
@ 83 kSPS, T_{MIN} to T_{MAX}		−97	−92		−99	−95	dB
@ 100 kSPS, +25°C		−97	−92		−99	−95	dB
@ 100 kSPS, T_{MIN} to T_{MAX}		−93			−95		dB
Signal-to-Noise and Distortion Ratio (S/(N+D))[2, 3]							
@ 83 kSPS, T_{MIN} to T_{MAX}	89	91		90	92		dB
@ 100 kSPS, +25°C	89	91		90	92		dB
@ 100 kSPS, T_{MIN} to T_{MAX}		89			90		dB
Peak Spurious or Peak Harmonic Component		−101			−101		dB
Intermodulation Distortion (IMD)[4]							
2nd Order Products		−102			−102		dB
3rd Order Products		−98			−98		dB
Full Power Bandwidth		1			1		MHz
Noise		160			160		μV rms

DIGITAL SPECIFICATIONS (for all grades T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.0		V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage		−0.3		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = V_{DD}$	−10		+10	μA
I_{IL}	Low Level Input Current	V_{IL} = 0 V	−10		+10	μA
C_{IN}	Input Capacitance			10		pF
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	V_{DD} − 1 V			V
		= 0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA			0.4	V

NOTES

[1]V_{REF} = 10.0 V, Conversion Rate = 100 kSPS, f_{IN} = 1.0 kHz, V_{IN} = −0.05 dB, Bandwidth = 50 kHz unless otherwise indicated. All measurements referred to a 0 dB (20 V p-p) input signal. Values are post-calibration.

[2]For other input amplitudes, refer to Figure 12.

[3]For dynamic performance with different voltage reference values see Figure 11.

[4]fa = 1008 Hz, fb = 1055 Hz. See Definition of Specifications section and Figure 16.

Specifications subject to change without notice.

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

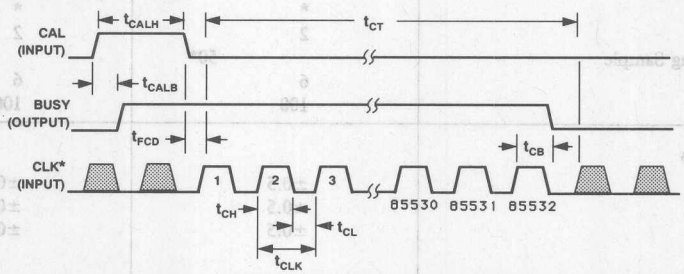
Parameter	AD677J/A Min	AD677J/A Typ	AD677J/A Max	AD677K/B Min	AD677K/B Typ	AD677K/B Max	Units
TEMPERATURE RANGE							
J, K Grades	0		+70	0		+70	°C
A, B Grades	−40		+85	−40		+85	°C
ACCURACY							
Resolution	16			16			Bits
Integral Nonlinearity (INL)							
@ 83 kSPS, T_{MIN} to T_{MAX}		±1			±1	±1.5	LSB
@ 100 kSPS, +25°C		±1			+1	±1.5	LSB
@ 100 kSPS, T_{MIN} to T_{MAX}		±2			±2		LSB
Differential Nonlinearity (DNL)—No Missing Codes		16		16			Bits
Bipolar Zero Error[2]		±2	±4		±1	±3	LSB
Positive, Negative FS Errors[2]							
@ 83 kSPS		±2	±4		±1	±3	LSB
@ 100 kSPS, +25°C		±2	±4		±1	±3	LSB
@ 100 kSPS		±4			±4		LSB
TEMPERATURE DRIFT[3]							
Bipolar Zero		±0.5			±0.5		LSB
Positive Full Scale		±0.5			±0.5		LSB
Negative Full Scale		±0.5			±0.5		LSB
VOLTAGE REFERENCE INPUT RANGE[4] (V_{REF})	5		10	5		10	V
ANALOG INPUT[5]							
Input Range (V_{IN})			±V_{REF}			±V_{REF}	V
Input Impedance		*			*		
Input Settling Time		2			2		µs
Input Capacitance During Sample			50*			50*	pF
Aperture Delay		6			6		ns
Aperture Jitter		100			100		ps
POWER SUPPLIES							
Power Supply Rejection[6]							
V_{CC} = +12 V ± 5%		±0.5			±0.5		LSB
V_{EE} = −12 V ± 5%		±0.5			±0.5		LSB
V_{DD} = +5 V ± 10%		±0.5			±0.5		LSB
Operating Current							
V_{REF} = +5 V							
I_{CC}		14.5	18		14.5	18	mA
I_{EE}		14.5	18		14.5	18	−mA
I_{DD}		3	5		3	5	mA
Power Consumption		360	480		360	480	mW
V_{REF} = +10 V							
I_{CC}		18	24		18	24	mA
I_{EE}		18	24		18	24	−mA
I_{DD}		3	5		3	5	mA
Power Consumption		450	630		450	630	mW

NOTES
[1]V_{REF} = 10.0 V, Conversion Rate = 100 kSPS unless otherwise noted. Values are post-calibration.
[2]Values shown apply to any temperature from T_{MIN} to T_{MAX} after calibration at that temperature at nominal supplies.
[3]Values shown are based upon calibration at +25°C with no additional calibration at temperature. Values shown are the typical variation from the value at +25°C.
[4]See "APPLICATIONS" section for recommended voltage reference circuit, and Figure 11 for dynamic performance with other reference voltage values.
[5]See "APPLICATIONS" section for recommended input buffer circuit.
[6]Typical deviation of bipolar zero, −full scale on +full scale from min to max rating.
*For explanation of input characteristics, see "ANALOG INPUT" section.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

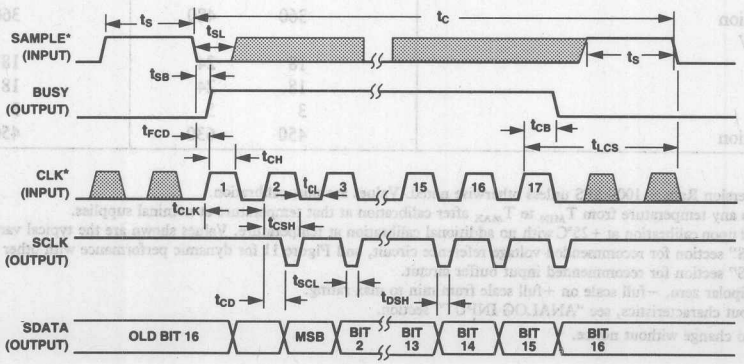
Parameter	Symbol	Min	Typ	Max	Units
Conversion Period[2, 3]	t_C	10		1000	µs
CLK Period[4]	t_{CLK}	480			ns
Calibration Time	t_{CT}			85532	t_{CLK}
Sampling Time	t_S	2			µs
Last CLK to SAMPLE Delay[5]	t_{LCS}	2.1			µs
SAMPLE Low	t_{SL}	100			ns
SAMPLE to Busy Delay	t_{SB}		30	75	ns
1st CLK Delay	t_{FCD}	50			ns
CLK Low[6]	t_{CL}	50			ns
CLK High[6]	t_{CH}	50			ns
CLK to BUSY Delay	t_{CB}		180	300	ns
CLK to SDATA Valid	t_{CD}	50	100	175	ns
CLK to SCLK High	t_{CSH}	100	180	300	ns
SCLK Low	t_{SCL}	50	80		ns
SDATA to SCLK High	t_{DSH}	50	80		ns
CAL High Time	t_{CALH}	50			ns
CAL to BUSY Delay	t_{CALB}		15	50	ns

NOTES
[1]See the "CONVERSION CONTROL" and "AUTOCALIBRATION" sections for detailed explanations of the above timing.
[2]Depends upon external clock frequency; includes acquisition time and conversion time. The maximum conversion period is specified to account for the droop of the internal sample/hold function. Operation at slower rates may degrade performance.
[3]$t_C = t_{FCD} + 16 \times t_{CLK} + t_{LCS}$
[4]580 ns is recommended for optimal accuracy over temperature (not necessary during calibration cycle).
[5]If SAMPLE goes high before the 17th CLK pulse, the device will start sampling approximately 100 ns after the rising edge of the 17th CLK pulse.
[6]$t_{CH} + t_{CL} = t_{CLK}$ and must be greater than 480 ns.



*SHADED PORTIONS OF INPUT SIGNALS ARE OPTIONAL. FOR BEST PERFORMANCE, WE RECOMMEND THAT THESE SIGNALS BE HELD LOW EXCEPT WHEN EXPLICITY SHOWN HIGH.

Figure 1. Calibration Timing



*SHADED PORTIONS OF INPUT SIGNALS ARE OPTIONAL. FOR BEST PERFORMANCE, WE RECOMMEND THAT THESE SIGNALS BE HELD LOW EXCEPT WHEN EXPLICITY SHOWN HIGH.

Figure 2. General Conversion Timing

ORDERING GUIDE

Model	Temperature Range	S/(N+D)	Max INL	Package Description	Package Option*
AD677JN	0°C to +70°C	89 dB	Typ Only	Plastic 16-Pin DIP	N-16
AD677KN	0°C to +70°C	90 dB	±1.5 LSB	Plastic 16-Pin DIP	N-16
AD677JD	0°C to +70°C	89 dB	Typ Only	Ceramic 16-Pin DIP	D-16
AD677KD	0°C to +70°C	90 dB	±1.5 LSB	Ceramic 16-Pin DIP	D-16
AD677JR	0°C to +70°C	89 dB	Typ Only	Plastic 28-Lead SOIC	R-28
AD677KR	0°C to +70°C	90 dB	±1.5 LSB	Plastic 28-Lead SOIC	R-28
AD677AD	−40°C to +85°C	89 dB	Typ Only	Ceramic 16-Pin DIP	D-16
AD677BD	−40°C to +85°C	90 dB	±1.5 LSB	Ceramic 16-Pin DIP	D-16

*D = Ceramic DIP; N = Plastic DIP; R = Small Outline IC (SOIC). For outline information see Package Information section.

2

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to V_{EE} . . . . . −0.3 V to +26.4 V
V_{DD} to DGND . . . . . −0.3 V to +7 V
V_{CC} to AGND . . . . . −0.3 V to +18 V
V_{EE} to AGND . . . . . −18 V to +0.3 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . 0 to +5.5 V
Analog Inputs, V_{REF} to AGND
. . . . . (V_{CC} +0.3 V) to (V_{EE} −0.3 V)
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . −65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

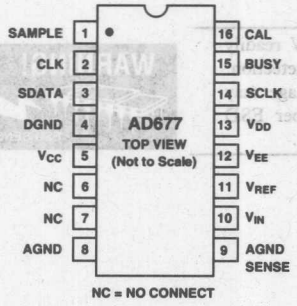
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD677 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

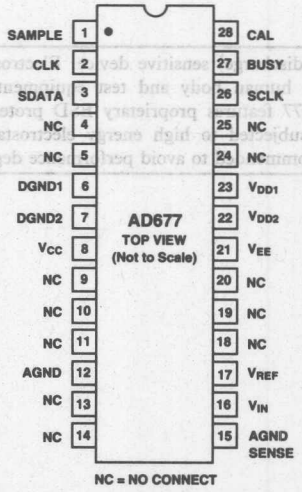
PIN DESCRIPTION

DIP Pin	SOIC Pin	Type	Name	Description
1	1	SAMPLE	DI	V_{IN} Acquisition Control Pin. Active HIGH. During conversion, SAMPLE controls the state of the internal sample-hold amplifier and the falling edge initiates conversion. During calibration, SAMPLE should be held LOW. If HIGH during calibration, diagnostic information will appear on SDATA.
2	2	CLK	DI	Master Clock Input. The AD677 requires 17 clock pulses to execute a conversion. CLK is also used to derive SCLK.
3	3	SDATA	DO	Serial Output Data Controlled by SCLK.
4	6, 7	DGND	P	Digital Ground.
5	8	V_{CC}	P	+12 V Analog Supply Voltage.
8	12	AGND	P	Analog Ground.
9	15	AGND SENSE	AI	Analog Ground Sense.
10	16	V_{IN}	AI	Analog Input Voltage.
11	17	V_{REF}	A1	External Voltage Reference Input.
12	21	V_{EE}	P	−12 V Analog Supply Voltage.
13	22, 23	V_{DD}	P	+5 V Logic Supply Voltage.
14	26	SCLK	DO	Clock Output for Data Read, derived from CLK.
15	27	BUSY	DO	Status Line for Converter. Active HIGH, indicating a conversion or calibration in progress.
16	28	CAL	DI	Calibration Control Pin.
6, 7	4, 5, 9, 10, 11, 13, 14, 18, 19, 20, 24, 25	NC	–	No Connection. No connections should be made to these pins.

Type: AI = Analog Input
DI = Digital Input
DO = Digital Output
P = Power



DIP Pinout



SOIC Pinout

NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist frequency" of a converter is that input frequency which is one half the sampling frequency of the converter.

TOTAL HARMONIC DISTORTION
Total harmonic distortion (THD) is the ratio of the rms sum of the harmonic components to the rms value of a full-scale input signal and is expressed in percent (%) or decibels (dB). For input signals or harmonics that are above the Nyquist frequency, the aliased components are used.

SIGNAL-TO-NOISE PLUS DISTORTION RATIO
Signal-to-noise plus distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

+/– FULL-SCALE ERROR
The last + transition (from 011 . . . 10 to 011 . . . 11) should occur for an analog voltage 1.5 LSB below the nominal full scale (4.99977 volts for a ±5 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

BIPOLAR ZERO ERROR
Bipolar zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are one LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

INTEGRAL NONLINEARITY (INL)
The ideal transfer function for an ADC is a straight line bisecting the center of each code drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the most negative code transition. "Full scale" is defined as a level 1.5 LSB beyond the most positive code transition. Integral nonlinearity is the worst-case deviation of a code center average from the straight line.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb), and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude, and the peak value of their sum is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

APERTURE DELAY
Aperture delay is the time required after SAMPLE pin is taken LOW for the internal sample-hold of the AD677 to open, thus holding the value of V_{IN}.

APERTURE JITTER
Aperture jitter is the variation in the aperture delay from sample to sample.

POWER SUPPLY REJECTION
DC variations in the power supply voltage will affect the overall transfer function of the ADC, resulting in zero error and full-scale error changes. Power supply rejection is the maximum change in either the bipolar zero error or full-scale error value. Additionally, there is another power supply variation to consider. AC ripple on the power supplies can couple noise into the ADC, resulting in degradation of dynamic performance. This is displayed in Figure 15.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

NOISE/DC CODE UNCERTAINTY
Ideally, a fixed dc input should result in the same output code for repetitive conversions. However, as a consequence of unavoidable circuit noise within the wideband circuits in the ADC, there is a range of output codes which may occur for a given input voltage. If you apply a dc signal to the ADC and record a large number of conversions, the result will be a distribution of codes. If you fit a Gaussian probability distribution to the histogram, the standard deviation is approximately equivalent to the rms input noise of the ADC.

The AD677 is a multipurpose 16-bit analog-to-digital converter and includes circuitry which performs an input sample/hold function, ground sense, and autocalibration. These functions are segmented onto two monolithic chips—an analog signal processor and a digital controller. Both chips are contained within the AD677 package.

The AD677 employs a successive-approximation technique to determine the value of the analog input voltage. However, instead of the traditional laser-trimmed resistor-ladder approach, this device uses a capacitor-array, charge redistribution technique. Binary-weighted capacitors subdivide the input sample to perform the actual analog-to-digital conversion. The capacitor array eliminates variation in the linearity of the device due to temperature-induced mismatches of resistor values. Since a capacitor array is used to perform the data conversions, the sample/hold function is included without the need for additional external circuitry.

Initial errors in capacitor matching are eliminated by an autocalibration circuit within the AD677. This circuit employs an on-chip microcontroller and a calibration DAC to measure and compensate capacitor mismatch errors. As each error is determined, its value is stored in on-chip memory (RAM). Subsequent conversions use these RAM values to improve conversion accuracy. The autocalibration routine may be invoked at any time. Autocalibration insures high performance while eliminating the need for any user adjustments and is described in detail below.

The microcontroller controls all of the various functions within the AD677. These include the actual successive approximation algorithm, the autocalibration routine, the sample/hold operation, and the internal output data latch.

AUTOCALIBRATION

The AD677 achieves rated performance without the need for user trims or adjustments. This is accomplished through the use of on-chip autocalibration.

In the autocalibration sequence, sample/hold offset is nulled by internally connecting the input circuit to the ground sense circuit. The resulting offset voltage is measured and stored in RAM for later use. Next, the capacitor representing the most significant bit (MSB) is charged to the reference voltage. This charge is then transferred to a capacitor of equal size (composed of the sum of the remaining lower weight bits). The voltage that results represents the amount of capacitor mismatch. A calibration digital-to-analog converter (DAC) adds an appropriate value of error correction voltage to cancel this mismatch. This correction factor is also stored in RAM. This process is repeated for each of the eight remaining capacitors representing the top nine bits. The accumulated values in RAM are then used during subsequent conversions to adjust conversion results accordingly.

As shown in Figure 1, when CAL is taken HIGH the AD677 internal circuitry is reset, the BUSY pin is driven HIGH, and the ADC prepares for calibration. This is an asynchronous hardware reset and will interrupt any conversion or calibration currently in progress. Actual calibration begins when CAL is taken LOW and completes in 85,532 clock cycles, indicated by BUSY going LOW. During calibration, it is preferable for SAMPLE to appear on SDATA. This data is of no value to the user.

In most applications, it is sufficient to calibrate the AD677 only upon power-up, in which case care should be taken that the power supplies and voltage reference have stabilized first. If calibration is not performed, the AD677 may come up in an unknown state, or performance could degrade to as low as 10 bits.

CONVERSION CONTROL

The AD677 is controlled by two signals: SAMPLE and CLK, as shown in Figure 2. It is assumed that the part has been calibrated and the digital I/O pins have the levels shown at the start of the timing diagram.

A conversion consists of an input acquisition followed by 17 clock pulses which execute the 16-bit internal successive approximation routine. The analog input is acquired by taking the SAMPLE line HIGH for a minimum sampling time of t_S. The actual sample taken is the voltage present on V_{IN} one aperture delay after the SAMPLE line is brought LOW, assuming the previous conversion has completed (signified by BUSY going LOW). Care should be taken to ensure that this negative edge is well defined and jitter free in ac applications to reduce the uncertainty (noise) in signal acquisition. With SAMPLE going LOW, the AD677 commits itself to the conversion—the input at V_{IN} is disconnected from the internal capacitor array, BUSY goes HIGH, and the SAMPLE input will be ignored until the conversion is completed (when BUSY goes LOW). SAMPLE must be held LOW for a minimum period of time t_{SL}. A period of time t_{FCD} after bringing SAMPLE LOW, the 17 CLK cycles are applied; CLK pulses that start before this period of time are ignored. BUSY goes HIGH t_{SB} after SAMPLE goes LOW, signifying that a conversion is in process, and remains HIGH until the conversion is completed. As indicated in Figure 2, the twos complement output data is presented MSB first. This data may be captured with the rising edge of SCLK or the falling edge of CLK, beginning with pulse #2. The AD677 will ignore CLK after BUSY has gone LOW and SDATA or SCLK will not change until a new sample is acquired.

CONTINUOUS CONVERSION

For maximum throughput rate, the AD677 can be operated in a continuous convert mode. This is accomplished by utilizing the fact that SAMPLE will no longer be ignored after BUSY goes LOW, so an acquisition may be initiated even during the HIGH time of the 17th CLK pulse for maximum throughput rate while enabling full settling of the sample/hold circuitry. If SAMPLE is already HIGH during the rising edge of the 17th CLK, then an acquisition is immediately initiated approximately 100 ns after the rising edge of the 17th clock pulse.

Care must be taken to adhere to the minimum/maximum timing requirements in order to preserve conversion accuracy.

GENERAL CONVERSION GUIDELINES

During signal acquisition and conversion, care should be taken with the logic inputs to avoid digital feedthrough noise. It is possible to run CLK continuously, even during the sample period. However, CLK edges during the sampling period, and especially when SAMPLE goes LOW, may inject noise into the sampling process. The AD677 is tested with no CLK cycles during the sampling period. The BUSY signal can be used to prevent the clock from running during acquisition, as illustrated

in Figure 3. In this circuit BUSY is used to reset the circuitry which divides the system clock down to provide the AD677 CLK. This serves to interrupt the clock until after the input signal has been acquired, which has occurred when BUSY goes HIGH. When the conversion is completed and BUSY goes LOW, the circuit in Figure 3 truncates the 17th CLK pulse width which is tolerable because only its rising edge is critical.

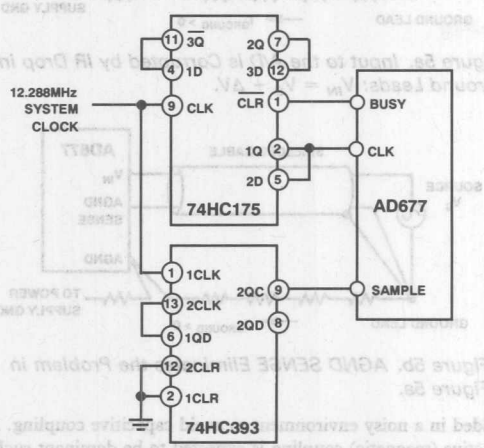


Figure 3.

Figure 3 also illustrates the use of a counter (74HC393) to derive the AD677 SAMPLE command from the system clock when a continuous convert mode is desirable. Pin 9 (2QC) provides a 96 kHz sample rate for the AD677 when used with a 12.288 MHz system clock. Alternately, Pin 8 (2QD) could be used for a 48 kHz rate.

If a continuous clock is used, then the user must avoid CLK edges at the instant of disconnecting V_{IN} which occurs at the falling edge of SAMPLE (see t_{FCD} specification). The duty cycle of CLK may vary, but both the HIGH (t_{CH}) and LOW (t_{CL}) phases must conform to those shown in the timing specifications. The internal comparator makes its decisions on the rising edge of CLK. To avoid a negative edge transition disturbing the comparator's settling, t_{CL} should be at least half the value of t_{CLK}. It is not recommended that the SAMPLE pin change state toward the end of a CLK cycle, in order to avoid transitions disturbing the internal comparator's settling.

During a conversion, internal dc error terms such as comparator voltage offset are sampled, stored on internal capacitors and used to correct for their corresponding errors when needed. Because these voltages are stored on capacitors, they are subject to leakage decay and so require refreshing. For this reason there is a maximum conversion time t_C (1000 μs). From the time SAMPLE goes HIGH to the completion of the 17th CLK pulse, no more than 1000 μs should elapse for specified performance. However, there is no restriction to the maximum time between individual conversions.

Output coding for the AD677 is twos complement as shown in Table I. The AD677 is designed to limit output coding in the event of out-of-range input.

Table I. Serial Output Coding Format (Twos Complement)

V_{IN}	Output Code
<Full Scale	011 . . . 11
Full Scale	011 . . . 11
Full Scale − 1 LSB	011 . . . 10
Midscale + 1 LSB	000 . . . 01
Midscale	000 . . . 00
Midscale − 1 LSB	111 . . . 11
−Full Scale + 1 LSB	100 . . . 01
−Full Scale	100 . . . 00
<−Full Scale	100 . . . 00

POWER SUPPLIES AND DECOUPLING

The AD677 has three power supply input pins. V_{CC} and V_{EE} provide the supply voltages to operate the analog portions of the AD677 including the capacitor DAC, input buffers and comparator. V_{DD} provides the supply voltage which operates the digital portions of the AD677 including the data output buffers and the autocalibration controller.

As with most high performance linear circuits, changes in the power supplies can produce undesired changes in the performance of the circuit. Optimally, well regulated power supplies with less than 1% ripple should be selected. The ac output impedance of a power supply is a complex function of frequency, and in general will increase with frequency. In other words, high frequency switching such as that encountered with digital circuitry requires fast transient currents which most power supplies cannot adequately provide. This results in voltage spikes on the supplies. If these spikes exceed the ±5% tolerance of the ±12 V supplies or the ±10% limits of the +5 V supply, ADC performance will degrade. Additionally, spikes at frequencies higher than 100 kHz will also degrade performance. To compensate for the finite ac output impedance of the supplies, it is necessary to store "reserves" of charge in bypass capacitors. These capacitors can effectively lower the ac impedance presented to the AD677 power inputs which in turn will significantly reduce the magnitude of the voltage spikes. For bypassing to be effective, certain guidelines should be followed. Decoupling capacitors, typically 0.1 μF, should be placed as closely as possible to each power supply pin of the AD677. It is essential that these capacitors be placed physically close to the IC to minimize the inductance of the PCB trace between the capacitor and the supply pin. The logic supply (V_{DD}) should be decoupled to digital common and the analog supplies (V_{CC} and V_{EE}) to analog common. The reference input is also considered as a power supply pin in this regard and the same decoupling procedures apply. These points are displayed in Figure 4.

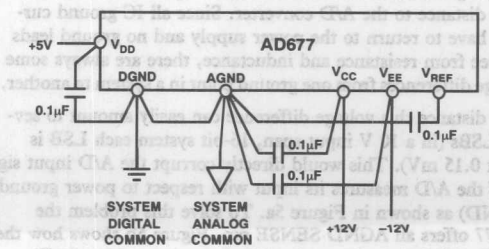


Figure 4. Grounding and Decoupling the AD677

Additionally, it is beneficial to have large capacitors (>47 μF) located at the point where the power connects to the PCB with 10 μF capacitors located in the vicinity of the ADC to further reduce low frequency ripple. In systems that will be subjected to particularly harsh environmental noise, additional decoupling may be necessary. RC-filtering on each power supply combined with dedicated voltage regulation can substantially decrease power supply ripple effects (this is further detailed in Figure 7).

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 4 LSBs at the 16-bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals.

Analog and digital signals should not share a common return path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point at the AD677 to minimize interference between analog and digital circuitry. Analog signals should be routed as far as possible from digital signals and should cross them, if at all, only at right angles. A solid analog ground plane around the AD677 will isolate it from large switching ground currents. For these reasons, the use of wire wrap circuit construction will not provide adequate performance; careful printed circuit board construction is preferred.

GROUNDING

The AD677 has three grounding pins, designated ANALOG GROUND (AGND), DIGITAL GROUND (DGND) and ANALOG GROUND SENSE (AGND SENSE). The analog ground pin is the "high quality" ground reference point for the device, and should be connected to the analog common point in the system.

AGND SENSE is intended to be connected to the input signal ground reference point. This allows for slight differences in level between the analog ground point in the system and the input signal ground point. However no more than 100 mV is recommended between the AGND and the AGND SENSE pins for specified performance.

Using AGND SENSE to remotely sense the ground potential of the signal source can be useful if the signal has to be carried some distance to the A/D converter. Since all IC ground currents have to return to the power supply and no ground leads are free from resistance and inductance, there are always some voltage differences from one ground point in a system to another.

Over distance this voltage difference can easily amount to several LSBs (in a 10 V input span, 16-bit system each LSB is about 0.15 mV). This would directly corrupt the A/D input signal if the A/D measures its input with respect to power ground (AGND) as shown in Figure 5a. To solve this problem the AD677 offers an AGND SENSE pin. Figure 5b shows how the AGND SENSE can be used to eliminate the problem in Figure 5a. Figure 5b also shows how the signal wires should be

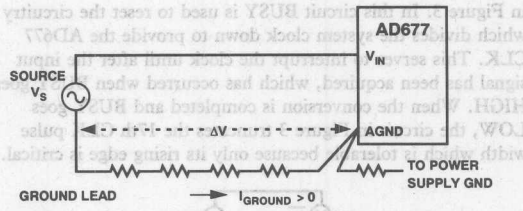


Figure 5a. Input to the A/D Is Corrupted by IR Drop in Ground Leads: $V_{IN} = V_S + \Delta V$.

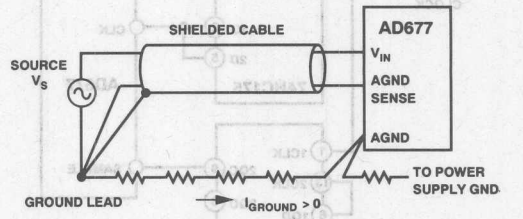


Figure 5b. AGND SENSE Eliminates the Problem in Figure 5a.

shielded in a noisy environment to avoid capacitive coupling. If inductive (magnetic) coupling is expected to be dominant such as where motors are present, twisted-pair wires should be used instead.

The digital ground pin is the reference point for all of the digital signals that operate the AD677. This pin should be connected to the digital common point in the system. As Figure 4 illustrated, the analog and digital grounds should be connected together at one point in the system, preferably at the AD677.

VOLTAGE REFERENCE

The AD677 requires the use of an external voltage reference. The input voltage range is determined by the value of the reference voltage; in general, a reference voltage of n volts allows an input range of ±n volts. The AD677 is specified for a voltage reference between +5 V and +10 V. A 10 V reference will typically require support circuitry operated from ±15 V supplies; a 5.0 V reference may be used with ±12 V supplies. Signal-to-noise performance is increased proportionately with input signal range (see Figure 12). In the presence of a fixed amount of system noise, increasing the LSB size (which results from increasing the reference voltage) will increase the effective S/(N+D) performance. Figure 11 illustrates S/(N+D) as a function of reference voltage. In contrast, dc accuracy will be optimal at lower reference voltage values (such as 5 V) due to capacitor nonlinearity at higher voltage values.

During a conversion, the switched capacitor array of the AD677 presents a dynamically changing current load at the voltage reference as the successive-approximation algorithm cycles through various choices of capacitor weighting. (See the following section "Analog Input" for a detailed discussion of the V_{REF} input characteristics.) The output impedance of the reference circuitry must be low so that the output voltage will remain sufficiently constant as the current drive changes. In some applications, this may require that the output of the voltage reference be buffered by an amplifier with low impedance at relatively high frequencies. In choosing a voltage reference, consideration should be

made for selecting one with low noise. A capacitor connected between REF IN and AGND will reduce the demands on the reference by decreasing the magnitude of high frequency components required to be sourced by the reference.

Figures 6 and 7 represent typical design approaches.

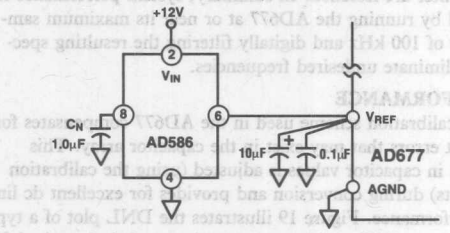


Figure 6.

Figure 6 shows a voltage reference circuit featuring the 5 V output AD586. The AD586 is a low cost reference which utilizes a buried Zener architecture to provide low noise and drift. Over the 0°C to +70°C range, the AD586M grade exhibits less than 1.0 mV output change from its initial value at +25°C. A noise-reduction capacitor, C_N, reduces the broadband noise of the AD586 output, thereby optimizing the overall performance of the AD677. It is recommended that a 10 μF to 47 μF high quality tantalum capacitor and a 0.1 μF capacitor be tied between the V_{REF} input of the AD677 and ground to minimize the impedance on the reference.

Using the AD677 with ±10 V input range (V_{REF} = 10 V) typically requires ±15 V supplies to drive op amps and the voltage reference. If ±12 V is not available in the system, regulators such as 78L12 and 79L12 can be used to provide power for the AD677. This is also the recommended approach (for any input range) when the ADC system is subjected to harsh environments such as where the power supplies are noisy and where voltage spikes are present. Figure 7 shows an example of such a system based upon the 10 V AD587 reference, which provides a 300 μV LSB. Circuitry for additional protection against power supply disturbances has been shown. A 100 μF capacitor at each

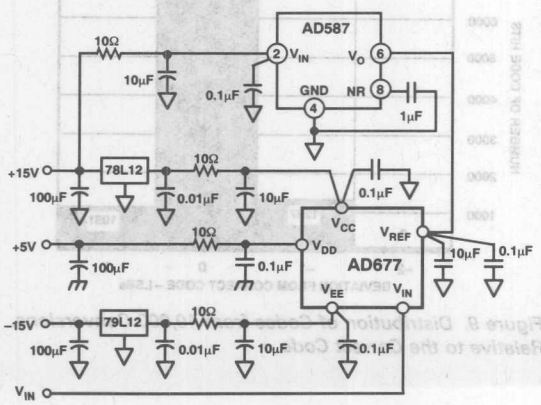


Figure 7.

regulator prevents very large voltage spikes from entering the regulators. Any power line noise which the regulators cannot eliminate will be further filtered by an RC filter (10 Ω/10 μF) having a −3 dB point at 1.6 kHz. For best results the regulators should be within a few centimeters of the AD677.

ANALOG INPUT

As previously discussed, the analog input voltage range for the AD677 is $\pm V_{REF}$. For purposes of ground drop and common mode rejection, the V_{IN} and V_{REF} inputs each have their own ground. V_{REF} is referred to the local analog system ground (AGND), and V_{IN} is referred to the analog ground sense pin (AGND SENSE) which allows a remote ground sense for the input signal.

The AD677 analog inputs (V_{IN}, V_{REF} and AGND SENSE) exhibit dynamic characteristics. When a conversion cycle begins, each analog input is connected to an internal, discharged 50 pF capacitor which then charges to the voltage present at the corresponding pin. The capacitor is disconnected when SAMPLE is taken LOW, and the stored charge is used in the subsequent conversion. In order to limit the demands placed on the external source by this high initial charging current, an internal buffer amplifier is employed between the input and this capacitance for a few hundred nanoseconds. During this time the input pin exhibits typically 20 kΩ input resistance, 10 pF input capacitance and ±40 μA bias current. Next, the input is switched directly to the now precharged capacitor and allowed to fully settle. During this time the input sees only a 50 pF capacitor. Once the sample is taken, the input is internally floated so that the external input source sees a very high input resistance and a parasitic input capacitance of typically only 2 pF. As a result, the only dominant input characteristic which must be considered is the high current steps which occur when the internal buffers are switched in and out.

In most cases, these characteristics require the use of an external op amp to drive the input of the AD677. Care should be taken with op amp selection; even with modest loading conditions, most available op amps do not meet the low distortion requirements necessary to match the performance capabilities of the AD677. Figure 8 represents a circuit, based upon the AD845, which will provide excellent overall performance.

For applications optimized more for low distortion and low noise, the AD845 of Figure 8 may be replaced by the AD743.

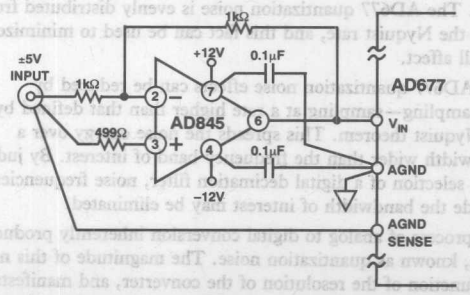


Figure 8.

AC parameters, which include S/(N+D), THD, etc., reflect the AD677's effect on the spectral content of the analog input signal. Figures 11 through 18 provide information on the AD677's ac performance under a variety of conditions.

A perfect n-bit ADC with no errors will yield a theoretical quantization noise of $q/\sqrt{12}$, where q is the weight of the LSB. This relationship leads to the well-known equation for theoretical full-scale rms sine wave signal-to-noise plus distortion level of $S/(N + D) = 6.02\ n + 1.76$ dB, here n is the bit resolution. An actual ADC, however, will yield a measured S/(N + D) less than the theoretical value. Solving this equation for n using the measured S/(N + D) value yields the equation for effective number of bits (ENOB):

$$ENOB = \frac{[S/(N + D)]_{ACTUAL} - 1.76\ dB}{6.02}$$

As a general rule, averaging the results from several conversions reduces the effects of noise, and therefore improves such parameters as S/(N+D). AD677 performance may be optimized by operating the device at its maximum sample rate of 100 kSPS and digitally filtering the resulting bit stream to the desired signal bandwidth. This succeeds in distributing noise over a wider frequency range, thus reducing the noise density in the frequency band of interest. This subject is discussed in the following section.

OVERSAMPLING AND NOISE FILTERING

The Nyquist rate for a converter is defined as one-half its sampling rate. This is established by the Nyquist theorem, which requires that a signal be sampled at a rate corresponding to at least twice its highest frequency component of interest in order to preserve the informational content. Oversampling is a conversion technique in which the sampling frequency is more than twice the frequency bandwidth of interest. In audio applications, the AD677 can operate at a 2 × F_S oversampling rate, where F_S = 48 kHz.

In quantized systems, the informational content of the analog input is represented in the frequency spectrum from dc to the Nyquist rate of the converter. Within this same spectrum are higher frequency noise and signal components. Antialias, or low pass, filters are used at the input to the ADC to reduce these noise and signal components so that their aliased components do not corrupt the baseband spectrum. However, wideband noise contributed by the AD677 will not be reduced by the antialias filter. The AD677 quantization noise is evenly distributed from dc to the Nyquist rate, and this fact can be used to minimize its overall affect.

The AD677 quantization noise effects can be reduced by oversampling—sampling at a rate higher than that defined by the Nyquist theorem. This spreads the noise energy over a bandwidth wider than the frequency band of interest. By judicious selection of a digital decimation filter, noise frequencies outside the bandwidth of interest may be eliminated.

The process of analog to digital conversion inherently produces noise, known as quantization noise. The magnitude of this noise is a function of the resolution of the converter, and manifests itself as a limit to the theoretical signal-to-noise ratio achievable. This limit is described by $S/(N+D) = (6.02n + 1.76 + 10 \log F_S/2F_A)$ dB, where n is the resolution of the converter in bits, interest. For audio bandwidth applications, the AD677 is capable of operating at a 2 × oversample rate (96 kSPS), which typically produces an improvement in S/(N+D) of 3 dB compared with operating at the Nyquist conversion rate of 48 kSPS. Oversampling has another advantage as well; the demands on the antialias filter are lessened. In summary, system performance is optimized by running the AD677 at or near its maximum sampling rate of 100 kHz and digitally filtering the resulting spectrum to eliminate undesired frequencies.

DC PERFORMANCE

The self-calibration scheme used in the AD677 compensates for bit weight errors that may exist in the capacitor array. This mismatch in capacitor values is adjusted (using the calibration coefficients) during conversion and provides for excellent dc linearity performance. Figure 19 illustrates the DNL plot of a typical AD677 at +25°C. A histogram test is a statistical method for deriving an A/D converter's differential nonlinearity. A ramp input is sampled by the ADC and a large number of conversions are taken and stored. Theoretically the codes would all be the same size and, therefore, have an equal number of occurrences. A code with an average number of occurrences would have a DNL of "0". A code with more or less than average will have a DNL of greater than or less than zero LSB. A DNL of −1 LSB indicates missing code (zero occurrences).

Figure 20 illustrates the code width distribution of the DNL plots of Figure 19.

DC CODE UNCERTAINTY

Ideally, a fixed dc input should result in the same output code for repetitive conversions. However, as a consequence of unavoidable circuit noise within the wideband circuits in the ADC, there is range of output codes which may occur for a given input voltage. If you apply a dc signal to the AD677 and record 10,000 conversions, the result will be a distribution of codes as shown in Figure 9 (using a 10 V reference). If you fit a Gaussian probability distribution to the histogram, the standard deviation is approximately equivalent to the rms input noise of ADC.

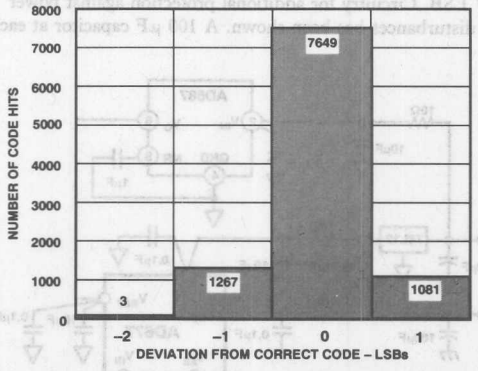


Figure 9. Distribution of Codes from 10,000 Conversions, Relative to the Correct Code

The standard deviation of this distribution is approximately 0.5 LSBs. If less uncertainty is desired, averaging multiple conversions will narrow this distribution by the inverse of the square root of the number of samples; i.e., the average of 4 conversions would have a standard deviation of 0.25 LSBs.

DSP INTERFACE

Figure 10 illustrates the use of the Analog Devices ADSP-2101 digital signal processor with the AD677. The ADSP-2101 FO (flag out) pin of Serial Port 1 (SPORT 1) is connected to the SAMPLE line and is used to control acquisition of data. The ADSP-2101 timer is used to provide precise timing of the FO pin.

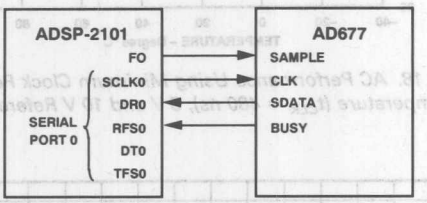


Figure 10. ADSP-2101 Interface

The SCLK pin of the ADSP-2101 SPORT0 provides the CLK input for the AD677. The clock should be programmed to be approximately 2 MHz to comply with AD677 specifications. To minimize digital feedthrough, the clock should be disabled (by setting Bit 14 in SPORT0 control register to 0) during data acquisition. Since the clock floats when disabled, a pull-down resistor of 12 kΩ–15 kΩ should be connected to SCLK to ensure it will be LOW at the falling edge of SAMPLE. To maximize the conversion rate, the serial clock should be enabled immediately after SAMPLE is brought LOW (hold mode).

The AD677 BUSY signal is connected to RF0 to notify SPORT0 when a new data word is coming. SPORT0 should be configured in normal, external, noninverting framing mode and can be programmed to generate an interrupt after the last data bit is received. To maximize the conversion rate, SAMPLE should be brought HIGH immediately after the last data bit is received.

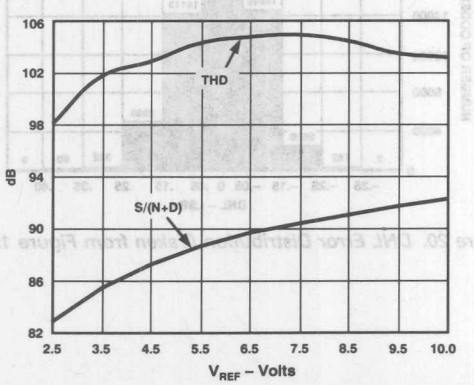


Figure 11.. S/(N+D) and THD vs. V_{REF}, f_S = 100 kHz (Calibration is not guaranteed below +5 V REF)

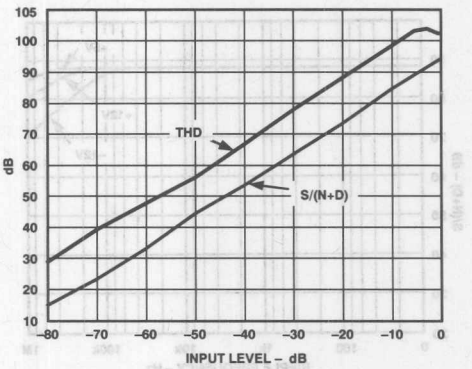


Figure 12. S/(N+D) and THD vs. Input Amplitude, f_S = 100 kHz

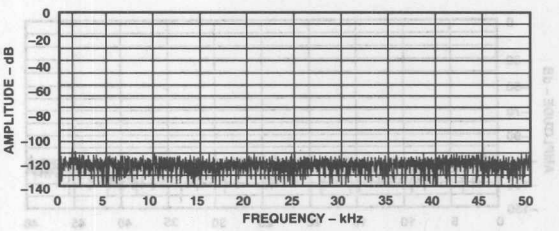


Figure 13. 4096 Point FFT at 100 kSPS, f_{IN} = 1 kHz, V_{REF} = 5 V

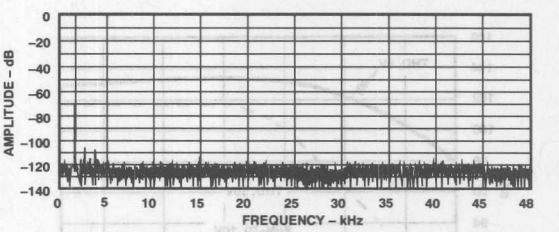


Figure 14. 4096 Point FFT at 100 kSPS, F_{IN} = 1 kHz, V_{REF} = 10 V

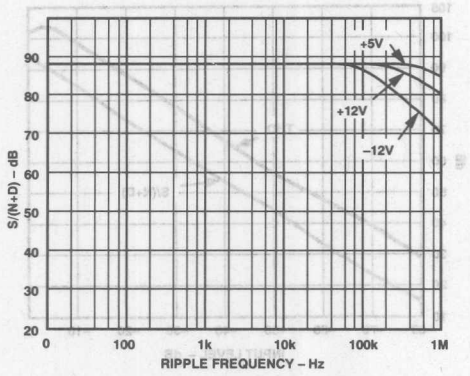


Figure 15. AC Power Supply Rejection (f_{IN} = 1.06 kHz) f_{SAMPLE} = 96 kSPS, V_{RIPPLE} = 0.13 V p-p

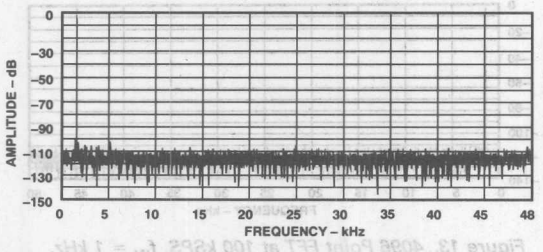


Figure 16. IMD Plot for f_{IN} = 1008 Hz (fa), 1055 Hz (fb) at 96 kSPS

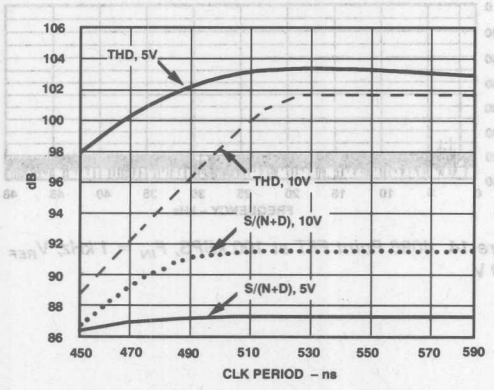


Figure 17. AC Performance vs. Clock Period, T_A = +85°C (5 V and 10 V Reference)

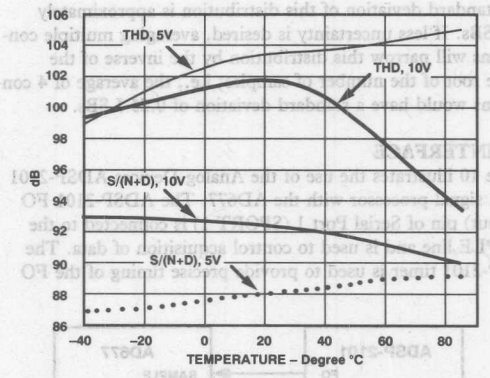


Figure 18. AC Performance Using Minimum Clock Period vs. Temperature (t_{CLK} = 480 ns), 5 V and 10 V Reference

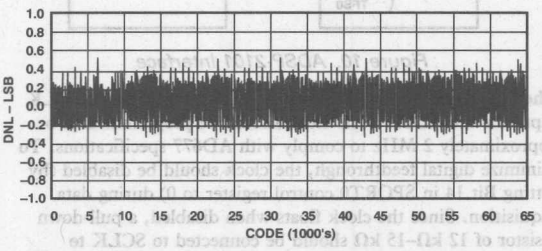


Figure 19. DNL Plot at V_{REF} = 10 V, T_A = +25°C, f_S = 100 kSPS

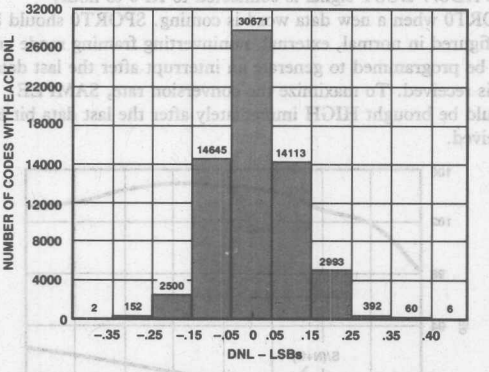


Figure 20. DNL Error Distribution (Taken from Figure 19)

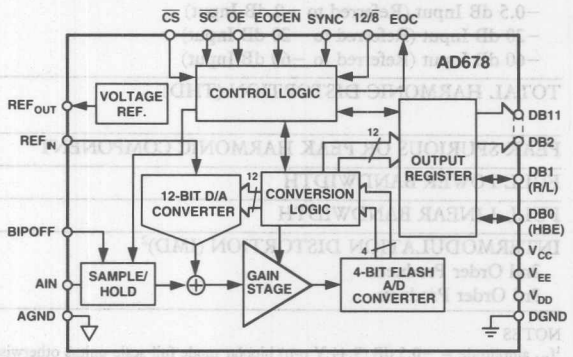
12-Bit 200 kSPS Complete Sampling ADC

AD678*

FEATURES

- AC and DC Characterized and Specified (K, B and T Grades)
- 200k Conversions per Second
- 1 MHz Full Power Bandwidth
- 500 kHz Full Linear Bandwidth
- 72 dB S/N+D (K, B, T Grades)
- Twos Complement Data Format (Bipolar Mode)
- Straight Binary Data Format (Unipolar Mode)
- 10 MΩ Input Impedance
- 8-Bit or 16-Bit Bus Interface
- On-Board Reference and Clock
- 10 V Unipolar or Bipolar Input Range
- Commercial, Industrial and Military Temperature Range Grades
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD678 is a complete, multipurpose 12-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The AD678 is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD which are important in signal processing applications. In addition, the AD678K, B and T grades are fully specified for dc parameters which are important in measurement applications.

The AD678 offers a choice of digital interface formats; the 12 data bits can be accessed by a 16-bit bus in a single read operation or by an 8-bit bus in two read operations (8+4), with right or left justification. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD678 operates from +5 V and ±12 V supplies and dissipates 560 mW (typ). The AD678 is available in 28-pin plastic DIP, ceramic DIP, and 44 J-leaded ceramic surface mount packages.

Screening to MIL-STD-883C Class B is also available.

*Protected by U.S. Patent Nos. 4,804,960; 4,814,767; 4,833,345; 4,250,445; 4,808,908; RE30,586.

PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD678 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. SPECIFICATIONS: The AD678K, B and T grades provide fully specified and tested ac and dc parameters. The AD678J, A and S grades are specified and tested for ac parameters; dc accuracy specifications are shown as typicals. DC specifications (such as INL, gain and offset) are important in control and measurement applications. AC specifications (such as S/N+D ratio, THD and IMD) are of value in signal processing applications.
3. EASE OF USE: The pinout is designed for easy board layout, and the choice of single or two read cycle output provides compatibility with 16- or 8-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
4. RELIABILITY: The AD678 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.
5. UPGRADE PATH: The AD678 provides the same pinout as the 14-bit, 128 kSPS AD679 ADC.
6. The AD678 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD678/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD678—SPECIFICATIONS

AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%, f_{SAMPLE} = 200 kSPS, f_{IN} = 10.06 kHz unless otherwise noted)[1]

Parameter	AD678J/A/S Min	AD678J/A/S Typ	AD678J/A/S Max	AD678K/B/T Min	AD678K/B/T Typ	AD678K/B/T Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO							
−0.5 dB Input (Referred to −0 dB Input)	70	71		72	73		dB
−20 dB Input (Referred to −20 dB Input)		51			53		dB
−60 dB Input (Referred to −60 dB Input)		11			13		dB
TOTAL HARMONIC DISTORTION (THD)		−88	−80		−88	−80	dB
		0.004	0.010		0.004	0.010	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−87	−80		−87	−80	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[2]							
2nd Order Products		−85	−80		−85	−80	dB
3rd Order Products		−90	−80		−90	−80	dB

NOTES

[1] f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a −0 dB (9.997 V p-p) input signal unless otherwise indicated.

[2] f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 200 kSPS.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		2.0	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{DD}	−10	+10	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V	−10	+10	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		0.4	V
I_{OZ}	High Z Leakage Current	V_{IN} = 0 or V_{DD}	−10	+10	μA
C_{OZ}	High Z Output Capacitance			10	pF

Specifications subject to change without notice.

DC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10% unless otherwise indicated)

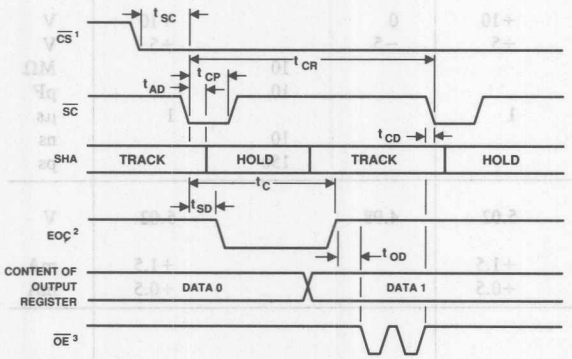
Parameter	AD678J/A/S Min	AD678J/A/S Typ	AD678J/A/S Max	AD678K/B/T Min	AD678K/B/T Typ	AD678K/B/T Max	Units
TEMPERATURE RANGE							
J, K Grades	0		+70	0		+70	°C
A, B Grades	−40		+85	−40		+85	°C
S, T Grades	−55		+125	−55		+125	°C
ACCURACY							
Resolution	12			12			Bits
Integral Nonlinearity (INL)		±1			±0.7	±1	LSB
Differential Nonlinearity (DNL)	12			12			Bits
Unipolar Zero Error (@ +25°C)[1]		±4			±2	±3	LSB
Bipolar Zero Error (@ +25°C)[1]		±4			±3	±5	LSB
Gain Error (@ +25°C)[1, 2]		±4			±3	±6	LSB
Temperature Drift							
Unipolar/Bipolar Zero							
J, K Grades		±2			±2	±4	LSB
A, B Grades		±4			±3	±4	LSB
S, T Grades		±5			±4	±5	LSB
Gain[3]							
J, K Grades		±4			±4	±6	LSB
A, B Grades		±7			±5	±7	LSB
S, T Grades		±10			±8	±10	LSB
Gain[4]							
J, K Grades		±2			±2	±4	LSB
A, B Grades		±4			±3	±4	LSB
S, T Grades		±6			±5	±6	LSB
ANALOG INPUT							
Input Ranges							
Unipolar Range	0		+10	0		+10	V
Bipolar Range	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1			1	μs
Aperture Delay		10			10		ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	4.98		5.02	4.98		5.02	V
External Load							
Unipolar Mode			+1.5			+1.5	mA
Bipolar Mode			+0.5			+0.5	mA
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = +12 V ± 5%		±2				±2	LSB
V_{EE} = −12 V ± 5%		±2				±2	LSB
V_{DD} = +5 V ± 10%		±2				±2	LSB
Operating Current							
I_{CC}		18	20		18	20	mA
I_{EE}		25	34		25	34	mA
I_{DD}		8	12		8	12	mA
Power Consumption		560	745		560	745	mW

NOTES
[1]Adjustable to zero.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.

Specifications subject to change without notice.

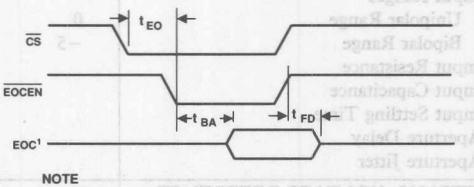
Parameter	Symbol	Min	Max	Units
$\overline{SC}$ Delay	t_{SC}	50		ns
Conversion Time	t_C	3.0	4.4	µs
Conversion Rate[1]	t_{CR}		5	µs
Convert Pulse Width	t_{CP}	97		ns
Aperture Delay	t_{AD}	5	20	ns
Status Delay	t_{SD}	0	400	ns
Access Time[2, 3]	t_{BA}	10	100	ns
		10	57[4]	ns
Float Delay[5]	t_{FD}	10	80	ns
Output Delay	t_{OD}		0	ns
Format Setup	t_{FS}	47		ns
$\overline{OE}$ Delay	t_{OE}	0		ns
Read Pulse Width	t_{RP}	97		ns
Conversion Delay	t_{CD}	150		ns
$\overline{EOCEN}$ Delay	t_{EO}	0		ns

NOTES
[1]Includes acquisition time.
[2]Measured from the falling edge of $\overline{OE}/\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 3.
[3]C_{OUT} = 100 pF.
[4]C_{OUT} = 50 pF.
[5]Measured from the rising edge of $\overline{OE}/\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 3; C_{OUT} = 10 pF.
Specifications subject to change without notice.



NOTES
[1] IN ASYNCHRONOUS MODE, STATE OF $\overline{CS}$ DOES NOT AFFECT OPERATION. SEE THE START CONVERSION TRUTH TABLE FOR DETAILS.
[2] $\overline{EOCEN}$ = LOW; SEE FIGURE 2. IN SYNCHRONOUS MODE, EOC IS A THREE-STATE OUTPUT. IN ASYNCHRONOUS MODE, EOC IS AN OPEN DRAIN OUTPUT.
[3] DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing



NOTE
[1]SEE END-OF-CONVERT (EOC) PARAGRAPH FOR DETAILS.

Figure 2. EOC Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	0 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	5 V	10 pF

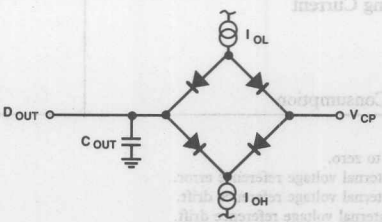


Figure 3. Load Circuit for Bus Timing Specifications

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC}	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	V_{EE}	V_{CC}	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C

Specification	With Respect To	Min	Max	Units
Operating Temperature				
J and K Grades		0	+70	°C
A and B Grades		−40	+85	°C
S and T Grades		−55	+125	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

ESD SENSITIVITY

The AD678 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD678 has been classified as a Category 1 device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

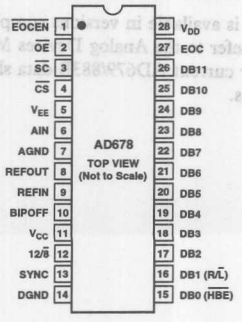
ORDERING GUIDE

Model[1]	Package	Temperature Range	Tested and Specified	Package Option[2]
AD678JN	28-Pin Plastic DIP	0°C to +70°C	AC	N-28
AD678KN	28-Pin Plastic DIP	0°C to +70°C	AC + DC	N-28
AD678JD	28-Pin Ceramic DIP	0°C to +70°C	AC	D-28
AD678KD	28-Pin Ceramic DIP	0°C to +70°C	AC + DC	D-28
AD678AD	28-Pin Ceramic DIP	−40°C to +85°C	AC	D-28
AD678BD	28-Pin Ceramic DIP	−40°C to +85°C	AC + DC	D-28
AD678AJ	44-Lead Ceramic JLCC	−40°C to +85°C	AC	J-44
AD678BJ	44-Lead Ceramic JLCC	−40°C to +85°C	AC + DC	J-44
AD678SD	28-Pin Ceramic DIP	−55°C to +125°C	AC	D-28
AD678TD	28-Pin Ceramic DIP	−55°C to +125°C	AC + DC	D-28

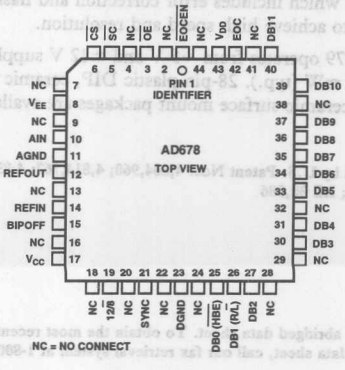
NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices Military Products Databook or /883 data sheet.
[2]N = Plastic DIP; D = Ceramic DIP; J = J-Leaded Ceramic Chip Carrier. For outline information see Package Information section.

PIN CONFIGURATIONS

DIP Package



JLCC Package



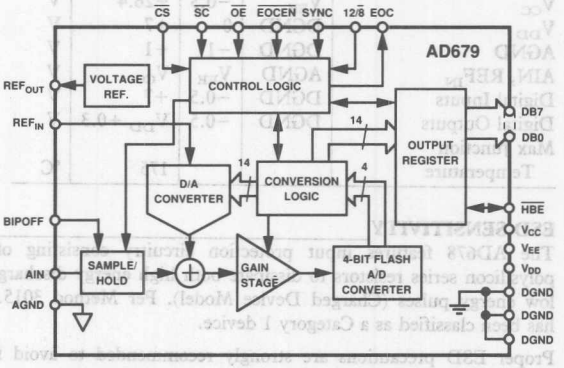
14-Bit 128 kSPS Complete Sampling ADC

AD679*

FEATURES

- AC and DC Characterized and Specified (K, B, T Grades)
- 128k Conversions per Second
- 1 MHz Full Power Bandwidth
- 500 kHz Full Linear Bandwidth
- 80 dB S/N+D (K, B, T Grades)
- Twos Complement Data Format (Bipolar Mode)
- Straight Binary Data Format (Unipolar Mode)
- 10 MΩ Input Impedance
- 8-Bit Bus Interface (See AD779 for 16-Bit Interface)
- On-Board Reference and Clock
- 10 V Unipolar or Bipolar Input Range
- Pin Compatible with AD678 12-Bit, 200 kSPS ADC
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD679 is a complete, multipurpose 14-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The AD679 is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD which are important in signal processing applications. In addition, the AD679K, B and T grades are fully specified for dc parameters which are important in measurement applications.

The 14 data bits are accessed in two read operations (8+6), with left justification. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation. Conversions can be initiated either under microprocessor control or by an external clock asynchronous to the system clock.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD679 operates from +5 V and ±12 V supplies and dissipates 560 mW (typ.). 28-pin plastic DIP, ceramic DIP and 44 J-leaded ceramic surface mount packages are available.

***Protected by U.S. Patent Nos. 4,804,960; 4,814,767; 4,833,345; 4,250,445; 4,808,908; RE 30,586**

PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD679 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. SPECIFICATIONS: The AD679K, B and T grades provide fully specified and tested ac and dc parameters. The AD679J, A and S grades are specified and tested for ac parameters; dc accuracy specifications are shown as typicals. DC specifications (such as INL, gain and offset) are important in control and measurement applications. AC specifications (such as S/N+D ratio, THD and IMD) are of value in signal processing applications.
3. EASE OF USE: The pinout is designed for easy board layout, and the two read output provides compatibility with 8-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
4. RELIABILITY: The AD679 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.
5. UPGRADE PATH: The AD679 provides the same pinout as the 12-bit, 200 kSPS AD678 ADC.
6. The AD679 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD679/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

AC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%, f_{SAMPLE} = 128 kSPS, f_{IN} = 10.009 kHz unless otherwise noted)[1]

Parameter	AD679J/A/S Min	AD679J/A/S Typ	AD679J/A/S Max	AD679K/B/T Min	AD679K/B/T Typ	AD679K/B/T Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO							
−0.5 dB Input (Referred to −0 dB Input)	78	79		80	81		dB
−20 dB Input (Referred to −20 dB Input)	58	59		60	61		dB
−60 dB Input (Referred to −60 dB Input)	18	19		20	21		dB
TOTAL HARMONIC DISTORTION (THD)							
@ +25°C		−90	−84		−90	−84	dB
		0.003	0.006		0.003	0.006	%
T_{MIN} to T_{MAX}		−88	−82		−88	−82	dB
		0.004	0.008		0.004	0.008	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−90	−84		−90	−84	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[2]							
2nd Order Products		−90	−84		−90	−84	dB
3rd Order Products		−90	−84		−90	−84	dB

DIGITAL SPECIFICATIONS (All device types T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		2.0	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	0.8	V
I_{IH}	High Level Input Current	V_{IN} = 5 V	−10	+10	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V	−10	+10	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		0.4	V
I_{OZ}	High Z Leakage Current	V_{IN} = 0 or 5 V	−10	+10	μA
C_{OZ}	High Z Output Capacitance			10	pF

NOTES

[1] f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a −0 dB (9.997 V p-p) input signal unless otherwise noted.

[2] f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 100 kSPS.

Specifications subject to change without notice.

Parameter	AD679J/A/S Min	AD679J/A/S Typ	AD679J/A/S Max	AD679K/B/T Min	AD679K/B/T Typ	AD679K/B/T Max	Units
TEMPERATURE RANGE							
J, K Grades	0		+70	0		+70	°C
A, B Grades	−40		+85	−40		+85	°C
S, T Grades	−55		+125	−55		+125	°C
ACCURACY							
Resolution	14			14			Bits
Integral Nonlinearity (INL)		±2			±1	±2	LSB
Differential Nonlinearity (DNL)	14			14			Bits
Unipolar Zero Error[1] (@ +25°C)		0.08			0.05	0.07	% FSR*
Bipolar Zero Error[1] (@ +25°C)		0.08			0.05	0.07	% FSR
Gain Error[1, 2] (@ +25°C)		0.12			0.09	0.11	% FSR
Temperature Drift							
Unipolar Zero[3]							
J, K Grades		0.04			0.04	0.05	% FSR
A, B Grades		0.05			0.05	0.07	% FSR
S, T Grades		0.09			0.09	0.10	% FSR
Bipolar Zero[3]							
J, K Grades		0.02			0.02	0.04	% FSR
A, B Grades		0.04			0.04	0.05	% FSR
S, T Grades		0.08			0.08	0.09	% FSR
Gain[3]							
J, K Grades		0.09			0.09	0.11	% FSR
A, B Grades		0.10			0.10	0.16	% FSR
S, T Grades		0.20			0.20	0.25	% FSR
Gain[4]							
J, K Grades		0.04			0.04	0.05	% FSR
A, B Grades		0.05			0.05	0.07	% FSR
S, T Grades		0.09			0.09	0.10	% FSR
ANALOG INPUT							
Input Ranges							
Unipolar Mode	0		+10	0		+10	V
Bipolar Mode	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1.5			1.5	µs
Aperture Delay		10			10		ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	4.98		5.02	4.98		5.02	V
External Load							
Unipolar Mode			+1.5			+1.5	mA
Bipolar Mode			+0.5			+0.5	mA
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = +12 V ± 5%		±6				±6	LSB
V_{EE} = −12 V ± 5%		±6				±6	LSB
V_{DD} = +5 V ± 10%		±6				±6	LSB
Operating Current							
I_{CC}		18	20		18	20	mA
I_{EE}		25	34		25	34	mA
I_{DD}		8	12		8	12	mA
Power Consumption		560	745		560	745	mW

NOTES
[1]Adjustable to zero.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.
*% FSR = percent of full-scale range.

TIMING SPECIFICATIONS

(All device types T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

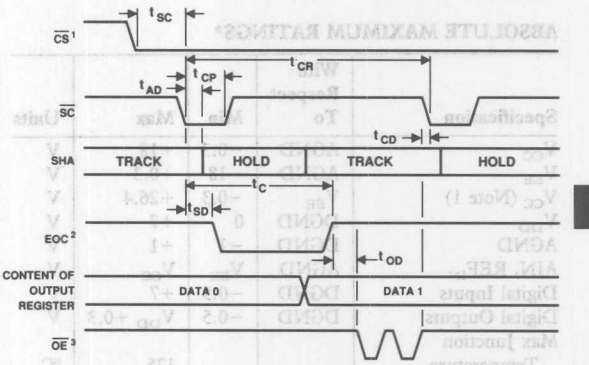
Parameter	Symbol	Min	Max	Units
$\overline{SC}$ Delay	t_{SC}	50		ns
Conversion Time	t_C		6.3	µs
Conversion Rate[1]	t_{CR}		7.8	µs
Convert Pulse Width	t_{CP}	0.097	3.0	µs
Aperture Delay	t_{AD}	5	20	ns
Status Delay	t_{SD}	0	400	ns
Access Time[2, 3]	t_{BA}	10	100	ns
		10	57[4]	ns
Float Delay[5]	t_{FD}	10	80	ns
Output Delay	t_{OD}		0	ns
Format Setup	t_{FS}	100		ns
$\overline{OE}$ Delay	t_{OE}	20		ns
Read Pulse Width	t_{RP}	195		ns
Conversion Delay	t_{CD}	400		ns
$\overline{EOCEN}$ Delay	t_{EO}	50		ns

NOTES
[1]Includes Acquisition Time.
[2]Measured from the falling edge of $\overline{OE}$/$\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 4.
[3]C_{OUT} = 100 pF.
[4]C_{OUT} = 50 pF.
[5]Measured from the rising edge of $\overline{OE}$/$\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5. See Figure 4; C_{OUT} = 10 pF.
Specifications subject to change without notice.

ORDERING GUIDE[1]

Model[2]	Package	Temperature Range	Tested and Specified	Package Option[3]
AD679JN	28-Pin Plastic DIP	0°C to +70°C	AC	N-28
AD679KN	28-Pin Plastic DIP	0°C to +70°C	AC + DC	N-28
AD679JD	28-Pin Ceramic DIP	0°C to +70°C	AC	D-28
AD679KD	28-Pin Ceramic DIP	0°C to +70°C	AC + DC	D-28
AD679AD	28-Pin Ceramic DIP	−40°C to +85°C	AC	D-28
AD679BD	28-Pin Ceramic DIP	−40°C to +85°C	AC + DC	D-28
AD679SD	28-Pin Ceramic DIP	−55°C to +125°C	AC	D-28
AD679TD	28-Pin Ceramic DIP	−55°C to +125°C	AC + DC	D-28
AD679AJ	44-Lead Ceramic JLCC	−40°C to +85°C	AC	J-44
AD679BJ	44-Lead Ceramic JLCC	−40°C to +85°C	AC + DC	J-44
AD679SJ	44-Lead Ceramic JLCC	−55°C to +125°C	AC	J-44
AD679TJ	44-Lead Ceramic JLCC	−55°C to +125°C	AC + DC	J-44

NOTES
[1]For parallel read (14-Bits) interface to 16-bit buses, see AD779.
[2]For details grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Miliary Products Databook or current AD679/883B data sheet.
[3]N = Plastic DIP; D = Ceramic DIP; J = J-Leaded Ceramic Chip Carrier. For outline information see Package Information section.



NOTES
[1] IN ASYNCHRONOUS MODE, STATE OF $\overline{CS}$ DOES NOT AFFECT OPERATION. SEE THE START CONVERSION TRUTH TABLE FOR DETAILS.
[2] $\overline{EOCEN}$ = LOW (SEE FIGURE 3). IN SYNCHRONOUS MODE, EOC IS A THREE-STATE OUTPUT. IN ASYNCHRONOUS MODE, EOC IS AN OPEN DRAIN OUTPUT.
[3] DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing

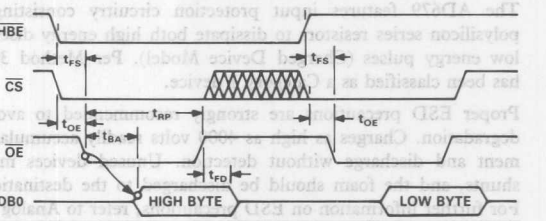
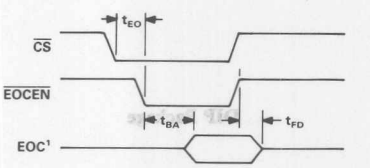


Figure 2. Output Timing



NOTE
[1]EOC IS A THREE-STATE OUTPUT IN SYNCHRONOUS MODE AND AN OPEN DRAIN OUTPUT IN ASYNCHRONOUS. ACCESS (t_{BA}) AND FLOAT (t_{FD}) TIMING SPECIFICATIONS DO NOT APPLY IN ASYNCHRONOUS MODE WHERE THEY ARE A FUNCTION THE TIME CONSTANT FORMED BY THE 10 pF OUTPUT CAPACITANCE AND THE PULL-UP RESISTOR.

Figure 3. EOC Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	0 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	5 V	10 pF

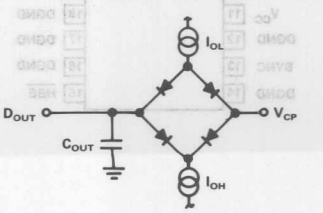


Figure 4. Load Circuit for Bus Timing Specifications

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC} (Note 1)	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	V_{EE}	V_{CC}	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C

Specification	With Respect To	Min	Max	Units
Operating Temperature				
J and K Grades		0	+70	°C
A and B Grades		−40	+85	°C
S and T Grades		−55	+125	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]The AD679 is not designed to operate from ±15 V supplies.

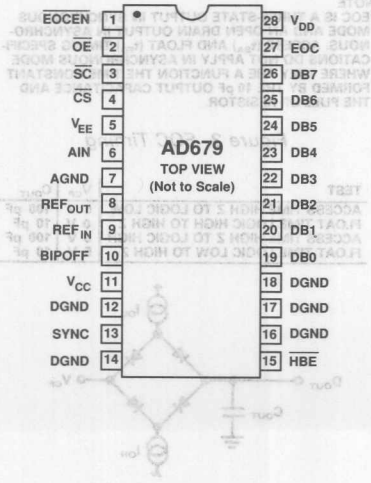
ESD SENSITIVITY

The AD679 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD679 has been classified as a Category 1 device.

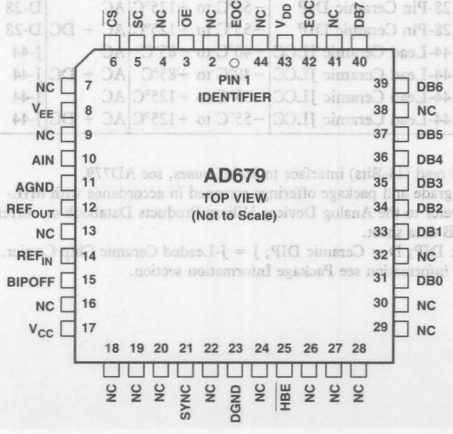
Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

PIN DESIGNATIONS

DIP Package



JLCC Package



NC = NO CONNECT

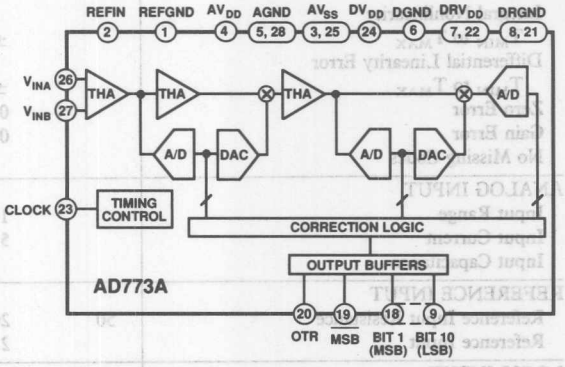
10-Bit 20 MSPS Monolithic A/D Converter

AD773A

FEATURES

- Monolithic 10-Bit 20 MSPS A/D Converter
- Low Power Dissipation: 1.0 W
- Signal-to-Noise Plus Distortion Ratio
  - f_{IN} = 1 MHz: 56 dB
  - f_{IN} = 10 MHz: 54 dB
- Guaranteed No Missing Codes
- On-Chip Track-and-Hold Amplifier
- 100 MHz Full Power Bandwidth
- High Impedance Reference Input
- Out of Range Output
- Twos Complement and Binary Output Data
- Available in Commercial and Military Temperature Ranges (See Military/Aerospace Reference Manual for Specifications)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD773A is a monolithic 10-bit, 20 Msps analog-to-digital converter incorporating an on-board, high performance track-and-hold amplifier (THA). The AD773A converts video bandwidth signals without the use of an external THA. The AD773A implements a multistage differential pipelined architecture with output error correction logic. The AD773A offers accurate performance and guarantees no missing codes over the full operating temperature range.

Output data is presented in binary and twos complement format. An out of range (OTR) signal indicates the analog input voltage is beyond the specified input range. OTR can be decoded with the MSB/$\overline{\text{MSB}}$ pins to signal an underflow or overflow condition. The high impedance reference input allows multiple AD773As to be driven in parallel from a single reference.

The combined dc precision and dynamic performance of the AD773A is useful in a variety of applications. Typical applications include: video enhancement, HDTV, ghost cancellation, ultrasound imaging, radar and high speed data acquisition.

The AD773A was designed using Analog Devices' ABCMOS-1 process which utilizes high speed bipolar and 2-micron CMOS transistors on a single chip. High speed, precision analog circuits are now combined with high density logic circuits. Laser trimmed thin film resistors are used to optimize accuracy and temperature stability.

The AD773A is packaged in a 28-pin ceramic DIP and is available in commercial (0°C to +70°C) and military (−55°C to +125°C) grades.

PRODUCT HIGHLIGHTS

1. On-board THA
   The high impedance differential input THA eliminates the need for external buffering or sample and hold amplifiers. The THA offers the choice of differential or single-ended inputs. Input current is typically 5 μA.
2. High Impedance Reference Input
   The high impedance reference input (200 kΩ) allows direct connection with standard +2.5 V references, such as the AD680, AD580 and REF43.
3. Output Data Flexibility
   Output data is available in bipolar offset and bipolar twos complement binary format.
4. Out of Range (OTR)
   The OTR output bit indicates when the input signal is beyond the AD773A's input range.
5. Military Temperature Range

Parameter	AD773AJ Min	AD773AJ Typ	AD773AJ Max	AD773AK Min	AD773AK Typ	AD773AK Max	Units
RESOLUTION	10			10			Bits
DC ACCURACY							
Integral Nonlinearity							LSB
T_{MIN} to T_{MAX}		±0.75			±0.75	±2	LSB
Differential Linearity Error							LSB
T_{MIN} to T_{MAX}		±0.75			±0.75	±1	LSB
Zero Error		0.5			0.5	3.5	% FSR
Gain Error		0.5			0.5	3.0	% FSR
No Missing Codes					GUARANTEED		
ANALOG INPUT							
Input Range		1			1		V p–p
Input Current		5	20		5	20	µA
Input Capacitance			10			10	pF
REFERENCE INPUT							
Reference Input Resistance	50	200		50	200		kΩ
Reference Input		2.5			2.5		Volts
LOGIC INPUT							
High Level Input Voltage	+3.5			+3.5			V
Low Level Input Voltage			+0.5			+0.5	V
High Level Input Current (V_{IN} = DV_{DD})	−10		+10	−10		+10	µA
Low Level Input Current (V_{IN} = 0 V)	−10		+10	−10		+10	µA
Input Capacitance		10			10		pF
LOGIC OUTPUTS							
High Level Output Voltage (I_{OH} = 0.5 mA)	+2.4			+2.4			V
Low Level Output Voltage (I_{OL} = 1.6 mA)			+0.4			+0.4	V
POWER SUPPLIES							
Operating Voltages							
AV_{DD}	+4.75		+5.25	+4.75		+5.25	Volts
AV_{SS}	−5.25		−4.75	−5.25		−4.75	Volts
DV_{DD}, DRV_{DD}	+4.75		+5.25	+4.75		+5.25	Volts
Operating Current							
IAV_{DD}		65	80		65	80	mA
IAV_{SS}		−115	−140		−115	−140	mA
IDV_{DD}		10	20		10	20	mA
$IDRV_{DD}$[1]		10	15		10	15	mA
POWER CONSUMPTION[2]		1.0	1.2		1.0	1.2	W
POWER SUPPLY REJECTION		10	18		10	18	mV/V
TEMPERATURE RANGE							
Specified (J/K)	0		+70	0		+70	°C

NOTES
[1]C_L = 15 pF.
[2]100% production tested.

Specifications subject to change without notice. See Definition of Specifications for additional information.

Parameter	Min	Typ	Max	Min	Typ	Max	Units
DYNAMIC PERFORMANCE[1]							
Signal-to-Noise plus Distortion (S/N+D) Ratio							
f_{IN} = 1 MHz	52	56		54	56		dB
f_{IN} = 10 MHz	50	54		51	54		dB
Effective Number of Bits (ENOB)							
f_{IN} = 1 MHz		9.0			9.0		Bits
f_{IN} = 10 MHz		8.7			8.7		Bits
Total Harmonic Distortion (THD)							
f_{IN} = 1 MHz		−67	−57		−67	−59	dB
f_{IN} = 10 MHz		−65	−54		−65	−55	dB
Spurious Free Dynamic Range[2]		70			70		dB
Full Power Bandwidth		100			100		MHz
Intermodulation Distortion (IMD)[3]							
Second Order Products		−69			−69		dB
Third Order Products		−64			−64		dB
Differential Phase		0.2			0.2		Degree
Differential Gain		0.5			0.5		%
Transient Response		25			25		ns
Overvoltage Recovery Time		25			25		ns

NOTES
[1]For typical dynamic performance curves at f_{SAMPLE} = 20 Msps see Figures 2 through 7.
[2]f_{IN} = 1 MHz.
[3]fa = 1.0 MHz, fb = 1.05 MHz.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (for all grades T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = −5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise indicated, f_{SAMPLE} = 20 Msps)

	Symbol	Min	Typ	Max	Units
Conversion Rate				20	Msps
Clock Period	t_{CLK}	50			ns
Clock High	t_{CH}	24.5			ns
Clock Low	t_{CL}	24.5			ns
Output Delay	t_{OD}		20		ns
Aperture Delay			7		ns
Aperture Jitter			9		ps
Pipeline Delay (Latency)				4	Clock Cycles

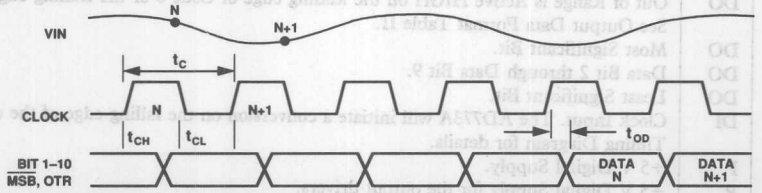


Figure 1. AD773A Timing Diagram

CAUTION

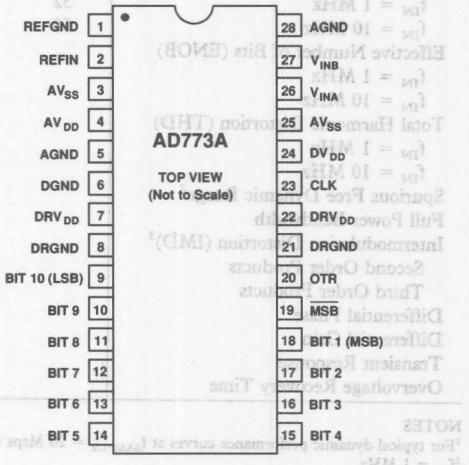
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD773A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AV_{DD}	AGND	−0.5	+6.5	V
AV_{SS}	AGND	−6.5	+0.5	V
V_{INA}, V_{INB}	AGND	−6.5	+6.5	V
DV_{DD}, DRV_{DD}	DGND, DRGND	−0.5	+6.5	V
AGND	DGND, DRGND	−1.0	+1.0	V
AV_{DD}	DV_{DD}, DRV_{DD}	−6.5	+0.5	V
CLK	DV_{DD}, DRV_{DD}	−6.5	+0.5	V
REFIN	REFGND, AGND	−0.5	+6.5	V
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE[1]

Model	Temperature Range	Description	Package Option[2]
AD773AJD	0°C to +70°C	28-Pin Ceramic DIP	D-28
AD773AKD	0°C to +70°C	28-Pin Ceramic DIP	D-28

NOTES
[1]See Military/Aerospace Reference Manual for AD773ASD/883B specifications.
[2]D = Ceramic DIP. For outline information see Package Information section.

PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	5, 28	P	Analog Ground.
AV_{DD}	4	P	+5 V Analog Supply.
AV_{SS}	3, 25	P	−5 V Analog Supply.
$\overline{MSB}$	19	DO	Inverted Most Significant Bit. Provides twos complement output data format.
OTR	20	DO	Out of Range is Active HIGH on the leading edge of Code 0 or the trailing edge of Code 1023. See Output Data Format Table II.
BIT 1 (MSB)	18	DO	Most Significant Bit.
BIT 2–BIT 9	17–10	DO	Data Bit 2 through Data Bit 9.
BIT 10 (LSB)	9	DO	Least Significant Bit.
CLK	23	DI	Clock Input. The AD773A will initiate a conversion on the falling edge of the clock input. See the Timing Diagram for details.
DV_{DD}	24	P	+5 V Digital Supply.
DRV_{DD}	7, 22	P	+5 V Digital Supply for the output drivers.
DGND	6	P	Digital Ground.
DRGND	8, 21	P	Digital Ground for the output drivers.
REFGND	1	AI	REFGND is connected to the ground of the external reference.
REFIN	2	AI	REFIN is the external 2.5 V reference input, taken with respect to REFGND.
V_{INA}	26	AI	(+) Analog input signal to the differential input THA.
V_{INB}	27	AI	(−) Analog input signal to the differential input THA.

Type: AI = Analog Input; DI = Digital Input; DO = Digital Output; P = Power.

INTEGRAL NONLINEARITY (INL)
Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

DIFFERENTIAL LINEARITY ERROR (DNL, NO MISSING CODES)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value.

ZERO EROR
The major carry transition should occur for an analog value 1/2 LSB below analog common. Zero error is defined as the deviation of the actual transition from that point.

GAIN ERROR
The first code transition should occur for an analog value 1/2 LSB above nominal negative full scale. The last transition should occur 1 1/2 LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

POWER SUPPLY REJECTION
One of the effects of power supply variation on the performance of the device will be a change in gain error. The specification shows the maximum gain error deviation as the supplies are varied from their nominal values to their specified limits.

SIGNAL-TO-NOISE PLUS DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)
ENOB is calculated from the following expression:

S/N+D = 6.02N + 1.76, where N is equal to the effective number of bits.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SPURIOUS FREE DYNAMIC RANGE
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa±nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa+fb) and (fa−fb) and the third order terms are (2fa+fb), (2fa−fb), (fa+2fb) and (fa−2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sums is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

DIFFERENTIAL GAIN
The percentage difference between the output amplitudes of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed.

DIFFERENTIAL PHASE
The difference in the output phase of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed.

TRANSIENT RESPONSE
The time required for the AD773A to achieve its rated accuracy after a full-scale step function is applied to its input.

OVERVOLTAGE RECOVERY TIME
The time required for the ADC to recover to full accuracy after an analog input signal 150% of full scale is reduced to 50% of the full-scale value.

APERTURE DELAY
The difference between the switch delay and the analog delay of the THA. This effective delay represents the point in time, relative to the falling edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER
The variations in aperture delay for successive samples.

PIPELINE DELAY (LATENCY)
The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

FULL POWER BANDWIDTH
The input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

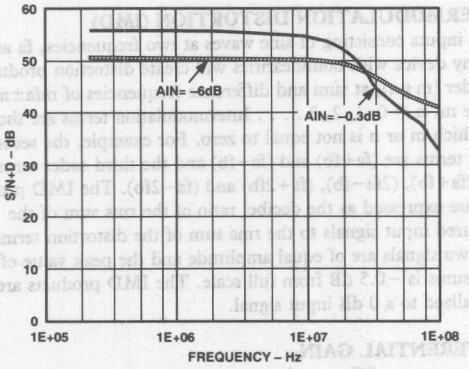


Figure 2. S/N+D vs. Input Frequency, f_{CLK} = 20 MSPS

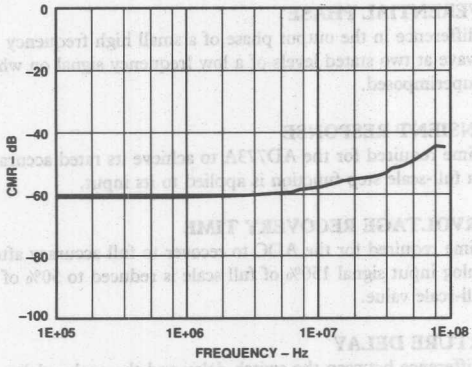


Figure 3. CMR vs. Input Frequency, f_{CLK} = 20 MSPS

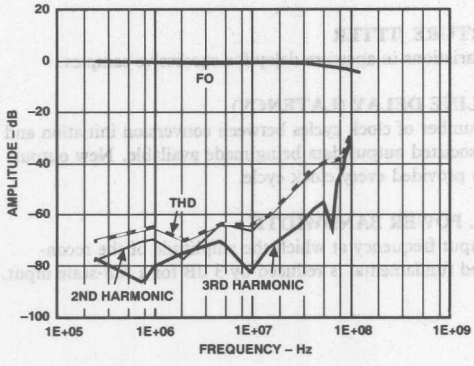


Figure 4. Harmonic Distortion vs. Input Frequency, f_{CLK} = 20 MSPS: Full Power

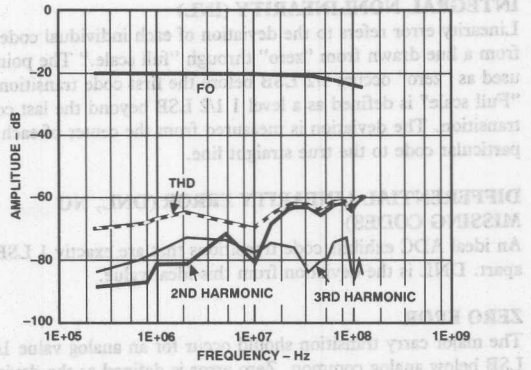


Figure 5. Harmonic Distortion vs. Input Frequency, f_{CLK} = 20 MSPS: Small Signal

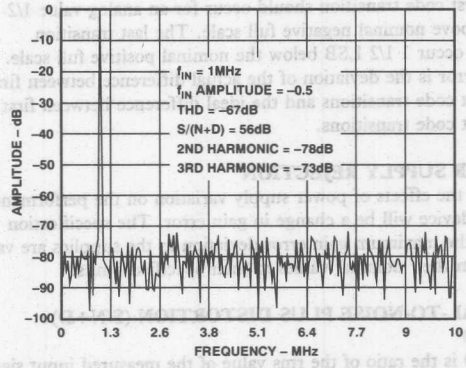


Figure 6. Typical FFT Plot of AD773A, f_{CLK} = 20 MSPS, f_{IN} = 1 MHz at 1 V p–p

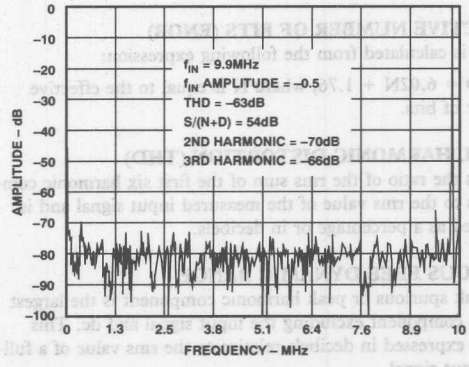


Figure 7. Typical FFT Plot of AD773A, f_{CLK} = 20 MSPS, f_{IN} = 9.9 MHz at 1 V p–p

Theory of Operation

The AD773A uses a pipelined multistage architecture with a differential input, fast settling track-and-hold amplifier (THA). Traditionally, high speed ADCs have used parallel, or flash architectures. When compared to flash converters, multistage architectures reduce the power dissipation and die size by reducing the number of comparators. For example, the AD773A uses 48 comparators compared to 1023 comparators for a 10-bit flash architecture.

The AD773A's main signal path transmits differential current mode signals. Low impedance current summing techniques are employed, increasing speed by reducing sensitivity to parasitic capacitances. Pipelining allows the stages to operate concurrently and maximizes system throughput.

The input THA is followed by three 4-bit conversion stages. At any given time, the first stage operates on the most recent sample, while the second stage operates on a signal dependent on the previous sample. This process continues throughout all three stages. The twelve digital bits provided by the three 4-bit stages are combined in the correction logic to produce a 10-bit representation of the sampled analog input.

Pipeline delay, or latency, is four clock cycles. New output data is provided every clock cycle and is provided in both binary and twos complement format. The AD773A will flag an out-of-range condition when the analog input exceeds the specified analog input range.

Applying the AD773A

DRIVING THE AD773A INPUT

The AD773A may be driven in a single-ended or differential fashion. V_{INA} is the positive input, and V_{INB} is the negative input. In the single-ended configuration either V_{INA} or V_{INB} is connected to Analog Ground (AGND) while the other input is driven with a full-scale input of ±500 mV p–p. An inverted mode of operation can be achieved by simply interchanging the input connections.

Both inputs of the AD773A, V_{INA} and V_{INB}, are high impedance and do not need to be driven by a low impedance source. Note, however, that as the source impedance increases, the input node becomes more susceptible to noise. The increased noise at the input will degrade performance. A 10 pF capacitor across V_{INA} and V_{INB} as shown in Figure 8 is recommended to bypass high frequency noise.

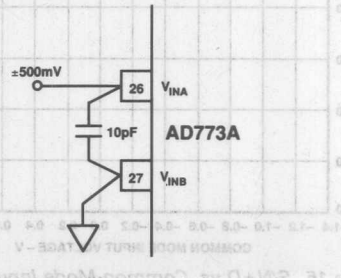


Figure 8. AD773A Single-Ended Input Connection

INPUT CONDITIONING

In some cases, it may be appropriate to buffer the input source, add dc offset, or otherwise condition the input signal of the AD773A. Choosing an appropriate op amp will vary with system requirements and the desired level of performance. Some suggested op amps are the AD9617, AD842, and AD827.

Figure 9 shows a typical application where a unipolar signal is level shifted to the bipolar input range of the AD773A. Note that the reference used with the AD773A can also provide a noise-free voltage source to generate the dc offset.

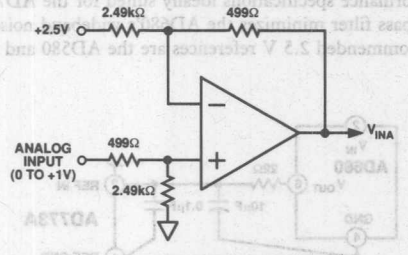


Figure 9. Unipolar to Bipolar Input Connection

DIFFERENTIAL INPUT CONNECTIONS

Operating the AD773A with fully differential inputs offers the advantage of rejecting common-mode signals present on both V_{INA} and V_{INB}. The full-scale input range of V_{INA} and V_{INB} when driven differentially is ±250 mV p–p as shown in Table I.

Table I. AD773A's Maximum Differential Input Voltage

V_{INA}	V_{INB}	$V_{INA}-V_{INB}$
+250 mV	−250 mV	+500 mV
−250 mV	+250 mV	−500 mV

In some applications it may be desirable to convert a single-ended signal to a differential signal before being applied to the AD773A. Figure 10 shows a single-ended to differential video line driver capable of driving doubly terminated cables.

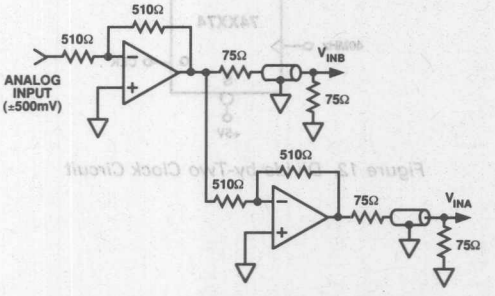


Figure 10. Single-Ended to Differential Connection

ladder requirements of a flash converter the AD773A's single pin, high impedance input can be driven from one low cost, low power reference. The high impedance input allows multiple AD773A's to be driven from one reference thus minimizing drift errors.

Figure 11 shows the AD773A connected to the AD680. The AD680 is a single supply, low power, low cost 2.5 V reference with performance specifications ideally suited for the AD773A. The low pass filter minimizes the AD680's wideband noise. Other recommended 2.5 V references are the AD580 and REF43.

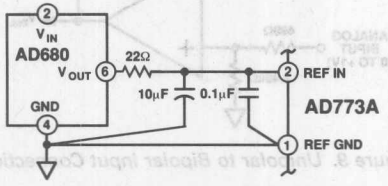


Figure 11. Recommended AD773A to AD680 Connection

CLOCK INPUT

The AD773A's pipelined architecture operates on both the rising and falling edges of the clock input. A low jitter, symmetrical clock will provide the highest level of performance. The recommended logic family to drive the clock input is HC. The AD773A's minimum clock half cycle may necessitate the use of an external divide-by-two circuit as shown in Figure 12. Power dissipation will vary with input clock frequency as shown in Figure 13.

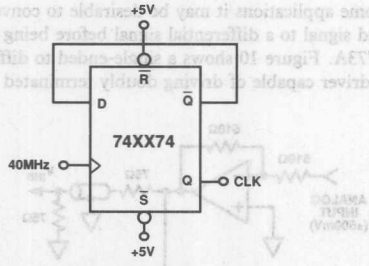


Figure 12. Divide-by-Two Clock Circuit

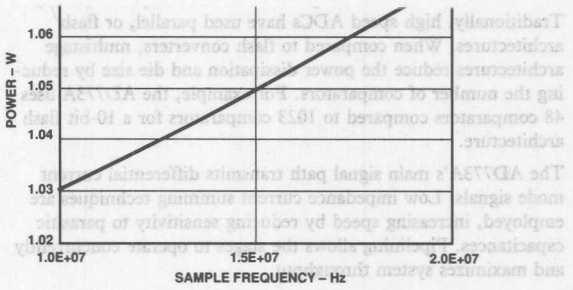


Figure 13. Power Dissipation vs. Sample Frequency

EQUIVALENT ANALOG INPUT CIRCUIT

The AD773A equivalent analog input circuit is shown in Figure 14. The typical input bias current is 5 μA, while input capacitance is typically 5 pF. In the single-ended input configuration one input is connected to AGND while the second input is driven to full scale (±500 mV). Under nominal conditions the collector of the input transistor is at +1.15 V. This allows signals to be offset by up to +0.65 V without significantly degrading performance. In the negative direction, the emitter of the input transistor should not drop below −1.25 V. Therefore, signals can be offset by −0.65 V without significant performance degradation. Figure 15 shows signal-to-noise ratio vs. common-mode input voltage.

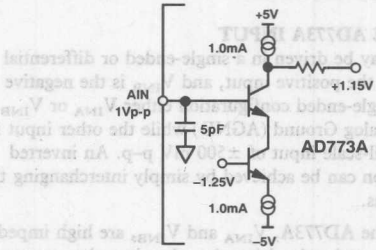


Figure 14. Equivalent Analog Input Circuit

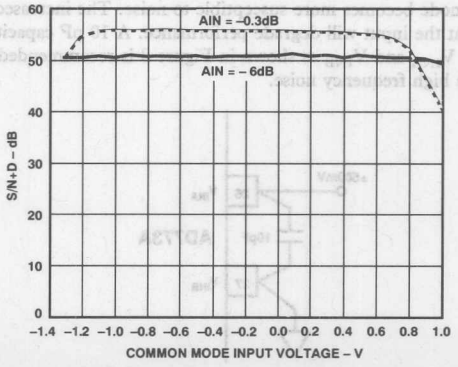


Figure 15. S/N+D vs. Common-Mode Input Voltage, f_{CLK} = 20 MSPS

EQUIVALENT REFERENCE INPUT CIRCUIT

The AD773A is designed to have a reference to analog input voltage ratio of 2.5:1. When the AD773A is configured for single-ended operation a 2.5 volt reference input establishes a full-scale analog input voltage of 1 V p-p (±500 mV with respect to V_{INB}). Although the AD773A is specified and tested with V_{REF} equal to 2.5 V and V_{IN} equal to ±500 mV the reference input voltage and analog input voltages can be changed. To optimize the AD773A's performance the 2.5:1 ratio should be maintained. The simplified model of the AD773A's reference input circuit is shown in Figure 16.

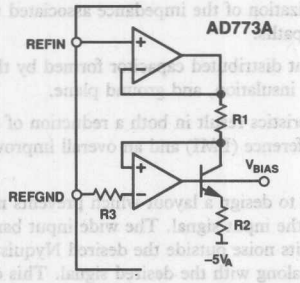


Figure 16. Typical Reference Input Circuit

The 2.5 V external reference is applied across resistor R1 producing a current which in turn generates a voltage V_{BIAS}. Multiple reference currents are generated from V_{BIAS} and are used throughout the converter. R3 is used to cancel errors induced by the input bias current of the REFGND buffer. Figure 17 shows the SNR performance as the reference voltage is varied from its nominal value of 2.5 V. The input full-scale voltage is defined by the following equation,

$$\textit{Input Full-Scale Voltage} = \frac{\textit{Reference Voltage}}{2.5}$$

The power dissipation is modulated by variations in the reference voltage. Figure 18 shows the variation in power dissipation versus reference voltage.

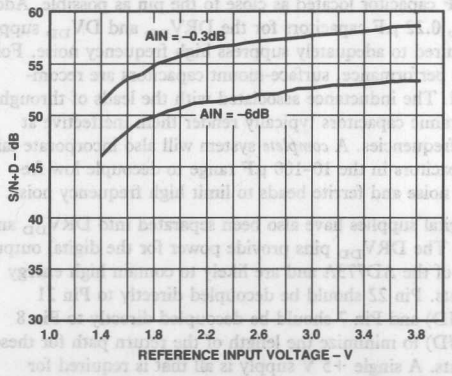


Figure 17. S/N+D vs. Reference Input Voltage, f_{CLK} = 20 MSPS, f_{IN} = 1 MHz

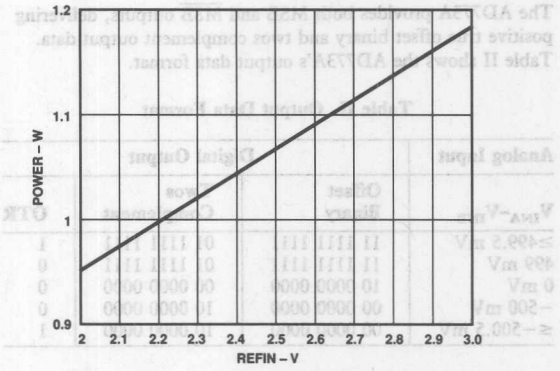


Figure 18. Power Dissipation vs. Reference Input Voltage, f_{CLOCK} = 20 MSPS

TRANSIENT RESPONSE

The fast settling input THA accurately converts full-scale input voltage swings in under one clock cycle. The THA's high impedance, fast slewing performance is critical in multiplexed or dc stepped (charge coupled devices, infrared detectors) systems. Figure 19 show the AD773A's settling performance with an input signal stepped from −500 mV to 0 V. As can be seen, the output code settles to its final value in under one clock cycle.

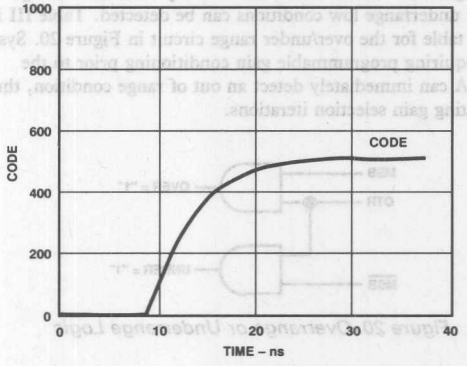


Figure 19. Typical AD773A Settling Time

OUTPUT DATA FORMAT

The AD773A provides both MSB and $\overline{MSB}$ outputs, delivering positive true offset binary and twos complement output data. Table II shows the AD773A's output data format.

Table II. Output Data Format

Analog Input	Digital Output		
$V_{INA}-V_{INB}$	Offset Binary	Twos Complement	OTR
≥499.5 mV	11 1111 1111	01 1111 1111	1
499 mV	11 1111 1111	01 1111 1111	0
0 mV	10 0000 0000	00 0000 0000	0
−500 mV	00 0000 0000	10 0000 0000	0
≤−500.5 mV	00 0000 0000	10 0000 0000	1

OUT OF RANGE

An out-of-range condition exists when the analog input voltage is beyond the input range (±500 mV) of the converter. [Note the AD773A has a 4 clock cycle latency.] OTR (Pin 20) is set low when the analog input voltage is within the analog input range. OTR is set HIGH and will remain HIGH when the analog input voltage exceeds the input range by 1/2 LSB from the center of the ± full-scale output codes. OTR will remain HIGH until the analog input is within the input range. Note that if the input is driven beyond +1.5 V, the digital outputs may not stay at +FS, but may actually fold back to midscale. By logical ANDing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table III is a truth table for the over/under range circuit in Figure 20. Systems requiring programmable gain conditioning prior to the AD773A can immediately detect an out of range condition, thus eliminating gain selection iterations.

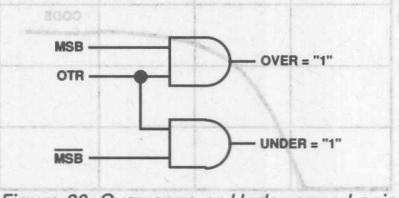


Figure 20. Overrange or Underrange Logic

Table III. Out-of-Range Truth Table

OTR	MSB	ANALOG INPUT IS
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

GROUNDING AND LAYOUT RULES

As is the case for any high performance device, proper grounding and layout techniques are essential in achieving optimal performance. (Note—Figures 22–26 are not to scale.) The analog and digital grounds on the AD773A have been separated to optimize the management of return currents in a system. It is recommended that a 4-layer printed circuit board (PCB) which employs ground planes and power planes be used with the AD773A. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout which prevents noise from coupling onto the input signal. The wide input bandwidth of the AD773A permits noise outside the desired Nyquist bandwidth to be sampled along with the desired signal. This can result in a higher overall level of spurious noise in the digitized output. Digital signals should not be run in parallel with the circuitry. It is also suggested that the traces associated with V_{INA} and V_{INB} be the same length.

Separate analog and digital grounds should be joined together directly under the AD773A (see Figure 24). A solid ground plane under the AD773A is also acceptable if care is taken in the management of the power and ground return currents. A general "rule-of-thumb" for mixed signal layouts dictates that the return currents from digital circuitry should not pass through critical analog circuitry.

POWER SUPPLY DECOUPLING

The analog and digital supplies of the AD773A have been separated to prevent the typically large transients associated with digital circuitry from coupling into the analog supplies (AV_{DD}, AV_{SS}). Each analog power supply pin should be decoupled with a 0.1 μF capacitor located as close to the pin as possible. Additionally, 0.22 μF capacitors for the DRV_{DD} and DV_{DD} supplies are required to adequately suppress high frequency noise. For optimal performance, surface-mount capacitors are recommended. The inductance associated with the leads of through-hole ceramic capacitors typically render them ineffective at higher frequencies. A *complete* system will also incorporate tantalum capacitors in the 10–100 μF range to decouple low frequency noise and ferrite beads to limit high frequency noise.

The digital supplies have also been separated into DRV_{DD} and DV_{DD}. The DRV_{DD} pins provide power for the digital output drivers of the AD773A and are likely to contain high energy transients. Pin 22 should be decoupled directly to Pin 21 (DRGND) and Pin 7 should be decoupled directly to Pin 8 (DRGND) to minimize the length of the return path for these transients. A single +5 V supply is all that is required for DRV_{DD} and DV_{DD}, but decoupling DV_{DD} with an RC filter network is suggested (see Figure 21).

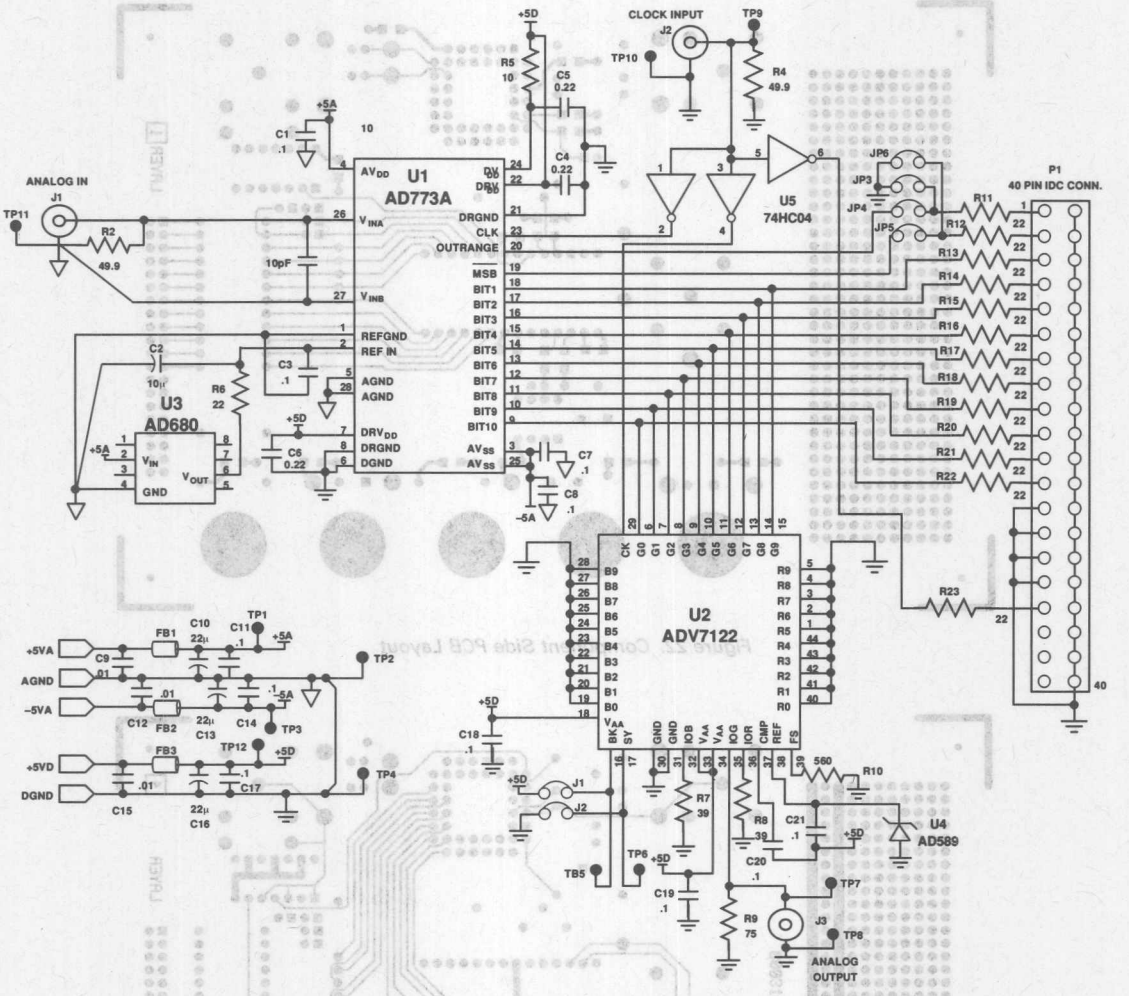


Figure 21. AD773A Evaluation Board Schematic

Table IV. Components List

Reference Designator	Description	Quantity
R2, R4	Resistor, 1%, 49.9 Ω	2
R5, R6, R11–R22	Resistor, 5%, 22 Ω	14
R7, R8	Resistor, 5%, 39 Ω	2
R9	Resistor, 5%, 75 Ω	1
R10	Resistor, 5%, 560 Ω	1
C1, C3–C8, C11, C14, C17–C21	Chip Cap, 0.1 μF	14
C2	Capacitor, Tantalum, 10 μF	1
C9, C12, C15	Chip Cap, 0.01 μF	3
C10, C13, C16	Capacitor, Tantalum, 22 μF	3
U1	AD773A	1
U2	ADV7122	1
U3	AD680	1
U4	AD589	1
U5	74AS04	1
FB1–FB3	Ferrite Bead	3

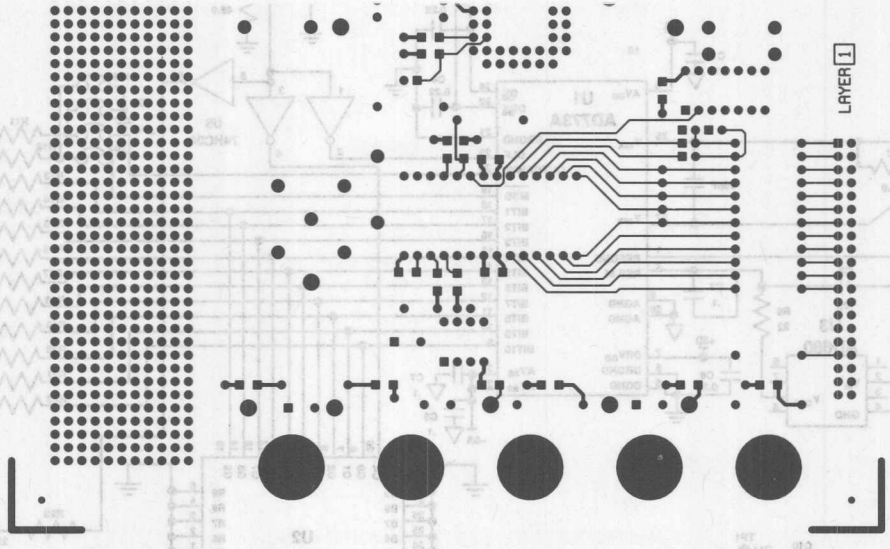


Figure 22. Component Side PCB Layout

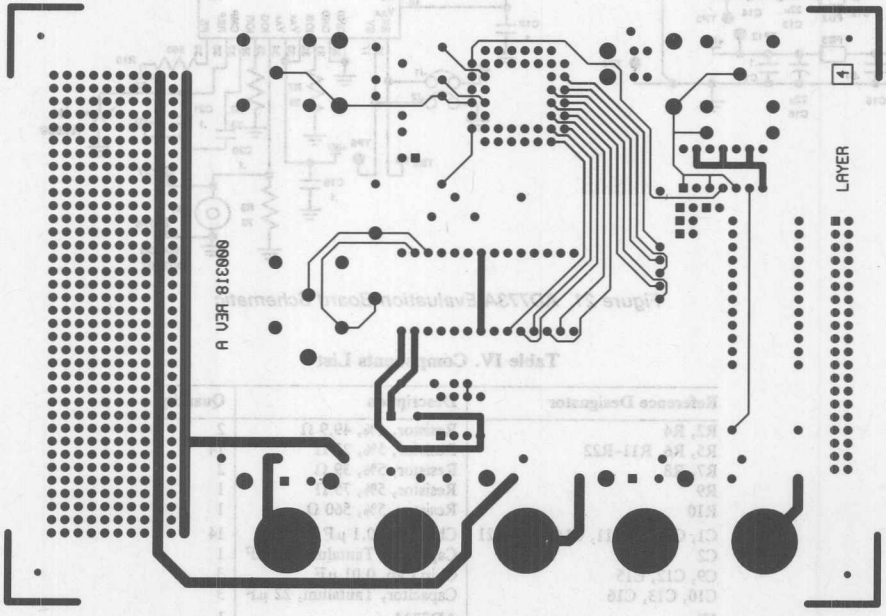


Figure 23. Solder Side PCB Layout

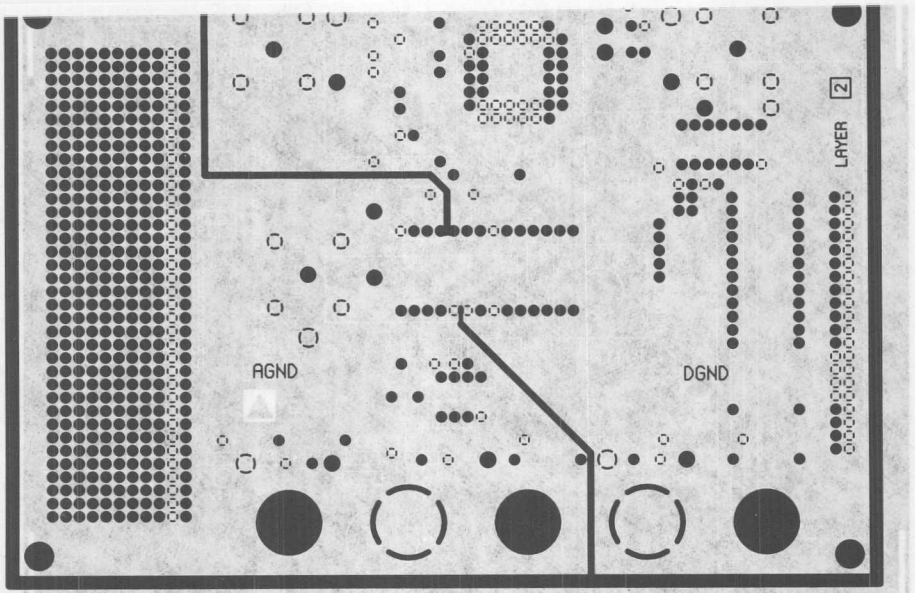


Figure 24. Ground Layer PCB Layout

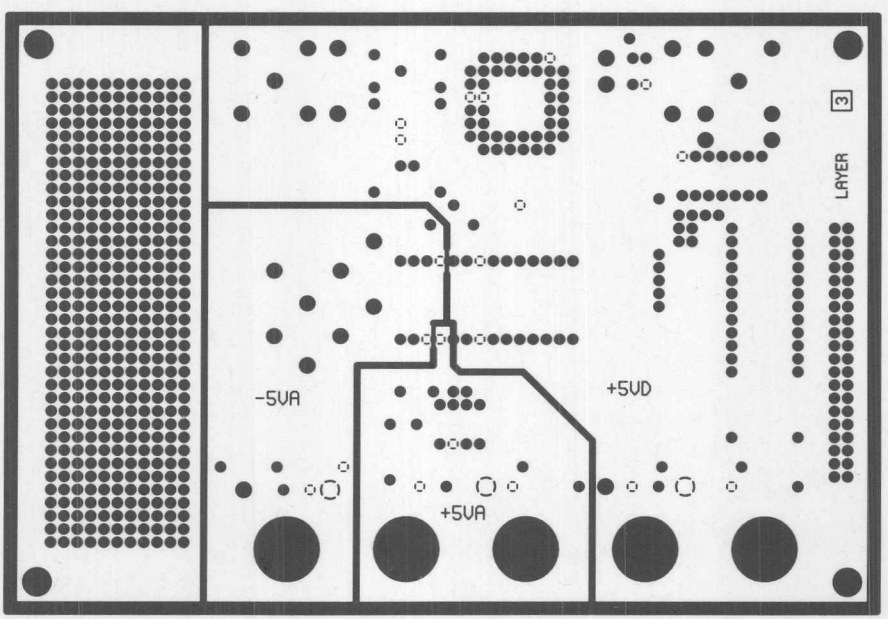


Figure 25. Power Layer PCB Layout

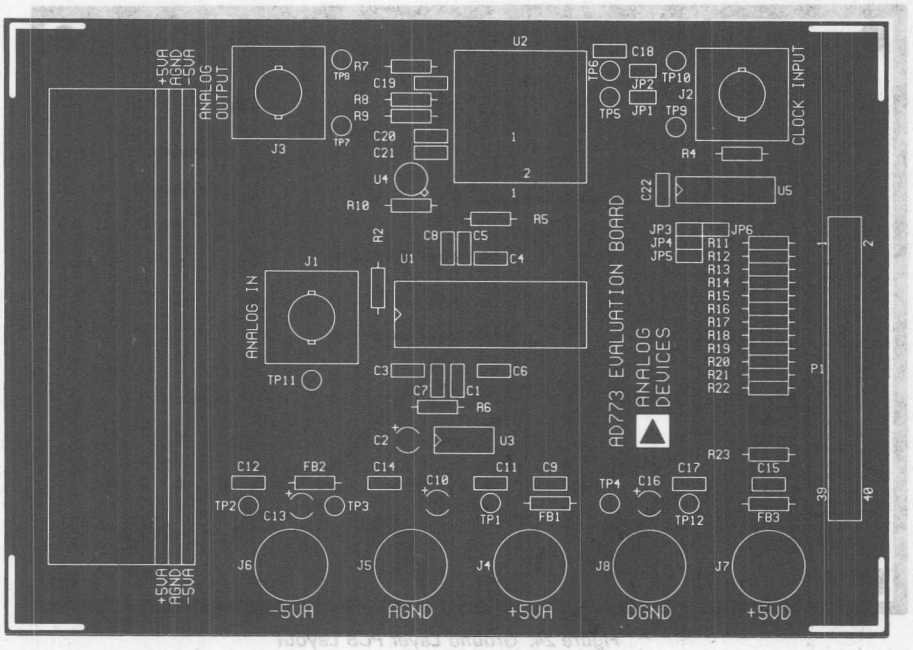
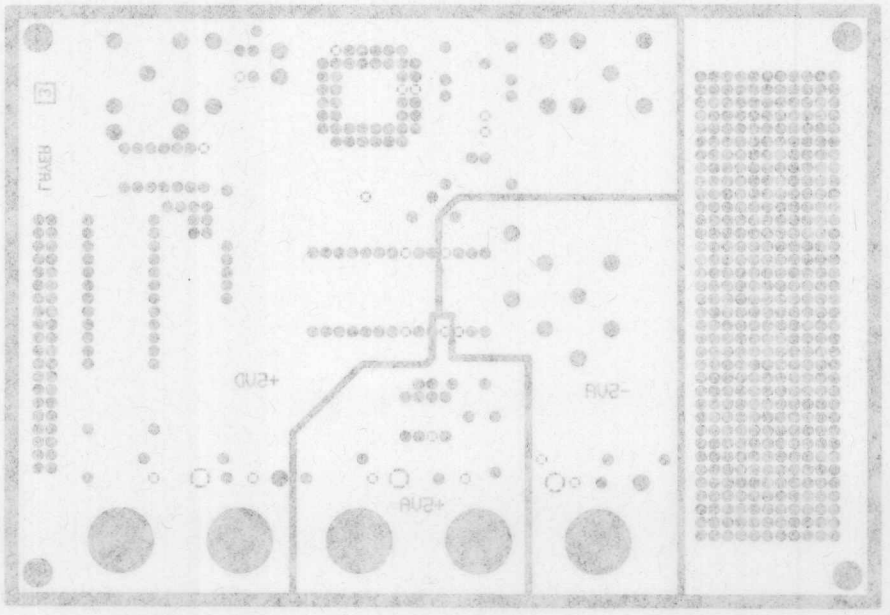


Figure 26. Silkscreen Layer PCB Layout



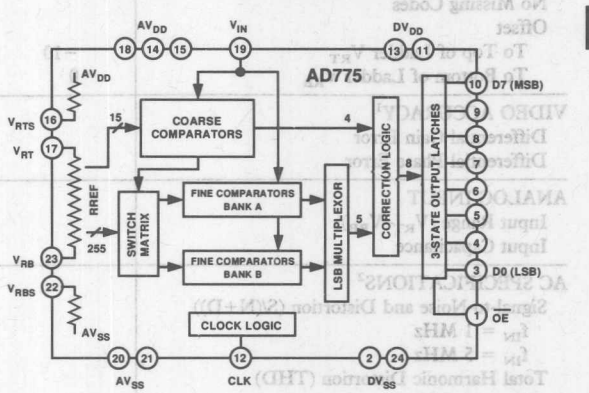
8-Bit 20 MSPS, 60 mW Sampling A/D Converter

AD775

FEATURES

CMOS 8-Bit 20 MSPS Sampling A/D Converter
Low Power Dissipation: 60 mW
+5 V Single Supply Operation
Differential Nonlinearity: 0.3 LSB
Differential Gain: 1%
Differential Phase: 0.5 Degrees
Three-State Outputs
On-Chip Reference Bias Resistors
Adjustable Reference Input
Video Industry Standard Pinout
Small Packages:
24-Pin, 300 Mil SOIC Surface Mount
24-Pin, 400 Mil Plastic DIP

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD775 is a CMOS, low power, 8-bit, 20 Msps sampling analog-to-digital converter (ADC). The AD775 features a built-in sampling function and on-chip reference bias resistors to provide a complete 8-bit ADC solution. The AD775 utilizes a pipelined/ping pong two-step flash architecture to provide high sampling rates (up to 35 MHz) while maintaining very low power consumption (60 mW).

Its combination of excellent DNL, fast sampling rate, low differential gain and phase errors, extremely low power dissipation, and single +5 V supply operation make it ideally suited for a variety of video and image acquisition applications, including portable equipment. The AD775's reference ladder may be connected in a variety of configurations to accommodate different input ranges. The low input capacitance (11 pF typical) provides an easy-to-drive input load compared to conventional flash converters.

The AD775 is offered in both 300 mil SOIC and 400 mil DIP plastic packages, and is designed to operate over an extended commercial temperature range (−20°C to +75°C).

PRODUCT HIGHLIGHTS

Low Power: The AD775 has a typical supply current of 12 mA, for a power consumption of 60 mW. Reference ladder current is also low: 6.6 mA typical, minimizing the reference power consumption.

Complete Solution: The AD775's switched capacitor design features an inherent sample/hold function: no external SHA is required. On-chip reference bias resistors are included to allow a supply-based reference to be generated without any external resistors.

Excellent Differential Nonlinearity: The AD775 features a typical DNL of 0.3 LSBs, with a maximum limit of 0.5 LSBs. No missing codes is guaranteed.

Single +5 V Supply Operation: The AD775 is designed to operate on a single +5 V supply, and the reference ladder may be configured to accommodate analog inputs inclusive of ground.

Low Input Capacitance: The 11 pF input capacitance of the AD775 can significantly decrease the cost and complexity of input driving circuitry, compared with conventional 8-bit flash ADCs.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

RESOLUTION	8			Bits
DC ACCURACY				
Integral Nonlinearity (INL)		+0.5	1.3	LSB
Differential Nonlinearity (DNL)		±0.3	±0.5	LSB
No Missing Codes		GUARANTEED		
Offset				
To Top of Ladder V_{RT}	−10	−35	−60	mV
To Bottom of Ladder V_{RB}	0	+15	+45	mV
VIDEO ACCURACY[1]				
Differential Gain Error		1.0		%
Differential Phase Error		0.5		Degrees
ANALOG INPUT				
Input Range (V_{RT}–V_{RB})		2.0		V p-p
Input Capacitance		11		pF
AC SPECIFICATIONS[2]				
Signal-to-Noise and Distortion (S/(N+D))				
f_{IN} = 1 MHz		47		dB
f_{IN} = 5 MHz		41		dB
Total Harmonic Distortion (THD)				
f_{IN} = 1 MHz		−51		dB
f_{IN} = 5 MHz		−42		dB
REFERENCE INPUT				
Reference Input Resistance (R_{REF})	230	300	450	Ω
Case 1: V_{RT} = V_{RTS}, V_{RB} = V_{RBS}				
Reference Bottom Voltage (V_{RB})	0.60	0.64	0.68	V
Reference Span (V_{RT}–V_{RB})	1.96	2.09	2.21	V
Reference Ladder Current (I_{REF})	4.4	7.0	9.6	mA
Case 2: V_{RT} = V_{RTS}, V_{RB} = AV_{SS}				
Reference Span (V_{RT}–V_{RB})	2.25	2.39	2.53	V
Reference Ladder Current (I_{REF})	5	8	11	mA
POWER SUPPLIES				
Operating Voltages				
AV_{DD}	+4.75		+5.25	Volts
DV_{DD}	+4.75		+5.25	Volts
Operating Current				
IAV_{DD}		9.5		mA
IDV_{DD}		2.5		mA
IAV_{DD} + IDV_{DD}		12	17	mA
POWER CONSUMPTION		60	85	mW
TEMPERATURE RANGE				
Operating	−20		+75	°C

NOTES

[1]NSTC 40 IRE modulation ramp, CLOCK = 14.3 Msps.

[2]f_{IN} amplitude = −0.3 dB full scale.

Specifications subject to change without notice. See Definition of Specifications for additional information.

DIGITAL SPECIFICATIONS (CLOCK = 20 MHz unless otherwise noted)

Parameter	Symbol	DV_{DD}	AD775J Min	AD775J Typ	AD775J Max	Units
LOGIC INPUT						
High Level Input Voltage	V_{IH}	5.0	4.0			V
Low Level Input Voltage	V_{IL}	5.0			1.0	V
High Level Input Current ($V_{IH} = DV_{DD}$)	I_{IH}	5.25			5	μA
Low Level Input Current (V_{IL} = 0 V)	I_{IL}	5.25	−5			μA
Logic Input Capacitance	C_{IN}			5		pF
LOGIC OUTPUTS						
High Level Output Current						
$\overline{OE}$ = DV_{SS}, $V_{OH} = DV_{DD}-0.5$ V	I_{OH}	4.75			−1.1	mA
$\overline{OE}$ = DV_{DD}, $V_{OH} = DV_{DD}$	I_{OZ}	5.25			16	μA
Low Level Output Current						
$\overline{OE}$ = DV_{SS}, V_{OL} = 0.4 V	I_{OL}	4.75	3.7			mA
$\overline{OE}$ = DV_{DD}, V_{OL} = 0 V	I_{OZ}	5.25			16	μA

TIMING SPECIFICATIONS

	Symbol	Min	Typ	Max	Units
Maximum Conversion Rate		20	35		MHz
Clock Period	t_C	50			ns
Clock High	t_{CH}	25			ns
Clock Low	t_{CL}	25			ns
Output Delay	t_{OD}		18	30	ns
Pipeline Delay (Latency)				2.5	Clock Cycles
Sampling Delay	t_{DS}		4		ns
Aperture Jitter			30		ps

Specifications subject to change without notice.

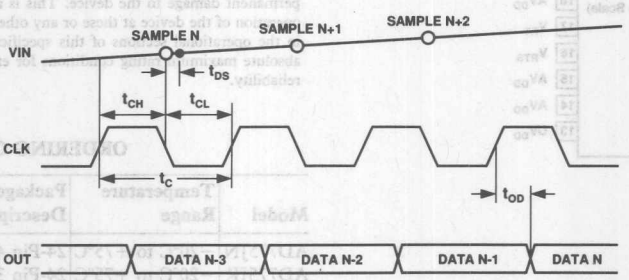


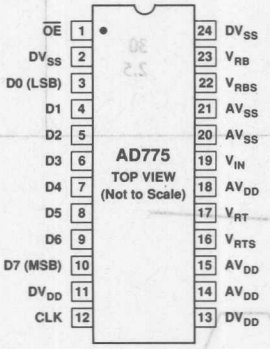
Figure 1. AD775 Timing Diagram

PIN DESCRIPTION

Pin No.	Symbol	Type	Name and Function
1	$\overline{OE}$	DI	$\overline{OE}$ = Low: Normal Operating Mode. $\overline{OE}$ = High: High Impedance Outputs.
2, 24	DV_{SS}	P	Digital Ground. Note: DV_{SS} and AV_{SS} pins should share a common ground plane on the circuit board.
3	D0 (LSB)	DO	Least Significant Bit, Data Bit 0.
4–9	D1–D6	DO	Data Bits 1 Through 6.
10	D7 (MSB)	DO	Most Significant Bit, Data Bit 7.
11, 13	DV_{DD}	P	+5 V Digital Supply. Note: DV_{DD} and AV_{DD} pins should share a common supply on the circuit board.
12	CLK	DI	Clock Input.
16	V_{RTS}	AI	Reference Top Bias. Short to V_{RT} for Self Bias.
17	V_{RT}	AI	Reference Ladder Top.
23	V_{RB}	AI	Reference Ladder Bottom.
22	V_{RBS}	AI	Reference Bottom Bias. Short to V_{RB} for Self Bias.
14, 15, 18	AV_{DD}	P	+5 V Analog Supply. Note: DV_{DD} and AV_{DD} pins should share a common supply within 0.5 inches of the AD775.
19	V_{IN}	AI	Analog Input. Input Span = V_{RT}–V_{RB}.
20, 21	AV_{SS}	P	Analog Ground. Note: DV_{SS} and AV_{SS} pins should share a common ground within 0.5 inches of the AD775.

NOTE
Type: AI = Analog Input; DI = Digital Input; DO = Digital Output; P = Power.

PIN CONFIGURATION (DIP and SOIC)



MAXIMUM RATINGS*

Supply Voltage (AV_{DD}, DV_{DD}) . . . . . 7 V
Supply Difference (AV_{DD}–DV_{DD}) . . . . . 0 V
Ground Difference (AV_{SS}–DV_{SS}) . . . . . 0 V
Reference Voltage (V_{RT}, V_{RB}) . . . . . V_{DD} to V_{SS}
Analog Input Voltage (V_{IN}) . . . . . V_{DD} to V_{SS}
Digital Input Voltage (CLK) . . . . . V_{DD} to V_{SS}
Digital Output Voltage (V_{OH},V_{OL}) . . . . . V_{DD} to V_{SS}
Storage Temperature . . . . . −55°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD775JN	−20°C to +75°C	24-Pin 400 Mil Plastic DIP	N-24B
AD775JR	−20°C to +75°C	24-Pin 300 Mil SOIC	R-24A

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD775 features ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

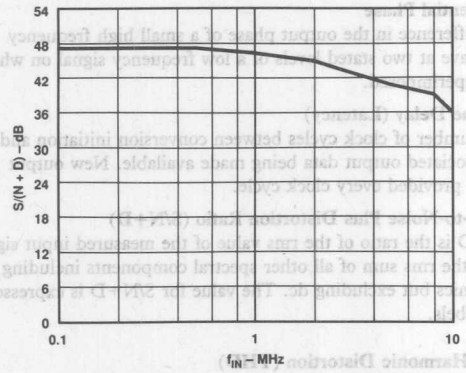


Figure 2. S/(N+D) vs. Input Frequency at 20 MSPS Clock Rate (V_{IN} = −0.3 dB)

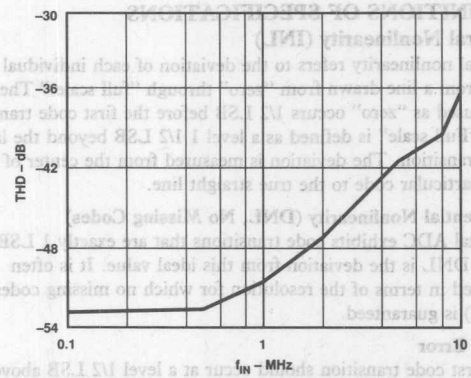


Figure 5. THD vs. Input Frequency at 20 MSPS Clock Rate (V_{IN} = −0.3 dB)

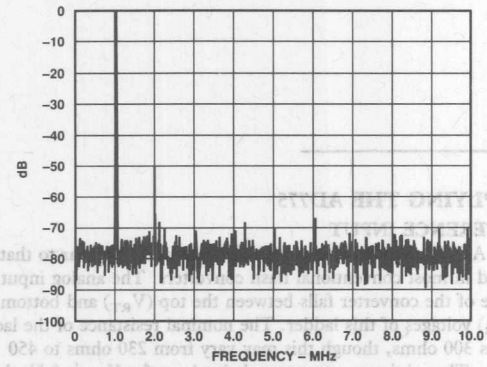


Figure 3. Typical FFT at 1 MHz Input, 20 MSPS Clock Rate (V_{IN} = −0.5 dB)

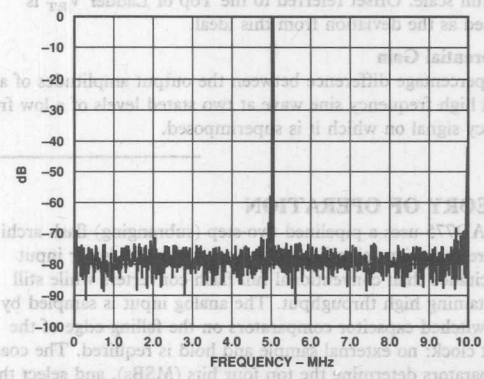


Figure 6. Typical FFT at 5 MHz Input, 20 MSPS Clock Rate (V_{IN} = −0.5 dB)

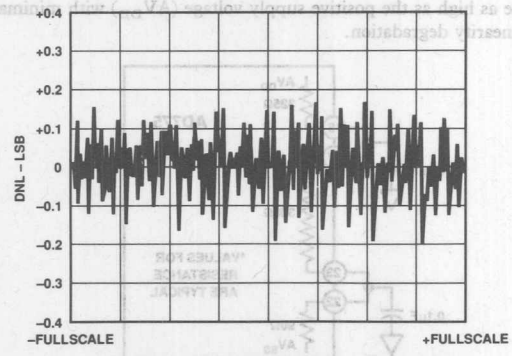


Figure 4. Typical Differential Nonlinearity (DNL)

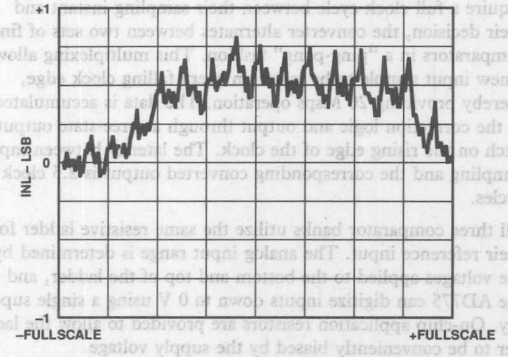


Figure 7. Typical Integral Nonlinearity (INL)

DEFINITIONS OF SPECIFICATIONS

Integral Nonlinearity (INL)

Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution for which no missing codes (NMC) is guaranteed.

Offset Error

The first code transition should occur at a level 1/2 LSB above nominal negative full scale. Offset referred to the Bottom of Ladder V_{RB} is defined as the deviation from this ideal. The last code transition should occur 1 1/2 LSB below the nominal positive full scale. Offset referred to the Top of Ladder V_{RT} is defined as the deviation from this ideal.

Differential Gain

The percentage difference between the output amplitudes of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed.

Differential Phase

The difference in the output phase of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed.

Pipeline Delay (Latency)

The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

Signal-to-Noise Plus Distortion Ratio (S/N+D)

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

THEORY OF OPERATION

The AD775 uses a pipelined two-step (subranging) flash architecture to achieve significantly lower power and lower input capacitance than conventional full flash converters while still maintaining high throughput. The analog input is sampled by the switched capacitor comparators on the falling edge of the input clock: no external sample and hold is required. The coarse comparators determine the top four bits (MSBs), and select the appropriate reference ladder taps for the fine comparators. With the next falling edge of the clock, the fine comparators determine the bottom four bits (LSBs). Since the LSB comparators require a full clock cycle between their sampling instant and their decision, the converter alternates between two sets of fine comparators in a "ping-pong" fashion. This multiplexing allows a new input sample to be taken on every falling clock edge, thereby providing 20 Msps operation. The data is accumulated in the correction logic and output through a three-state output latch on the rising edge of the clock. The latency between input sampling and the corresponding converted output is 2.5 clock cycles.

All three comparator banks utilize the same resistive ladder for their reference input. The analog input range is determined by the voltages applied to the bottom and top of the ladder, and the AD775 can digitize inputs down to 0 V using a single supply. On-chip application resistors are provided to allow the ladder to be conveniently biased by the supply voltage.

The AD775 uses switched capacitor auto-zeroing techniques to cancel the comparators' offsets and achieve excellent differential nonlinearity performance: typically ±0.3 LSB. The integral nonlinearity is determined by the linearity of the reference ladder and is typically +0.5 LSB.

APPLYING THE AD775

REFERENCE INPUT

The AD775 features a resistive reference ladder similar to that found in most conventional flash converters. The analog input range of the converter falls between the top (V_{RT}) and bottom (V_{RB}) voltages of this ladder. The nominal resistance of the ladder is 300 ohms, though this may vary from 230 ohms to 450 ohms. The minimum recommended voltage for V_{RB} is 0 V; the linearity performance of the converter may deteriorate for input spans (V_{RB}–V_{RB}) below 1.8 V. While 2.8 V is the recommended maximum ladder top voltage (V_{RT}), the top of the ladder may be as high as the positive supply voltage (AV_{DD}) with minimal linearity degradation.

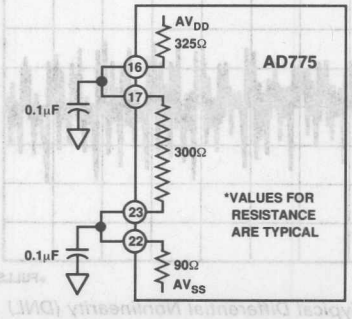


Figure 8. Reference Configuration: 0.64 V to 2.73 V

To simplify biasing of the AD775, on-chip reference bias resistors are provided on Pins 16 and 22. The two recommended configurations for these resistors are shown in Figures 8 and 9.

In the topology shown in Figure 8, the top of the ladder (V_{RT}) is shorted to the top bias resistor (V_{RTS}) (Pin 17 shorted to Pin 16), while the bottom of the ladder (V_{RB}) is shorted to the bottom bias resistor (V_{RBS}) (Pin 23 shorted to Pin 22). This creates a resistive path (nominally 725 ohms) between AV_{DD} and AV_{SS}. For nominal supply voltages (5 V and 0 V respectively), this creates an input range of 0.64 V to 2.73 V.

Both top and bottom of the reference ladder should be decoupled, preferably with a chip capacitor to ground to minimize reference noise.

The topology shown in Figure 9 provides a ground-inclusive input range. The bottom of the ladder (V_{RB}) is shorted to AV_{SS}. (0 V), while the top of the ladder (V_{RT}) is connected to the on-board bias resistor (V_{RTS}). This provides a nominal input range of 0 V to +2.4 V for AV_{DD} of 5 V. The V_{RBS} pin may be left floating, or shorted to AV_{SS}.

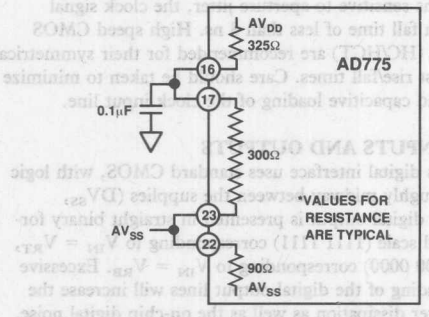


Figure 9. Reference Configuration: 0 V to +2.4 V

More elaborate topologies can be used for those wishing to provide an input span based on an external reference voltage. The circuit in Figure 10 uses the AD780 2.5 V reference to drive the top of the ladder (V_{RT}), with the bottom (V_{RB}) of the ladder grounded to provide an input span of 0 V to +2.5 V. This is modified in Figure 11 to shift the 2.5 V span up 700 mV.

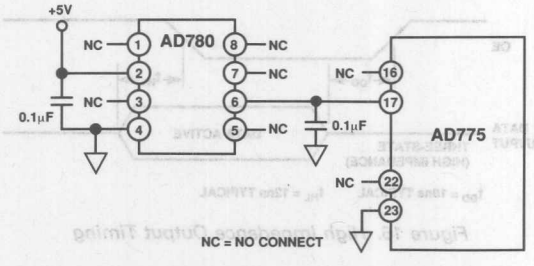


Figure 10. Reference Configuration: 0 V to 2.5V

The AD775 can accommodate dynamic changes in the reference voltage for gain or offset adjustment. However, conversions that are in progress, including those in the converter pipeline, while the reference voltages are changing will be invalid.

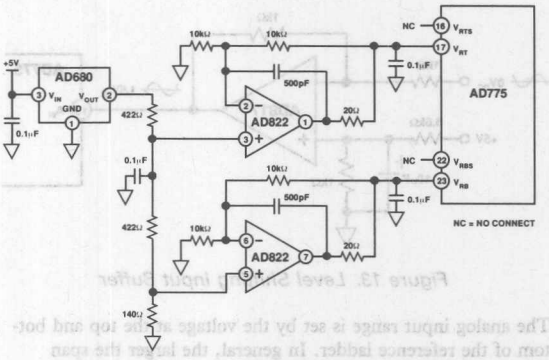


Figure 11. Reference Configuration: 0.7 V to 3.2 V

ANALOG INPUT

The impedance looking into the analog input is essentially capacitive, as shown in the equivalent circuit of Figure 12, typically totalling around 11 pF. A portion of this capacitance is parasitic; the remainder is part of the switched capacitor structure of the comparator arrays. The switches close on the rising edge of the clock, acquire the input voltage, and open on the clock's falling edge (the sampling instant). The charge that must be moved onto the capacitors during acquisition will be a function of the converter's previous two samples, but there should be no sample-to-sample crosstalk so long as ample driving impedance and acquisition time are provided.

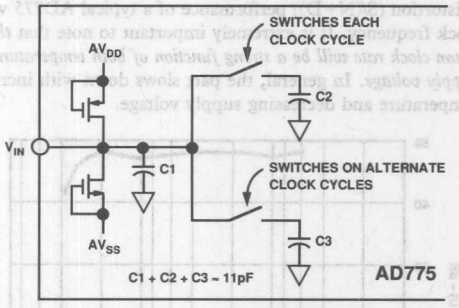


Figure 12. Equivalent Analog Input Circuit (V_{IN})

For example, to ensure accurate acquisition (to 1/4 bit accuracy) of a full-scale input step in less than 20 ns, a source impedance of less than 100 ohms is recommended. Figure 13 shows one option of input buffer circuitry using the AD817. The AD817 acts as both an inverting buffer and level shifting circuit. In order to level shift the ground-based input signal to the dc level required by the input of the AD775, the supply voltage is resistively divided to produce the appropriate voltage at the noninverting input of the AD817. For most applications, the AD817 provides a low cost, high performance level shifter. The AD811 is recommended for systems which require faster settling times.

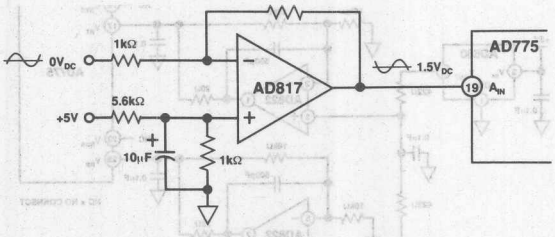


Figure 13. Level Shifting Input Buffer

The analog input range is set by the voltage at the top and bottom of the reference ladder. In general, the larger the span (V_{RT}–V_{RB}), the better the differential nonlinearity (DNL) of the converter; a 1.8 V span is suggested as a minimum to realize good linearity performance. As the input voltage exceeds 2.8 V (for AV_{DD} = 4.75 V), the input circuitry may start to slightly degrade the acquisition performance.

CLOCK INPUT

The AD775's internal control circuitry makes use of both clock edges to generate on-chip timing signals. To ensure proper settling and linearity performance, both t_{CH} and t_{CL} times should be 25 ns or greater. For sampling frequencies at or near 20 Msps, a 50% duty cycle clock is recommended. For slower sampling applications, the AD775 can accommodate a wider range of duty cycles, provided each clock phase is as least 25 ns.

Under certain conditions, the AD775 can be operated at sampling rates above 20 Msps. Figure 14 shows the signal-to-noise plus distortion (S/(N+D)) performance of a typical AD775 versus clock frequency. It is extremely important to note that *the maximum clock rate will be a strong function of both temperature and supply voltage*. In general, the part slows down with increasing temperature and decreasing supply voltage.

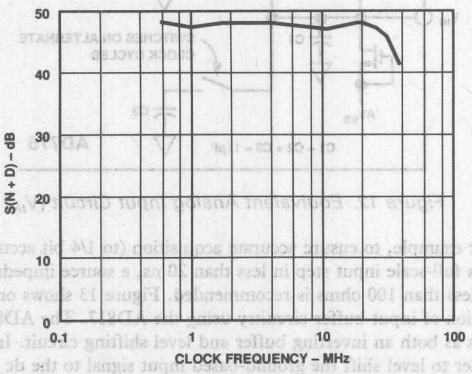


Figure 14. S(N+D) vs. Clock Frequency (Temperature = +25°C)

A significant portion of the AD775's power dissipation is proportional to the clock frequency: Figure 15 illustrates this tradeoff for a typical part.

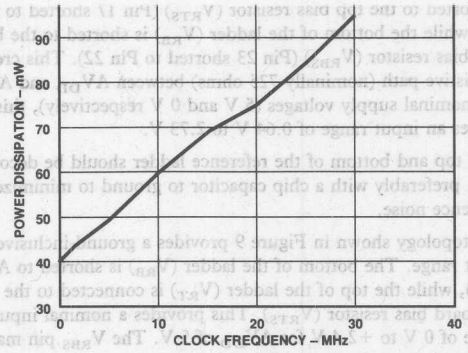


Figure 15. Power Dissipation vs. Clock Frequency

In applications sensitive to aperture jitter, the clock signal should have a fall time of less than 3 ns. High speed CMOS logic families (HC/HCT) are recommended for their symmetrical swing and fast rise/fall times. Care should be taken to minimize the fanout and capacitive loading of the clock input line.

DIGITAL INPUTS AND OUTPUTS

The AD775's digital interface uses standard CMOS, with logic thresholds roughly midway between the supplies (DV_{SS}, DV_{DD}). The digital output is presented in straight binary format, with full scale (1111 1111) corresponding to V_{IN} = V_{RT}, and zero (0000 0000) corresponding to V_{IN} = V_{RB}. Excessive capacitive loading of the digital output lines will increase the dynamic power dissipation as well as the on-chip digital noise. Logic fanout and parasitic capacitance on these lines should be minimized for optimum noise performance.

The data output lines may be placed in a high output impedance state by bringing $\overline{OE}$ (Pin 1) to a logic high. Figure 16 indicates typical timing for access and float delay times (t_{HL} and t_{DD} respectively). Note that even when the outputs are in a high impedance state, activity on the digital bus can couple back to the sensitive analog portions of the AD775 and corrupt conversions in progress.

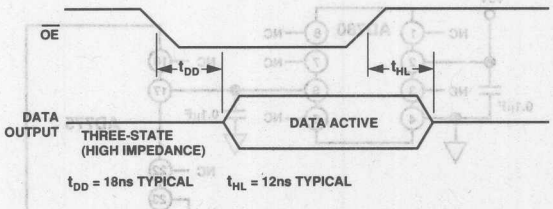


Figure 16. High Impedance Output Timing

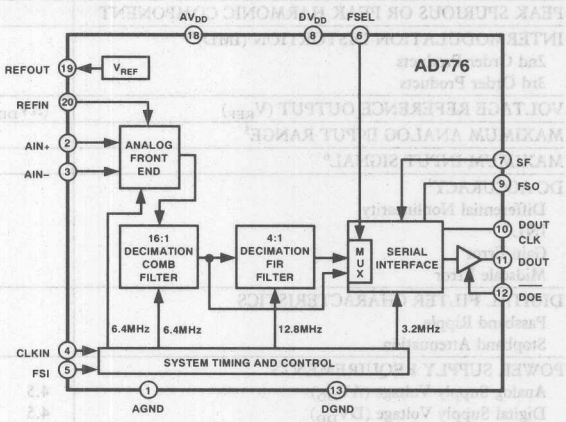
16-Bit 100 kSPS Oversampling ADC

AD776

FEATURES
- Monolithic 16-Bit Sigma-Delta ADC
- Third-Order Noise Shaping
- 96 dB Dynamic Range
- 90 dB SNR
- 16-Bit 100 kHz Output from FIR Filter
- 12-Bit 400 kHz Output from Comb Filter
- No Missing Codes
- <0.001 dB In-Band Ripple

APPLICATIONS
- Digital Audio Disk/Tape
- Voice Bandwidth Communications
- ADC Support for ADSP-21XX
- High Accuracy Measurement Systems

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD776 is a 16-bit sigma-delta oversampled ADC, incorporating a 1-bit third-order modulator and digital decimation filter. An on-chip voltage reference circuit is also included.

The AD776 does not generally require the use of sample-hold circuits or complex antialiasing filters as a result of its sigma-delta architecture. The output is available both before and after the final Finite Impulse Response (FIR) decimation filter. This provides the flexibility of optimizing conversion speed or dynamic range: 12-bit/400 kHz (from the comb filter) or 16-bit/100 kHz (from the FIR filter). The serial port provides easy interface with a variety of standard processors including the ADSP-21XX.

The AD776 is specified for ac (or "dynamic") parameters such as SNR, THD and IMD which are important in signal processing and audio applications. Third order noise shaping is employed using 64 times oversampling to provide 90 dB SNR and −100 dB peak spurious component for signal bandwidths up to 45 kHz.

The AD776 operates from a single +5 V supply and typically consumes 350 mW during conversion. The device is packaged in 20-pin ceramic DIP (cerdip) and is offered in an industrial temperature grade (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. Analog Front End. The analog input is differential providing increased signal swing, increased power supply rejection ratio, and reduced sensitivity to clock jitter. Since the input signal is oversampled by a factor of 64, a complex antialiasing filter is not needed.
2. Flexible Digital Interface. The AD776 has three output pins for the serial interface: 1) serial data out (DOUT), 2) frame sync out (FSO), and 3) serial clock out (DOUT CLOCK). The serial port can interface with general purpose DSPs such as the ADSP-21XX, TMS320XX, and DSP56001/2 without additional "glue" logic.
3. Inherently Self-Sampling. The AD776 needs no external sample-and-hold amplifier to capture and freeze the analog input while the conversion takes place.
4. Speed/Performance Options. In addition to the standard 16-bit resolution at 100 kHz, the output of the comb filter can be accessed to provide 12-bit resolution at 400 kHz.

AD776—SPECIFICATIONS (T_{MIN} to T_{MAX}; AV_{DD}, DV_{DD} = +5 V, FIR filter output mode unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	16			Bits
TEMPERATURE RANGE	−40		+85	°C
TOTAL HARMONIC DISTORTION (THD)[1, 2, 3]	−80	−83		dB
	0.01	0.003		%
SIGNAL-TO-NOISE RATIO (SNR)[1, 2], f_S = 48 ksps	88	90		dB
Signal to Noise-Ratio (SNR)[1, 2], f_S = 100 ksps		86		dB
Comb Filter Mode, CLKIN = 12.8 MHz		72		dB
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−100		dB
INTERMODULATION DISTORTION (IMD)[4]				
2nd Order Products		−102		dB
3rd Order Products		−98		dB
VOLTAGE REFERENCE OUTPUT (V_{REF})	(AV_{DD} × 0.4) − 4%	AV_{DD} × 0.4 V	(AV_{DD} × 0.4) + 4%	V
MAXIMUM ANALOG INPUT RANGE[5]		2 × V_{REF} − 0.5		V p–p
MAXIMUM INPUT SIGNAL[6]		±0.5 V_{REF}		V p–p
DC ACCURACY[1]				
Differential Nonlinearity		±0.5		LSB
INL		2		LSB
Gain Error		1.0		%
Midscale Error		0.5		%
DIGITAL FILTER CHARACTERISTICS				
Passband Ripple		0.001		dB
Stopband Attenuation		−96		dB
POWER SUPPLY REQUIREMENTS[7]				
Analog Supply Voltage (AV_{DD})	4.5	5.0	5.5	V
Digital Supply Voltage (DV_{DD})	4.5		AV_{DD}	V
Analog Supply Current		20		mA
Digital Supply Current		20		mA
Power Consumption[8]		300	400	mW
Power Supply Rejection[9]		70		dB

DIGITAL SPECIFICATIONS

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
I_{IH}	High Level Input Current	V_{IH} = V_{DD}		1		μA
I_{IL}	Low Level Input Current	V_{IL} = 0 V		1		μA
C_{IN}	Input Capacitance			10		pF
I_Z	Hi-Z Input Current for SDO				10	μA
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.4 mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.0 mA			0.5	V

NOTES
[1]At +25°C.
[2]Analog Input = 1.2 V rms @ 10 kHz, $V_{COMMON\ MODE}$ = 2.5 V, CLKIN = 6.4 MHz.
[3]THD performance can be improved, depending upon the application, by making slight adjustments to the dc common mode voltage at the analog inputs.
[4]IMD measured at f_s = 48 kHz and using 61.6 Hz and 986.4 Hz as the input tones (sum of the two peaks added to be −3 dB FS).
[5]Applied differentially between AIN+ and AIN−.
[6]The input signal may be centered at any choice of dc offset voltage as long as peak values are bounded by the Maximum Analog Input Range value. Performance may be improved by reducing the maximum input signal by 3 dB. For nominal operation, 2.5 V dc offset is recommended.
[7]The AD776 may be operated from a single +5 V supply.
[8]AV_{DD}, DV_{DD} = 5.5 V; f = 12.8 MHz; T_A = +85°C.
[9]With external voltage reference.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (AV_{DD}, DV_{DD} = +5 V ± 10%, T_{MIN} to T_{MAX}) — see Figures 14 through 18.

Symbol	Parameter	Min	Max	Units
f	Clock in Frequency	1	12.8	MHz
t_{CLK}	Clock in Period (= 1/f)	78	1000	ns
t_D	Duty Cycle	0.475 t_{CLK}	0.525 t_{CLK}	ns
t_{CL}	Clock LOW	37	41	ns[1]
		475	525	ns[2]
t_{CH}	Clock HIGH	37	41	ns[1]
		475	525	ns[2]
t_R	Rise Time	5		ns
t_F	Fall Time	5		ns
t_{FSS}	Frame Sync Input Setup Time	20	78	ns
t_{FSH}	Frame Sync Input Hold Time	20	–[3]	ns
t_{FSIL}	Frame Sync Input LOW	2		t_{CLK}
t_{DOD}	Data Output Clock Delay	25	75	ns
t_{DOP}	Data Output Clock Period	156		ns[1, 4]
			312	ns[1, 5]
t_{FSOSC}	FSO Setup Time Before CLKIN	130		ns[5]
t_{FSOHC}	FSO Hold Time After CLKIN	130		ns[5]
t_{FSOSD}	FSO Setup Time Before DOUT CLK	110		ns[5]
t_{FSOHD}	FSO HIGH to DOUT CLK Rising Edge	110		ns[5]
t_{IO}	FSI to FSO Delay	1		t_{CLK}[4]
		5		t_{CLK}[5]
t_{DSU}	Data Output Setup Time	40		ns[4]
		130		ns[5]
t_{DH}	Data Output Hold Time	40		ns[4]
		130		ns[5]
t_{DD}	Data Delay Time	0	20	ns
t_{DF}	Data Float Time	0	20	ns

NOTES
[1]CLKIN = 12.8 MHz.
[2]CLKIN = 1 MHz.
[3]FSI must be deasserted for at least two CLKIN periods prior to being asserted.
[4]Comb Filter mode.
[5]FIR Filter mode.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

AV_{DD} to AGND	−0.3 V to +7.0 V
DV_{DD} to DGND	−0.3 V to +7.0 V
AGND to DGND	±0.3 V
Digital Inputs to DGND	−0.3 V to DV_{DD}
Analog Inputs to AGND	−0.3 V to AV_{DD}
REFIN to AGND	−0.3 V to +2.5 V
Soldering (10 sec)	+300°C
Storage Temperature	−55°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

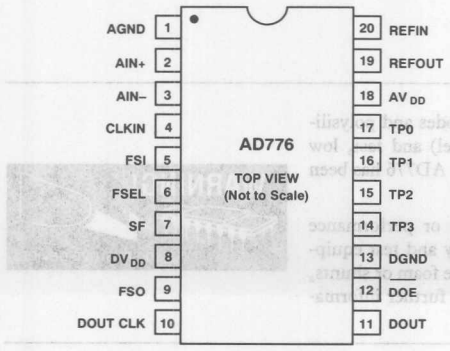
The AD776 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD776 has been classified as a Category 1 Device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment, and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam discharged to the destination socket before devices are removed. For further information on ESD precaution, refer to Analog Devices' *ESD Prevention Manual*.

Symbol	Pin Number	Type	Name and Function
AGND	1		Analog Ground. Return current for analog front end. No internal connection to DGND.
AIN+	2	I	Analog Signal Input. Noninverting terminal.
AIN–	3	I	Analog Signal Input. Inverting terminal.
CLKIN	4	I	Clock In. This TTL compatible input accepts clock frequencies in the range of 1.0 MHz–12.8 MHz, with the output sample rate of the AD776 equal to CLKIN divided by 128 in FIR filter mode and 32 in comb filter mode.
FSI	5	I	Frame Sync Input. FSI is an optional control pin used to synchronize internal circuits and to start or reset the serial output data. If FSI is grounded, frame syncs will be automatically generated internally. When FSI is brought HIGH, serial data is presented at the output (DOUT–Pin 11). The purpose of FSI is to control externally the phasing of the A/D conversion process. FSI should be a periodic signal occurring every 16 DOUT CLK clock cycles in the 12-bit/400 kHz mode and every 32 DOUT CLK clock cycles in the 16-bit/ 100 kHz mode. When utilized, FSI must be synchronized to CLKIN as defined in the timing specification (see Figure 17). FSI allows multiple AD776s to be synchronized using a common frame sync source, requiring a common CLKIN signal.
FSEL	6	I	Filter Select. FSEL = "0" selects FIR output. FSEL = "1" selects comb filter output.
SF	7	I	Serial Format. Selects output format of DOUT and FSO when FSEL = "0." See Figures 14b and 15b.
DV_{DD}	8		+5 V ±10%. Digital Power Supply.
FSO	9	O	Frame Sync Output. Indicates beginning of serial data transmission on DOUT. See Timing Diagrams.
DOUT CLK	10	O	Serial Data Clock. See Figures 14a and 14b. In the FIR filter output mode (FSEL = 0), DOUT CLK is CLKIN divided by four; in the comb filter output mode (FSEL = 1), DOUT CLK is CLKIN divided by two.
DOUT	11	O	Data Output. Serial data is transmitted MSB first, twos complement format, once per FSO cycle with the data synchronous with DOUT CLK.
$\overline{DOE}$	12	I	Data Output Enable. Serial data (Pin 11) is an active output when $\overline{DOE}$ = "0." Serial data is three stated when $\overline{DOE}$ = "1."
DGND	13		Digital Ground. Return current for digital circuitry and pad drivers.
TP3, TP2, TP1, TP0	14, 15, 16, 17		Test Points. These pins must be connected to DGND.
AV_{DD}	18		+5 V ±10%. Analog Power Supply.
REFOUT	19	O	Internal Reference Output. Nominally +2 V with AV_{DD} = +5.0 V.
REFIN	20	I	Reference Input. +2 V maximum.

I = Input
O = Output

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD776AQ	–40°C to +85°C	20-Pin Cerdip	Q-20

*For outline information see Package Information section.

TOTAL HARMONIC DISTORTION
Total Harmonic Distortion (THD) is the ratio of the rms sum of the harmonic components to the rms value of a full-scale input signal and is expressed in percent (%) or decibels (dB).

SIGNAL-TO-NOISE RATIO (SNR)
Signal-to-Noise Ratio (SNR) is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the passband.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa± nfb, where m, n = 0, 1, 2, 3. . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa+fb) and (fa−fb), and the third order terms are (2fa+fb), (2fa−fb), (fa+2fb) and (fa−2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the IMD products are normalized to a 0 dB input signal.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are one LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

INTEGRAL NONLINEARITY (INL)
The ideal transfer function for an ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the most negative code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the most positive code transition. INL is the worst-case deviation of a code center average from the straight line.

GAIN ERROR
The last transition should ideally occur at an analog value 1.5 LSB below the nominal full scale. The gain error is the deviation of the actual difference between the first and last code transition from the ideal difference between the first and last code transition.

MIDSCALE ERROR
Midscale error is the difference between the ideal midscale analog input voltage and the actual voltage producing the midscale output code.

PASSBAND
The passband is the region of the frequency spectrum unaffected by the attenuation of the decimation filter. In the case of the AD776, the passband is a function of the CLKIN frequency (see Table I).

PASSBAND RIPPLE
Passband ripple is defined as the variation in the amplitude response of the converter for input signal frequencies within the passband.

STOPBAND
The stopband is the region of the frequency spectrum in which the amplitude response is fully attenuated by the digital filter. In the case of the AD776, the stopband is a function of the CLKIN frequency (see Table I).

STOPBAND ATTENUATION
Stopband attenuation is defined to be the amount by which spectral components in the stopband are attenuated by the digital filter relative to the full-scale input range of the converter.

POWER SUPPLY REJECTION
DC variations in the power supply voltage will affect the midscale transition point, resulting in offset error. Power supply rejection is the maximum change in the midscale transition point due to a change in power-supply voltage from the nominal value. Additionally, there is another power supply variation to consider. AC ripple on the power supplies can couple noise into the ADC, resulting in degradation of dynamic performance.

GENERAL OVERVIEW
The AD776 is a single supply (+5 V) ADC providing simple analog and digital interface requirements. A minimal number of external connections are required to achieve the specified performance:

1. POWER
2. GROUNDS
3. CLOCKING
4. INPUT BUFFER CIRCUIT

These points will be further explored in the Application Information section.

THEORY OF OPERATION
The AD776 differs from traditional multi-bit ADCs through its use of sigma-delta conversion architecture. A 1-bit analog-to-digital conversion is performed at a very high rate, which redistributes quantization noise to beyond the frequency band of interest (see Figure 1). The frequency band of interest is denoted by f_C, and f_S is the sample frequency; $f_S/2$ is the expanded noise spectrum resulting from oversampling. The total noise energy remains constant, but by spreading it over a wider spectrum, the amount in the frequency band of interest is reduced. Noise shaping, performed by the modulator, attenuates noise in the signal passband and pushes out the noise energy into the higher frequency range (Figure 2). The oversampled signal is presented to the digital filter circuitry for:

- sophisticated averaging (filtering).
- removing high frequency noise (quantization noise removal).
- reducing sampling rate (decimation).

The resulting output data stream is presented in a format equivalent to a traditional ADC at a much reduced output sample rate.

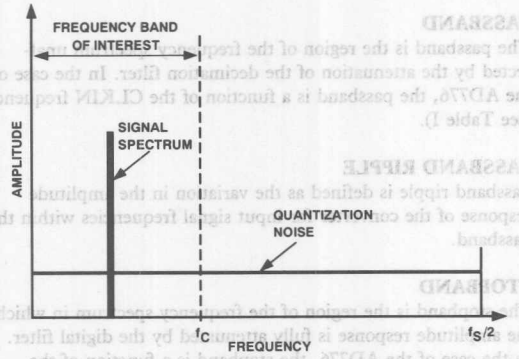


Figure 1. Noise Spectrum from Oversampling

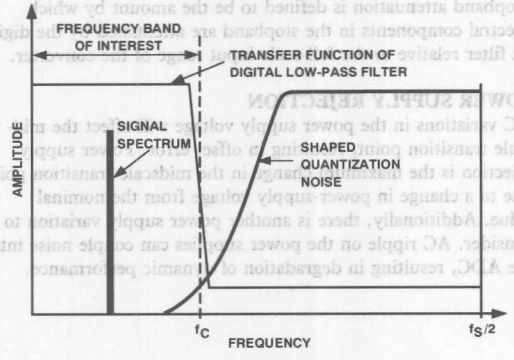


Figure 2. Noise Shaping

Figure 3 provides a block diagram of the various sections of the AD776. The Analog Front End is comprised of three differential switched-capacitor linear integrators which perform the noise-shaping function. Digital filter complexity of the AD776 is reduced by performing the filtering and decimation in two stages. The first section contains a 16:1 decimating comb filter stage with the output presented to a 4:1 decimating low-pass/compensation FIR filter, resulting in a final decimation ratio of 64:1. The decimation function is described in detail in the DECIMATION paragraph. The output data is presented in twos complement, MSB first serial data format, providing serial communication to a host processor.

This interface uses three dedicated pins: serial data output (DOUT), frame sync output (FSO), and serial clock output (DOUT CLK). The serial interface format of operation is pin selectable. The timing diagrams for the serial interface are described in the **DIGITAL TIMING** section.

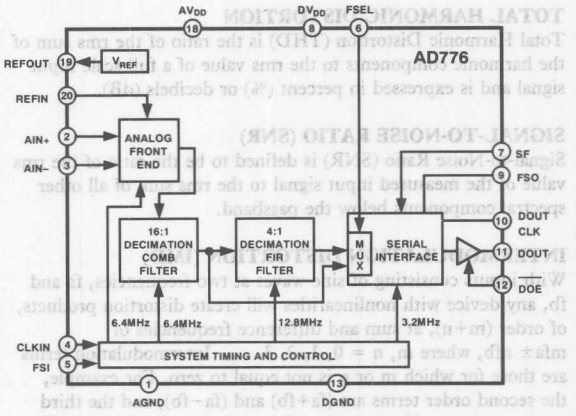


Figure 3. Block Diagram

ANALOG FRONT-END

The integrators of the third-order modulator front-end form a differential switched-capacitor network which results in increased signal swing, increased power supply rejection, and reduced sensitivity to clock jitter. Due to the nature of switched-capacitor circuits, the input impedance of AIN+, AIN−, and REFIN will vary with clock frequency. More information about these inputs is given in Table II and Table III.

The AD776 modulator is a third-order noise shaper which reduces quantization noise in the passband to the 16-bit level. The input signal is sampled at the rate of CLKIN/4. Since the input signal is oversampled by a factor of 64, a complex anti-aliasing filter is not needed; a single-pole RC filter will generally be sufficient. High quality polystyrene or NPO ceramic capacitors should be used for this filter.

DIGITAL FILTER OVERVIEW

The digital filters of the AD776 have two functions: high performance low-pass filtering and digital decimation. The shaped quantization noise from the output of the modulator is low-pass filtered to reduce the out-of-band noise components to a level which will not alias into the passband during the decimation process. Decimation then reduces the data rate to a manageable level.

DECIMATION

The comb filter performs the first-stage filtering of the analog front-end's quantized and noise-shaped output and decimates the input sample rate by a factor of 16:1. The z-domain transfer function for the comb filter is expressed by

$$H(z) = \frac{(1 - z^{-16})^4}{(1 - z^{-1})^4}$$

The frequency domain equivalent transfer function is

$$H(f) = \left[\frac{1}{16}\frac{sin\,(16\,\pi\,fT)}{sin\,(\pi\,fT)}\right]^4$$

where $T = 1/f_S$

f_S = the input sample rate for the Analog Front End (maximum 6.4 MHz).

The attenuation characteristics of the comb filter are shown in Figure 4. As illustrated, the frequency response in the passband region exhibits a nonflat behavior. In the 400 kHz mode, the output of the comb filter provides conversion data. The dynamic range is equivalent to approximately 72 dB, or 12 bits, in this mode. In the 16-bit/100 kHz mode, the comb filter serves as the input to the FIR filter. The FIR filter compensates for the passband roll-off of the comb filter and provides the final sharp cutoff required for stopband attenuation, removing the out-of-band noise components while partially serving as the system antialiasing filter.

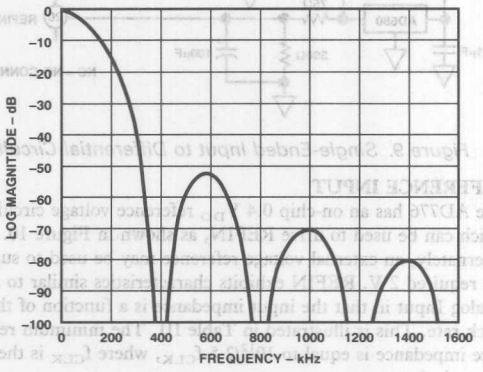


Figure 4. Comb Filter Response

Figure 5 illustrates the low-pass response of the FIR filter and Figure 6 shows the compensation function of the filter. The 255-tap FIR filter is low-pass with 9% transition-band, and with a CLKIN frequency of 12.8 MHz has a 45.5 kHz passband cutoff frequency, 50 kHz stopband frequency, 0.001 dB passband ripple, and a stopband ripple of −96 dB.

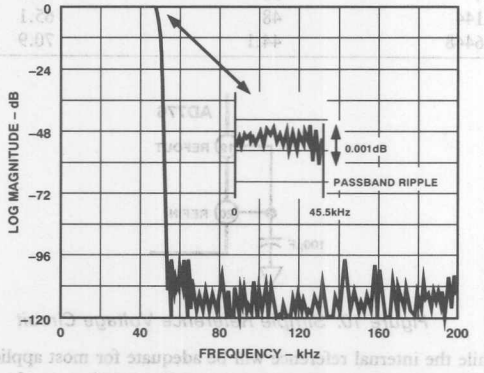


Figure 5. FIR Filter, Low-Pass Response

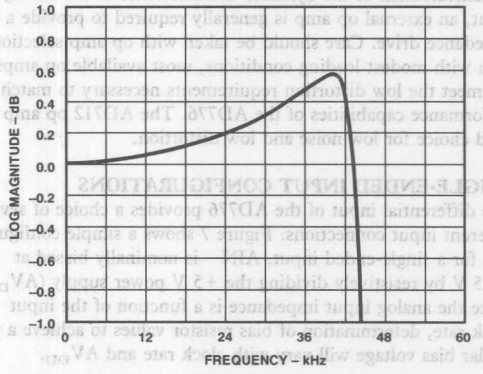


Figure 6. FIR Filter, Compensation Function

The passband and stopband frequencies of both the comb and FIR filters scale linearly with the CLKIN frequency, as shown in Table I.

Table I. FIR and Comb Filter Characteristics

CLKIN (MHz)	Passband (kHz)	Stopband (kHz)
12.8	45.5	50
12.288	43.7	48
11.2896	40.1	44.1
10.0	35.5	39.1
6.4	24.6	27.1

ANALOG INPUT

The input to the AD776, as previously described in the discussion of the analog front end, uses a switched-capacitor structure. As a result, the input impedance of AIN+ and AIN− will vary with clock frequency. Table II gives the typical analog input impedance for some common CLKIN frequencies. The input impedance is equal to $\approx 10^{12}/3f_{CLKIN}$, where f_{CLKIN} is the input clock rate.

Table II. Analog Input Impedance

Input Clock Rate (MHz)	Output Sample Rate (kHz) (FIR Filter Mode)	Analog Input Impedance (kΩ)
12.8	100	26
6.4	50	52
6.144	48	54.3
5.6448	44.1	59

The AD776 is designed to accept input signals of $(2 \times V_{REF})$ −0.5 V which can be centered at various dc offsets (common-mode inputs) as long as the signal peaks are bounded by +4.0 V and 0 V. Signal peaks outside this range will result in signal clipping and increased distortion products.

Capacitive coupling between the CLKIN and AIN pins can cause degradation to dynamic performance. Special care should be taken with respect to the layout of the clock and analog inputs.

input, an external op amp is generally required to provide a low impedance drive. Care should be taken with op amp selection; even with modest loading conditions, most available op amps do not meet the low distortion requirements necessary to match the performance capabilities of the AD776. The AD712 op amp is a good choice for low noise and low distortion.

SINGLE-ENDED INPUT CONFIGURATIONS

The differential input of the AD776 provides a choice of several different input connections. Figure 7 shows a simple configuration for a single-ended input. AIN− is nominally biased at +2.5 V by resistively dividing the +5 V power supply (AV_{DD}). Since the analog input impedance is a function of the input clock rate, determination of bias resistor values to achieve a particular bias voltage will vary with clock rate and AV_{DD}.

The circuit shown in Figure 7 is a low cost, minimal component solution, but may suffer from poor power supply rejection as noise present on the power supply could be coupled directly into the AIN− pin. An improved input circuit is shown in Figure 8, where the offset voltage is derived from the AD680 voltage reference. The AD680 has 40 μV/V line regulation which results in only a 20 μV error due to 10% supply fluctuation. This improves power supply rejection of AIN− input to approximately 88 dB.

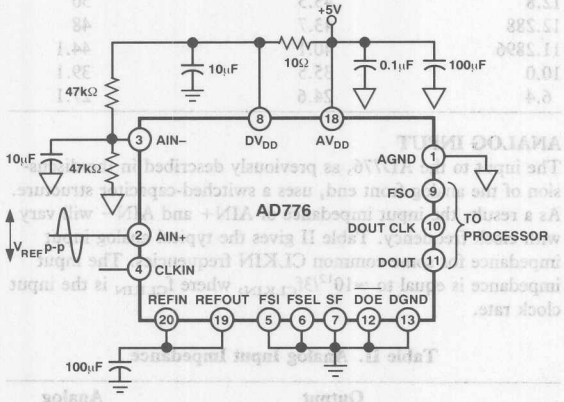


Figure 7. Simple Single-Ended Input Circuit

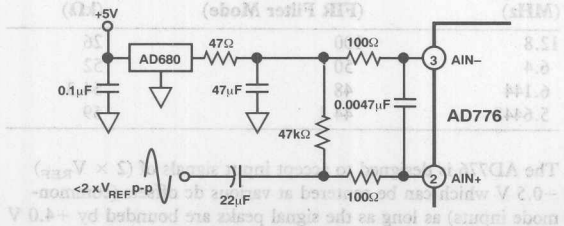


Figure 8. Single-Ended Input Circuit for Improved PSRR

For optimal performance in single-ended input applications, the circuit in Figure 9 may be used to convert the input to a differential signal.

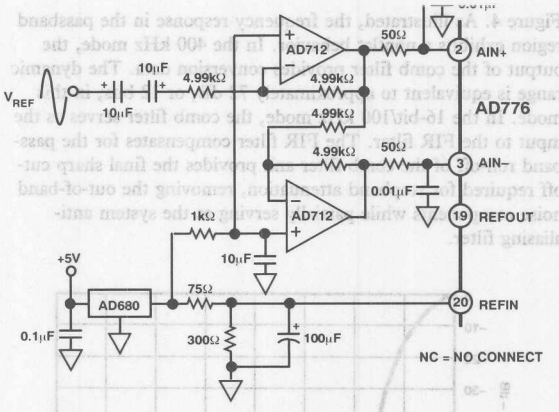


Figure 9. Single-Ended Input to Differential Circuit

REFERENCE INPUT

The AD776 has an on-chip 0.4 V_{DD} reference voltage circuit which can be used to drive REFIN, as shown in Figure 10. Alternately, an external voltage reference may be used to supply the required 2 V. REFIN exhibits characteristics similar to the Analog Input in that the input impedance is a function of the clock rate. This is illustrated in Table III. The minimum reference impedance is equal to $10^{12}/2.5\ f_{CLK}$, where f_{CLK} is the input clock rate.

Table III. Reference Input Impedance

Input Clock Rate (MHz)	Output Sample Rate (kHz)	Reference Input Impedance (kΩ min)
12.8	100	31.3
6.4	50	62.5
6.144	48	65.1
5.6448	44.1	70.9

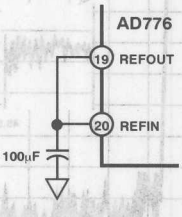


Figure 10. Simple Reference Voltage Circuit

While the internal reference will be adequate for most applications, power supply rejection and overall regulation may be improved through the use of an external reference. The process of selecting an external voltage reference should include consideration of drive capability, initial error, noise, and drift characteristics. A suitable choice would be the AD680 as shown in Figure 11.

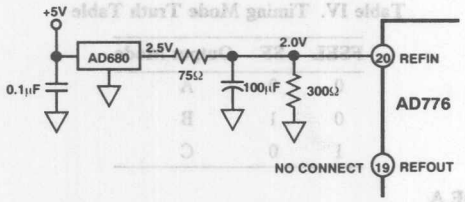


Figure 11. External Voltage Reference Circuit

MULTIPLEXING

The AD776 can also be used with an input multiplexer when the comb filter output is selected by setting FSEL = 1. If f_{CLK} = 12.8 MHz, the minimum multiplex intervals are (including the time to shift the data out from the serial interface):

15 μs (if the FSI and mux are perfectly synchronized)
17.5 μs (if the FSI and mux are not synchronized).

CLOCK GENERATION

With sigma-delta converters, it is critical that clock jitter be minimized in order to achieve optimal performance. Figure 12 illustrates a simple circuit used to derive a clock source for the AD776. An alternative would be to use an oscillator such as the CK1100 series from Cardinal Components (Montclair, NJ) or the F1100 from Fox Electronics. Compared with performance obtained with a typical crystal, use of an oscillator improves SNR by approximately 4 dB.

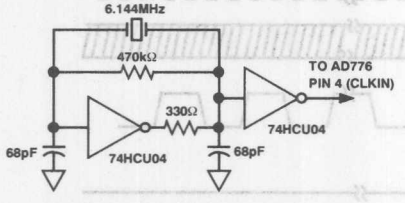


Figure 12. Basic Clock Circuit

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 20 LSBs at the 16 bit level for a 2 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals.

Analog and digital signals should not share a common return path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point at (or under) the part to minimize ground loops. This is preferred to interconnecting the grounds at the supplies.

Analog signals should be routed as far as possible from digital signals and should cross them, if at all, only at right angles. The AD776 may be treated as an analog component, with both AGND and DGND connected to a single analog ground plane. This helps to isolate the AD776 from large digital ground currents. For these reasons, the use of wire wrap circuit construction will not provide adequate performance; careful printed circuit board construction is preferred.

POWER SUPPLIES AND DECOUPLING

With high performance linear circuits, changes in the power supplies can produce undesired changes in the performance of the circuit. Optimally, well regulated power supplies with less than 1% ripple should be selected. The ac output impedance of a power supply is a complex function of frequency, but in general will increase with frequency. High frequency switching such as that encountered with digital circuitry requires fast transient currents which most power supplies cannot adequately provide. This results in voltage spikes on the supplies. To compensate for the finite ac output impedance of the supplies, it is necessary to store "reserves" of charge in bypass capacitors. These capacitors can effectively lower the ac impedance presented to the AD776 power inputs which in turn will significantly reduce the magnitude of the voltage spikes. Decoupling capacitors, typically 0.1 μF, should be placed as close as possible to each power supply pin of the AD776. It is essential that these capacitors be placed physically close to the AD776 to minimize the inductance of the PCB trace between the capacitor and the supply pin.

Additionally, it is beneficial to have large capacitors (>47 μF) located at the point where the power connects to the PCB with 10 μF capacitors located in the vicinity of the ADC to further reduce low frequency ripple.

The AD776 may be operated from a single +5 V supply. However, performance is optimized by using separate analog (AV_{DD}) and digital (DV_{DD}) supplies. Separate supplies enable isolation of digital noise from the analog circuitry. When separate supplies are used, AV_{DD} should be decoupled to analog ground (AGND) and DV_{DD} should be decoupled to digital ground (DGND) with decoupling capacitors.

When a single +5 V supply is used, the circuit shown in Figure 13 provides adequate decoupling.

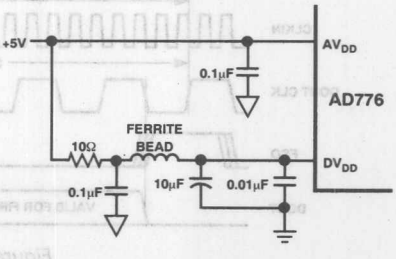


Figure 13. Single Supply Decoupling

DIGITAL TIMING

The CLKIN frequency and the choice of output filter mode (FIR or Comb) determine the output sample rate of the AD776. With FSEL LOW, the FIR filter output is selected and the output rate is equal to CLKIN divided by 128. When FSEL is HIGH, the Comb filter is selected and the output sample rate is equal to CLKIN divided by 32. The input sample rate (or modulator frequency) is always the CLKIN frequency divided by 2.

The flexible serial data output interface of the AD776 may be configured in one of three modes. MODE A and MODE B are used when the FIR filter output is desired. MODE C should be selected when output from the comb filter is used. Output data is always transmitted as 16-bit, twos complement, MSB first, serial words. In all modes, the FSI pin may be asserted to reset the serial data output and synchronize internal circuits. A $\overline{DOE}$ pin is available to place the DOUT pin in a high impedance state.

Configuring the appropriate timing mode is controlled by the FSEL and SF pins. The truth table is shown in Table IV.

Table IV. Timing Mode Truth Table

FSEL	SF	Output Mode
0	0	A
0	1	B
1	0	C

MODE A

The timing diagrams for MODE A are shown in Figures 14a and 14b. If MODE A is selected, an internal multiplexer routes serial data from the output of the FIR filter to the DOUT pin. The output sample rate is a function of the clock present at the CLKIN pin where:

Output Sample Rate = CLKIN/128

A continuous serial output clock, DOUT CLK, is available with the bit rate determined by:

DOUT CLK = CLKIN/4.

Serial data from the DOUT pin is valid on the falling edges of DOUT CLK. A framing signal, FSO, occurs with a period equal to the output sample rate (Figure 14b). The FSO signal is HIGH during the falling edge of DOUT CLK prior to the beginning of a new output data word.

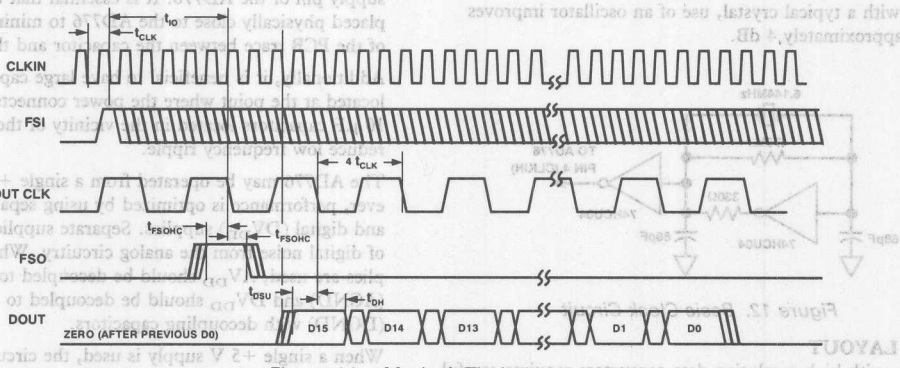


Figure 14a. Mode A Timing

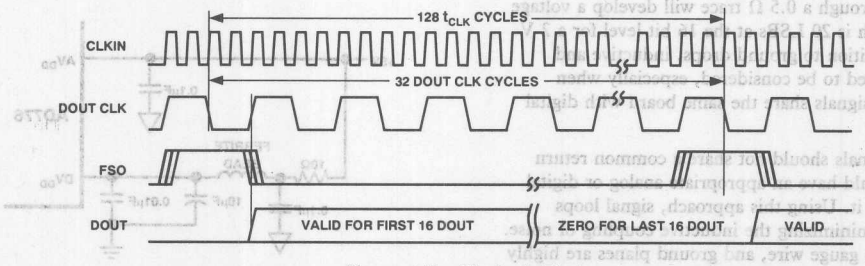


Figure 14b. Mode A Timing

MODE B

The timing diagrams for MODE B are shown in Figures 15a and 15b. If Mode B is selected, the internal multiplexer routes serial data from the output of the FIR filter to the DOUT pin similar to MODE A. The output sample rate is a function of the clock present at the CLKIN pin where:

Output Sample Rate = CLKIN/128.

A continuous serial output clock, DOUT CLK, is available with the bit rate determined by:

DOUT CLK = CLKIN/4.

Note that serial data present at the DOUT pin is valid on the rising edges of DOUT CLK. The framing signal, FSO, occurs with a period equal to the output sample rate. In MODE B, the FSO signal goes LOW at the beginning of the output data word and remains LOW until the entire word is transmitted.

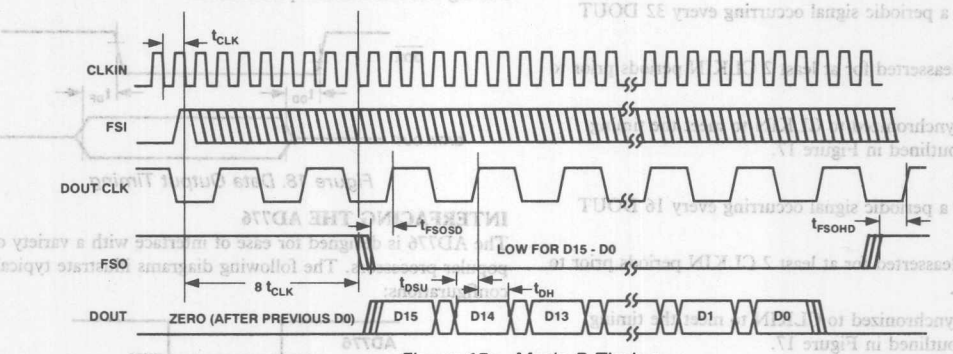


Figure 15a. Mode B Timing

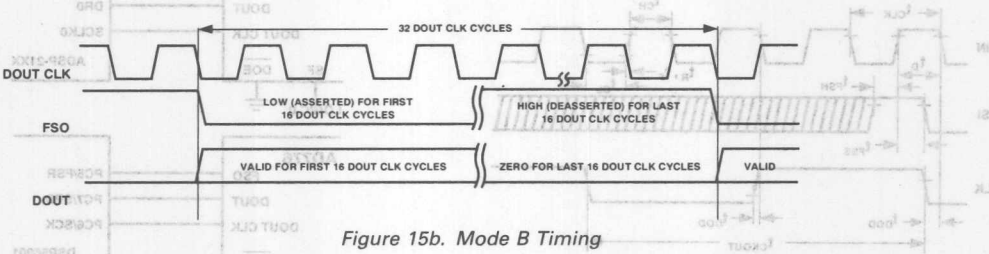


Figure 15b. Mode B Timing

MODE C

The timing diagrams for MODE C are shown in Figure 16. If Mode C is selected, the internal multiplexer routes serial data from the output of the COMB filter to the DOUT pin, bypassing the FIR filter. The output sample rate is a function of the clock present at the CLKIN pin where:

Output Sample Rate = CLKIN/32.

A continuous serial output clock, DOUT CLK, is available with the bit rate determined by:

DOUT CLK = CLKIN/2.

Serial output data is valid on the falling edges of DOUT CLK. The framing signal, FSO, occurs with a period equal to the output sample rate. The FSO signal is HIGH during the falling edge of DOUT CLK prior to transmission of the next output data word. Note that in MODE C, this is also when the LSB, (D0), of the previous data word is valid.

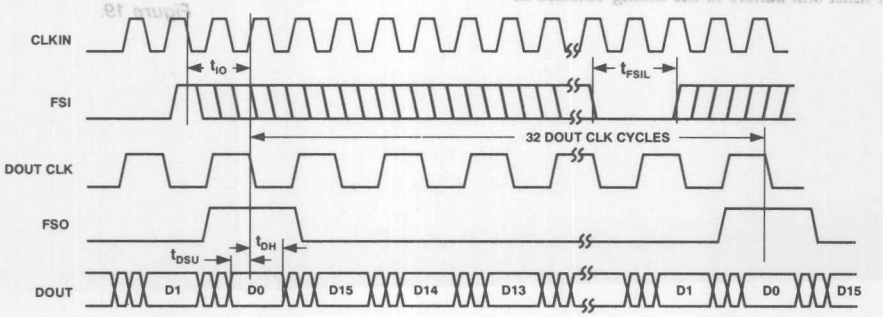


Figure 16. Mode C Timing

FSI Operation

A frame sync input is available to the user on the FSI pin to reset the serial data output and synchronize internal circuits.

Referring to Figure 17, the FSI pin is sampled on the falling edge of CLKIN. The FSI pin must adhere to several conditions depending on which mode is being used as follows:

FSI in MODE A, MODE B

1. FSI should be a periodic signal occurring every 32 DOUT CLK periods.
2. FSI must be deasserted for at least 2 CLKIN periods prior to being asserted.
3. FSI must be synchronized to CLKIN to meet the timing requirements outlined in Figure 17.

FSI in MODE C

1. FSI should be a periodic signal occurring every 16 DOUT CLK periods.
2. FSI must be deasserted for at least 2 CLKIN periods prior to being asserted.
3. FSI must be synchronized to CLKIN to meet the timing requirements outlined in Figure 17.

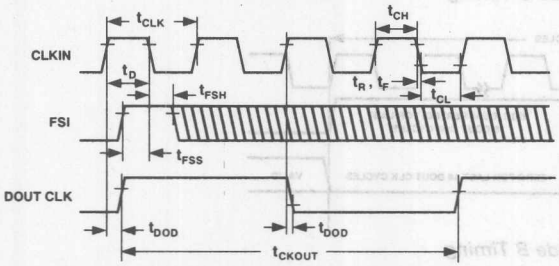


Figure 17. Frame Sync Input (FSI) Timing (FIR Filter Output Mode)

Synchronizing Two Channels

The FSI pin is useful when multiple AD776s are used together and must be synchronized. In such a case, a single pulse may be applied to FSI inputs of the converters. This causes the internal "state-machine" of the AD776 to be reset. Thus, the internal clocking for both the analog and digital circuitry of each individual converter is synchronized and in-phase. In the case of a single FSI pulse, it must still adhere to the timing outlined in Figure 17.

Three-Stating the DOUT Pin ($\overline{DOE}$)

In all modes DOUT may be three-stated using the $\overline{DOE}$ pin. Operation of the $\overline{DOE}$ input is shown in Figure 18. When the $\overline{DOE}$ input is HIGH, serial data will be present and active at the DOUT pin. When $\overline{DOE}$ is brought LOW, the DOUT pin is placed in a high-impedance state. $\overline{DOE}$ is completely asynchronous and independent of input and output clocks. DOUT loading will affect actual performance.

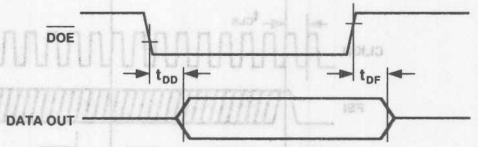


Figure 18. Data Output Timing

INTERFACING THE AD776

The AD776 is designed for ease of interface with a variety of popular processors. The following diagrams illustrate typical configurations:

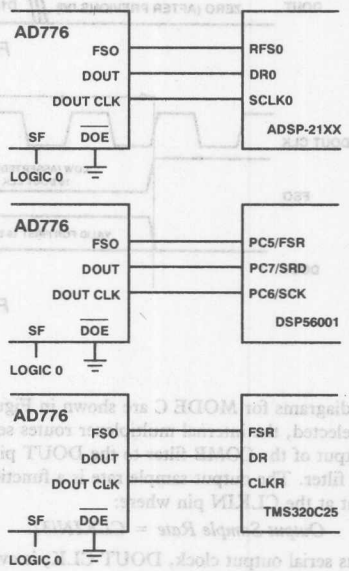


Figure 19.

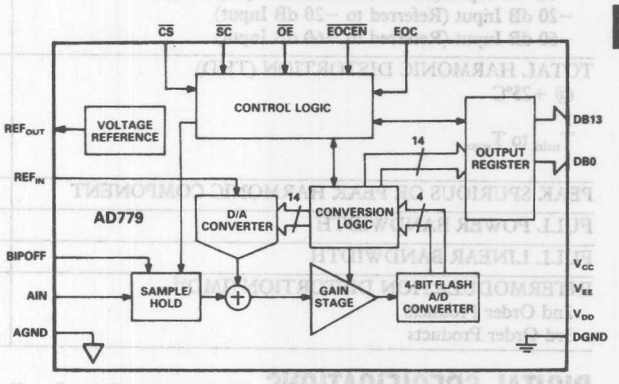
14-Bit 128 kSPS Complete Sampling ADC

AD779*

FEATURES

- AC and DC Characterized and Specified (K, B, T Grades)
- 128k Conversions per Second
- 1 MHz Full Power Bandwidth
- 500 kHz Full Linear Bandwidth
- 80 dB S/N+D (K, B, T Grades)
- Twos Complement Data Format (Bipolar Mode)
- Straight Binary Data Format (Unipolar Mode)
- 10 MΩ Input Impedance
- 16-Bit Bus Interface (See AD679 for 8-Bit Interface)
- On-Board Reference and Clock
- 10 V Unipolar or Bipolar Input Range
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD779 is a complete, multipurpose 14-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The AD779 is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD which are important in signal processing applications. In addition, the AD779K, B and T grades are fully specified for dc parameters which are important in measurement applications.

The 14 data bits are accessed by a 16-bit bus in a single read operation. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD779 operates from +5 V and ±12 V supplies and dissipates 560 mW (typ). Twenty-eight-pin plastic DIP and ceramic DIP packages are available.

***Protected by U.S. Patent Numbers 4,804,960; 4,814,767; 4,833,345; 4,250,445; 4,808,908; RE30,586.**

PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD779 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. SPECIFICATIONS: The AD779K, B and T grades provide fully specified and tested ac and dc parameters. The AD779J, A and S grades are specified and tested for ac parameters; dc accuracy specifications are shown as typicals. DC specifications (such as INL, gain and offset) are important in control and measurement applications. AC specifications (such as S/N+D ratio, THD and IMD) are of value in signal processing applications.
3. EASE OF USE: The pinout is designed for easy board layout, and the single cycle read output provides compatibility with 16-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
4. RELIABILITY: The AD779 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.
5. The AD779 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD779/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD779—SPECIFICATIONS

AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%, f_{SAMPLE} = 128 kSPS, f_{IN} = 10.009 kHz unless otherwise noted)[1]

Parameter	AD779J/A/S Min	AD779J/A/S Typ	AD779J/A/S Max	AD779K/B/T Min	AD779K/B/T Typ	AD779K/B/T Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO							
−0.5 dB Input (Referred to −0 dB Input)	78	79		80	81		dB
−20 dB Input (Referred to −20 dB Input)	58	59		60	61		dB
−60 dB Input (Referred to −60 dB Input)	18	19		20	21		dB
TOTAL HARMONIC DISTORTION (THD)							
@ +25°C		−90	−84		−90	−84	dB
		0.003	0.006		0.003	0.006	%
T_{min} to T_{max}		−88	−82		−88	−82	dB
		0.004	0.008		0.004	0.008	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−90	−84		−90	−84	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[2]							
2nd Order Products		−90	−84		−90	−84	dB
3rd Order Products		−90	−84		−90	−84	dB

DIGITAL SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		2.0	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{DD}	−10	+10	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V	−10	+10	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		0.4	V
I_{OZ}	High Z Leakage Current	V_{IN} = V_{DD}	−10	+10	μA
C_{OZ}	High Z Output Capacitance			10	pF

NOTES

[1] f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a −0 dB (9.997 V p-p) input signal unless otherwise noted.

[2] f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 128 kSPS.

Specifications subject to change without notice.

DC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10% unless otherwise indicated)

Parameter	AD779J/A/S Min	AD779J/A/S Typ	AD779J/A/S Max	AD779K/B/T Min	AD779K/B/T Typ	AD779K/B/T Max	Units
TEMPERATURE RANGE							
J, K Grades	0		+70	0		+70	°C
A, B Grades	−40		+85	−40		+85	°C
S, T Grades	−55		+125	−55		+125	°C
ACCURACY							
Resolution	14			14			Bits
Integral Nonlinearity (INL)		±2			±1	±2	LSB
Differential Nonlinearity (DNL)	14			14			Bits
Unipolar Zero Error[1] (@ +25°C)		0.08			0.05	0.07	% FSR*
Bipolar Zero Error[1] (@ +25°C)		0.08			0.05	0.07	% FSR
Gain Error[1, 2] (@ +25°C)		0.12			0.09	0.11	% FSR
Temperature Drift							
Unipolar Zero[3]							
J, K Grades		0.04			0.04	0.05	% FSR
A, B Grades		0.05			0.05	0.07	% FSR
S, T Grades		0.09			0.09	0.10	% FSR
Bipolar Zero[3]							
J, K Grades		0.02			0.02	0.04	% FSR
A, B Grades		0.04			0.04	0.06	% FSR
S, T Grades		0.08			0.08	0.09	% FSR
Gain[3]							
J, K Grades		0.09			0.09	0.11	% FSR
A, B Grades		0.10			0.10	0.16	% FSR
S, T Grades		0.20			0.20	0.25	% FSR
Gain[4]							
J, K Grades		0.04			0.04	0.05	% FSR
A, B Grades		0.05			0.05	0.07	% FSR
S, T Grades		0.09			0.09	0.10	% FSR
ANALOG INPUT							
Input Ranges							
Unipolar Mode	0		+10	0		+10	V
Bipolar Mode	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1.5			1.5	µs
Aperture Delay		10			10		ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	4.98		5.02	4.98		5.02	V
External Load							
Unipolar Mode			+1.5			+1.5	mA
Bipolar Mode			+0.5			+0.5	mA
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = +12 V ± 5%		±6				±6	LSB
V_{EE} = −12 V ± 5%		±6				±6	LSB
V_{DD} = +5 V ± 10%		±6				±6	LSB
Operating Current							
I_{CC}		18	20		18	20	mA
I_{EE}		25	34		25	34	mA
I_{DD}		8	12		8	12	mA
Power Consumption		560	745		560	745	mW

NOTES
[1]Adjustable to zero.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.
*% FSR = percent of full-scale range.

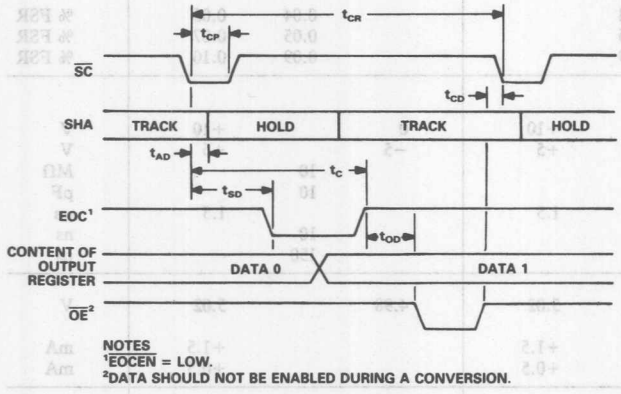
Specifications subject to change without notice.

TIMING SPECIFICATIONS

(All device types T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter	Symbol	Min	Max	Units
Conversion Rate[1]	t_{CR}		7.8	µs
Convert Pulse Width	t_{CP}	0.097	3.0	µs
Aperture Delay	t_{AD}	5	20	ns
Conversion Time	t_C		6.3	µs
Status Delay	t_{SD}	0	400	ns
Access Time[2, 3]	t_{BA}	10	100	ns
		10	57[4]	ns
Float Delay[5]	t_{FD}	10	80	ns
Output Delay	t_{OD}		0	ns
$\overline{OE}$ Delay	t_{OE}	20		ns
Read Pulse Width	t_{RP}	100		ns
Conversion Delay	t_{CD}	400		ns

NOTES
[1]Includes Acquisition Time.
[2]Measured from the falling edge of $\overline{OE}/\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 4.
[3]C_{OUT} = 100 pF.
[4]C_{OUT} = 50 pF.
[5]Measured from the rising edge of $\overline{OE}/\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 4; C_{OUT} = 10 pF.
Specifications subject to change without notice.



NOTES
[1]$\overline{EOCEN}$ = LOW.
[2]DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing

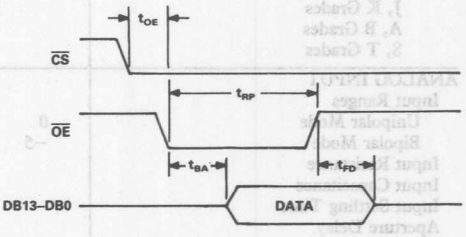


Figure 3. EOC Timing

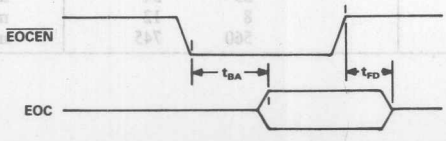


Figure 2. Output Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	0 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	5 V	10 pF

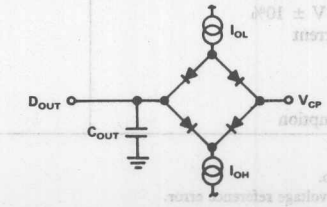


Figure 4. Load Circuit for Bus Timing Specifications

ABSOLUTE MAXIMUM RATINGS[1]

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC} (Note 2)	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	V_{EE}	V_{CC}	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C
Operating Temperature				
J and K Grades		0	+70	°C
A and B Grades		−40	+85	°C
S and T Grades		−55	+125	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]The AD779 is not designed to operate from ±15 V supplies.

ESD SENSITIVITY

The AD779 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD779 has been classified as a Category 1 device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

ORDERING GUIDE[1]

Model[2]	Package	Temperature Range	Tested and Specified	Package Option[3]
AD779JN	28-Pin Plastic DIP	0 to +70°C	AC	N-28
AD779KN	28-Pin Plastic DIP	0 to +70°C	AC + DC	N-28
AD779JD	28-Pin Ceramic DIP	0 to +70°C	AC	D-28
AD779KD	28-Pin Ceramic DIP	0 to +70°C	AC + DC	D-28
AD779AD	28-Pin Ceramic DIP	−40°C to +85°C	AC	D-28
AD779BD	28-Pin Ceramic DIP	−40°C to +85°C	AC + DC	D-28
AD779SD	28-Pin Ceramic DIP	−55°C to +125°C	AC	D-28
AD779TD	28-Pin Ceramic DIP	−55°C to +125°C	AC + DC	D-28

NOTES

[1]For two cycle read (8+16 bits) interface to 8-bit buses, see AD679.

[2]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD779/883B data sheet.

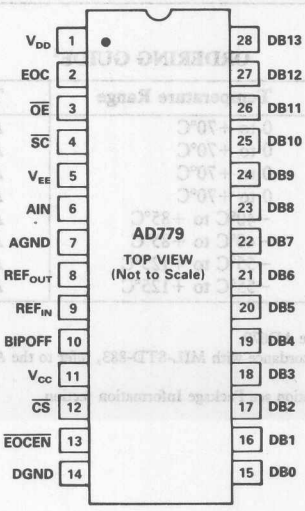
[3]D = Ceramic DIP; N = Plastic DIP. For outline information see Package Information section.

Symbol	28-Pin DIP Pin No.	44-Lead JLCC Pin No.	Type	Name and Function
AGND	7	11	P	Analog Ground. This is the ground return for AIN only.
AIN	6	10	AI	Analog Signal Input.
BIPOFF	10	15	AI	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} for ±5 V input bipolar mode and twos-complement binary output coding.
$\overline{CS}$	12	19	DI	Chip Select. Active LOW.
DGND	14	23	P	Digital Ground
DB13–DB0	28–15	43, 42, 40, 39, 37, 36, 35, 34, 33, 31, 30, 27, 26, 25	DO	Data Bits. These pins provide all 14 bits in one 14 bit parallel output. Active HIGH
EOC	2	3	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. EOC is a three-state output. See $\overline{EOCEN}$ pin for information on EOC gating.
$\overline{EOCEN}$	13	21	DI	End-of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{OE}$	3	5	DI	Output Enable. A down-going transition on $\overline{OE}$ enables data bits. Active LOW.
REF_{IN}	9	14	AI	Reference Input. +5 V input gives 10 V full scale range.
REF_{OUT}	8	12	AO	+5 V Reference Output. Tied to REF_{IN} for normal operation.
$\overline{SC}$	4	6	DI	Start Convert. Active LOW.
V_{CC}	11	17	P	+12 V Analog Power.
V_{EE}	5	8	P	−12 V Analog Power.
V_{DD}	1	1	P	+5 V Digital Power.

Type: AI = Analog Input.
AO = Analog Output.
DI = Digital Input.
DO = Digital Output. All DO pins are three-state drivers.
P = Power.

PIN CONFIGURATION

DIP Package



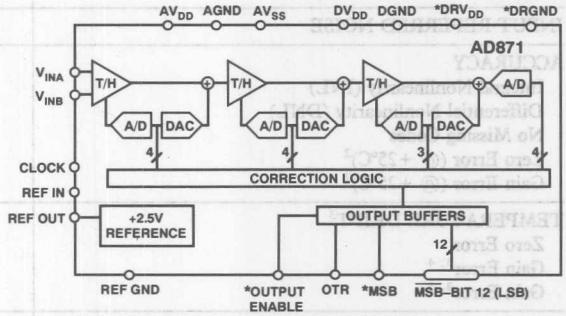
Complete 12-Bit 5 MSPS Monolithic A/D Converter

AD871

FEATURES

- Monolithic 12-Bit 5 MSPS A/D Converter
- Low Noise: 0.17 LSB RMS Referred to Input
- No Missing Codes Guaranteed
- Differential Nonlinearity Error: 0.5 LSB
- Signal-to-Noise and Distortion Ratio: 68 dB
- Spurious-Free Dynamic Range: 73 dB
- Power Dissipation: 1.03 W
- Complete: On-Chip Track-and-Hold Amplifier and Voltage Reference
- Pin Compatible with the AD872
- Twos Complement Binary Output Data
- Out of Range Indicator
- 28-Pin Ceramic DIP or 44-Pin Surface Mount Package

FUNCTIONAL BLOCK DIAGRAM



*ONLY AVAILABLE ON 44-PIN SURFACE MOUNT PACKAGE.

PRODUCT DESCRIPTION

The AD871 is a monolithic 12-bit, 5 Msps analog to digital converter with an on-chip, high performance track-and-hold amplifier and voltage reference. The AD871 uses a multistage differential pipelined architecture with error correction logic to provide 12-bit accuracy at 5 Msps data rates and guarantees no missing codes over the full operating temperature range. The AD871 is a redesigned variation of the AD872 12-bit, 10 Msps ADC, optimized for lower noise in applications requiring sampling rates of 5 Msps or less. The AD871 is pin compatible with the AD872, allowing the parts to be used interchangeably as system requirements change.

The low-noise input track-and-hold (T/H) of the AD871 is ideally suited for high-end imaging applications. In addition, the T/H's high input impedance and fast settling characteristics allow the AD871 to easily interface with multiplexed systems that switch multiple signals through a single A/D converter. The dynamic performance of the input T/H also renders the AD871 suitable for sampling single channel inputs at frequencies up to and beyond the Nyquist rate. The AD871 provides both reference output and reference input pins, allowing the on-board reference to serve as a system reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. A single clock input is used to control all internal conversion cycles. The digital output data is presented in twos complement binary output format. An out-of-range signal indicates an overflow condition, and can be used with the most significant bit to determine low or high overflow.

The AD871 is fabricated on Analog Devices ABCMOS-1 process which utilizes high speed bipolar and CMOS transistors on a single chip. High speed, precision analog circuits are now combined with high density logic circuits.

The AD871 is packaged in a 28-pin ceramic DIP and a 44-pin leadless ceramic surface mount package and is specified for operation from 0°C to +70°C and −55°C to +125°C.

PRODUCT HIGHLIGHTS

The AD871 offers a complete single-chip sampling 12-bit, 5 Msps analog-to-digital conversion function in a 28-pin DIP or 44-pin leadless ceramic surface mount package (LCC).

Low Noise—The AD871 features 0.17 LSB referred-to-input noise, producing essentially a "1 code wide" histogram for a code-centered dc input.

Low Power—The AD871 at 1.03 W consumes a fraction of the power of presently available hybrids.

On-Chip Track-and-Hold (T/H)—The low noise, high impedance T/H input eliminates the need for external buffers and can be configured for single ended or differential inputs.

Ease of Use—The AD871 is complete with T/H and voltage reference and is pin-compatible with the AD872 (12-bit, 10 Msps monolithic ADC).

Out of Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD871's input range.

AD871—SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, AV_{SS} = −5 V, f_{SAMPLE} = 5 MHz unless otherwise indicated)

Parameter	J Grade[1]	S Grade[1]	Units
RESOLUTION	12	12	Bits min
MAX CONVERSION RATE	5	5	MHz min
INPUT REFERRED NOISE	0.17	0.17	LSB rms typ
ACCURACY			
Integral Nonlinearity (INL)	±1.5	±1.5	LSB typ
Differential Nonlinearity (DNL)	±0.5	±0.5	LSB typ
No Missing Codes	12	12	Bits Guaranteed
Zero Error (@ +25°C)[2]	±0.75	±0.75	% FSR max
Gain Error (@ +25°C)[2]	±1.25	±1.25	% FSR max
TEMPERATURE DRIFT[3]			
Zero Error	±0.15	±0.3	% FSR max
Gain Error[3, 4]	±0.80	±1.75	% FSR max
Gain Error[3, 5]	±0.25	±0.50	% FSR max
POWER SUPPLY REJECTION[6]			
AV_{DD}, DV_{DD} (+5 V ± 0.25 V)	±0.125	±0.125	% FSR max
AV_{SS} (−5 V ± 0.25 V)	±0.125	±0.125	% FSR max
ANALOG INPUT			
Input Range	±1	±1	Volts max
Input Resistance	50	50	kΩ typ
Input Capacitance	10	10	pF typ
INTERNAL VOLTAGE REFERENCE			
Output Voltage	2.5	2.5	Volts typ
Output Voltage Tolerance	±20	±40	mV max
Output Current (Available for External Loads) (External load should not change during conversion.)	2.0	2.0	mA typ
REFERENCE INPUT RESISTANCE	5	5	kΩ typ
POWER SUPPLIES			
Supply Voltages			
AV_{DD}	+5	+5	V (±5% AV_{DD} Operating)
AV_{SS}	−5	−5	V (±5% AV_{SS} Operating)
DV_{DD}	+5	+5	V (±5% DV_{DD} Operating)
DRV_{DD}[7]	+5	+5	V (±5% DRV_{DD} Operating)
Supply Current			
IAV_{DD}	87	88	mA max (82 mA typ)
IAV_{SS}	147	150	mA max (115 mA typ)
IDV_{DD}	20	21	mA max (7 mA typ)
$IDRV_{DD}$[7]	2	2	mA max
POWER CONSUMPTION	1.03	1.03	W typ
	1.25	1.3	W max

NOTES
[1]Temperature ranges are as follows: J Grade: 0°C to +70°C, S Grade: −55°C to +125°C.
[2]Adjustable to zero with external potentiometers (see Zero and Gain Error Calibration section).
[3]+25°C to T_{MIN} and +25°C to T_{MAX}.
[4]Includes internal voltage reference error.
[5]Excludes internal reference drift.
[6]Change in Gain Error as a function of the dc supply voltage (V nominal to V min, V nominal to V max).
[7]LCC package only.
Specifications subject to change without notice.

AC SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, AV_{SS} = −5 V, f_{SAMPLE} = 5 Msps, unless otherwise noted)[1]

	J Grade	S Grade	Units
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)			
f_{INPUT} = 750 kHz	68	68	dB typ
f_{INPUT} = 1 MHz	66	66	dB typ
	63	62	dB min
f_{INPUT} = 2.49 MHz	60	60	dB typ
TOTAL HARMONIC DISTORTION (THD)			
f_{INPUT} = 750 kHz	−72	−72	dB typ
f_{INPUT} = 1 MHz	−69	−69	dB typ
	−64	−63	dB max
f_{INPUT} = 2.49 MHz	−62	−62	dB typ
SPURIOUS FREE DYNAMIC RANGE (SFDR)			
f_{INPUT} = 750 kHz	73	73	dB typ
f_{INPUT} = 1 MHz	70	70	dB typ
f_{INPUT} = 2.49 MHz	62	62	dB typ
INTERMODULATION DISTORTION (IMD)[2]			
Second Order Products	−80	−80	dB typ
Third Order Products	−73	−73	dB typ
FULL POWER BANDWIDTH	15	15	MHz typ
SMALL SIGNAL BANDWIDTH	15	15	MHz typ
APERTURE DELAY	6	6	ns typ
APERTURE JITTER	16	16	ps rms typ
ACQUISITION TO FULL-SCALE STEP	80	80	ns typ
OVERVOLTAGE RECOVERY TIME	80	80	ns typ

NOTES
[1]f_{IN} amplitude = −0.5 dB full scale unless otherwise indicated. All measurements referred to a 0 dB (1 V pk) input signal unless otherwise indicated.
[2]fa = 1.0 MHz, fb = 0.95 MHz with f_{SAMPLE} = 5 MHz.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, AV_{SS} = −5 V unless otherwise noted)

Parameter	Symbol	J, S Grades	Units
LOGIC INPUTS			
High Level Input Voltage	V_{IH}	+2.0	V min
Low Level Input Voltage	V_{IL}	+0.8	V max
High Level Input Current (V_{IN} = DV_{DD})	I_{IH}	±10	μA max
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	±10	μA max
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUTS			
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	+2.4	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	+0.4	V max
Output Capacitance	C_{OUT}	5	pF typ
Leakage (Three-State, LCC Only)	IZ	±10	μA max

Specifications subject to change without notice.

Parameter	Symbol	J, S Grades	Units
Clock Period[1]	t_C	200	ns min
CLOCK Pulse Width High	t_{CH}	95	ns min
CLOCK Pulse Width Low	t_{CL}	95	ns min
Clock Duty Cycle[2]		40	% min (50% typ)
		60	% max
Output Delay	t_{OD}	10	ns min (20 ns typ)
Pipeline Delay (Latency)		3	Clock Cycles
Data Access Time (LCC Package Only)[3]	t_{DD}	50	ns typ (100 pF Load)
Output Float Delay (LCC Package Only)[3]	t_{HL}	50	ns typ (10 pF Load)

NOTES
[1]Conversion rate is operational down to 10 kHz without degradation in specified performance.
[2]For clock periods of 200 ns or greater, see Clock Input Section.
[3]See Section on Three-State Outputs for timing diagrams and application information.
Specifications subject to change without notice.

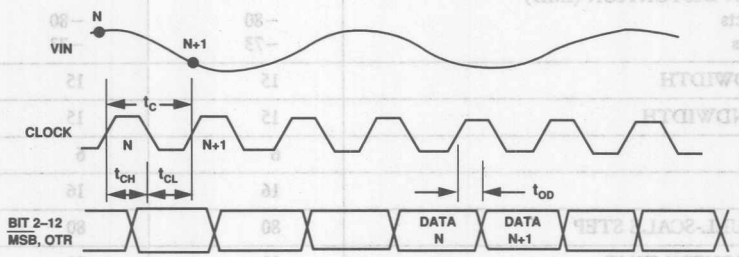


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	With Respect to	Min	Max	Units
AV_{DD}	AGND	−0.5	+6.5	Volts
AV_{SS}	AGND	−6.5	+0.5	Volts
DV_{DD}, DRV_{DD}	DGND, DRGND	−0.5	+6.5	Volts
DRV_{DD}[2]	DV_{DD}	−6.5	+6.5	Volts
DRGND[2]	DGND	−0.3	+0.3	Volts
AGND	DGND	−1.0	+1.0	Volts
AV_{DD}	DV_{DD}	−6.5	+6.5	Volts
Clock Input, OEN	DGND	−0.5	DV_{DD} + 0.5	Volts
Digital Outputs	DGND	−0.5	DV_{DD} + 0.3	Volts
V_{INA}, V_{INB} REF IN	AGND	−6.5	+6.5	Volts
REF IN	AGND	AV_{SS}	AV_{DD}	Volts
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
[2]LCC Package Only.

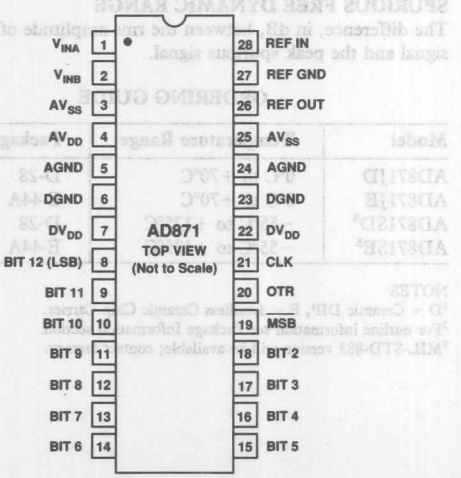
PIN DESCRIPTION

Symbol	DIP Pin No.	LCC Pin No.	Type	Name and Function
AGND	5, 24	9, 36	P	Analog Ground.
AV_{DD}	4	6, 38	P	+5 V Analog Supply.
AV_{SS}	3, 25	5, 40	P	−5 V Analog Supply.
$\overline{MSB}$	19	29	DO	Inverted Most Significant Bit. Provides twos complement output data format.
MSB	N/A	27	DO	Most Significant Bit.
BIT 2–BIT 11	18–9	26–17	DO	Data Bits 2 through 11.
BIT 12 (LSB)	8	16	DO	Least Significant Bit.
CLK	21	31	DI	Clock Input. The AD871 will initiate a conversion on the rising edge of the clock input. See the Timing Diagram for details.
DV_{DD}	7, 22	33	P	+5 V Digital Supply.
DGND	6, 23	10	P	Digital Ground.
DRV_{DD}	N/A	12, 32	P	+5 V Digital Supply for the output drivers.
DRGND	N/A	11, 34	P	Digital Ground for the output drivers. (See section on Power Supply Decoupling for details on DRV_{DD} and DRGND.)
OTR	20	30	DO	Out of Range is Active HIGH on the leading edge of code 0 or the trailing edge of code 4096. See Output Data Format Table III.
OEN	N/A	13	DI	Output Enable. See the Three State Output Timing Diagram for details.
REF GND	27	42	AI	Reference Ground.
REF IN	28	43	AI	Reference Input. +2.5 V input gives ±1 V full-scale range.
REF OUT	26	41	AO	+2.5 V Reference Output. Tie to REF IN for normal operation.
V_{INA}	1	1	AI	(+) Analog Input Signal on the differential input amplifier.
V_{INB}	2	2	AI	(−) Analog Input Signal on the differential input amplifier.
NC	N/A	3, 4, 7, 8, 14, 15, 28, 35, 37, 39, 44		No Connect.

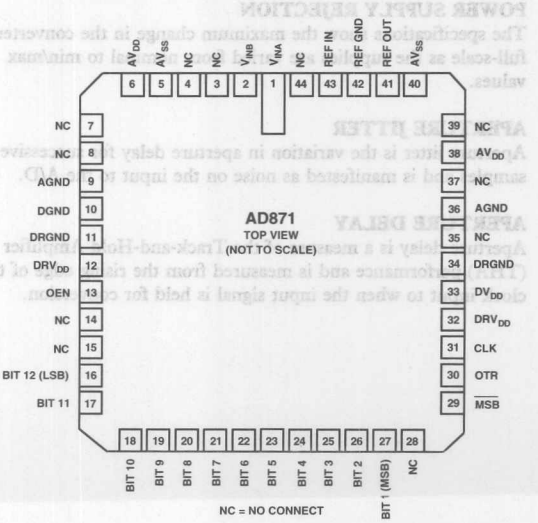
TYPE: AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; P = Power; N/A = Not Available on 28-pin DIP. Only available on 44-pin surface mount package.

PIN CONFIGURATIONS

28-Pin Ceramic DIP



44-Pin LCC



DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL LINEARITY ERROR (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes must be present over all operating ranges.

ZERO ERROR

The major carry transition should occur for an analog value 1/2 LSB below analog common. Zero error is defined as the deviation of the actual transition from that point. The zero error and temperature drift specify the initial deviation and maximum change in the zero error over temperature.

GAIN ERROR

The first code transition should occur for an analog value 1/2 LSB above nominal negative full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

TEMPERATURE DRIFT

The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The specifications show the maximum change in the converter's full-scale as the supplies are varied from nominal to min/max values.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

APERTURE DELAY

Aperture delay is a measure of the Track-and-Hold Amplifier (THA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

OVERVOLTAGE RECOVERY TIME

Overvoltage recovery time is defined as that amount of time required for the ADC to achieve a specified accuracy after an overvoltage (50% greater than full-scale range), measured from the time the overvoltage signal reenters the converter's range.

DYNAMIC SPECIFICATIONS

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

INTERMODULATION DISTORTION (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb), and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (2 fb − fa). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sums is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

FULL-POWER BANDWIDTH

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

SPURIOUS FREE DYNAMIC RANGE

The difference, in dB, between the rms amplitude of the input signal and the peak spurious signal.

ORDERING GUIDE

Model	Temperature Range	Package Option[1, 2]
AD871JD	0°C to +70°C	D-28
AD871JE	0°C to +70°C	E-44A
AD871SD[3]	−55°C to +125°C	D-28
AD871SE[3]	−55°C to +125°C	E-44A

NOTES
[1]D = Ceramic DIP, E = Leadless Ceramic Chip Carrier.
[2]For outline information see Package Information section.
[3]MIL-STD-883 version will be available; contact factory.

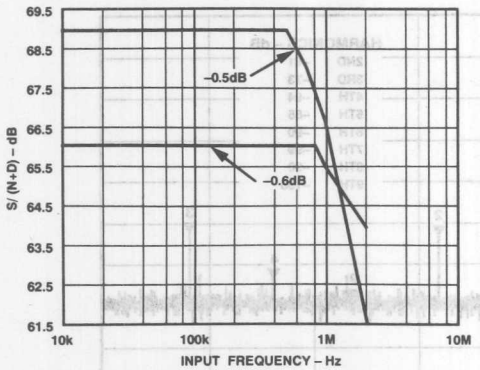


Figure 2. AD871 S/(N+D) vs. Input Frequency

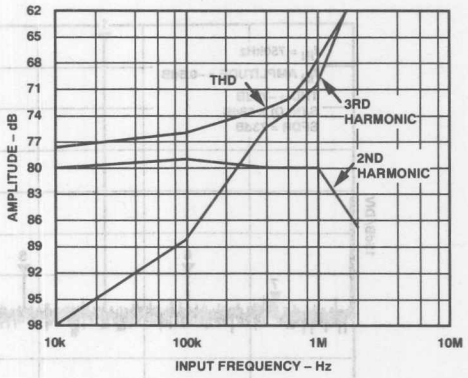


Figure 3. AD871 Distortion vs. Input Frequency, Full-Scale Input

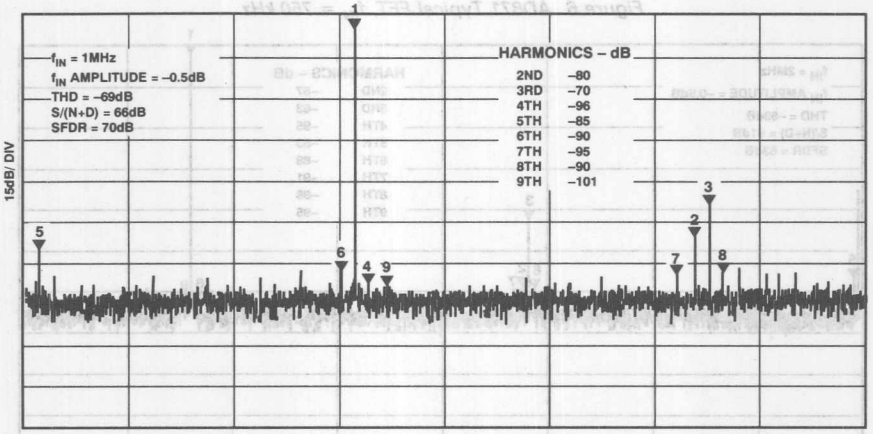


Figure 4. AD871 Typical FFT, f_{IN} = 1 MHz, f_{IN} Amplitude = −0.5 dB

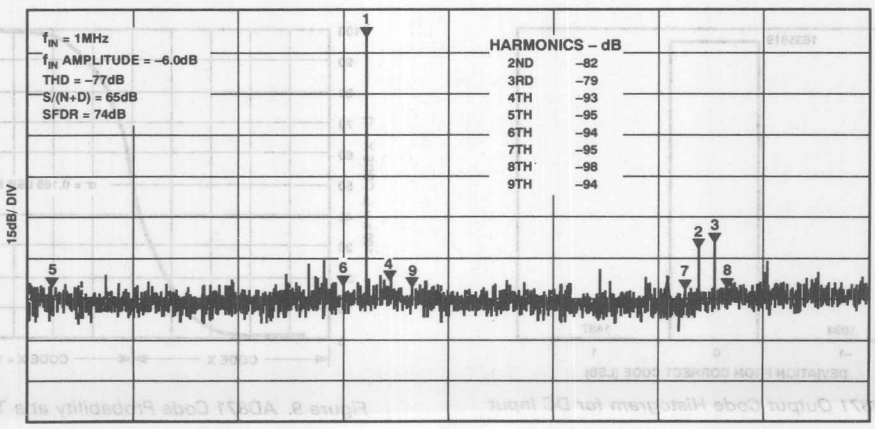


Figure 5. AD871 Typical FFT, f_{IN} = 1 MHz, f_{IN} Amplitude = −6 dB

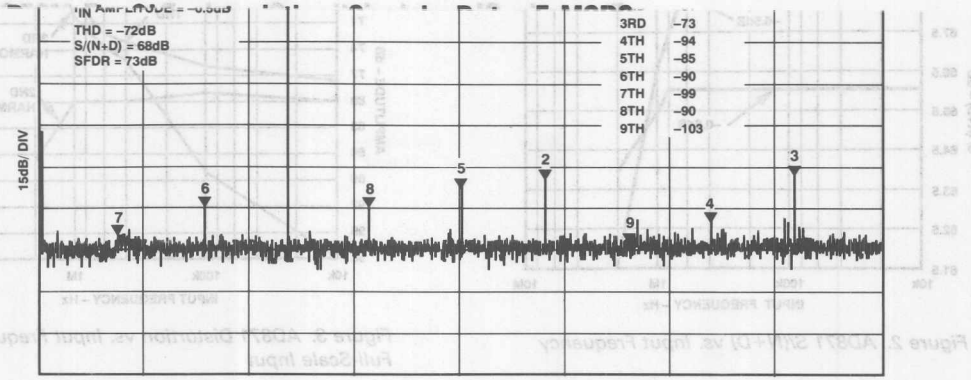


Figure 6. AD871 Typical FFT, f_{IN} = 750 kHz

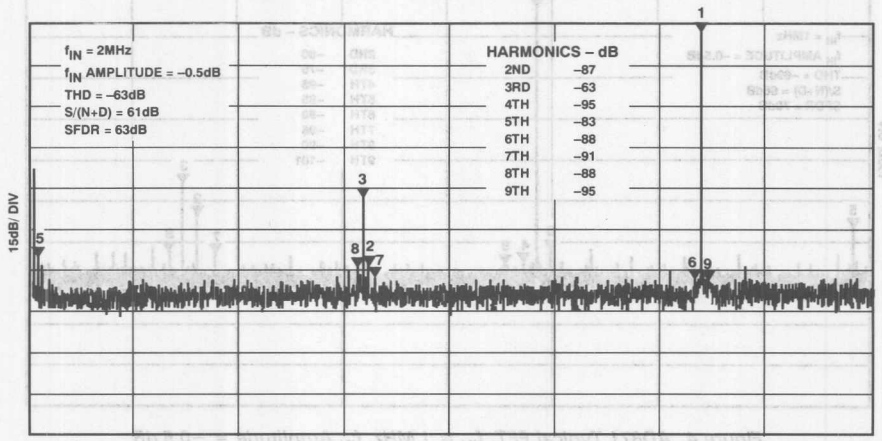


Figure 7. AD871 Typical FFT, f_{IN} = 2 MHz

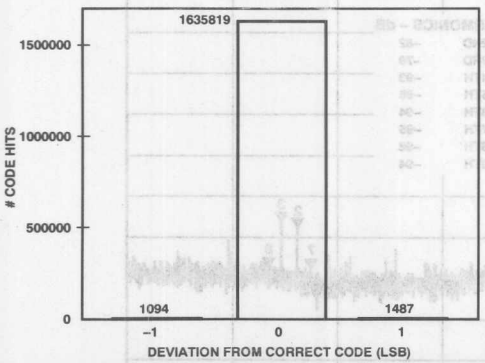


Figure 8. AD871 Output Code Histogram for DC Input

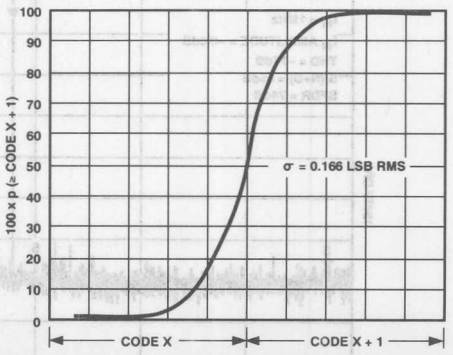


Figure 9. AD871 Code Probability at a Transition

THEORY OF OPERATION

The AD871 is implemented using a 4-stage pipelined multiple flash architecture. A differential input track-and-hold amplifier (THA) acquires the input and converts the input voltage into a differential current. A 4-bit approximation of the input is made by the first flash converter, and an accurate analog representation of this 4-bit guess is generated by a digital-to-analog converter. This approximation is subtracted from the THA output to produce a remainder, or residue. This residue is then sampled and held by the second THA, and a 4-bit approximation is generated and subtracted by the second stage. Once the second THA goes into hold, the first stage goes back into track to acquire a new input signal. The third stage provides a 3-bit approximation/subtraction operation, and produces the final residue, which is passed to a final 4-bit flash converter. The 15 output bits from the 4 flash converters are accumulated in the correction logic block, which adds the bits together using the appropriate correction algorithm, to produce the 12-bit output word. The digital output, together with overrange indicator, is latched into an output buffer to drive the output pins.

The additional THA inserted in each stage of the AD871 architecture allows pipelining of the conversion. In essence, the converter is converting multiple inputs simultaneously, processing them through the converter chain serially. This means that while the converter is capable of capturing a new input sample every clock cycle, it actually takes three clock cycles for the conversion to be fully processed and appear at the output. This "pipeline delay" is often referred to as latency, and is not a concern in most applications, however there are some cases where it may be a consideration. For example, some applications call for the A/D converter to be placed in a high speed feedback loop, where its input is servoed to provide a desired result at the digital output (e.g., offset calibration or zero restoration in video applications). In these cases the 3 clock cycle delay through the pipeline must be accounted for in the loop stability calculations. Also, because the converter is working on three conversions simultaneously, major disruptions to the part (such as a large glitch on the supplies or reference) may corrupt three data samples. Finally, there will be a minimum clock rate below which the THA droop corrupts the signal in the pipeline. In the case of the AD871, this minimum clock rate is 10 kHz.

The high impedance differential inputs of the AD871 allow a variety of input configurations (see APPLYING THE AD871). The AD871 converts the voltage difference between the V_{INA} and V_{INB} pins. For single-ended applications, one input pin (V_{INA} or V_{INB}) may be grounded, but even in this case the differential input can provide a performance boost: for example, for an input coming from a coaxial cable, V_{INB} can be tied to the shield ground, allowing the AD871 to reject shield noise as common mode. The high input impedance of the device minimizes external driving requirements and allows the user to externally select the appropriate termination impedance for the application.

The AD871 clock circuitry uses both edges of the clock in its internal timing circuitry (see spec page for exact timing requirements.) The AD871 samples the analog input on the rising edge of the clock input. During the clock low time (between the falling edge and rising edge of the clock) the input THA is in track mode; during the clock high time it is in hold. System disturbances just prior to the rising edge of the clock may cause the part to acquire the wrong value, and should be minimized.

While the part uses both clock edges for its timing, jitter is only a significant issue for the rising edge of the clock (see CLOCK INPUT section).

APPLYING THE AD871

ANALOG INPUTS

The AD871 features a high impedance differential input that can readily operate on either single-ended or differential input signals. Table I summarizes the nominal input voltage span for both single-ended and differential modes, assuming a 2.5 V reference input.

Table I. Input Voltage Span

	V_{INA}	V_{INB}	$V_{INA}-V_{INB}$
Single-Ended	+1 V	GND	+1 V (Positive Full Scale)
	−1 V	GND	−1 V (Negative Full Scale)
Differential	+0.5 V	−0.5 V	+1 V (Positive Full Scale)
	−0.5 V	+0.5 V	−1 V (Negative Full Scale)

Figure 10 shows an approximate model for the analog input circuit. As this model indicates, when the input exceeds 1.6 V (with respect to AGND), the input device may saturate, causing the input impedance to drop substantially and significantly reducing the performance of the part. Input compliance in the negative direction is somewhat larger, showing virtually no degradation in performance for inputs as low as −1.9 V.

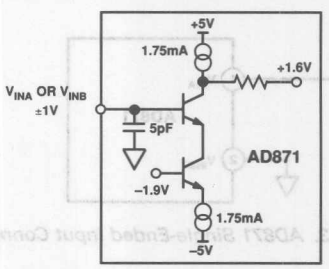


Figure 10. AD871 Equivalent Analog Input Circuit

Figure 11 illustrates the effect of varying the common-mode voltage of a −0.5 dB input signal on total harmonic distortion.

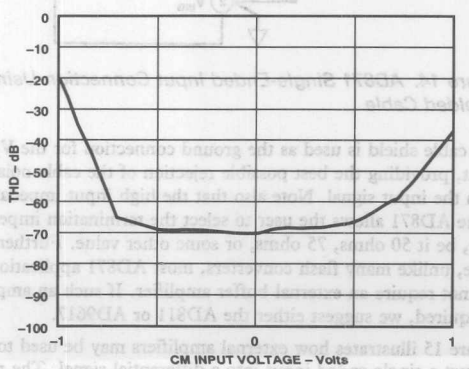


Figure 11. AD871 Total Harmonic Distortion vs. CM Input Voltage, f_{IN} = 1 MHz, FS = 5 MSPS

Figure 12 shows the common-mode rejection performance vs. frequency for a 1 V p-p common mode input. This excellent common-mode rejection over a wide bandwidth affords the user the opportunity to eliminate many potential sources of input noise as common mode by using the differential input structure of the AD871.

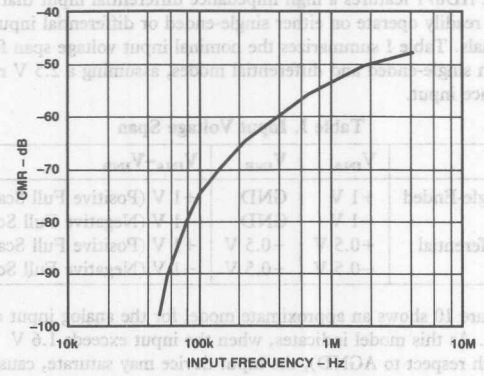


Figure 12. Common-Mode Rejection vs. Input Frequency, 1 V p-p Input

Figures 13 and 14 illustrate typical input connections for single-ended inputs.

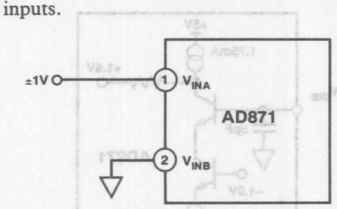


Figure 13. AD871 Single-Ended Input Connection

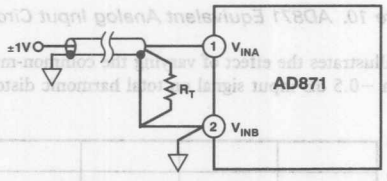


Figure 14. AD871 Single-Ended Input Connection Using a Shielded Cable

The cable shield is used as the ground connection for the V_{INB} input, providing the best possible rejection of the cable noise from the input signal. Note also that the high input impedance of the AD871 allows the user to select the termination impedance, be it 50 ohms, 75 ohms, or some other value. Furthermore, unlike many flash converters, most AD871 applications will not require an external buffer amplifier. If such an amplifier is required, we suggest either the AD811 or AD9617.

Figure 15 illustrates how external amplifiers may be used to convert a single-ended input into a differential signal. The resistor values of 536 Ω and 562 Ω were selected to provide optimum phase matching between U1 and U2.

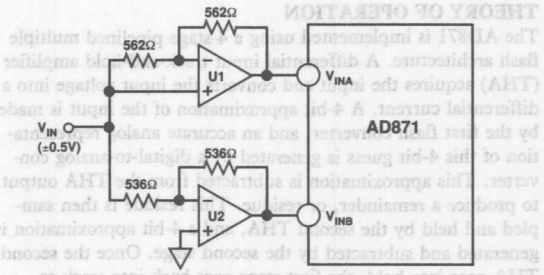


Figure 15. Single-Ended to Differential Connections; U1, U2 = AD811 or AD9617

The use of the differential input signal can help to minimize even-order distortion from the input THA where performance beyond −70 dB is desired.

Figure 16 shows the AD871 large signal (−0.5 dB) and small signal (−20 dB) frequency response.

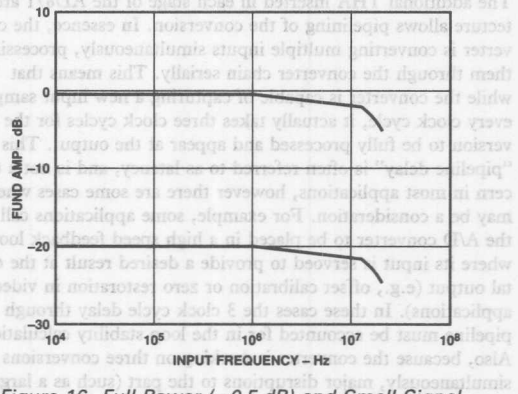


Figure 16. Full Power (−0.5 dB) and Small Signal Response (−20 dB) vs. Input Frequency

The AD871's wide input bandwidth facilitates rapid acquisition of transient input signals: the input THA can typically settle to 12-bit accuracy from a full-scale input step in less than 80 ns. Figure 17 illustrates the typical acquisition of a full-scale input step.

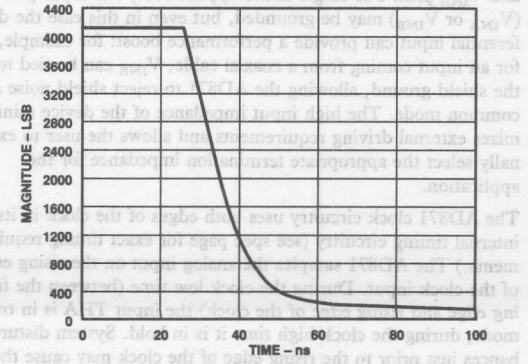


Figure 17. Typical AD871 Settling Time

The wide input bandwidth and superior dynamic performance of the input THA make the AD871 suitable for sampling inputs at frequencies up to the Nyquist Rate. The input THA is designed to recover rapidly from input overdrive conditions, returning from a 50% overdrive in less than 100 ns.

Because of the THA's exceptionally wide input bandwidth, some users may find the AD871 is sensitive to noise at frequencies from 10 MHz to 50 MHz that other converters are incapable of responding to. This sensitivity can be mitigated by careful use of the differential inputs (see previous paragraphs). Additionally, Figure 18 shows how a small capacitor (10 pF–20 pF for 50 Ω terminated inputs) may be placed between V_{INA} and V_{INB} to help reduce high frequency noise in applications where limiting the input bandwidth is acceptable.

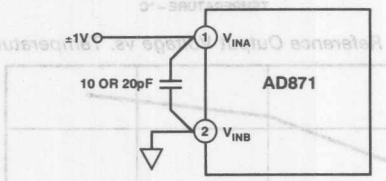


Figure 18. Optional High Frequency Noise Reduction

The AD871 will contribute its own wideband thermal noise. As a result of the integrated wideband noise (0.17 LSB rms, referred-to-input), applying a dc analog input may produce more than one code at the output. A histogram of the ADC output codes, for a dc input voltage, will be between 1 and 3 codes wide, depending on how well the input is centered on a given code and how many samples are taken. Figure 8 shows a typical AD871 code histogram, and Figure 9 illustrates the AD871's transition noise.

REFERENCE INPUT

The nominal reference input should be 2.5 V, taken with respect to REFERENCE GROUND (REF GND). Figure 19 illustrates the equivalent model for the reference input: there is no clock or signal-dependent activity associated with the reference input circuitry, therefore, no "kickback" into the reference.

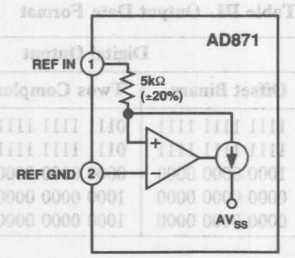


Figure 19. Equivalent Reference Input Circuit

However, in order to realize the lowest noise performance of the AD871, care should be taken to minimize noise at the reference input.

The AD871's reference input impedance is equal to 5 kΩ (±20%), and its effective noise bandwidth is 10 MHz, with a referred-to-input noise gain of 0.8. For example, the internal reference, with an rms noise of 28 μV (using an external 1 μF capacitor), contributes 24 μV (0.05 LSB) of noise to the transfer function of the AD871.

The full-scale peak-to-peak input voltage is a function of the reference voltage, according to the equation:

$$(V_{INA} - V_{INB})\ Full\ Scale = 0.8*(V_{REF} - REF\ GND)$$

Note that the AD871's performance was optimized for a 2.5 V reference input: performance may degrade somewhat for other reference voltages. Figure 20 illustrates the S/(N+D) performance vs. reference voltage for a 1 MHz, −0.5 dB input signal. Note also that if the reference is changed during a conversion, all three conversions in the pipeline will be invalidated.

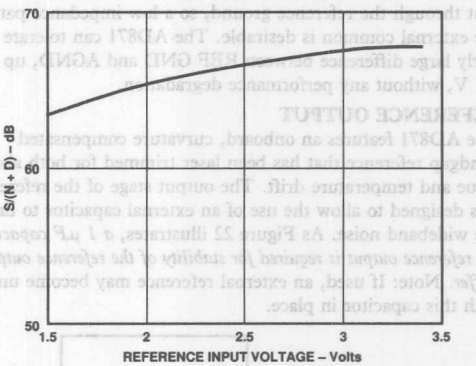


Figure 20. S/(N+D) vs. Reference Input Voltage, f_{IN} = 1 MHz, FS = 5 MHz

Table II summarizes various 2.5 V references suitable for use with the AD871, including the onboard bandgap reference (see REFERENCE OUTPUT section).

Table II. Suitable 2.5 V References

	Drift (PPM/°C)	Initial Accuracy %
REF-43B	6 (max)	0.2
AD680JN	10 (max)	0.4
Internal	30 (typ)	0.4

If an external reference is connected to REF IN, REF OUT must be connected to +5 V. This should lower the current in REF GND to less than 350 μA and eliminate the need for a 1 μF capacitor, although decoupling the reference for noise reduction purposes is recommended.

Alternatively, Figure 21 shows how the AD871 may be driven from other references by use of an external resistor. The external resistor forms a resistor divider with the on-chip 5 kΩ resistor to realize 2.5 V at the reference input pin (REF IN). A trim potentiometer is needed to accommodate the tolerance of the AD871's 5 kΩ resistor.

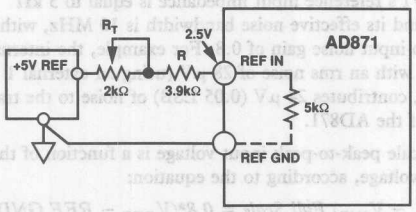


Figure 21. Optional +5 V Reference Input Circuit

REFERENCE GROUND

The REF GND pin provides the reference point for both the reference input, and the reference output. When the internal reference is operating, it will draw approximately 500 μA of current through the reference ground, so a low impedance path to the external common is desirable. The AD871 can tolerate a fairly large difference between REF GND and AGND, up to ±1 V, without any performance degradation.

REFERENCE OUTPUT

The AD871 features an onboard, curvature compensated bandgap reference that has been laser trimmed for both absolute value and temperature drift. The output stage of the reference was designed to allow the use of an external capacitor to limit the wideband noise. As Figure 22 illustrates, *a 1 μF capacitor on the reference output is required for stability of the reference output buffer.* Note: If used, an external reference may become unstable with this capacitor in place.

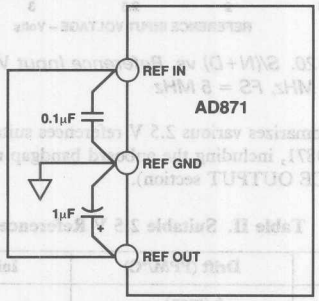


Figure 22. Typical Reference Decoupling Connection

With this capacitor in place, the noise on the reference output is approximately 28 μV rms at room temperature. Figure 23 shows the typical temperature drift performance of the reference, while Figure 24 illustrates the variation in reference voltage with load currents.

The output stage is designed to provide at least 2 mA of output current, allowing a single reference to drive up to four AD871s, or other external loads. The power supply rejection of the reference is better than 54 dB at dc.

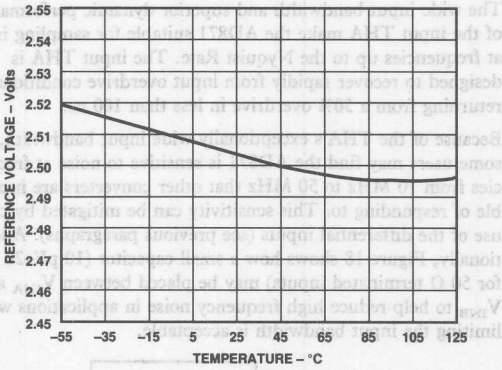


Figure 23. Reference Output Voltage vs. Temperature

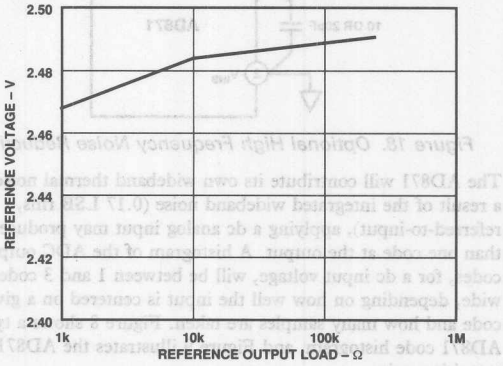


Figure 24. Reference Output Voltage vs. Output Load

DIGITAL OUTPUTS

In 28-pin packages, the AD871 output data is presented in twos complement format. Table III indicates offset binary and twos complement output for various analog inputs.

Table III. Output Data Format

Analog Input	Digital Output		
V_{INA}–V_{INB}	Offset Binary	Twos Complement	OTR
≥0.999756 V	1111 1111 1111	0111 1111 1111	1
0.999268 V	1111 1111 1111	0111 1111 1111	0
0 V	1000 0000 0000	0000 0000 0000	0
−1 V	0000 0000 0000	1000 0000 0000	0
−1.000244 V	0000 0000 0000	1000 0000 0000	1

Users requiring offset binary encoding may simply invert the $\overline{MSB}$ pin. In the 44-pin surface mount packages, both MSB and $\overline{MSB}$ bits are provided.

The AD871 features a digital out-of-range (OTR) bit that goes high when the input exceeds positive full scale or falls below negative full scale. As Table III indicates, the output bits will be set appropriately according to whether it is an out-of-range high condition or an out-of-range low condition. Note that if the input is driven beyond +1.5 V, the digital outputs may not stay at +FS, but may actually fold back to midscale.

The AD871's CMOS digital output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause glitches on the supplies and may affect S/(N+D) performance. Applications requiring the AD871 to drive large capacitive loads or large fanout may require additional decoupling capacitors on DRV_{DD} and DV_{DD}. In extreme cases, external buffers or latches could be used.

THREE-STATE OUTPUTS

The 44-pin surface mount AD871 offers three-state outputs. The digital outputs can be placed into a three-state mode by pulling the OUTPUT ENABLE (OEN) pin LOW. Note that this function is not intended to be used to pull the AD871 on and off a bus at 5 MHz. Rather, it is intended to allow the ADC to be pulled off the bus for evaluation or test modes. Also, to avoid corruption of the sampled analog signal during conversion (3 clock cycles), it is highly recommended that the AD871 be placed on the bus prior to the first sampling.

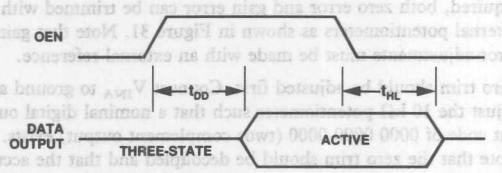


Figure 25. Three-State Output Timing Diagram

For timing budgetary purposes, the typical access and float delay times for the AD871 are 50 ns.

CLOCK INPUT

The AD871 internal timing control uses the two edges of the clock input to generate a variety of internal timing signals. The optimal clock input should have a 50% duty cycle; however, sensitivity to duty cycle is significantly reduced for clock rates of less than 5 megasamples per second.

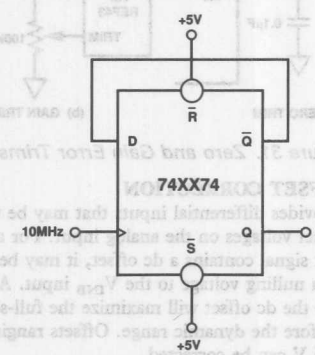


Figure 26. Divide-by-Two Clock Circuit

Due to the nature of on-chip compensation circuitry, the duty cycle should be maintained between 40% and 60% even for clock rates less than 5 Msps. One way to realize a 50% duty cycle clock is to divide down a clock of higher frequency, as shown in Figure 26.

In this case, a 10 MHz clock is divided by 2 to produce the 5 MHz clock input for the AD871. In this configuration, the duty cycle of the 10 MHz clock is irrelevant.

The input circuitry for the CLKIN pin is designed to accommodate both TTL and CMOS inputs. The quality of the logic input, particularly the rising edge, is critical in realizing the best possible jitter performance for the part: the faster the rising edge, the better the jitter performance.

As a result, careful selection of the logic family for the clock driver, as well as the fanout and capacitive load on the clock line, is important. Jitter-induced errors become more pronounced at higher frequency, large amplitude inputs, where the input slew rate is greatest.

The AD871 is designed to support a sampling rate of 5 Msps; running at slightly faster clock rates may be possible, although at reduced performance levels. Conversely, some slight performance improvements might be realized by clocking the AD871 at slower clock rates. Figure 27 presents the S/(N+D) vs. clock frequency for a 1 MHz analog input.

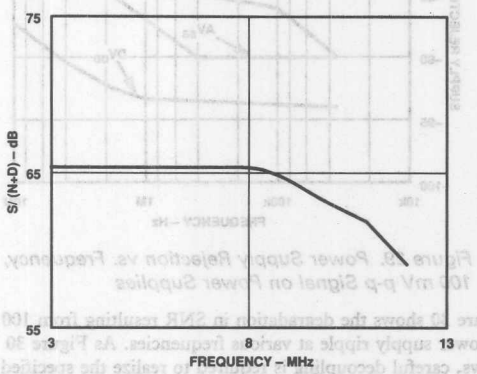


Figure 27. Typical S/(N+D) vs. Clock Frequency f_{IN} = 1 MHz, Full-Scale Input

The power dissipated by the correction logic and output buffers is largely proportional to the clock frequency; running at reduced clock rates provides a slight reduction in power consumption. Figure 28 illustrates this tradeoff.

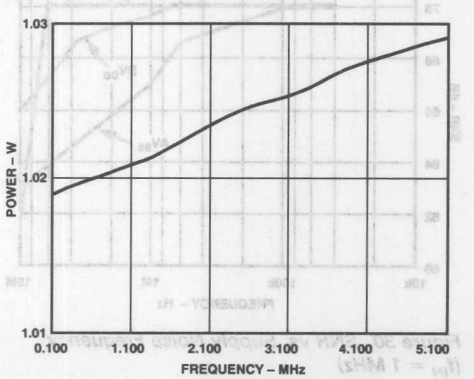


Figure 28. Typical Power Dissipation vs. Clock Frequency

ANALOG SUPPLIES AND GROUNDS

The AD871 features separate analog and digital supply and ground pins, helping to minimize digital corruption of sensitive analog signals. In general, AV_{SS} and AV_{DD}, the analog supplies,

should be decoupled to AGND, the analog common, as close to the chip as physically possible. Care has been taken to minimize the signal dependence of the power supply currents; however, the analog supply currents will be proportional to the reference input. With REFIN at 2.5 V, the typical current into AV_{DD} is 82 mA, while the typical current out of AV_{SS} is 115 mA. Typically, 33 mA will flow into the AGND pin.

Careful design and the use of differential circuitry provide the AD871 with excellent rejection of power supply noise over a wide range of frequencies, as illustrated in Figure 29.

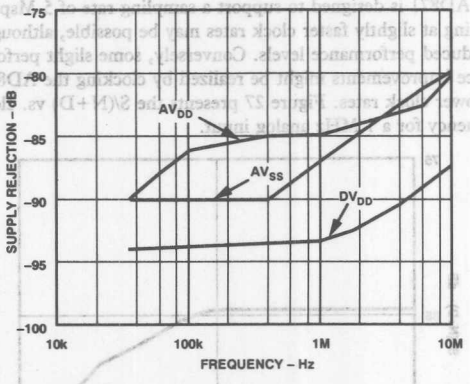


Figure 29. Power Supply Rejection vs. Frequency, 100 mV p-p Signal on Power Supplies

Figure 30 shows the degradation in SNR resulting from 100 mV of power supply ripple at various frequencies. As Figure 30 shows, careful decoupling is required to realize the specified dynamic performance. Figure 34 demonstrates the recommended decoupling strategy for the supply pins. Note that in extremely noisy environments, a more elaborate supply filtering scheme may be necessary.

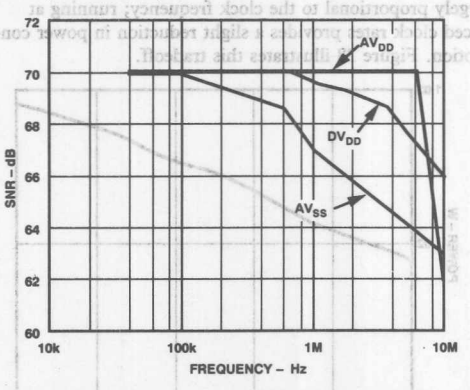


Figure 30. SNR vs. Supply Noise Frequency (f_{IN} = 1 MHz)

DIGITAL SUPPLIES AND GROUNDS

The digital activity on the AD871 chip falls into two general categories: CMOS correction logic, and CMOS output drivers. The internal correction logic draws relatively small surges of current, mainly during the clock transitions; in the 44-pin package, these currents flow through pins DGND and DV_{DD}. The output drivers draw large current impulses while the output bits are changing. The size and duration of these currents is a function of the load on the output bits: large capacitive loads are to be avoided. In the 44-pin package, the output drivers are supplied through dedicated pins DRGND and DRV_{DD}. Pin count constraints in the 28-pin packages require that the digital and driver supplies share package pins (although they have separate bond wires and on-chip routing). The decoupling shown in Figure 34 is appropriate for a reasonable capacitive load on the digital outputs (typically 20 pF on each pin). Applications involving greater digital loads should consider increasing the digital decoupling proportionately, and/or using external buffers/latches.

APPLICATIONS

OPTIONAL ZERO AND GAIN TRIM

The AD871 is factory trimmed to minimize zero error, gain error and linearity errors. In some applications the zero and gain errors of the AD871 need to be externally adjusted to zero. If required, both zero error and gain error can be trimmed with external potentiometers as shown in Figure 31. Note that gain error adjustments must be made with an external reference.

Zero trim should be adjusted first. Connect V_{INA} to ground and adjust the 10 kΩ potentiometer such that a nominal digital output code of 0000 0000 0000 (twos complement output) exists. Note that the zero trim should be decoupled and that the accuracy of the ±2.5 V reference signals will directly affect the offset.

Gain error may then be calibrated by adjusting the REF IN voltage. The REF IN voltage should be adjusted such that a +1 V input on V_{INA} results in the digital output code 0111 1111 1111 (twos complement output).

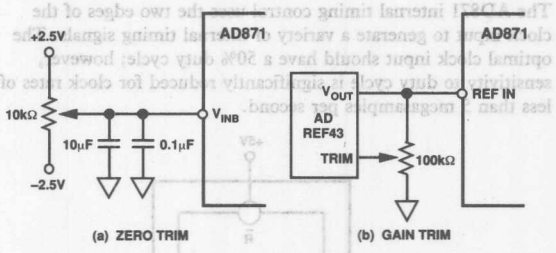


Figure 31. Zero and Gain Error Trims

DIGITAL OFFSET CORRECTION

The AD871 provides differential inputs that may be used to correct for any offset voltages on the analog input. For applications where the input signal contains a dc offset, it may be advantageous to apply a nulling voltage to the V_{INB} input. Applying a voltage equal to the dc offset will maximize the full-scale input range and therefore the dynamic range. Offsets ranging from −0.7 V to +0.5 V can be corrected.

Figure 32 shows how a dc offset can be applied using the AD568 12-bit, high speed digital-to-analog converter (DAC). This circuit can be used for applications requiring offset adjustments on every clock cycle. The AD568 connection scheme is used to provide a −0.512 V to +0.512 V output range. The offset voltage must be stable on the rising edge of the AD871 clock input.

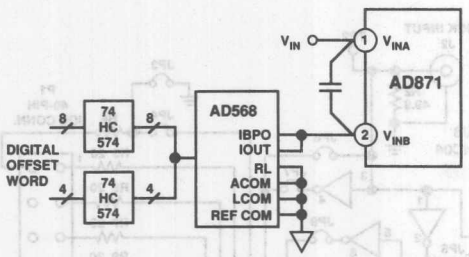


Figure 32. Offset Correction Using the AD568

UNDERSAMPLING USING THE AD871 AND AD9100

The AD871's on-chip THA optimizes transient response while maintaining low noise performance. For super-Nyquist (undersampling) applications it may be necessary to use an external THA with fast track-mode slew rate and hold mode settling time. An excellent choice for this application is the AD9100, an ultrahigh speed track-and-hold amplifier.

In order to maximize the spurious free dynamic range of the circuit in Figure 33 it is advantageous to present a small signal to the input of the AD9100 and then amplify the output to the AD871's full-scale input range. This can be accomplished with a low distortion, wide bandwidth amplifier such as the AD9617. The circuit uses a gain of 3.5 to optimize S/(N+D).

The peak performance of this circuit is obtained by driving the AD871 + AD9100 combination with a full-scale input. For small scale input signals (−20dB, −40 dB), the AD871 performs better without the track-and-hold because slew-limiting effects are no longer dominant. To gain the advantages of the added track-and-hold, it is important to give the AD871 a full-scale input.

An alternative to the configuration presented above is to use the AD9101 track-and-hold amplifier. The AD9101 provides a built-in post amplifier with a gain of 4, providing excellent ac characteristics in conjunction with a high level of integration.

As illustrated in Figure 33, it is necessary to skew the AD871 sample clock and the AD9100 sample/hold control. Clock skew (t_S) is defined as the time starting at the AD9100's transition into hold mode and ending at the moment the AD871 samples. The AD871 samples on the rising edge of the sample clock, and the AD9100 samples on the falling edge of the sample/hold control. The choice of t_S is primarily determined by the settling time of the AD9100. The droop rate of the AD9100 must also be taken into consideration. Using these values, the ideal t_S is 17 ns. When choosing clock sources, it is extremely important that the front end track-and-hold sample/hold control is given a very low jitter clock source. This is not as crucial for the AD871 sample clock, because it is sampling a dc signal.

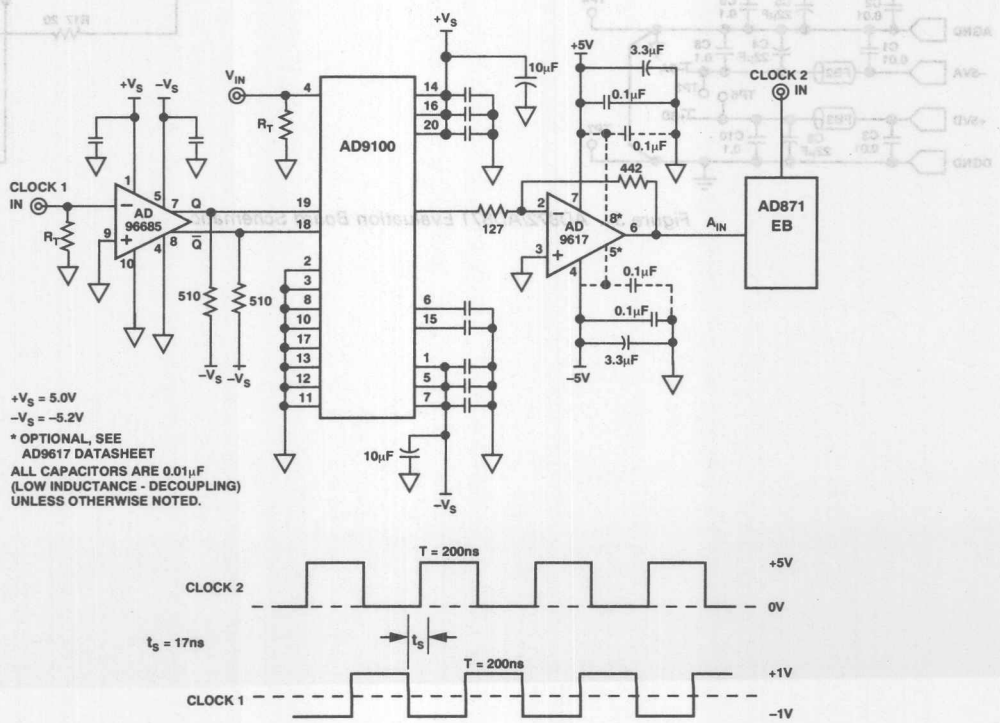


Figure 33. Undersampling Using the AD871 and AD9100

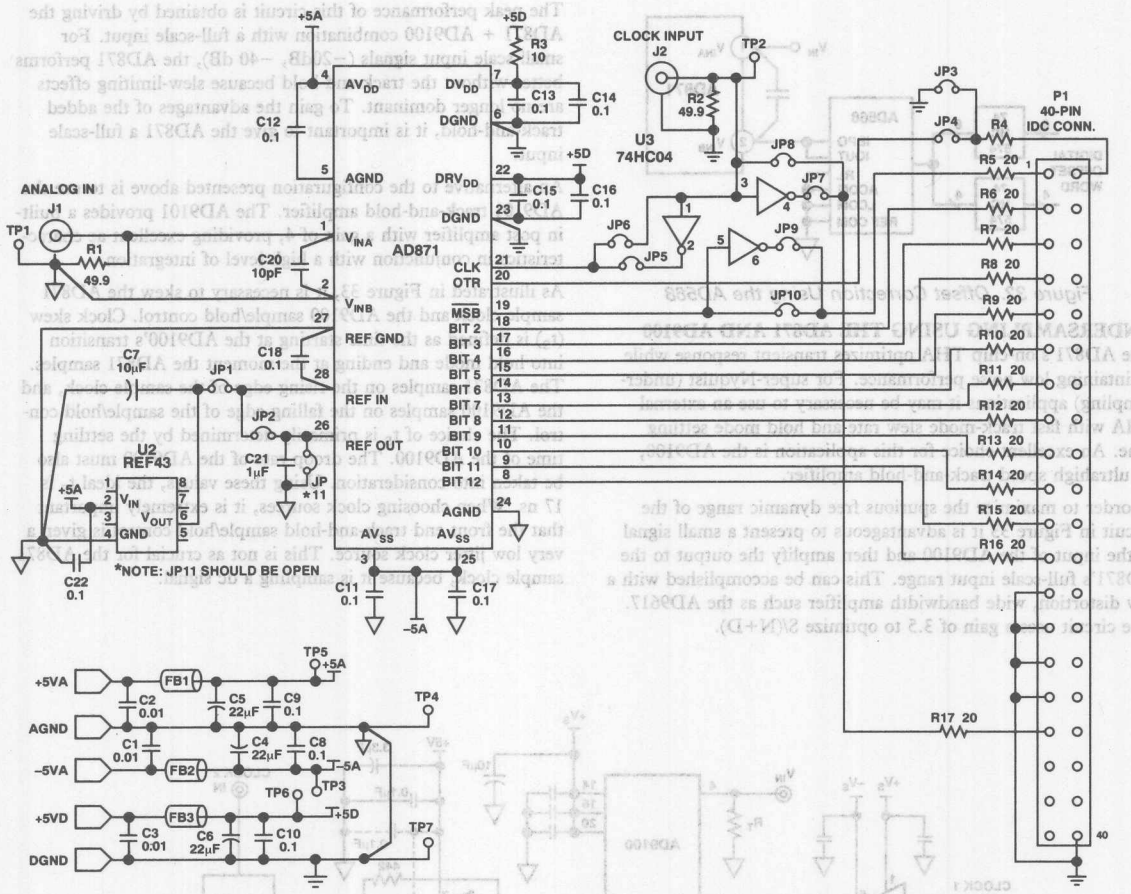


Figure 34. AD872/AD871 Evaluation Board Schematic

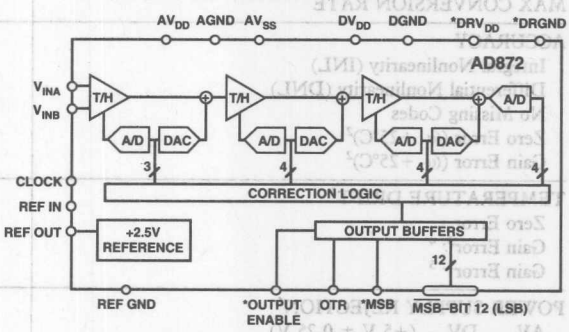
Complete 12-Bit 10 MSPS Monolithic A/D Converter

AD872

FEATURES

- Monolithic 12-Bit 10 MSPS A/D Converter
- Low Power Dissipation: 1.15 W
- No Missing Codes Guaranteed
- Differential Nonlinearity Error: 0.5 LSB
- Complete: On-Chip Track-and-Hold Amplifier and Voltage Reference
- Signal-to-Noise and Distortion Ratio: 65 dB
- Spurious-Free Dynamic Range: 72 dB
- Out of Range Indicator
- Twos Complement Binary Output Data
- 28-Pin Ceramic DIP or 44-Pin Surface Mount Package

FUNCTIONAL BLOCK DIAGRAM



* ONLY AVAILABLE ON 44 PIN SURFACE MOUNT PACKAGE.

PRODUCT DESCRIPTION

The AD872 is a monolithic 12-bit, 10 Msps analog to digital converter with an on-chip, high performance track-and-hold amplifier and voltage reference. The AD872 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 10 Msps data rates and guarantees no missing codes over the full operating temperature range. The AD872 combines a merged high speed bipolar/CMOS process and a novel architecture to achieve the resolution and speed of hybrid implementations at a fraction of the power consumption. Additionally, the greater reliability of monolithic construction offers improved system reliability and lower costs than hybrid designs.

The high input impedance, fast-settling input track-and-hold (T/H) amplifier is equally suited for both multiplexed systems that switch negative to positive full-scale voltage levels in successive channels and sampling single-channel inputs at frequencies up to and beyond the Nyquist rate. The AD872's wideband input combined with the power and cost savings over previously available hybrids will allow new design opportunities in communications, imaging and medical applications. The AD872 provides both reference output and reference input pins, allowing the onboard reference to serve as a system reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. A single clock input is used to control all internal conversion cycles. The digital output data is presented in twos complement binary output format. An out-of-range signal indicates an overflow condition. It can be used with the most significant bit to determine low or high overflow.

The AD872 is fabricated on Analog Devices ABCMOS-1 process which utilizes high speed bipolar and CMOS transistors on a single chip. High speed, precision analog circuits are now combined with high density logic circuits.

The AD872 is packaged in a 28-pin ceramic DIP and a 44-pin leadless ceramic surface mount package and is specified for operation from 0°C to +70°C and −55°C to +125°C.

PRODUCT HIGHLIGHTS

The AD872 offers a complete single-chip sampling 12-bit, 10 Msps analog-to-digital conversion function in a 28-pin DIP or 44-pin leadless ceramic surface mount package (LCC).

Low Power—The AD872 at 1.15 W consumes a fraction of the power of presently available hybrids.

Onboard Track-and-Hold (T/H)—The high impedance T/H input eliminates the need for external buffers and can be configured for single ended or differential inputs.

Out of Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD872's input range.

Ease-of-Use—The AD872 is complete with T/H and voltage reference.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter	J Grade[1]	S Grade[1]	Units
RESOLUTION	12	12	Bits min
MAX CONVERSION RATE	10	10	MHz min
ACCURACY			
Integral Nonlinearity (INL)	±2.5	±2.5	LSB typ
Differential Nonlinearity (DNL)	±0.5	±0.5	LSB typ
No Missing Codes	12	12	Bits Guaranteed
Zero Error (@ +25°C)[2]	±0.75	±0.75	% FSR max
Gain Error (@ +25°C)[2]	±1.25	±1.25	% FSR max
TEMPERATURE DRIFT[3]			
Zero Error	±0.15	±0.30	% FSR max
Gain Error[3, 4]	±0.80	±1.75	% FSR max
Gain Error[3, 5]	±0.25	±0.50	% FSR max
POWER SUPPLY REJECTION[6]			
AV_{DD}, DV_{DD} (+5 V ± 0.25 V)	±0.125	±0.125	% FSR max
AV_{SS} (−5 V ± 0.25 V)	±0.125	±0.125	% FSR max
ANALOG INPUT			
Input Range	±1	±1	Volts max
Input Resistance	50	50	kΩ typ
Input Capacitance	10	10	pF typ
INTERNAL VOLTAGE REFERENCE			
Output Voltage	2.5	2.5	Volts typ
Output Voltage Tolerance	±20	±40	mV max
Output Current (Available for External Loads)	2.0	2.0	mA typ
(External load should not change during conversion.)			
REFERENCE INPUT RESISTANCE	5	5	kΩ typ
POWER SUPPLIES			
Supply Voltages			
AV_{DD}	+5	+5	V (±5% AV_{DD} Operating)
AV_{SS}	−5	−5	V (±5% AV_{SS} Operating)
DV_{DD}	+5	+5	V (±5% DV_{DD} Operating)
Supply Current			
IAV_{DD}	87	88	mA max (78 mA typ)
IAV_{SS}	147	150	mA max (134 mA typ)
IDV_{DD}	20	21	mA max (15 mA typ)
POWER CONSUMPTION	1.15	1.15	W typ
	1.25	1.3	W max

NOTES

[1]Temperature ranges are as follows: J Grade: 0°C to +70°C, S Grade: −55°C to +125°C.

[2]Adjustable to zero with external potentiometers (See Zero and Gain Error Calibration section).

[3]+25°C to T_{MIN} and +25°C to T_{MAX}.

[4]Includes internal voltage reference error.

[5]Excludes internal reference drift.

[6]Change in Gain Error as a function of the dc supply voltage.

Specifications subject to change without notice.

AC SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, AV_{SS} = −5 V, f_{SAMPLE} = 10 Msps, unless otherwise noted)[1]

	J Grade	S Grade	Units
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)			
f_{INPUT} = 1 MHz	65	64	dB typ
	61	61	dB min
f_{INPUT} = 4.99 MHz	63	63	dB typ
TOTAL HARMONIC DISTORTION (THD)			
f_{INPUT} = 1 MHz	−70	−68	dB typ
	−63	−62	dB max
f_{INPUT} = 4.99 MHz	−66	−65	dB typ
SPURIOUS FREE DYNAMIC RANGE			
f_{INPUT} = 1 MHz	72	72	dB typ
f_{INPUT} = 4.99 MHz	70	70	dB typ
INTERMODULATION DISTORTION (IMD)[2]	70	70	dB typ
FULL POWER BANDWIDTH	70	70	MHz typ
SMALL SIGNAL BANDWIDTH	70	70	MHz typ
APERTURE DELAY	8	8	ns typ
APERTURE JITTER	10	10	ps rms typ
ACQUISITION TO FULL-SCALE STEP	40	40	ns typ
OVERVOLTAGE RECOVERY TIME	40	40	ns typ

NOTES
[1]f_{IN} amplitude = −0.5 dB full scale unless otherwise indicated. All measurements referred to a 0 dB (1 V pk) input signal unless otherwise indicated.
[2]fa = 1.0 MHz, fb = 0.95 MHz with f_{SAMPLE} = 10 MHz, typical value for second and third order products.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, AV_{SS} = −5 V unless otherwise noted)

Parameter	Symbol	J, S Grades	Units
LOGIC INPUTS			
High Level Input Voltage	V_{IH}	+2.0	V min
Low Level Input Voltage	V_{IL}	+0.8	V max
High Level Input Current (V_{IN} = DV_{DD})	I_{IH}	±10	μA max
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	±10	μA max
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUTS			
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	+2.4	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	+0.4	V max
Output Capacitance	C_{OUT}	5	pF typ
Leakage (Three-State, LCC Only)	IZ	±10	μA max

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, AV_{SS} = −5 V; V_{IL} = 0.8 V, V_{IH} = 2.0 V, V_{OL} = 0.4 V and V_{OH} = 2.4 V)

Parameter	Symbol	J, S Grades	Units
Clock Period[1]	t_C	100	ns min
CLOCK Pulse Width High	t_{CH}	45	ns min
CLOCK Pulse Width Low	t_{CL}	45	ns min
Clock Duty Cycle[2]		40	% min (50% typ)
		60	% max
Output Delay	t_{OD}	10	ns min (20 ns typ)
Pipeline Delay (Latency)		3	Clock Cycles max
Data Access Time (LCC Package Only)[3]	t_{DD}	50	ns typ (100 pF Load)
Output Float Delay (LCC Package Only)[3]	t_{HL}	50	ns typ (10 pF Load)

NOTES
[1]Conversion rate is operational down to 10 kHz without degradation in specified performance.
[2]For clock periods of 200 ns or greater, see Clock Input Section.
[3]See Section on Three-State Outputs for timing diagrams and application information.
Specifications subject to change without notice.

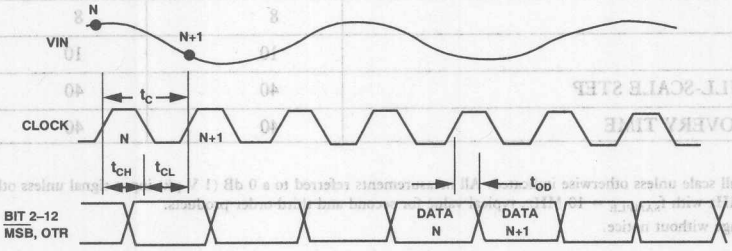


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	With Respect to	Min	Max	Units
AV_{DD}	AGND	−0.5	+6.5	Volts
AV_{SS}	AGND	−6.5	+0.5	Volts
DV_{DD}, DRV_{DD}[2]	DGND, DRGND	−0.5	+6.5	Volts
DRV_{DD}[2]	DV_{DD}	−6.5	+6.5	Volts
DRGND[2]	DGND	−0.3	+0.3	Volts
AGND	DGND	−1.0	+1.0	Volts
AV_{DD}	DV_{DD}	−6.5	+6.5	Volts
Clock Input, OEN	DGND	−0.5	DV_{DD} + 0.5	Volts
Digital Outputs	DGND	−0.5	DV_{DD} + 0.3	Volts
V_{INA}, V_{INB} REF IN	AGND	−6.5	+6.5	Volts
REF IN	AGND	AV_{SS}	AV_{DD}	Volts
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
[2]LCC Package Only.

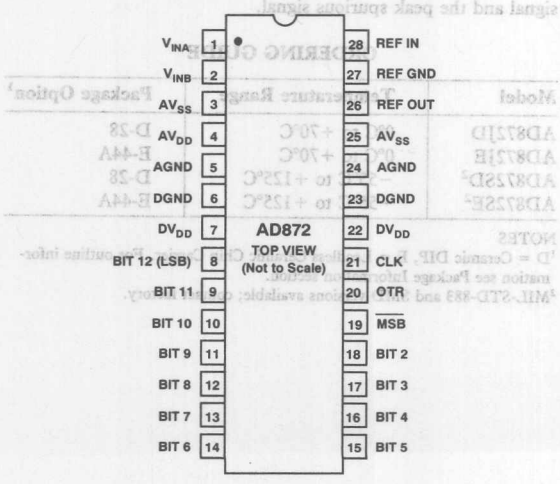
PIN DESCRIPTION

Symbol	DIP Pin No.	LCC Pin No.	Type	Name and Function
AGND	5, 24	9, 36	P	Analog Ground.
AV_{DD}	4	6, 38	P	+5 V Analog Supply.
AV_{SS}	3, 25	5, 40	P	−5 V Analog Supply.
$\overline{MSB}$	19	29	DO	Inverted Most Significant Bit. Provides twos complement output data format.
MSB	N/A	27	DO	Most Significant Bit.
BIT 2–BIT 11	18–9	26–17	DO	Data Bits 2 through 11.
BIT 12 (LSB)	8	16	DO	Least Significant Bit.
CLK	21	31	DI	Clock Input. The AD872 will initiate a conversion on the rising edge of the clock input. See the Timing Diagram for details.
DV_{DD}	7, 22	33	P	+5 V Digital Supply.
DGND	6, 23	10	P	Digital Ground.
DRV_{DD}	N/A	12, 32	P	+5 V Digital Supply for the output drivers.
DRGND	N/A	11, 34	P	Digital Ground for the output drivers. (See section on Power Supply Decoupling for details on DRV_{DD} and DRGND.)
OTR	20	30	DO	Out of Range is Active HIGH on the leading edge of code 0 or the trailing edge of code 4096. See Output Data Format Table III.
OEN	N/A	13	DI	Output Enable. See the Three State Output Timing Diagram for details.
REF GND	27	42	AI	Reference Ground.
REF IN	28	43	AI	Reference Input. +2.5 V input gives ±1 V full-scale range.
REF OUT	26	41	AO	+2.5 V Reference Output. Tie to REF IN for normal operation.
V_{INA}	1	1	AI	(+) Analog Input Signal on the differential input amplifier.
V_{INB}	2	2	AI	(−) Analog Input Signal on the differential input amplifier.
NC	N/A	3, 4, 7, 8, 14, 15 28, 35, 37, 39, 44		No Connect.

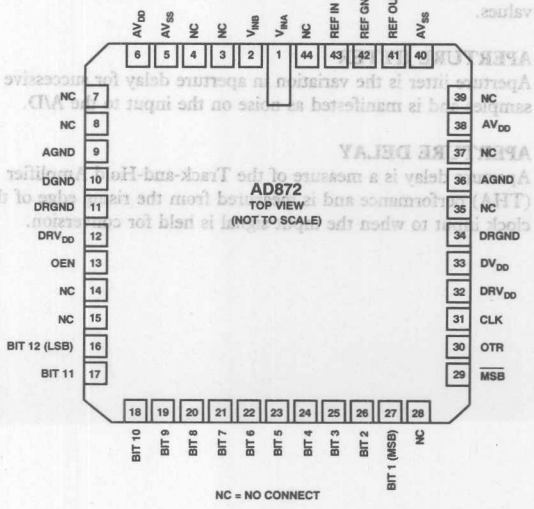
TYPE: AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; P = Power; N/A = Not Available on 28-pin DIP. Only available on 44-pin surface mount package.

PIN CONFIGURATIONS

28-Pin Ceramic DIP



44-Pin LCC



Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL LINEARITY ERROR (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes must be present over all operating ranges.

ZERO ERROR

The major carry transition should occur for an analog value 1/2 LSB below analog common. Zero error is defined as the deviation of the actual transition from that point. The zero error and temperature drift specify the initial deviation and maximum change in the zero error over temperature.

GAIN ERROR

The first code transition should occur for an analog value 1/2 LSB above nominal negative full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

TEMPERATURE DRIFT

The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The specifications show the maximum change in the converter's full scale as the supplies are varied from nominal to min/max values.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

APERTURE DELAY

Aperture delay is a measure of the Track-and-Hold Amplifier (THA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

OVERVOLTAGE RECOVERY

The number of clock cycles required for the ADC to achieve a specified accuracy after an overvoltage (50% greater than full-scale range), measured from the time the overvoltage signal reenters the converter's range.

DYNAMIC SPECIFICATIONS

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

INTERMODULATION DISTORTION (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb), and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (2 fb − fa). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sums is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

FULL-POWER BANDWIDTH

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

SPURIOUS FREE DYNAMIC RANGE

The difference, in dB, between the rms amplitude of the input signal and the peak spurious signal.

ORDERING GUIDE

Model	Temperature Range	Package Option[1]
AD872JD	0°C to +70°C	D-28
AD872JE	0°C to +70°C	E-44A
AD872SD[2]	−55°C to +125°C	D-28
AD872SE[2]	−55°C to +125°C	E-44A

NOTES
[1]D = Ceramic DIP, E = Leadless Ceramic Chip Carrier. For outline information see Package Information section.
[2]MIL-STD-883 and SMD versions available; contact factory.

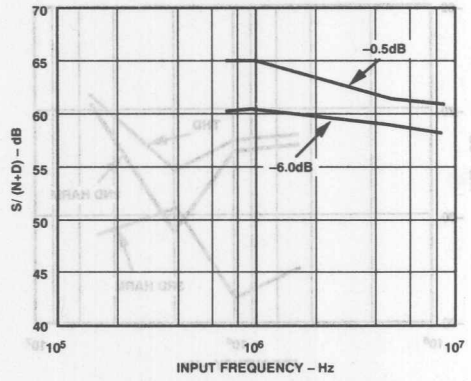


Figure 2. AD872 S/(N+D) vs. Input Frequency

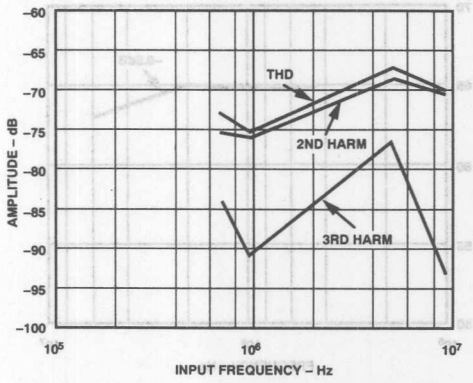


Figure 3. AD872 Distortion vs. Input Frequency, Full-Scale Input

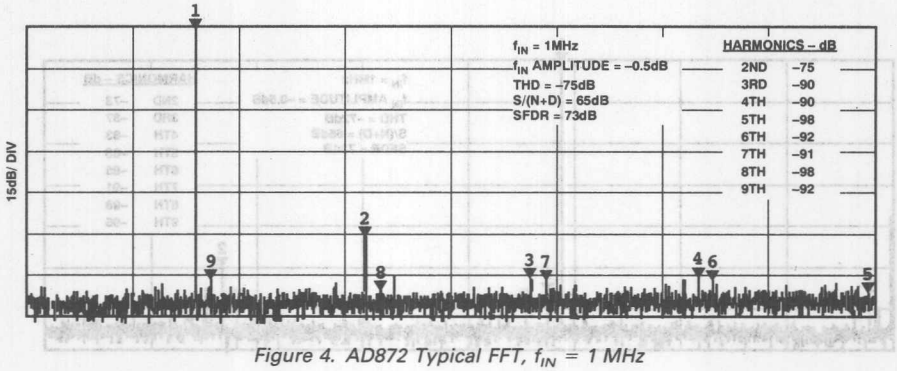


Figure 4. AD872 Typical FFT, f_{IN} = 1 MHz

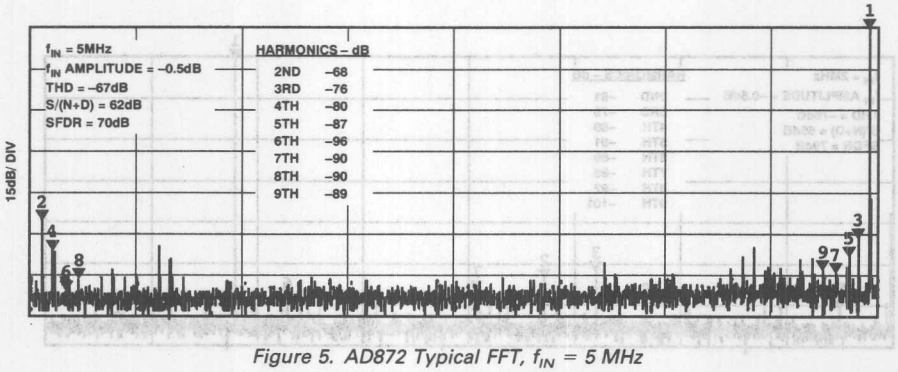


Figure 5. AD872 Typical FFT, f_{IN} = 5 MHz

AD872—Dynamic Characteristics–Sample Rate: 5 MSPS

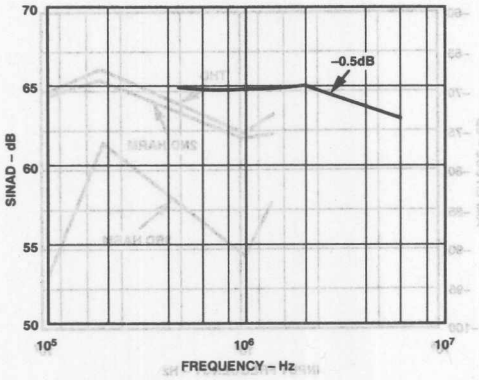


Figure 6. AD872 S/(N+D) vs. Input Frequency

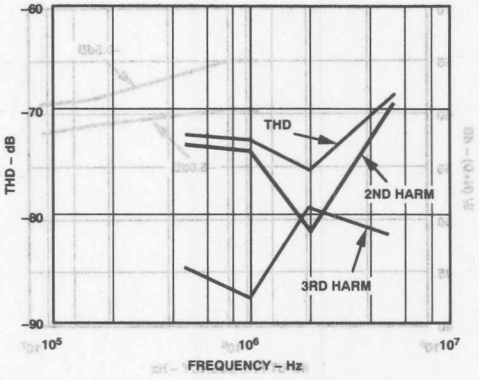


Figure 7. AD872 Distortion vs. Input Frequency, Full-Scale Input

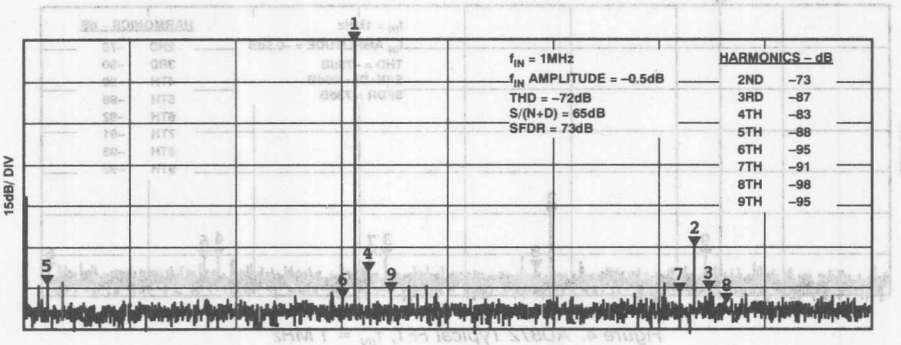


Figure 8. AD872 Typical FFT, f_{IN} = 1 MHz

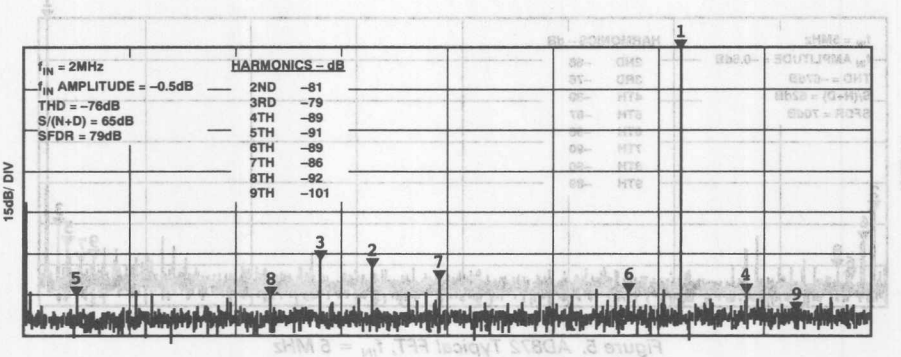


Figure 9. AD872 Typical FFT, f_{IN} = 2 MHz

THEORY OF OPERATION

The AD872 is implemented using a 4-stage pipelined multiple flash architecture. A differential input track-and-hold amplifier (THA) acquires the input and converts the input voltage into a differential current. A 3-bit approximation of the input is made by the first flash converter, and an accurate analog representation of this 3-bit guess is generated by a digital-to-analog converter. This approximation is subtracted from the THA output to produce a remainder, or residue. This residue is then sampled and held by the second THA, and a 4-bit approximation is generated and subtracted by the second stage. Once the second THA goes into hold, the first stage goes back into track to acquire a new input signal. The third stage provides another 4-bit approximation/subtraction operation, and produces the final residue, which is passed to a final 4-bit flash converter. The 15 output bits from the 4 flash converters are accumulated in the correction logic block, which adds the bits together using the appropriate correction algorithm, to produce the 12-bit output word. The digital output, together with overrange indicator, is latched into an output buffer to drive the output pins.

The additional THA inserted in each stage of the AD872 architecture allows pipelining of the conversion. In essence, the converter is converting multiple inputs simultaneously, processing them through the converter chain serially. This means that while the converter is capable of capturing a new input sample every clock cycle, it actually takes three clock cycles for the conversion to be fully processed and appear at the output. This "pipeline delay" is often referred to as latency, and is not a concern in most applications, however there are some cases where it may be a consideration. For example, some applications call for the A/D converter to be placed in a high speed feedback loop, where its input is servoed to provide a desired result at the digital output (e.g., offset calibration or zero restoration in video applications). In these cases the 3 clock cycle delay through the pipeline must be accounted for in the loop stability calculations. Also, because the converter is working on three conversions simultaneously, major disruptions to the part (such as a large glitch on the supplies or reference) may corrupt three data samples. Finally, there will be a minimum clock rate below which the THA droop corrupts the signal in the pipeline. In the case of the AD872, this minimum clock rate is 10 kHz.

The high impedance differential inputs of the AD872 allow a variety of input configurations (see APPLYING THE AD872). The AD872 converts the voltage difference between the V_{INA} and V_{INB} pins. For single-ended applications, one input pin (V_{INA} or V_{INB}) may be grounded, but even in this case the differential input can provide a performance boost: for example, for an input coming from a coaxial cable, V_{INB} can be tied to the shield ground, allowing the AD872 to reject shield noise as common mode. The high input impedance of the device minimizes external driving requirements and allows the user to externally select the appropriate termination impedance for the application.

The AD872 clock circuitry uses both edges of the clock in its internal timing circuitry (see spec page for exact timing requirements.) The AD872 samples the analog input on the rising edge of the clock input. During the clock low time (between the falling edge and rising edge of the clock) the input THA is in track mode; during the clock high time it is in hold. System disturbances just prior to the rising edge of the clock may cause the part to acquire the wrong value, and should be minimized.

While the part uses both clock edges for its timing, jitter is only a significant issue for the rising edge of the clock (see CLOCK INPUT section).

APPLYING THE AD872

ANALOG INPUTS

The AD872 features a high impedance differential input that can readily operate on either single-ended or differential input signals. Table I summarizes the nominal input voltage span for both single-ended and differential modes, assuming a 2.5 V reference input.

Table I. Input Voltage Span

	V_{INA}	V_{INB}	$V_{INA}-V_{INB}$
Single-Ended	+1 V	GND	+1 V (Positive Full Scale)
	−1 V	GND	−1 V (Negative Full Scale)
Differential	+0.5 V	−0.5 V	+1 V (Positive Full Scale)
	−0.5 V	+0.5 V	−1 V (Negative Full Scale)

Figure 10 shows an approximate model for the analog input circuit. As this model indicates, when the input exceeds 1.6 V (with respect to AGND), the input device may saturate, causing the input impedance to drop substantially and significantly reducing the performance of the part. Input compliance in the negative direction is somewhat larger, showing virtually no degradation in performance for inputs as low as −1.9 V.

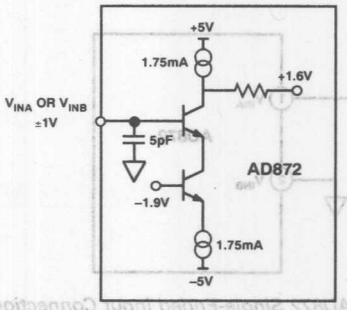


Figure 10. AD872 Equivalent Analog Input Circuit

Figure 11 illustrates the effect of varying the common-mode voltage of a −1 dB input signal on total harmonic distortion.

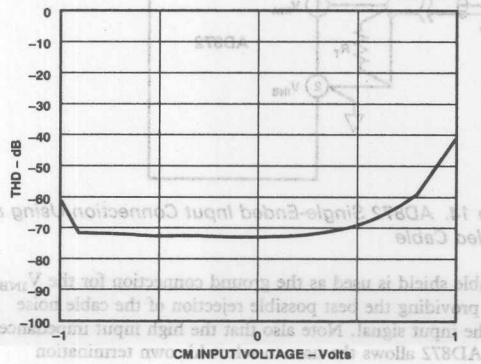


Figure 11. AD872 Total Harmonic Distortion vs. CM Input Voltage, f_{IN} = 1 MHz, FS = 10 MSPS

common-mode rejection out over a wide bandwidth affords the user the opportunity to eliminate many potential sources of input noise as common mode by using the differential input structure of the AD872.

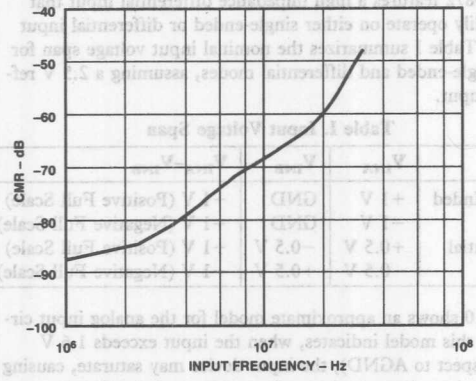


Figure 12. Common-Mode Rejection vs. Input Frequency, 1 V p-p Input

Figures 13 and 14 illustrate typical input connections for single-ended inputs.

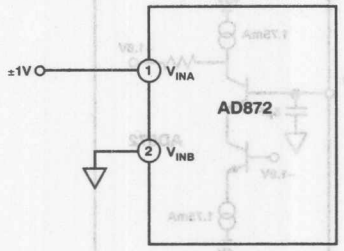


Figure 13. AD872 Single-Ended Input Connection

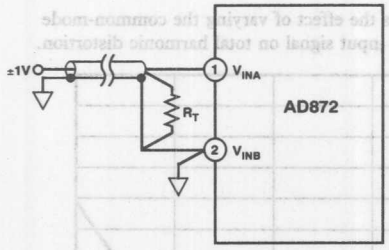


Figure 14. AD872 Single-Ended Input Connection Using a Shielded Cable

The cable shield is used as the ground connection for the V_{INB} input, providing the best possible rejection of the cable noise from the input signal. Note also that the high input impedance of the AD872 allows the user to select his own termination impedance, be it 50 ohms, 75 ohms, or some other value. Furthermore, unlike many flash converters, most AD872 applica-

Figure 15 illustrates how external amplifiers may be used to convert a single-ended input into a differential signal. The resistor values of 536 Ω and 562 Ω were selected to provide optimum phase matching between U1 and U2.

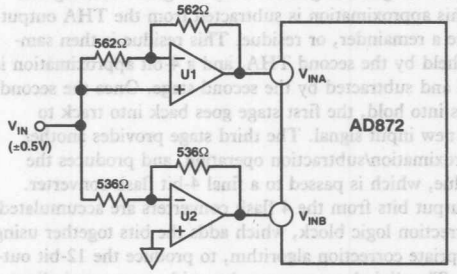


Figure 15. Single-Ended to Differential Connections; U1, U2 = AD811 or AD9617

The use of the differential input signal can help to minimize even-order distortion from the input THA where performance beyond −70 dB is desired.

Figure 16 shows the AD872 large signal (−0.5 dB) and small signal (−20 dB) frequency response.

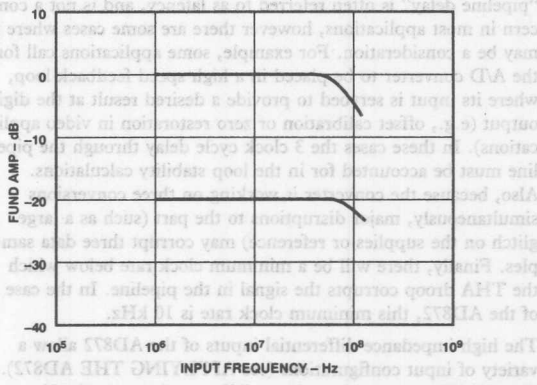


Figure 16. Full Power (−0.5 dB) and Small Signal Response (−20 dB) vs. Input Frequency

The AD872's wide input bandwidth facilitates rapid acquisition of transient input signals: the input THA can typically settle to 12-bit accuracy from a full-scale input step in less than 40 ns. Figure 17 illustrates the typical acquisition of a full-scale input step.

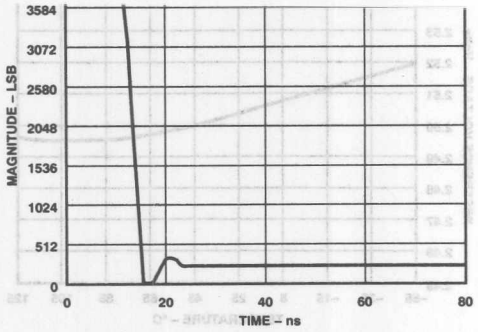


Figure 17. Typical AD872 Settling Time

The wide input bandwidth and superior dynamic performance of the input THA makes the AD872 suitable for undersampling applications where the input frequency exceeds half the sampling frequency. The input THA is designed to recover rapidly from input overdrive conditions, returning from a 50% overdrive in less than 50 ns.

Because of the THA's exceptionally wide input bandwidth, some users may find the AD872 is sensitive to noise at frequencies from 50 MHz to 100 MHz that other converters are incapable of responding to. This sensitivity can be mitigated by careful use of the differential inputs (see previous paragraphs). Additionally, Figure 18 shows how a small capacitor (10 pF–20 pF for 50-ohm terminated inputs) may be placed between V_{INA} and V_{INB} to help reduce high frequency noise in applications where limiting the input bandwidth is acceptable.

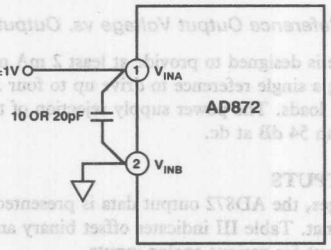


Figure 18. Optional High Frequency Noise Reduction

The AD872 will contribute its own wideband thermal noise. As a result of the integrated wideband noise (1/2 LSB rms, referred-to-input), applying a dc analog input produces more than one code at the output. A histogram analysis of the AD872 with a dc input will show a bell shaped curve consistent with the Guassian nature of the thermal noise. This histogram will be between 3 and 5 codes wide, depending on how well the input is centered on a given code and how many samples are taken.

REFERENCE INPUT

The nominal reference input should be 2.5 V, taken with respect to REFERENCE GROUND (REF GND). Figure 19 illustrates the equivalent model for the reference input: there is no clock or signal-dependent activity associated with the reference input circuitry, therefore, no "kickback" into the reference.

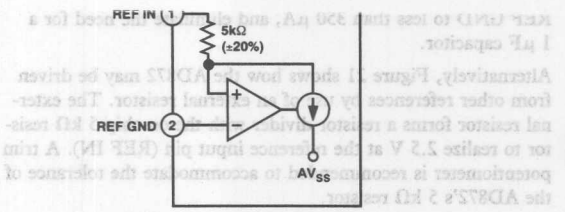


Figure 19. Equivalent Reference Input Circuit

The AD872's input impedance is 5 kΩ, with a tolerance of ±20%. The effective noise bandwidth through the input channel is 10 MHz, and the referred-to-input noise gain is 0.4. For example, the internal reference, with peak-to-peak noise of 180 μV (using an external 1 μF capacitor), contributes 0.3 LSBs of noise to the transfer function of the AD872.

The full-scale peak-to-peak input voltage is a function of the reference voltage, according to the equation:

$$(V_{INA} - V_{INB})\ Full\ Scale = 0.8*(V_{REF} - REF\ GND)$$

Note that the AD872's performance was optimized for a 2.5 V reference input: performance will degrade somewhat for other reference voltages. Figure 20 illustrates the S/(N+D) performance vs. reference voltage for a 1 MHz, −0.5 dB input signal. Note also that if the reference is changed during a conversion, all three conversions in the pipeline will be invalidated.

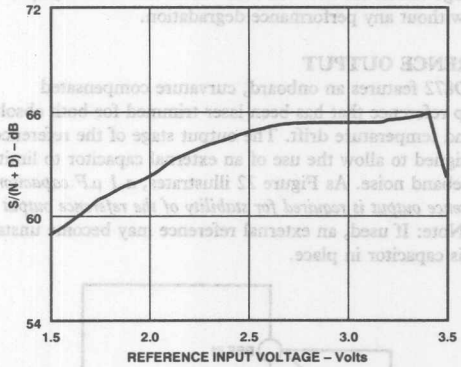


Figure 20. S/(N+D) vs. Reference Input Voltage, f_{IN} = 1 MHz, FS = 10 MHz

Table II summarizes various 2.5 V references suitable for use with the AD872, including the onboard bandgap reference (see REFERENCE OUTPUT section).

Table II. Suitable 2.5 V References

	Drift (PPM/°C)	Initial Accuracy %
REF-43B	6 (max)	0.2
AD680JN	10 (max)	0.4
Internal	30 (typ)	0.4

If an external reference is connected to REF IN, REF OUT must be connected to +5 V. This should lower the current in REF GND to less than 350 μA, and eliminate the need for a 1 μF capacitor.

Alternatively, Figure 21 shows how the AD872 may be driven from other references by use of an external resistor. The external resistor forms a resistor divider with the on-chip 5 kΩ resistor to realize 2.5 V at the reference input pin (REF IN). A trim potentiometer is recommended to accommodate the tolerance of the AD872's 5 kΩ resistor.

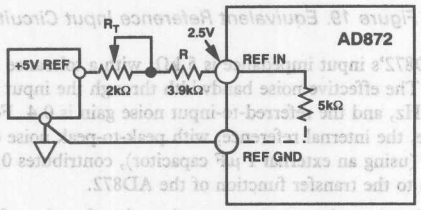


Figure 21. Optional +5 V Reference Input Circuit

REFERENCE GROUND

The REF GND pin provides the reference point for both the reference input, and the reference output. When the internal reference is operating, it will draw approximately 500 μA of current through the reference ground, so a low impedance path to the external common is desirable. The AD872 can tolerate a fairly large difference between REF GND and AGND, up to ±1 V, without any performance degradation.

REFERENCE OUTPUT

The AD872 features an onboard, curvature compensated bandgap reference that has been laser trimmed for both absolute value and temperature drift. The output stage of the reference was designed to allow the use of an external capacitor to limit the wideband noise. As Figure 22 illustrates, *a 1 μF capacitor on the reference output is required for stability of the reference output buffer.* Note: If used, an external reference may become unstable with this capacitor in place.

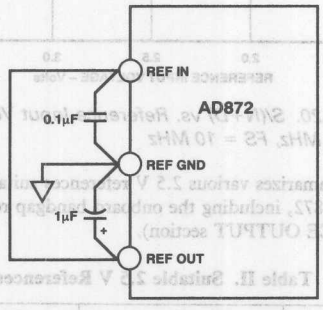


Figure 22. Typical Reference Decoupling Connection

With this capacitor in place, the noise on the reference output is approximately 30 μV rms at room temperature. Figure 23 shows the typical temperature drift performance of the reference, while Figure 24 illustrates the variation in reference voltage with load currents.

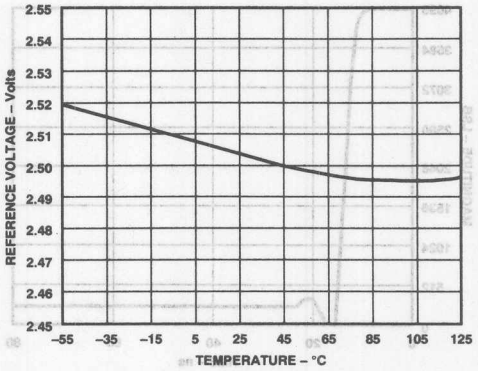


Figure 23. Reference Output Voltage vs. Temperature

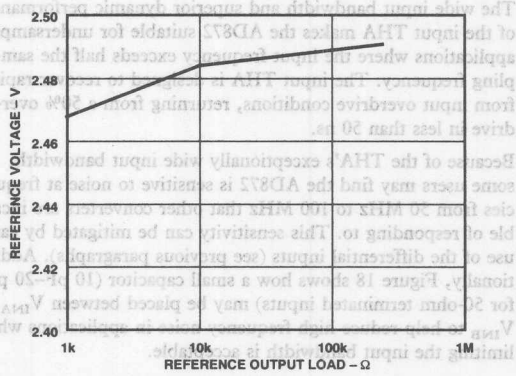


Figure 24. Reference Output Voltage vs. Output Load

The output stage is designed to provide at least 2 mA of output current, allowing a single reference to drive up to four AD872s, or other external loads. The power supply rejection of the reference is better than 54 dB at dc.

DIGITAL OUTPUTS

In 28-pin packages, the AD872 output data is presented in twos complement format. Table III indicates offset binary and twos complement output for various analog inputs.

Table III. Output Data Format

Analog Input	Digital Output		
V_{INA}–V_{INB}	Offset Binary	Twos Complement	OTR
≥0.999756 V	1111 1111 1111	0111 1111 1111	1
0.999268 V	1111 1111 1111	0111 1111 1111	0
0 V	1000 0000 0000	0000 0000 0000	0
−1 V	0000 0000 0000	1000 0000 0000	0
−1.000244 V	0000 0000 0000	1000 0000 0000	1

Users requiring offset binary encoding may simply invert the $\overline{\text{MSB}}$ pin. In the 44-pin surface mount packages, both MSB and $\overline{\text{MSB}}$ bits are provided.

The AD872 features a digital out-of-range (OTR) bit that goes high when the input exceeds positive full scale or falls below negative full scale. As Table III indicates, the output bits will be

set appropriately according to whether it is an out-of-range high condition or an out-of-range low condition.

The AD872's CMOS digital output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause glitches on the supplies and may affect S/(N+D) performance. Applications requiring the AD872 to drive large capacitive loads or large fanout may require additional decoupling capacitors on DRV_{DD} and DV_{DD}. In extreme cases, external buffers or latches could be used.

THREE-STATE OUTPUTS

The 44-pin surface mount AD872 offers three-state outputs. The digital outputs can be placed into a three-state mode by pulling the OUTPUT ENABLE (OEN) pin LOW. Note that this function is not intended to be used to pull the AD872 on and off a bus at 10 MHz. Rather, it is intended to allow the ADC to be pulled off the bus for evaluation or test modes. Also, to avoid corruption of the sampled analog signal during conversion (3 clock cycles), it is highly recommended that the AD872 be placed on the bus prior to the first sampling.

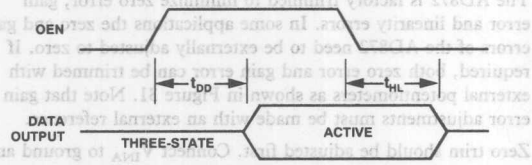


Figure 25. Three-State Output Timing Diagram

For timing budgetary purposes, the maximum access and float delay times for the AD872 are 200 ns.

CLOCK INPUT

The AD872 internal timing control uses the two edges of the clock input to generate a variety of internal timing signals. The optimal clock input should have a 50% duty cycle; however, sensitivity to duty cycle is significantly reduced for clock rates of less than 10 megasamples per second.

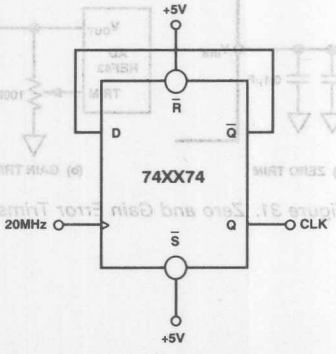


Figure 26. Divide-by-Two Clock Circuit

Due to the nature of on-chip compensation circuitry, the duty cycle should be maintained between 40% and 60% even for clock rates less than 10 Msps. One way to realize a 50% duty cycle clock is to divide down a clock of higher frequency, as shown in Figure 26.

In this case, a 20 MHz clock is divided by 2 to produce the 10 MHz clock input for the AD872. In this configuration, the duty cycle of the 20 MHz clock is irrelevant.

The input circuitry for the CLKIN pin is designed to accommodate both TTL and CMOS inputs. The quality of the logic input, particularly the rising edge, is critical in realizing the best possible jitter performance for the part: the faster the rising edge, the better the jitter performance.

As a result, careful selection of the logic family for the clock driver, as well as the fanout and capacitive load on the clock line, is important. Jitter-induced errors become more predominant at higher frequency, large amplitude inputs, where the input slew rate is greatest.

The AD872 is designed to support a sampling rate of 10 Msps; running at slightly faster clock rates may be possible, although at reduced performance levels. Conversely, some slight performance improvements might be realized by clocking the AD872 at slower clock rates. Figure 27 presents the SNR vs. clock frequency for a 1 MHz analog input.

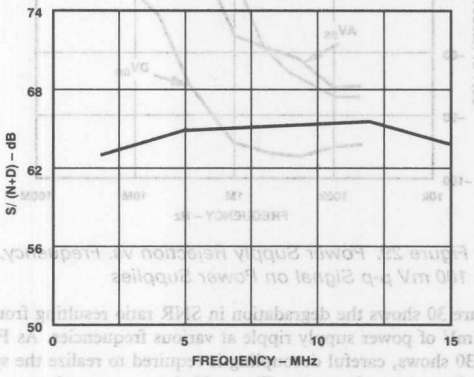


Figure 27. Typical S/(N+D) vs. Clock Frequency f_{IN} = 1 MHz, Full-Scale Input

The power dissipated by the correction logic and output buffers is largely proportional to the clock frequency; running at reduced clock rates provides a slight reduction in power consumption. Figure 28 illustrates this tradeoff.

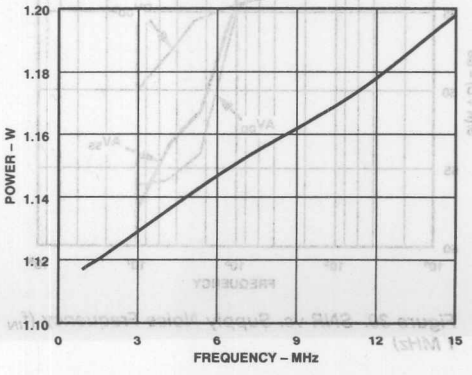


Figure 28. Typical Power Dissipation vs. Clock Frequency

ANALOG SUPPLIES AND GROUNDS

The AD872 features separate analog and digital supply and ground pins, helping to minimize digital corruption of sensitive analog signals. In general, AV_{SS} and AV_{DD}, the analog supplies, should be decoupled to AGND, the analog common, as close to the chip as physically possible. Care has been taken to minimize the signal dependence of the power supply currents; however, the analog supply currents will be proportional to the reference input. With REFIN at 2.5 V, the typical current into AV_{DD} is 78 mA, while the typical current out of AV_{SS} is 134 mA. Typically, 55 mA will flow into the AGND pin.

Careful design and the use of differential circuitry provide the AD872 with excellent rejection of power supply noise over a wide range of frequencies, as illustrated in Figure 29.

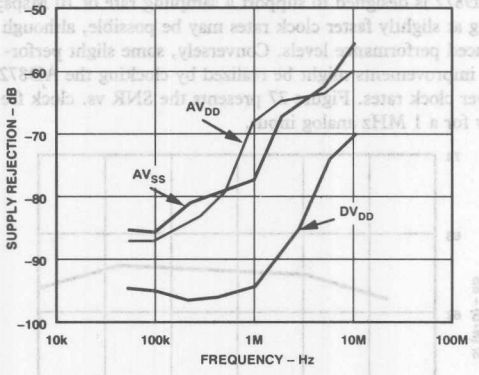


Figure 29. Power Supply Rejection vs. Frequency, 100 mV p-p Signal on Power Supplies

Figure 30 shows the degradation in SNR ratio resulting from 100 mV of power supply ripple at various frequencies. As Figure 30 shows, careful decoupling is required to realize the specified dynamic performance. Figure 35 demonstrates the recommended decoupling strategy for the supply pins. Note that in extremely noisy environments, a more elaborate supply filtering scheme may be necessary.

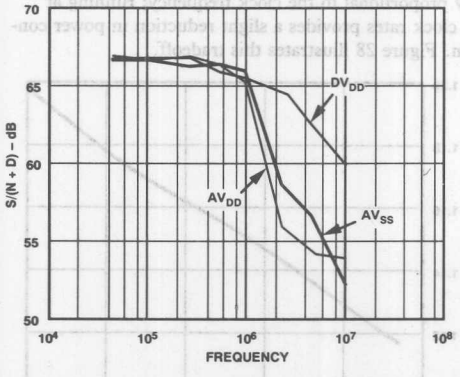


Figure 30. SNR vs. Supply Noise Frequency (f_{IN} = 1 MHz)

DIGITAL SUPPLIES AND GROUNDS

The digital activity on the AD872 chip falls into two general categories: CMOS correction logic, and CMOS output drivers. The internal correction logic draws relatively small surges of current, mainly during the clock transitions; in the 44-pin package, these currents flow through pins DGND and DV_{DD}. The output drivers draw large current impulses while the output bits are changing. The size and duration of these currents is a function of the load on the output bits: large capacitive loads are to be avoided. In the 44-pin package, the output drivers are supplied through dedicated pins DRGND and DRV_{DD}. Pin count constraints in the 28-pin packages require that the digital and driver supplies share package pins (although they have separate bond wires and on-chip routing). The decoupling shown in Figure 35 is appropriate for a reasonable capacitive load on the digital outputs (typically 20 pF on each pin). Applications involving greater digital loads should consider increasing the digital decoupling proportionately.

APPLICATIONS

OPTIONAL ZERO AND GAIN TRIM

The AD872 is factory trimmed to minimize zero error, gain error and linearity errors. In some applications the zero and gain errors of the AD872 need to be externally adjusted to zero. If required, both zero error and gain error can be trimmed with external potentiometers as shown in Figure 31. Note that gain error adjustments must be made with an external reference.

Zero trim should be adjusted first. Connect V_{INA} to ground and adjust the 10 kΩ potentiometer such that a nominal digital output code of 0000 0000 0000 (twos complement output) exists. Note that the zero trim should be decoupled and that the accuracy of the ±2.5 V reference signals will directly affect the offset.

Gain error may then be calibrated by adjusting the REF IN voltage. The REF IN voltage should be adjusted such that a +1 V input on V_{INA} results in the digital output code 01111 1111 1111 (twos complement output).

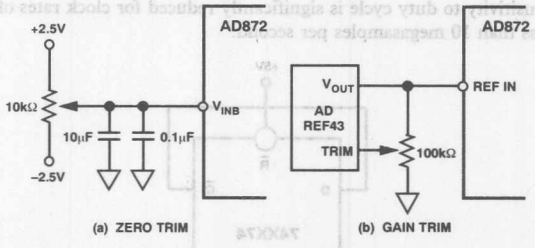


Figure 31. Zero and Gain Error Trims

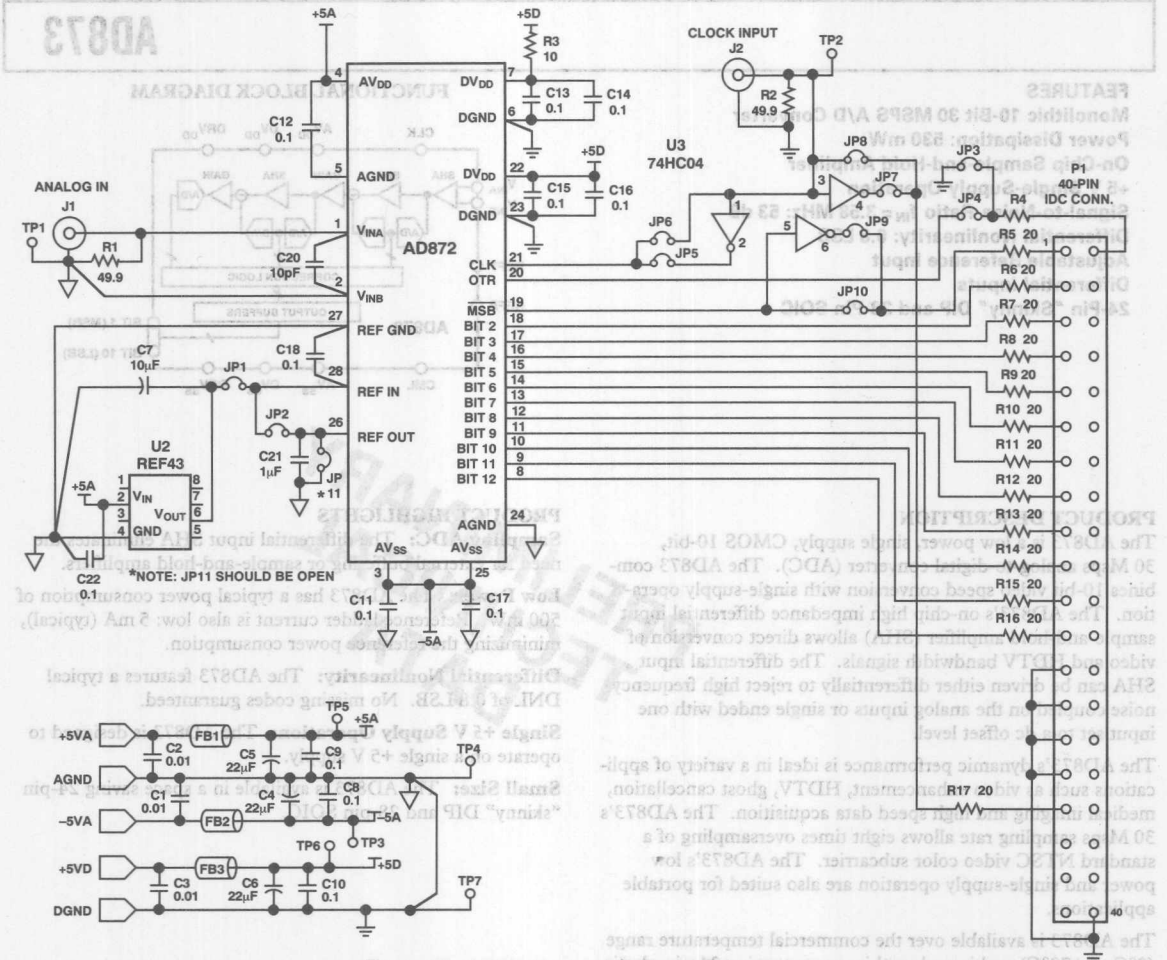
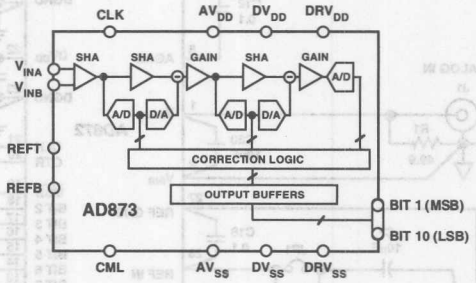


Figure 32. AD872 Evaluation Board Schematic

FEATURES

Monolithic 10-Bit 30 MSPS A/D Converter
Power Dissipation: 530 mW
On-Chip Sample-and-Hold Amplifier
+5 V Single-Supply Operation
Signal-to-Noise Ratio f_{IN} = 3.58 MHz: 53 dB
Differential Nonlinearity: 0.8 LSB
Adjustable Reference Input
Differential Inputs
24-Pin "Skinny" DIP and 28-Pin SOIC

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD873 is a low power, single supply, CMOS 10-bit, 30 Msps analog-to-digital converter (ADC). The AD873 combines 10-bit video speed conversion with single-supply operation. The AD873's on-chip high impedance differential input sample-and-hold amplifier (SHA) allows direct conversion of video and HDTV bandwidth signals. The differential input SHA can be driven either differentially to reject high frequency noise coupled on the analog inputs or single ended with one input set to a dc offset level.

The AD873's dynamic performance is ideal in a variety of applications such as video enhancement, HDTV, ghost cancellation, medical imaging and high speed data acquisition. The AD873's 30 Msps sampling rate allows eight times oversampling of a standard NTSC video color subcarrier. The AD873's low power and single-supply operation are also suited for portable applications.

The AD873 is available over the commercial temperature range (0°C to +70°C) and is packaged in a space saving 24-pin plastic "skinny" DIP (JN) and 28-pin SOIC (JR).

PRODUCT HIGHLIGHTS

Sampling ADC: The differential input SHA eliminates the need for external buffering or sample-and-hold amplifiers.

Low Power: The AD873 has a typical power consumption of 500 mW. Reference ladder current is also low: 5 mA (typical), minimizing the reference power consumption.

Differential Nonlinearity: The AD873 features a typical DNL of 0.8 LSB. No missing codes guaranteed.

Single +5 V Supply Operation: The AD873 is designed to operate on a single +5 V supply.

Small Size: The AD873 is available in a space saving 24-pin "skinny" DIP and 28-pin SOIC.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, f_{CLOCK} = 30 MHz, V_{REFT} = +3.0 V, V_{REFB} = +1.5 V unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	10			Bits
DC ACCURACY				
Linearity Error		±4		LSB
Differential Linearity Error		±0.8		LSB
Offset (+25°C)		2.2		% FSR
Gain Error (+25°C)		5		% FSR
ANALOG INPUT				
Input Range		3		V p-p
Input Current		30		µA
Input Capacitance		5		pF
REFERENCE INPUT				
Reference Input Resistance		300		Ω
Reference Input Voltage, Top		3.0		V
Reference Input Voltage, Bottom		1.5		V
CLOCK INPUT				
High Level Input Voltage	+3.5			V
Low Level Input Voltage			+1.0	V
High Level Input Current (CLK = DV_{DD})	–10		+10	µA
Low Level Input Current (CLK = 0 V)	–10		+10	µA
Input Capacitance		5		pF
LOGIC OUTPUTS				
High Level Output Voltage (I_{OH} = 0.5 mA)	+2.4			V
High Level Output Voltage (I_{OH} = 50 µA)	+4.5			V
Low Level Output Voltage (I_{OL} = 0.6 mA)			+0.4	V
Low Level Output Voltage (I_{OL} = 50 µA)			+0.5	V
POWER SUPPLIES				
Operating Voltages				
AV_{DD}	+4.75		+5.25	V
DV_{DD}	+4.75		+5.25	V
Operating Current				
IAV_{DD}		84	TBD	mA
IDV_{DD}		22	TBD	mA
POWER SUPPLY REJECTION		9		mV/V
POWER CONSUMPTION		530	TBD	mW
TEMPERATURE RANGE				
Specified	0		+70	°C

Specifications subject to change without notice. See Definition of Specifications for additional information.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AC SPECIFICATIONS

(AV_{DD} = +5 V, DV_{DD} = +5 V, f_{CLOCK} = 30 MHz, V_{REFT} = +3.0 V, V_{REFB} = +1.5 V, f_{IN} Amplitude = –0.9 dB, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Signal-to-Noise and Distortion (S/N+D) Ratio				
f_{IN} = 1.0 MHz		51		dB
f_{IN} = 10 MHz		46		dB
Signal-to-Noise Ratio (S/N)				
f_{IN} = 1.0 MHz		53		dB
f_{IN} = 10 MHz		51		dB
Total Harmonic Distortion (THD)				
f_{IN} = 1.0 MHz		–56	–TBD	dB
f_{IN} = 10 MHz		–47	–TBD	dB
Spurious Free Dynamic Range[1]		–56		dB
Full Power Bandwidth		200		MHz
Intermodulation Distortion (IMD)[2]				
Second Order Products			TBD	dB
Third Order Products			TBD	dB
Differential Phase		0.5		Degree
Differential Gain		1.5		%

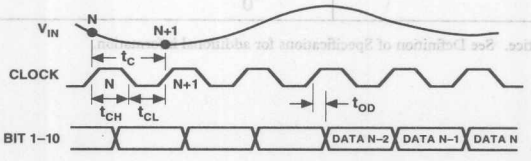
NOTES
[1]f_{IN} = 1 MHz.
[2]fa = TBD MHz, fb = TBD MHz.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

TIMING SPECIFICATIONS

	Symbol	Min	Typ	Max	Units
MAXIMUM CONVERSION RATE[1]		30			Msps
Clock Period	t_C	33			ns
Clock High	t_{CH}	16			ns
Clock Low	t_{CL}	16			ns
Output Delay[2]	t_{OD}	8			ns
Aperture Delay			TBD		ns
Aperture Jitter			TBD		ps
Pipeline Delay (Latency)			5		Clock Cycles
Output Rise Time[2]	t_R			5	ns
Output Fall Time[2]	t_F			5	ns

NOTES
[1]Conversion rate is operational down to xx kHz without degradation in specified performance.
[2]C_L = 25 pF.



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PIN DESCRIPTION

Symbol	Pin No. DIP	Pin No. SOIC	Type	Name and Function
AV_{SS}	6	6, 7	P	Analog Ground.
AV_{DD}	7	8 ,9	P	+5 V Analog Supply.
BIT 1 (MSB)	12	14	DO	Most Significant Bit.
BIT 2–BIT 9	13–16, 21–24	15–18, 25–28	DO	Data Bit 2 through Data Bit 9.
BIT 10 (LSB)	1	1	DO	Least Significant Bit.
CLK	11	13	DI	Clock Input.
DV_{SS}	20	23, 24	P	Digital Ground.
DV_{DD}	17	19, 20	P	+5 V Digital Supply.
DRV_{SS}	19	22	P	Digital Ground for the digital output drivers.
DRV_{DD}	18	21	P	+5 V Digital Supply for the digital output drivers.
REFT	9	11	AI	Reference Top Input.
REFB	8	10	AI	Reference Bottom Input.
V_{INA}	5	5	AI	(+) Analog Input Signal to the differential input SHA.
V_{INB}	4	4	AI	(–) Analog Input Signal to the differential input SHA.
CML	3	3	AO	Bypass pin for an internal bias point.
NC	2, 10	2, 12		No Connection. Connect to AV_{SS}.

TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD873JN	0°C to +70°C	24-Pin Plastic DIP	N-24
AD873JR	0°C to +70°C	28-Pin SOIC	R-28

*For outline information see Package Information section.

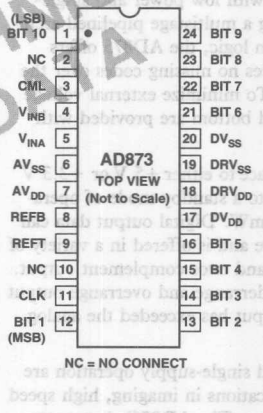
ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AV_{DD}, DV_{DD}	AV_{SS}, DV_{SS}, DRV_{SS}	–0.5	+6.5	Volts
AV_{SS}	DV_{SS}, DRV_{SS}	–1.0	+1.0	Volts
Analog Inputs	AV_{SS}	–0.5	+6.5	Volts
CLK	DV_{SS}	–0.5	+6.5	Volts
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

PIN CONFIGURATIONS

24-Pin DIP



NC = NO CONNECT

28-Pin SOIC

NC = NO CONNECT

PRELIMINARY TECHNICAL DATA

CAUTION

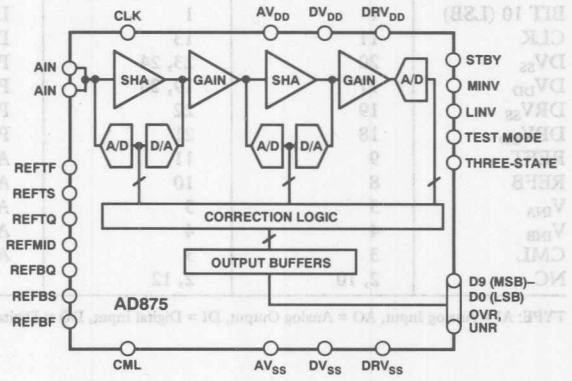
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD873 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

FEATURES

CMOS 10-Bit 15 MHz A/D Converter
Low Power Dissipation: 185 mW
+5 V Single-Supply Operation
Differential Nonlinearity: 0.4 LSB
Guaranteed No Missing Codes
Power-Down (Standby) Mode: <50 mW
Three-State Outputs
Digital I/Os Compatible with +5 V or +3.3 V Logic
Adjustable Reference Input
Small Size: 48-Pin Thin Quad Flatpack (TQFP)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD875 is a CMOS, low power 10-bit, 15 MHz analog-to-digital converter (ADC). The AD875 combines high speed 10-bit resolution and performance with low power and single-supply operation. By implementing a multistage pipelined architecture with output error correction logic, the AD875 offers accurate performance and guarantees no missing codes over the full operating temperature range. To minimize external voltage drops, the reference ladder top and bottom are provided with force and sense pins.

The AD875's digital I/Os can interface to either +5 V or +3.3 V logic. The AD875 can be placed into a standby mode of operation reducing the power below 50 mW. Digital output data can be placed in a high impedance state and is offered in a variety of formats, including straight binary and twos complement output. The AD875 also provides both underrange and overrange output bits, indicating when the analog input has exceeded the analog input range.

The AD875's speed, resolution and single-supply operation are ideally suited for a variety of applications in imaging, high speed data acquisition and communications. The AD875's low power and single supply operation are required for high speed portable applications. Its speed and resolution are ideally suited for charge coupled device (CCD) input systems such as color scanners, digital copiers, electronic still cameras and camcorders.

The AD875 is packaged in a space saving 48-pin thin quad flatpack (TQFP) and is specified over the commercial (0°C to +70°C) temperature range.

PRODUCT HIGHLIGHTS

Low Power—The AD875 at 185 mW consumes a fraction of the power of presently available 10-bit, video-speed converters. Power-down mode and single-supply operation further enhance its desirability in low power, battery operated applications such as electronic still cameras, camcorders and communication systems.

Superior Differential Nonlinearity Performance—The AD875's typical DNL performance is 0.4 LSB and a maximum of 0.8 LSBs for the 0 to 255 code range (ideal for imaging systems). No missing codes are guaranteed.

Very Small Package—The AD875 is available in a 48-pin surface mount, thin quad flatpack. The TQFP package is ideal for very tight, low headroom designs. The AD875 is available in tape-and-reel.

Digital I/O Functionality—The AD875 offers several digital features which allow output data formatting, fixed output test pattern generation to facilitate in-circuit testing, three-state output control and over/underrange indicators.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

DC SPECIFICATIONS

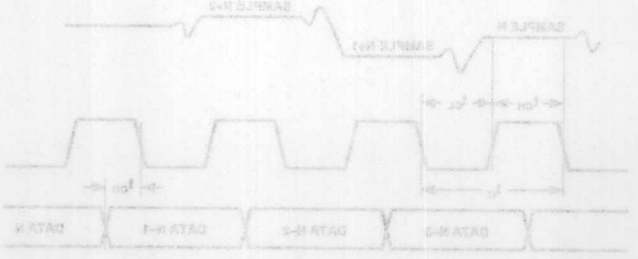
(T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, DRV_{DD} = +3.3 V, V_{REFTF} = +4.0 V, V_{REFBF} = +2.0 V, f_{CLOCK} = 15 MHz, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	10			Bits
DC ACCURACY				
Integral Nonlinearity (INL)		±1.5	±2.5	LSB
Differential Nonlinearity (DNL)				
Codes 0 to 255		±0.4	±0.8	LSB
Codes 256 to 1023		±0.4	±1	LSB
No Missing Codes		GUARANTEED		
Offset		0.1		%FSR
Gain		0.2		%FSR
ANALOG INPUT				
Input Range	1.8	2	2.2	V p-p
Input Resistance		100		kΩ
Input Current		10		μA
Input Capacitance		5		pF
REFERENCE INPUT				
Reference Top Voltage	3.6	4.0	4.1	V
Reference Bottom Voltage	1.6	2.0	2.1	V
Reference Input Resistance	250	400		Ω
Reference Input Current		5	8	mA
Force-Sense Offset				
Top		25		mV
Bottom		25		mV
POWER SUPPLIES				
Operating Voltages				
AV_{DD}	+4.5		+5.25	Volts
DV_{DD}	+4.5		+5.25	Volts
DRV_{DD}	+3.0		+5.25	Volts
Operating Current				
IAV_{DD}		19	34	mA
IDV_{DD}		17	25	mA
$IDRV_{DD}$[1]		1	5	mA
POWER CONSUMPTION		185	235	mW
TEMPERATURE RANGE				
Operating	0		+70	°C

NOTES

[1] C_L = 20 pF

Specifications subject to change without notice. See Definition of Specifications for additional information.



DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, DRV_{DD} = +3.3 V, V_{REFTF} = +4.0 V, V_{REFBF} = +2.0 V, f_{CLOCK} = 15 MHz, C_L = 20 pF unless otherwise noted)

Parameter	Symbol	DRV_{DD}	Min	Typ	Max	Units
LOGIC INPUT						
High Level Input Voltage	V_{IH}	3.0	2.4			V
		4.75	3.8			V
		5.25	4.2			V
Low Level Input Voltage	V_{IL}	3.0			0.6	V
		4.75			0.95	V
		5.25			1.05	V
High Level Input Current	I_{IH}	4.75	−10		+10	μA
Low Level Input Current	I_{IL}	4.75	−50		+50	μA
Low Level Input Current (CLK Only)	I_{IL}	4.75	−10		+10	μA
Input Capacitance	C_{IN}			5		pF
LOGIC OUTPUTS						
High Level Output Voltage	V_{OH}					
(I_{OH} = 50 μA)		3.0	2.4			V
		4.75	3.8			V
(I_{OH} = 0.5 mA)		4.75	2.4			V
Low Level Output Voltage	V_{OL}					
(I_{OL} = 50 μA)		3.6			0.7	V
		5.25			1.05	V
(I_{OL} = 0.6 mA)		5.25			0.4	V
Output Capacitance	C_{OUT}			5		pF
Output Leakage Current	I_{OZ}		−10		+10	μA

Specifications subject to change without notice.

TIMING SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, DRV_{DD} = +3.3 V, V_{REFTF} = +4.0 V, V_{REFBF} = +2.0 V, f_{CLOCK} = 15 MHz, C_L = 20 pF unless otherwise noted)

	Symbol	Min	Typ	Max	Units
Maximum Conversion Rate[1]		15			MHz
Clock Period	t_C	66			ns
Clock High	t_{CH}	30	33		ns
Clock Low	t_{CL}	30	33		ns
Output Delay[2]	t_{OD}	12	15		ns
Pipeline Delay (Latency)				3	Clock Cycles
Sampling Delay 1[3]	t_{S1}		2.5		ns
Sampling Delay 2[3]	t_{S2}		2.5		ns
External Settling Requirement[3]	V_{SE}			±16	mV

NOTES
[1]Conversion rate is operational down to 10 kHz without degradation in specified performance.
[2]C_L = 20 pF.
[3]See the section entitled "Driving the Analog Input."
Specifications subject to change without notice.

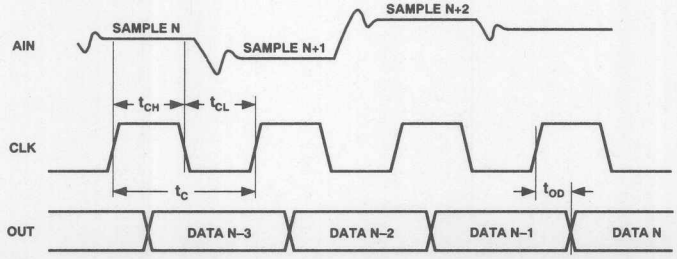
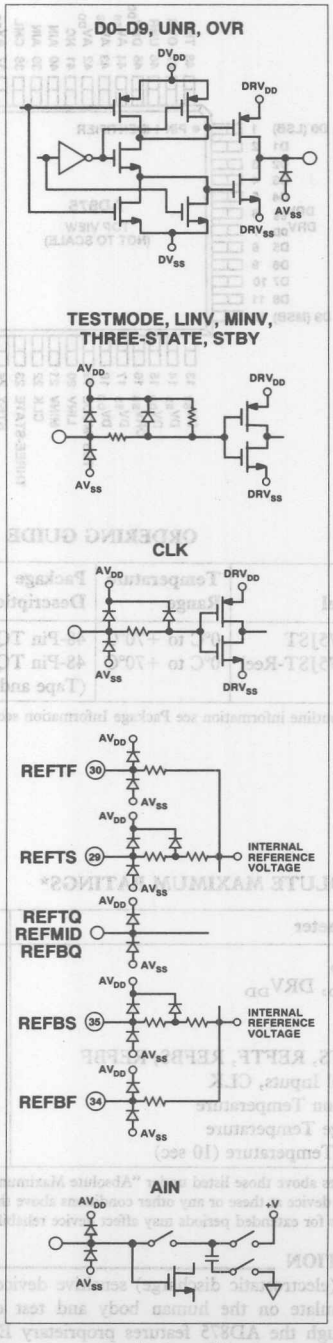


Figure 1. AD875 Timing Diagram

PIN DESCRIPTION

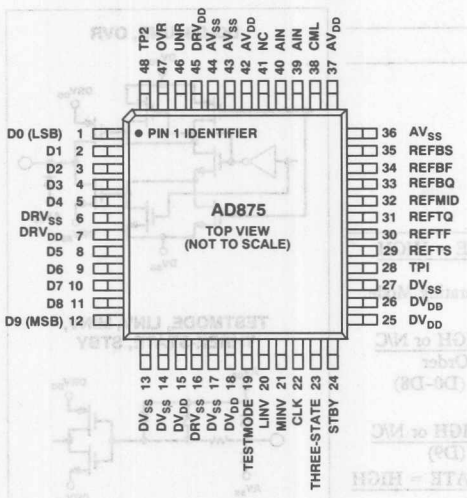
Symbol	Pin No.	Type	Name and Function
D0 (LSB)	1	DO	Least Significant Bit
D1–D4	2–5	DO	Data Bits 1 Through 4
D5–D8	8–11	DO	Data Bits 5 Through 8
D9 (MSB)	12	DO	Most Significant Bit
UNR	46	DO	Underrange Output
OVR	47	DO	Overrange Output
TESTMODE	19	DI	TESTMODE = LOW: 1 0 1 0 . . . Pattern On D0–D9; TESTMODE = HIGH or N/C: Normal Operating Mode
LINV	20	DI	Invert the Lower Order Output Bits. LINV = LOW: No Inversion; LINV = HIGH or N/C: Invert Low Order Output Bits (D0–D8)
MINV	21	DI	Invert the Most Significant Bit. MINV = LOW: No Inversion; MINV = HIGH or N/C: Invert MSB (D9)
THREE-STATE	23	DI	THREE-STATE = LOW: Normal Operating Mode; THREE-STATE = HIGH or N/C: High Impedance Outputs
STBY	24	DI	STBY = LOW: Normal Operating Mode; STBY = HIGH or N/C: Standby Mode
CLK	22	DI	Clock Input
CML	38	AO	Bypass Pin for an Internal Bias Point. A 10 µF capacitor in parallel with a 0.1 µF capacitor must be connected to CML. CML is not to be used to drive external circuitry.
REFTS	29	AI	Reference Top Sense
REFTF	30	AI	Reference Top Force
REFTQ	31	AI	Reference Top Quarter Point (Bypass)
REFMID	32	AI	Reference Midpoint (Bypass)
REFBQ	33	AI	Reference Bottom Quarter Point (Bypass)
REFBF	34	AI	Reference Bottom Force
REFBS	35	AI	Reference Bottom Sense
AIN	39, 40	AI	Analog Input
AV_{DD}	37, 42	P	+5 V Analog Supply
AV_{SS}	36, 43, 44	P	Analog Ground
DV_{DD}	15, 18, 25, 26	P	+5 V Digital Supply
DV_{SS}	13, 14, 17, 27	P	Digital Ground
DRV_{DD}	7, 45	P	+3.3 V/+5 V Digital Supply. Supply for Digital Input and Output Buffers
DRV_{SS}	6, 16	P	+3.3 V/+5 V Digital Ground. Ground for Digital Input and Output Buffers
TP1	28	P	Connect to AV_{SS} (Analog Ground)
TP2	48	P	Connect to DV_{SS} (Digital Ground)
N/C	41		No Connect

TYPE: AI = Analog Input; AO = Analog Output; DI = Digital Input;
DO = Digital Output;
P = Power



Equivalent Circuits

PIN CONFIGURATION



TYPICAL CHARACTERISTIC CURVES

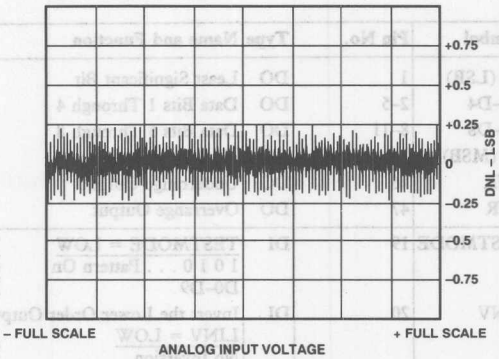


Figure 2. Typical DNL

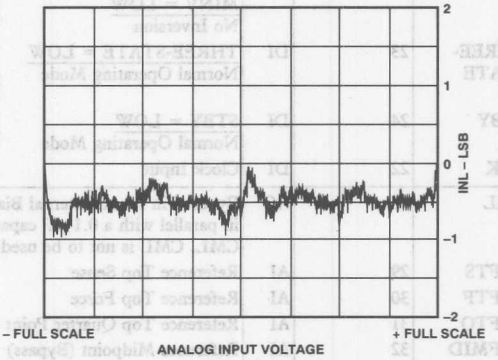


Figure 3. Typical INL

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD875JST	0°C to +70°C	48-Pin TQFP	ST-48
AD875JST-Reel	0°C to +70°C	48-Pin TQFP (Tape and Reel 13″)	

*For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AV_{DD}	AV_{SS}	−0.5	+6.5	Volts
DV_{DD}, DRV_{DD}	DV_{SS}, DRV_{SS}	−0.5	+6.5	Volts
AV_{SS}	DV_{SS}, DRV_{SS}	−0.5	+0.5	Volts
AIN	AV_{SS}	−0.5	+6.5	Volts
REFTS, REFTF, REFBS, REFBF	AV_{SS}	−0.5	+6.5	Volts
Digital Inputs, CLK	DV_{SS}, DRV_{SS}	−0.5	+6.5	Volts
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD875 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DEFINITIONS OF SPECIFICATIONS

Integral Nonlinearity (INL)
Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution for which no missing codes (NMC) are guaranteed.

Offset Error
The first transition should occur at a level 1/2 LSB above "zero." Offset is defined as the deviation of the actual first code transition from that point.

Gain Error
The first code transition should occur for an analog value 1/2 LSB above nominal negative full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

Pipeline Delay (Latency)
The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

Reference Force/Sense Offset
Resistance between the reference input and comparator input tap points causes offset errors. These errors can be nulled out by using the force-sense connection as shown in the Reference Input section.

THEORY OF OPERATION

The AD875 uses a pipelined multistage architecture to achieve high sample rate with low power. The multistage approach distributes the conversion over several smaller A/D sub-blocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage. As a consequence of the distributed conversion, the AD875 requires only a small fraction of the 1023 comparators that would be required in a more traditional 10-bit flash type A/D. A sample-and-hold (SHA) function within each of the stages permits the first stage to operate on a new sample of the input while the second and third stages operate on the two preceding samples. This "assembly line" operation on multiple samples, known as pipelining, allows higher throughput at the cost of some delay, referred to as latency. (See the output timing diagram.)

The detailed operation is as follows: the first stage makes a 4-bit estimate of the analog input voltage by means of the first stage A/D sub-block. The first stage estimate is converted to analog form by the first stage D/A and subtracted from the original input signal. The remainder, or residue, is the difference between the first stage estimate and the actual analog input. Next, the residue is amplified and passed to the second stage where another A/D sub-block makes a 4-bit estimate of its value. Again the analog version of the estimate is subtracted from the signal, and an even finer residue is generated. Finally, the A/D sub-block in the last stage measures the value of this second stage residue.

The A/D sub-blocks within each stage are actually 4-bit flash converters. Ideally 3 bits in the second and third stages would be sufficient for a 10-bit A/D. The additional bits allow for digital correction of errors in preceding stages, reducing the tolerances on the sub-block components and making a more robust A/D. The reference ladders for all three of these flash sub-blocks are wired in parallel and connected to the reference pins of the AD875.

Inside the AD875 all signals are processed differentially. This not only enhances the internal dynamic range of the components but provides a high level of noise immunity in a digital environment.

APPLYING THE AD875

DRIVING THE ANALOG INPUT

The high input resistance and low input capacitance features of the AD875 simplify the current and settling time demands placed on input drive circuitry. Figure 4 shows the equivalent input circuit of the AD875.

The full-scale input range is set by the voltage span, REFTF–REFBF (see "Driving the Reference" section). The recommended span should nominally be 2 V peak-to-peak. This span must remain bounded by the minimum and maximum input range (specified in the Analog Input section under DC Specifications). Some example input ranges are given in Table I.

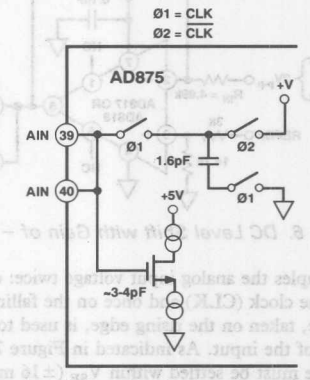


Figure 4. AD875 Equivalent Input Structure

Table I. Input Range Examples

–Full Scale = REFBF (V)	+Full Scale = REFTF (V)	Input Span (V)
+1.6	+3.6	+2.0
+2.0	+4.0	+2.0
+2.1	+4.1	+2.0

While the input impedance of the AD875 is quite high, the switched-capacitor input structure results in a small dynamic input current. In order to prevent gain variations as a result of the input current, maintaining a source impedance of less than or equal to 75 Ω is suggested (Figure 5). In general, a low drive impedance is suggested to minimize noise coupled on the AIN inputs.

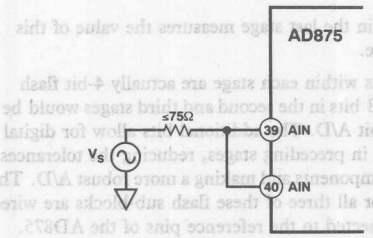


Figure 5. Simple AD875 Drive Requirements

For systems which must level shift a ground-referenced signal in order to comply with the input requirements of the AD875, a circuit like Figure 6 is recommended. The suggested op amp, an AD817 or AD818, is configured in inverting mode, where the ac gain of the input signal is −1. The amount of dc-level shifting is controlled by the dc voltage at the noninverting input of the op amp. The REFBF signal is attenuated by a resistive voltage divider and then multiplied by 2. In the case where REFBF = 1.6 V, the dc output level will be 2.6 V. The AD817 is a low cost, fast settling, single-supply op amp with a 29 MHz unity gain bandwidth. The AD818 is similar to the AD817 but has a 50 MHz unity gain bandwidth.

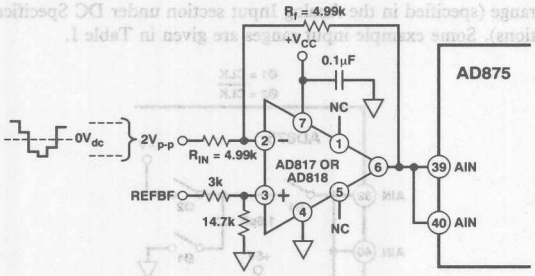


Figure 6. DC Level Shift with Gain of −1×

The AD875 samples the analog input voltage twice: once on the rising edge of the clock (CLK) and once on the falling edge. The first sample, taken on the rising edge, is used to perform a coarse estimate of the input. As indicated in Figure 7, the analog input voltage must be settled within V_{SE} (±16 mV) of its final value at this time and must remain within V_{SE} until the second sample has been taken. The second sample, taken on the falling edge of the clock, will determine the exact value digitized and should be accurate to within 10 bits (0.1%). Note that the actual sample points are delayed by t_{S1} and t_{S2}.

For applications where step input signals are expected (i.e., CCD or multiplexed outputs), the settling time of the input drive circuitry should be examined carefully. In most cases, the settling time requirements placed on the input amplifier are easily met by the AD817 or AD818. For higher speed operation, it may be necessary to use faster op amps such as the AD810 or AD811.

As a result of the AD875's settling requirements, there is a maximum slew rate limitation placed on the analog input signal. For applications using CCDs and other sampled analog systems, the AD875 can be used directly. However, for continuous signal applications, Figure 7 implies a maximum slew rate limitation on the analog input:

$$Slew\ Rate\ of\ Analog\ Input\ (maximum) = \frac{16\ mV}{t_{CH}}\ (V/sec)$$

where t_{CH} is the "high" period of the sample clock in seconds, or one-half the full period when the clock is run with 50% duty cycle. For example, at 15 MHz clock rate, the maximum slew rate is about 0.48 V/μs. This corresponds to a maximum analog input frequency of 76 kHz when a full-scale (2 V peak-to-peak) sine wave is used. For input signals with higher slew rates, a sample-and-hold amplifier must be used for accurate digitization.

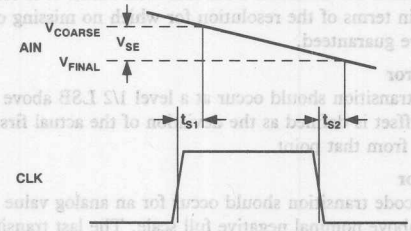


Figure 7. Analog Input Settling Requirement

REFERENCE INPUT

Driving the Reference Terminals

The AD875 requires an external reference on pins REFTF and REFBF. Reference sense pins REFTS and REFBS are also provided for Kelvin connections to minimize voltage drops due to external and internal wiring resistances. A resistor ladder nominally 400 Ω is connected internally between pins REFTF and REFBF.

The voltage drop across the internal resistor ladder determines the input span of the AD875. The driving voltages required at the REFTF and REFBF pins are nominally +4 V and +2 V respectively resulting in a 2 V input span. In order to maintain the requisite 2 V drop across the internal ladder, the external reference must be capable of typically providing 5 mA of dc current.

Transient current flows in and out of the REFTF and REFBF pins. Therefore, a low ac impedance is required at these terminals for proper operation. Bypassing each pin with suitable capacitive decoupling should effectively attenuate any transients. See the AD875 Evaluation Board Schematic for recommended values. Mid (REFMID) and quarter (REFTQ, REFBQ) ladder tap points are also available for additional decoupling if required. It is important to note that these tap points cannot be used to correct integral linearity as is sometimes done in a typical flash converters.

There are several reference configurations suitable for the AD875 depending on the application, desired performance and cost trade-offs. The simplest configuration, shown in Figure 8, utilizes a resistor string to generate the reference voltages from the converter's analog power supply. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor will provide adequate decoupling for both the REFTF and REFBF pins. The 0.1 μF capacitors should be physically located within 1cm of REFTF and REFBF. A 10 μF capacitor connected between REFTF and REFBF is also recommended for optimum performance. This reference configuration provides the lowest cost

solution but has several disadvantages including poor dc power supply rejection and poor accuracy due to the variability of the internal and external resistor values.

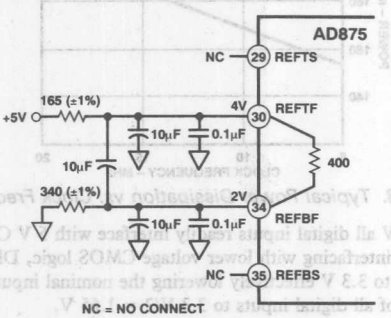


Figure 8. Low Cost Reference Circuit

A higher performance solution employs a voltage regulator to improve dc power supply rejection and absolute accuracy. Figure 9 shows a LM317 adjustable regulator configured to generate a 1.6 V output for REFBF. This output is also used to generate the 3.6 V REFTF signal by multiplying the REFBF signal by 2.25. Note that the AD817 op amp used to multiply REFBF has been compensated to ensure stability while driving the large capacitive load. The accuracy of this solution is limited by the external resistors and the initial accuracy of the reference.

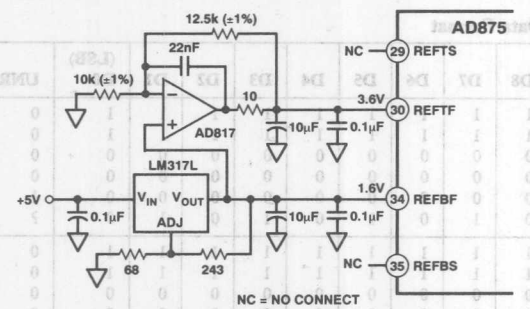


Figure 9. Reference Circuit with Good PSRR

For optimal performance, a force sense or Kelvin configuration can be used as shown in Figure 10. This circuit uses a high-accuracy reference (AD589) and a dual op amp (OP-295) to maintain accuracy and minimize voltage drops which are generated in the wire connections to the REFTF and REFBF inputs. The output of the AD589 is increased to 1.6 V and 3.6 V at the outputs of the op amps as required. Both op amps are compensated to maintain stability while driving the decoupling capacitors required at the REFTF and REFBF pins.

These outputs, being connected in a feedback loop, tend to cancel any errors caused by the voltage drops in the wires. Note that if the REFTS and REFBS are not used in a force sense configuration, they should be left unconnected and should not be connected to REFTF and REFBF.

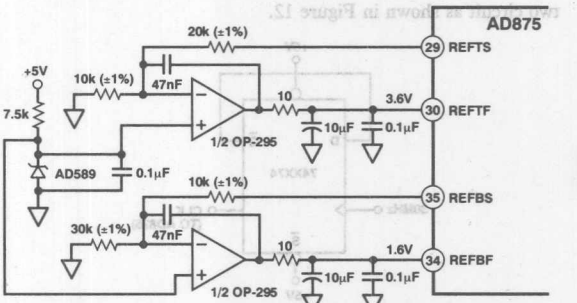


Figure 10. High Performance Reference Circuit Using Kelvin Connections

Like any high resolution converter, the layout and decoupling of the reference is critical. The actual voltage digitized by the AD875 is relative to the reference voltages. In Figure 11, for example, the reference returns and the bypass capacitors are connected to the shield of the incoming analog signal. Disturbances in the ground of the analog input, which will be common-mode to the REFTF, REFBF, and AIN pins because of the common ground, are effectively removed by the AD875's high common-mode rejection.

High frequency noise sources, V_{N1} and V_{N2}, are shunted to ground by decoupling capacitors. Any voltage drops between the analog input ground and the reference bypassing points will be treated as input signals by the converter via the reference inputs. Consequently, the reference decoupling capacitors should be connected to the same analog ground point used to define the analog input voltage. (For further suggestions, see the "Grounding and Layout Rules" section of the data sheet.)

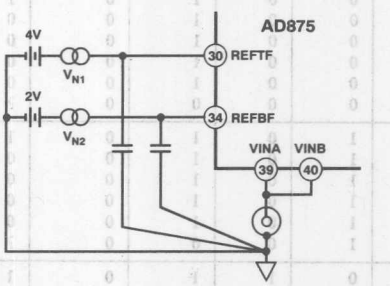


Figure 11. Recommended Bypassing for the Reference Inputs

CLOCK INPUT

The AD875 clock input is buffered internally with an inverter powered from the DRV_{DD} pin. This feature allows the AD875 to accommodate either +5 V or +3.3 V CMOS logic input signal swings with the input threshold for the CLK pin nominally at $DRV_{DD}/2$.

The AD875's pipelined architecture operates on both rising and falling edges of the input clock. To minimize duty cycle variations the recommended logic family to drive the clock input is high speed CMOS (HC/HCT) logic. HCMOS logic provides both symmetrical voltage threshold levels and sufficient rise and fall times to support 15 MHz operation. The AD875's minimum

clock half cycle may necessitate the use of an external divide-by-two circuit as shown in Figure 12.

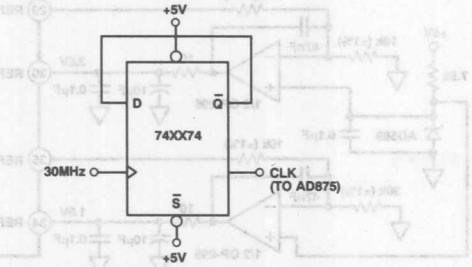


Figure 12. Divide-By-Two Clock Input Circuit

The AD875 is designed to support a conversion rate of 15 MHz; running the part at slightly faster clock rates may be possible, although at reduced performance levels. Conversely, some slight performance improvements might be realized by clocking the AD875 at slower clock rates.

The power dissipated by the correction logic and output buffers is largely proportional to the clock frequency; running at reduced clock rates provides a reduction in power consumption. Figure 13 illustrates this trade-off.

DIGITAL INPUTS AND OUTPUTS

Each of the AD875's digital control inputs, MINV, LINV, TEST MODE, THREE-STATE, and STBY is buffered with an inverter powered from the DRV_{DD} supply pins. With DRV_{DD} set to +5 V all digital inputs readily interface with 5 V CMOS logic. For interfacing with lower voltage CMOS logic, DRV_{DD} can be set to 3.3 V effectively lowering the nominal input threshold of all digital inputs to 3.3 V/2 = 1.65 V.

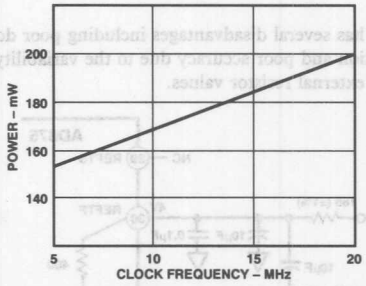


Figure 13. Typical Power Dissipation vs. Clock Frequency

The AD875 provides several convenient digital input pins for controlling the converter output format. By utilizing digital input pins MINV and LINV, three digital output formats are possible: binary, twos complement, and ones complement.

Another element of digital functionality is provided with the TEST MODE pin. To facilitate in-circuit testing of the digital portion of your application, a fixed digital pattern controlled by a digital input is available. For TEST MODE = LOW, an alternating 1010101010 pattern is established. This pattern is further manipulated when used in conjunction with the LINV and MINV pins (see Output Data Format, Table II below).

Table II. Output Data Format

Approx AIN (V)	MINV	LINV	TEST MODE	THREE-STATE	OVR	(MSB) D9	D8	D7	D6	D5	D4	D3	D2	D1	(LSB) D0	UNR
>4	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0
4	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0
3	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
<2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
X	0	0	0	0	?	1	0	1	0	1	0	1	0	1	0	?
>4	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	0
4	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0
3	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
<2	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1
X	1	0	0	0	?	0	0	1	0	1	0	1	0	1	0	?
>4	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0
4	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
3	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	0
2	0	1	1	0	0	0	1	1	1	1	1	1	1	1	1	0
<2	0	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
X	0	1	0	0	?	1	1	0	1	0	1	0	1	0	1	?
>4	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
4	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
3	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	0
2	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	0
<2	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
X	1	1	0	0	?	0	1	0	1	0	1	0	1	0	1	?
>4	X	X	X	0	1	?	?	?	?	?	?	?	?	?	?	0
2<AIN<4	X	X	X	0	0	?	?	?	?	?	?	?	?	?	?	0
<2	X	X	X	0	0	?	?	?	?	?	?	?	?	?	?	1
X	X	X	X	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Z = High Impedance; X = Don't Care; ? = Determined By AIN.

Also, a sleep mode feature is provided such that for STBY = HIGH and the clock disabled, the static power of the AD875 will drop below 50 mW. The AD875 reaches rated accuracy 4 clock cycles after STBY is brought LOW and the clock is started.

DIGITAL OUTPUTS

Each of the on-chip buffers for the AD875 output bits (D0–D9, OVR, UNR) is powered from the DRV_{DD} supply pins, separate from AV_{DD} or DV_{DD}. The output drivers are sized to handle a variety of logic families while minimizing the amount of glitch energy generated. In all cases, a fan-out of one is recommended to keep the capacitive load on the output data bits below the specified 20 pF level.

For DRV_{DD} = 5 V, the AD875 output signal swing is compatible with both high speed CMOS and TTL logic families. For TTL, the AD875 on-chip, output drivers were designed to support several of the high speed TTL families (F, AS, S). For applications where the clock rate is below 15 MHz, other TTL families may be appropriate. For interfacing with lower voltage CMOS logic, the AD875 sustains 15 MHz operation with DRV_{DD} = 3.3 V. In all cases, check your logic family data sheets for compatibility with the AD875 Digital Specification table.

THREE-STATE OUTPUTS

The digital outputs of the AD875 can be placed in a high impedance state by setting the THREE-STATE pin to HIGH. This feature is provided to facilitate in-circuit testing or evaluation. Note that this function is not intended for enabling/disabling the ADC outputs from a bus at 15 MHz. Also, to avoid corruption of the sampled analog signal during conversion (three clock cycles), it is highly recommended that the AD875 outputs be enabled on the bus prior to the first sampling. For the purpose of budgetary timing, the maximum access and float delay times (t_{DD}, t_{HL} shown in Figure 14) for the AD875 are 150 ns.

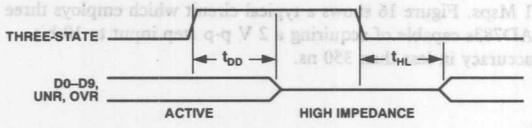


Figure 14. High Impedance Output Timing Diagram

OUT OF RANGE

As Table II indicates, an Underrange (UNR) or Overrange (OVR) condition exists when the analog input voltage is beyond the input range (nominally +2 V to +4 V) of the converter. UNR (Pin 46) is set LOW when the analog input voltage is within the analog input range. UNR is set HIGH (after accounting for pipeline latency) and will remain HIGH when the analog input voltage is less than the input range by 1/2 LSB from the center of the negative full-scale output code. OVR (Pin 47) is set LOW when the analog input voltage is within the analog input range. OVR is set HIGH (after accounting for pipeline latency) and will remain HIGH when the analog input voltage is greater than the input range by 1/2 LSB from the center of the positive full-scale output code.

GROUNDING AND LAYOUT RULES

As is the case for any high performance device, proper grounding and layout techniques are essential in achieving optimal performance. The analog and digital grounds on the AD875 have been separated to optimize the management of return currents in a system. It is recommended that a 4-layer printed circuit board (PCB) which employs a ground plane and power planes be used with the AD875. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout which prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with the input signal traces and should be routed away from the input circuitry.

Separate analog and digital grounds should be joined together directly under the AD875. A solid ground plane under the AD875 is also acceptable if care is taken in the management of the power and ground return currents. A general "rule-of-thumb" for mixed signal layouts dictates that the return currents from digital circuitry should not pass through critical analog circuitry.

POWER SUPPLY DECOUPLING

The analog and digital supplies of the AD875 have been separated to prevent the typically large transients associated with digital circuitry from coupling into the analog supply (AV_{DD}).

The digital supplies have also been separated into DRV_{DD} and DV_{DD}. The DRV_{DD} pins provide power for the digital I/O's of the AD875 and are likely to contain high energy transients. Each power supply pin should be decoupled with a 0.1 μF capacitor located as close to the pin as possible. For optimal performance, surface-mount capacitors are recommended. The inductance associated with the leads of through-hole ceramic capacitors typically render them ineffective at higher frequencies. A *complete* system will also incorporate tantalum capacitors in the 10–100 μF range to decouple low frequency noise and ferrite beads to limit high frequency noise.

APPLICATIONS

IMAGING SYSTEM OVERVIEW

While the specifics of a particular imaging system will vary, most architectures will employ some or all of the building blocks shown in Figure 15. The image sensor, often a charged-coupled device (CCD), transforms light to electrical output. The resultant pixel stream is conditioned by a clamp/sample-hold circuit which is sometimes referred to as a correlated double sampler (CDS). A gain block sets signal levels which maximize the utilization of the dynamic range of the A/D converter. DC restoration is often used to remove any static dc errors which may accumulate over time and temperature. The digitized signal is then processed by the application specific digital signal processor.

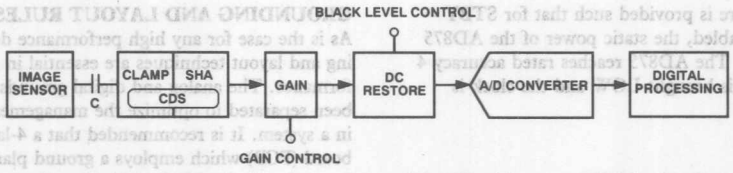


Figure 15. Typical Imaging System Block Diagram

For optimum performance the CDS is tailored to the sensor output characteristics. When used in conjunction with a CCD, the CDS acts to remove low frequency signal variations, kT/C noise, and other noise components, all of which are artifacts generated by the CCD. The output signal from the CCD is characterized by a series of pixels, each containing both a reset level and the actual video data. Aside from the various noise components, the video data is essentially a stream of stepped dc signals. This pixel stream from the CCD is then ac-coupled through a capacitor to a switch (contained within the CDS block).

This switch, in turn, is connected to a clamp reference voltage. The switch is closed during the reset portion of each pixel. As a result, the difference between the reset level of each pixel and the clamp reference voltage is stored on the coupling capacitor. When the switch is opened, the dc voltage stored on the coupling capacitor sets the dc level for the pixel stream. The video portion of each pixel is then sampled and held using traditional sample/hold (SHA) architectures. Since the CCD noise sources are correlated between the reset and video portions of the pixel stream, and the output of the SHA represents the difference between these two levels, the noise is effectively eliminated.

The output of the CDS will generally require some form of gain control in order to maximize the full-scale input range of the A/D converter. In some applications, a fixed gain may be adequate while in many applications such as camcorders, variable gain control is used to automatically account for variations in scene brightness. Gain control can be achieved using analog or digital techniques and often times must be able to respond at a rate equivalent to the pixel rate. Gilbert multiplier cells and multiplying D/As are two common circuits used for the gain block.

The dc restore block acts to set the final dc level of the signal before digitization by the A/D converter. A fixed voltage level (equivalent to the black level or negative full scale) generated by the CCD is sampled by the dc restoration circuit usually at the beginning or end of a "scan line." Any difference between the sampled black level and the desired negative full scale is removed either by a servo loop or corrected digitally. To maximize the use of the A/D's input range, the error must be removed prior to the A/D. This is generally accomplished by a high dc-gain feedback path which servos any error detected at the output. The dc restoration effectively removes dc level shifts which may occur as a result of long-term parameter shifts such as component drift and temperature variations.

The main criterion for choosing the A/D converter is generally based on resolution and speed. Resolution affects the signals-to-noise ratio of the system, dictates the maximum digital dynamic range of the image, and is a consideration for round-off errors produced in the digital signal processing. The speed of the A/D converter is related to the number of pixel elements and the pixel output rate of the particular image sensor. Multichannel systems may multiplex more than one pixel stream into a single A/D, thus requiring faster conversion rates. Similarly, area CCDs (CCDs which capture video information in two dimensions) operate at higher rates than linear (one dimensional) CCDs.

MULTICHANNEL IMAGE ACQUISITION SYSTEM

The AD875's fast conversion rate combined with the AD783 sample/hold amplifiers (SHAs) and the AD9300 high speed multiplexer can be used to construct an analog front-end capable of acquiring and digitizing three or more analog signals at a rate of 1 Msps. Figure 16 shows a typical circuit which employs three AD783s capable of acquiring a 2 V p-p step input to 10-bit accuracy in less than 350 ns.

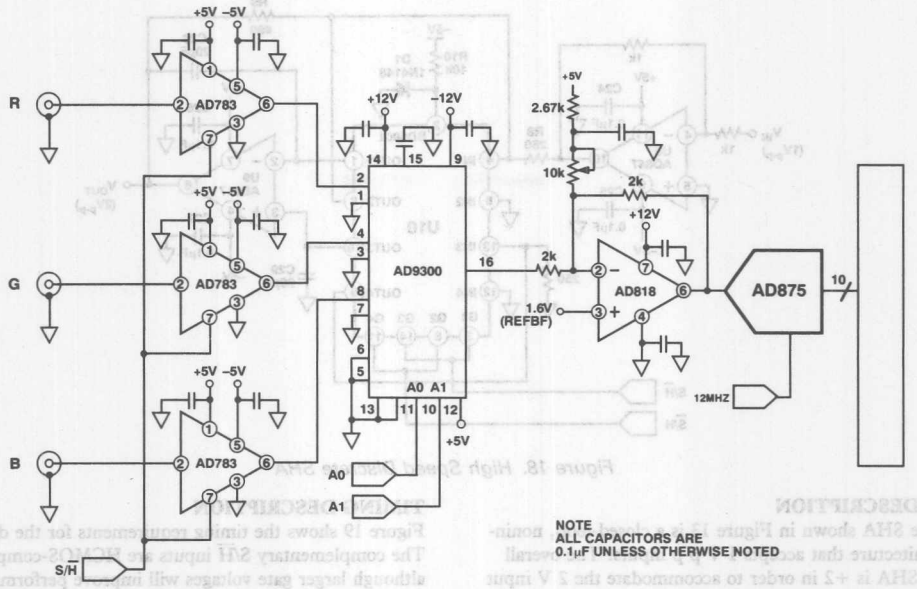


Figure 16. Multichannel Image Acquisition System

Referring to the timing diagram in Figure 17, the three analog inputs are simultaneously sampled on the falling edge of S/$\overline{H}$. After allowing the SHAs to settle (250 ns), the R channel is digitized at the conversion rate of 12 MHz (83.3 ns). Next, the MUX is switched to the G channel, allowed to settle (83.3 ns), and digitized. The B channel is digitized similarly. While the B channel is converted, the R channel data becomes available at the output of the AD875 (due to the pipelined latency). The rising edges of the signals RDAV, GDAV, and BDAV are the signals which indicate when valid data is available at the output of the A/D converter.

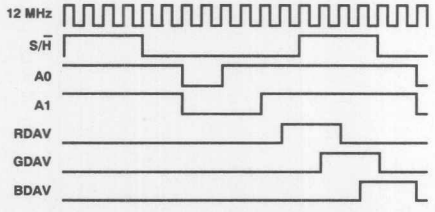


Figure 17. Timing Diagram for Figure 16

HIGH SPEED SAMPLE-AND-HOLD AMPLIFIER (SHA)

A sample-hold amplifier is often needed as part of a correlated double sampler or when high bandwidth inputs such as video signals are to be converted by the AD875. For fast, precise sampling required for video signals, an integrated solution such as the AD9101 track-and-hold amplifier is suggested for optimum performance. However, the requirements of many 10-bit imaging systems can be achieved using a SHA architecture similar to the one shown in Figure 18. This discrete SHA can accurately acquire a 1 V input step within 1 mV accuracy in less than 200 ns. Hold-mode settling within 1 mV is typically less than 50 ns. The resultant throughput rate is 3.3 Msps.

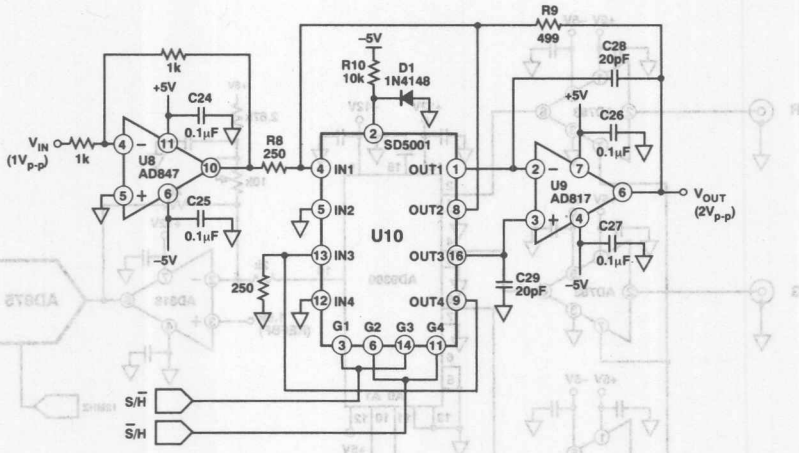


Figure 18. High Speed Discrete SHA

CIRCUIT DESCRIPTION

The discrete SHA shown in Figure 13 is a closed-loop, noninverting architecture that accepts 1 V p-p inputs. The overall gain of the SHA is +2 in order to accommodate the 2 V input span of the AD875. The AD847, with 0.1% settling time of 65 ns, is the suggested input buffer to the SHA. The circuit also employs an SD5001 that contains four ultrahigh speed DMOS switches (Q1–Q4). The low cost, fast settling time and high CMRR of the AD817 op amp are critical features necessary for optimal performance and economy.

In sample mode, Q1 and Q3 of the SD5001 are closed (Q2 and Q4 are open). C28 is charged to the input voltage level at a rate primarily determined by the time constant, R9 × C28, and the gain (2×). Simultaneously, C29 is connected to ground through a 250 Ω resistor. If C28 is equal to C29, charge injection from Q1 will be approximately equal to charge injection form Q3 based on the symmetry of the circuit and the inherent matching of the switch capacitance. The resultant pedestal errors appear as a common-mode signal to the AD817 and are approximately canceled from the differential architecture.

In hold mode, Q2 and Q4 are closed (Q1 and Q3 are open) to reduce feedthrough. The AD817 buffers the voltage held on C28 and settles within the requisite 1 mV within 50 ns. The output of the AD817 must then be level-shifted in order to interface with the AD875 input span requirements. Throughput rates greater than 3.3 Msps using this architecture are limited by the R_{ON} of the SD5001. Faster sample rates require open-loop architectures or diode-bridge switching in order to reduce the on-resistance.

TIMING DESCRIPTION

Figure 19 shows the timing requirements for the discrete SHA. The complementary S/$\overline{H}$ inputs are HCMOS-compatible although larger gate voltages will improve performance slightly by lowering the on resistances of the DMOS switches. The conversion is started as soon as the output of the SHA has settled within 16 mV of its final value.

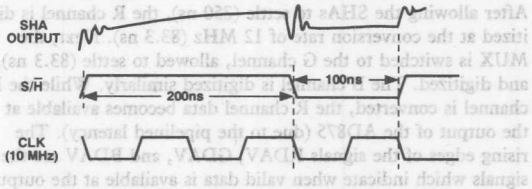


Figure 19. Timing Diagram for Discrete SHA

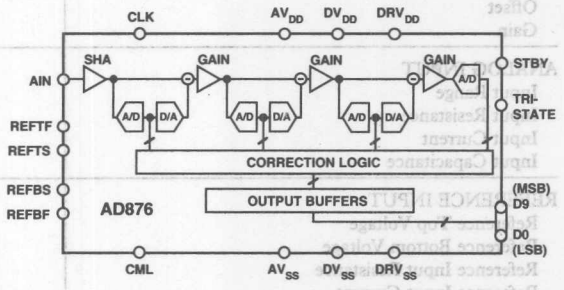
10-Bit 20 MSPS, 140 mW CMOS A/D Converter

AD876

FEATURES

CMOS 10-Bit 20 MSPS Sampling A/D Converter
Power Dissipation: 140 mW
+5 V Single Supply Operation
Differential Nonlinearity: 0.5 LSB
Guaranteed No Missing Codes
Power Down (Stand-By) Mode
Three-State Outputs
Digital I/Os Compatible with +5 V or +3.3 V Logic
Adjustable Reference Input
Small Size: 28-Pin SOIC or 48-Pin Thin Quad Flatpack (TQFP)

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD876 is a CMOS, 140 mW, 10-bit, 20 Msps analog-to-digital converter (ADC). The AD876 has an on-chip input sample-and-hold amplifier. The AD876's digital I/Os interface to either +5 V or +3.3 V logic. By implementing a multistage pipelined architecture with output error correction logic, the AD876 offers accurate performance and guarantees no missing codes over the full operating temperature range. To minimize external voltage drops, the reference ladder top and bottom are provided with force and sense pins.

The AD876 can be placed into a standby mode of operation reducing the power below 50 mW. Digital output data can be placed in a high impedance state and is offered in straight binary output.

The AD876's speed, resolution and single supply operation are ideally suited for a variety of applications in video, multimedia, imaging, high speed data acquisition and communications. The AD876's low power and single supply operation are required for high speed portable applications. Its speed and resolution are ideally suited for charge coupled device (CCD) input systems such as color scanners, digital copiers, electronic still cameras and camcorders.

The AD876 is packaged in a space saving 28-pin SOIC and 48-pin thin quad flatpack (TQFP) and is specified over the commercial (0°C to +70°C) temperature range.

PRODUCT HIGHLIGHTS

Low Power: The AD876 at 140 mW consumes a fraction of the power of presently available 10-bit, video-speed converters. Power-down mode and single supply operation further enhance its desirability in low power, battery operated applications such as electronic still cameras, camcorders and communication systems.

Very Small Package: The AD876 is available in both a 28-pin SOIC and 48-pin surface mount, thin quad flat package. The TQFP package is ideal for very tight, low headroom designs.

Digital I/O Functionality: The AD876 offers three-state output control.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD876–SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, DRV_{DD} = +3.3 V, V_{REFT} = +4.0 V, V_{REFB} = +2.0 V, f_{CLOCK} = 20 Msps, unless otherwise noted)

Parameter	AD876 Min	AD876 Typ	AD876 Max	Units
RESOLUTION	10			Bits
DC ACCURACY				
Integral Nonlinearity (INL)		±1.0	±2.0	LSB
Differential Nonlinearity (DNL)		±0.5	±1	LSB
No Missing Codes		Guaranteed		
Offset		0.5		% FSR
Gain		1.5		% FSR
ANALOG INPUT				
Input Range		2		V p-p
Input Resistance		50		kΩ
Input Current		60		μA
Input Capacitance		2.4		pF
REFERENCE INPUT				
Reference Top Voltage	3.5	4.0	4.2	V
Reference Bottom Voltage	1.8	2.0	2.5	V
Reference Input Resistance	TBD	330		Ω
Reference Input Current		6.0	7.0	mA
Reference Top Offset		25		mV
Reference Bottom Offset		25		mV
DYNAMIC PERFORMANCE				
Effective Number of Bits				
f_{IN} = 1 MHz		9.0		Bits
f_{IN} = 3.58 MHz		8.9		Bits
f_{IN} = 10 MHz		8.2		Bits
Signal-to-Noise and Distortion (S/N+D) Ratio				
f_{IN} = 1 MHz		56		dB
f_{IN} = 3.58 MHz		55		dB
f_{IN} = 10 MHz		51		dB
Total Harmonic Distortion (THD)				
f_{IN} = 1 MHz		60		dB
f_{IN} = 3.58 MHz		58		dB
f_{IN} = 10 MHz		54		dB
Spurious Free Dynamic Range		62		dB
Full Power Bandwidth		250		MHz
Intermodulation Distortion (IMD)[1]				
Second Order Products		TBD		dB
Third Order Products		TBD		dB
Differential Phase		0.5		Degree
Differential Gain		1		%
POWER SUPPLIES				
Operating Voltages				
AV_{DD}	+4.5		+5.25	Volts
DV_{DD}	+4.5		+5.25	Volts
DRV_{DD}	+3.0		+5.25	Volts
Operating Current				
IAV_{DD}		18	21	mA
IDV_{DD}		9	12	mA
$IDRV_{DD}$		1	3	mA
POWER CONSUMPTION		140	170	mW
TEMPERATURE RANGE				
Specified	0		+70	°C

NOTES

[1]fa = 4.5 MHz, fb = 5.5 MHz

Specifications subject to change without notice. See Definition of Specifications for additional information.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

DIGITAL SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, DRV_{DD} = +3.3 V, V_{REFT} = +4.0 V, V_{REFB} = +2.0 V, f_{CLOCK} = 20 Msps, C_L = 20 pF unless otherwise noted)

Parameter	Symbol	DRV_{DD}	AD876J Min	Typ	Max	Units
LOGIC INPUT						
High Level Input Voltage	V_{IH}	3.0	2.4			V
		5.0	4.0			V
		5.25		4.2		V
Low Level Input Voltage	V_{IL}	3.0			0.6	V
		5.0			1.0	V
		5.25			1.05	V
High Level Input Current	I_{IH}	5.0	–10		+10	µA
Low Level Input Current	I_{IL}	5.0	–50		+50	µA
Low Level Input Current (CLK Only)	I_{IL}	5.0	–10		+10	µA
Input Capacitance	C_{IN}			5		pF
LOGIC OUTPUTS						
High Level Output Voltage	V_{OH}					
(I_{OH} = 50 µA)		3.0	2.4			V
		5.0	3.8			V
(I_{OH} = 0.5 mA)		5.0	2.4			V
Low Level Output Voltage	V_{OL}					
(I_{OL} = 50 µA)		3.6			0.7	V
		5.25			1.05	V
(I_{OL} = 0.6 mA)		5.25			0.4	V
Output Capacitance	C_{OUT}			5		pF
Output Leakage Current	I_{OZ}		–10		10	µA

TIMING SPECIFICATIONS

	Symbol	Min	Typ	Max	Units
Maximum Conversion Rate[1]		20			MHz
Clock Period	t_C		50		ns
Clock High	t_{CH}	24	25		ns
Clock Low	t_{CL}	24	25		ns
Output Delay	t_{OD}	34	35		ns
Pipeline Delay (Latency)				4	Clock Cycles
Aperture Delay Time			TBD		ns
Aperture Jitter			TBD		ps

NOTE
[1]Conversion rate is operational down to 10 kHz without degradation in specified performance.

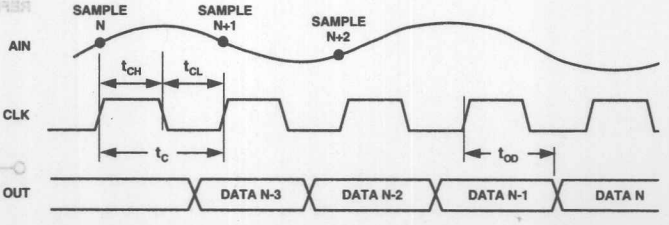


Figure 1. Timing Diagram

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

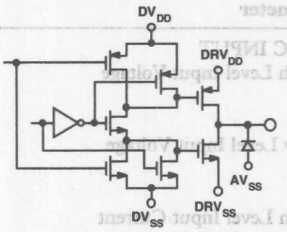
SOIC PIN DESCRIPTIONS

Symbol	Pin No.	Type	Name and Function
D0 (LSB)	3	DO	Least Significant Bit.
D1-D8	4–11	DO	Data Bits 1 through 4.
D9 (MSB)	12	DO	Most Siginificant Bit.
THREE-STATE	16	DI	THREE-STATE = LOW or N/C: Normal Operating Mode, Outputs THREE-STATE = HIGH: High Impedance
STBY	17	DI	STBY = LOW or N/C: Normal Operating Mode STBY = HIGH: Standby Mode
CLK	15	DI	Clock Input.
CML	26	AO	Bypass Pin for an Internal Bias Point.
REFTF	22	AI	Reference Top Force.
REFBF	24	AI	Reference Bottom Force.
REFTS	21	AI	Reference Top Sense.
REFBS	25	AI	Reference Bottom Sense.
AIN	27	AI	Analog Input.
AV_{DD}	28	P	+5 V Analog Supply.
AV_{SS}	1, 19	P	Analog Ground.
DV_{DD}	18	P	+5 V Digital Supply.
DV_{SS}	14	P	Digital Ground.
DRV_{DD}	2	P	+3.3 V/+5 V Digital Supply. Supply for digital input and output buffers.
DRV_{SS}	13	P	+3.3 V/+5 V Digital Ground. Supply for digital input and output buffers.
TP1	20	P	Connect to DV_{SS}.

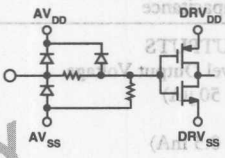
Type: AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; P = Power.

EQUIVALENT CIRCUITS

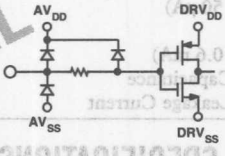
D0 – D9

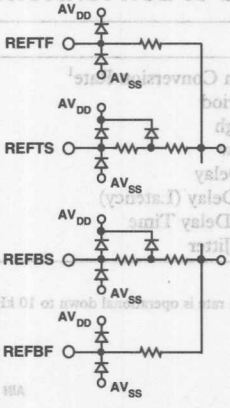


Three-State, STBY

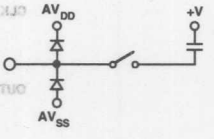


CLK

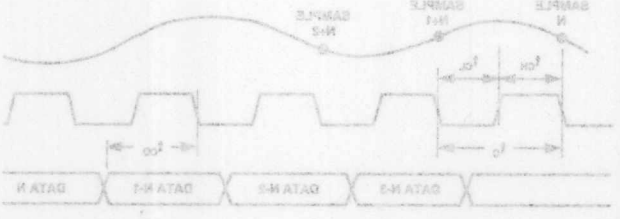




AIN



PRELIMINARY TECHNICAL DATA



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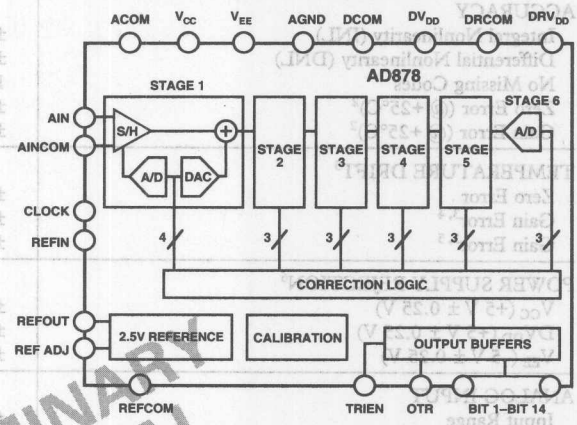
Complete 14-Bit 2.2 MSPS Monolithic A/D Converter

AD878

FEATURES

- Monolithic 14-Bit 2.2 MSPS A/D Converter
- Low Power Dissipation: 500 mW
- No Missing Codes Guaranteed
- Differential Nonlinearity Error: 0.5 LSB
- Complete: On-Chip Track-and-Hold Amplifier and Voltage Reference
- Signal-to-Noise and Distortion Ratio: 80 dB
- Spurious-Free Dynamic Range: 85 dB
- Out-of-Range Indicator
- 44-Pin PLCC

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD878 is a monolithic 14-bit, 2.2 Msps analog-to-digital converter with an on-chip, high performance sample-and-hold amplifier and voltage reference. The AD878 uses a multistage pipelined architecture with factory programmed calibration circuitry and output error correction logic to provide 14-bit accuracy at 2.2 Msps data rates. The AD878 combines a merged high speed bipolar/CMOS process and a novel architecture to achieve the resolution and speed of hybrid implementations at a fraction of the power consumption. Additionally, the greater reliability of monolithic construction offers improved system reliability and lower costs than hybrid designs.

The high input impedance, fast-settling input sample-and-hold (S/H) amplifier is well suited for both multiplexed systems that switch negative to positive full-scale voltage levels in successive channels and sampling single-channel inputs at frequencies up to the Nyquist rate. The AD878's wideband input combined with the power and cost savings over previously available hybrids will allow new design opportunities in communications, imaging and medical applications. The AD878 provides both reference output and reference input pins, allowing the on-board reference to serve as a system reference. An external reference can also be substituted to suit the dc accuracy and temperature drift requirements of the application. A single clock input is used to control all internal conversion cycles. The digital output data is presented in binary output format. An out-of-range signal indicates an overflow condition. It can be used with the most significant bit to determine low or high overflow.

The AD878 is fabricated on Analog Devices' ABCMOS process which utilizes high speed bipolar and CMOS transistors on a single chip. High speed, precision analog circuits are now combined with high density logic circuits.

The AD878 is packaged in a 44-pin plastic leaded chip carrier (PLCC) package and is specified for operation from 0°C to +70°C and –40°C to +85°C.

PRODUCT HIGHLIGHTS

The AD878 offers a complete single-chip sampling 14-bit, 2.2 Msps analog-to-digital conversion function in a 44-pin PLCC surface mount package.

Low Power: The AD878 at 650 mW max consumes a fraction of the power of presently available hybrids.

On-Chip Sample-and-Hold (S/H): The high impedance S/H input eliminates the need for external buffers.

Out of Range (OTR): The OTR output bit indicates when the input signal is beyond the AD878's input range.

Ease-of-Use: The AD878 is complete with S/H and voltage reference.

PRELIMINARY TECHNICAL DATA

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	J Grade[1]	A Grade[1]	Units
RESOLUTION	14	14	Bits min
MAX CONVERSION RATE	2.2	2.2	MHz min
ACCURACY			
Integral Nonlinearity (INL)	±2.5	±2.5	LSB typ
Differential Nonlinearity (DNL)	±0.5	±0.5	LSB typ
No Missing Codes	14	14	Bits Guaranteed
Zero Error (@ +25°C)[2]	±TBD	±TBD	% FSR max
Gain Error (@ +25°C)[2]	±TBD	±TBD	% FSR max
TEMPERATURE DRIFT[3]			
Zero Error	±TBD	±TBD	% FSR max
Gain Error[3, 4]	±TBD	±TBD	% FSR max
Gain Error[3, 5]	±TBD	±TBD	% FSR max
POWER SUPPLY REJECTION[6]			
V_{CC} (+5 V ± 0.25 V)	±TBD	±TBD	% FSR max
DV_{DD} (+5 V ± 0.25 V)	±TBD	±TBD	% FSR max
V_{EE} (–5 V ± 0.25 V)	±TBD	±TBD	% FSR max
ANALOG INPUT			
Input Range	±2.5	±2.5	Volts max
Input Resistance	1	1	MΩ typ
Input Capacitance	10	10	pF typ
INTERNAL VOLTAGE REFERENCE			
Output Voltage	2.5	2.5	Volts typ
Output Voltage Tolerance	±25	±25	mV max
Output Current (Available for External Loads)	2.5	2.5	mA typ
(External Load Should Not Change During Conversion)			
REFERENCE INPUT RESISTANCE	2	2	kΩ typ
POWER SUPPLIES			
Supply Voltages			
V_{CC}	+5	+5	V (±5% V_{CC} Operating)
V_{EE}	–5	–5	V (±5% V_{EE} Operating)
DV_{DD}, DRV_{DD}	+5	+5	V (±5% DV_{DD}, DRV_{DD} Operating)
Supply Current			
IV_{CC}	80	80	mA max
IV_{EE}	45	45	mA max
$IDRV_{DD}$, IDV_{DD}	5	5	mA max
POWER CONSUMPTION	500	500	mW typ
	650	650	mW max

NOTES
[1]Temperature ranges are as follows: J Grade: 0°C to +70°C; A Grade: –40°C to +85°C.
[2]Adjustable to zero with external potentiometers (See Zero and Gain Error Calibration section).
[3]+25°C to T_{MIN} and +25°C to T_{MAX}.
[4]Includes internal voltage reference error.
[5]Excludes internal reference drift.
[6]Change in Gain Error as a function of the dc supply voltage.
Specification subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, V_{EE} = –5 V, f_{SAMPLE} = 2.2 Msps, unless otherwise noted)[1]

Parameters	J Grade	A Grade	Units
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)			
f_{INPUT} = 100 kHz	80	80	dB typ
	TBD	TBD	dB min
f_{INPUT} = 1 MHz	TBD	TBD	dB typ
TOTAL HARMONIC DISTORTION (THD)			
f_{INPUT} = 100 kHz	–83	–83	dB typ
	TBD	TBD	dB max
f_{INPUT} = 1.0 MHz	TBD	TBD	dB typ
SPURIOUS FREE DYNAMIC RANGE (SFDR)			
f_{INPUT} = 100 kHz	85	85	dB typ
INTERMODULATION DISTORTION (IMD)[2]			
Second Order Products	80	80	dB typ
Third Order Products	80	80	dB typ
FULL POWER BANDWIDTH	2.0	2.0	MHz typ
SMALL SIGNAL BANDWIDTH	5	5	MHz typ
APERTURE DELAY	TBD	TBD	ns typ
APERTURE JITTER	20	TBD	ps rms typ
ACQUISITION TO FULL-SCALE STEP	200	200	ns typ
OVERVOLTAGE RECOVERY TIME	TBD	TBD	ns typ

NOTES
[1]f_{IN} amplitude = –0.5 dB full scale unless otherwise indicated. All measurements referred to a 0 dB (2.5 V pk) input signal unless otherwise indicated.
[2]fa = 100 kHz, fb = 95 kHz with f_{SAMPLE} = 2.2 MHz.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V, DV_{DD} = +5 V, DRV_{DD} =+5 V, V_{EE} = –5 V, f_{SAMPLE} = 2.2 Msps, unless otherwise noted)

Parameters	Symbol	J, A Grades	Units
LOGIC INPUTS			
High Level Input Voltage	V_{IH}	+3.8	V min
Low Level Input Voltage	V_{IL}	+0.95	V max
High Level Input Current (V_{IN} = DV_{DD})	I_{IH}	±10	µA max
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	±10	µA max
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUTS			
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	+2.4	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	+0.4	V max
Output Capacitance	C_{OUT}	5	pF typ

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SWITCHING SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, V_{EE} = –5 V; V_{IL} = 0.95 V, V_{IH} = 3.8 V, V_{OL} = 0.4 V and V_{OH} = 2.4 V)

Parameters	Symbol	J, A Grades	Units
Clock Period[1]	t_C	455	ns min
CLOCK Pulse Width High	t_{CH}	227	ns min
CLOCK Pulse Width Low	t_{CL}	227	ns min
Clock Duty Cycle[2]		TBD	% min (50% typ)
		TBD	% max
Output Delay	t_{OD}	20	ns min
Pipeline Delay (Latency)		4	Clock Cycles max
Data Access Time	t_{DD}	TBD	ns typ (100 pF Load)
Output Float Delay	t_{HL}	TBD	ns typ (10 pF Load)

NOTES
[1]Conversion rate is operational to TBD without degradation in specified performance.
[2]See Clock Input section for clock periods of TBD ns or greater.
Specifications subject to change without notice.

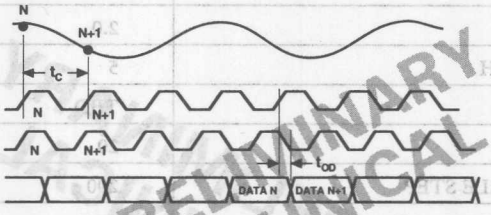


Figure 1. Timing Diagram

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
V_{CC}	ACOM	–0.5	+6.5	Volts
V_{EE}	ACOM	–6.5	+0.5	Volts
DV_{DD}	DCOM	–0.5	+6.5	Volts
DRV_{DD}	DRCOM	–0.5	+6.5	Volts
ACOM	DCOM	–1.0	+1.0	Volts
AINCOM	ACOM	–1.0	+1.0	Volts
REFCOM	ACOM	–1.0	+1.0	Volts
DRCOM	DCOM	–1.0	+1.0	Volts
V_{CC}	DV_{DD}	–6.5	+6.5	Volts
Clock Input	DCOM	–0.5	DV_{DD} + 0.5	Volts
Digital Outputs	DCOM	–0.5	DRV_{DD} + 0.3	Volts
AIN, REF IN	AGND	TBD	TBD	Volts
REF IN	V_{CC}	V_{EE}	0	Volts
REF IN	V_{EE}	0	V_{CC}	Volts
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Complete 12-Bit 1.25 MSPS Monolithic A/D Converter

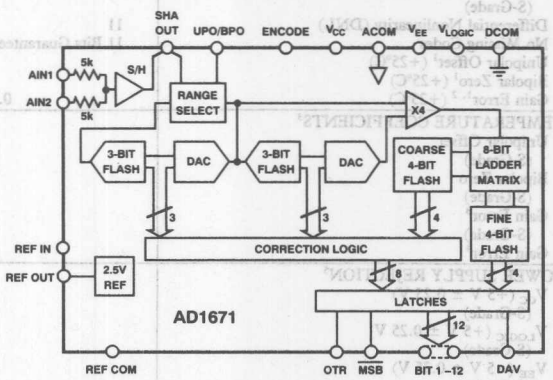
AD1671

2

FEATURES

Conversion Time: 800 ns
1.25 MHz Throughput Rate
Complete: On-Chip Sample-and-Hold Amplifier and Voltage Reference
Low Power Dissipation: 570 mW
No Missing Codes Guaranteed
Signal-to-Noise Plus Distortion Ratio
f_{IN} = 100 kHz: 70 dB
Pin Configurable Input Voltage Ranges
Twos Complement or Offset Binary Output Data
28-Pin DIP and 28-Pin Surface Mount Package
Out of Range Indicator

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1671 is a monolithic 12-bit, 1.25 MSPS analog-to-digital converter with an on-board, high performance sample-and-hold amplifier (SHA) and voltage reference. The AD1671 guarantees no missing codes over the full operating temperature range. The combination of a merged high speed bipolar/CMOS process and a novel architecture results in a combination of speed and power consumption far superior to previously available hybrid implementations. Additionally, the greater reliability of monolithic construction offers improved system reliability and lower costs than hybrid designs.

The fast settling input SHA is equally suited for both multiplexed systems that switch negative to positive full-scale voltage levels in successive channels and sampling inputs at frequencies up to and beyond the Nyquist rate. The AD1671 provides both reference output and reference input pins, allowing the on-board reference to serve as a system reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

The AD1671 uses a subranging flash conversion technique, with digital error correction for possible errors introduced in the first part of the conversion cycle. An on-chip timing generator provides strobe pulses for each of the four internal flash cycles. A single ENCODE pulse is used to control the converter. The digital output data is presented in twos complement or offset binary output format. An out-of-range signal indicates an overflow condition. It can be used with the most significant bit to determine low or high overflow.

The performance of the AD1671 is made possible by using high speed, low noise bipolar circuitry in the linear sections and low power CMOS for the logic sections. Analog Devices' ABCMOS-1 process provides both high speed bipolar and 2-micron CMOS devices on a single chip. Laser trimmed thin-film resistors are used to provide accuracy and temperature stability.

The AD1671 is available in two performance grades and three temperature ranges. The AD1671J and K grades are available over the 0°C to +70°C temperature range. The AD1671A grade is available over the −40°C to +85°C temperature range. The AD1671S grade is available over the −55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

The AD1671 offers a complete single chip sampling 12-bit, 1.25 MSPS analog-to-digital conversion function in a 28-pin package.

The AD1671 at 570 mW consumes a fraction of the power of currently available hybrids.

An OUT OF RANGE output bit indicates when the input signal is beyond the AD1671's input range.

Input signal ranges are 0 V to +5 V unipolar or ±5 V bipolar, selected by pin strapping, with an input resistance of 10 kΩ. The input signal range can also be pin strapped for 0 V to +2.5 V unipolar or ±2.5 V bipolar with an input resistance of 10 MΩ.

Output data is available in unipolar, bipolar offset or bipolar twos complement binary format.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter	AD1671J/A/S Min	AD1671J/A/S Typ	AD1671J/A/S Max	AD1671K Min	AD1671K Typ	AD1671K Max	Units
RESOLUTION	12			12			Bits
CONVERSION TIME			800			800	ns
ACCURACY							
Integral Nonlinearity (INL)		±1.5	±2.5		±0.7	±2.5	LSB
(S-Grade)			±3.0				
Differential Nonlinearity (DNL)	11			12			Bits
No Missing Codes	11 Bits Guaranteed			12 Bits Guaranteed			
Unipolar Offset[1] (+25°C)			±9			±9	LSB
Bipolar Zero[1] (+25°C)			±10			±10	LSB
Gain Error[1, 2] (+25°C)		0.1	0.35		0.1	0.35	% FSR
TEMPERATURE COEFFICIENTS[3]							
Unipolar Offset			±25			±25	ppm/°C
(S-Grade)			±25				
Bipolar Zero			±25			±25	ppm/°C
(S-Grade)			±30				
Gain Error[3]			±30			±30	ppm/°C
(S-Grade)			±40				
Gain Error[4]			±20			±20	ppm/°C
POWER SUPPLY REJECTION[5]							
V_{CC} (+5 V ± 0.25 V)			±4			±4	LSB
(S-Grade)			±5				
V_{LOGIC} (+5 V ± 0.25 V)			±4			±4	LSB
(S-Grade)			±5				
V_{EE} (−5 V ± 0.25 V)			±4			±4	LSB
(S-Grade)			±5				
ANALOG INPUT							
Input Ranges							
Bipolar	−2.5		+2.5	−2.5		+2.5	Volts
	−5.0		+5.0	−5.0		+5.0	Volts
Unipolar	0		+2.5	0		+2.5	Volts
	0		+5.0	0		+5.0	Volts
Input Resistance							
(0 V to +2.5 V or ±2.5 V Range)		10			10		MΩ
(0 V to +5.0 V or ±5 V Range)	8	10	12	8	10	12	kΩ
Input Capacitance		10			10		pF
Aperture Delay		15			15		ns
Aperture Jitter		20			20		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage	2.475	2.5	2.525	2.475	2.5	2.525	Volts
Output Current							
Unipolar Mode			+2.5			+2.5	mA
Bipolar Mode			+1.0			+1.0	mA
LOGIC INPUTS							
High Level Input Voltage, V_{IH}	2.0			2.0			Volts
Low Level Input Voltage, V_{IL}			0.8			0.8	Volts
High Level Input Current, I_{IH} ($V_{IN} = V_{LOGIC}$)	−10		+10	−10		+10	μA
Low Level Input Current, I_{IL} ($V_{IN} = 0$ V)	−10		+10	−10		+10	μA
Input Capacitance, C_{IN}		5			5		pF
LOGIC OUTPUTS							
High Level Output Voltage, V_{OH} ($I_{OH} = 0.5$ mA)	2.4			2.4			Volts
Low Level Output Voltage, V_{OL} ($I_{OL} = 1.6$ mA)			0.4			0.4	Volts
POWER SUPPLIES							
Operating Voltages							
V_{CC}	+4.75		+5.25	+4.75		+5.25	Volts
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	Volts
V_{EE}	−4.75		−5.25	−4.75		−5.25	Volts
Operating Current							
I_{CC}		55	68		55	68	mA
I_{LOGIC}[6]		3	5		3	5	mA
I_{EE}		−55	−68		−55	−68	mA
POWER CONSUMPTION		570	750		570	750	mW
TEMPERATURE RANGE (SPECIFIED)							
J/K	0		+70	0		+70	°C
A	−40		+85	−40		+85	°C
S	−55		+125	−55		+125	°C

NOTES
[1]Adjustable to zero with external potentiometers.
[2]Includes internal voltage reference error.
[3]+25°C to T_{MIN} and +25°C to T_{MAX}.
[4]Excludes internal reference drift.
[5]Change in gain error as a function of the dc supply voltage.
[6]Tested under static conditions. See Figure 15 for typical curve of I_{LOGIC} vs. load capacitance at maximum t_C.

Specifications subject to change without notice.

AC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%, f_{SAMPLE} = 1 MSPS, f_{INPUT} = 100 kHz, unless otherwise noted)[1]

Parameter	AD1671J/A/S Min	AD1671J/A/S Typ	AD1671J/A/S Max	AD1671K Min	AD1671K Typ	AD1671K Max	Units
SIGNAL-TO-NOISE PLUS DISTORTION RATIO (S/N + D)							
−0.5 dB Input	68	70		68	71		dB
−20 dB Input		50			51		dB
EFFECTIVE NUMBER OF BITS (ENOB)	11.2			11.2			Bits
TOTAL HARMONIC DISTORTION (THD)		−80	−75		−83	−75	dB
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−80	−77		−81	−77	dB
SMALL SIGNAL BANDWIDTH		12			12		MHz
FULL POWER BANDWIDTH		2			2		MHz
INTERMODULATION DISTORTION (IMD)[2]							
2nd Order Products		−80	−75		−80	−75	dB
3rd Order Products		−85	−75		−85	−75	dB

NOTES
[1]f_{IN} amplitude = −0.5 dB (9.44 V p–p) bipolar mode full scale unless otherwise indicated. All measurements referred to a 0 dB (±5 V) input signal, unless otherwise indicated.
[2]f_A = 99 kHz, f_B = 100 kHz with f_{SAMPLE} = 1 MSPS.
Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (For all grades T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%; V_{IL} = 0.8 V, V_{IH} = 2.0 V, V_{OL} = 0.4 V and V_{OH} = 2.4 V)

Parameters	Symbol	Min	Typ	Max	Units
Conversion Time	t_C			800	ns
Sample Rate	F_S			1.25	Msps
ENCODE Pulse Width High (Figure 1a)	t_{ENC}	20		50	ns
ENCODE Pulse Width Low (Figure 1b)	t_{ENCL}	20			ns
DAV Pulse Width	t_{DAV}	150		300	ns
ENCODE Falling Edge Delay	t_F	0			ns
Start New Conversion Delay	t_R	0			ns
Data and OTR Delay from DAV Falling Edge	t_{DD}[1]	20	75		ns
Data and OTR Valid before DAV Rising Edge	t_{SS}[2]	20	75		ns

NOTES
[1]t_{DD} is measured from when the falling edge of DAV crosses 0.8 V to when the output crosses 0.4 V or 2.4 V with a 25 pF load capacitor on each output pin.
[2]t_{SS} is measured from when the outputs cross 0.4 V or 2.4 V to when the rising edge of DAV crosses 2.4 V with a 25 pF load capacitor on each output pin.
Specifications subject to change without notice.

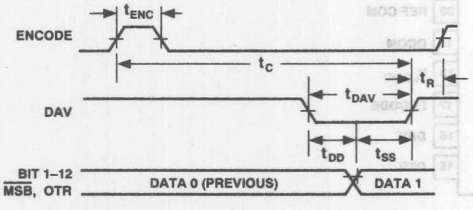


Figure 1a. Encode Pulse HIGH

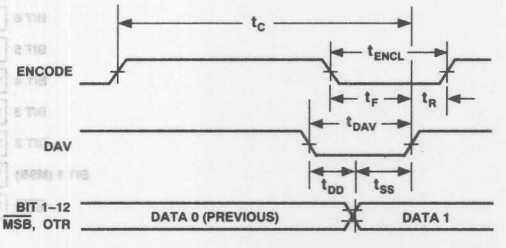


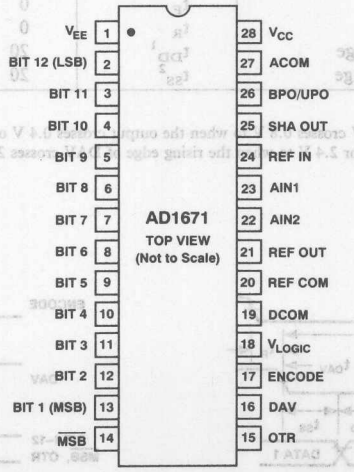
Figure 1b. Encode Pulse LOW

PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
ACOM	27	P	Analog Ground.
AIN	22, 23	AI	Analog Inputs, AIN1 and AIN2. The AD1671 can be pin strapped for four input ranges: Range — Pin Strap — Signal Input 0 to +2.5 V, ±2.5 V — Connect AIN1 to AIN2 — AIN1 or AIN2 0 to +5 V, ±5 V — Connect AIN1 or AIN2 to ACOM — AIN1 or AIN2
BIT 1 (MSB)	13	DO	Most Significant Bit.
BIT 2–BIT 11	12–3	DO	Data Bits 2 through 11.
BIT 12 (LSB)	2	DO	Least Significant Bit.
BPO/UPO	26	AI	Bipolar or Unipolar Configuration Pin. See section on Input Range Connections for details.
DAV	16	DO	Data Available Output. The rising edge of DAV indicates an end of conversion and can be used to latch current data into an external register. The falling edge of DAV can be used to latch previous data into an external register.
DCOM	19	P	Digital Ground.
ENCODE	17	DI	The analog input is sampled on the rising edge of ENCODE.
$\overline{\text{MSB}}$	14	DO	Inverted Most Significant Bit. Provides twos complement output data format.
OTR	15	DO	Out of Range is Active HIGH when the analog input is out of range. See Output Data Format, Table III.
REF COM	20	AI	REF COM is the internal reference ground pin. REF COM should be connected as indicated in the Grounding and Decoupling Rules and Optional External Reference Connection Sections.
REF IN	24	AI	REF IN is the external 2.5 V reference input.
REF OUT	21	AO	REF OUT is the internal 2.5 V reference output.
SHA OUT	25	AO	No Connect for bipolar input ranges. Connect SHA OUT to BPO/UPO for unipolar input ranges.
V_{CC}	28	P	+5 V Analog Power.
V_{EE}	1	P	−5 V Analog Power.
V_{LOGIC}	18	P	+5 V Digital Power.

TYPE: AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; P = Power.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
V_{CC}	ACOM	−0.5	+6.5	Volts
V_{EE}	ACOM	−6.5	+0.5	Volts
V_{LOGIC}	DCOM	−0.5	+6.5	Volts
ACOM	DCOM	−1.0	+1.0	Volts
V_{CC}	V_{LOGIC}	−6.5	+6.5	Volts
ENCODE	DCOM	−0.5	V_{LOGIC}+0.5	Volts
REF IN	ACOM	−0.5	V_{CC}+0.5	Volts
AIN	ACOM	−11.0	+11.0	Volts
BPO/UPO	ACOM	−0.5	V_{CC}+0.5	Volts
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model[1]	Linearity	Temperature Range	Package Option[2, 3]
AD1671JQ	±2.5 LSB	0°C to +70°C	Q-28
AD1671KQ	±2 LSB	0°C to +70°C	Q-28
AD1671JP	±2.5 LSB	0°C to +70°C	P-28A
AD1671KP	±2 LSB	0°C to +70°C	P-28A
AD1671AQ	±2.5 LSB	−40°C to +85°C	Q-28
AD1671AP	±2.5 LSB	−40°C to +85°C	P-28A
AD1671SQ	±3 LSB	−55°C to +125°C	Q-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices' Military Products Databook or current AD1671/883 data sheet.
[2]P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.
[3]Analog Devices reserves the right to ship side brazed ceramic packages in lieu of cerdip.

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB (1.22 mV for a 10 V span) before the first code transition (all zeros to only the LSB on). "Full-scale" is defined as a level 1 1/2 LSB beyond the last code transition (to all ones). The deviation is measured from the low side transition of each particular code to the true straight line.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from the ideal value. Thus every code has a finite width. Guaranteed no missing codes to 11 or 12-bit resolution indicates that all 2048 and 4096 codes, respectively, must be present over all operating ranges. No missing codes to 11 bits (in the case of a 12-bit resolution ADC) also means that no two consecutive codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual from that point. This offset can be adjusted as discussed later. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustments.

BIPOLAR ZERO

In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

GAIN ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (4.9963 volts for 5.000 volts full scale). The gain error is the deviation of the actual level at the last transition from the ideal level. The gain error can be adjusted to zero as shown in Figures 4 through 7.

TEMPERATURE COEFFICIENTS

The temperature coefficients for unipolar offset, bipolar zero and gain error specify the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

One of the effects of power supply error on the performance of the device will be a small change in gain. The specifications show the maximum full-scale change from the initial value with the supplies at the various limits.

DYNAMIC SPECIFICATIONS

SIGNAL-TO-NOISE PLUS DISTORTION (S/N+D) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

ENOB is calculated from the expression (S/N+D) = 6.02N + 1.76 dB, where N is equal to the effective number of bits.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

INTERMODULATION DISTORTION (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products of order (m+n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb), and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (2fb − fa). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sum is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT

The peak spurious or peak harmonic component is the largest spectral component, excluding the input signal and dc. This

value is expressed in decibels relative to the rms value of a full-scale input signal.

APERTURE DELAY

Aperture delay is the difference between the switch delay and the analog delay of the SHA. This delay represents the point in time, relative to the rising edge of ENCODE input, that the analog input is sampled.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples.

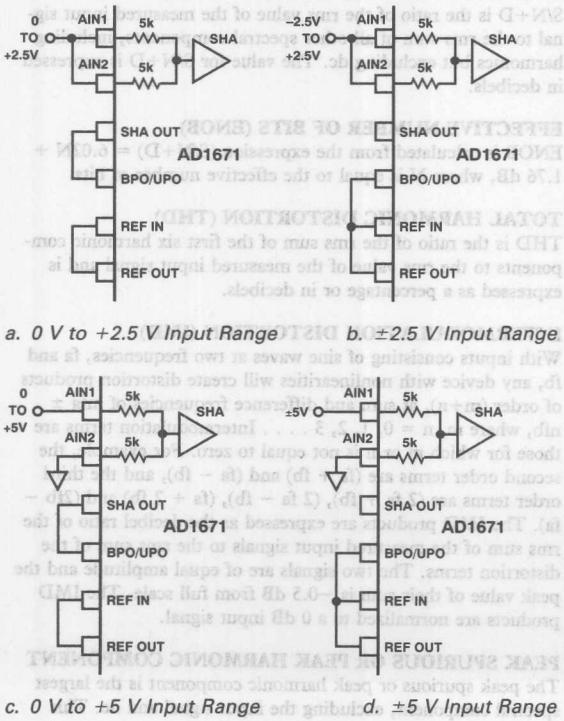
FULL POWER BANDWIDTH

The input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

THEORY OF OPERATION

The AD1671 uses a successive subranging architecture. The analog-to-digital conversion takes place in four independent steps or flashes. The sampled analog input signal is subranged to an intermediate residue voltage for the final 12-bit result by utilizing multiple flashes with subtraction DACs (see the AD1671 functional block diagram).

The AD1671 can be configured to operate with unipolar (0 V to +5 V, 0 V to +2.5 V) or bipolar (±5 V, ±2.5 V) inputs by connecting AIN (Pins 22, 23), SHA OUT (Pin 25) and BPO/UPO (Pin 26) as shown in Figure 2.



a. 0 V to +2.5 V Input Range *b. ±2.5 V Input Range*

c. 0 V to +5 V Input Range *d. ±5 V Input Range*

Figure 2. AD1671 Input Range Connections

The AD1671 conversion cycle begins by simply providing an active HIGH level on the ENCODE pin (Pin 17). The rising edge of the ENCODE pulse starts the conversion. The falling edge of the ENCODE pulse is specified to operate within a window of time, less than 50 ns after the rising edge of ENCODE or after the falling edge of DAV. The time window prevents digitally coupled noise from being introduced during the final stages of conversion. An internal timing generator circuit accurately controls SHA, flash and DAC timing.

Upon receipt of an ENCODE command the input voltage is held by the front-end SHA and the first 3-bit flash converts the analog input voltage. The 3-bit result is passed to a correction logic register and a segmented current output DAC. The DAC output is connected through a resistor (within the Range/Span Select Block) to SHA OUT. A residue voltage is created by subtracting the DAC output from SHA OUT, which is less than one eighth of the full-scale analog input. The second flash has an input range that is configured with one bit of overlap with the previous DAC. The overlap allows for errors during the flash conversion. The first residue voltage is connected to the second 3-bit flash and to the noninverting input of a high speed, differential, gain of eight amplifier. The second flash result is passed to the correction logic register and to the second segmented current output DAC. The output of the second DAC is connected to the inverting input of the differential amplifier. The differential amplifier output is connected to a two-step, backend, 8-bit flash. This 8-bit flash consists of coarse and fine flash converters. The result of the coarse 4-bit flash converter, also configured to overlap one bit of DAC 2, is connected to the correction logic register and selects one of 16 resistors from which the fine 4-bit flash will establish its span voltage. The fine 4-bit flash is connected directly to the output latches.

The internal timing generator automatically places the SHA into the acquire mode when DAV goes LOW. Upon completion of conversion (when DAV is set HIGH), the SHA has acquired the analog input to the specified level of accuracy and will remain in the sample mode until the next ENCODE command.

The AD1671 will flag an out-of-range condition when the input voltage exceeds the analog input range. OTR (Pin 15) is active HIGH when an out-of-range high or low condition exists. Bits 1–12 are HIGH when the analog input voltage is greater than the selected input range and LOW when the analog input is less than the selected input range.

AD1671 DYNAMIC PERFORMANCE

The AD1671 is specified for dc and dynamic performance. A sampling converter's dynamic performance reflects both quantizer and sample-and-hold amplifier (SHA) performance. Quantizer nonlinearities, such as INL and DNL, can degrade dynamic performance. However, a SHA is the critical element which has to accurately sample fast slewing analog input signals. The AD1671's high performance, low noise, patented on-chip SHA minimizes distortion and noise specifications. Nonlinearities are minimized by using a fast slewing, low noise architecture and subregulation of the sampling switch to provide constant offsets (therefore reducing input signal dependent nonlinearities).

Figure 3 is a typical 2k point Fast Fourier Transform (FFT) plot of a 100 kHz input signal sampled at 1 MHz. The fundamental amplitude is set at −0.5 dB to avoid input signal clipping of offset or gain errors. Note the total harmonic distortion is approximately −81 dB, signal to noise plus distortion is 71 dB and the spurious free dynamic range is 84 dB.

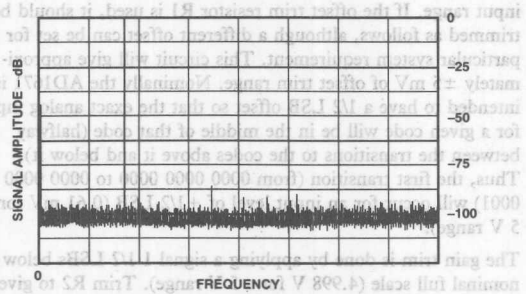


Figure 3. AD1671 FFT Plot, f_{IN} = 100 kHz, f_{SAMPLE} = 1 MHz

Figure 4 plots both S/(N+D) and Effective Number of Bits (ENOB) for a 100 kHz input signal sampled from 666 kHz to 1.25 MHz.

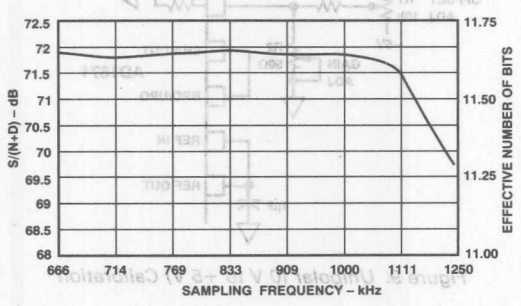


Figure 4. S/(N+D) vs. Sampling Frequency, f_{IN} = 100 kHz

Figure 5 is a THD plot for a full-scale 100 kHz input signal with the sample frequency swept from 666 kHz to 1.25 MHz.

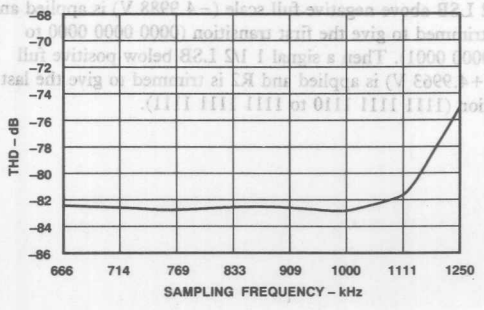


Figure 5. THD vs. Sampling Rate, f_{IN} = 100 kHz

The AD1671's SFDR performance is ideal for use in communication systems such as high speed modems and digital radios. The SFDR is better than 84 dB with sample rates up to 1.11 MHz and increases as the input signal amplitude is attenuated by approximately 3 dB. Note also the SFDR is typically better than 80 dB with input signals attenuated by up to −7 dB.

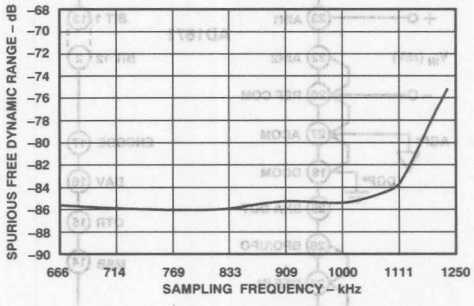


Figure 6. Spurious Free Dynamic Range vs. Sampling Rate, f_{IN} = 100 kHz

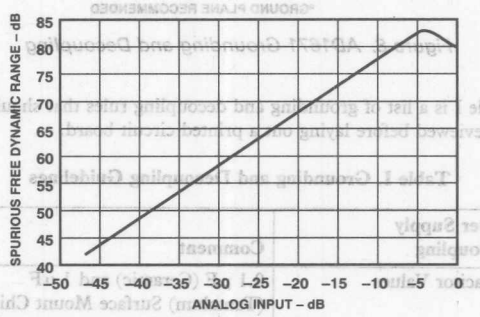


Figure 7. Spurious Free Dynamic Range vs. Input Amplitude, f_{IN} = 250 kHz

APPLYING THE AD1671

GROUNDING AND DECOUPLING RULES

Proper grounding and decoupling should be a primary design objective in any high speed, high resolution system. The AD1671 separates analog and digital grounds to optimize the management of analog and digital ground currents in a system. The AD1671 is designed to minimize the current flowing from REF COM (Pin 20) by directing the majority of the current from V_{CC} (+5 V–Pin 28) to V_{EE} (−5 V–Pin 1). Minimizing analog ground currents hence reduces the potential for large ground voltage drops. This can be especially true in systems that do not utilize ground planes or wide ground runs. REF COM is also configured to be code independent, therefore reducing input dependent analog ground voltage drops and errors. Code dependent ground current is diverted to ACOM (Pin 27). Also critical in any high speed digital design is the use of proper digital grounding techniques to avoid potential CMOS "ground bounce." Figure 3 is provided to assist in the proper layout, grounding and decoupling techniques.

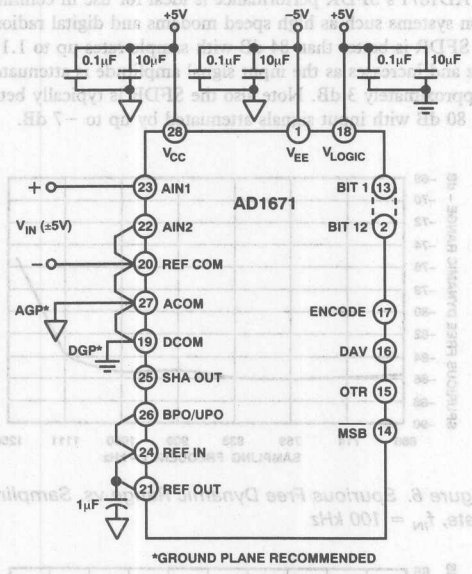


Figure 8. AD1671 Grounding and Decoupling

Table I is a list of grounding and decoupling rules that should be reviewed before laying out a printed circuit board.

Table I. Grounding and Decoupling Guidelines

Power Supply Decoupling	**Comment**
Capacitor Values	0.1 μF (Ceramic) and 1 μF (Tantalum) Surface Mount Chip Capacitors Recommended to Reduce Lead Inductance
Capacitor Locations	Directly at Positive and Negative Supply Pins to Common Ground Plane
Reference (REF OUT)	
Capacitor Value	1 μF (Tantalum) to ACOM
Grounding	
Analog Ground	Ground Plane or Wide Ground Return Connected to the Analog Power Supply
Reference Ground (REF COM)	Critical Common Connections Should be Star Connected to REF COM (as Shown in Figure 8)
Digital Ground	Ground Plane or Wide Ground Return Connected to the Digital Power Supply
Analog and Digital Ground	Connected Together Once at the AD1671

UNIPOLAR (0 V TO +5 V) CALIBRATION

The AD1671 is factory trimmed to minimize offset, gain and linearity errors. In some applications the offset and gain errors of the AD1671 need to be externally adjusted to zero. This is accomplished by trimming the voltage at AIN2 (Pin 22). The circuit in Figure 9 is recommended for calibrating offset and gain errors of the AD1671 when configured in the 0 V to +5 V input range. If the offset trim resistor R1 is used, it should be trimmed as follows, although a different offset can be set for a particular system requirement. This circuit will give approximately ±5 mV of offset trim range. Nominally the AD1671 is intended to have a 1/2 LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above it and below it). Thus, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2 LSB (0.61 mV for 5 V range).

The gain trim is done by applying a signal 1 1/2 LSBs below the nominal full scale (4.998 V for a 5 V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111). This circuit will give approximately ±0.5% FS of adjustment range.

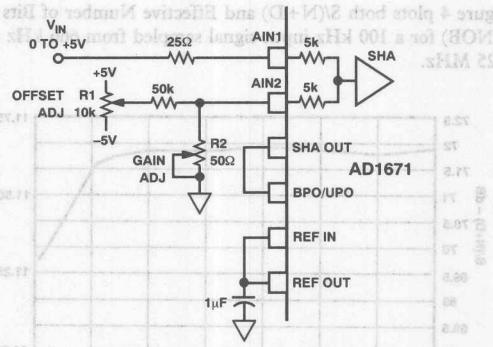


Figure 9. Unipolar (0 V to +5 V) Calibration

BIPOLAR (±5 V) CALIBRATION

The connections for the bipolar ±5 V input range is shown in Figure 10.

Bipolar calibration is similar to unipolar calibration. First, a signal 1/2 LSB above negative full scale (−4.9988 V) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2 LSB below positive full scale (+4.9963 V) is applied and R2 is trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

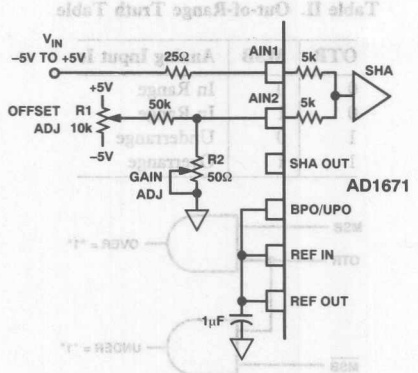


Figure 10. Bipolar (±5 V) Calibration

UNIPOLAR (0 V TO +2.5 V) CALIBRATION

The connections for the 0 V to +2.5 V input range calibration is shown in Figure 11. Figure 11 shows an example of how the offset error can be trimmed in front of the AD1671. The procedure for trimming the offset and gain errors is the same as for the unipolar 5 V range.

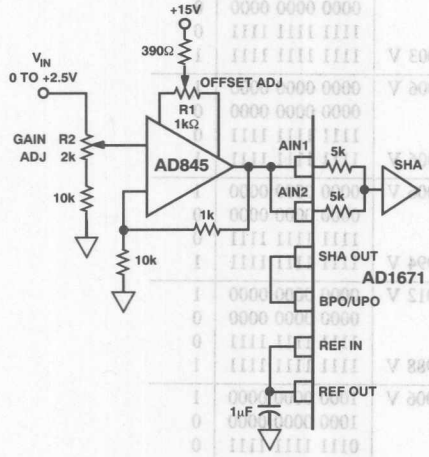


Figure 11. Unipolar (0 V to +2.5 V) Calibration

BIPOLAR (±2.5 V) CALIBRATION

The connections for the bipolar ±2.5 V input range is shown in Figure 12.

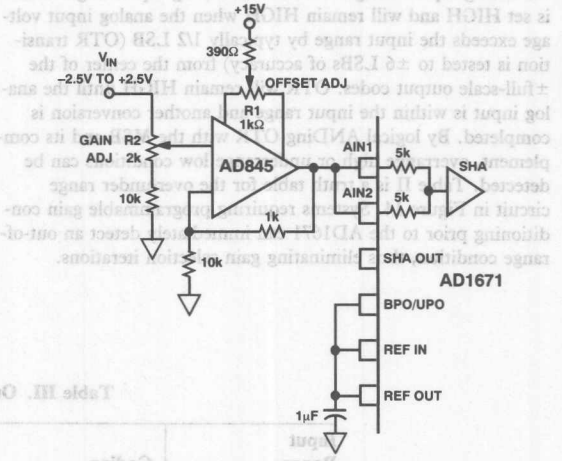


Figure 12. Bipolar (±2.5 V) Calibration

OUTPUT LATCHES

Figure 13 shows the AD1671 connected to the 74HC574 octal D-type edge-triggered latches with 3-state outputs. The latch can drive highly capacitive loads (i.e., bus lines, I/O ports) while maintaining the data signal integrity. The maximum setup and hold times of the 574 type latch must be less than 20 ns (t_{DD} and t_{SS} minimum). To satisfy the requirements of the 574 type latch the recommended logic families are S, AS, ALS, F or BCT. New data from the AD1671 is latched on the rising edge of the DAV (Pin 16) output pulse. Previous data can be latched by inverting the DAV output with a 7404 type inverter.

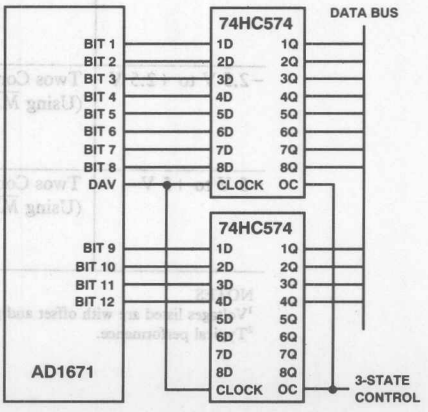


Figure 13. AD1671 to Output Latches

OUT OF RANGE

An out-of-range condition exists when the analog input voltage is beyond the input range (0 V to +2.5 V, 0 V to +5 V, ±2.5 V, ±5 V) of the converter. OTR (Pin 15) is set low when the analog input voltage is within the analog input range. OTR is set HIGH and will remain HIGH when the analog input voltage exceeds the input range by typically 1/2 LSB (OTR transition is tested to ±6 LSBs of accuracy) from the center of the ±full-scale output codes. OTR will remain HIGH until the analog input is within the input range and another conversion is completed. By logical ANDing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table II is a truth table for the over/under range circuit in Figure 14. Systems requiring programmable gain conditioning prior to the AD1671 can immediately detect an out-of-range condition, thus eliminating gain selection iterations.

Table II. Out-of-Range Truth Table

OTR	MSB	Analog Input Is
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

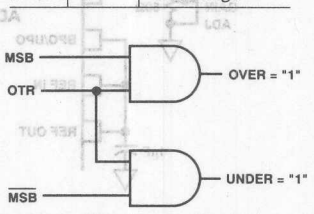


Figure 14. Overrange or Underrange Logic

Table III. Output Data Format

Input Range	Coding	Analog Input[1]	Digital Output	OTR[2]
0 V to +2.5 V	Straight Binary	≤ −0.0003 V	0000 0000 0000	1
		0 V	0000 0000 0000	0
		+2.5 V	1111 1111 1111	0
		≥ +2.5003 V	1111 1111 1111	1
0 V to +5 V	Straight Binary	≤ −0.0006 V	0000 0000 0000	1
		0 V	0000 0000 0000	0
		+5 V	1111 1111 1111	0
		≥ +5.0006 V	1111 1111 1111	1
−2.5 V to +2.5 V	Offset Binary	≤ −2.5006 V	0000 0000 0000	1
		−2.5 V	0000 0000 0000	0
		+2.5 V	1111 1111 1111	0
		≥ +2.4994 V	1111 1111 1111	1
−5 V to +5 V	Offset Binary	≤ −5.0012 V	0000 0000 0000	1
		−5 V	0000 0000 0000	0
		+5 V	1111 1111 1111	0
		≥ +4.9988 V	1111 1111 1111	1
−2.5 V to +2.5 V	Twos Complement (Using $\overline{MSB}$)	≤ −2.5006 V	1000 0000 0000	1
		−2.5 V	1000 0000 0000	0
		+2.5 V	0111 1111 1111	0
		≥ +2.4994 V	0111 1111 1111	1
−5 V to +5 V	Twos Complement (Using $\overline{MSB}$)	≤ −5.0012 V	1000 0000 0000	1
		−5 V	1000 0000 0000	0
		+5 V	0111 1111 1111	0
		≥ +4.9988 V	0111 1111 1111	1

NOTES
[1]Voltages listed are with offset and gain errors adjusted to zero.
[2]Typical performance.

OUTPUT DATA FORMAT

The AD1671 provides both MSB and $\overline{\text{MSB}}$ outputs, delivering data in positive true straight binary for unipolar input ranges and positive true offset binary or twos complement for bipolar input ranges. Straight binary coding is used for systems that accept positive-only signals. If straight binary coding is used with bipolar input signals, a 0 V input would result in a binary output of 2048. The application software would have to subtract 2048 to determine the true input voltage. Host registers typically perform math on signed integers and assume data is in that format. Twos complement format minimizes software overhead which is especially important in high speed data transfers, such as a DMA operation. The CPU is not bogged down performing data conversion steps, hence the total system throughput is increased.

OPTIONAL EXTERNAL REFERENCE

The AD1671 includes an on-board +2.5 V reference. The reference input pin (REF IN) can be connected to reference output pin (REF OUT) or a standard external +2.5 V reference can be selected to meet specific system requirements. Fast switching input dependent currents are modulated at the reference input. The reference input voltage can be held with the use of a capacitor. To prevent the AD1671's on-board reference from oscillating when not connected to REF IN, REF OUT must be connected to +5 V. It is possible to connect REF OUT to +5 V due to its output circuit implementation which shuts down the reference.

I_{LOGIC} vs. CONVERSION RATE

Figure 15 is the typical logic supply current vs. conversion rate for various capacitor loads on the digital outputs.

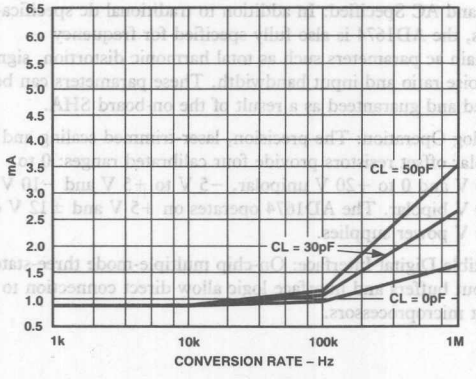


Figure 15. I_{LOGIC} vs. Conversion Rate for Various Capacitive Loads on the Digital Outputs

APPLICATIONS

AD1671 TO ADSP-2100A

Figure 16 demonstrates the AD1671 to ADSP-2100A interface. The 2100A with a clock frequency of 12.5 MHz can execute an instruction in one 80 ns cycle. The AD1671 is configured to perform continuous time sampling. The DAV output of the AD1671 is asserted at the end of each conversion. DAV can be used to latch the conversion result into the two 574 octal D-latches. The falling edge of the sampling clock is used to generate an interrupt (IRQ3) for the processor. Upon interrupt, the ADSP-2100A starts a data memory read by providing an address on the DMA bus. The decoded address generates OE for the latches and the processor reads their output over the DMA bus. The conversion result is read within a single processor cycle.

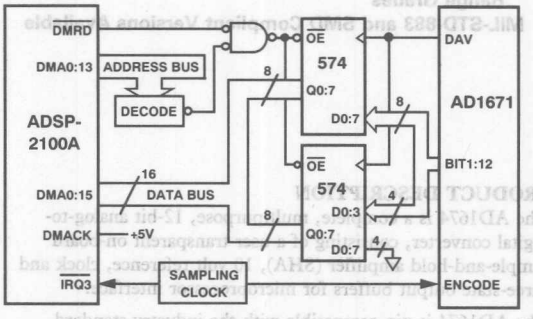


Figure 16. AD1671 to ADSP-2100A Interface

AD1671 TO ADSP-2101/2102

Figure 17 is identical to the 2100A interface except the sampling clock is used to generate an interrupt (IRQ2) for the processor. Upon interrupt the ADSP-2100A starts a data memory read by providing an address on the address (A) bus. The decode address generates OE for the D-latches and the processor reads their output over the Data (D) bus. Reading the conversion result is thus completed within a single processor cycle.

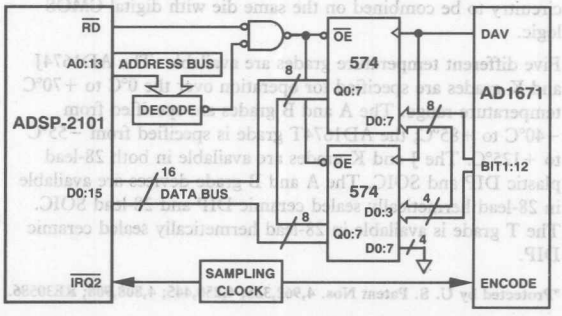
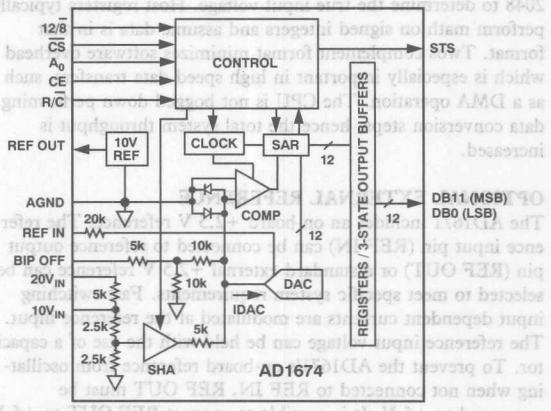


Figure 17. AD1671 to ADSP-2101/ADSP-2102 Interface

FEATURES

Complete Monolithic 12-Bit 10 μs Sampling ADC
On-Board Sample-and-Hold Amplifier
Industry Standard Pinout
8- and 16-Bit Microprocessor Interface
AC and DC Specified and Tested
Unipolar and Bipolar Inputs
±5 V, ±10 V, 0–10 V, 0–20 V Input Ranges
Commercial, Industrial and Military Temperature Range Grades
MIL-STD-883 and SMD Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1674 is a complete, multipurpose, 12-bit analog-to-digital converter, consisting of a user-transparent on-board sample-and-hold amplifier (SHA), 10 volt reference, clock and three-state output buffers for microprocessor interface.

The AD1674 is pin compatible with the industry standard AD574A and AD674A, but includes a sampling function while delivering a faster conversion rate. The on-chip SHA has a wide input bandwidth supporting 12-bit accuracy over the full Nyquist bandwidth of the converter.

The AD1674 is fully specified for ac parameters (such as S/(N+D) ratio, THD, and IMD) and dc parameters (offset, full-scale error, etc.). With both ac and dc specifications, the AD1674 is ideal for use in signal processing and traditional dc measurement applications.

The AD1674 design is implemented using Analog Devices' BiMOS II process allowing high performance bipolar analog circuitry to be combined on the same die with digital CMOS logic.

Five different temperature grades are available. The AD1674J and K grades are specified for operation over the 0°C to +70°C temperature range. The A and B grades are specified from −40°C to +85°C; the AD1674T grade is specified from −55°C to +125°C. The J and K grades are available in both 28-lead plastic DIP and SOIC. The A and B grade devices are available in 28-lead hermetically sealed ceramic DIP and 28-lead SOIC. The T grade is available in 28-lead hermetically sealed ceramic DIP.

*Protected by U. S. Patent Nos. 4,962,325; 4,250,445; 4,808,908; RE30586.

PRODUCT HIGHLIGHTS

Industry Standard Pinout: The AD1674 utilizes the pinout established by the industry standard AD574A and AD674A.

Integrated SHA: The AD1674 has an integrated SHA which supports the full Nyquist bandwidth of the converter. The SHA function is transparent to the user; no wait-states are needed for SHA acquisition.

DC and AC Specified: In addition to traditional dc specifications, the AD1674 is also fully specified for frequency domain ac parameters such as total harmonic distortion, signal-to-noise ratio and input bandwidth. These parameters can be tested and guaranteed as a result of the on-board SHA.

Analog Operation: The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 V and 0 to +20 V unipolar, −5 V to +5 V and −10 V to +10 V bipolar. The AD1674 operates on +5 V and ±12 V or ±15 V power supplies.

Flexible Digital Interface: On-chip multiple-mode three-state output buffers and interface logic allow direct connection to most microprocessors.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

DC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −15 V ± 10% or −12 V ± 5% unless otherwise noted)

Parameter	AD1674J Min	AD1674J Typ	AD1674J Max	AD1674K Min	AD1674K Typ	AD1674K Max	Units
RESOLUTION	12			12			Bits
INTEGRAL NONLINEARITY (INL)			±1			±1/2	LSB
DIFFERENTIAL NONLINEARITY (DNL) (No Missing Codes)	12			12			Bits
UNIPOLAR OFFSET[1] @ 25°C			±3			±2	LSB
BIPOLAR OFFSET[1] @ 25°C			±6			±4	LSB
FULL-SCALE ERROR[1, 2] @ 25°C (with Fixed 50 Ω Resistor from REF OUT to REF IN)		0.1	0.25		0.1	0.25	% of FSR
TEMPERATURE RANGE	0		+70	0		+70	°C
TEMPERATURE DRIFT[3]							
Unipolar Offset[2]			±2			±1	LSB
Bipolar Offset[2]			±2			±1	LSB
Full-Scale Error[2]			±6			±3	LSB
POWER SUPPLY REJECTION							
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2	LSB
V_{EE} = −15 V ± 1.5 V or −12 V ± 0.6 V			±2			±1	LSB
ANALOG INPUT							
Input Ranges							
Bipolar	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	Volts
	0		+20	0		+20	Volts
Input Impedance							
10 Volt Span	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	kΩ
POWER SUPPLIES							
Operating Voltages							
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−16.5		−11.4	−16.5		−11.4	Volts
Operating Current							
I_{LOGIC}		5	8		5	8	mA
I_{CC}		10	14		10	14	mA
I_{EE}		14	18		14	18	mA
POWER DISSIPATION		385	575		385	575	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output Current (Available for External Loads)[4] (External Load Should Not Change During Conversion)			2.0			2.0	mA

NOTES
[1]Adjustable to zero.
[2]Includes internal voltage reference error.
[3]Maximum change from 25°C value to the value at T_{min} or T_{max}.
[4]Reference should be buffered for ±12 V operation.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

DC SPECIFICATIONS (Continued)

Parameter	AD1674A Min	AD1674A Typ	AD1674A Max	AD1674B Min	AD1674B Typ	AD1674B Max	AD1674T Min	AD1674T Typ	AD1674T Max	Units
RESOLUTION	12			12			12			Bits
INTEGRAL NONLINEARITY (INL) @ 25°C			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY (DNL) (No Missing Codes)	12			12			12			Bits
UNIPOLAR OFFSET[1] @ 25°C			±2			±2			±2	LSB
BIPOLAR OFFSET[1] @ 25°C			±6			±3			±3	LSB
FULL-SCALE ERROR[1, 2] @ 25°C (with Fixed 50 Ω Resistor from REF OUT to REF IN)		0.1	0.25		0.1	0.125		0.1	0.125	% of FSR
TEMPERATURE RANGE	−40		+85	−40		+85	−55		+125	°C
TEMPERATURE DRIFT[3]										
Unipolar Offset[2]			±2			±1			±1	LSB
Bipolar Offset[2]			±2			±1			±2	LSB
Full-Scale Error[2]			±8			±5			±7	LSB
POWER SUPPLY REJECTION										
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15 V ± 1.5 V or −12 V ± 0.6 V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
POWER SUPPLIES										
Operating Voltages										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−16.5		−11.4	−16.5		−11.4	−16.5		−11.4	Volts
Operating Current										
I_{LOGIC}		5	8		5	8		5	8	mA
I_{CC}		10	14		10	14		10	14	mA
I_{EE}		14	18		14	18		14	18	mA
POWER DISSIPATION		385	575		385	575		385	575	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output Current (Available for External Loads)[4] (External Load Should Not Change During Conversion)			2.0			2.0			2.0	mA

SPECIFICATIONS

AC SPECIFICATIONS

(T_{min} to T_{max}, with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −15 V ± 10% or −12 V ± 5%, f_{SAMPLE} = 100 kSPS, f_{IN} = 10 kHz, stand-alone mode unless otherwise noted)[1]

Parameter	AD1674J/A Min	AD1674J/A Typ	AD1674J/A Max	AD1674K/B/T Min	AD1674K/B/T Typ	AD1674K/B/T Max	Units
Signal to Noise and Distortion (S/N+D) Ratio[2, 3]	69	70		70	71		dB
Total Harmonic Distortion (THD)[4]		−90	−82		−90	−82	dB
			0.008			0.008	%
Peak Spurious or Peak Harmonic Component		−92	−82		−92	−82	dB
Full Power Bandwidth		1			1		MHz
Full Linear Bandwidth		500			500		kHz
Intermodulation Distortion (IMD)[5]							
Second Order Products		−90	−80		−90	−80	dB
Third Order Products		−90	−80		−90	−80	dB
SHA (specifications are included in overall timing specifications)							
Aperture Delay		50			50		ns
Aperture Jitter		250			250		ps
Acquisition Time		1			1		µs

DIGITAL SPECIFICATIONS

(for all grades T_{min} to T_{max}, with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −15 V ± 10% or −12 V ± 5%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		+2.0	V_{LOGIC} +0.5 V	V
V_{IL}	Low Level Input Voltage		−0.5	+0.8	V
I_{IH}	High Level Input Current (V_{IN} = 5 V)	V_{IN} = V_{LOGIC}	−10	+10	µA
I_{IL}	Low Level Input Current (V_{IN} = 0 V)	V_{IN} = 0 V	−10	+10	µA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.5 mA	+2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		+0.4	V
I_{OZ}	High-Z Leakage Current	V_{IN} = 0 to V_{LOGIC}	−10	+10	µA
C_{OZ}	High-Z Output Capacitance			10	pF

NOTES

[1] f_{IN} amplitude = −0.5 dB (9.44 V p–p) 10 V bipolar mode unless otherwise noted. All measurements referred to −0 dB (9.997 V p–p) input signal unless otherwise noted.

[2] Specified at worst case temperatures and supplies after one minute warm-up.

[3] See Figures 12 and 13 of full-length data sheet for other input frequencies and amplitudes.

[4] See Figure 11 of full-length data sheet.

[5] fa = 9.08 kHz, fb = 9.58 kHz with f_{SAMPLE} = 100 kHz. See *Definition of Specifications* section and Figure 15.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

V_{EE} to Digital Common . . . . . 0 to −16.5 V
V_{LOGIC} to Digital Common . . . . . 0 to +7 V
Analog Common to Digital Common . . . . . ±1 V
Digital Inputs to Digital Common . . −0.5 V to V_{LOGIC} +0.5 V
Analog Inputs to Analog Common . . . . . V_{EE} to V_{CC}
20 V_{IN} to Analog Common . . . . . V_{EE} to +24 V
REF OUT . . . . . Indefinite Short to Common
. . . . . Momentary Short to V_{CC}
Lead Temperature, Soldering . . . . . 300°C, 10 sec
Storage Temperature . . . . . −65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

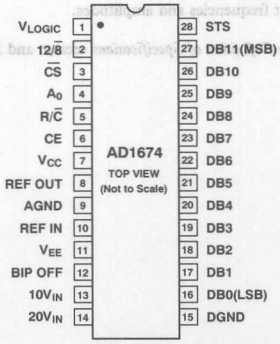
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

Model[1]	Temperature Range	INL (T_{min} to T_{max})	S/(N+D) (T_{min} to T_{max})	Package Description	Package Option[2]
AD1674JN	0°C to +70°C	±1 LSB	69 dB	Plastic DIP	N-28
AD1674KN	0°C to +70°C	±1/2 LSB	70 dB	Plastic DIP	N-28
AD1674JR	0°C to +70°C	±1 LSB	69 dB	Plastic SOIC	R-28
AD1674KR	0°C to +70°C	±1/2 LSB	70 dB	Plastic SOIC	R-28
AD1674AR	−40°C to +85°C	±1 LSB	69 dB	Plastic SOIC	R-28
AD1674BR	−40°C to +85°C	±1/2 LSB	70 dB	Plastic SOIC	R-28
AD1674AD	−40°C to +85°C	±1 LSB	69 dB	Ceramic DIP	D-28
AD1674BD	−40°C to +85°C	±1/2 LSB	70 dB	Ceramic DIP	D-28
AD1674TD	−55°C to +125°C	±1 LSB	70 dB	Ceramic DIP	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices *Military/Aerospace Reference Manual Products Databook* or current AD1674/883B data sheet. SMD is also available.
[2]N = Plastic DIP; D = Hermetic Ceramic DIP; R = Plastic SOIC. For outline information see Package Information section.

PIN CONFIGURATION

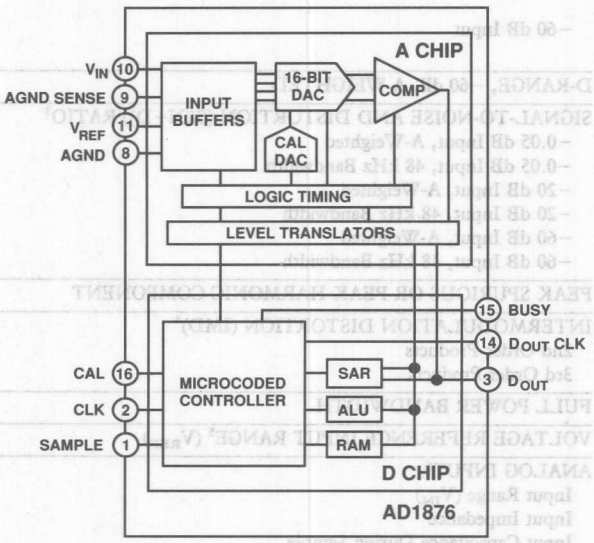


16-Bit 100 kSPS Sampling ADC

AD1876

FEATURES
Autocalibrating
0.002% THD
90 dB S/(N+D)
1 MHz Full Power Bandwidth
On-Chip Sample & Hold Function
2× Oversampling for Audio Applications
16-Pin DIP Package
Serial Twos Complement Output Format
Low Input Capacitance—typ 50 pF
AGND Sense for Improved Noise Immunity

FUNCTIONAL BLOCK DIAGRAM



PRODUCTION DESCRIPTION

The AD1876 is a 16-bit serial output sampling A/D converter which uses a switched capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 μs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The circuitry of the AD1876 is partitioned onto two monolithic chips, a digital control chip fabricated with Analog Devices' DSP CMOS process and an analog ADC chip fabricated with the BiMOS II process. Both chips are contained in a single package.

The serial output interface requires an external clock and sample command signal. The output data rate may be as high as 2.08 MHz, and is controlled by the external clock. The twos complement format of the output data is MSB first and is directly compatible with the NPC SM5805 digital decimation filter used in consumer audio products. The AD1876 is also compatible with a variety of DSP processors.

The AD1876 is packaged in a space saving 16-pin plastic DIP and operates from +5 V and ±12 V supplies; typical power consumption is 235 mW. The digital supply (V_{DD}) is isolated from the linear supplies (V_{EE} and V_{CC}) for reduced digital crosstalk. Separate analog and digital grounds are also provided.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD1876—SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD1876J Min	Typ	Max	Units
TEMPERATURE RANGE	0		70	°C
TOTAL HARMONIC DISTORTION (THD)[2]				
−0.05 dB Input		−95	**−88**	dB
		0.002	**0.004**	%
−20 dB Input		−78		dB
		0.01		%
−60 dB Input		−40		dB
		1.0		%
D-RANGE, −60 dB, A-WEIGHTED		92		dB
SIGNAL-TO-NOISE AND DISTORTION (S/(N+D)) RATIO[3]				
−0.05 dB Input, A-Weighted		92		dB
−0.05 dB Input, 48 kHz Bandwidth	**83**	90		dB
−20 dB Input, A-Weighted		73		dB
−20 dB Input, 48 kHz Bandwidth		70		dB
−60 dB Input, A-Weighted		34		dB
−60 dB Input, 48 kHz Bandwidth		31		dB
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−99	**−89**	dB
INTERMODULATION DISTORTION (IMD)[4]				
2nd Order Products		−102		dB
3rd Order Products		−98		dB
FULL POWER BANDWIDTH		1		MHz
VOLTAGE REFERENCE INPUT RANGE[5] (V_{REF})	3	5	10.0	V
ANALOG INPUT[6]				
Input Range (V_{IN})			±V_{REF}	V
Input Impedance		*		
Input Capacitance During Sample		50*		pF
Aperture Delay		6		ns
Aperture Jitter		100		ps
POWER SUPPLIES				
Operating Current				
I_{CC}		9	12	mA
I_{EE}		9	12	mA
I_{DD}		3	12	mA
Power Consumption		235	350	mW

NOTES

[1]V_{REF} = 5.00 V; conversion rate = 96 kSPS; f_{IN} = 1.06 kHz; V_{IN} = −0.05 dB unless otherwise indicated. All measurements referred to a 0 dB (10 V_{PP}) input signal. Values are post calibration.

[2]Includes first 19 harmonics.

[3]Minimum value of S/(N+D) corresponds to 5.0 V reference; typical values of S/(N+D) correspond to 10.0 V reference.

[4]f_a = 1008 Hz; f_b = 1055 Hz. See Definition of Specifications section and Figure 14.

[5]See Applications section for recommended voltage reference circuit and Figure 11 for performance with other reference voltage values.

[6]See Applications section for recommended input buffer circuit.

*For explanation of input characteristics, see "Analog Input" section.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test at worst case temperature. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

ORDERING GUIDE

Model	Temperature Range	THD dB	Package Description	Package Option*
AD1876JN	0°C to +70°C	−95	Plastic 16-Pin DIP	N-16

*N = Narrow Plastic DIP. For outline information see Package Information section.

DIGITAL SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.4			V
V_{IL}	Low Level Input Voltage		−0.3		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = V_{DD}$	−10		+10	μA
I_{IL}	Low Level Input Current	V_{IL} = 0 V	−10		+10	μA
C_{IN}	Input Capacitance				10	pF
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	V_{DD}−1 V			V
		I_{OH} = 0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA			0.4	V

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test at worst case temperature. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to V_{EE} . . . . . −0.3 V to +26.4 V
V_{DD} to DGND . . . . . −0.3 V to +7 V
V_{CC} to AGND . . . . . −0.3 V to +18 V
V_{EE} to AGND . . . . . −18 V to +0.3 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . 0 V to 5.5 V
Analog Inputs, V_{REF} to AGND . . . . . (V_{CC} + 0.3 V) to (V_{EE} −0.3 V)
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . −60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The AD1876 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD1876 has been classified as a Category 1 Device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment, and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam discharged to the destination socket before devices are removed. For further information on ESD precaution, refer to Analog Devices' *ESD Prevention Manual.*

TIMING SPECIFICATIONS[1] (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%, V_{REF} = 5.00 V)

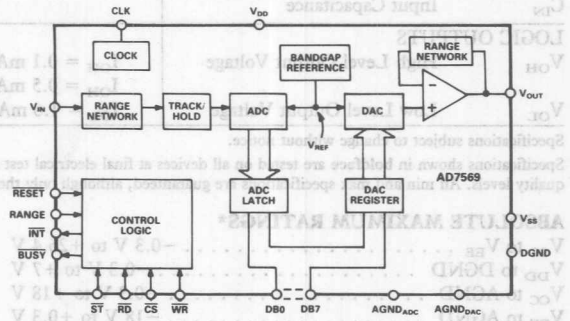
Parameter	Symbol	Min	Typ	Max	Units
Sampling Rate[2]	$f_S = 1/t_S$	1		100	kSPS
Sampling Period[2]	$t_S = 1/f_S$	10		1000	μs
Acquisition Time (Included in t_S)	t_A	2			μs
Calibration Time	t_{CT}			5000	t_C
CLK Period	t_C	480			ns
CAL to BUSY Delay	t_{CALB}	0			ns
CLK to BUSY Delay	t_{CB}	50	120	175	ns
CLK to D_{OUT} Hold Time	t_{CD}	10			ns
CLK HIGH	t_{CH}	160			ns
CLK LOW	t_{CL}	50			ns
D_{OUT} CLK LOW	t_{DCL}	30	80	200	ns
SAMPLE LOW to 1st CLK Delay	t_{SC}	50			ns
CAL HIGH Time	t_{CALH}	4			t_C
CLK to D_{OUT} CLK	t_{CDH}	150	200	275	ns
SAMPLE LOW	t_{SL}	50			ns

NOTES
[1]See Figure 1 and Figure 2 and the Conversion Control and Autocalibration sections for detailed explanations of the above timing.
[2]Depends upon external clock frequency; includes acquisition time and conversion time. The minimum sampling rate/maximum sampling period is specified to account for droop of the internal sample/hold. Operation at slower rates than specified may degrade performance.

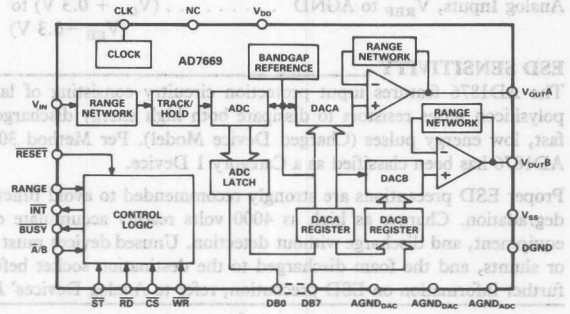
FEATURES

- **2µs ADC with Track/Hold**
- **1µs DAC with Output Amplifier**
  - **AD7569, Single DAC Output**
  - **AD7669, Dual DAC Output**
- **On-Chip Bandgap Reference**
- **Fast Bus Interface**
- **Single or Dual 5V Supplies**

AD7569 FUNCTIONAL BLOCK DIAGRAM



AD7669 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7569/AD7669 is a complete, 8-bit, analog I/O system on a single monolithic chip. The AD7569 contains a high speed successive approximation ADC with 2µs conversion time, a track/hold with 200kHz bandwidth, a DAC and output buffer amplifier with 1µs settling time. A temperature-compensated 1.25V bandgap reference provides a precision reference voltage for the ADC and the DAC. The AD7669 is similar but contains two DACs with output buffer amplifiers.

A choice of analog input/output ranges is available. Using a supply voltage of +5V, input and output ranges of zero to 1.25V and zero to 2.5 volts may be programmed using the RANGE input pin. Using a ±5V supply, bipolar ranges of ±1.25V or ±2.5V may be programmed.

Digital interfacing is via an 8-bit I/O port and standard microprocessor control lines. Bus interface timing is extremely fast, allowing easy connection to all popular 8-bit microprocessors. A separate start convert line controls the track/hold and ADC to give precise control of the sampling period.

The AD7569/AD7669 is fabricated in Linear-Compatible CMOS (LC^2MOS), an advanced, mixed technology process combining precision bipolar circuits with low power CMOS logic. The AD7569 is packaged in a 24-pin, 0.3" wide "skinny" DIP, a 24-terminal SOIC and 28-terminal PLCC and LCCC packages. The AD7669 is available in a 28-pin, 0.6" plastic DIP, 28-terminal SOIC, and 28-terminal PLCC package.

PRODUCT HIGHLIGHTS

1. Complete Analog I/O on a Single Chip.
   The AD7569/AD7669 provides everything necessary to interface a microprocessor to the analog world. No external components or user trims are required, and the overall accuracy of the system is tightly specified, eliminating the need to calculate error budgets from individual component specifications.
2. Dynamic Specifications for DSP Users.
   In addition to the traditional ADC and DAC specifications the AD7569/AD7669 is specified for AC parameters, including signal-to-noise ratio, distortion and input bandwidth.
3. Fast Microprocessor Interface.
   The AD7569/AD7669 has bus interface timing compatible with all modern microprocessors, with bus access and relinquish times less than 75ns and Write pulse width less than 80ns.

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SPECIFICATIONS

DAC SPECIFICATIONS[1]

(V_{DD} = +5V ±5%; V_{SS}[2] = RANGE = $AGND_{DAC}$ = $AGND_{ADC}$ = DGND = 0V; R_L = 2kΩ, C_L = 100pF to $AGND_{DAC}$ unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	AD7569 J, A Versions[3] AD7669 J Version	AD7569 K, B Versions	AD7569 S Version	AD7569 T Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution[4]	8	8	8	8	Bits	
Total Unadjusted Error[5]	±2	±2	±3	±3	LSB typ	
Relative Accuracy[5]	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity[5]	±1	±3/4	±1	±3/4	LSB max	Guaranteed Monotonic
Unipolar Offset Error						DAC data is all 0s; V_{SS} = 0V
@ 25°C	±2	±1.5	±2	±1.5	LSB max	Typical tempco is 10μV/°C for +1.25V range
T_{min} to T_{max}	±2.5	±2	±2.5	±2	LSB max	
Bipolar Zero Offset Error						DAC data is all 0s; V_{SS} = −5V
@ 25°C	±2	±1.5	±2	±1.5	LSB max	Typical tempco is 20μV/°C for ±1.25V range
T_{min} to T_{max}	±2.5	±2	±2.5	±2	LSB max	
Full-Scale Error[6] (AD7569 Only)						V_{DD} = 5V
@ 25°C	±2	±1	±2	±1	LSB max	
T_{min} to T_{max}	±3	±2	±4	±3	LSB max	
Full-Scale Error[6] (AD7669 Only)						V_{DD} = 5V
@ 25°C	±3				LSB max	
T_{min} to T_{max}	±4.5				LSB max	
DACA/DACB Full Scale Error Match[6] (AD7669 Only)	±2.5				LSB max	V_{DD} = 5V
ΔFull Scale/ΔV_{DD}, T_A = 25°C	0.5	0.5	0.5	0.5	LSB max	V_{OUT} = 2.5V; ΔV_{DD} = ±5%
ΔFull Scale/ΔV_{SS}, T_A = 25°C	0.5	0.5	0.5	0.5	LSB max	V_{OUT} = −2.5V; ΔV_{SS} = ±5%
Load Regulation at Full Scale	0.2	0.2	0.2	0.2	LSB max	R_L = 2kΩ to 0/C
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio[5] (SNR)	44	46	44	46	dB min	V_{OUT} = 20kHz full-scale sine wave with $f_{SAMPLING}$ = 400kHz
Total Harmonic Distortion[5] (THD)	48	48	48	48	dB max	V_{OUT} = 20kHz full-scale sine wave with $f_{SAMPLING}$ = 400kHz
Intermodulation Distortion[5] (IMD)	55	55	55	55	dB typ	fa = 18.4kHz, fb = 14.5kHz with $f_{SAMPLING}$ = 400kHz
ANALOG OUTPUT						
Output Voltage Ranges						
Unipolar	0 to +1.25/2.5				Volts	V_{DD} = +5V, V_{SS} = 0V
Bipolar	±1.25/±2.5				Volts	V_{DD} = +5V, V_{SS} = −5V
LOGIC INPUTS						
$\overline{CS}$, A/$\overline{B}$, $\overline{WR}$, RANGE, $\overline{RESET}$, DB0 – DB7						
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Leakage Current	10	10	10	10	μA max	V_{IN} = 0 to V_{DD}
Input Capacitance[7]	10	10	10	10	pF max	
DB0 – DB7						
Input Coding (Single Supply)			Binary			
Input Coding (Dual Supply)			2s Complement			
AC CHARACTERISTICS[7]						
Voltage Output Settling Time						Settling time to within ±1/2LSB of final value
Positive Full-Scale Change	2	2	2	2	μs max	Typically 1μs
Negative Full-Scale Change (Single Supply)	4	4	4	4	μs max	Typically 2μs
Negative Full-Scale Change (Dual Supply)	2	2	2	2	μs max	Typically 1μs
Digital-to-Analog Glitch Impulse[5]	15	15	15	15	nV secs typ	
Digital Feedthrough[5]	1	1	1	1	nV secs typ	
V_{IN} to V_{OUT} Isolation	60	60	60	60	dB typ	V_{IN} = ±2.5V, 50kHz Sine Wave
DAC to DAC Crosstalk[5] (AD7669 Only)	1				nV secs typ	
DACA to DACB Isolation[5] (AD7669 Only)	−70				dB max	
POWER REQUIREMENTS						
V_{DD} Range	4.75/5.25	4.75/5.25	4.75/5.25	4.75/5.25	Vmin/Vmax	For Specified Performance
V_{SS} Range (Dual Supplies)	−4.75/−5.25	−4.75/−5.25	−4.75/−5.25	−4.75/−5.25	Vmin/Vmax	Specified Performance also applies to V_{SS} = 0V for unipolar ranges.
I_{DD}						V_{OUT} = V_{IN} = 2.5V; Logic Inputs = 2.4V; CLK = 0.8V
(AD7569)	13	13	13	13	mA max	Output unloaded
(AD7669)	18				mA max	Outputs unloaded
I_{SS} (Dual Supplies)						V_{OUT} = V_{IN} = −2.5V; Logic Inputs = 2.4V; CLK = 0.8V
(AD7569)	4	4	4	4	mA max	Output unloaded
(AD7669)	6				mA max	Outputs unloaded
DAC/ADC MATCHING						
Gain Matching[6]						V_{IN} to V_{OUT} match with V_{IN} = ±2.5V, 20kHz sine wave
@25°C	1	1	1	1	% typ	
T_{min} to T_{max}	1	1	1	1	% typ	

NOTES

[1]Specifications apply to both DACs in the AD7669. V_{OUT} applies to both V_{OUT}A and V_{OUT}B of the AD7669.

[2]Except where noted, specifications apply for all output ranges including bipolar ranges with dual supply operation.

[3]Temperature ranges are as follows: J, K versions; 0 to +70°C
A, B versions; −40°C to +85°C
S, T versions; −55°C to +125°C

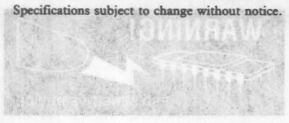
[4]1LSB = 4.88mV for 0 to +1.25V output range, 9.76mV for 0 to +2.5V and ±1.25V ranges and 19.5mV for ±2.5V range.

[5]See Terminology.

[6]Includes internal voltage reference error and is calculated after offset error has been adjusted out. Ideal unipolar full-scale voltage is (FS – 1LSB); ideal bipolar positive full-scale voltage is (FS/2 – 1LSB) and ideal bipolar negative full-scale voltage is −FS/2.

[7]Sample tested at 25°C to ensure compliance.

Specifications subject to change without notice.



AD7569/AD7669—SPECIFICATIONS

ADC SPECIFICATIONS

(V_{DD} = +5V ±5%; V_{SS}[1] = RANGE = $AGND_{DAC}$ = $AGND_{ADC}$ = DGND = 0V; f_{CLK} = 5MHz external unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated.) Specifications apply to Mode 1 interface.

Parameter	AD7569 J, A Versions[2] AD7669 J Version	AD7569 K, B Versions	AD7569 S Version	AD7569 T Version	Units	Conditions/Comments
DC ACCURACY						
Resolution[3]	8	8	8	8	Bits	
Total Unadjusted Error[4]	±3	±3	±4	±4	LSB typ	
Relative Accuracy[4]	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity[4]	±1	±3/4	±1	±3/4	LSB max	No Missing Codes
Unipolar Offset Error						Typical tempco is 10μV/°C for +1.25V range; V_{SS} = 0V
@25°C	±2	±1.5	±2	±1.5	LSB max	
T_{min} to T_{max}	±3	±2.5	±3	±2.5	LSB max	
Bipolar Zero Offset Error						Typical tempco is 20μV/°C for ±1.25V range; V_{SS} = −5V
@25°C	±3	±2.5	±3	±2.5	LSB max	
T_{min} to T_{max}	±3.5	±3	±4	±3.5	LSB max	
Full-Scale Error[5]						V_{DD} = 5V
@25°C	−4, +0	−4, +0	−4, +0	−4, +0	LSB max	
T_{min} to T_{max}	−5.5, +1.5	−5.5, +1.5	−7.5, +2	−7.5, +2	LSB max	
ΔFull Scale/ΔV_{DD}, T_A = 25°C	0.5	0.5	0.5	0.5	LSB max	V_{IN} = +2.5V; ΔV_{DD} = ±5%
ΔFull Scale/ΔV_{SS}, T_A = 25°C	0.5	0.5	0.5	0.5	LSB max	V_{IN} = −2.5V; ΔV_{SS} = ±5%
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio[4] (SNR)	44	46	44	45	dB min	V_{IN} = 100kHz full-scale sine wave with $f_{SAMPLING}$ = 400kHz[6]
Total Harmonic Distortion[4] (THD)	48	48	48	48	dB max	V_{IN} = 100kHz full-scale sine wave with $f_{SAMPLING}$ = 400kHz[6]
Intermodulation Distortion[4] (IMD)	60	60	60	60	dB typ	fa = 99kHz, fb = 96.7kHz with $f_{SAMPLING}$ = 400kHz
Frequency Response	0.1	0.1	0.1	0.1	dB typ	V_{IN} = ±2.5V, dc to 200kHz sine wave
Track/Hold Acquisition Time[7]	200	200	300	300	ns typ	
ANALOG INPUT						
Input Voltage Ranges						
Unipolar	0 to +1.25/+2.5				Volts	V_{DD} = +5V; V_{SS} = 0V
Bipolar	±1.25/±2.5				Volts	V_{DD} = +5V; V_{SS} = −5V
Input Current	±300	±300	±300	±300	μA max	See equivalent circuit Fig. 5
Input Capacitance	10	10	10	10	pF typ	
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, $\overline{ST}$, CLK, $\overline{RESET}$, RANGE						
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Capacitance[8]	10	10	10	10	pF max	
$\overline{CS}$, $\overline{RD}$, $\overline{ST}$, RANGE, $\overline{RESET}$						
Input Leakage Current	10	10	10	10	μA max	V_{IN} = 0 to V_{DD}
CLK						
Input Current						
I_{INL}	−1.6	−1.6	−1.6	−1.6	mA max	V_{IN} = 0V
I_{INH}	40	40	40	40	μA max	V_{IN} = V_{DD}
LOGIC OUTPUTS						
DB0–DB7, $\overline{INT}$, $\overline{BUSY}$						
V_{OL}, Output Low Voltage	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 200μA
DB0–DB7						
Floating State Leakage Current	10	10	10	10	μA max	
Floating State Output Capacitance[8]	10	10	10	10	pF max	
Output Coding (Single Supply)		Binary				
Output Coding (Dual Supply)		2s Complement				
CONVERSION TIME						
With External Clock	2	2	2	2	μs max	f_{CLK} = 5MHz
With Internal Clock, T_A = 25°C	1.6	1.6	1.6	1.6	μs min	Using recommended clock components shown in Figure 21. Clock frequency can be adjusted by varying R_{CLK}.
	2.6	2.6	2.6	2.6	μs max	
POWER REQUIREMENTS	As per DAC Specifications					

NOTES

[1]Except where noted, specifications apply for all ranges including bipolar ranges with dual supply operation.

[2]Temperature ranges are as follows: J, K versions; 0 to +70°C
A, B versions; −40°C to +85°C
S, T versions; −55°C to +125°C

[3]1LSB = 4.88mV for 0 to +1.25V range, 9.76mV for 0 to +2.5V and ±1.25V ranges and 19.5mV for ±2.5V range.

[4]See Terminology.

[5]Includes internal voltage reference error and is calculated after offset error has been adjusted out. Ideal unipolar last code transition occurs at (FS – 3/2LSB); Ideal bipolar last code transition occurs at (FS/2 – 3/2LSB).

[6]Exact frequencies are 101kHz and 384kHz to avoid harmonics coinciding with sampling frequency.

[7]Rising edge of $\overline{BUSY}$ to falling edge of $\overline{ST}$. The time given refers to the acquisition time which gives a 3dB degradation in SNR from the tested figure.

[8]Sample tested at 25°C to ensure compliance.

Specifications subject to change without notice.

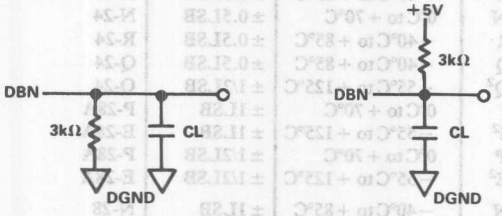
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TIMING CHARACTERISTICS[1] (See Figures 8, 10, 12; V_{DD} = 5V ±5%; V_{SS} = 0V or −5V ±5%)

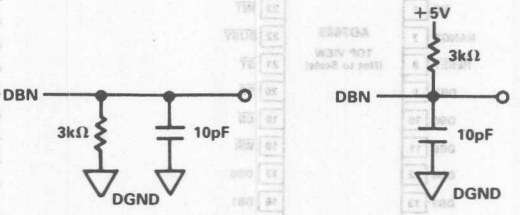
Parameter	Limit at 25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, A, B Grades)	Limit at T_{min}, T_{max} (S, T Grades)	Units	Test Conditions/Comments
DAC Timing					
t_1	80	80	90	ns min	$\overline{WR}$ Pulse Width
t_2	0	0	0	ns min	$\overline{CS}$, A/$\overline{B}$ to $\overline{WR}$ Setup Time
t_3	0	0	0	ns min	$\overline{CS}$, A/$\overline{B}$ to $\overline{WR}$ Hold Time
t_4	60	70	80	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5	10	10	10	ns min	Data Valid to $\overline{WR}$ Hold Time
ADC Timing					
t_6	50	50	50	ns min	$\overline{ST}$ Pulse Width
t_7	110	130	150	ns max	$\overline{ST}$ to $\overline{BUSY}$ Delay
t_8	20	30	30	ns max	$\overline{BUSY}$ to $\overline{INT}$ Delay
t_9	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Delay
t_{10}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_{11}	60	75	90	ns min	$\overline{RD}$ Pulse Width. Determined by t_{13}.
t_{12}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{13}[2]	60	75	90	ns max	Data Access Time after $\overline{RD}$; C_L = 20pF
	95	120	135	ns max	Data Access Time after $\overline{RD}$; C_L = 100pF
t_{14}[3]	10	10	10	ns min	Bus Relinquish Time after $\overline{RD}$
	60	75	85	ns max	
t_{15}	65	75	85	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_{16}	120	140	160	ns max	$\overline{RD}$ to $\overline{BUSY}$ Delay
t_{17}[2]	60	75	90	ns max	Data Valid Time after $\overline{BUSY}$; C_L = 20pF
	90	115	135	ns max	Data Valid Time after $\overline{BUSY}$; C_L = 100pF

NOTES
[1]Sample tested at +25°C to ensure compliance. All input control signals are specified with $t_R = t_F$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_{13} and t_{17} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross either 0.8V or 2.4V.
[3]t_{14} is defined as the time required for the data line to change 0.5V when loaded with the circuit of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 2. Load Circuits for Bus Relinquish Time Test

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to $AGND_{DAC}$ or $AGND_{ADC}$ . . . . . −0.3V, +7V
V_{DD} to DGND . . . . . −0.3V, +7V
V_{DD} to V_{SS} . . . . . −0.3V, +14V
$AGND_{DAC}$ or $AGND_{ADC}$ to DGND . . −0.3V, V_{DD} +0.3V
$AGND_{DAC}$ to $AGND_{ADC}$ . . . . . ±5V
Logic Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
CLK Input Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
V_{OUT} (V_{OUT}A, V_{OUT}B) to
$AGND^1_{DAC}$ . . . . . V_{SS} −0.3V, V_{DD}+0.3V
V_{IN} to $AGND_{ADC}$ . . . . . V_{SS} −0.3V, V_{DD} +0.3V

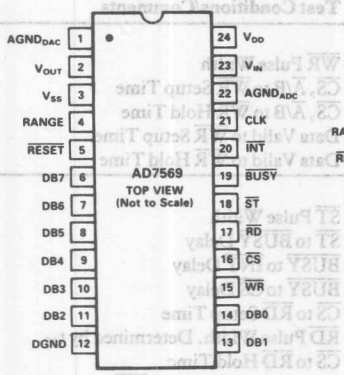
NOTE
[1]Output may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit current for a short to AGND or V_{SS} is 50mA.

Power Dissipation (Any Package) to +75°C 450mW
Derates above 75°C by . . . . . 6mW/°C
Operating Temperature Range
Commercial (J, K) . . . . . 0 to +70°C
Industrial (A, B) . . . . . −40°C to +85°C
Extended (S, T) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 Secs) . . . . . +300°C

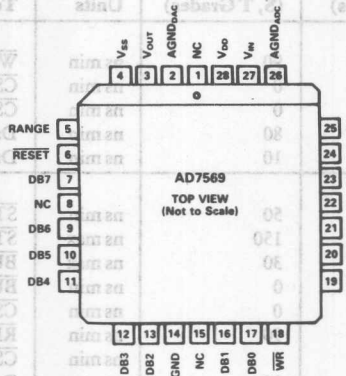
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AD7569 PIN CONFIGURATIONS

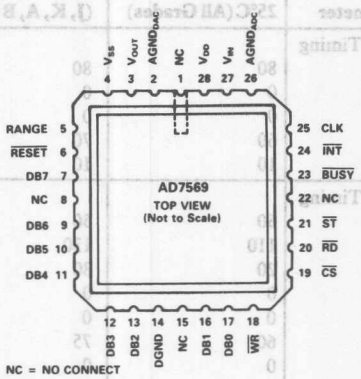
DIP, SOIC



PLCC



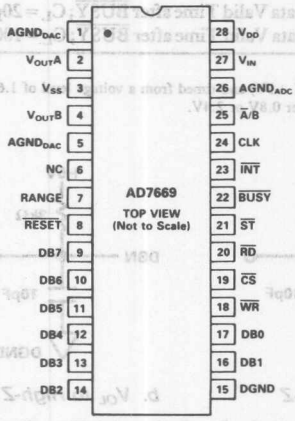
LCCC



NC = NO CONNECT

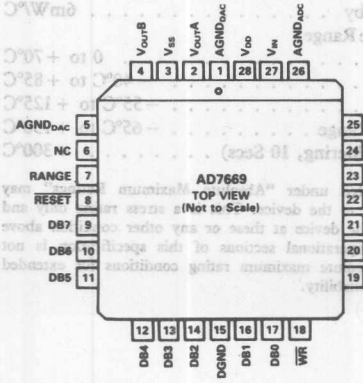
AD7669 PIN CONFIGURATIONS

DIP, SOIC



NC = NO CONNECT

PLCC



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy $T_{MIN}-T_{MAX}$	Package Option[1]
AD7569JN	0°C to +70°C	±1LSB	N-24
AD7569JR	0°C to +70°C	±1LSB	R-24
AD7569AQ	−40°C to +85°C	±1LSB	Q-24
AD7569SQ[2]	−55°C to +125°C	±1LSB	Q-24
AD7569BN	−40°C to +85°C	±0.5LSB	N-24
AD7569KN	0°C to +70°C	±0.5LSB	N-24
AD7569BR	−40°C to +85°C	±0.5LSB	R-24
AD7569BQ	−40°C to +85°C	±0.5LSB	Q-24
AD7569TQ[2]	−55°C to +125°C	±1/2LSB	Q-24
AD7569JP	0°C to +70°C	±1LSB	P-28A
AD7569SE[2]	−55°C to +125°C	±1LSB	E-28A
AD7569KP	0°C to +70°C	±1/2LSB	P-28A
AD7569TE[2]	−55°C to +125°C	±1/2LSB	E-28A
AD7669AN	−40°C to +85°C	±1LSB	N-28
AD7669JN	0°C to +70°C	±1LSB	N-28
AD7669JP	0°C to +70°C	±1LSB	P-28A
AD7669AR	−40°C to +85°C	±1LSB	R-28
AD7669JR	0°C to +70°C	±1LSB	R-28

NOTES

[1]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline SOIC. For outline information see Package Information section.

[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.

PIN FUNCTION DESCRIPTION

(Applies to the AD7569 and AD7669 unless otherwise stated.)

Pin Mnemonic	Description
$AGND_{DAC}$	Analog Ground for the DAC(s). Separate ground return paths are provided for the DAC(s) and ADC to minimize crosstalk.
V_{OUT} ($V_{OUT}A$, $V_{OUT}B$)	Output Voltage. V_{OUT} is the buffered output voltage from the AD7569 DAC. $V_{OUT}A$ and $V_{OUT}B$ are the buffered DAC output voltages from the AD7669. Four different output voltage ranges can be achieved (see Table I).
V_{SS}	Negative Supply Voltage ($-5V$ for dual supply or 0V for single supply). This pin is also used with the RANGE pin to select the different input/output ranges and changes the data format from binary ($V_{SS} = 0V$) to 2s complement ($V_{SS} = -5V$) (see Table I).
RANGE	Range Selection Input. This is used with the V_{SS} input to select the different ranges as per Table I. The range selected applies to both the analog input voltage of the ADC and the output voltage from the DAC(s).
$\overline{RESET}$	Reset Input (Active Low). This is an asynchronous system reset which clears the DAC register(s) to all 0s and clears the $\overline{INT}$ line of the ADC (i.e., makes the ADC ready for new conversion). In unipolar operation this input sets the output voltage to 0V; in bipolar operation it sets the output to negative full scale.
DB7	Data Bit 7. Most Significant Bit (MSB).
DB6–DB2	Data Bit 6 to Data Bit 2.
DGND	Digital Ground.
DB1	Data Bit 1.
DB0	Data Bit 0. Least Significant Bit (LSB).
$\overline{WR}$	Write Input (Edge triggered). This is used in conjunction with $\overline{CS}$ to write data into the AD7569 DAC register. It is used in conjunction with $\overline{CS}$ and $\overline{A}/B$ to write data into the selected DAC register of the AD7669. Data is transferred on the rising edge of $\overline{WR}$.

Pin Mnemonic	Description
$\overline{CS}$	Chip Select Input (Active Low). The device is selected when this input is active.
$\overline{RD}$	READ Input (Active Low). This input must be active to access data from the part. In the Mode 2 interface, $\overline{RD}$ going low starts conversion. It is used in conjunction with the $\overline{CS}$ input (see Digital Interface Section).
$\overline{ST}$	Start Conversion (Edge triggered). This is used when precise sampling is required. The falling edge of $\overline{ST}$ starts conversion and drives $\overline{BUSY}$ low. The $\overline{ST}$ signal is not gated with $\overline{CS}$.
$\overline{BUSY}$	BUSY Status Output (Active Low). When this pin is active the ADC is performing a conversion. The input signal is held prior to the falling edge of $\overline{BUSY}$ (see Digital Interface Section).
$\overline{INT}$	INTERRUPT Output (Active Low). $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ goes high on the rising edge of $\overline{CS}$ or $\overline{RD}$ and is also set high by a low pulse on $\overline{RESET}$ (see Digital Interface Section).
$\overline{A}/B$ (AD7669 Only)	DAC Select Input. This input selects which DAC register data is written to under control of $\overline{CS}$ and $\overline{WR}$. With this input low data is written to the DACA register; with this input high data is written to the DACB register.
CLK	A TTL compatible clock signal may be used to determine the ADC conversion time. Internal clock operation is achieved by connecting a resistor and capacitor to ground.
$AGND_{ADC}$	Analog Ground for the ADC.
V_{IN}	Analog Input. Various input ranges can be selected (see Table I).
V_{DD}	Positive Supply Voltage ($+5V$).

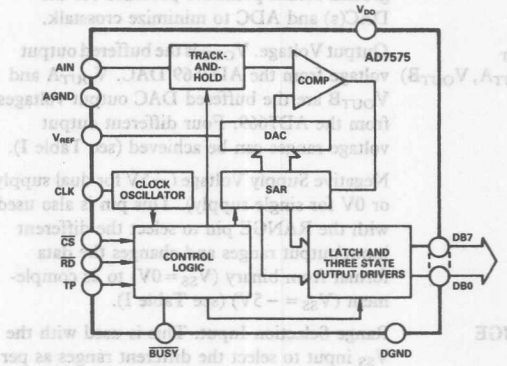
Range	V_{SS}	Input/Output Voltage Range	DB0–DB7 Data Format
0	0V	0 to +1.25V	Binary
1	0V	0 to +2.5V	Binary
0	−5V	±1.25V	2s Complement
1	−5V	±2.5V	2s Complement

Table I. Input/Output Ranges

FEATURES

Fast Conversion Time: 5µs
On-Chip Track/Hold
Low Total Unadjusted Error: 1LSB
Full Power Signal Bandwidth: 50kHz
Single +5V Supply
100ns Data Access Time
Low Power (15mW typ)
Low Cost
Standard 18-Pin DIPs or 20-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7575 is a high-speed 8-bit ADC with a built-in track/hold function. The successive approximation conversion technique is used to achieve a fast conversion time of 5µs, while the built-in track/hold allows full-scale signals up to 50kHz (386mV/µs slew rate) to be digitized. The AD7575 requires only a single +5V supply and a low-cost, 1.23V bandgap reference in order to convert an input signal range of 0 to $2V_{REF}$.

The AD7575 is designed for easy interfacing to all popular 8-bit microprocessors using standard microprocessor control signals ($\overline{CS}$ and $\overline{RD}$) to control starting of the conversion and reading of the data. The interface logic allows the AD7575 to be easily configured as a memory mapped device and the part can be interfaced as SLOW-MEMORY or ROM. All data outputs of the AD7575 are latched and three-state buffered to allow direct connection to a microprocessor data bus or I/O port.

The AD7575 is fabricated in an advanced, all ion-implanted high speed Linear Compatible CMOS (LC^2MOS) process and is available in a small, 0.3" wide, 18-pin DIP or in 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time/Low Power
   The fast, 5µs conversion time of the AD7575 makes it suitable for digitizing wideband signals at audio and ultrasonic frequencies, while retaining the advantage of low CMOS power consumption.
2. On-Chip Track/Hold
   The on-chip track/hold function is completely self-contained and requires no external hold capacitor. Signals with slew rates up to 386mV/µs (e.g., 2.46V peak-to-peak 50kHz sine waves) can be digitized with full accuracy.
3. Low Total Unadjusted Error
   The zero, full-scale and linearity errors of the AD7575 are so low that the total unadjusted error at any point on the transfer function is less than 1LSB and offset and gain adjustments are not required.
4. Single Supply Operation
   Operation from a single +5V supply with a low-cost +1.23V bandgap reference allows the AD7575 to be used in 5V microprocessor systems without any additional power supplies.
5. Fast Digital Interface
   Fast interface timing allows the AD7575 to interface easily to the fast versions of most popular microprocessors such as the Z80H, 8085A-2, 6502B, 68B09 and the DSP processor, the TMS32010.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +1.23V, AGND = DGND = 0V; f_{CLK} = 4MHz external; All specifications T_{min} to T_{max} unless otherwise specified)

Parameter	J, A Versions[1]	K, B Versions	S Version	T Version	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	
Relative Accuracy	±1	±½	±1	±½	LSB max	
Minimum Resolution for which						
No Missing Codes is Guaranteed	8	8	8	8	Bits max	
Full Scale Error						
25°C	±1	±1	±1	±1	LSB max	Full Scale TC is typically 5ppm/°C
T_{min} to T_{max}	±1	±1	±1	±1	LSB max	
Offset Error[2]						
25°C	±½	±½	±½	±½	LSB max	Offset TC is typically 5ppm/°C
T_{min} to T_{max}	±½	±½	±½	±½	LSB max	
ANALOG INPUT						
Voltage Range	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	Volts	1LSB = $2V_{REF}$/256; See Figure 16
DC Input Impedance	10	10	10	10	MΩ min	
Slew Rate, Tracking	0.386	0.386	0.386	0.386	V/μs max	
SNR[3]	45	45	45	45	dB min	V_{IN} = 2.46V p-p @ 10kHz; See Figure 11
REFERENCE INPUT						
V_{REF} (For specified Performance)	1.23	1.23	1.23	1.23	Volts	±5%
I_{REF}	500	500	500	500	μA max	
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{IN}, Input Current						
25°C	±1	±1	±1	±1	μA max	V_{IN} = 0 or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Input Capacitance[3]	10	10	10	10	pF max	
CLK						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{INL}, Input Low Current	700	700	800	800	μA max	V_{INL} = 0V
I_{INH}, Input High Current	700	700	800	800	μA max	V_{INH} = V_{DD}
LOGIC OUTPUTS						
$\overline{BUSY}$, DB0 to DB7						
V_{OL}, Output Low Voltage	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40μA
DB0 to DB7						
Floating State Leakage Current	±1	±1	±10	±10	μA max	V_{OUT} = 0 to V_{DD}
Floating State Output Capacitance[3]	10	10	10	10	pF max	
CONVERSION TIME[4]						
With External Clock	5	5	5	5	μs	f_{CLK} = 4MHz
With Internal Clock, T_A = 25°C	5	5	5	5	μs min	Using recommended clock
	15	15	15	15	μs max	components shown in Figure 15.
POWER REQUIREMENTS[5]						
V_{DD}	+5	+5	+5	+5	Volts	±5% for Specified Performance
I_{DD}	6	6	7	7	mA max	Typically 3mA with V_{DD} = +5V
Power Dissipation	15	15	15	15	mW typ	
Power Supply Rejection	±¼	±¼	±¼	±¼	LSB max	4.75V≤V_{DD}≤5.25V

NOTES

[1]Temperature Ranges are as follows:
J, K Versions; 0 to +70°C
A, B Versions; −25°C to +85°C
S, T Versions; −55°C to +125°C

[2]Offset error is measured with respect to an ideal first code transition which occurs at 1/2LSB.

[3]Sample tested at 25°C to ensure compliance.

[4]Accuracy may degrade at conversion times other than those specified.

[5]Power supply current is measured when AD7575 is inactive i.e. when $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = logic HIGH.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +5V, V_{REF} = +1.23V, AGND = DGND = 0V)

Parameter	Limit at +25°C (All Versions)	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (S, T Versions)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	100	100	120	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	100	100	120	ns max	Data Access Time after $\overline{RD}$
t_4	100	100	120	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	80	80	100	ns max	Data Access Time after $\overline{BUSY}$
t_7[3]	10	10	10	ns min	Data Hold Time
	80	80	100	ns max	
t_8	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Delay

NOTES

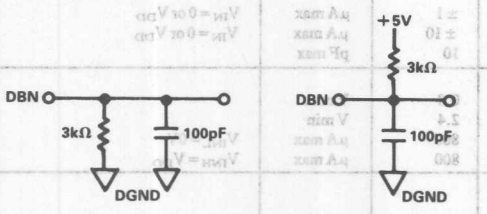
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

[3]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

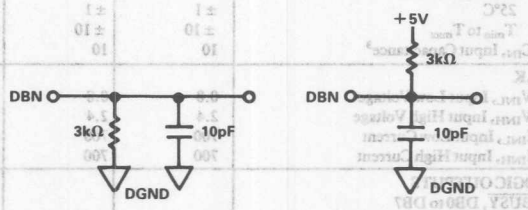
Specifications subject to change without notice.

Test Circuits



a. High-Z to V_{OH} b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

ABSOLUTE MAXIMUM RATINGS*

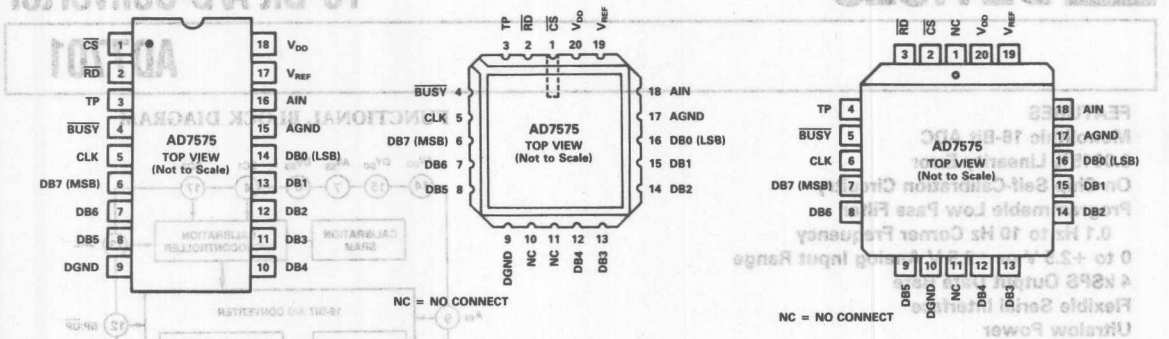
V_{DD} to AGND	−0.3V, +7V
V_{DD} to DGND	−0.3V, +7V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND	−0.3V, V_{DD} +0.3V
CLK Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD}
AIN to AGND	−0.3V, V_{DD}
Operating Temperature Range	
Commercial (J, K Versions)	0 to +70°C
Industrial (A, B Versions)	−25°C to +85°C
Extended (S, T Versions)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS



ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy (LSB)	Package Options[2]
AD7575JN	0 to +70°C	±1 max	N-18
AD7575KN	0 to +70°C	±1/2 max	N-18
AD7575JP	0 to +70°C	±1 max	P-20A
AD7575KP	0 to +70°C	±1/2 max	P-20A
AD7575AQ	−25°C to +85°C	±1 max	Q-18
AD7575BQ	−25°C to +85°C	±1/2 max	Q-18
AD7575SQ	−55°C to +125°C	±1 max	Q-18
AD7575TQ	−55°C to +125°C	±1/2 max	Q-18
AD7575SE	−55°C to +125°C	±1 max	E-20A
AD7575TE	−55°C to +125°C	±1/2 max	E-20A

NOTES
[1]To order MIL-STD-883, Class B process parts, add /883B to part number. Contact local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962-87762.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

An ADC with 8-bits resolution can resolve 1 part in 2^8 (i.e., 256) of full scale. For the AD7575 with +2.46V full scale one LSB is 9.61mV.

TOTAL UNADJUSTED ERROR

This is a comprehensive specification which includes full scale error, relative accuracy and offset error.

RELATIVE ACCURACY

Relative Accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the devices measured first LSB transition point and the measured full scale transition point.

SNR

Signal-to-Noise Ratio (SNR) is the ratio of the desired signal to the noise produced in the sampled and digitized analog signal. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave input is given by

$$SNR = (6.02N + 1.76)dB$$

where N is the number of bits in the ADC.

FULL SCALE ERROR (GAIN ERROR)

The gain of a unipolar ADC is defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation of the actual span from the ideal span of FS – 2LSB's.

ANALOG INPUT RANGE

With V_{REF} = +1.23V the maximum analog input voltage range is 0 to +2.46V. The output data in LSB's is related to the analog input voltage by the integer value of the following expression:

$$\text{Data (LSB's)} = \frac{256\ AIN}{2V_{REF}} + 0.5$$

SLEW RATE

Slew Rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error. Slew Rate limitations may restrict the analog signal bandwidth for full-scale analog signals below the bandwidth allowed from sampling theorem considerations.

FEATURES

Monolithic 16-Bit ADC
0.0015% Linearity Error
On-Chip Self-Calibration Circuitry
Programmable Low Pass Filter
0.1 Hz to 10 Hz Corner Frequency
0 to +2.5 V or ±2.5 V Analog Input Range
4 kSPS Output Data Rate
Flexible Serial Interface
Ultralow Power

APPLICATIONS

Industrial Process Control
Weigh Scales
Portable Instrumentation
Remote Data Acquisition

GENERAL DESCRIPTION

The AD7701 is a 16-bit ADC which uses a sigma delta conversion technique. The analog input is continuously sampled by an analog modulator whose mean output duty cycle is proportional to the input signal. The modulator output is processed by an on-chip digital filter with a six-pole Gaussian response, which updates the output data register with 16-bit binary words at word rates up to 4 kHz. The sampling rate, filter corner frequency and output word rate are set by a master clock input that may be supplied externally, or by a crystal-controlled on-chip clock oscillator.

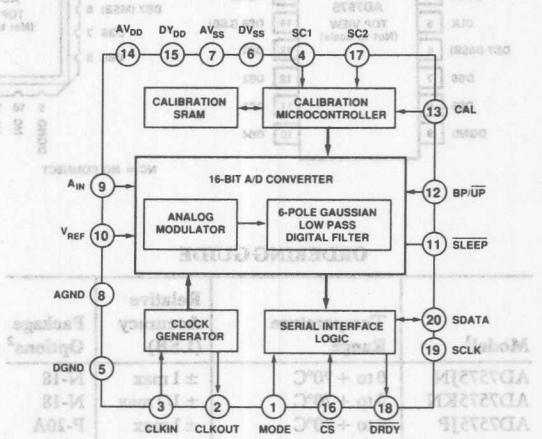
The inherent linearity of the ADC is excellent, and end-point accuracy is ensured by self-calibration of zero and full-scale which may be initiated at any time. The self-calibration scheme can also be extended to null system offset and gain errors in the input channel.

The output data is accessed through a flexible serial port, which has an asynchronous mode compatible with UARTs and two synchronous modes suitable for interfacing to shift registers or the serial ports of industry-standard microcontrollers.

CMOS construction insures low power dissipation, and a power down mode reduces the idle power consumption to only 10 μW.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. The AD7701 offers 16-bit resolution coupled with outstanding 0.0015% accuracy.
2. No missing codes ensures true, usable, 16-bit dynamic range, removing the need for programmable gain and level-setting circuitry.
3. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero and gain error. External circuits can also be included in the calibration loop to remove system offsets and gain errors.
4. A flexible synchronous/asynchronous interface allows the AD7701 to interface directly to UARTs or to the serial ports of industry-standard microcontrollers.
5. Low operating power consumption and an ultralow power standby mode make the AD7701 ideal for loop-powered remote sensing applications, or battery-powered portable instruments.

SPECIFICATIONS

(T_A = +25°C; AV_{DD} = DV_{DD} = +5 V; AV_{SS} = DV_{SS} = −5 V; V_{REF} = +2.5 V; f_{CLKIN} = 4.096 MHz; Bipolar Mode; MODE = +5 V; A_{IN} Source Resistance = 750 Ω[1] with 1 nF to AGND at A_{IN}, unless otherwise stated.)

Parameter	A, S Versions[2]	B, T Versions[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	16	16	Bits	
Integral Nonlinearity				
T_{min} to T_{max}		±0.0007	% FSR typ	
	±0.003	±0.0015	% FSR max	
Differential Nonlinearity				
T_{min} to T_{max}	±0.125	±0.125	LSB typ	Guaranteed No Missing Codes
	±0.5	±0.5	LSB max	
Positive Full-Scale Error[3]	±0.13	±0.13	LSB typ	
	±0.5	±0.5	LSB max	
Full-Scale Drift[4]	±1.2 (±2.3 S Version)	±1.2 (±2.3 T Version)	LSB typ	
Unipolar Offset Error[3]	±0.25	±0.25	LSB typ	
	±1	±1	LSB max	
Unipolar Offset Drift[4]	±1.6 (+3/−25 S Version)	±1.6 (+3/−25 T Version)	LSB typ	
Bipolar Zero Error[3]	±0.25	±0.25	LSB typ	
	±1	±1	LSB max	
Bipolar Zero Drift[4]	±0.8 (+1.5/−12.5 S Version)	±0.8 (+1.5/−12.5 T Version)	LSB typ	
Bipolar Negative Full-Scale Error[3]	±0.5	±0.5	LSB typ	
	±2	±2	LSB max	
Bipolar Negative Full-Scale Drift[4]	±0.6 (±1.2 S Version)	±0.6 (±1.2 T Version)	LSB typ	
Noise (Referred to Output)	0.1	0.1	LSB rms typ	
DYNAMIC PERFORMANCE				
Sampling Frequency, f_S	f_{CLKIN}/256	f_{CLKIN}/256	Hz	
Output Update Rate, f_{OUT}	f_{CLKIN}/1024	f_{CLKIN}/1024	Hz	
Filter Corner Frequency, $f_{-3\ dB}$	f_{CLKIN}/409,600	f_{CLKIN}/409,600	Hz	
Settling Time to ±0.0007% FS	507904/f_{CLKIN}	507904/f_{CLKIN}	sec	For Full-Scale Input Step
SYSTEM CALIBRATION				Applies to Unipolar and Bipolar Ranges. After Calibration, If $A_{IN} > V_{REF}$, the Device Will Output All 1s If $A_{IN} < 0$ (Unipolar) or $-V_{REF}$ (Bipolar), the Device Will Output All 0s.
Positive Full-Scale Overrange	V_{REF} +0.1	V_{REF} +0.1	V max	
Positive Full-Scale Overrange	V_{REF} +0.1	V_{REF} +0.1	V max	
Negative Full-Scale Overrange	−(V_{REF} +0.1)	−(V_{REF} +0.1)	V max	
Maximum Offset Calibration Range[5, 6]				
Unipolar Input Range	−(V_{REF} +0.1)	−(V_{REF} +0.1)	V max	
Bipolar Input Range	−0.4 V_{REF} to +0.4 V_{REF}	−0.4 V_{REF} to +0.4 V_{REF}	V max	
Input Span[7]	0.8 V_{REF}	0.8 V_{REF}	V min	
	2 V_{REF} +0.2	2 V_{REF} +0.2	V max	
ANALOG INPUT				
Unipolar Input Range	0 to +2.5	0 to +2.5	Volts	
Bipolar Input Range	±2.5	±2.5	Volts	
Input Capacitance	10	10	pF typ	
Input Bias Current[1]	1	1	nA typ	
LOGIC INPUTS				
All Inputs Except CLKIN				
V_{INL}, Input Low Voltage	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.0	2.0	V min	
CLKIN				
V_{INL}, Input Low Voltage	0.8	0.8	V max	
V_{INH}, Input High Voltage	3.5	3.5	V min	
I_{IN}, Input Current	10	10	μA max	
LOGIC OUTPUTS				
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	DV_{DD}−1	DV_{DD}−1	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	±10	μA max	
Floating State Output Capacitance	9	9	pF typ	

Parameter	A, S Versions[2]	B, T Versions[2]	Units	Test Conditions/Comments
POWER REQUIREMENTS[8]				
Power Supply Voltages				
Analog Positive Supply (AV_{DD})	4.5/5.5	4.5/5.5	Vmin/Vmax	
Digital Positive Supply (DV_{DD})	4.5/AV_{DD}	4.5/AV_{DD}	Vmin/Vmax	
Analog Negative Supply (AV_{SS})	−4.5/−5.5	−4.5/−5.5	Vmin/Vmax	
Digital Negative Supply (DV_{SS})	−4.5/−5.5	−4.5/−5.5	Vmin/Vmax	
Calibration Memory Retention				
Power Supply Voltage	2.0	2.0	V min	
DC Power Supply Currents[8]				
Analog Positive Supply (AI_{DD})	2.7	2.7	mA max	Typically 2 mA
Digital Positive Supply (DI_{DD})	2	2	mA max	Typically 1 mA
Analog Negative Supply (AI_{SS})	2.7	2.7	mA max	Typically 2 mA
Digital Negative Supply (DI_{SS})	0.1	0.1	mA max	Typically 0.03 mA
Power Supply Rejection[9]				
Positive Supplies	70	70	dB typ	
Negative Supplies	75	75	dB typ	
Power Dissipation				
Normal Operation	40	40	mW max	$\overline{SLEEP}$ = Logic 1, Typically 25 mW
Standby Operation[10]	20 (40 S Version)	20 (40 T Version)	μW max	$\overline{SLEEP}$ = Logic 0, Typically 10 μW

NOTES

[1]The A_{IN} pin presents a very high impedance dynamic load which varies with clock frequency.

[2]Temperature ranges are as follows: A, B Versions; −40°C to +85°C; S, T Versions; −55°C to +125°C.

[3]Apply after calibration at the temperature of interest. Full-scale error applies for both unipolar and bipolar input ranges.

[4]Total drift over the specified temperature range since calibration at power-up at +25°C. This is guaranteed by design and/or characterization. Recalibration at any temperature will remove these errors.

[5]In unipolar mode the offset can have a negative value ($-V_{REF}$) such that the unipolar mode can mimic bipolar mode operation.

[6]The specifications for input overrange and for input span apply additional constraints on the offset calibration range.

[7]For unipolar mode, input span is the difference between full-scale and zero scale. Fir bipolar mode, input span is the difference between positive and negative full-scale points. When using less than the maximum input span, the span range may be placed anywhere within the range of $\pm(V_{REF} + 0.1)$.

[8]All digital outputs unloaded. All digital inputs at 5 V CMOS levels.

[9]Applies in 0.1 Hz to 10 Hz bandwidth. PSRR at 60 Hz will exceed 120 dB due to the digital filter.

[10]CLKIN is stopped. All digital inputs are grounded.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to AV_{DD} . . . . . −0.3 V to +0.3 V
DV_{SS} to AGND . . . . . +0.3 V to −6 V
AV_{DD} to AGND . . . . . −0.3 V to +6 V
AV_{SS} to AGND . . . . . +0.3 V to −6 V
AGND to DGND . . . . . −0.3 V to +0.3 V
Digital Input Voltage to DGND . . . −0.3 V to DV_{DD} +0.3 V
Analog Input
  Voltage to AGND . . . . . AV_{SS} −0.3 V to AV_{DD} +0.3 V
Input Current to Any Pin Except Supplies[2] . . . . . ±10 mA
Operating Temperature Range
  Commercial Plastic (A, B Versions) . . . . . −40°C to +85°C
  Industrial Cerdip (A, B Versions) . . . . . −40°C to +85°C
  Extended Cerdip (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

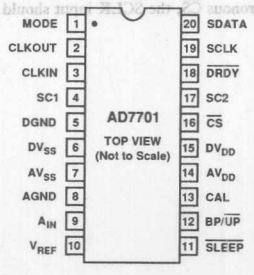
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	MODE	Selects the Serial Interface Mode. If MODE is tied to −5 V, the AD7701 will operate in the asynchronous communications (AC) mode. The SCLK pin is configured as an input, and data is transmitted in two bytes, each with one start bit and two stop bits. If MODE is tied to DGND, the synchronous external clocking (SEC) mode is selected. SCLK is configured as an input, and the output appears without formatting, the MSB coming first. If MODE is tied to +5 V, the AD7701 operates in the synchronous self-clocking (SSC) mode. SCLK is configured as an output, with a clock frequency of $f_{CLKIN}/4$ and 25% duty-cycle.
2	CLKOUT	Clock Output to generate an Internal Master Clock by connecting a crystal between CLKOUT and CLKIN. If an external clock is used, CLKOUT is not connected.
3	CLKIN	Clock Input for External Clock.
4, 17	SC1, SC2	System Calibration Pins. The state of these pins, when CAL is taken high, determines the type of calibration performed.
5	DGND	Digital Ground. Ground reference for all digital signals.
6	DV_{SS}	Digital Negative Supply, −5 V nominal.
7	AV_{SS}	Analog Negative Supply, −5 V nominal.
8	AGND	Analog Ground. Ground reference for all analog signals.
9	A_{IN}	Analog Input.
10	V_{REF}	Voltage Reference Input, +2.5 V nominal. This determines the value of positive full-scale in the unipolar mode and of both positive and negative full-scale in the bipolar mode.
11	$\overline{SLEEP}$	Sleep mode pin. When this pin is taken low, the AD7701 goes into a low-power mode with typically 10 μW power consumption.
12	BP/$\overline{UP}$	Bipolar/Unipolar Mode Pin. When this pin is low, the AD7701 is configured for a unipolar input range going from AGND to V_{REF}. When Pin 12 is high, the AD7701 is configured for a bipolar input range, $\pm V_{REF}$.
13	CAL	Calibration Mode Pin. When CAL is taken high for more than 4 cycles, the AD7701 is reset and performs a calibration cycle when CAL is brought low again. The CAL pin can also be used as a strobe to synchronize the operation of several AD7701s.
14	AV_{DD}	Analog Positive Supply, +5 V nominal.
15	DV_{DD}	Digital Positive Supply, +5 V nominal.
16	$\overline{CS}$	Chip Select Input. When $\overline{CS}$ is brought low, the AD7701 will begin to transmit serial data in a format determined by the state of the MODE pin.
18	$\overline{DRDY}$	Data Ready output. $\overline{DRDY}$ is low when valid data is available in the output register. It goes high after transmission of a word is completed. It also goes high for four clock cycles when a new data word is being loaded into the output register, to indicate that valid data is not available, irrespective of whether data transmission is complete or not.
19	SCLK	Serial Clock Input/Output. The SCLK pin in configured as an input or output, dependent on the type of serial data transmission that has been selected by the MODE pin. When configured as an output in the synchronous self-clocking mode, it has a frequency of $f_{CLKIN}/4$ and a duty cycle of 25%.
20	SDATA	Serial Data Output. The AD7701's output data is available at this pin as a 16-bit serial word. The transmission format is determined by the state of the MODE pin.

PIN CONFIGURATION



ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error (%FSR)	Package Options[2]
AD7701AN	−40°C to +85°C	0.003	N-20
AD7701BN	−40°C to +85°C	0.0015	N-20
AD7701AR	−40°C to +85°C	0.003	R-20
AD7701BR	−40°C to +85°C	0.0015	R-20
AD7701AQ	−40°C to +85°C	0.003	Q-20
AD7701BQ	−40°C to +85°C	0.0015	Q-20
AD7701SQ[3]	−55°C to +125°C	0.003	Q-20
AD7701TQ[3]	−55°C to +125°C	0.0015	Q-20

NOTES
[1]To order MIL-STD-883B, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[3]Available to /883B processing only.

Parameter	Limit at T_{min}, T_{max} (A, B Versions)	Limit at T_{min}, T_{max} (S, T Versions)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	40	40	kHz min	Master Clock Frequency: Internal Gate Oscillator
	5	5	MHz max	Typically 4.096 MHz
	40	40	kHz min	Master Clock Frequency: Externally Supplied
	5	5	MHz max	
t_r[5]	50	50	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	50	50	ns max	Digital Output Fall Time. Typically 20 ns
t_1	0	0	ns min	SC1, SC2 to CAL High Setup Time
t_2	50	50	ns min	SC1, SC2 Hold Time After CAL Goes High
t_3[6]	1000	1000	ns min	$\overline{SLEEP}$ High to CLKIN High Setup Time
SSC Mode				
t_4[7]	$3/f_{CLKIN}$	$3/f_{CLKIN}$	ns min	Data Access Time ($\overline{CS}$ Low to Data Valid)
t_5	100	100	ns max	SCLK Falling Edge to Data Valid Delay (25 ns typ)
t_6	250	250	ns min	MSB Data Setup Time. Typically 380 ns
t_7	300	300	ns max	SCLK High Pulse Width. Typically 240 ns
t_8	790	790	ns max	SCLK Low Pulse Width. Typically 730 ns
t_9[8]	$1/f_{CLKIN}$ +200	$1/f_{CLKIN}$ +200	ns max	SCLK Rising Edge to Hi-Z Delay ($1/f_{CLKIN}$ +100 ns typ)
t_{10}[8, 9]	$(4/f_{CLKIN})$ +200	$(4/f_{CLKIN})$ +200	ns max	$\overline{CS}$ High to Hi-Z Delay
SEC Mode				
f_{SCLK}	5	5	MHz	Serial Clock Input Frequency
t_{11}	50	50	ns min	SCLK Input High Pulse Width
t_{12}	180	180	ns min	SCLK Low Pulse Width
t_{13}[7, 10]	160	160	ns max	Data Access Time ($\overline{CS}$ Low to Data Valid). Typically 80 ns
t_{14}[11]	150	150	ns min	SCLK Falling Edge to Data Valid Delay. Typically 75 ns
t_{15}[8]	250	250	ns min	$\overline{CS}$ High to Hi-Z Delay
t_{16}[8]	200	200	ns min	SCLK Falling Edge to Hi-Z Delay. Typically 100 ns
AC Mode				
t_{17}	40	40	ns max	$\overline{CS}$ Setup Time. Typically 20 ns
t_{18}	180	180	ns max	Data Delay Time. Typically 90 ns
t_{19}	200	200	ns max	SCLK Falling Edge to Hi-Z Delay. Typically 100 ns

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 1 to 5.

[3]CLKIN Duty Cycle range is 20% to 80%. CLKIN must be supplied whenever the AD7701 is not in SLEEP mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7701 is production tested with f_{CLKIN} at 4.096 MHz. It is guaranteed by characterization to operate at 200 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]In order to synchronize several AD7701s together using the $\overline{SLEEP}$ pin, this specification is met.

[7]t_4 and t_{13} are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[8]t_8, t_{10}, t_{15} and t_{16} are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the Timing Characteristics is the true bus relinquish time of the part and as such as independent of external bus loading capacitance.

[9]If $\overline{CS}$ is returned high before all 16 bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

[10]If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for four clock cycles. The propagation delay time may be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asynchronous $\overline{CS}$, the SCLK input should not be taken high sooner then 4 CLKIN cycles plus 160 ns after $\overline{CS}$ goes low.

[11]SDATA is clocked out on the falling edge of the SCLK input.

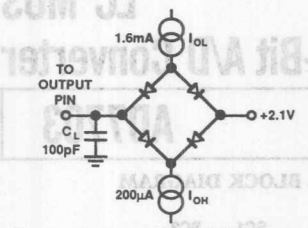
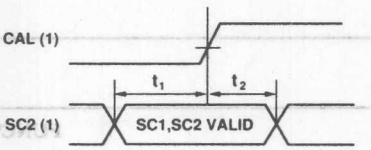
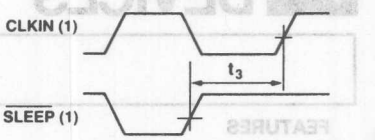


Figure 1. Load Circuit for Access Time and Bus Relinquish Time



2a. Calibration Control Timing



2b. $\overline{SLEEP}$ Mode Timing

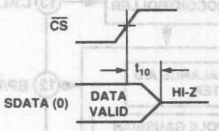


Figure 3. SSC Mode Data Hold Time

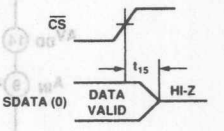


Figure 4a. SEC Mode Data Hold Time

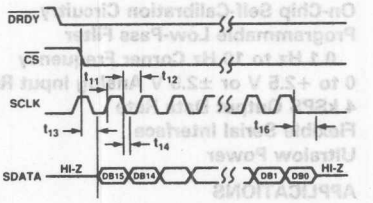


Figure 4b. SEC Mode Timing Diagram

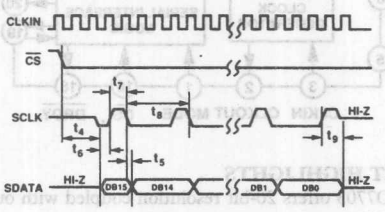


Figure 5. SSC Mode Timing Diagram

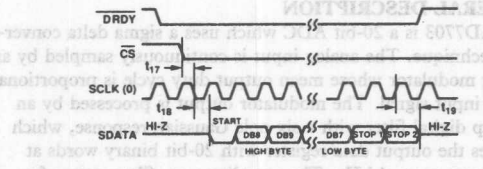


Figure 6. AC Mode Timing Diagram

TERMINOLOGY

LINEARITY ERROR

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are Zero-Scale (not to be confused with Bipolar Zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and Full-Scale, a point 1.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

DIFFERENTIAL LINEARITY ERROR

This is the difference between any code's actual width and the ideal (1 LSB) width. Differential Linearity Error is expressed in LSBs. A differential linearity specification of ±1 LSB or less guarantees monotonicity.

POSITIVE FULL-SCALE ERROR

Positive Full-Scale Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal (V_{REF} −3/2 LSBs). It applies to both positive and negative analog input ranges and it is expressed in microvolts.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the deviation of the first code transition from the ideal (AGND + 0.5 LSB) when operating in the unipolar mode. It is expressed in microvolts.

BIPOLAR ZERO ERROR

This is the deviation of the mid-scale transition (0111 . . . 111 to 1000 . . . 000) from the ideal (AGND − 0.5 LSB) when operating in the bipolar mode. It is expressed in microvolts.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal ($-V_{REF}$ + 0.5 LSB), when operating in the bipolar mode. It is expressed in microvolts.

POSITIVE FULL-SCALE OVERRANGE

Positive Full-Scale Overrange is the amount of overhead available to handle input voltages greater than $+V_{REF}$ (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter. It is expressed in millivolts.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages below $-V_{REF}$ without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks even in the unipolar mode. The overhead is expressed in millivolts.

LC²MOS 20-Bit A/D Converter

AD7703

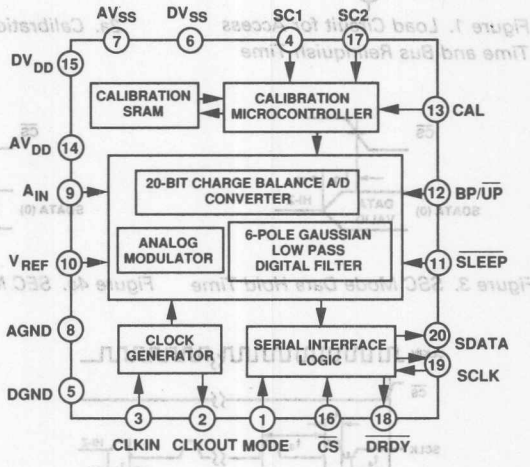
FEATURES

Monolithic 20-Bit ADC
0.0003% Linearity Error
20-Bit No Missed Codes
On-Chip Self-Calibration Circuitry
Programmable Low-Pass Filter
0.1 Hz to 10 Hz Corner Frequency
0 to +2.5 V or ±2.5 V Analog Input Range
4 kSPS Output Data Rate
Flexible Serial Interface
Ultralow Power

APPLICATIONS

Industrial Process Control
Weigh Scales
Portable Instrumentation
Remote Data Acquisition

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7703 is a 20-bit ADC which uses a sigma delta conversion technique. The analog input is continuously sampled by an analog modulator whose mean output duty cycle is proportional to the input signal. The modulator output is processed by an on-chip digital filter with a six-pole Gaussian response, which updates the output data register with 20-bit binary words at word rates up to 4 kHz. The sampling rate, filter corner frequency and output word rate are set by a master clock input that may be supplied externally, or by an on-chip gate oscillator.

The inherent linearity of the ADC is excellent, and endpoint accuracy is ensured by self-calibration of zero and full scale which may be initiated at any time. The self-calibration scheme can also be extended to null system offset and gain errors in the input channel.

The output data is accessed through a serial port, which has two synchronous modes suitable for interfacing to shift registers or the serial ports of industry standard microcontrollers.

CMOS construction ensures low power dissipation, and a power down mode reduces the idle power consumption to only 10 μW.

PRODUCT HIGHLIGHTS

1. The AD7703 offers 20-bit resolution coupled with outstanding 0.0003% accuracy.
2. No missing codes ensures true, usable, 20-bit dynamic range, removing the need for programmable gain and level-setting circuitry.
3. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero and gain error. External circuits can also be included in the calibration loop to remove system offsets and gain errors.
4. A flexible synchronization allows the AD7703 to interface directly to the serial ports of industry standard microcontrollers and DSP processors.
5. Low operating power consumption and an ultralow power standby mode make the AD7703 ideal for loop powered remote sensing applications, or battery-powered portable instruments.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

(T_A = +25°C; AV_{DD} = DV_{DD} = +5 V; AV_{SS} = DV_{SS} = −5 V; V_{REF} = +2.5 V; f_{CLKIN} = 4.096 MHz; BP/UP = +5 V; MODE = +5 V; A_{IN} Source Resistance = 750 Ω[1] with 1 nF to AGND at A_{IN} unless otherwise stated.)

Parameter	A/S Versions[2]	B Version[2]	C Version[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	20	20	20	Bits	
Integral Nonlinearity, T_{min} to T_{max}	±0.0015	±0.0007	±0.0003	% FSR typ	
+25°C	±0.003	±0.0015	±0.0008	% FSR max	
T_{min} to T_{max}	±0.003	±0.0015	±0.0012	% FSR max	
Differential Nonlinearity, T_{min} to T_{max}	±0.5	±0.5	±0.5	LSB typ	Guaranteed No Missing Codes
Positive Full-Scale Error[3]	±4	±4	±4	LSB typ	
	±16	±16	±16	LSB max	
Full-Scale Drift[4]	±19/±37	±19	±19	LSB typ	
Unipolar Offset Error[3]	±4	±4	±4	LSB typ	
	±16	±16	±16	LSB max	
Unipolar Offset Drift[4]	±26	±26	±26	LSB typ	Temp Range: 0 to +70°C
	±67 +48/−400	±67	±67	LSB typ	Specified Temp Range
Bipolar Zero Error[3]	±4	±4	±4	LSB typ	
	±16	±16	±16	LSB max	
Bipolar Zero Drift[4]	±13	±13	±13	LSB typ	Temp Range: 0 to +70°C
	±34 +24/−200	±34	±34	LSB typ	Specified Temp Range
Bipolar Negative Full-Scale Error[3]	±8	±8	±8	LSB typ	
	±32	±32	±32	LSB max	
Bipolar Negative Full-Scale Drift[4]	±10/±20	±10	±10	LSB typ	
Noise (Referred to Output)	1.6	1.6	1.6	LSB rms typ	
DYNAMIC PERFORMANCE					
Sampling Frequency, f_S	f_{CLKIN}/256	f_{CLKIN}/256	f_{CLKIN}/256	Hz	
Output Update Rate, f_{OUT}	f_{CLKIN}/1024	f_{CLKIN}/1024	f_{CLKIN}/1024	Hz	
Filter Corner Frequency, $f_{-3\ dB}$	f_{CLKIN}/409,600	f_{CLKIN}/409,600	f_{CLKIN}/409,600	Hz	
Settling Time to ±0.0007% FS	507904/f_{CLKIN}	507904/f_{CLKIN}	507904/f_{CLKIN}	sec	For Full-Scale Input Step
SYSTEM CALIBRATION					
Positive Full-Scale Calibration Range	V_{REF} + 0.1	V_{REF} + 0.1	V_{REF} + 0.1	V max	System Calibration Applies to
Positive Full-Scale Overrange	V_{REF} + 0.1	V_{REF} + 0.1	V_{REF} + 0.1	V max	Unipolar and Bipolar Ranges.
Negative Full-Scale Overrange	−(V_{REF} + 0.1)	−(V_{REF} + 0.1)	−(V_{REF} − + 0.1)	V max	After Calibration, if A_{IN}>V_{REF},
Maximum Offset Calibration Range[5, 6]					the Device Will Output All 1s.
Unipolar Input Range	−(V_{REF} + 0.1)	−(V_{REF} + 0.1)	−(V_{REF} + 0.1)	V max	If A_{IN}<0 (Unipolar) or −V_{REF}
Bipolar Input Range	−0.4 V_{REF} to +0.4 V_{REF}	−0.4 V_{REF} to +0.4 V_{REF}	−0.4 V_{REF} to +0.4 V_{REF}	V max	(Bipolar), the Device Will
Input Span[7]	0.8 V_{REF}	0.8 V_{REF}	0.8 V_{REF}	V min	Output all 0s
	2 V_{REF} + 0.2	2 V_{REF} + 0.2	2 V_{REF} + 0.2	V max	
ANALOG INPUT					
Unipolar Input Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Bipolar Input Range	±2.5	±2.5	±2.5	Volts	
Input Capacitance	20	20	20	pF typ	
Input Bias Current[1]	1	1	1	nA typ	
LOGIC INPUTS					
All Inputs except CLKIN					
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.0	2.0	2.0	V min	
CLKIN					
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	3.5	3.5	3.5	V min	
I_{IN}, Input Current	10	10	10	μA max	
LOGIC OUTPUTS					
V_{OL}, Output Low Voltage	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	DV_{DD}−1	DV_{DD}−1	DV_{DD}−1	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	±10	±10	μA max	
Floating State Output Capacitance	9	9	9	pF typ	
POWER REQUIREMENTS[8]					
Power Supply Voltages					
Analog Positive Supply (AV_{DD})	4.5/5.5	4.5/5.5	4.5/5.5	V min/V max	For Specified Performance
Digital Positive Supply (DV_{DD})	4.5/AV_{DD}	4.5/AV_{DD}	4.5/AV_{DD}	V min/V max	
Analog Negative Supply (AV_{SS})	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	V min/V max	
Digital Negative Supply (DV_{SS})	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	V min/V max	
Calibration Memory Retention					
Power Supply Voltage	2.0	2.0	2.0	V min	

Parameter	A/S Versions[2]	B Version[2]	C Version[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
DC Power Supply Currents[8]					
Analog Positive Supply (AI_{DD})	3.2	3.2	3.2	mA max	Typically 2 mA
Digital Positive Supply (DI_{DD})	1.5	1.5	1.5	mA max	Typically 1 mA
Analog Negative Supply (AI_{SS})	3.2	3.2	3.2	mA max	Typically 2 mA
Digital Negative Supply (DI_{SS})	0.1	0.1	0.1	mA max	Typically 0.03 mA
Power Supply Rejection[9]					
Positive Supplies	70	70	70	dB typ	
Negative Supplies	75	75	75	dB typ	
Power Dissipation					
Normal Operation	40	40	40	mW max	$\overline{SLEEP}$ = Logic 1, Typically 25 mW
Standby Operation[10]					$\overline{SLEEP}$ = Logic 0
A, B, C	20	20	20	μW max	Typically 10 μW
S	40	40	40	μW max	

NOTES

[1]The A_{IN} pin presents a very high impedance dynamic load which varies with clock frequency. A ceramic 1 nF capacitor from the A_{IN} to AGND is necessary. Source resistance should be 750 Ω or less.

[2]Temperature Ranges are as follows: A, B, C Versions: −40°C to +85°C; S Version: −55°C to +125°C.

[3]Applies after calibration at the temperature of interest. Full-Scale Error applies for both unipolar and bipolar input ranges.

[4]Total drift over the specified temperature range after calibration at power-up at +25°C. This is guaranteed by design and/or characterization. Recalibration at any temperature will remove these errors.

[5]In unipolar mode the offset can have a negative value ($-V_{REF}$) such that the unipolar mode can mimic bipolar mode operation.

[6]The specifications for input overrange and for input span apply additional constraints on the offset calibration range.

[7]For unipolar mode, input span is the difference between full scale and zero scale. For bipolar mode, input span is the difference between positive and negative full-scale points. When using less than the maximum input span, the span range may be placed anywhere within the range of $\pm(V_{REF} + 0.1)$.

[8]All digital outputs unloaded. All digital inputs at 5 V CMOS levels.

[9]Applies in 0.1 Hz to 10 Hz bandwidth. PSRR at 60 Hz will exceed 120 dB due to the digital filter.

[10]CLKIN is stopped. All digital inputs are grounded.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to AV_{DD} . . . . . −0.3 V to +0.3 V
DV_{SS} to AGND . . . . . +0.3 V to −6 V
AV_{DD} to AGND . . . . . −0.3 V to +6 V
AV_{SS} to AGND . . . . . +0.3 V to −6 V
AGND to DGND . . . . . −0.3 V to +0.3 V
Digital Input Voltage to DGND . . . −0.3 V to DV_{DD} + 0.3 V
Analog Input Voltage to AGND . . . . . AV_{SS} −0.3 V to AV_{DD} + 0.3 V
Input Current to any Pin Except Supplies[1] . . . . . ±10 mA
Operating Temperature Range
Industrial (A, B, C Versions) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (DIP Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C
Power Dissipation (SOIC Package) to +75°C . . . . . 250 mW
Derates above +75°C by . . . . . 15 mW/°C

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (% FSR)	Package Option[1]
AD7703AN	−40°C to +85°C	0.003	N-20
AD7703BN	−40°C to +85°C	0.0015	N-20
AD7703CN	−40°C to +85°C	0.0012	N-20
AD7703AR	−40°C to +85°C	0.003	R-20
AD7703BR	−40°C to +85°C	0.0015	R-20
AD7703CR	−40°C to +85°C	0.0012	R-20
AD7703AQ	−40°C to +85°C	0.003	Q-20
AD7703BQ	−40°C to +85°C	0.0015	Q-20
AD7703CQ	−40°C to +85°C	0.0012	Q-20
AD7703SQ[2]	−55°C to +125°C	0.003	Q-20

NOTES

[1]N = Plastic DIP; R = SOIC; Q = Cerdip. For outline information see Package Information section.

[2]Available to /883B processing only. Contact local sales office for military data sheet.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TIMING CHARACTERISTICS[1, 2] (AV_{DD} = DV_{DD} = +5 V ± 10%; AV_{SS} = DV_{SS} = −5 V ± 10%; AGND = DGND = 0 V; f_{CLKIN} = 4.096 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD}; unless otherwise stated.)

Parameter	Limit at T_{min}, T_{max} (A, B, C Versions)	Limit at T_{min}, T_{max} (S Version)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	40	40	kHz min	Master Clock Frequency: Internal Gate Oscillator
	5	5	MHz max	Typically 4096 kHz
	40	40	kHz min	Master Clock Frequency: Externally Supplied
	5	5	MHz max	
t_r[5]	50	50	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	50	50	ns max	Digital Output Fall Time. Typically 20 ns
t_1	0	0	ns min	SC1, SC2 to CAL High Setup Time
t_2	50	50	ns min	SC1, SC2 Hold Time After CAL Goes High
t_3[6]	1000	1000	ns min	$\overline{SLEEP}$ High to CLKIN High Setup Time
SSC MODE				
t_4[7]	$3/f_{CLKIN}$	$3/f_{CLKIN}$	ns min	Data Access Time ($\overline{CS}$ Low to Data Valid)
t_5	100	100	ns max	SCLK Falling Edge to Data Valid Delay (25 ns typ)
t_6	250	250	ns min	MSB Data Setup Time. Typically 380 ns
t_7	300	300	ns max	SCLK High Pulse Width. Typically 240 ns
t_8	790	790	ns max	SCLK Low Pulse Width. Typically 730 ns
t_9	$1/f_{CLKIN}$ + 200	$1/f_{CLKIN}$ + 200	ns max	SCLK Rising Edge to Hi-Z Delay ($1/f_{CLKIN}$ + 100 ns typ)
t_{10}[8, 9]	$4/f_{CLKIN}$ + 200	$4/f_{CLKIN}$ + 200	ns max	$\overline{CS}$ High to Hi-Z Delay
SEC MODE				
f_{SCLK}	5	5	MHz max	Serial Clock Input Frequency
t_{11}	50	50	ns min	SCLK High Pulse Width
t_{12}	180	180	ns min	SCLK Low Pulse Width
t_{13}[7, 10]	160	160	ns max	Data Access Time ($\overline{CS}$ Low to Data Valid). Typically 80 ns
t_{14}[11]	150	150	ns min	SCLK Falling Edge to Data Valid Delay. Typically 75 ns
t_{15}[8]	250	250	ns min	$\overline{CS}$ High to Hi-Z Delay
t_{16}[8]	200	200	ns min	SCLK Falling Edge to Hi-Z Delay. Typically 100 ns

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 1 to 6.

[3]CLKIN duty cycle range is 20% to 80%. CLKIN must be supplied whenever the AD7703 is not in SLEEP mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7703 is production tested with f_{CLKIN} at 4.096 MHz. It is guaranteed by characterization to operate at 200 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]In order to synchronize several AD7703s together using the $\overline{SLEEP}$ pin, this specification must be met.

[7]t_4 and t_{13} are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[8]t_9, t_{10}, t_{15} and t_{16} are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the Timing Characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

[9]If $\overline{CS}$ is returned high before all 20 bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

[10]If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for four clock cycles. The propagation delay time may be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asynchronous $\overline{CS}$, The SCLK input should not be taken high sooner than 4 CLKIN cycles plus 160 ns after $\overline{CS}$ goes low.

[11]SDATA is clocked out on the falling edge of the SCLK input.

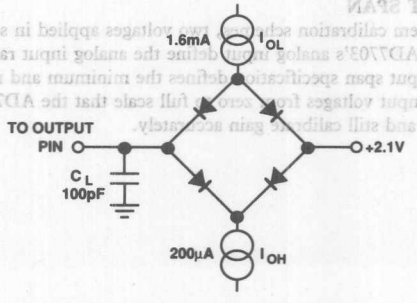


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

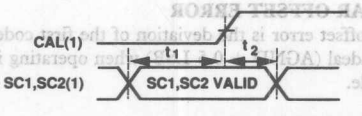


Figure 2. Calibration Control Timing

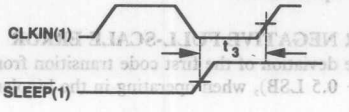


Figure 3. Sleep Mode Timing

Figure 4. SSC Mode Data Hold Time

Figure 5a. SEC Mode Data Hold Time

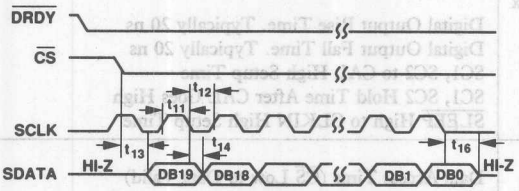


Figure 5b. SEC Mode Timing Diagram

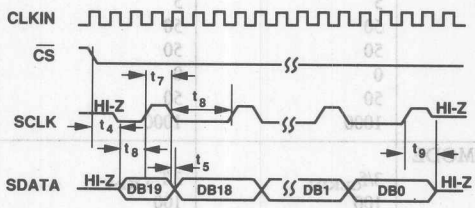


Figure 6. SSC Mode Timing Diagram

TERMINOLOGY

LINEARITY ERROR

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero-scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 1.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

DIFFERENTIAL LINEARITY ERROR

This is the difference between any code's actual width and the ideal (1 LSB) width. Differential linearity error is expressed in LSBs. A differential linearity specification of ±1 LSB or less guarantees monotonicity.

POSITIVE FULL-SCALE ERROR

Positive full-scale error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal (V_{REF} − 3/2 LSBs). It applies to both positive and negative analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar offset error is the deviation of the first code transition from the ideal (AGND + 0.5 LSB) when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal (AGND − 0.5 LSB) when operating in the bipolar mode.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal ($-V_{REF}$ + 0.5 LSB), when operating in the bipolar mode.

POSITIVE FULL-SCALE OVERRANGE

Positive full-scale overrange is the amount of overhead available to handle input voltages greater than $+V_{REF}$ (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages below $-V_{REF}$ without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks even in the unipolar mode.

OFFSET CALIBRATION RANGE

In the system calibration modes (SC2 Low) the AD7703 calibrates its offset with respect to the A_{IN} pin. The offset calibration range specification defines the range of voltages that the AD7701 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7703 can accept in the system calibration mode and still calibrate full scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7703's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7703 can accept and still calibrate gain accurately.

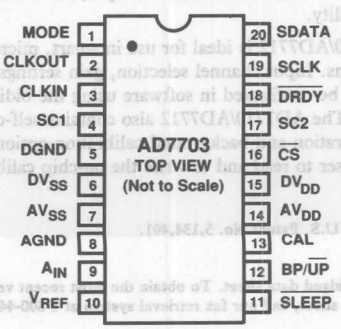
PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	MODE	Selects the Serial Interface Mode. If MODE is tied to DGND, the Synchronous External Clocking (SEC) mode is selected. SCLK is configured as an input, and the output appears without formatting, the MSB coming first. If MODE is tied to +5 V, the AD7703 operates in the Synchronous Self-Clocking (SSC) mode. SCLK is configured as an output, with a clock frequency of $f_{CLKIN}/4$ and 25% duty cycle.
2	CLKOUT	Clock Output to generate an Internal Master Clock by connecting a crystal between CLKOUT and CLKIN. If an external clock is used, CLKOUT is left open circuit.
3	CLKIN	Clock Input for External Clock.
4, 17	SC1, SC2	System Calibration Pins. The state of these pins, when CAL is taken high, determines the type of calibration performed.
5	DGND	Digital Ground. Ground reference for all digital signals.
6	DV_{SS}	Digital Negative Supply, −5 V nominal.
7	AV_{SS}	Analog Negative Supply, −5 V nominal.
8	AGND	Analog Ground. Ground reference for all analog signals.
9	A_{IN}	Analog Input.
10	V_{REF}	Voltage Reference Input, +2.5 V nominal. This determines the value of positive full scale in the unipolar mode and of both positive and negative full-scale in the Bipolar Mode.
11	$\overline{SLEEP}$	Sleep mode pin. When this pin is taken Low, the AD7703 goes into a low-power mode with typically 10 μW power consumption.
12	BP/$\overline{UP}$	Bipolar/Unipolar mode pin. When this pin is low the AD7703 is configured for a unipolar input range of AGND to V_{REF}. When Pin 12 is High, the AD7703 is configured for a bipolar input range, $\pm V_{REF}$.
13	CAL	Calibration mode pin. When CAL is taken High for more than 4 master clock cycles, the AD7703 is reset and performs a calibration cycle when CAL is brought Low again. The CAL pin can also be used as a strobe to synchronize the operation of several AD7703s.
14	AV_{DD}	Analog Positive Supply, +5 V nominal.
15	DV_{DD}	Digital Positive Supply, +5 V nominal.
16	$\overline{CS}$	Chip Select Input. When $\overline{CS}$ is brought low, the AD7703 will begin to transmit serial data in a format determined by the state of the MODE pin.
18	$\overline{DRDY}$	Data Ready Output. $\overline{DRDY}$ is low when valid data is available in the output register. It goes High after transmission of a word is completed. It also goes High for four clock cycles when a new data word is being loaded into the output register, to indicate that valid data is not available, irrespective of whether data transmission is complete or not.
19	SCLK	Serial Clock Input/Output. The SCLK pin in configured as an input or output, dependent on the type of serial data transmission that has been selected by the MODE pin. When configured as an output in the Synchronous Self-Clocking mode, it has a frequency of $f_{CLKIN}/4$ and a duty cycle of 25%.
20	SDATA	Serial Data Output. The AD7703's output data is available at this pin as a 20-bit serial word.

	UNIPOLAR MODE			BIPOLAR MODE		
μV	LSBs	% FS	ppm FS	LSBs	% FS	ppm FS
0.596	0.25	0.0000238	0.24	0.13	0.0000119	0.12
1.192	0.5	0.0000477	0.48	0.26	0.0000238	0.24
2.384	1.00	0.0000954	0.95	0.5	0.0000477	0.48
4.768	2.00	0.0001907	1.91	1.00	0.0000954	0.95
9.537	4.00	0.0003814	3.81	2.00	0.0001907	1.91

Table I. Bit Weight Table (2.5 V Reference Voltage)

PIN CONFIGURATION



LC²MOS Signal Conditioning ADCs

AD7710/AD7712*

FEATURES

Charge Balancing ADC
- 24 Bits No Missing Codes
- ±0.0015% Nonlinearity

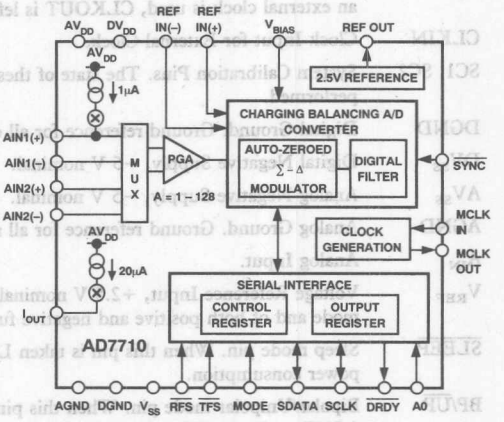
Two-Channel Programmable Gain Front End
- Gains from 1 to 128
- Differential Input for Low Level Channels
- High-Level Input on AD7712

Low-Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
Bidirectional Microcontroller Serial Interface
Internal/External Reference Option
Single or Dual Supply Operation
Low Power (25 mW typ) with Power-Down Mode

APPLICATIONS

Weigh Scales
Thermocouples
Process Control
Smart Transmitters
Portable Industrial Instruments

AD7710 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7710/AD7712 is a complete analog front end for low frequency measurement applications. The device has two analog input channels and accepts either low level signals directly from a transducer or high level ($\pm 4 \times V_{REF}$ for AD7712 AIN2) signals and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The input signals are applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

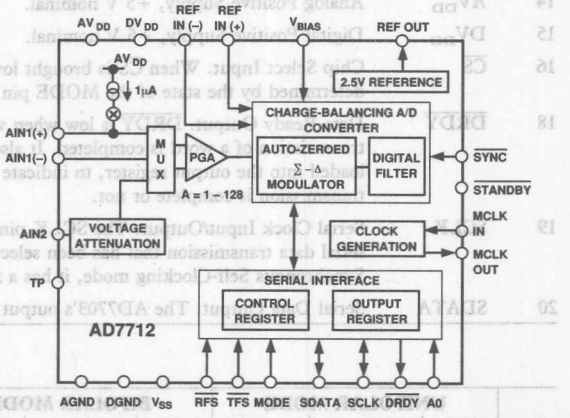
Normally, one of the channels will be used as the main channel with the second channel used as an auxiliary input to periodically measure a second voltage. The part can be operated from a single supply (by tying the V_{SS} pin to AGND) provided that the input signals on the low level analog inputs are more positive than −30 mV. By taking the V_{SS} pin negative, the part can convert signals down to $-V_{REF}$ on the low level inputs. The low-level inputs, as well as the reference input, features differential input capability.

The AD7710/AD7712 is ideal for use in smart, microcontroller-based systems. Input channel selection, gain settings and signal polarity can be configured in software using the bidirectional serial port. The AD7710/AD7712 also contains self-calibration, system calibration and background calibration options and also allows the user to read and to write the on-chip calibration registers.

***Protected by U.S. Patent No. 5,134,401.**

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7712 FUNCTIONAL BLOCK DIAGRAM



CMOS construction ensures low power dissipation and a power-down mode reduces the standby power consumption to only 100 μW typical (AD7712) and 7 μW typical (AD7710). The part is available in a 24-pin, 0.3 inch wide, plastic and hermetic dual-in-line package (DIP) as well as a 24-lead small outline (SOIC) package.

AD7712–SPECIFICATIONS

(AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; V_{SS} = 0 V or −5 V ± 5%; REF IN(+) = +2.5 V; REF IN(−) = AGND; MCLK IN = 10 MHz unless otherwise stated. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. For Filter Notches ≤ 60 Hz
	22	Bits min	For Filter Notch = 100 Hz
	18	Bits min	For Filter Notch = 250 Hz
	15	Bits min	For Filter Notch = 500 Hz
	12	Bits min	For Filter Notch = 1 kHz
Output Noise	See Tables I & II		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity			
@ 25°C	±0.0045	% of FSR max	Filter Notches ≤ 60 Hz; Typically ±0.0015%
T_{MIN} to T_{MAX}	±0.0075	% of FSR max	Filter Notches ≤ 60 Hz
Positive Full-Scale Error[2, 3]	See Note 4		Excluding Reference
Full-Scale Drift[5]	3/GAIN	µV/°C typ	Excluding Reference. For Gains of 1, 2, 4, 8
	0.35	µV/°C typ	Excluding Reference. For Gains of 16, 32, 64, 128
Unipolar Offset Error[2]	See Note 4		
Unipolar Offset Drift[5]	2.5/GAIN	µV/°C typ	For Gains of 1, 2, 4, 8
	0.3	µV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Zero Error[2]	See Note 4		
Bipolar Zero Drift[5]	2.5/GAIN	µV/°C typ	For Gains of 1, 2, 4, 8
	0.3	µV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Negative Full-Scale Error[2]	±0.006	% of FSR max	Excluding Reference; Typically ±0.0015%
Bipolar Negative Full-Scale Drift[5]	4/GAIN	µV/°C typ	Excluding Reference. For Gains of 1, 2, 4, 8
	0.5	µV/°C typ	Excluding Reference. For Gains of 16, 32, 64, 128
ANALOG INPUTS/REFERENCE INPUTS			
Normal Mode 50 Hz Rejection[6]	100	dB min	For Filter Notches of 10 Hz, 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Normal Mode 60 Hz Rejection[6]	100	dB min	For Filter Notches of 10 Hz, 30 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
AIN1/REF IN			
DC Input Leakage Current[6] @ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[6]	20	pF max	
Common-Mode Rejection (CMR)	92	dB min	At DC
Common-Mode 50 Hz Rejection[6]	150	dB min	For Filter Notches of 10, 25, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 60 Hz Rejection[6]	150	dB min	For Filter Notches of 10, 30, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode Voltage Range[7]	V_{SS} to AV_{DD}	V min to V max	
Analog Inputs[8]			
Input Sampling Rate, f_S	See Table III		
AIN1 Input Voltage Range[9]			For Normal Operation. Depends on Gain Selected
	0 to $+V_{REF}$[10]	V max	Unipolar Input Range (B/U Bit of Control Register = 1)
	$\pm V_{REF}$	V max	Bipolar Input Range (B/U Bit of Control Register = 0)
AIN2 Input Voltage Range[9]			For Normal Operation. Depends on Gain Selected
	0 to $+4 \times V_{REF}$[10]	V max	Unipolar Input Range (B/U Bit of Control Register = 1)
	$\pm 4 \times V_{REF}$	V max	Bipolar Input Range (B/U Bit of Control Register = 0)
AIN2 DC Input Impedance	30	kΩ min	
AIN2 Gain Error[11]	±0.05	% typ	Additional Error Contributed by Resistor Attenuator
AIN2 Gain Drift	1	ppm/°C typ	Additional Drift Contributed by Resistor Attenuator
AIN2 Offset Error[11]	15	mV max	Additional Error Contributed by Resistor Attenuator
Reference Inputs			
REF IN(+) − REF IN(−) Voltage[12]	+2.5 to +5	V min to V max	For Specified Performance. Part Functions with Lower V_{REF} Voltages
Input Sampling Rate, f_S	$f_{CLK\ IN}/512$		

NOTES

[1]Temperature ranges are as follows: A Version, −40°C to +85°C; S Version, −55°C to +125°C.

[2]Applies after calibration at the temperature of interest.

[3]Positive full-scale error applies to both unipolar and bipolar input ranges.

[4]These errors will be of the order of the output noise of the part, as shown in Table I.

[5]Recalibration at any temperature or use of the background calibration mode will remove these drift errors.

[6]These numbers are guaranteed by design and/or characterization.

[7]This common-mode voltage range is allowed provided that the absolute value of the input voltage on AIN1(+) and AIN1(−) does not exceed AV_{DD} + 30 mV and V_{SS} − 30 mV.

[8]The AIN1 analog input presents a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance depends on the selected gain (see Tables IV and V).

[9]The analog input voltage range on the AIN1(+) input is given here with respect to the voltage on the AIN1(−) input. The input voltage range on the AIN2 input is with respect to AGND. The absolute voltage on the AIN1 input should not go more positive than AV_{DD} + 30 mV or more negative than V_{SS} − 30 mV.

[10]V_{REF} = REF IN(+) − REF IN(−).

Parameter	A, S Versions[1]	Units	Conditions/Comments
REFERENCE OUTPUT			
Output Voltage	2.5	V nom	
Initial Tolerance	±4	% max	
Drift	20	ppm/°C typ	
Output Noise	50	μV typ	pk-pk Noise; 0.1 Hz to 10 Hz Bandwidth
Line Regulation (AV_{DD})	1	mV/V max	
Load Regulation	1.5	mV/mA max	Maximum Load Current 1 mA
External Current	1	mA max	
V_{BIAS} INPUT[13]			
Input Voltage Range	$AV_{DD} - 0.85 \times V_{REF}$		See V_{BIAS} Input Section
	or $AV_{DD} - 3$	V max	Whichever Is Smaller; +5 V/−5 V or +10 V/0 V Nominal AV_{DD}/V_{SS}
	or $AV_{DD} - 2.1$	V max	Whichever Is Smaller; +5 V/0 V Nominal AV_{DD}/V_{SS}.
	$V_{SS} + 0.85 \times V_{REF}$		See V_{BIAS} Input Section
	or $V_{SS} + 3$	V min	Whichever Is Greater; +5 V/−5 V or +10 V/0 V Nominal AV_{DD}/V_{SS}
	or $V_{SS} + 2.1$	V min	Whichever Is Greater; +5 V/0 V Nominal AV_{DD}/V_{SS}
V_{BIAS} Rejection	65 to 85	dB typ	Increasing with Gain
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[14]	9	pF typ	
TRANSDUCER BURN-OUT			
Current	100	nA nom	
Initial Tolerance	±10	% typ	
Drift	0.1	%/°C typ	
SYSTEM CALIBRATION			
AIN1			
Positive Full-Scale Calibration Limit[15]	$(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[15]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[16, 17]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[15]	$0.8 \times V_{REF}/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(2.1 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
AIN2			
Positive Full-Scale Calibration Limit[15]	$(4.2 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[15]	$-(4.2 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[17]	$-(4.2 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span	$3.2 \times V_{REF}/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(8.4 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)

[11]This error can be removed using the system calibration capabilities of the AD7712. This error is not removed by the AD7712's self-calibration feature. The offset drift on the AIN2 input is 4 times the value given in the STATIC PERFORMANCE section.

[12]The reference voltage range may be restricted by the input voltage range requirement on the V_{BIAS} input.

[13]The AD7712 is tested with the following V_{BIAS} voltages. With AV_{DD} = +5 V and V_{SS} = 0 V, V_{BIAS} = +2.5 V; with AV_{DD} = +10 V and V_{SS} = 0 V, V_{BIAS} = +5 V and with AV_{DD} = +5 V and V_{SS} = −5 V, V_{BIAS} = 0 V.

[14]Sample tested at +25°C to ensure compliance.

[15]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale, then the device will output all 0s.

[16]These calibration and span limits apply provided the absolute voltage on the AIN1 analog input does not exceed AV_{DD} + 30 mV or does not go more negative than V_{SS} − 30 mV.

[17]The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

Specifications subject to change without notice.

Parameter	A, S Versions[1]	Units	Conditions/Comments
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage[18]	+5 to +10	V nom	±5% for Specified Performance
DV_{DD} Voltage[19]	+5	V nom	±5% for Specified Performance
AV_{DD} – V_{SS} Voltage	+10.5	V max	For Specified Performance
Power Supply Currents			
AV_{DD} Current	4	mA max	
DV_{DD} Current	4.5	mA max	
V_{SS} Current	1.5	mA max	V_{SS} = −5 V
Power Supply Rejection[20]			Rejection w.r.t. AGND. Assumes V_{BIAS} Is Fixed
Positive Supply (AV_{DD})	See Note 21	dB typ	
Negative Supply (V_{SS})	90	dB typ	
Power Dissipation			
Normal Mode	45	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V; Typically 25 mW
Normal Mode	52.5	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = −5 V; Typically 30 mW
Standby (Power-Down) Mode[22]	200	μW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V or −5 V; Typically 100 μW

[18]The AD7712 is specified with a 10 MHz clock for AV_{DD} voltages of +5 V ± 5%. It is specified with an 8 MHz clock for AV_{DD} voltages greater than 5.25 V and less than 10.5 V. Operating with AV_{DD} voltages in the range 5.25 V to 10.5 V is only guaranteed over the 0°C to +70°C temperature range.
[19]The ±5% tolerance on the DV_{DD} input is allowed provided DV_{DD} does not exceed AV_{DD} by more than 0.3 V.
[20]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 10 Hz, 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 10 Hz, 30 Hz or 60 Hz.
[21]PSRR depends on gain: gain of 1 = 70 dB typ; gain of 2 = 75 dB typ; gain of 4 = 80 dB typ; gains of 8 to 128 = 85 dB typ. These numbers can be improved (to 95 dB typ) by deriving the V_{BIAS} voltage (via Zener diode or reference) from the AV_{DD} supply.
[22]Using the hardware STANDBY pin. Standby power dissipation using the software standby bit (PD) of the Control Register is 5 mW typ.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AV_{DD} to DV_{DD} . . . . . −0.3 V to +12 V
AV_{DD} to V_{SS} . . . . . −0.3 V to +12 V
AV_{DD} to AGND . . . . . −0.3 V to +12 V
AV_{DD} to DGND . . . . . −0.3 V to +12 V
DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to DGND . . . . . −0.3 V to +6 V
V_{SS} to AGND . . . . . +0.3 V to −6 V
V_{SS} to DGND . . . . . +0.3 V to −6 V
AIN1 Input Voltage to AGND . V_{SS} − 0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND
. . . . . V_{SS} − 0.3 V to AV_{DD} + 0.3 V
REF OUT to AGND . . . . . −0.3 V to AV_{DD}
Digital Input Voltage to DGND . . . −0.3 V to AV_{DD} + 0.3 V
Digital Output Voltage to DGND . . −0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Commercial (A Version) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7712AN	−40°C to +85°C	N-24
AD7712AR	−40°C to +85°C	R-24
AD7712AQ	−40°C to +85°C	Q-24
AD7712SQ	−55°C to +125°C	Q-24

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

AD7710–SPECIFICATIONS

(AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; V_{SS} = 0 V or −5 V ± 5%; REF IN(+) = +2.5 V; REF IN(−) = AGND; MCLK IN = 10 MHz unless otherwise stated. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. For Filter Notches ≤ 60 Hz
	22	Bits min	For Filter Notch = 100 Hz
	18	Bits min	For Filter Notch = 250 Hz
	15	Bits min	For Filter Notch = 500 Hz
	12	Bits min	For Filter Notch = 1 kHz
Output Noise	Tables I & II		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity			
@ 25°C	±0.0045	% of FSR max	Filter Notches ≤ 60 Hz; Typically ±0.0015%
T_{MIN} to T_{MAX}	±0.0075	% of FSR max	Filter Notches ≤ 60 Hz
Positive Full Scale Error[2, 3]	See Note 4		Excluding Reference
Full-Scale Drift[5]	3/GAIN	μV/°C typ	Excluding Reference. For Gains of 1, 2, 4, 8
	0.35	μV/°C typ	Excluding Reference. For Gains of 16, 32, 64, 128
Unipolar Offset Error[2]	See Note 4		
Unipolar Offset Drift[5]	2.5/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.3	μV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Zero Error[2]	See Note 4		
Bipolar Zero Drift[5]	2.5/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.3	μV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Negative Full-Scale Error[2]	±0.006	% of FSR max	Excluding Reference; Typically ±0.0015%
Bipolar Negative Full-Scale Drift[5]	4/GAIN	μV/°C typ	Excluding Reference. For Gains of 1, 2, 4, 8
	0.5	μV/°C typ	Excluding Reference. For Gains of 16, 32, 64, 128
ANALOG INPUTS/REFERENCE INPUTS			
Common-Mode Rejection (CMR)	92	dB min	At DC
Common-Mode Voltage Range[6]	V_{SS} to AV_{DD}	V min to V max	
Normal Mode 50 Hz Rejection[7]	100	dB min	For Filter Notches of 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Normal Mode 60 Hz Rejection[7]	100	dB min	For Filter Notches of 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode 50 Hz Rejection[7]	150	dB min	For Filter Notches of 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Common-Mode 60 Hz Rejection[7]	150	dB min	For Filter Notches of 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
DC Input Leakage Current[7] @ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[7]	20	pF max	
Analog Inputs[8]			
Input Voltage Range[9]			For Normal Operation. Depends on Gain Selected
	0 to $+V_{REF}$[10]	nom	Unipolar Input Range (B/U Bit of Control Register = 1)
	$\pm V_{REF}$	nom	Bipolar Input Range (B/U Bit of Control Register = 0)
Input Sampling Rate, fs	See Table III		
Reference Inputs			
REF IN(+) − REF IN(−) Voltage[11]	+2.5 to +5	V min to V max	For Specified Performance. Part Functions with Lower V_{REF} Voltages
Input Sampling Rate, f_S	$f_{CLK\ IN}$/512		
REFERENCE OUTPUT			
Output Voltage	2.5	V nom	
Initial Tolerance	±4	% max	
Drift	20	ppm/°C typ	
Output Noise	50	μV typ	pk-pk Noise 0.1 Hz to 10 Hz Bandwidth
Line Regulation (AV_{DD})	1	mV/V max	
Load Regulation	1.5	mV/mA max	Maximum Load Current 1mA
External Current	1	mA max	

NOTES

[1]Temperature ranges are as follows: A Version, −40°C to +85°C; S Version, −55°C to +125°C. See also Note 16.

[2]Applies after calibration at the temperature of interest.

[3]Positive full-scale error applies to both unipolar and bipolar input ranges.

[4]These errors will be of the order of the output noise of the part as shown in Table I.

[5]Recalibration at any temperature or use of the background calibration mode will remove these drift errors.

[6]This common-mode voltage range is allowed provided that the input voltage on AIN(+) and AIN(−) does not exceed AV_{DD} + 30 mV and V_{SS} − 30 mV.

[7]These numbers are guaranteed by design and/or characterization.

[8]The analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance depends on the selected gain (see Tables IV and V).

[9]The analog input voltage range on the AIN1(+) and AIN2(+) inputs is given here with respect to the voltage on the AIN1(−) and AIN2(−) inputs. The absolute voltage on the analog inputs should not go more positive than AV_{DD} + 30 mV or go more negative than V_{SS} − 30 mV.

[10]V_{REF} = REF IN(+) − REF IN(−).

[11]The reference input voltage range may be restricted by the input voltage range requirement on the V_{BIAS} input.

Parameter	A, S Versions[1]	Units	Conditions/Comments
V_{BIAS} INPUT[12]			
Input Voltage Range	$AV_{DD} - 0.85 \times V_{REF}$		See V_{BIAS} Input Section
	or $AV_{DD} - 3$	V max	Whichever Is Smaller; +5 V/−5 V or +10 V/0 V Nominal AV_{DD}/V_{SS}
	or $AV_{DD} - 2.1$	V max	Whichever Is Smaller; +5 V/0 V Nominal AV_{DD}/V_{SS}
	$V_{SS} + 0.85 \times V_{REF}$		See V_{BIAS} Input Section
	or $V_{SS} + 3$	V min	Whichever Is Greater; +5 V/−5 V or +10 V/0 V Nominal AV_{DD}/V_{SS}
	or $V_{SS} + 2.1$	V min	Whichever Is Greater; +5 V/0 V Nominal AV_{DD}/V_{SS}
V_{BIAS} Rejection	65 to 85	dB typ	Increasing with Gain
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	$DV_{DD} - 1$	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[13]	9	pF typ	
TRANSDUCER BURN-OUT			
Current	100	nA nom	
Initial Tolerance	±10	% typ	
Drift	0.1	%/°C typ	
COMPENSATION CURRENT			
Output Current	20	μA nom	
Initial Tolerance	±4	μA max	
Drift	35	ppm/°C typ	
Line Regulation (AV_{DD})	20	nA/V max	AV_{DD} = +5 V
Load Regulation	20	nA/V max	
Output Compliance	$AV_{DD} - 2$	V max	
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[14]	$(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[14]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[15]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[15]	$0.8 \times V_{REF}/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(2.1 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)

NOTES

[12]The AD7710 is tested with the following V_{BIAS} voltages. With AV_{DD} = +5 V and V_{SS} = 0 V, V_{BIAS} = +2.5 V; with AV_{DD} = +10 V and V_{SS} = 0 V, V_{BIAS} = +5 V and with AV_{DD} = +5 V and V_{SS} = −5 V, V_{BIAS} = 0 V.

[13]Sample tested at +25°C to ensure compliance.

[14]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale then the device will output all 0s.

[15]These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed AV_{DD} + 30 mV or go more negative than V_{SS} − 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

Parameter	A, S Versions[1]	Units	Conditions/Comments
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage[16]	+5 to +10	V nom	±5% for Specified Performance
DV_{DD} Voltage[17]	+5	V nom	±5% for Specified Performance
AV_{DD}–V_{SS} Voltage	+10.5	V max	For Specified Performance
Power Supply Currents			
AV_{DD} Current	4	mA max	
DV_{DD} Current	4.5	mA max	
V_{SS} Current	1.5	mA max	V_{SS} = −5 V
Power Supply Rejection[18]			Rejection w.r.t. AGND; Assumes V_{BIAS} Is Fixed
Positive Supply (AV_{DD})	See Note 19	dB typ	
Negative Supply (V_{SS})	90	dB typ	
Power Dissipation			
Normal Mode	45	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V; Typically 25 mW
Normal Mode	52.5	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = −5 V; Typically 30 mW
Standby (Power-Down) Mode	15	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V or −5 V; Typically 7 mW

NOTES

[16]The AD7710 is specified with a 10 MHz clock for AV_{DD} voltages of +5 V ± 5%. It is specified with an 8 MHz clock for AV_{DD} voltages greater than 5.25 V and less than 10.5 V. Operation with AV_{DD} voltages in the range 5.25 V to 10.5 V is only guaranteed over the 0 to +70°C temperature range.

[17]The ±5% tolerance on the DV_{DD} input is allowed provided that DV_{DD} does not exceed AV_{DD} by more than 0.3 V.

[18]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 10 Hz, 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 10 Hz, 30 Hz or 60 Hz.

[19]PSRR depends on gain: Gain of 1: 70 dB typ; Gain of 2: 75 dB typ; Gain of 4: 80 dB typ; Gains of 8 to 128: 85 dB typ. These numbers can be improved (to 95 dB typ) by deriving the V_{BIAS} voltage (via Zener diode or reference) from the AV_{DD} supply.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C, unless otherwise noted)

AV_{DD} to DV_{DD} . . . . . −0.3 V to +12 V
AV_{DD} to V_{SS} . . . . . −0.3 V to +12 V
AV_{DD} to AGND . . . . . −0.3 V to +12 V
AV_{DD} to DGND . . . . . −0.3 V to +12 V
DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to DGND . . . . . −0.3 V to +6 V
V_{SS} to AGND . . . . . +0.3 V to −6 V
V_{SS} to DGND . . . . . +0.3 V to −6 V
Analog Input Voltage to AGND
. . . . . V_{SS} − 0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND
. . . . . V_{SS} − 0.3 V to AV_{DD} + 0.3 V
REF OUT to AGND . . . . . −0.3 V to AV_{DD}
Digital Input Voltage to DGND . . . −0.3 V to AV_{DD} + 0.3 V
Digital Output Voltage to DGND . . −0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Commercial (A Version) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates Above +75°C . . . . . 6 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD7710AN	−40°C to +85°C	N-24
AD7710AR	−40°C to +85°C	R-24
AD7710AQ	−40°C to +85°C	Q-24
AD7710SQ	−55°C to +125°C	Q-24

NOTES

[1]To order MIL-STD-883B, Class B processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.

[2]N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

TIMING CHARACTERISTICS[1, 2]

(DV_{DD} = +5 V ± 5%; AV_{DD} = +5 V or +10 V[3] ± 5%; V_{SS} = 0 V or −5 V ± 5%; AGND = DGND = 0 V; f_{CLKIN} = 10 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD}, unless otherwise stated.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
$f_{CLK\ IN}$[4, 5]			Master Clock Frequency: Crystal Oscillator or Externally Supplied
	400	kHz min	AV_{DD} = +5 V ± 5%
	10	MHz max	For Specified Performance
	8	MHz max	AV_{DD} = +5.25 V to +10.5 V
$t_{CLK\ IN\ LO}$	0.4 × $t_{CLK\ IN}$	ns min	Master Clock Input Low Time; $t_{CLK\ IN} = 1/f_{CLK\ IN}$
$t_{CLK\ IN\ HI}$	0.4 × $t_{CLK\ IN}$	ns min	Master Clock Input High Time
t_r[6]	50	ns max	Digital Output Rise Time; Typically 20 ns
t_f[6]	50	ns max	Digital Output Fall Time; Typically 20 ns
t_1	1000	ns min	$\overline{SYNC}$ Pulse Width
Self-Clocking Mode			
t_2	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time; $t_{CLK\ IN} = 1/f_{CLK\ IN}$
t_3	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_4	2 × $t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_5	50	ns min	A0 to $\overline{RFS}$ Hold Time
t_6	4 × $t_{CLK\ IN}$	ns max	$\overline{RFS}$ Low to SCLK Falling Edge
t_7[7]	4 × $t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_8[7]	$t_{CLK\ IN}$/2	ns min	SCLK Falling Edge to Data Valid Delay
	$t_{CLK\ IN}$/2 + 30	ns max	
t_9	$t_{CLK\ IN}$/2	ns nom	SCLK High Pulse Width
t_{10}	3 × $t_{CLK\ IN}$/2	ns nom	SCLK Low Pulse Width
t_{11}	10	ns min	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
	$t_{CLK\ IN}$/2	ns max	
t_{12}	3 × $t_{CLK\ IN}$/2 + 20	ns max	$\overline{RFS}$/$\overline{TFS}$ to SCLK Delay
t_{13}[8]	3 × $t_{CLK\ IN}$/2 + 20	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{14}	0	ns min	A0 to $\overline{TFS}$ Setup Time
t_{15}	0	ns min	A0 to $\overline{TFS}$ Hold Time
t_{16}	4 × $t_{CLK\ IN}$	ns max	$\overline{TFS}$ to SCLK Falling Edge Delay Time
t_{17}	4 × $t_{CLK\ IN}$	ns min	$\overline{TFS}$ to SCLK Falling Edge Hold Time
t_{18}	0	ns min	Data Valid to SCLK Setup Time
t_{19}	10	ns min	Data Valid to SCLK Hold Time

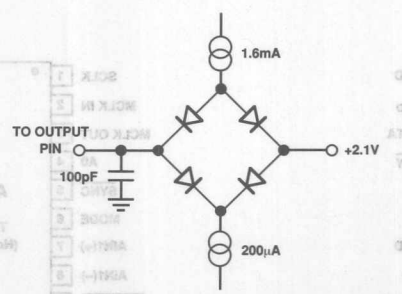


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
External Clocking Mode			
f_{SCLK}	$f_{CLK\ IN}/5$	MHz max	Serial Clock Input Frequency
t_{20}	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time
t_{21}	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_{22}	$2 \times t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_{23}	50	ns min	A0 to $\overline{RFS}$ Hold Time
t_{24}[7]	$4 \times t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_{25}[7]	$t_{CLK\ IN}/2$	ns min	SCLK Falling Edge to Data Valid Delay
	$2 \times t_{CLK\ IN} + 20$	ns max	
t_{26}	$2 \times t_{CLK\ IN}$	ns min	SCLK High Pulse Width
t_{27}	$2 \times t_{CLK\ IN}$	ns min	SCLK Low Pulse Width
t_{28}	$t_{CLK\ IN} + 10$	ns max	SCLK Falling Edge to $\overline{DRDY}$ High
t_{29}[8]	0	ns min	$\overline{DRDY}$ to Data Valid Hold Time
	20	ns max	
t_{30}	10	ns min	$\overline{RES}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
t_{31}[8]	$5 \times t_{CLK\ IN}/2 + 20$	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{32}	0	ns min	A0 to $\overline{TFS}$ Setup Time
t_{33}	0	ns min	A0 to $\overline{TFS}$ Hold Time
t_{34}	$4 \times t_{CLK\ IN}$	ns min	SCLK Falling Edge to $\overline{TFS}$ Hold Time
t_{35}	$5 \times t_{CLK\ IN}/2 - $ SCLK High	ns min	Data Valid to SCLK Setup Time
t_{36}	30	ns min	Data Valid to SCLK Hold Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 6 to 9.

[3]The AD7710/AD7712 is specified with a 10 MHz clock for AV_{DD} voltages of +5 V ± 5%. It is specified with an 8 MHz clock for AV_{DD} voltages greater than 5.25 V and less than 10.5 V. Operation with AV_{DD} voltages in the range 5.25 V to 10.5 V is only guaranteed over the 0°C to +70°C temperature range.

[4]CLK IN duty cycle range is 45% to 55%. CLK IN must be supplied whenever the AD7710/AD7712 is not in STANDBY mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

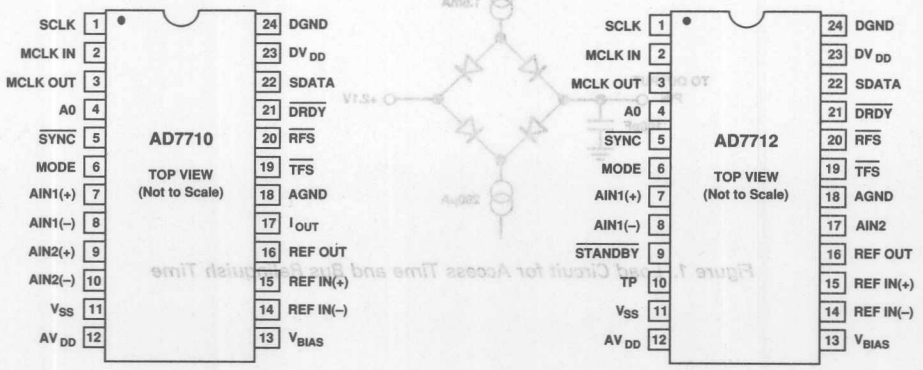
[5]The AD7710/AD7712 is production tested with $f_{CLK\ IN}$ at 10 MHz (8 MHz for AV_{DD} < +5.25 V). It is guaranteed by characterization to operate at 400 kHz.

[6]Specified using 10% and 90% points on waveform of interest.

[7]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

[8]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 100 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.

PIN CONFIGURATION
DIP and SOIC



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1	SCLK	Serial Clock. Logic Input/Output depending on the status of the MODE pin. When MODE is high, the device is in its self-clocking mode and the SCLK pin provides a serial clock output. This SCLK becomes active when $\overline{RFS}$ or $\overline{TFS}$ goes low and it goes high impedance when either $\overline{RFS}$ or $\overline{TFS}$ returns high or when the device has completed transmission of an output word. When MODE is low, the device is in its external clocking mode and the SCLK pin acts as an input. This input serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7710/AD7712 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal or external clock. A crystal can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The clock input frequency is nominally 10 MHz.
3	MCLK OUT	When the master clock for the device is a crystal, the crystal is connected between MCLK IN and MCLK OUT.
4	A0	Address Input. With this input low, reading and writing to the device is to the control register. With this input high, access is to either the data register or the calibration registers.
5	$\overline{SYNC}$	Logic Input which allows for synchronization of the digital filters when using a number of AD7710/AD7712s. It resets the nodes of the digital filter.
6	MODE	Logic Input. When this pin is high, the device is in its self-clocking mode; with this pin low, the device is in its external clocking mode.
7	AIN1(+)	Analog Input Channel 1. Positive input of the programmable gain differential analog input. The AIN1(+) input is connected to an output current source which can be used to check that an external transducer has burnt out or gone open circuit. This output current source can be turned on/off via the control register.
8	AIN1(−)	Analog Input Channel 1. Negative input of the programmable gain differential analog input.
9	AIN2(+)	AD7710 Only. Analog Input Channel 2. Positive input of the programmable gain differential analog input.
9	$\overline{STANDBY}$	AD7712 Only. Logic Input. Taking this pin low shuts down the internal analog and digital circuitry, reducing power consumption to less than 50 μW.
10	AIN2(−)	AD7710 Only. Analog Input Channel 2. Negative input of the programmable gain differential analog input.
10	TP	AD7712 Only. Test Pin. Used when testing the device. Do not connect anything to this pin.
11	V_{SS}	Analog Negative Supply, 0 V to −5 V. Tied to AGND for single supply operation. The input voltage on AIN1 should not go > 30 mV negative w.r.t. V_{SS} for correct operation of the device.
12	AV_{DD}	Analog Positive Supply Voltage, +5 V to +10 V.
13	V_{BIAS}	Input Bias Voltage. This input voltage should be set such that $V_{BIAS} + 0.85 \times V_{REF} < AV_{DD}$ and $V_{BIAS} - 0.85 \times V_{REF} > V_{SS}$ where V_{REF} is REF IN(+) − REF IN(−). Ideally, this should be tied halfway between AV_{DD} and V_{SS}. Thus, with AV_{DD} = +5 V and V_{SS} = 0, it can be tied to REF OUT; with AV_{DD} = +5 V and V_{SS} = −5 V, it can be tied to AGND, while with AV_{DD} = +10 V, it can be tied to +5 V or to REF OUT.
14	REF IN(−)	Reference Input. The REF IN(−) can lie anywhere between AV_{DD} and V_{SS} provided REF IN(+) is greater than REF IN(−).
15	REF IN(+)	Reference Input. The reference input is differential providing that REF IN(+) is greater than REF IN(−). REF IN(+) can lie anywhere between AV_{DD} and V_{SS}.
16	REF OUT	Reference Output. The internal +2.5 V reference is provided at this pin. This is a single-ended output which is referred to AGND.
17	I_{OUT}	AD7710 Only. Compensation Current Output. A 20 μA constant current is provided at this pin. This current can be used in conjunction with an external thermistor to provide cold junction compensation.
17	AIN2	AD7712 Only. Analog Input Channel 2. High level analog input which accepts an analog input voltage range of $\pm 4 \times V_{REF}$/GAIN. At the nominal V_{REF} of +2.5 V and a gain of 1, the AIN2 input voltage range is ±10 V.
18	AGND	Ground reference point for analog circuitry.

		serial data expected after the falling edge of this pulse. In the self-clocking mode, the serial clock becomes active after $\overline{TFS}$ goes low. In the external clocking mode, $\overline{TFS}$ must go low before the first bit of the data word is written to the part.
20	$\overline{RFS}$	Receive Frame Synchronization. Active low logic input used to access serial data from the device. In the self-clocking mode, the SCLK and SDATA lines both become active after $\overline{RFS}$ goes low. In the external clocking mode, the SDATA line becomes active after $\overline{RFS}$ goes low.
21	$\overline{DRDY}$	Logic output. A falling edge indicates that a new output word is available for transmission. The $\overline{DRDY}$ pin will return high upon completion of transmission of a full output word. $\overline{DRDY}$ is also used to indicate when the AD7710/AD7712 has completed its on-chip calibration sequence.
22	SDATA	Serial Data. Input/Output with serial data being written to the control register or the calibration registers and serial data being accessed from the control register, calibration registers or the data register. During an output data read operation, serial data becomes active after $\overline{RFS}$ goes low (provided $\overline{DRDY}$ is low). During a write operation, valid serial data is expected on the rising edges of SCLK when $\overline{TFS}$ is low. The output data coding is natural binary for unipolar inputs and offset binary for bipolar inputs.
23	DV_{DD}	Digital Supply Voltage, +5 V. DV_{DD} should never exceed AV_{DD} by more than 0.3 V. If DV_{DD} powers up before AV_{DD}, or if DV_{DD} can exceed AV_{DD} by more than 0.3 V at any other time, the protection scheme outlined in Figure 5 should be used.
24	DGND	Ground reference point for digital circuitry.

TERMINOLOGY

INTEGRAL NONLINEARITY

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full-scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

POSITIVE FULL-SCALE ERROR

Positive full-scale error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal input full-scale voltage. For AIN(+),* the ideal full-scale input voltage is (AIN(−) + V_{REF}/GAIN −3/2 LSBs); for AIN2 of AD7712, the ideal full-scale voltage is +4 × V_{REF}/GAIN −3/2 LSBs. Positive full-scale error applies to both unipolar and bipolar analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar offset error is the deviation of the first code transition from the ideal input voltage. For AIN(+), the ideal input voltage is (AIN(−) +0.5 LSB); for AIN2 of AD7712, the ideal input is 0.5 LSB when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal input voltage. For AIN(+), the ideal input voltage is (AIN(−) −0.5 LSB); for AIN2 of AD7712, the ideal input voltage is −0.5 LSB when operating in the bipolar mode.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal input voltage. For AIN(+), the ideal input voltage is (AIN(−) −V_{REF}/GAIN + 0.5 LSB); for AIN2 of AD7712, the ideal input voltage is (−4 × V_{REF}/GAIN+0.5 LSB) when operating in the bipolar mode.

POSITIVE FULL-SCALE OVERRANGE

Positive full-scale overrange is the amount of overhead available to handle input voltages on AIN(+) input greater than (AIN(−)+V_{REF}/GAIN) or on AIN2 of AD7712 of greater than +4 × V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages on AIN(+) below (AIN(−)−V_{REF}/GAIN) or on AIN2 of AD7712 below −4 × V_{REF}/GAIN without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks on AIN1(+) even in the unipolar mode provided that AIN(+) is greater than AIN(−) and greater than V_{SS} −30 mV.

OFFSET CALIBRATION RANGE

In the system calibration modes, the AD7710/AD7712 calibrates its offset with respect to the analog input. The offset calibration range specification defines the range of voltages that the AD7710/AD7712 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7710/AD7712 can accept in the system calibration mode and still calibrate full scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7710/AD7712's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full-scale that the AD7710/AD7712 can accept and still calibrate gain accurately.

*AIN(+) refers to AIN1(+) and AIN2(+) of AD7710 and AIN1(+) of AD7712. AIN(−) refers to AIN1(−) and AIN2(−) of AD7710 and AIN1(−) of AD7712.

CONTROL REGISTER (24 BITS)

A write to the device with the A0 input low writes data to the control register. A read to the device with the A0 input low accesses the contents of the control register. The control register is 24-bits wide and when writing to the register 24 bits of data must be written otherwise the data will not be loaded to the control register. In other words, it is not possible to write just the first 12-bits of data into the control register. If more than 24 clock pulses are provided before $\overline{TFS}$ returns high, then all clock pulses after the 24th clock pulse are ignored. Similarly, a read operation from the control register should access 24 bits of data.

MSB

MD2	MD1	MD0	G2	G1	G0	CH	PD	WL	IO[1]	BO	B/U
FS11[2]	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

LSB

[1]Don't Care on AD7712.
[2]Must always be 0 to ensure correct operation of the part.

Operating Mode			
MD2	**MD1**	**MD0**	**Operating Mode**
0	0	0	Normal Mode. This is the normal mode of operation of the device whereby a read to the device accesses data from the data register. This is the default condition of these bits after the internal power-on reset.
0	0	1	Activate Self-Calibration. This activates self-calibration on the channel selected by CH. This is a one-step calibration sequence, and when complete the part returns to Normal Mode (with MD2, MD1, MD0 of the control registers returning to 0,0,0). The $\overline{DRDY}$ output indicates when this self-calibration is complete and valid data is available in the output register. For this calibration type, the zero scale calibration is done internally on shorted (zeroed) inputs and the full-scale calibration is done on V_{REF}.
0	1	0	Activate System Calibration. This activates system calibration on the channel selected by CH. This is a two-step calibration sequence, with the zero scale calibration done first on the selected input channel and $\overline{DRDY}$ indicating when this zero scale calibration is complete. The part returns to Normal Mode at the end of this first step in the two-step sequence.
0	1	1	Activate System Calibration. This is the second step of the system calibration sequence with full-scale calibration being performed on the selected input channel. Once again, $\overline{DRDY}$ indicates when this full-scale calibration is complete. When this calibration is complete, the part returns to Normal Mode.
1	0	0	Activate System-Offset Calibration. This activates system-offset calibration on the channel selected by CH. This is a one-step calibration sequence and when complete the part returns to Normal Mode with $\overline{DRDY}$ indicating when this system offset calibration is complete. For this calibration type, the zero scale calibration is done on the selected input channel and the full-scale calibration is done internally on V_{REF}.
1	0	1	Activate Background Calibration. This activates background calibration on the channel selected by CH. If the background calibration mode is on, then the AD7710/AD7712 provides continuous self-calibration of the reference and shorted (zeroed) inputs. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the device when there is a change in the ambient temperature. In this mode, shorted (zeroed) inputs and V_{REF}, as well as the analog input voltage, are continuously monitored and the calibration registers of the device are automatically updated.
1	1	0	Read/Write Zero-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the zero scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the zero scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits regardless, of the status of the WL bit of the control register. Therefore, when writing to the calibration register, 24 bits of data must be written, otherwise the new data will not be transferred to the calibration register.
1	1	1	Read/Write Full-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the full-scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the full-scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Therefore, when writing to the calibration register, 24 bits of data must be written, otherwise the new data will not be transferred to the calibration register.

PGA Gain

G2	G1	G0	Gain	
0	0	0	1	(Default Condition After the Internal Power-On Reset)
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

Channel Selection

CH	Channel		
0	AIN1	Low Level Input	(Default Condition After the Internal Power-On Reset)
1	AIN2	High Level Input	

Power-Down

PD		
0	Normal Operation	(Default Condition After the Internal Power-On Reset)
1	Power-Down	

Word Length

WL	Output Word Length	
0	16-Bit	(Default Condition After Internal Power-On Reset)
1	24-Bit	

Output Compensation Current (AD7710 Only)

IO		
0	Off	(Default Condition After Internal Power-On Reset)
1	On	

Burn-Out Current

BO		
0	Off	(Default Condition After Internal Power-On Reset)
1	On	

Bipolar/Unipolar Selection (Both Inputs)

B/U		
0	Bipolar	(Default Condition After Internal Power-On Reset)
1	Unipolar	

Filter Selection (FS11–FS0)

The on-chip digital filter provides a Sinc^3 (or (Sinx/x)^3) filter response. The 12 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device.

The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency = ($f_{CLK\ IN}$/512)/*code* where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 2,000. With the nominal $f_{CLK\ IN}$ of 10 MHz, this results in a first notch frequency range from 9.76 Hz to 1.028 kHz. To ensure correct operation of the part, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I and II show the effect of the filter notch frequency and gain on the effective resolution of the part. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1 kHz, a new word is available every 1 ms.

The settling time of the filter to a full-scale step input change is worst case 4 × 1/(output data rate). This settling time is to 100% of the final value. For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. If the first notch is at 1 kHz, the settling time of the filter to a full-scale input step is 4 ms max. This settling time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with $\overline{SYNC}$ low, the settling time will be 3 × 1/(output data rate). If a change of channel takes place, the settling time is 3 × 1/(output data rate) regardless of the $\overline{SYNC}$ input, but $\overline{DRDY}$ does not stay high for 3 × 1/output rate.

The −3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter −3 dB frequency = 0.262 × first notch frequency, but $\overline{DRDY}$ does not stay high for 3 × 1/output rate.

Tables I and II show the output rms noise for some typical notch and −3 dB frequencies. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V. These numbers are typical and are generated with an analog input voltage of 0 V. The output noise from the part comes from two sources. First, there is the electrical noise in the semiconductor devices used in the implementation of the modulator (device noise). Secondly, when the analog input signal is converted into the digital domain, quantization noise is added. The device noise is at a low level and is largely independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. Consequently, lower filter notch settings (below 60 Hz approximately) tend to be device noise dominated while higher notch settings are dominated by quantization noise. Changing the filter notch and cutoff frequency in the quantization noise dominated region results in a more dramatic improvement in noise performance than it does in the device noise dominated region as shown in Table I. Furthermore, quantization noise is added after the PGA, so effective resolution is independent of gain for the higher filter notch frequencies. Meanwhile, device noise is added in the PGA, and therefore effective resolution suffers a little at high gains for lower notch frequencies.

At the lower filter notch settings (below 60 Hz), the no missing codes performance of the device is at the 24-bit level. At the higher settings, more codes will be missed until at 1 kHz notch setting, no missing codes performance is only guaranteed to the 12-bit level. However, since the effective resolution of the part is 10.5 bits for this filter notch setting, this no missing codes performance should be more than adequate for all applications.

The effective resolution of the device is defined as the ratio of the output rms noise to the input full scale. This does not remain constant with increasing gain or with increasing bandwidth. Table II shows the same table as Table I except that the output is now expressed in terms of effective resolution (the magnitude of the rms noise with respect to 2 × V_{REF}/GAIN, i.e., the input full scale). It is possible to do post filtering on the device to improve the output data rate for a given −3 dB frequency and also to further reduce the output noise (see Digital Filtering section).

Table I. Output Noise vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate[1]	−3 dB Frequency	Typical Output RMS Noise (μV)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz[2]	2.62 Hz	1.7	1.0	0.5	0.36	0.36	0.36	0.36	0.36
25 Hz[2]	6.55 Hz	4.9	2.2	1.2	0.6	0.36	0.36	0.36	0.36
30 Hz[2]	7.86 Hz	6.1	2.4	1.2	0.84	0.5	0.36	0.36	0.36
50 Hz[2]	13.1 Hz	7.5	3.8	2.0	1.0	0.6	0.5	0.5	0.45
60 Hz[2]	15.72 Hz	8.5	4.0	2.0	1.0	0.6	0.5	0.5	0.45
100 Hz[3]	26.2 Hz	13	6.4	3.7	1.8	1.1	0.9	0.65	0.65
250 Hz[3]	65.5 Hz	130	75	25	12	7.5	4	2.7	1.7
500 Hz[3]	131 Hz	0.6 × 10^3	0.26 × 10^3	140	70	35	25	15	8
1 kHz[3]	262 Hz	3.1 × 10^3	1.6 × 10^3	0.7 × 10^3	0.29 × 10^3	180	120	70	40

NOTES
[1]The default condition (after the internal power-on reset) for the first notch of filter is 60 Hz.
[2]For these filter notch frequencies, the output rms noise is primarily dominated by device noise and as a result is independent of the value of the reference voltage. Therefore, increasing the reference voltage will give an increase in the effective resolution of the device (i.e., the ratio of the rms noise to the input full scale is increased since the output rms noise remains constant as the input full-scale increases).
[3]For these filter notch frequencies, the output rms noise is dominated by quantization noise and as a result is proportional to the value of the reference voltage.

Table II. Effective Resolution vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate	−3 dB Frequency	Effective Resolution[1] (Bits)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz	2.62 Hz	21.5	21.5	21.5	20.5	19.5	18.5	17.5	16.5
25 Hz	6.55 Hz	20	20	20	20	19.5	18.5	17.5	16.5
30 Hz	7.86 Hz	19.5	20	20	19.5	19.5	18.5	17.5	16.5
50 Hz	13.1 Hz	19.5	19.5	19.5	19.5	19	18.5	17.5	16.5
60 Hz	15.72 Hz	19	19.5	19.5	19.5	19	18.5	17.5	16.5
100 Hz	26.2 Hz	18.5	18.5	18.5	18.5	18	17.5	17	16
250 Hz	65.5 Hz	15	15	15.5	15.5	15.5	15.5	15	14.5
500 Hz	131 Hz	13	13	13	13	13	12.5	12.5	12.5
1 kHz	262 Hz	10.5	10.5	11	11	11	10.5	10	10

NOTE
[1]Effective resolution is defined as the magnitude of the output rms noise with respect to the input full scale (i.e., 2 × V_{REF}/GAIN). The above table applies for a V_{REF} of +2.5 V and resolution numbers are rounded to the nearest 0.5 LSB.

CIRCUIT DESCRIPTION

The AD7710/AD7712 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in industrial control or process control applications. It contains a sigma-delta (or charge balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bidirectional serial communications port.

The part contains two programmable gain analog input channels. The gain range on both inputs is from 1 to 128. For the differential inputs, this means that the input can accept unipolar signals of between 0 mV to +20 mV and 0 mV to +2.5 V or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals +2.5 V. The input voltage range for the AIN2 input of the AD7712 is $\pm 4 \times V_{REF}$/GAIN and is ±10 V with the nominal reference of +2.5 V and a gain of 1. The input signal to the selected analog input channel is continuously sampled at a rate determined by the frequency of the master clock, CLK IN, and the selected gain (see Table III). A charge balancing A/D converter (Sigma-Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma-delta modulator with the input sampling frequency being modified to give the higher gains. A sinc^3 digital low-pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and hence its −3 dB frequency) can be programmed via an on-chip control register. The programmable range for this first notch frequency is from 9.76 Hz to 1.028 kHz, giving a programmable range for the −3 dB frequency of 2.58 Hz to 269 Hz.

The AD7710/AD7712 provides a number of calibration options which can be programmed via the on-chip control register. A calibration cycle may be initiated at any time by writing to this control register. The part can perform self-calibration using the on-chip calibration microcontroller and SRAM to store calibration parameters. Other system components may also be included in the calibration loop to remove offset and gain errors in the input channel using the system calibration mode. Another option is a background calibration mode where the part continuously performs self-calibration and updates the calibration coefficients. Once the part is in this mode, the user does not have to worry about issuing periodic calibration commands to the device or asking the device to recalibrate when there is a change in the ambient temperature or power supply voltage.

The AD7710/AD7712 gives the user access to the on-chip calibration registers allowing the microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part from prestored values in E^2PROM. This gives the microprocessor much greater control over the part's calibration procedure. It also means that the user can verify that the device has performed its calibration correctly by comparing the coefficients after calibration with prestored values in E^2PROM.

The AD7710/AD7712 can be operated in single supply systems provided that the analog input voltage on the differential inputs does not go more negative than −30 mV. For larger bipolar signals on the differential inputs, a V_{SS} of −5 V is required by the part. For battery operation or low power systems, the part offers a standby mode that reduces idle power consumption to typically 100 μW on AD7712 and 7 μW on AD7710.

The AD7710/AD7712 uses a second-order sigma-delta modulator and a digital filter that provides a rolling average of the sampled output. After power-up, or if there is a step change in the input voltage, there is a settling time that must elapse before valid data is obtained.

Input Sample Rate

The modulator sample frequency for the device remains at $f_{CLK\ IN}/512$ (19.5 kHz @ $f_{CLK\ IN}$ = 10 MHz) regardless of the selected gain. However, gains greater than ×1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of reference capacitor to input capacitor. As a result of the multiple sampling, the input sample rate of the device varies with the selected gain (see Table III). The effective input impedance is $1/C \cdot f_S$ where C is the input sampling capacitance and f_S is the input sample rate.

Table III. Input Sampling Frequency vs. Gain

Gain	Input Sampling Frequency (f_S)
1	$f_{CLK\ IN}/512$ (19.5 kHz @ $f_{CLK\ IN}$ = 10 MHz)
2	$2 \times f_{CLK\ IN}/512$ (39 kHz @ $f_{CLK\ IN}$ = 10 MHz)
4	$4 \times f_{CLK\ IN}/512$ (78 kHz @ $f_{CLK\ IN}$ = 10 MHz)
8	$8 \times f_{CLK\ IN}/512$ (156 kHz @ $f_{CLK\ IN}$ = 10 MHz)
16	$8 \times f_{CLK\ IN}/512$ (156 kHz @ $f_{CLK\ IN}$ = 10 MHz)
32	$8 \times f_{CLK\ IN}/512$ (156 kHz @ $f_{CLK\ IN}$ = 10 MHz)
64	$8 \times f_{CLK\ IN}/512$ (156 kHz @ $f_{CLK\ IN}$ = 10 MHz)
128	$8 \times f_{CLK\ IN}/512$ (156 kHz @ $f_{CLK\ IN}$ = 10 MHz)

DIGITAL FILTERING

The part's digital filter behaves like a similar analog filter, with a few minor differences.

First, since digital filtering occurs after the A-to-D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full-scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the part has over-range headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 5% above the analog input range. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the input channel voltage so that its full-scale is half that of the analog input channel full-scale. This will provide an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

Filter Characteristics

The cutoff frequency of the digital filter is determined by the value loaded to bits FS0 to FS11 in the control register. At the maximum clock frequency of 10 MHz, the minimum cutoff frequency of the filter is 2.58 Hz while the maximum programmable cutoff frequency is 269 Hz.

Figure 2 shows the filter frequency response for a cutoff frequency of 2.62 Hz which corresponds to a first filter notch frequency of 10 Hz. This is a $(\sin x/x)^3$ response (also called sinc^3) that provides >100 dB of 50 Hz and 60 Hz rejection. Programming a different cutoff frequency via FS0–FS11 does not alter the profile of the filter response, it changes the frequency of the notches as outlined in the Control Register section.

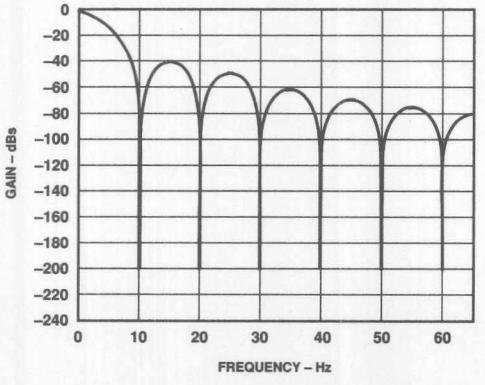


Figure 2. Frequency Response of AD7710/AD7712 Filter

Since the AD7710/AD7712 contains this on-chip, low-pass filtering, there is a settling time associated with step function inputs and data on the output will be invalid after a step change until the settling time has elapsed. The settling time depends upon the notch frequency chosen for the filter. The output data rate equates to this filter notch frequency and the settling time of the filter to a full-scale step input is 4 times the output data period. In applications using both input channels, the settling time of the filter must be allowed to elapse before data from the second channel is accessed.

Post Filtering

The on-chip modulator provides samples at a 19.5 kHz output rate. The on-chip digital filter decimates these samples to provide data at an output rate which corresponds to the programmed first notch frequency of the filter. Since the output data rate exceeds the Nyquist criterion, the output rate for a given bandwidth will satisfy most application requirements. However, there may be some applications which require a higher data rate for a given bandwidth and noise performance. Applications which need this higher data rate will require some post filtering following the digital filter of the AD7710/AD7712.

For example, if the required bandwidth is 7.86 Hz but the required update rate is 100 Hz, the data can be taken from the AD7710/AD7712 at the 100 Hz rate giving a −3 dB bandwidth of 26.2 Hz. Post filtering can be applied to this to reduce the bandwidth and output noise, to the 7.86 Hz bandwidth level, while maintaining an output rate of 100 Hz.

Post filtering can also be used to reduce the output noise from the device for bandwidths below 2.62 Hz. At a gain of 128, the output rms noise is 420 nV. This is essentially device noise or white noise, and since the input is chopped, the noise has a flat frequency response. By reducing the bandwidth below 2.62 Hz, the noise in the resultant passband can be reduced. A reduction in bandwidth by a factor of 2 results in a $\sqrt{2}$ reduction in the output rms noise. This additional filtering will result in a longer settling time.

Antialias Considerations

The digital filter does not provide any rejection at integer multiples of the modulator sample frequency (n × 19.5 kHz, where n = 1, 2, 3 . . .). This means that there are frequency bands, $\pm f_{3\ dB}$ wide ($f_{3\ dB}$ is cutoff frequency selected by FS0 to FS11) where noise passes unattenuated to the output. However, due to the AD7710/AD7712's high oversampling ratio, these bands occupy only a small fraction of the spectrum and most broadband noise is filtered. In any case, because of the high oversampling ratio a simple, RC, single pole filter is generally sufficient to attenuate the signals in these bands on the analog input and thus provide adequate antialiasing filtering.

is low enough so as not to introduce gain errors in the system. The dc input impedance for the differential inputs is over 1 GΩ. The input appears as a dynamic load which varies with the clock frequency and with the selected gain (see Figure 3). The input sample rate, as shown in Table III, determines the time allowed for the analog input capacitor, C_{IN}, to be charged. External impedances result in a longer charge time for this capacitor and this may result in gain errors being introduced on the analog inputs. Table IV shows the allowable external resistance/capacitance values such that no gain error to the 16-bit level is introduced while Table V shows the allowable external resistance/capacitance values such that no gain error to the 20-bit level is introduced. Both inputs of the differential input channels look into similar input circuitry.

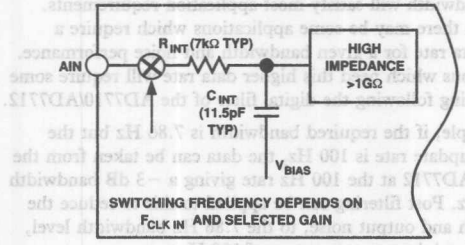


Figure 3. Differential Inputs Impedance

Table IV. Typical External Series Resistance Which Will Not Introduce 16-Bit Gain Error

	External Capacitance (pF)					
Gain	**0**	**50**	**100**	**500**	**1000**	**5000**
1	184 kΩ	45.3 kΩ	27.1 kΩ	7.3 kΩ	4.1 kΩ	1.1 kΩ
2	88.6 kΩ	22.1 kΩ	13.2 kΩ	3.6 kΩ	2.0 kΩ	560 Ω
4	41.4 kΩ	10.6 kΩ	6.3 kΩ	1.7 kΩ	970 Ω	270 Ω
8–128	17.6 kΩ	4.8 kΩ	2.9 kΩ	790 Ω	440 Ω	120 Ω

	External Capacitance (pF)					
Gain	**0**	**50**	**100**	**500**	**1000**	**5000**
1	145 kΩ	34.5 kΩ	20.4 kΩ	5.2 kΩ	2.8 kΩ	700 Ω
2	70.5 kΩ	16.9 kΩ	10 kΩ	2.5 kΩ	1.4 kΩ	350 Ω
4	31.8 kΩ	8.0 kΩ	4.8 kΩ	1.2 kΩ	670 Ω	170 Ω
8–128	13.4 kΩ	3.6 kΩ	2.2 kΩ	550 Ω	300 Ω	80 Ω

The numbers in the above tables assume a full-scale change on the analog input. In any case, the error introduced due to longer charging times is a gain error which can be removed using the system calibration capabilities of the AD7710/AD7712 provided that the resultant span is within the span limits of the system calibration techniques for the AD7710/AD7712.

The AIN2 input of the AD7712 contains a resistive attenuation network as outlined in Figure 4. The typical input impedance on this input is 44 kΩ. As a result, the AIN2 input of the AD7712 should be driven from a low impedance source.

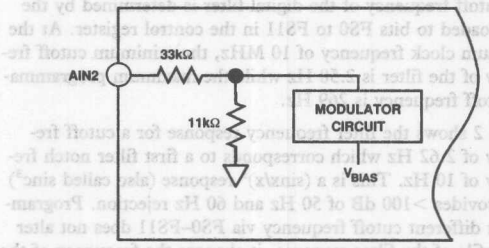
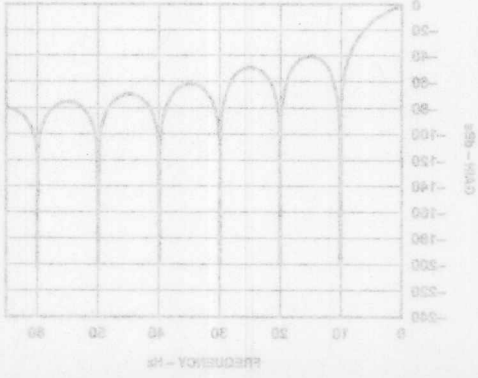


Figure 4. AIN2 of AD7712 Input Impedance



ANALOG INPUT FUNCTIONS

Analog Input Ranges

The analog inputs on the AD7710/AD7712 provide the user with considerable flexibility in terms of analog input voltage ranges. One of the inputs is a differential, programmable gain, input channel which can handle either unipolar or bipolar input signals. The common mode range of this input is from V_{SS} to AV_{DD} provided that the absolute value of the analog input voltage lies between V_{SS} −30 mV and AV_{DD}+30 mV. The second analog input is a single-ended, programmable gain high level input which accepts analog input ranges of 0 to +4 × V_{REF}/GAIN or ±4 × V_{REF}/GAIN.

The dc input leakage current on the AIN1 input is 10 pA maximum at 25°C (±1 nA over temperature). This results in a dc offset voltage developed across the source impedance. However, this dc offset effect can be compensated for by a combination of the differential input capability of the part and its system calibration mode. The dc input current on the AIN2 input depends on the input voltage, For the nominal input voltage range of ±10 V, the input current is ±225 μA typ.

Burn-Out Current

The AIN1(+) input of the AD7710/AD7712 contains a 1 μA current source which can be turned on/off via the control register. This current source can be used in checking that a transducer has not burnt-out or gone open circuit before attempting to take measurements on that channel. If the current is turned on and is allowed flow into the transducer and a measurement of the input voltage on the AIN1 input is taken, it can indicate that the transducer is not functioning correctly. For normal operation, this burn-out current is turned off by writing a 0 to the BO bit in the control register.

Bipolar/Unipolar Inputs

The two analog inputs on the AD7710/AD7712 can accept either unipolar or bipolar input voltage ranges. Bipolar or unipolar options are chosen by programming the B/U bit of the control register. This programs both channels for either unipolar or bipolar operation. Programming the part for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding. The data coding is binary for unipolar inputs and offset binary for bipolar inputs.

Both analog inputs on the AD7710 and the AIN1 input channel of the AD7712 are differential and, as a result, the voltage to which the unipolar and bipolar signals are referenced is the voltage on the AIN(−) input. For example, if AIN(−) is +1.25 V and the part is configured for unipolar operation with a gain of 1 and a V_{REF} of +2.5 V, the input voltage range on the AIN(+) input is +1.25 V to +3.75 V. If AIN(−) is +1.25 V and the part is configured for bipolar mode with a gain of 1 and a V_{REF} of +2.5 V, the analog input range on the AIN(+) input is −1.25 V to +3.75 V. For the AIN2 input of the AD7712, the input signals are referenced to AGND.

REFERENCE INPUT/OUTPUT

The AD7710/AD7712 contains a temperature compensated +2.5 V reference which has an initial tolerance of ±4%. This reference voltage is provided at the REF OUT pin and it can be used as the reference voltage for the part by connecting the REF OUT pin to the REF IN(+) pin. This REF OUT pin is a single-ended output, referenced to AGND, which is capable of providing up to 1mA to an external load. In applications where REF OUT is connected directly to REF IN(+), REF IN(−) should be tied to AGND to provide the nominal +2.5 V reference for the AD7710/AD7712.

The reference inputs of the AD7710/AD7712, REF IN(+) and REF IN(−), provide a differential reference input capability. The common mode range for these differential inputs is from V_{SS} to AV_{DD}. The nominal differential voltage, V_{REF} (REF IN(+)−REF IN(−)), is +2.5 V for specified operation, but the reference voltage can go to +5 V with no degradation in performance provided that the absolute value of REF IN(+) and REF IN(−) does not exceed its AV_{DD} and V_{SS} limits and the V_{BIAS} input voltage range limits are obeyed. The part is also functional with V_{REF} voltages down to 1 V but with degraded performance as the output noise will, in terms of LSB size, be larger. REF IN(+) must always be greater than REF IN(−) for correct operation of the AD7710/AD7712.

Both reference inputs provide a high impedance, dynamic load similar to the AIN1 analog input. The maximum dc input leakage current is 10 pA (±1 nA over temperature) and source resistance may result in gain errors on the part. The reference inputs look like the AIN1 analog input (see Figure 7). In this case, R_{INT} is 5 kΩ typ and C_{INT} varies with gain. The input sample rate is $f_{CLK\ IN}$/512 and does not vary with gain. For gains of 1 to 8 C_{INT} is 20 pF; for a gain of 16 it is 10 pF; for a gain of 32 it is 5 pF; for a gain of 64 it is 2.5 pF, and for a gain of 128 it is 1.25 pF.

The digital filter of the part removes noise from the reference input just as it does with the analog input, and the same limitations apply regarding lack of noise rejection at integer multiples of the sampling frequency. The output noise performance outlined in Tables I and II assumes a clean reference. If the reference noise in the bandwidth of interest is excessive, it can degrade the performance of the AD7710/AD7712. Using the on-chip reference as the reference source for the part (i.e., connecting REF OUT to REF IN) results in somewhat degraded output noise performance from the AD7710/AD7712 for portions of the noise table that are dominated by the device noise. The on-chip reference noise effect is eliminated in ratiometric applications where the reference is used to provide its excitation voltage for the analog front end. Recommended reference voltage sources for the AD7710/AD7712 include the AD780 and AD680 2.5 V references.

V_{BIAS} Input

The V_{BIAS} input determines at what voltage the internal analog circuitry is biased. It essentially provides the return path for analog currents flowing in the modulator and, as such, it should be driven from a low impedance point to minimize errors.

For maximum internal headroom, the V_{BIAS} voltage should be set halfway between AV_{DD} and V_{SS}. The difference between AV_{DD} and (V_{BIAS} + 0.85 × V_{REF}) determines the amount of headroom which the circuit has at the upper end while the difference between V_{SS} and (V_{BIAS} − 0.85 × V_{REF}) determines the amount of headroom the circuit has at the lower end. Care should be taken in choosing a V_{BIAS} voltage to ensure that is stays within prescribed limits. For single +5 V operation, the selected V_{BIAS} voltage must ensure that V_{BIAS} ± 0.85 × V_{REF} does not exceed AV_{DD} or V_{SS} or that the V_{BIAS} voltage itself is greater than V_{SS} + 2.1 V and less than AV_{DD} − 2.1 V. For single +10 V operation or dual ±5 V operation, the selected V_{BIAS} voltage must ensure that V_{BIAS} ± 0.85 × V_{REF} does not exceed AV_{DD} or V_{SS} or that the V_{BIAS} voltage itself is greater than V_{SS} + 3 V or less than AV_{DD} − 3 V. For example, with AV_{DD} = +4.75 V, V_{SS} = 0 V and V_{REF} = +2.5 V, the allowable range for the V_{BIAS} voltage is +2.125 V to +2.625 V. With AV_{DD} = +9.5 V, V_{SS} = 0 V and V_{REF} = +5 V, the range for V_{BIAS} is +4.25 V to +5.25 V. With AV_{DD} = +4.75 V, V_{SS} = −4.75 V and V_{REF} = +2.5 V, the V_{BIAS} range is −2.625 V to +2.625 V.

The V_{BIAS} voltage does have an effect on the AV_{DD} power supply rejection performance of the AD7710/AD7712. If the V_{BIAS} voltage tracks the AV_{DD} supply, it improves the power supply rejection from the AV_{DD} supply line from 80 dB to 95 dB. Using an external Zener diode, connected between the AV_{DD} line and V_{BIAS}, as the source for the V_{BIAS} voltage gives the improvement in AV_{DD} power supply rejection performance.

USING THE AD7710/AD7712: SYSTEM DESIGN CONSIDERATIONS

The AD7710/AD7712 operates differently from successive approximation ADCs or integrating ADCs. Since it samples the signal continuously, like a tracking ADC, there is no need for a start convert command. The output register is updated at a rate determined by the first notch of the filter and the output can be read at any time, either synchronously or asynchronously.

Clocking

The AD7710/AD7712 requires a master clock input, which may be an external TTL/CMOS compatible clock signal applied to the MCLK IN pin with the MCLK OUT pin left unconnected. Alternatively, a crystal of the correct frequency can be connected between MCLK IN and MCLK OUT, in which case the clock circuit will function as a crystal controlled oscillator. For lower clock frequencies, a ceramic resonator may be used instead of the crystal. For these lower frequency oscillators, external capacitors may be required on either the ceramic resonator or on the crystal.

The input sampling frequency, the modulator sampling frequency, the −3 dB frequency, output update rate and calibration time are all directly related to the master clock frequency, $f_{CLK\ IN}$. Reducing the master clock frequency by a factor of 2 will halve the above frequencies and update rate and will double the calibration time.

The current drawn from the DV_{DD} power supply is also directly related to $f_{CLK\ IN}$. Reducing $f_{CLK\ IN}$ by a factor of 2 will halve the DV_{DD} current but will not affect the current drawn from the AV_{DD} power supply.

System Synchronization

If multiple AD7710/AD7712s are operated from a common master clock, they can be synchronized to update their output registers simultaneously. A falling edge on the $\overline{SYNC}$ input resets the filter and places the AD7710/AD7712 into a consistent, known state. A common signal to the AD7710/AD7712s' $\overline{SYNC}$ inputs will synchronize their operation. This would normally be done after each AD7710/AD7712 has performed its own calibration or has had calibration coefficients loaded to it.

The $\overline{SYNC}$ input can also be used to reset the digital filter in systems where the turn-on time of the digital power supply (DV_{DD}) is very long. In such cases, the AD7710/AD7712 will start operating internally before the DV_{DD} line has reached its minimum operating level, +4.75 V. With a low DV_{DD} voltage, the AD7710/AD7712's internal digital filter logic does not operate correctly. Thus, the AD7710/AD7712 may have clocked itself into an incorrect operating condition by the time that DV_{DD} has reached its correct level. The digital filter will be reset upon issue of a calibration command (whether it is self-calibration, system calibration or background calibration) to the AD7710/AD7712. This ensures correct operation of the AD7710/AD7712. In systems where the power-on default conditions of the AD7710/AD7712 are acceptable, and no calibration is performed after power-on, issuing a $\overline{SYNC}$ pulse to the AD7710/AD7712 will reset the AD7710/AD7712's digital filter logic. An R, C on the $\overline{SYNC}$ line, with R, C time constant longer than the DV_{DD} power-on time, will perform the $\overline{SYNC}$ function.

Accuracy

Sigma-Delta ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no missing codes performance. The AD7710/AD7712 achieves excellent linearity by the use of high quality, on-chip silicon dioxide capacitors, which have a very low capacitance/voltage coefficient. The device also achieves low input drift through the use of chopper stabilized techniques in its input stage. To ensure excellent performance over time and temperature, the AD7710/AD7712 uses digital calibration techniques that minimize offset and gain error.

Autocalibration

Autocalibration on the AD7710/AD7712 removes offset and gain errors from the device. A calibration routine should be initiated on the device whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the selected gain, filter notch or bipolar/unipolar input range. However, if the AD7710/AD7712 is in its background calibration mode, the above changes are all automatically taken care of (after the settling time of the filter has been allowed for).

The AD7710/AD7712 offers self-calibration, system calibration and background calibration facilities. For calibration to occur on the selected channel, the on-chip microcontroller must record the modulator output for two different input conditions. These are "zero scale" and "full-scale" points. With these readings, the microcontroller can calculate the gain slope for the input to output transfer function of the converter. Internally, the part works with a resolution of 33 bits to determine its conversion result of either 16 bits or 24 bits.

The AD7710/AD7712 also provides the facility to write to the on-chip calibration registers and in this manner the span and offset for the part can be adjusted by the user. The offset calibration register contains a value which is subtracted from all conversion results, while the full-scale calibration register contains a value which is multiplied by all conversion results. The offset calibration coefficient is subtracted from the result prior to the multiplication by the full-scale coefficient. In the first three modes outlined here, the $\overline{DRDY}$ indicates that calibration is complete by going low. If $\overline{DRDY}$ is low before (or goes low during) the calibration command, it may take up to one modulator cycle before $\overline{DRDY}$ goes high to indicate that calibration is in progress. Therefore, the $\overline{DRDY}$ line should be ignored for up to one modulator cycle after the last bit of the calibration command is written to the control register.

Self-Calibration

In the self-calibration mode with a unipolar input range, the zero scale point used in determining the calibration coefficients is with both inputs shorted (i.e., AIN(+) = AIN(−) = V_{BIAS} for differential inputs and AIN = V_{BIAS} for single-ended inputs) and the full-scale point is V_{REF}. The zero scale coefficient is determined by converting an internal shorted inputs node. The full scale coefficient is determined from the span between this shorted inputs conversion and a conversion on an internal V_{REF} node. The self-calibration mode is invoked by writing the appropriate values (0, 0, 1) to the MD2, MD1 and MD0 bits of the control register. In this calibration mode, the shorted inputs node is switched in to the modulator first and a conversion is performed; the V_{REF} node is then switched in and another conversion is performed. When the calibration sequence is complete, the calibration coefficients updated and the filter resettled to the analog input voltage, the $\overline{DRDY}$ output goes low. The self-calibration procedure takes into account the selected gain on the PGA.

For bipolar input ranges in the self-calibrating mode, the sequence is very similar to that just outlined. In this case, the two points which the AD7710/AD7712 calibrates are midscale (bipolar zero) and positive full-scale.

System Calibration

System calibration allows the AD7710/AD7712 to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self-calibration but uses voltage values presented by the system to the AIN inputs for the zero and full-scale points. System calibration is a two-step process. The zero scale point must be presented to the converter first. It must be applied to the converter before the calibration step is initiated and remain stable until the step is complete. System calibration is initiated by writing the appropriate values (0, 1, 0) to the MD2, MD1 and MD0 bits of the control register. The $\overline{DRDY}$ output from the device will signal when the step is complete by going low. After the zero scale point is calibrated, the full-scale point is applied and the second step of the calibration process is initiated by again writing the appropriate values (0, 1, 1) to MD2, MD1 and MD0. Again the full-scale voltage must be set up before the calibration is initiated and it must remain stable throughout the calibration step. $\overline{DRDY}$ goes low at the end of this second step to indicate that the system calibration is complete. In the unipolar mode, the system calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

This two-step system calibration mode offers another feature. After the sequence has been completed, additional offset or gain calibrations can be performed by themselves to adjust the zero reference point or the system gain. This is achieved by performing the first step of the system calibration sequence (by writing 0, 1, 0 to MD2, MD1, MD0). This will adjust the zero scale or offset point but will not change the slope factor from what was set during a full system calibration sequence.

System calibration can also be used to remove any errors from an antialiasing filter on the analog input. A simple R, C antialiasing filter on the front end may introduce a gain error on the analog input voltage but the system calibration can be used to remove this error.

System Offset Calibration

System offset calibration is a variation of both the system calibration and self-calibration. In this case, the zero scale point for the system is presented to the AIN input of the converter. System offset calibration is initiated by writing 1, 0, 0 to MD2, MD1, MD0. The system zero scale coefficient is determined by converting the voltage applied to the AIN input, while the full-scale coefficient is determined from the span between this AIN conversion and a conversion on V_{REF}. The zero scale point should be applied to the AIN input for the duration of the calibration sequence. This is a one step calibration sequence with $\overline{DRDY}$ going low when the sequence is completed. In the unipolar mode, the system offset calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

Background Calibration

The AD7710/AD7712 also offers a background calibration mode where the part interleaves its calibration procedure with its normal conversion sequence. In the background calibration mode, the same voltages are used as the calibration points as are used in the self-calibration mode, i.e., shorted inputs and V_{REF}. The background calibration mode is invoked by writing 1, 0, 1 to MD2, MD1, MD0 of the control register. When invoked, the background calibration mode reduces the output data rate of the

performing calibration and automatically updating its calibration coefficients. As a result, the effects of temperature drift, supply sensitivity and time drift on zero and full scale errors are automatically removed. When the background calibration mode is turned on, the part will remain in this mode until bits MD2, MD1 and MD0 of the control register are changed. With background calibration mode on, the first result from the AD7710/ond output update will have settled to 100% of the final value.

Table VI summarizes the calibration modes and the calibration points associated with them. It also gives the duration from when the calibration is invoked to when valid data is available to the user.

Table VI. Calibration Truth Table

Cal Type	MD2, MD1, MD0	Zero Scale Cal	Full-Scale Cal	Sequence	Duration
Self-Cal	0, 0, 1	Shorted Inputs	V_{REF}	One Step	9 × 1/Output Rate
System Cal	0, 1, 0	AIN	–	Two Step	4 × 1/Output Rate
System Cal	0, 1, 1	–	AIN	Two Step	4 × 1/Output Rate
System Offset Cal	1, 0, 0	AIN	V_{REF}	One Step	9 × 1/Output Rate
Background Cal	1, 0, 1	Shorted Inputs	V_{REF}	One Step	6 × 1/Output Rate

Span and Offset Limits

Whenever a system calibration mode is used, there are limits on the amount of offset and span that can be accommodated. The range of input span in both the unipolar and bipolar modes for both inputs on the AD7710 and AIN1 of the AD7712 has a minimum value of $0.8 \times V_{REF}/GAIN$ and a maximum value of $2.1 \times V_{REF}/GAIN$. For AIN2 on the AD7712, both numbers are a factor of 4 higher.

The amount of offset that can be accommodated depends on whether the unipolar or bipolar mode is being used. This offset range is limited by the requirement that the positive full-scale calibration limit is $\leq 1.05 \times V_{REF}/GAIN$ for the differential inputs. Therefore, the offset range plus the span range cannot exceed $1.05 \times V_{REF}/GAIN$ for the differential inputs. If the span is at its minimum ($0.8 \times V_{REF}/GAIN$) the maximum the offset can be is ($0.25 \times V_{REF}/GAIN$) for the differential inputs. For AIN2 of AD7712, both ranges are multiplied by a factor of 4.

In the bipolar mode, the system offset calibration range is again restricted by the span range. The span range of the converter in bipolar mode is equidistant around the voltage used for the zero scale point thus the offset range plus half the span range cannot exceed ($1.05 \times V_{REF}/GAIN$) for the differential inputs. If the span is set to $2 \times V_{REF}/GAIN$, the offset span cannot move more than $\pm(0.05 \times V_{REF}/GAIN)$ before the endpoints of the transfer function exceed the input overrange limits $\pm(1.05 \times V_{REF}/GAIN)$ for the differential inputs. If the span range is set to the minimum $\pm(0.4 \times V_{REF}/GAIN)$ the maximum allowable offset range is $\pm(0.65 \times V_{REF}/GAIN)$ for the differential inputs. Once again, for AIN2 of AD7712, both ranges are multiplied by a factor of 4.

POWER-UP AND CALIBRATION

On power-up, the AD7710/AD7712 performs an internal reset which sets the contents of the control register to a known state. However, to ensure correct calibration for the device a calibration routine should be performed after power-up.

The power dissipation and temperature drift of the AD7710/AD7712 are low and no warm-up time is required before the initial calibration is performed. However, if an external reference is being used, this reference must have stabilized before calibration is initiated.

Drift Considerations

The AD7710/AD7712 uses chopper stabilization techniques to minimize input offset drift. Charge injection in the analog switches and dc leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. The dc input leakage current is essentially independent of the selected gain. Gain drift within the converter depends primarily upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter or by operating the part in the background calibration mode. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. Integral and differential linearity errors are not significantly affected by temperature changes.

POWER SUPPLIES AND GROUNDING

Since the analog inputs and reference input are differential, most of the voltages in the analog modulator are common-mode voltages. V_{BIAS} provides the return path for most of the analog currents flowing in the analog modulator. As a result, the V_{BIAS} input should be driven from a low impedance to minimize errors due to charging/discharging impedances on this line. When the internal reference is used as the reference source for the part, AGND is the ground return for this reference voltage.

The analog and digital supplies to the AD7710/AD7712 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital supply (DV_{DD}) must never exceed the analog positive supply (AV_{DD}) by more than 0.3 V. Power supply sequencing therefore is important. If separate analog and digital supplies are used, care must be taken to ensure that the analog supply is powered up first. If this cannot be ensured or if DV_{DD} can exceed AV_{DD} at any other time, the protection scheme outlined in Figure 5 is recommended to protect the device. In systems where $AV_{DD} = +5$ V and $DV_{DD} = +5$ V, it is recommended that AV_{DD} and DV_{DD} are driven from the same +5 V supply, although each supply should be decoupled separately. It is preferable that the common supply is the system's analog +5 V supply.

It is also important that power is applied to the AD7710/AD7712 before signals at REF IN, AIN or the logic input pins in order to avoid latch-up. If separate supplies are used for the AD7710/AD7712 and the system digital circuitry, then the AD7710/AD7712 should be powered up first. If it is not possible to guarantee this, then current limiting resistors should be placed in series with the logic inputs.

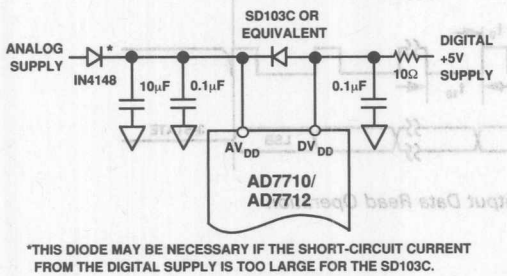


Figure 5. Protection Scheme for DV_{DD} Powering-Up Before AV_{DD}

DIGITAL INTERFACE

The AD7710/AD7712's serial communications port provides a flexible arrangement to allow easy interfacing to industry standard microprocessors, microcontrollers and digital signal processors. A serial read to the part can access data from the output register, the control register or from the calibration registers. A serial write to the part can write data to the control register or the calibration registers.

Two different modes of operation are available, optimized for different types of interface where the AD7710/AD7712 can act either as master in the system (it provides the serial clock) or as slave (an external serial clock can be provided to the AD7710/AD7712). These two modes, labelled self-clocking mode and external clocking mode, are discussed in detail in the following sections.

Self-Clocking Mode

The part is configured for its self-clocking mode by tying the MODE pin high. In this mode, the part provides the serial clock signal used for the transfer of data to and from the AD7710/AD7712. This self-clocking mode can be used with processors that allow an external device to clock their serial port including most digital signal processors and microcontrollers such as the 68HC11 and 68HC05. It also allows easy interfacing to serial parallel conversion circuits in systems with parallel data communication, allowing interfacing to 74XX299 Universal Shift registers without any additional decoding. In the case of shift registers, the serial clock line should have a pull-down resistor instead of the pull-up resistor shown in Figure 6 and Figure 7.

Read Operation

Data can be read from either the output register, the control register or the calibration registers. A0 determines whether the data read accesses data from the control register or from the output/calibration registers. This A0 signal must remain valid for the duration of the serial read operation. With A0 high, data is accessed from either the output register or from the calibration registers. With A0 low, data is accessed from the control register.

The function of the $\overline{\text{DRDY}}$ line is dependent only on the output update rate of the device and the reading of the output data register. $\overline{\text{DRDY}}$ goes low when a new data word is available in the output data register. It is reset high when the last bit of data (either 16th bit or 24th bit) is read from the output register. If data is not read from the output register, the $\overline{\text{DRDY}}$ line will remain low. The output register will continue to be updated at the output update rate but $\overline{\text{DRDY}}$ will not indicate this. A read from the device in this circumstance will access the most recent word in the output register. If a new data word becomes available to the output register while data is being read from the output register, $\overline{\text{DRDY}}$ will not indicate this and the new data word will be lost to the user. $\overline{\text{DRDY}}$ is not affected by reading from the control register or the calibration registers.

Data can only be accessed from the output data register when $\overline{\text{DRDY}}$ is low. If $\overline{\text{RFS}}$ goes low with $\overline{\text{DRDY}}$ high, no data transfer will take place. $\overline{\text{DRDY}}$ does not have any effect on reading data from the control register or from the calibration registers.

Figures 6a and 6b show timing diagrams for reading from the part in the self-clocking mode. Figure 6a shows a situation where all the data is read from the part in one read operation. Figure 6b shows a situation where the data is read from the AD7710/AD7712 over a number of read operations. Both read operations show a read from the part's output data register. A read from the control register or calibration registers is similar but in these cases the $\overline{\text{DRDY}}$ line is not related to the read function. Depending on the output update rate, it can go low at any stage in the control/calibration register read cycle without affecting the read and its status should be ignored. A read operation from either the control or calibration registers must always read 24 bits of data from the respective register.

Figure 6a shows a read operation from the part where $\overline{\text{RFS}}$ remains low for the duration of the data word transmission. For the timing diagram shown, it is assumed that there is a pull-up resistor on the SCLK output. With $\overline{\text{DRDY}}$ low, the $\overline{\text{RFS}}$ input is brought low. $\overline{\text{RFS}}$ going low enables the serial clock of the AD7710/AD7712 and also places the MSB of the word on the serial data line. All subsequent data bits are clocked out on a high to low transition of the serial clock and are valid prior to the following rising edge of this clock. The final active falling edge of SCLK clocks out the LSB and this LSB is valid prior to the final active rising edge of SCLK. Coincident with the next falling edge of SCLK, $\overline{\text{DRDY}}$ is reset high. $\overline{\text{DRDY}}$ going high turns off the SCLK and the SDATA outputs. This means that the data hold time for the LSB is slightly shorter than for all other bits.

Figure 6b shows a timing diagram for a read operation where $\overline{\text{RFS}}$ returns high during the transmission of the word and returns low again to access the rest of the data word. As before, the waveform for SCLK assumes that there is a pull-up resistor on this line. Timing parameters and functions are very similar to that outlined for Figure 6a, but Figure 6b has a number of additional times to show timing relationships when $\overline{\text{RFS}}$ returns high in the middle of transferring a word.

$\overline{\text{RFS}}$ should return high during a low time of SCLK. On the rising edge of $\overline{\text{RFS}}$, the SCLK and SDATA outputs are turned

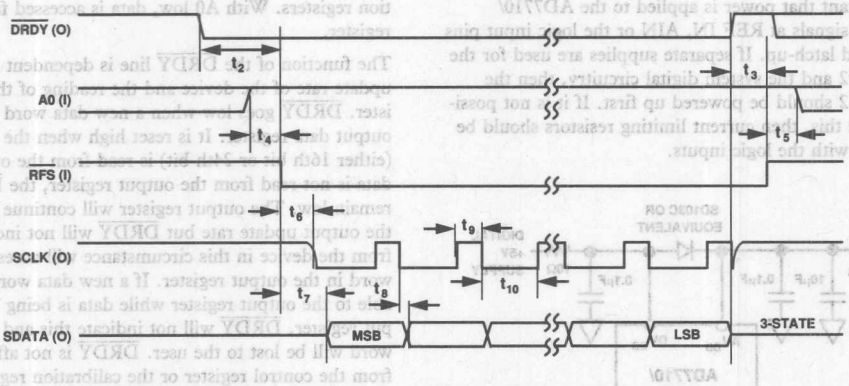


Figure 6a. Self-Clocking Mode, Output Data Read Operation

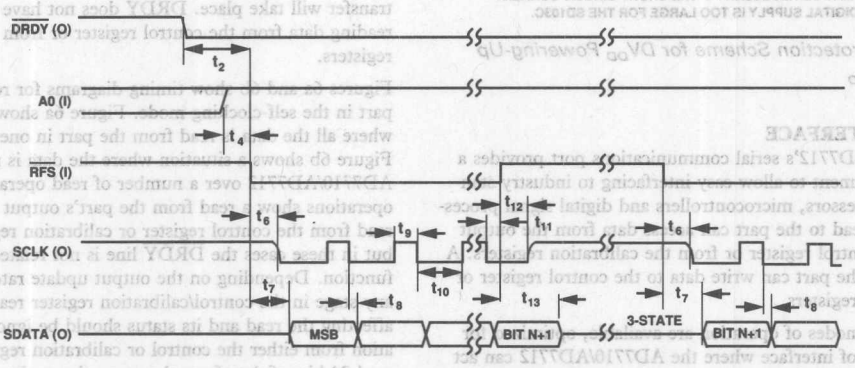


Figure 6b. Self-Clocking Mode, Output Data Read Operation (RFS Returns High During Read Operation)

off. DRDY remains low and will remain low until all bits of the data word are read from the part, regardless of the number of times RFS changes state during the read operation. Depending on the time between the falling edge of SCLK and the rising edge of RFS, the next bit (BIT N + 1) may appear on the databus before RFS goes high. When RFS returns low again, it turns on the SCLK output and activates the SDATA output. When the entire word is transmitted, the DRDY line will go high turning off the SDATA and SCLK lines as per Figure 6a.

Write Operation

Data can be written to either the control register or calibration registers. In either case, the write operation is not affected by the DRDY line and the write operation does not have any effect on the status of DRDY. A write operation to the control register or the calibration register must always write 24 bits to the respective register.

Figure 7a shows a write operation to the AD7710/AD7712 with TFS remaining low for the duration of the write operation. A0 determines whether a write operation transfers data to the control register or to the calibration registers. This A0 signal must remain valid for the duration of the serial write operation. The falling edge of TFS enables the internally generated SCLK output. The serial data to be loaded to the AD7710/AD7712 must be valid on the rising edge of this SCLK signal. Data is clocked into the AD7710/AD7712 on the rising edge of the SCLK signal with the MSB transferred first. On the last active high time of SCLK, the LSB is loaded to the AD7710/AD7712. Subsequent to the next falling edge of SCLK, the SCLK output is turned off. (The timing diagram of Figure 7a assumes a pull-up resistor on the SCLK line.)

Figure 7b shows a timing diagram for a write operation to the AD7710/AD7712 with TFS returning high during the write operation and returning low again to write the rest of the data word. Once again, the timing diagram of Figure 7b assumes a pull-up resistor on the SCLK output. Timing parameters and functions are very similar to that outlined for Figure 7a but Figure 7b has a number of additional times to show timing relationships when TFS returns high in the middle of transferring a word.

The falling edge of TFS again initiates the SCLK output and data to be loaded to the AD7710/AD7712 must be valid prior to the rising edge of this SCLK signal. The rising edge of TFS turns off the SCLK output. TFS should return high during the low time of SCLK. When TFS returns low again, it turns on the SCLK output. When all data bits have been written to the device, the SCLK output is turned off as per Figure 7a.

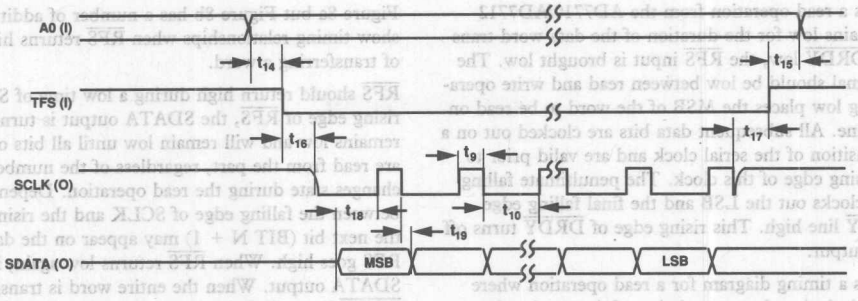


Figure 7a. Self-Clocking Mode, Control/Calibration Register Write Operation

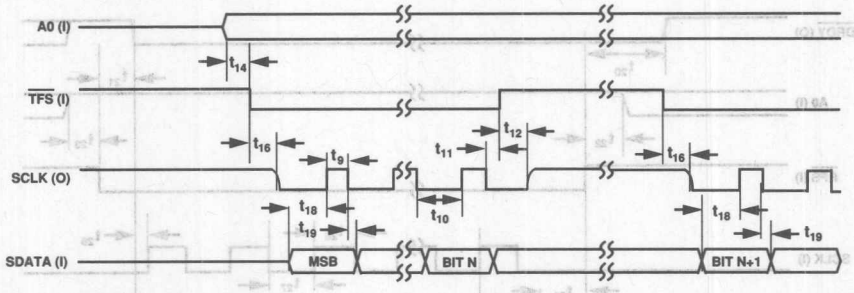


Figure 7b. Self-Clocking Mode, Control/Calibration Register Write Operation (TFS Returns High During Write Operation)

External Clocking Mode

The AD7710/AD7712 is configured for its external clocking mode by tying the MODE pin low. In this mode, SCLK of the part is configured as an input and an external serial clock must be provided to this SCLK pin. This external clocking mode is designed for direct interface to systems which provide a serial clock output that is synchronized to the serial data output, including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

Read Operation

As with the self-clocking mode, data can be read from either the output register, the control register or the calibration registers. A0 determines whether the data read accesses data from the control register or from the output/calibration registers. This A0 signal must remain valid for the duration of the serial read operation. With A0 high, data is accessed from either the output register or from the calibration registers. With A0 low, data is accessed from the control register.

The function of the $\overline{\text{DRDY}}$ line is dependent only on the output update rate of the device and the reading of the output data register. $\overline{\text{DRDY}}$ goes low when a new data word is available in the output data register. It is reset high when the last bit of data (either 16th bit or 24th bit) is read from the output register. If data is not read from the output register, the $\overline{\text{DRDY}}$ line will remain low. The output register will continue to be updated at the output update rate but $\overline{\text{DRDY}}$ will not indicate this. A read from the device in this circumstance will access the most recent word in the output register. If a new data word becomes available to the output register while data is being read from the output register, $\overline{\text{DRDY}}$ will not indicate this and the new data word will be lost to the user. $\overline{\text{DRDY}}$ is not affected by reading from the control register or the calibration register.

Data can only be accessed from the output data register when $\overline{\text{DRDY}}$ is low. If $\overline{\text{RFS}}$ goes low while $\overline{\text{DRDY}}$ is high, no data transfer will take place. $\overline{\text{DRDY}}$ does not have any effect on reading data from the control register or from the calibration registers.

Figures 8a and 8b show timing diagrams for reading from the part's in the external clocking mode. Figure 8a shows a situation where all the data is read from the part in one read operation. Figure 8b shows a situation where the data is read from the part over a number of read operations. Both read operations show a read from the part's output data register. A read from the control register or calibration registers is similar but in these cases the $\overline{\text{DRDY}}$ line is not related to the read function. Depending on the output update rate, it can go low at any stage in the control/calibration register read cycle without affecting the read and its status should be ignored. A read operation from either the control or calibration registers must always read 24 bits of data from the respective register.

Figure 8a shows a read operation from the AD7710/AD7712 where $\overline{RFS}$ remains low for the duration of the data word transmission. With $\overline{DRDY}$ low, the $\overline{RFS}$ input is brought low. The input SCLK signal should be low between read and write operations. $\overline{RFS}$ going low places the MSB of the word to be read on the serial data line. All subsequent data bits are clocked out on a high to low transition of the serial clock and are valid prior to the following rising edge of this clock. The penultimate falling edge of SCLK clocks out the LSB and the final falling edge resets the $\overline{DRDY}$ line high. This rising edge of $\overline{DRDY}$ turns off the serial data output.

Figure 8b shows a timing diagram for a read operation where $\overline{RFS}$ returns high during the transmission of the word and returns low again to access the rest of the data word. Timing parameters and functions are very similar to that outlined for Figure 8a but Figure 8b has a number of additional times to show timing relationships when $\overline{RFS}$ returns high in the middle of transferring a word.

$\overline{RFS}$ should return high during a low time of SCLK. On the rising edge of $\overline{RFS}$, the SDATA output is turned off. $\overline{DRDY}$ remains low and will remain low until all bits of the data word are read from the part, regardless of the number of times $\overline{RFS}$ changes state during the read operation. Depending on the time between the falling edge of SCLK and the rising edge of $\overline{RFS}$, the next bit (BIT N + 1) may appear on the databus before $\overline{RFS}$ goes high. When $\overline{RFS}$ returns low again, it activates the SDATA output. When the entire word is transmitted, the $\overline{DRDY}$ line will go high, turning off the SDATA output as per Figure 8a.

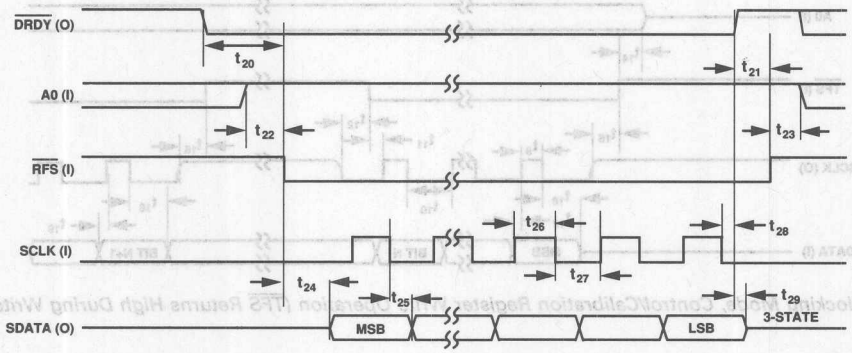


Figure 8a. External Clocking Mode, Output Data Read Operation

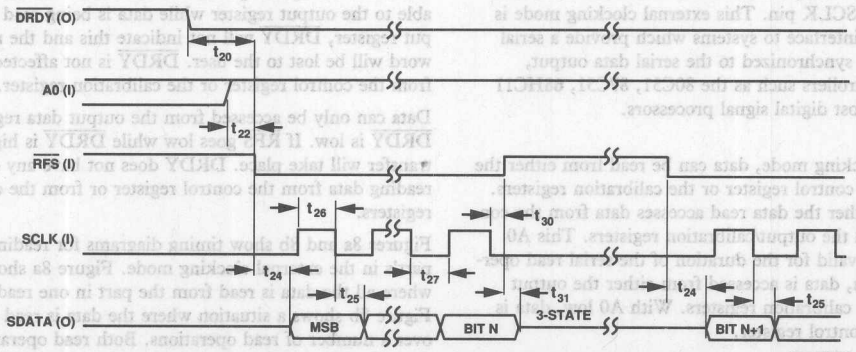


Figure 8b. External Clocking Mode, Output Data Read Operation ($\overline{RFS}$ Returns High During Read Operation)

Write Operation

Data can be written to either the control register or calibration registers. In either case, the write operation is not affected by the $\overline{DRDY}$ line and the write operation does not have any effect on the status of $\overline{DRDY}$. A write operation to the control register or the calibration register must always write 24 bits to the respective register.

Figure 9a shows a write operation to the part with $\overline{TFS}$ remaining low for the duration of the write operation. A0 determines whether a write operation transfers data to the control register or to the calibration registers. This A0 signal must remain valid for the duration of the serial write operation. As before, the serial clock line should be low between read and write operations. The serial data to be loaded to the part must be valid on the high level of the externally applied SCLK signal. Data is clocked into the part on the high level of this SCLK signal with the MSB transferred first. On the last active high time of SCLK, the LSB is loaded to the part.

Figure 9b shows a timing diagram for a write operation to the AD7710/AD7712 with $\overline{TFS}$ returning high during the write operation and returning low again to write the rest of the data word. Timing parameters and functions are very similar to that outlined for Figure 9a, but Figure 9b has a number of additional times to show timing relationships when $\overline{TFS}$ returns high in the middle of transferring a word.

Data to be loaded to the part must be valid for 5/2 MCLK IN cycles prior to the falling edge of the SCLK signal. $\overline{TFS}$ should return high during the low time of SCLK. After $\overline{TFS}$ returns low again, the next bit of the data word to be loaded to the part is clocked in on next high level of the SCLK input. On the last active high time of the SCLK input, the LSB is loaded to the part.

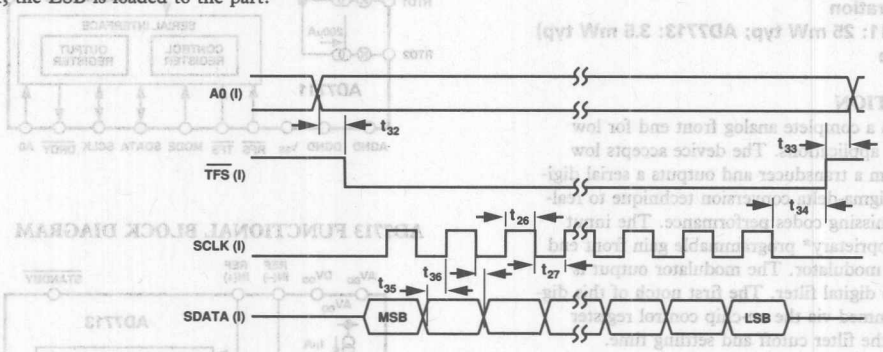


Figure 9a. External Clocking Mode, Control/Calibration Register Write Operation

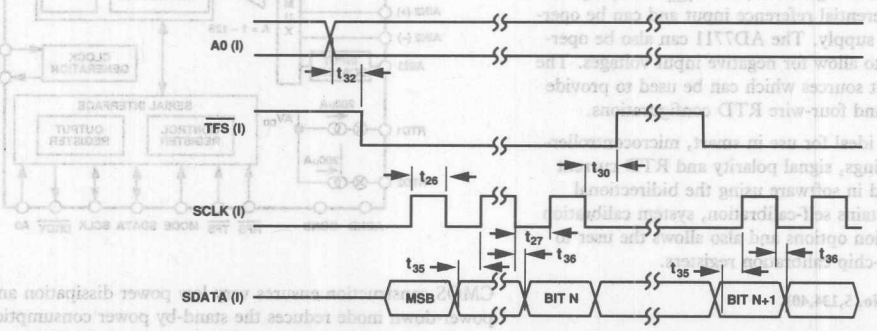


Figure 9b. External Clocking Mode, Control/Calibration Register Write Operation ($\overline{TFS}$ Returns High During Write Operation)

LC²MOS Signal Conditioning ADCs with RTD Excitation Currents

AD7711/AD7713

FEATURES

Charge Balancing ADC
24 Bits No Missing Codes
±0.0015% Nonlinearity
Programmable Gain Front End
Gains from 1 to 128
Three Input Channels (AD7713)
Two Input Channels (AD7711)
Low-Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
RTD Excitation Current Sources
Bidirectional Microcontroller Serial Interface
Single Supply Operation
Low Power (AD7711: 25 mW typ; AD7713: 3.5 mW typ)
Power-Down Mode

GENERAL DESCRIPTION

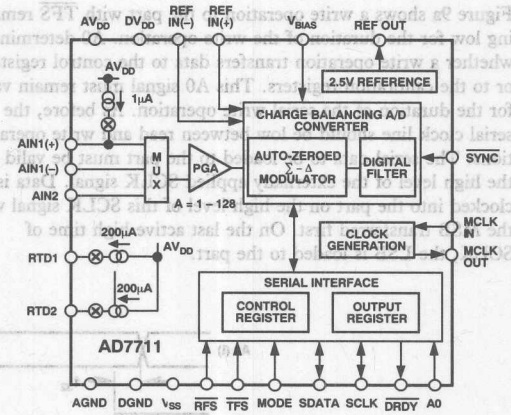
The AD7711/AD7713 is a complete analog front end for low frequency measurement applications. The device accepts low level signals directly from a transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The input signal is applied to a proprietary* programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The AD7711 features one differential analog input and one single-ended analog input. The AD7713 features two differential inputs and one single-ended high level ($4 \times V_{REF}$/Gain) input. Both parts feature a differential reference input and can be operated from a single +5 V supply. The AD7711 can also be operated from dual supplies to allow for negative input voltages. The parts provide two current sources which can be used to provide excitation in three-wire and four-wire RTD configurations.

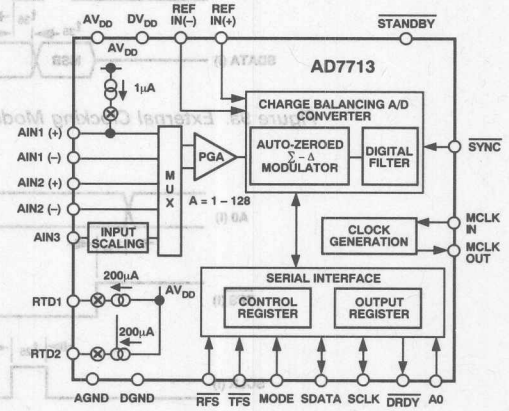
The AD7711/AD7713 is ideal for use in smart, microcontroller-based systems. Gain settings, signal polarity and RTD current control can be configured in software using the bidirectional serial port. The part contains self-calibration, system calibration and background calibration options and also allows the user to read and to write the on-chip calibration registers.

*Protected by U.S. Patent No. 5,134,401.

AD7711 FUNCTIONAL BLOCK DIAGRAM



AD7713 FUNCTIONAL BLOCK DIAGRAM



CMOS construction ensures very low power dissipation and a power-down mode reduces the stand-by power consumption to 7 mW typical (AD7711) and 300 μW typical (AD7713). The part is available in a 24-pin, 0.3 inch wide, plastic and hermetic dual-in-line package (DIP) as well as a 24-lead small outline (SOIC) package.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7713—SPECIFICATIONS

(AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; REF IN(+) = +2.5 V; REF IN(−) = AGND; MCLK IN = 2 MHz, unless otherwise stated. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. For Filter Notches ≤ 12 Hz
	22	Bits min	For Filter Notch = 20 Hz
	18	Bits min	For Filter Notch = 50 Hz
	15	Bits min	For Filter Notch = 100 Hz
	12	Bits min	For Filter Notch = 200 Hz
Output Noise	See Tables I & II		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity			
@ 25°C	±0.0045	% of FSR max	Filter Notches ≤ 12 Hz; Typically ±0.0015%
T_{MIN} to T_{MAX}	±0.0075	% of FSR max	Filter Notches ≤ 12 Hz
Positive Full-Scale Error[2, 3]	See Note 4		
Full-Scale Drift[5]	3/GAIN	µV/°C typ	For Gains of 1, 2, 4, 8
	0.35	µV/°C typ	For Gains of 16, 32, 64, 128
Unipolar Offset Error[2]	See Note 4		
Unipolar Offset Drift[5]	2.5/GAIN	µV/°C typ	For Gains of 1, 2, 4, 8
	0.3	µV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Zero Error[2]	See Note 4		
Bipolar Zero Drift[5]	2.5/GAIN	µV/°C typ	For Gains of 1, 2, 4, 8
	0.3	µV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Negative Full-Scale Error[2]	±0.006	% of FSR max	Typically ±0.0015%
Bipolar Negative Full-Scale Drift[5]	4/GAIN	µV/°C typ	For Gains of 1, 2, 4, 8
	0.5	µV/°C typ	For Gains of 16, 32, 64, 128
ANALOG INPUTS			
Input Sampling Rate, f_S	See Table III		
Normal Mode 50 Hz Rejection[6]	100	dB min	For Filter Notches of 2, 5, 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Normal Mode 60 Hz Rejection[6]	100	dB min	For Filter Notches of 2, 6, 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
AIN1, AIN2[7]			
Input Voltage Range[8]			For Normal Operation. Depends on Gain Selected.
	0 to $+V_{REF}$[9]	V max	Unipolar Input Range (B/U Bit of Control Register = 1)
	$\pm V_{REF}$	V max	Bipolar Input Range (B/U Bit of Control Register = 0)
Common-Mode Rejection (CMR)	92	dB min	At DC
Common-Mode 50 Hz Rejection[6]	150	dB min	For Filter Notches of 2, 5, 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Common-Mode 60 Hz Rejection[6]	150	dB min	For Filter Notches of 2, 6, 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode Voltage Range[10]	AGND to AV_{DD}	V min to V max	
DC Input Leakage Current @ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[6]	20	pF max	
AIN3			
Input Voltage Range	0 to +4 × V_{REF}	V max	For Normal Operation. Depends on Gain Selected.
Gain Error[11]	±0.05	% typ	Additional Error Contributed by Resistor Attenuator
Gain Drift	1	ppm/°C typ	Additional Drift Contributed by Resistor Attenuator
Offset Error[11]	8	mV max	Additional Error Contributed by Resistor Attenuator

NOTES

[1]Temperature ranges are as follows: A Version, −40°C to +85°C; S Version, −55°C to +125°C. See also Note 16.

[2]Applies after calibration at the temperature of interest.

[3]Positive full-scale error applies to both unipolar and bipolar input ranges.

[4]These errors will be of the order of the output noise of the part as shown in Table I.

[5]Recalibration at any temperature or use of the background calibration mode will remove these drift errors.

[6]These numbers are guaranteed by design and/or characterization.

[7]The AIN1 and AIN2 analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance depends on the selected gain.

[8]The analog input voltage range on the AIN1(+) and AIN2(+) inputs is given here with respect to the voltage on the AIN1(−) and AIN2(−) inputs. The input voltage range on the AIN3 input is with respect to AGND. The absolute voltage on the AIN1 and AIN2 inputs should not go more positive than AV_{DD} + 30 mV or more negative than AGND − 30 mV.

[9]V_{REF} = REF IN(+) − REF IN(−).

[10]This common-mode voltage range is allowed provided that the input voltage on AIN(+) and AIN(−) does not exceed AV_{DD} + 30 mV and AGND − 30 mV.

[11]This error can be removed using the system calibration capabilities of the AD7711/AD7713. This error is not removed by the AD7711/AD7713's self-calibration feature. The offset drift on the AIN3 input is four times the value given in the Static Performance section.

AD7713—SPECIFICATIONS

Parameter	A, S Versions[1]	Units	Conditions/Comments
REFERENCE INPUT			
REF IN(+) – REF IN(–) Voltage	+2.5 to AV_{DD}/1.8	V min to V max	For Specified Performance. Part Is Functional with Lower V_{REF} Voltages
Input Sampling Rate, f_S	$f_{CLK\ IN}$/512		
Normal-Mode 50 Hz Rejection[6]	100	dB min	For Filter Notches of 2, 5, 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Normal-Mode 60 Hz Rejection[6]	100	dB min	For Filter Notches of 2, 6, 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode Rejection (CMR)	100	dB min	At DC
Common-Mode 50 Hz Rejection[6]	150	dB min	For Filter Notches of 2, 5, 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Common-Mode 60 Hz Rejection[6]	150	dB min	For Filter Notches of 2, 6, 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode Voltage Range[10]	AGND to AV_{DD}	V min to V max	
DC Input Leakage Current @ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[12]	9	pF typ	
TRANSDUCER BURN OUT			
Current	20	nA nom	
Initial Tolerance	±10	% typ	
Drift	0.1	%/°C typ	
RTD EXCITATION CURRENTS (RTD1, RTD2)			
Output Current	200	μA nom	
Initial Tolerance	±20	% max	
Drift	20	ppm/°C typ	
Initial Matching	±1	% max	Matching Between RTD1 and RTD2 Currents
Drift Matching	3	ppm/°C typ	Matching Between RTD1 and RTD2 Current Drift
Line Regulation (AV_{DD})	200	nA/V max	AV_{DD} = +5 V
Load Regulation	200	nA/V max	
SYSTEM CALIBRATION			
AIN1, AIN2			
Positive Full-Scale Calibration Limit[13]	+(1.05 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[13]	–(1.05 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[14, 15]	–(1.05 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[14]	+0.8 × V_{REF}/GAIN	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	+(2.1 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
AIN3			
Positive Full-Scale Calibration Limit[13]	+(4.2 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[15]	0 to V_{REF}/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span	+3.2 × V_{REF}/GAIN	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	+(4.2 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)

NOTES

[12]Sample tested at +25°C to ensure compliance.

[13]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale, then the device will output all 0s.

[14]These calibration and span limits apply provided the absolute voltage on the AIN1 and AIN2 analog inputs does not exceed AV_{DD} + 30 mV or go more negative than AGND – 30 mV.

[15]The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

Parameter	A, S Versions[1]	Units	Conditions/Comments
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage[16]	+5 to +10	V nom	±5% for Specified Performance
DV_{DD} Voltage[17]	+5	V nom	±5% for Specified Performance
Power Supply Currents			
AV_{DD} Current	0.6	mA max	AV_{DD} = +5 V
AV_{DD} Current	0.7	mA max	AV_{DD} = +10 V
DV_{DD} Current	0.5	mA max	$f_{CLK\ IN}$ = 1 MHz. Digital Inputs 0 V or DV_{DD}
DV_{DD} Current	1	mA max	$f_{CLK\ IN}$ = 2 MHz. Digital Inputs 0 V or DV_{DD}
Power Supply Rejection[18]			Rejection w.r.t. AGND
(AV_{DD})	See Note 19	dB typ	
Power Dissipation			
Normal Mode	5.5	mW max	AV_{DD} = DV_{DD} = +5 V, $f_{CLK\ IN}$ = 1 MHz; Typically 3.5 mW
Standby (Power-Down) Mode	500	μW max	AV_{DD} = DV_{DD} = +5 V; Typically 300 μW

NOTES
[16]Operation with AV_{DD} voltages in the range 5.25 V to 10.5 V is only guaranteed over the 0°C to +70°C temperature range.
[17]The ±5% tolerance on the DV_{DD} input is allowed provided that DV_{DD} does not exceed AV_{DD} by more than 0.3 V.
[18]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 2, 5, 10, 25 or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 2, 6, 10, 30 or 60 Hz.
[19]PSRR depends on gain: Gain of 1 = 70 dB typ; Gain of 2 = 75 dB typ; Gain of 4 = 80 dB typ; Gains of 8 to 128 = 85 dB typ.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND . . . . . −0.3 V to +12 V
AV_{DD} to DGND . . . . . −0.3 V to +12 V
DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to DGND . . . . . −0.3 V to +6 V
AGND to DGND . . . . . −0.3 V to +6 V
AIN1, AIN2 Input Voltage
to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
AIN3 Input Voltage to AGND . . . . . −0.3 V to +22 V
Reference Input Voltage to AGND . . −0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND . . . −0.3 V to AV_{DD} + 0.3 V
Digital Output Voltage to DGND . . . −0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Commercial (A Version) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +150°C
Plastic DIP Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 105°C/W
Lead Temperature, Soldering (10 sec) . . . . . +260°C
Cerdip Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 70°C/W
Lead Temperature, Soldering . . . . . +300°C
SOIC Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V, which readily accumulate on the human body and on test equipment, can discharge without detection. Although devices feature proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper precautions are recommended to avoid any performance degradation or loss of functionality.

AD7713 ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD7713AN	−40°C to +85°C	N-24
AD7713AR	−40°C to +85°C	R-24
AD7713AQ	−40°C to +85°C	Q-24
AD7713SQ	−55°C to +125°C	Q-24

NOTES
[1]To order MIL-STD-883B, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet and availability.
[2]N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

AD7711—SPECIFICATIONS

REF IN(+) = +2.5 V; REF IN(−) = AGND; MCLK IN = 10 MHz unless otherwise stated. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. For Filter Notches ≤ 60 Hz
	22	Bits min	For Filter Notch = 100 Hz
	18	Bits min	For Filter Notch = 250 Hz
	15	Bits min	For Filter Notch = 500 Hz
	12	Bits min	For Filter Notch = 1 kHz
Output Noise	See Tables I & II		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity			
@ 25°C	±0.0045	% of FSR max	Filter Notches ≤ 60 Hz. Typically ±0.0015%
T_{MIN} to T_{MAX}	±0.0075	% of FSR max	Filter Notches ≤ 60 Hz
Positive Full-Scale Error[2, 3]	See Note 4		Excluding Reference
Full-Scale Drift[5]	3/GAIN	µV/°C typ	Excluding Reference. For Gains of 1, 2, 4, 8
	0.35	µV/°C typ	Excluding Reference. For Gains of 16, 32, 64, 128
Unipolar Offset Error[2]	See Note 4		
Unipolar Offset Drift[5]	2.5/GAIN	µV/°C typ	For Gains of 1, 2, 4, 8
	0.3	µV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Zero Error[2]	See Note 4		
Bipolar Zero Drift[5]	2.5/GAIN	µV/°C typ	For Gains of 1, 2, 4, 8
	0.3	µV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Negative Full-Scale Error[2]	±0.006	% of FSR max	Excluding Reference. Typically ±0.0015%
Bipolar Negative Full-Scale Drift[5]	4/GAIN	µV/°C typ	Excluding Reference. For Gains of 1, 2, 4, 8
	0.5	µV/°C typ	Excluding Reference. For Gains of 16, 32, 64, 128
ANALOG INPUTS/REFERENCE INPUTS			
Normal Mode 50 Hz Rejection[6]	100	dB min	For Filter Notches of 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Normal Mode 60 Hz Rejection[6]	100	dB min	For Filter Notches of 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
DC Input Leakage Current[6] @ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[6]	20	pF max	
AIN1/REF IN			
Common-Mode Rejection (CMR)	92	dB min	At DC
Common-Mode 50 Hz Rejection[6]	150	dB min	For Filter Notches of 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Common-Mode 60 Hz Rejection[6]	150	dB min	For Filter Notches of 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode Voltage Range[7]	V_{SS} to AV_{DD}	V min to V max	
Analog Inputs[8]			
Input Voltage Range[9]			For Normal Operation. Depends on Gain Selected.
	0 to $+V_{REF}$[10]	max	Unipolar Input Range (B/U Bit of Control Register = 1)
	$\pm V_{REF}$	max	Bipolar Input Range (B/U Bit of Control Register = 0)
Input Sampling Rate, f_S	See Table III		
AIN2 Offset Error	4	mV max	Removed by System Calibrations but not by Self-Calibration
AIN2 Offset Drift	2	µV/°C	Removed by System Calibration but not by Self-Calibration
Reference Inputs			
REF IN(+) − REF IN(−) Voltage[11]	+2.5 to +5	V min to V max	For Specified Performance; Part Is Functional with Lower V_{REF} Voltages
Input Sampling Rate, f_S	$f_{CLK\ IN}/512$		
REFERENCE OUTPUT			
Output Voltage	2.5	V nom	
Initial Tolerance	±4	% max	
Drift	25	ppm/°C typ	
Output Noise	50	µV typ	pk–pk Noise. 0.1 Hz to 10 Hz Bandwidth
Line Regulation (AV_{DD})	1	mV/V max	
Load Regulation	1.5	mV/mA max	Maximum Load Current 1 mA
External Current	1	mA max	

NOTES

[1]Temperature ranges are as follows: A Version, −40°C to +85°C; S Version, −55°C to +125°C. See also Note 16.

[2]Applies after calibration at the temperature of interest.

[3]Positive full-scale error applies to both unipolar and bipolar input ranges.

[4]These errors will be of the order of the output noise of the part as shown in Table I.

[5]Recalibration at any temperature or use of the background calibration mode will remove these drift errors.

[6]These numbers are guaranteed by design and/or characterization.

[7]This common-mode voltage range is allowed, provided that the input voltage on AIN(+) or AIN(−) does not exceed AV_{DD} + 30 mV and V_{SS} − 30 mV.

[8]The analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance depends on the selected gain (see Tables IV and V).

[9]The analog input voltage range on the AIN1(+) input is given here with respect to the voltage on the AIN1(−) input. The input voltage range on the AIN2 input is with respect to AGND. The absolute voltage on the analog inputs should not go more positive than AV_{DD} + 30 mV or go more negative than V_{SS} − 30 mV.

[10]V_{REF} = REF IN(+) − REF IN(−).

[11]The reference voltage range may be restricted by the input voltage range requirement on the V_{BIAS} input.

Parameter	A, S Versions[1]	Units	Conditions/Comments
V_{BIAS} INPUT[12]			
Input Voltage Range	$AV_{DD} - 0.85 \times V_{REF}$		See V_{BIAS} Input Section
	or $AV_{DD} - 3$	V max	Whichever Is Smaller; +5 V/−5 V or +10 V/0 V Nominal AV_{DD}/V_{SS}
	or $AV_{DD} - 2.1$	V max	Whichever Is Smaller; +5 V/0 V Nominal AV_{DD}/V_{SS}
	$V_{SS} + 0.85 \times V_{REF}$		See V_{BIAS} Input Section
	or $V_{SS} + 3$	V min	Whichever Is Greater; +5 V/−5 V or +10 V/0 V Nominal AV_{DD}/V_{SS}
	or $V_{SS} + 2.1$	V min	Whichever Is Greater; +5 V/0 V Nominal AV_{DD}/V_{SS}
V_{BIAS} Rejection	65 to 85	dB typ	Increasing with Gain
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[13]	9	pF typ	
TRANSDUCER BURN-OUT			
Current	100	nA nom	
Initial Tolerance	±10	% typ	
Drift	0.1	%/°C typ	
RTD EXCITATION CURRENTS (RTD1, RTD2)			
Output Current	200	μA nom	
Initial Tolerance	±20	% max	
Drift	20	ppm/°C typ	
Initial Matching	±1	% max	Matching Between RTD1 and RTD2 Currents
Drift Matching	3	ppm/°C typ	Matching Between RTD1 and RTD2 Current Drift
Line Regulation (AV_{DD})	200	nA/V max	AV_{DD} = +5 V
Load Regulation	200	nA/V max	
Output Compliance	$AV_{DD} - 2$	V max	
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[14]	$(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[14]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[15]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[15]	$0.8 \times V_{REF}/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(2.1 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)

NOTES

[12]The AD7711 is tested with the following V_{BIAS} voltages. With AV_{DD} = +5 V and V_{SS} = 0 V, V_{BIAS} = +2.5 V; with AV_{DD} = +10 V and V_{SS} = 0 V, V_{BIAS} = +5 V and with AV_{DD} = +5 V and V_{SS} = −5 V, V_{BIAS} = 0 V.

[13]Sample tested at +25°C to ensure compliance.

[14]After calibration, if the analog input exceeds positive full scale, then the converter will output all 1s. If the analog input is less than negative full scale, then the device will output all 0s.

[15]These calibration and span limits apply provided that the absolute voltage on the analog inputs does not exceed AV_{DD} + 30 mV or does not go more negative than V_{SS} − 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

AD7711—SPECIFICATIONS

Parameter	A, S Versions[1]	Units	Conditions/Comments
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage[16]	+5 to +10	V nom	±5% for Specified Performance
DV_{DD} Voltage[17]	+5	V nom	±5% for Specified Performance
$AV_{DD} - V_{SS}$ Voltage	+10.5	V max	For Specified Performance
Power Supply Currents			
AV_{DD} Current	4	mA max	
DV_{DD} Current	4.5	mA max	
V_{SS} Current	1.5	mA max	V_{SS} = −5 V
Power Supply Rejection[18]			Rejection w.r.t. AGND; Assumes V_{BIAS} Is Fixed
Positive Supply (AV_{DD})	See Note 19	dB typ	
Negative Supply (V_{SS})	90	dB typ	
Power Dissipation			
Normal Mode	45	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V; Typically 25 mW
Normal Mode	52.5	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = −5 V; Typically 30 mW
Standby (Power-Down) Mode	15	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V or −5 V; Typically 7 mW

[16]The AD7711 is specified with a 10 MHz clock for AV_{DD} voltages of +5 V ± 5%. It is specified with an 8 MHz clock for AV_{DD} voltages greater than 5.25 V and less than 10.5 V. Operating with AV_{DD} voltages in the range 5.25 V to 10.5 V is only guaranteed over the 0°C to +70°C temperature range.
[17]The ±5% tolerance on the DV_{DD} input is allowed provided that DV_{DD} does not exceed AV_{DD} by more than 0.3 V.
[18]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 10 Hz, 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 10 Hz, 30 Hz or 60 Hz.
[19]PSRR depends on gain: Gain of 1 = 70 dB typ; Gain of 2 = 75 dB typ; Gain of 4 = 80 dB typ; Gains of 8 to 128 = 85 dB typ. These numbers can be improved (to 95 dB typ) by deriving the V_{BIAS} voltage (via Zener diode or reference) from the AV_{DD} supply.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AV_{DD} to DV_{DD} . . . . . −0.3 V to +12 V
AV_{DD} to V_{SS} . . . . . −0.3 V to +12 V
AV_{DD} to AGND . . . . . −0.3 V to +12 V
AV_{DD} to DGND . . . . . −0.3 V to +12 V
DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to DGND . . . . . −0.3 V to +6 V
V_{SS} to AGND . . . . . +0.3 V to −6 V
V_{SS} to DGND . . . . . +0.3 V to −6 V
Analog Input Voltage to AGND
. . . . . V_{SS} − 0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND
. . . . . V_{SS} − 0.3 V to AV_{DD} + 0.3 V
REF OUT to AGND . . . . . −0.3 V to AV_{DD}
Digital Input Voltage to DGND . . . −0.3 V to AV_{DD} + 0.3 V
Digital Output Voltage to DGND . . . −0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Commercial (A Version) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +150°C
Plastic DIP Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 105°C/W
Lead Temperature, Soldering (10 sec) . . . . . +260°C
Cerdip Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 70°C/W
Lead Temperature, Soldering . . . . . +300°C
SOIC Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7711 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD7711 ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7711AN	−40°C to +85°C	N-24
AD7711AR	−40°C to +85°C	R-24
AD7711AQ	−40°C to +85°C	Q-24
AD7711SQ	−55°C to +125°C	Q-24

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

TIMING CHARACTERISTICS[1, 2]

(DV_{DD} = +5 V ± 5%; AV_{DD} = +5 V or +10 V[3] ± 5%; AGND = DGND = 0 V; $f_{CLK\ IN}$ = 10 MHz (AD7711) or 2 MHz (AD7713); Input Logic 0 = 0 V, Logic 1 = DV_{DD} unless otherwise stated.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
$f_{CLK\ IN}$[4, 5]	400	kHz min	Master Clock Frequency
	2	MHz max	AD7713
	10	MHz max	AD7711
$t_{CLK\ IN\ LO}$	0.4 × $t_{CLK\ IN}$	ns min	Master Clock Input Low Time; $t_{CLK\ IN}$ = 1/$f_{CLK\ IN}$
$t_{CLK\ IN\ HI}$	0.4 × $t_{CLK\ IN}$	ns min	Master Clock Input High Time
t_r[6]	50	ns max	Digital Output Rise Time; Typically 20 ns
t_f[6]	50	ns max	Digital Output Fall Time; Typically 20 ns
t_1	1000	ns min	$\overline{SYNC}$ Pulse Width
Self-Clocking Mode			
t_2	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time
t_3	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_4	2 × $t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_5	50	ns min	A0 to $\overline{RFS}$ Hold Time
t_6	4 × $t_{CLK\ IN}$	ns max	$\overline{RFS}$ Low to SCLK Falling Edge
t_7[7]	4 × $t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_8[7]	$t_{CLK\ IN}$/2	ns min	SCLK Falling Edge to Data Valid Delay
	$t_{CLK\ IN}$/2 + 30	ns max	
t_9	$t_{CLK\ IN}$/2	ns nom	SCLK High Pulse Width
t_{10}	3 × $t_{CLK\ IN}$/2	ns nom	SCLK Low Pulse Width
t_{11}	10	ns min	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
	$t_{CLK\ IN}$/2	ns max	
t_{12}	3 × $t_{CLK\ IN}$/2 + 20	ns max	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Delay
t_{13}[8]	3 × $t_{CLK\ IN}$/2 + 20	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{14}	0	ns min	A0 to $\overline{TFS}$ Setup Time
t_{15}	0	ns min	A0 to $\overline{TFS}$ Hold Time
t_{16}	4 × $t_{CLK\ IN}$	ns max	$\overline{TFS}$ to SCLK Falling Edge Delay Time
t_{17}	4 × $t_{CLK\ IN}$	ns min	$\overline{TFS}$ to SCLK Falling Edge Hold Time
t_{18}	0	ns min	Data Valid to SCLK Setup Time
t_{19}	10	ns min	Data Valid to SCLK Hold Time

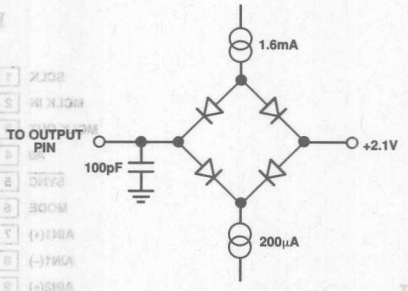


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
External-Clocking Mode			
f_{SCLK}	$f_{CLK\ IN}/5$	MHz max	Serial Clock Input Frequency
t_{20}	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time
t_{21}	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_{22}	$2 \times t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_{23}	50	ns min	A0 to $\overline{RFS}$ Hold Time
t_{24}[7]	$4 \times t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_{25}[7]	$t_{CLK\ IN}/2$	ns min	SCLK Falling Edge to Data Valid Delay
	$2 \times t_{CLK\ IN} + 20$	ns max	
t_{26}	$2 \times t_{CLK\ IN}$	ns min	SCLK High Pulse Width
t_{27}	$2 \times t_{CLK\ IN}$	ns min	SCLK Low Pulse Width
t_{28}	$t_{CLK\ IN} + 10$	ns max	SCLK Falling Edge to $\overline{DRDY}$ High
t_{29}[8]	0	ns min	$\overline{DRDY}$ to Data Valid Hold Time
	20	ns max	
t_{30}	10	ns min	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
t_{31}[8]	$5 \times t_{CLK\ IN}/2 + 20$	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{32}	0	ns min	A0 to $\overline{TFS}$ Setup Time
t_{33}	0	ns min	A0 to $\overline{TFS}$ Hold Time
t_{34}	$4 \times t_{CLK\ IN}$	ns min	SCLK Falling Edge to $\overline{TFS}$ Hold Time
t_{35}	$5 \times t_{CLK\ IN}/2$ − SCLK High	ns min	Data Valid to SCLK Setup Time
t_{36}	30	ns min	Data Valid to SCLK Hold Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 6 to 9 of AD7710/AD7712 data sheet.

[3]Operation with AV_{DD} voltages in the range 5.25 V to 10.5 V is only guaranteed over the 0°C to +70°C temperature range.

[4]CLK IN duty cycle range is 45% to 55%. CLK IN must be supplied whenever the AD7711/AD7713 is not in STANDBY mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[5]The AD7711 is production tested at 10 MHz. The AD7713 is production tested with $f_{CLK\ IN}$ at 2 MHz. Both are guaranteed by characterization to operate at 400 kHz.

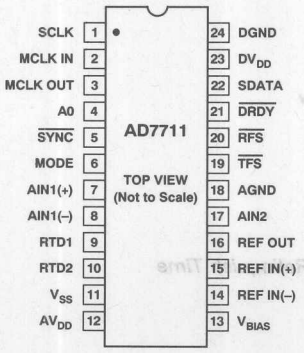
[6]Specified using 10% and 90% points on waveform of interest.

[7]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

[8]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 100 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

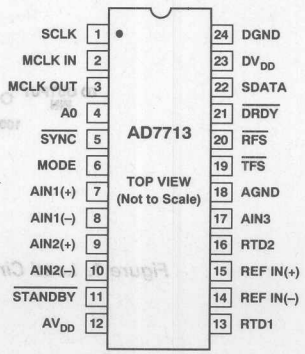
AD7711 PIN CONFIGURATION

DIP and SOIC



AD7713 PIN CONFIGURATION

DIP and SOIC



PIN FUNCTION DESCRIPTION

Mnemonic	Function
SCLK	Serial Clock. Logic input/output depending on the status of the MODE pin. When MODE is high, the device is in its self-clocking mode and the SCLK pin provides a serial clock output. This SCLK becomes active when $\overline{RFS}$ or $\overline{TFS}$ goes low and it goes high impedance when either $\overline{RFS}$ or $\overline{TFS}$ returns high or when the device has completed transmission of an output word. When MODE is low, the device is in its external clocking mode and the SCLK pin acts as an input. This input serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7711/AD7713 in smaller batches of data.
MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal or external clock. A crystal can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The clock input frequency is nominally 2 MHz for AD7713 and 10 MHz for AD7711.
MCLK OUT	When the master clock for the device is a crystal, the crystal is connected between MCLK IN and MCLK OUT.
A0	Address Input. With this input low, reading and writing to the device is to the control register. With this input high, access is to either the data register or the calibration registers.
$\overline{SYNC}$	Logic Input which allows for synchronization of the digital filters when using a number of AD7711/AD7713s. It resets the nodes of the digital filter.
MODE	Logic Input. When this pin is high, the device is in its self-clocking mode; with this pin low, the device is in its external clocking mode.
AIN1(+)	Analog Input Channel 1. Positive input of the programmable-gain differential analog input. The AIN1(+) input is connected to an output current source which can be used to check that an external transducer has burnt out or has gone open circuit. This output current source can be turned on/off via the control register.
AIN1(−)	Analog Input Channel 1. Negative input of the programmable gain differential analog input.
AIN2	AD7711 Only. Analog Input Channel 2. Single-ended programmable gain analog input.
REF OUT	AD7711 Only. Reference Output. The internal +2.5 V reference is provided at this pin. This is a single-ended output which is reference to AGND. It is a buffered output capable of providing 1 mA to an external load.
V_{BIAS}	AD7711 Only. Input Bias Voltage. This input voltage should be set such that $V_{BIAS} + 0.85 \times V_{REF} < AV_{DD}$ and $V_{BIAS} - 0.85 \times V_{REF} > V_{SS}$ where V_{REF} is REF IN(+) − REF IN(−). See V_{BIAS} input section.
V_{SS}	AD7711 Only. Analog Negative Supply, 0 V to −5 V. Tied to AGND for single supply operation. The input voltage on AIN1 or AIN2 should not go >30 mV negative w.r.t. V_{SS} for correct operation of the device.
AIN2(+)	AD7713 Only. Analog Input Channel 2. Positive input of the programmable gain differential analog input.
AIN2(−)	AD7713 Only. Analog Input Channel 2. Negative input of the programmable gain differential analog input.
$\overline{STANDBY}$	AD7713 Only. Logic Input. Taking this pin low shuts down the internal analog and digital circuitry, reducing power consumption to less than 50 μW.
AV_{DD}	Analog Positive Supply Voltage, +5 V to +10 V.
RTD1	Constant Current Output. A nominal 200 μA constant current is provided at this pin and this can be used as the excitation current for RTDs. This, current can be turned on or off via the control register.
RTD2	Constant Current Output. A nominal 200 μA constant current is provided at this pin and this can be used as the excitation current for RTDs. This current can be turned on or off via the control register. This second current can be used to eliminate lead resistance errors in three-wire RTD configurations.
REF IN(−)	Reference Input. The REF IN(−) can lie anywhere between AV_{DD} and AGND provided REF IN(+) is greater than REF IN(−).
REF IN(+)	Reference Input. The reference input is differential with the provision that REF IN(+) must be greater than REF IN(−). REF IN(+) can lie anywhere between AV_{DD} and AGND.
AIN3	AD7713 only. Analog Input Channel 3. High level analog input which accepts an analog input voltage range of $4 \times V_{REF}$/GAIN. At the nominal V_{REF} of +2.5 V and a gain of 1, the AIN3 input voltage range is 0 to +10 V.
AGND	Ground Reference Point for Analog Circuitry.
$\overline{TFS}$	Transmit Frame Synchronization. Active low logic input used to write serial data to the device with serial data expected after the falling edge of this pulse. In the self-clocking mode, the serial clock becomes active after $\overline{TFS}$ goes low. In the external clocking mode, $\overline{TFS}$ must go low before the first bit of the data word is written to the part.
$\overline{RFS}$	Receive Frame Synchronization. Active low logic input used to access serial data from the device. In the self-clocking mode, the SCLK and SDATA lines both become active after $\overline{RFS}$ goes low. In the external clocking mode, the SDATA line becomes active after $\overline{RFS}$ goes low.

Mnemonic	Function
$\overline{DRDY}$	Logic Output. A falling edge indicates a new output word is available for transmission. The $\overline{DRDY}$ pin will return high upon completion of transmission of a full output word. $\overline{DRDY}$ is also used to indicate when the AD7711/AD7713 has completed its on-chip calibration sequence.
SDATA	Serial Data. Input/Output with serial data being written to either the control register or the calibration registers and serial data being accessed from the control register, calibration registers or the data register. During an output data read operation, serial data becomes active after $\overline{RFS}$ goes low (provided $\overline{DRDY}$ is low). During a write operation, valid serial data is expected on the rising edges of SCLK when $\overline{TFS}$ is low. The output data is natural binary for unipolar inputs and offset binary for bipolar inputs.
DV_{DD}	Digital Supply Voltage, +5 V. DV_{DD} should never exceed AV_{DD} by more than 0.3 V. If DV_{DD} powers up before AV_{DD} or if DV_{DD} can exceed AV_{DD} by more than 0.3 V at any other time, the protection scheme outlined in Figure 5 should be used.
DGND	Ground Reference Point for Digital Circuitry.

TERMINOLOGY

INTEGRAL NONLINEARITY

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

POSITIVE FULL-SCALE ERROR

Positive full-scale error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal input full-scale voltage. For AIN(+), the ideal full-scale input voltage is (AIN(−) + V_{REF}/GAIN − 3/2 LSBs); for AIN2 of AD7711, the ideal full-scale input voltage is V_{REF}/GAIN − 3/2 LSBs; for AIN3 of AD7713, the ideal full-scale voltage is +4 × V_{REF}/GAIN − 3/2 LSBs. Positive full-scale error applies to both unipolar and bipolar analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar offset error is the deviation of the first code transition from the ideal input voltage. For AIN(+), the ideal input voltage is (AIN(−) + 0.5 LSB); for AIN2 of AD7711 and AIN3 of AD7713, the ideal input is 0.5 LSB when operating in the Unipolar Mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal input voltage. For AIN(+), the ideal input voltage is (AIN(−) − 0.5 LSB); for AIN2 of AD7711 the ideal input is −0.5 LSB; AIN3 of AD7713 can only accommodate unipolar input ranges.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal input voltage. For AIN(+), the ideal input voltage is (AIN(−) −V_{REF}/GAIN + 0.5 LSB); for AIN2 of AD7711 the ideal input is −V_{REF}/GAIN to 0.5 LSB when operating from dual supplies; AIN3 of AD7713 can only accommodate unipolar input ranges.

POSITIVE FULL-SCALE OVERRANGE

Positive full-scale overrange is the amount of overhead available to handle input voltages on the AIN(+) inputs greater than (AIN(−) + V_{REF}/GAIN) or on AIN2 of AD7711 of greater than V_{REF}/GAIN or AIN3 of AD7713 of greater than +4 × V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or to overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages on AIN(+) below (AIN(−) − V_{REF}/GAIN) or on AIN2 of AD7711 below −V_{REF}/GAIN without overloading the analog modulator or overflowing the digital filter.

OFFSET CALIBRATION RANGE

In the system calibration modes, the AD7711/AD7713 calibrates its offset with respect to the analog input. The offset calibration range specification defines the range of voltages that the AD7711/AD7713 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7711/AD7713 can accept in the system calibration mode and still calibrate full scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7711/AD7713's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7711/AD7713 can accept and still calibrate gain accurately.

Control Register (24 Bits)

A write to the device with the A0 input low writes data to the control register. A read to the device with the A0 input low accesses the contents of the control register. The control register is 24-bits wide and when writing to the register 24 bits of data must be written otherwise the data will not be loaded to the control register. In other words, it is not possible to write just the first 12 bits of data into the control register. If more than 24 clock pulses are provided before $\overline{TFS}$ returns high, then all clock pulses after the 24th clock pulse are ignored. Similarly, a read operation from the control register should access 24 bits of data.

MSB

MD2	MD1	MD0	G2	G1	G0	S1[1]	S2[2]	WL	RO	BO	B/U
FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

LSB

NOTES
[1]On the AD7711 this bit is CH, and on the AD7713 this bit is CH1.
[2]On the AD7711 this bit is PD, and on the AD7713 this bit is CH0.

Operating Mode

MD2	MD1	MD0	Operating Mode
0	0	0	Normal Mode. This is the normal mode of operation of the device whereby a read to the device with A0 high accesses data from the data register. This is the default condition of these bits after the internal power-on reset.
0	0	1	Activate Self-Calibration. This activates self-calibration on the channel selected by CH (CH0 and CH1 on AD7713). This is a one-step calibration sequence, and when complete, the part returns to Normal Mode (with MD2, MD1, MD0 of the control register returning to 0, 0, 0). The $\overline{DRDY}$ line indicated when this self-calibration is complete and valid data is available in the output register. For this calibration type, the zero-scale calibration is done internally on shorted (zeroed) inputs and the full-scale calibration is done internally on V_{REF}.
0	1	0	Activate System Calibration. This activates system calibration on the channel selected by CH (CH0 and CH1 on AD7713). This is a two-step calibration sequence, with the zero-scale calibration done first on the selected input channel and $\overline{DRDY}$ indicating when this zero-scale calibration is complete. The part returns to Normal Mode at the end of this first step in the two-step sequence.
0	1	1	Activate System Calibration. This is the second step of the system calibration sequence with full-scale calibration being performed on the selected input channel. Once again, $\overline{DRDY}$ indicated when this full-scale calibration is complete. When this calibration is complete, the part returns to Normal Mode.
1	0	0	Activate System-Offset Calibration. This activates system-offset calibration on the channel selected by CH (CH0 and CH1 on AD7713). This is a one step calibration sequence and when complete the part returns to Normal Mode with $\overline{DRDY}$ indicating when this system offset calibration is complete. For this calibration type, the zero-scale calibration is done on the selected input channel and the full-scale calibration is done internally on V_{REF}.
1	0	1	Activate Background Calibration. This activates background calibration on the channel selected by CH (CH0 and CH1 on AD7713). If the background calibration mode is on, then the AD7711/AD7713 provides continuous self-calibration of the reference and shorted (zeroed) inputs. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the device when there is a change in the ambient temperature. In this mode, shorted (zeroed) inputs and V_{REF}, as well as the analog input voltage, are continuously monitored and the calibration registers of the device are updated.
1	1	0	Read/Write Zero-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the zero-scale calibration coefficients of the channel selected by CH (CH0 and CH1 on AD7713). A write to the device with A0 high writes data to the zero-scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Therefore, when writing to the calibration register, 24 bits of data must be written, otherwise the new data will not be transferred to the calibration register.
1	1	1	Read/Write Full-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the full-scale calibration coefficients of the channel selected by CH (CH0 and CH1 on AD7713). A write to the device with A0 high writes data to the full-scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Therefore, when writing to the calibration register, 24 bits of data must be written, otherwise, the new data will not be transferred to the calibration register.

0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Channel Selection

CH1 (AD7713 Only)	CH0	Channel	
0	0	AIN1	(Default Condition After the Internal Power-On Reset)
0	1	AIN2	
1	0	AIN3	AD7713 Only

Power-Down (AD7711 Only)

PD

0 Normal Operation (Default Condition After Internal Power-On Reset)
1 Power-Down

Word Length

WL Output Word Length

0 16-Bit (Default Condition After Internal Power-On Reset)
1 24-Bit

RTD Excitation Currents

RO

0 Off (Default Condition After Internal Power-On Reset)
1 On

Burn-Out Current

BO

0 Off (Default Condition After Internal Power-On Reset)
1 On

Bipolar/Unipolar Selection (Both Inputs)

B/U

0 Bipolar (Default Condition After Internal Power-On Reset)
1 Unipolar

Filter Selection (FS11–FS0)

The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$) filter response. The 12 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device.

The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency = $(f_{CLK\ IN}/512)/code$ where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 2,000. The value of the code loaded to these bits **must** be within this range. Failure to do this will result in unspecified operation of the device.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I and II show the effect of the filter notch frequency and gain on the effective resolution of the part. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is at 10 Hz then a new word is available at a 10 Hz rate or every 100 ms. If the first notch is at 200 Hz, a new word is available every 5 ms.

The settling time of the filter to a full-scale step input change is worst case 4 × 1/(the output data rate). This settling time is to 100% of the final value. For example, with the first filter notch at 10 Hz, the settling time of the filter to a full-scale step input change is 400 ms max. This settling time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with $\overline{SYNC}$ low, the settling time will be 3 × 1/(output data rate). If a change of channel takes place, the settling time is 3 × 1/(output data rate) regardless of the $\overline{SYNC}$ input, but $\overline{DRDY}$ does not stay high for 3 × 1/output rate. The −3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter −3 dB frequency = 0.262 × first notch frequency.

Tables I and II show the output rms noise for some typical notch and −3 dB frequencies for the AD7711. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V. These numbers are typical and are generated with an analog input voltage of 0 V. The output noise from the part comes from two sources. The first is the electrical noise in the semiconductor devices used in the implementation of the modulator (device noise). The second occurs when the analog input signal is converted into the digital domain adding quantization noise. The device noise is at a low level and is largely independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. Consequently, lower filter notch settings (below 60 Hz approximately) tend to be device noise dominated while higher notch settings are dominated by quantization noise. Changing the filter notch and cutoff frequency in the quantization noise dominated region results in a more dramatic improvement in noise performance than it does in the device noise dominated region as shown in Table I. Furthermore, quantization noise is added after the PGA, so effective resolution is independent of gain for the higher filter notch frequencies. Meanwhile, device noise is added in the PGA and, therefore, effective resolution suffers a little at high gains for lower notch frequencies.

At the lower filter notch settings (below 60 Hz), the no missing codes performance of the device is at the 24-bit level. At the higher settings, more codes will be missed until at 1 kHz notch setting, no missing codes performance is only guaranteed to the 12-bit level. However, since the effective resolution of the part is 10.5 bits for this filter notch setting, this no missing codes performance should be more than adequate for all applications.

The effective resolution of the device is defined as the ratio of the output rms noise to the input full scale. This does not remain constant with increasing gain or with increasing bandwidth. Table II shows the same table as Table I except that the output is now expressed in terms of effective resolution (the magnitude of the rms noise with respect to 2 × V_{REF}/GAIN, i.e., the input full scale). It is possible to do post filtering on the device to improve the output data rate for a given −3 dB frequency and also to further reduce the output noise (see Digital Filtering section).

Table I. Output Noise vs. Gain and First Notch Frequency for AD7711

First Notch of Filter and O/P Data Rate[1]	−3 dB Frequency	Typical Output RMS Noise (μV) Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz[2]	2.62 Hz	1.7	1.0	0.5	0.36	0.36	0.36	0.36	0.36
25 Hz[2]	6.55 Hz	4.9	2.2	1.2	0.6	0.36	0.36	0.36	0.36
30 Hz[2]	7.86 Hz	6.1	2.4	1.2	0.84	0.5	0.36	0.36	0.36
50 Hz[2]	13.1 Hz	7.5	3.8	2.0	1.0	0.6	0.5	0.5	0.45
60 Hz[2]	15.72 Hz	8.5	4.0	2.0	1.0	0.6	0.5	0.5	0.45
100 Hz[3]	26.2 Hz	13	6.4	3.7	1.8	1.1	0.9	0.65	0.65
250 Hz[3]	65.5 Hz	130	75	25	12	7.5	4	2.7	1.7
500 Hz[3]	131 Hz	0.6 × 10^3	0.26 × 10^3	140	70	35	25	15	8
1 kHz[3]	262 Hz	3.1 × 10^3	1.6 × 10^3	0.7 × 10^3	0.29 × 10^3	180	120	70	40

NOTES
[1]The default condition (after the internal power-on reset) for the first notch of filter is 60 Hz.
[2]For these filter notch frequencies, the output rms noise is primarily dominated by device noise and as a result is independent of the value of the reference voltage. Therefore, increasing the reference voltage will give an increase in the effective resolution of the device (i.e., the ratio of the rms noise to the input full scale is increased since the output rms noise remains constant as the input full scale increases).
[3]For these filter notch frequencies, the output rms noise is dominated by quantization noise and as a result is proportional to the value of the reference voltage.

Table II. Effective Resolution vs. Gain and First Notch Frequency for AD7711

First Notch of Filter and O/P Data Rate	−3 dB Frequency	Effective Resolution[1] (Bits) Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz	2.62 Hz	21.5	21.5	21.5	20.5	19.5	18.5	17.5	16.5
25 Hz	6.55 Hz	20	20	20	20	19.5	18.5	17.5	16.5
30 Hz	7.86 Hz	19.5	20	20	19.5	19.5	18.5	17.5	16.5
50 Hz	13.1 Hz	19.5	19.5	19.5	19.5	19	18.5	17.5	16.5
60 Hz	15.72 Hz	19	19.5	19.5	19.5	19	18.5	17.5	16.5
100 Hz	26.2 Hz	18.5	18.5	18.5	18.5	18	17.5	17	16
250 Hz	65.5 Hz	15	15	15.5	15.5	15.5	15.5	15	14.5
500 Hz	131 Hz	13	13	13	13	13	12.5	12.5	12.5
1 kHz	262 Hz	10.5	10.5	11	11	11	10.5	10	10

NOTE
[1]Effective resolution is defined as the magnitude of the output rms noise with respect to the input full scale (i.e., 2 × V_{REF}/GAIN). The above table applies for a V_{REF} of +2.5 V and resolution numbers are rounded to the nearest 0.5 LSB.

Tables Ia and IIa show the output rms noise for some typical notch and −3 dB frequencies for the AD7713. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V. These numbers are typical and are generated with an analog input voltage of 0 V. The output noise from the part comes from two sources. Firstly, there is the electrical noise in the semiconductor devices used in the implementation of the modulator (device noise). Secondly, when the analog input signal is converted into the digital domain, quantization noise is added. The device noise is at a low level and is largely independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. Consequently, lower filter notch settings (below 12 Hz approximately) tend to be device noise dominated while higher notch settings are dominated by quantization noise. Changing the filter notch and cutoff frequency in the quantization-noise dominated region results in a more dramatic improvement in noise performance than it does in the device-noise dominated region as shown in Table Ia. Furthermore, quantization noise is added after the PGA, so effective resolution is independent of gain for the higher filter notch frequencies. Meanwhile, device noise is added in the PGA and, therefore, effective resolution suffers a little at high gains for lower notch frequencies.

At the lower filter notch settings (below 12 Hz), the no missing codes performance of the device is at the 24-bit level. At the higher settings, more codes will be missed until at 200 Hz notch setting, no missing codes performance is only guaranteed to the 12-bit level. However, since the effective resolution of the part is 10.5 bits for this filter notch setting, this no missing codes performance should be more than adequate for all applications.

The effective resolution of the device is defined as the ratio of the output rms noise to the input full scale. This does not remain constant with increasing gain or with increasing bandwidth. Table IIa shows the same table as Table Ia except that the output is now expressed in terms of effective resolution (the magnitude of the rms noise with respect to $2 \times V_{REF}$/GAIN, i.e., the input full scale). It is possible to do post filtering on the device to improve the output data rate for a given −3 dB frequency and also to further reduce the output noise (see Digital Filtering section).

Table Ia. Output Noise vs. Gain and First Notch Frequency for AD7713

First Notch of Filter and O/P Data Rate[1]	−3 dB Frequency	Typical Output RMS Noise (μV)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
2 Hz[2]	0.52 Hz	1.7	1.0	0.5	0.36	0.36	0.36	0.36	0.36
5 Hz[2]	1.31 Hz	4.9	2.2	1.2	0.6	0.36	0.36	0.36	0.36
6 Hz[2]	1.57 Hz	6.1	2.4	1.2	0.84	0.5	0.36	0.36	0.36
10 Hz[2]	2.62 Hz	7.5	3.8	2.0	1.0	0.6	0.5	0.5	0.45
12 Hz[2]	3.14 Hz	8.5	4.0	2.0	1.0	0.6	0.5	0.5	0.45
20 Hz[3]	5.24 Hz	13	6.4	3.7	1.8	1.1	0.9	0.65	0.65
50 Hz[3]	13.1 Hz	130	75	25	12	7.5	4	2.7	1.7
100 Hz[3]	26.2 Hz	0.6×10^3	0.26×10^3	140	70	35	25	15	8
200 Hz[3]	52.4 Hz	3.1×10^3	1.6×10^3	0.7×10^3	0.29×10^3	180	120	70	40

NOTES
[1]The default condition (after the internal power-on reset) for the first notch of filter is 12 Hz.
[2]For these filter notch frequencies, the output rms noise is primarily dominated by device noise and a result is independently of the value of the reference voltage. Therefore, increasing the reference voltage will give an increase in the effective resolution of the device (i.e., the ratio of the rms noise to the input full scale is increased since the output rms noise remains constant as the input full-scale increases).
[3]For these filter notch frequencies, the output rms noise is dominated by quantization noise and as a result is proportional to the value of the reference voltage.

Table IIa. Effective Resolution vs. Gain and First Notch Frequency for AD7713

First Notch of Filter and O/P Data Rate	−3 dB Frequency	Effective Resolution[1] (Bits)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
2 Hz	0.52 Hz	21.5	21.5	21.5	20.5	19.5	18.5	17.5	16.5
5 Hz	1.31 Hz	20	20	20	20	19.5	18.5	17.5	16.5
6 Hz	1.57 Hz	19.5	20	20	19.5	19.5	18.5	17.5	16.5
10 Hz	2.62 Hz	19.5	19.5	19.5	19.5	19	18.5	17.5	16.5
12 Hz	3.14 Hz	19	19.5	19.5	19.5	19	18.5	17.5	16.5
20 Hz	5.24 Hz	18.5	18.5	18.5	18.5	18	17.5	17	16
50 Hz	13.1 Hz	15	15	15.5	15.5	15.5	15.5	15	14.5
100 Hz	26.2 Hz	13	13	13	13	13	12.5	12.5	12.5
200 Hz	52.4 Hz	10.5	10.5	11	11	11	10.5	10	10

NOTE
[1]Effective resolution is defined as the magnitude of the output rms noise with respect to the input full scale (i.e., $2 \times V_{REF}$/GAIN). The above table applies for a V_{REF} of +2.5 V and resolution numbers are rounded to the nearest 0.5 LSB.

CIRCUIT DESCRIPTION

The AD7711/AD7713 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in industrial control or process control applications. It contains a sigma-delta (or charge-balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bidirectional serial communications port.

The AD7711 contains two programmable gain input channels, one differential and one single-ended. The AD7713 contains three programmable gain analog input channels, two differential input and one high-level single-ended input. The gain range on all inputs is from 1 to 128. For the low-level inputs, this means that the input can accept unipolar signals of between 0 mV to +20 mV and 0 V to +2.5 V or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals +2.5 V. The input voltage range for the AIN3 of the AD7713 input is $+4 \times V_{REF}/GAIN$ and is 0 V to +10 V with the nominal reference of +2.5 V and a gain of 1. The input signal to the selected analog input channel is continuously sampled at a rate determined by the frequency of the master clock, CLK IN, and the selected gain (see Table III). A charge balancing A/D converter (Sigma-Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma-delta modulator with the input sampling frequency being modified to give the higher gains. A $sinc^3$ digital low-pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and hence its −3 dB frequency) can be programmed via an on-chip control register.

The AD7711/AD7713 provides a number of calibration options which can be programmed via the on-chip control register. A calibration cycle may be initiated at any time by writing to this control register. The part can perform self-calibration using the on-chip calibration microcontroller and SRAM to store calibration parameters. Other system components may also be included in the calibration loop to remove offset and gain errors in the input channel using the system calibration mode. Another option is a background calibration mode where the part continuously performs self-calibration and updates the calibration coefficients. Once the part is in this mode, the user does not have to worry about issuing periodic calibration commands to the device or asking the device to recalibrate when there is a change in the ambient temperature or power supply voltage.

The AD7711/AD7713 gives the user access to the on-chip calibration registers allowing the microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part from prestored values in E^2PROM. This gives the microprocessor much greater control over the part's calibration procedure. It also means that the user can verify that the device has performed its calibration correctly by comparing the coefficients after calibration with prestored values in E^2PROM.

The AD7713 is a positive supply only part while the AD7711 can be operated from positive and negative supplies. For battery operation or low power systems, both parts offer a standby mode that reduces idle power consumption to 300 μW typical on AD7713 and 7 mW typical on the AD7711.

The AD7711/AD7713 uses a second-order sigma-delta modulator and a digital filter that provides a rolling average of the sampled output. After power-up or if there is a step change in the input voltage, there is a settling time that must elapse before valid data is obtained.

Input Sample Rate

The modulator sample frequency for the device remains at $f_{CLK\ IN}/512$ (3.9 kHz @ $f_{CLK\ IN}$ = 2 MHz and 19.5 kHz @ f_{CLKIN} = 10 MHz) regardless of the selected gain. However, gains greater than ×1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of reference capacitor to input capacitor. As a result of the multiple sampling, the input sample rate of the device varies with the selected gain (see Table III). The effective input impedance is $1/C \cdot f_S$ where C is the input sampling capacitance and f_S is the input sample rate.

Table III. Input Sampling Frequency vs. Gain

Gain	Input Sampling Frequency (f_S)
1	$f_{CLK\ IN}/512$
2	$2 \times f_{CLK\ IN}/512$
4	$4 \times f_{CLK\ IN}/512$
8	$8 \times f_{CLK\ IN}/512$
16	$8 \times f_{CLK\ IN}/512$
32	$8 \times f_{CLK\ IN}/512$
64	$8 \times f_{CLK\ IN}/512$
128	$8 \times f_{CLK\ IN}/512$

DIGITAL FILTERING

The part's digital filter behaves like a similar analog filter, with a few minor differences.

First, since digital filtering occurs after the A-to-D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the part has over-range headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 5% above the analog input range. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the input channel voltage so that its full scale is half that of the analog input channel full scale. This will provide an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

Filter Characteristics

The cutoff frequency of the digital filter is determined by the value loaded to bits FS0 to FS11 in the control register. At a clock frequency of 2 MHz, the minimum cutoff frequency of the filter is 0.52 Hz while the maximum programmable cutoff frequency is 53.9 Hz. At a clock frequency of 10 MHz (AD7711 only), the minimum cutoff frequency of the filter is 2.58 Hz while the maximum programmable cutoff frequency is 269 Hz.

Figure 2 shows the filter frequency response for a cutoff frequency of 2.62 Hz which corresponds to a first filter notch frequency of 10 Hz. This is a $(\sin x/x)^3$ response (also called $sinc^3$) that provides >100 dB of 50 Hz and 60 Hz rejection. Programming a different cutoff frequency via FS0–FS11 does not alter

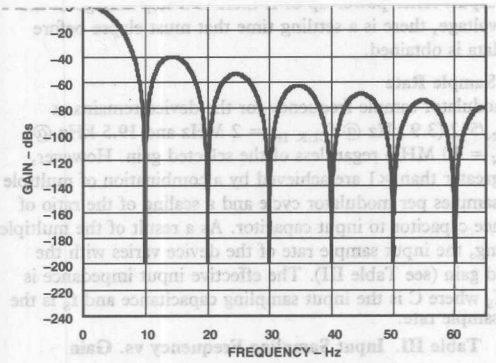


Figure 2. Frequency Response of AD7711/AD7713 Filter

Since the AD7711/AD7713 contains this on-chip, low-pass filtering, there is a settling time associated with step function inputs and data on the output will be invalid after a step change until the settling time has elapsed. The settling time depends upon the notch frequency chosen for the filter. The output data rate equates to this filter notch frequency and the settling time of the filter to a full-scale step input is 4 times the output data period. In applications using both input channels, the settling time of the filter must be allowed to elapse before data from the second channel is accessed.

Post Filtering

The on-chip modulator provides samples at a 3.9 kHz output rate (2 MHz clock) and 19.5 kHz (10 MHz clock). The on-chip digital filter decimates these samples to provide data at an output rate which corresponds to the programmed first notch frequency of the filter. Since the output data rate exceeds the Nyquist criterion, the output rate for a given bandwidth will satisfy most application requirements. However, there may be some applications which require a higher data rate for a given bandwidth and noise performance. Applications which need this higher data rate will require some post filtering following the digital filter of the AD7711/AD7713.

For example, if the required bandwidth is 7.86 Hz but the required update rate is 100 Hz, the data can be taken from the AD7711/AD7713 at the 100 Hz rate giving a −3 dB bandwidth of 26.2 Hz. Post filtering can be applied to this to reduce the bandwidth and output noise, to the 7.86 Hz bandwidth level, while maintaining an output rate of 100 Hz.

Post filtering can also be used to reduce the output noise from the device for low bandwidths. Noise in these bandwidths is essentially device noise or white noise, and since the input is chopped, the noise has a flat frequency response. By reducing the bandwidth, the noise in the resultant passband can be reduced. A reduction in bandwidth by a factor of 2 results in a $\sqrt{2}$ reduction in the output rms noise. This additional filtering will result in a longer settling time.

Antialias Considerations

The digital filter does not provide any rejection at integer multiples of the modulator sample frequency. This means that there are frequency bands, $\pm f_{3\ dB}$ wide ($f_{3\ dB}$ is cutoff frequency most broadband noise is filtered. In any case, because of the high oversampling ratio a simple, RC, single-pole filter is generally sufficient to attenuate the signals in these bands on the analog input and thus provide adequate antialiasing filtering.

If passive components are placed in front of the AIN1 and AIN2 inputs of the AD7711/AD7713, care must be taken to ensure that the source impedance is low enough so as not to introduce gain errors in the system. The dc input impedance for the AIN1 and AIN2 inputs is over 1 GΩ. The input appears as a dynamic load which varies with the clock frequency and with the selected gain (see Figure 3). The input sample rate, as shown in Table III, determines the time allowed for the analog input capacitor, C_{IN}, to be charged. External impedances result in a longer charge time for this capacitor and this may result in gain errors being introduced on the analog inputs. Both inputs of the differential input channels look into similar input circuitry.

In any case, the error introduced due to longer charging times is a gain error which can be removed using the system calibration capabilities of the AD7711/AD7713 provided that the resultant span is within the span limits of the system calibration techniques for the AD7711/AD7713.

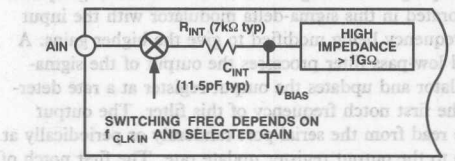


Figure 3. AIN1, AIN2 Input Impedance

The AIN3 input of the AD7713 contains a resistive attenuation network as outlined in Figure 4. The typical input impedance on this input is 44 kΩ. As a result, the AIN3 input of the AD7713 should be driven from a low impedance source.

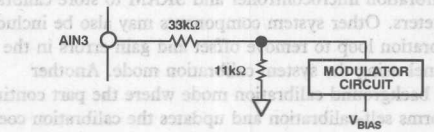


Figure 4. AIN3 Input Impedance

ANALOG INPUT FUNCTIONS

Analog Input Ranges

Both analog inputs on the AD7711 are programmable-gain, input channels which can handle either unipolar or bipolar input signals. The AIN1 channel of the AD7711 is a differential input channel having a common-mode range from V_{SS} to AV_{DD}, provided that the absolute value of the analog input voltage lies between V_{SS} − 30 mV and AV_{DD} + 30 mV. The AIN2 input channel is a single-ended input that is referred to AGND.

The analog inputs on the AD7713 provide the user with considerable flexibility in terms of analog input voltage ranges. Two of the inputs are differential, programmable-gain, input channels which can handle either unipolar or bipolar input signals. The common-mode range of these inputs is from AGND to AV_{DD}

provided that the absolute value of the analog input voltage lies between AGND −30 mV and AV_{DD}+30 mV. The third analog input is a single-ended, programmable gain high-level input which accepts analog input ranges of 0 to +4 × V_{REF}/GAIN.

The dc input leakage current on the AIN1 and AIN2 inputs is 10 pA maximum at 25°C (±1 nA over temperature). This results in a dc offset voltage developed across the source impedance. However, this dc offset effect can be compensated for by a combination of the differential input capability of the part and its system calibration mode. The dc input current on the AIN3 of the AD7713 input depends on the input voltage, For the nominal input voltage range of +10 V, the input current is 225 μA typ.

Burn Out Current

The AIN1(+) input of the AD7711/AD7713 contains a current source which can be turned on/off via the control register. This current source can be used in checking that a transducer has not burnt out or gone open circuit before attempting to take measurements on that channel. If the current is turned on and is allowed flow into the transducer and a measurement of the input voltage on the AIN1 input is taken, it can indicate that the transducer is not functioning correctly. For normal operation, this burn out current is turned off by writing a 0 to the BO bit in the control register. The burn-out current is 1 μA for the AD7711 and 200 nA for the AD7713.

RTD Excitation Currents

The AD7711/AD7713 also contains two matched 200 μA constant current sources which are provided at the RTD1 and RTD2 pins of the device. These currents can be turned on/off via the control register. Writing a 1 to the RO bit of the control register enables these excitation currents.

For four-wire RTD applications, one of these excitation currents is used to provide the excitation current for the RTD, the second current source can be left unconnected. For three-wire RTD configurations, the second on-chip current source can be used to eliminate errors due to voltage drops across lead resistances.

The temperature coefficient of the RTD current sources is typically 20 ppm/°C with a typical matching between the temperature coefficients of both current sources of 3 ppm/°C. For applications where the absolute value of the temperature coefficient is too large, the following schemes can be used to remove the drift error.

The conversion result from the AD7711/AD7713 is ratiometric to the V_{REF} voltage. Therefore, if the V_{REF} voltage varies with the RTD temperature coefficient, the temperature drift from the current source will be removed. For four-wire RTD applications, the reference voltage can be made ratiometric to RTD current source by using the second current with a low TC resistor to generate the reference voltage for the part. In this case if a 12.5 kΩ resistor is used, the 200 μA current source generates +2.5 V across the resistor. This +2.5 V can be applied to the REF IN(+) input of the part and with the REF IN(−) input at ground it will supply a V_{REF} of 2.5 V for the part. For three-wire RTD configurations, the reference voltage for the part is generated by placing a low TC resistor (12.5 kΩ for 2.5 V reference) in series with one of the constant current sources. The RTD current sources can be driven to within 2 V of AV_{DD}. The reference input of the part is differential so the REF IN(+) and REF IN(−) of the part are driven from either side of the resistor. Both schemes ensure that the reference voltage for the part tracks the RTD current sources over temperature and, thereby, removes the temperature drift error.

Bipolar/Unipolar Inputs

The AIN1 and AIN2 inputs on both parts can accept either unipolar or bipolar input voltage ranges while the AIN3 of the AD7713 accepts only unipolar signals. Bipolar or unipolar options for AIN1 and AIN2 are chosen by programming the B/U bit of the control register. This programs both channels for either unipolar or bipolar operation. Programming the part for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding. The data coding is binary for unipolar inputs and offset binary for bipolar inputs.

The AIN1 and AIN2 channels of the AD7713 and the AIN1 input of the AD7711 are differential, and as a result, the voltage to which the unipolar and bipolar signals are referenced is the voltage on the respective AIN(−) input. For example, if AIN(−) is +1.25 V and the part is configured for unipolar operation with a gain of 1 and a V_{REF} of +2.5 V, the input voltage range on the AIN(+) input is +1.25 V to +3.75 V. For the AIN3 input of the AD7713 and the AIN2 input of the AD7711, the input signals are referenced to AGND.

REFERENCE INPUT

The reference inputs of the part, REF IN(+) and REF IN(−), provide a differential reference input capability. The common-mode range for these differential inputs is from V_{SS} to AV_{DD} (AGND to AV_{DD} on AD7713). The nominal differential voltage, V_{REF} (REF IN(+) − REF IN(−)), is +2.5 V for specified operation but the reference voltage can go to +5 V with no degradation in performance provided that the absolute value of REF IN(+) and REF IN(−) does not exceed its supply limits. The part is also functional with V_{REF} voltages down to 1 V but with degraded performance as the output noise will, in terms of LSB size, be larger. REF IN(+) must always be greater than REF IN(−) for correct operation of the AD7711/AD7713.

Both reference inputs provide a high impedance, dynamic load similar to the analog inputs. The maximum dc input leakage current is 10 pA (±1 nA over temperature) and source resistance may result in gain errors on the part. The reference inputs look like the AIN1 analog input (see Figure 3). In this case, R_{INT} is 5 kΩ typ and C_{INT} varies with gain. The input sample rate is $f_{CLK\ IN}$/512 and does not vary with gain. For gains of 1 to 8 C_{INT} is 20 pF; for a gain of 16 it is 10 pF, for a gain of 32 it is 5 pF, for a gain of 64 it is 2.5 pF, and for a gain of 128 it is 1.25 pF.

The digital filter of the part removes noise from the reference input just as it does with the analog input, and the same limitations apply regarding lack of noise rejection at integer multiples of the sampling frequency. The output noise performance outlined in Tables I and II assumes a clean reference. If the reference noise in the bandwidth of interest is excessive, it can degrade the performance of the AD7711/AD7713. Recommended references for the AD7711/AD7713 are the AD680 and AD780, +2.5 V references.

REFERENCE OUTPUT (AD7711 ONLY)

The AD7711 contains a temperature compensated +2.5 V reference which has an initial tolerance of ±4%. This reference voltage is provided at the REF OUT pin, and it can be used as the reference voltage for the part by connecting REF OUT to the REF IN(+) pin. This REF OUT pin is a single-ended output, referenced to AGND, which is capable of providing up to 1 mA to an external load. In applications where REF OUT is connected

directly to REF IN(+), REF IN(−) should be tied to AGND to provide the nominal +2.5 V reference for the AD7711.

Using the on-chip reference as the reference source for the part results in somewhat degraded output noise performance from the AD7711 for portions of the noise table that are dominated by the device noise. The on-chip reference noise effect is eliminated in ratiometric applications where the reference is used to provide the excitation voltage for the analog front end.

V_{BIAS} Input (AD7711 only)

The V_{BIAS} input determines at what voltage the internal analog circuitry is biased. It essentially provides the return path for analog currents flowing in the modulator and, as such, it should be driven from a low impedance point to minimize errors.

For maximum internal headroom, the V_{BIAS} voltage should be set halfway between AV_{DD} and V_{SS}. The difference between AV_{DD} and (V_{BIAS} + 0.85 × V_{REF}) determines the amount of headroom the circuit has at the upper end, while the difference between V_{SS} and (V_{BIAS} − 0.85 × V_{REF}) determines the amount of headroom the circuit has at the lower end. Care should be taken in choosing a V_{BIAS} voltage to ensure that it stays within prescribed limits. For single +5 V operation, the selected V_{BIAS} voltage must ensure that V_{BIAS} ± 0.85 × V_{REF} does not exceed AV_{DD} or V_{SS} or that the V_{BIAS} voltage itself is greater than V_{SS} + 2.1 V and less than AV_{DD} − 2.1 V. For single +10 V operation or dual ±5 V operation, the selected V_{BIAS} voltage must ensure that V_{BIAS} × 0.85 × V_{REF} does not exceed AV_{DD} or V_{SS} or that the V_{BIAS} voltage itself is greater than V_{SS} + 3 V or less than AV_{DD} − 3 V. For example, with AV_{DD} = +4.75 V, V_{SS} = 0 V and V_{REF} = +2.5 V, the allowable range for the V_{BIAS} voltage is +2.125 V to +2.625 V. With AV_{DD} = +9.5 V, V_{SS} = 0 V and V_{REF} = 5 V, the range for V_{BIAS} is +4.25 V to +5.25 V. With AV_{DD} = +4.75 V, V_{SS} = −4.75 V and V_{REF} = +2.5 V, the V_{BIAS} range is −2.625 V to +2.625 V.

The V_{BIAS} voltage does have an effect on the AV_{DD} power supply rejection performance of the AD7711. If the V_{BIAS} voltage tracks the AV_{DD} supply, it improves the power supply rejection from the AV_{DD} supply line from 80 dB to 95 dB. Using an external Zener diode, connected between the AV_{DD} line and V_{BIAS}, as the source for the V_{BIAS} voltage gives the improvement in AV_{DD} power supply rejection performance.

USING THE AD7711/AD7713

SYSTEM DESIGN CONSIDERATIONS

The AD7711/AD7713 operates differently from successive approximation ADCs or integrating ADCs. Since it samples the signal continuously, like a tracking ADC, there is no need for a start convert command. The output register is updated at a rate determined by the first notch of the filter and the output can be read at any time, either synchronously or asynchronously.

Clocking

The AD7711/AD7713 requires a master clock input, which may be an external TTL/CMOS compatible clock signal applied to the MCLK IN pin with the MCLK OUT pin left unconnected. Alternatively, a crystal of the correct frequency can be connected between MCLK IN and MCLK OUT, in which case the clock circuit will function as a crystal controlled oscillator. For lower clock frequencies, a ceramic resonator may be used instead of the crystal. For these lower frequency oscillators, external capacitors may be required on either the ceramic resonator or on the crystal.

The input sampling frequency, the modulator sampling frequency, the −3 dB frequency, output update rate and calibration time are all directly related to the master clock frequency, $f_{CLK\ IN}$. Reducing the master clock frequency by a factor of 2 will halve the above frequencies and update rate and will double the calibration time.

The current drawn from the DV_{DD} power supply is also directly related to $f_{CLK\ IN}$. Reducing $f_{CLK\ IN}$ by a factor of 2 will halve the DV_{DD} current but will not affect the current drawn from the AV_{DD} power supply.

System Synchronization

If multiple AD7711/AD7713s are operated from a common master clock, they can be synchronized to update their output registers simultaneously. A falling edge on the $\overline{SYNC}$ input resets the filter and places the part into a consistent, known state. A common signal to the parts' $\overline{SYNC}$ inputs will synchronize their operation. This would normally be done after each AD7711/AD7713 has performed its own calibration or has had calibration coefficients loaded to it.

The $\overline{SYNC}$ input can also be used to reset the digital filter in systems where the turn-on time of the digital power supply (DV_{DD}) is very long. In such cases, the AD7711/AD7713 will start operating internally before the DV_{DD} line has reached its minimum operating level, +4.75 V. With a low DV_{DD} voltage, the part's internal digital filter logic does not operate correctly. Thus, the AD7711/AD7713 may have clocked itself into an incorrect operating condition by the time that DV_{DD} has reached its correct level. The digital filter will be reset upon issue of a calibration command (whether it is self-calibration, system calibration or background calibration) to the AD7711/AD7713. This ensures correct operation of the AD7711/AD7713. In systems where the power-on default conditions of the part are acceptable and no calibration is performed after power-on, issuing a $\overline{SYNC}$ pulse to the part will reset the AD7711/AD7713's digital filter logic. An R, C on the $\overline{SYNC}$ line, with R, C time constant longer than the DV_{DD} power-on time, will perform the $\overline{SYNC}$ function.

ACCURACY

Sigma-Delta ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no missing codes performance. The AD7711/AD7713 achieves excellent linearity by the use of high quality, on-chip silicon dioxide capacitors, which have a very low capacitance/voltage coefficient. The device also achieves low input drift through the use of chopper-stabilized techniques in its input stage. To ensure excellent performance over time and temperature, the AD7711/AD7713 uses digital calibration techniques which minimize offset and gain error.

AUTOCALIBRATION

Autocalibration on the AD7711/AD7713 removes offset and gain errors from the device. A calibration routine should be initiated on the device whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the selected gain, filter notch or bipolar/unipolar input range. However, if the AD7711/AD7713 is in its background calibration mode, the above changes are all automatically taken care of (after the settling time of the filter has been allowed for).

The AD7711/AD7713 offers self-calibration, system calibration and background calibration facilities. For calibration to occur on the selected channel, the on-chip microcontroller must record the modulator output for two different input conditions. These are "zero-scale" and "full-scale" points. With these readings, the microcontroller can calculate the gain slope for the input to output transfer function of the converter. Internally, the part works with a resolution of 33 bits to determine its conversion result of either 16 bits or 24 bits.

The part also provides the facility to write to the on-chip calibration registers and in this manner the span and offset for the part can be adjusted by the user. The offset calibration register contains a value which is subtracted from all conversion results, while the full-scale calibration register contains a value which is multiplied by all conversion results. The offset calibration coefficient is subtracted from the result prior to the multiplication by the full-scale coefficient. In the first three modes outlined here, the $\overline{\text{DRDY}}$ line indicates that calibration is complete by going low. If $\overline{\text{DRDY}}$ is low before (or goes low during) the calibration command, it may take up to one modulator cycle before $\overline{\text{DRDY}}$ goes high to indicate that calibration is in progress. Therefore, $\overline{\text{DRDY}}$ should be ignored for up to one modulator cycle after the last bit of the calibration command is written to the control register.

Self-Calibration

In the self-calibration mode with a unipolar input range, the zero-scale point used in determining the calibration coefficients is with both inputs shorted (i.e., AIN(+) = AIN(−) = V_{BIAS} for the differential inputs and AIN = V_{BIAS} for AIN2 of the AD7711 and AIN3 of the AD7713) and the full-scale point is V_{REF}. The zero-scale coefficient is determined by converting an internal shorted inputs node. The full-scale coefficient is determined from the span between this shorted inputs conversion and a conversion on an internal V_{REF} node. The self-calibration mode is invoked by writing the appropriate values (0, 0, 1) to the MD2, MD1 and MD0 bits of the control register. In this calibration mode, the shorted inputs node is switched in to the modulator first and a conversion is performed; the V_{REF} node is then switched in and another conversion is performed. When the calibration sequence is complete, the calibration coefficients updated and the filter resettled to the analog input voltage, the $\overline{\text{DRDY}}$ output goes low. The self-calibration procedure takes into account the selected gain on the PGA.

For bipolar input ranges in the self-calibrating mode, the sequence is very similar to that just outlined. In this case, the two points which the AD7711/AD7713 calibrates are midscale (bipolar zero) and positive full scale.

System Calibration

System calibration allows the AD7711/AD7713 to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self-calibration but uses voltage values presented by the system to the AIN inputs for the zero and full-scale points. System calibration is a two-step process. The zero-scale point must be presented to the converter first. It must be applied to the converter before the calibration step is initiated and remain stable until the step is complete. System calibration is initiated by writing the appropriate values (0, 1, 0) to the MD2, MD1 and MD0 bits of the control register. The $\overline{\text{DRDY}}$ output from the device will signal when the step is complete by going low. After the zero-scale point is calibrated, the full-scale point is applied and the second step of the calibration process is initiated by again writing the appropriate values (0, 1, 1) to MD2, MD1 and MD0. Again the full-scale voltage must be set up before the calibration is initiated and it must remain stable throughout the calibration step. $\overline{\text{DRDY}}$ goes low at the end of this second step to indicate that the system calibration is complete. In the unipolar mode, the system calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

This two-step system calibration mode offers another feature. After the sequence has been completed, additional offset or gain calibrations can be performed by themselves to adjust the zero reference point or the system gain. This is achieved by performing the first step of the system calibration sequence (by writing 0, 1, 0 to MD2, MD1, MD0). This will adjust the zero scale or offset point but will not change the slope factor from what was set during a full system calibration sequence.

System calibration can also be used to remove any errors from an antialiasing filter on the analog input. A simple R, C antialiasing filter on the front end may introduce a gain error on the analog input voltage but the system calibration can be used to remove this error.

System Offset Calibration

System offset calibration is a variation of both the system calibration and self-calibration. In this case, the zero-scale point for the system is presented to the AIN input of the converter. System offset calibration is initiated by writing 1, 0, 0 to MD2, MD1, MD0. The system zero-scale coefficient is determined by converting the voltage applied to the AIN input, while the full-scale coefficient is determined from the span between this AIN conversion and a conversion on V_{REF}. The zero-scale point should be applied to the AIN input for the duration of the calibration sequence. This is a one-step calibration sequence with $\overline{\text{DRDY}}$ going low when the sequence is completed. In the unipolar mode, the system offset calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

Background Calibration

The AD7711/AD7713 also offers a background calibration mode where the part interleaves its calibration procedure with its normal conversion sequence. In the background calibration mode, the same voltages are used as the calibration points as are used in the self-calibration mode, i.e., shorted inputs and V_{REF}. The background calibration mode is invoked by writing 1, 0, 1 to MD2, MD1, MD0 of the control register. When invoked, the background calibration mode reduces the output data rate of the part by a factor of six while the −3 dB bandwidth remains unchanged. Its advantage is that the part is continually performing calibration and automatically updating its calibration coefficients. As a result, the effects of temperature drift, supply sensitivity and time drift on zero and full-scale errors are automatically removed. When the background calibration mode is turned on, the part will remain in this mode until bits MD2, MD1 and MD0 of the control register are changed. With background calibration mode on, the first result from the AD7711/AD7713 will be incorrect as the full-scale calibration will not have been performed. For a step change on the input, the second output update will have settled to 100% of the final value.

Table IV summarizes the calibration modes and the calibration points associated with them. It also gives the duration from

when the calibration is invoked to when valid data is available to the user.

Span and Offset Limits

Whenever a system calibration mode is used, there are limits on the amount of offset and span that can be accommodated. The range of input span in both the unipolar and bipolar modes for the AIN1 and AIN2 inputs of both the AD7711 and AD7713 has a minimum value of $0.8 \times V_{REF}/GAIN$ and a maximum value of $2.1 \times V_{REF}/GAIN$. For AIN3 of the AD7713, the minimum value is $3.2 \times V_{REF}/GAIN$ while the maximum value is $4.2 \times V_{REF}/GAIN$.

The amount of offset that can be accommodated depends on whether the unipolar or bipolar mode is being used. This offset range is limited by the requirement that the positive full-scale calibration limit is $\leq 1.05 \times V_{REF}/GAIN$ for AIN1 and AIN2. Therefore, the offset range plus the span range cannot exceed $1.05 \times V_{REF}/GAIN$ for AIN1 and AIN2. If the span is at its minimum ($0.8 \times V_{REF}/GAIN$) the maximum the offset can be is ($0.25 \times V_{REF}/GAIN$) for AIN1 and AIN2. For AIN3, both ranges are multiplied by a factor of 4.

In the bipolar mode, the system offset calibration range is again restricted by the span range. The span range of the converter in bipolar mode is equidistant around the voltage used for the zero-scale point thus the offset range plus half the span range cannot exceed ($1.05 \times V_{REF}/GAIN$) for AIN1 and AIN2. If the span is set to $2 \times V_{REF}/GAIN$, the offset span cannot move more than $\pm(0.05 \times V_{REF}/GAIN)$ before the endpoints of the transfer function exceed the input overrange limits $\pm(1.05 \times V_{REF}/GAIN)$ for AIN1. If the span range is set to the minimum $\pm(0.4 \times V_{REF}/GAIN)$ the maximum allowable offset range is $\pm(0.65 \times V_{REF}/GAIN)$ for AIN1 and AIN2. The AIN3 input can only be used in the unipolar mode.

Table IV. Calibration Truth Table

Cal Type	MD2, MD1, MD0	Zero-Scale Cal	Full-Scale Cal	Sequence	Duration
Self-Cal	0, 0, 1	Shorted Inputs	V_{REF}	One Step	9 × 1/Output Rate
System Cal	0, 1, 0	AIN		Two Step	4 × 1/Output Rate
System Cal	0, 1, 1		AIN	Two Step	4 × 1/Output Rate
System Offset Cal	1, 0, 0	AIN	V_{REF}	One Step	9 × 1/Output Rate
Background Cal	1, 0, 1	Shorted Inputs	V_{REF}	One Step	6 × 1/Output Rate

POWER-UP AND CALIBRATION

On power-up, the AD7711/AD7713 performs an internal reset which sets the contents of the control register to a known state. However, to ensure correct calibration for the device, a calibration routine should be performed after power-up.

The power dissipation and temperature drift of the part are low and no warm-up time is required before the initial calibration is performed. However, the external reference must have stabilized before calibration is initiated.

Drift Considerations

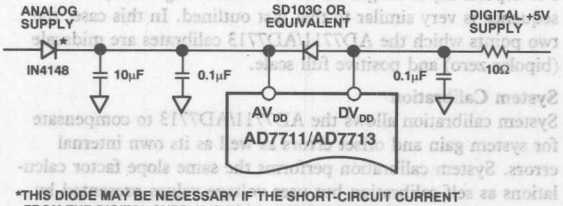
The AD7711/AD7713 uses chopper stabilization techniques to minimize input offset drift. Charge injection in the analog switches and dc leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. The dc input leakage current is essentially independent of the selected gain. Gain drift within the converter depends primarily upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter or by operating the part in the background calibration mode. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. Integral and differential linearity errors are not significantly affected by temperature changes.

POWER SUPPLIES AND GROUNDING

The analog and digital supplies to the AD7711/AD7713 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital supply (DV_{DD}) must never exceed the analog positive supply (AV_{DD}) by more than 0.3 V. Power supply sequencing is, therefore, important. If separate analog and digital supplies are used, care must be taken to ensure that the analog supply is powered up first. If this cannot be ensured or if DV_{DD} can exceed AV_{DD} at any other time, the protection scheme outlined in Figure 5 is recommended to protect the device. In systems where $AV_{DD} = +5$ V and $DV_{DD} = +5$ V, it is recommended that AV_{DD} and DV_{DD} are driven from the same +5 V supply, although each supply should be decoupled separately. It is preferable that the common supply is the system's analog +5 V supply.

It is also important that power is applied to the AD7711/AD7713 before signals at REF IN, AIN or the logic input pins in order to avoid latch-up. If separate supplies are used for the AD7711/AD7713 and the system digital circuitry, then the AD7711/AD7713 should be powered up first. If it is not possible to guarantee this, then current limiting resistors should be placed in series with the logic inputs.



*THIS DIODE MAY BE NECESSARY IF THE SHORT-CIRCUIT CURRENT FROM THE DIGITAL SUPPLY IS TOO LARGE FOR THE SD103C.

Figure 5. Protection Scheme for DV_{DD} Powering-Up Before AV_{DD}

DIGITAL INTERFACE

The digital interface section for the AD7711/AD7713 is identical to that outlined in the DIGITAL INTERFACE section of the AD7710/AD7712 data sheet.

LC²MOS Signal Conditioning ADC with RTD Current Source

AD7711A*

2

FEATURES

Charge Balancing ADC
- 24 Bits No Missing Codes
- ±0.0015% Nonlinearity

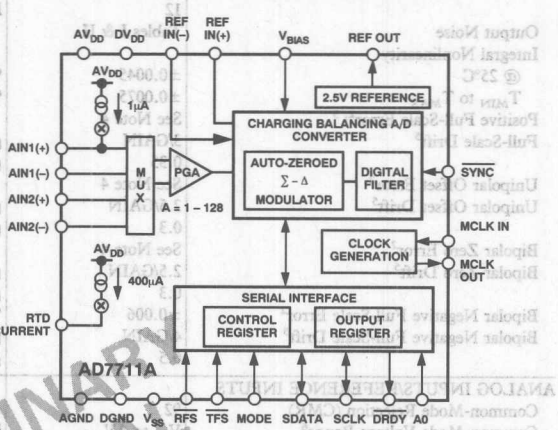
Two-Channel Programmable Gain Front End
- Gains from 1 to 128
- Differential Inputs

Low-Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
Bidirectional Microcontroller Serial Interface
Internal/External Reference Option
Single or Dual Supply Operation
Low Power (25 mW typ) with Power-Down Mode (7 mW typ)

APPLICATIONS

RTD Transducers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

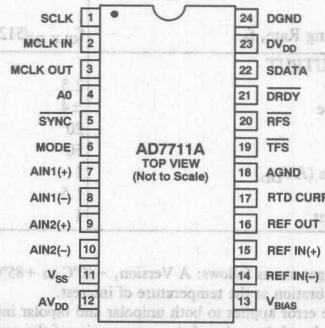
The AD7711A is a complete analog front end for low frequency measurement applications. The device accepts low level signals directly from a transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The part features two differential analog inputs and a differential reference input. Normally, one of the channels will be used as the main channel with the second channel used as an auxiliary input to periodically measure a second voltage. It can be operated from a single supply (by tying the V_{SS} pin to AGND) provided that the input signals on the analog inputs are more positive than −30 mV. By taking the V_{SS} pin negative, the part can convert signals down to $-V_{REF}$ on its inputs. The part also provides a 400 μA current source that can be used to provide excitation for RTD transducers. The AD7711A thus performs all signal conditioning and conversion for a single or dual channel system.

The AD7711A is ideal for use in smart, microcontroller based systems. Input channel selection, gain settings and signal polarity can be configured in software using the bidirectional serial port. The AD7711A contains self-calibration, system calibration and background calibration options and also allows the user to read and write the on-chip calibration registers.

CMOS construction ensures low power dissipation and a software programmable power down mode reduces the standby power consumption to only 7 mW typical. The part is available in a 24-pin, 0.3 inch-wide, plastic and hermetic dual-in-line package (DIP) as well as a 24-lead small outline (SOIC) package.

PIN CONFIGURATION
DIP and SOIC



PRELIMINARY TECHNICAL DATA

***Protected by U.S. Patent No. 5,134,401.**

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. For Filter Notches ≤ 60 Hz
	22	Bits min	For Filter Notch = 100 Hz
	18	Bits min	For Filter Notch = 250 Hz
	15	Bits min	For Filter Notch = 500 Hz
	12	Bits min	For Filter Notch = 1 kHz
Output Noise	Tables I & II		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity			
@ 25°C	±0.0045	% of FSR max	Filter Notches ≤ 60 Hz; Typically ±0.0015%
T_{MIN} to T_{MAX}	±0.0075	% of FSR max	Filter Notches ≤ 60 Hz
Positive Full-Scale Error[2, 3]	See Note 4		Excluding Reference
Full-Scale Drift[5]	3/GAIN	µV/°C typ	Excluding Reference. For Gains of 1, 2, 4, 8
	0.35	µV/°C typ	Excluding Reference. For Gains of 16, 32, 64, 128
Unipolar Offset Error[2]	See Note 4		
Unipolar Offset Drift[5]	2.5/GAIN	µV/°C typ	For Gains of 1, 2, 4, 8
	0.3	µV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Zero Error[2]	See Note 4		
Bipolar Zero Drift[5]	2.5/GAIN	µV/°C typ	For Gains of 1, 2, 4, 8
	0.3	µV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Negative Full-Scale Error[2]	±0.006	% of FSR max	Excluding Reference; Typically ±0.0015%
Bipolar Negative Full-Scale Drift[5]	4/GAIN	µV/°C typ	Excluding Reference. For Gains of 1, 2, 4, 8
	0.5	µV/°C typ	Excluding Reference. For Gains of 16, 32, 64, 128
ANALOG INPUTS/REFERENCE INPUTS			
Common-Mode Rejection (CMR)	92	dB min	At DC
Common-Mode Voltage Range[6]	V_{SS} to AV_{DD}	V min to V max	
Normal Mode 50 Hz Rejection[7]	100	dB min	For Filter Notches of 10, 25, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Normal Mode 60 Hz Rejection[7]	100	dB min	For Filter Notches of 10, 30, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 50 Hz Rejection[7]	150	dB min	For Filter Notches of 10, 25, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 60 Hz Rejection[7]	150	dB min	For Filter Notches of 10, 30, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
DC Input Leakage Current[7] @ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[7]	20	pF max	
Analog Inputs[8]			
Input Voltage Range[9]			For Normal Operation. Depends on Gain Selected
	0 to $+V_{REF}$[10]	nom	Unipolar Input Range (B/U Bit of Control Register = 1)
	$\pm V_{REF}$	nom	Bipolar Input Range (B/U Bit of Control Register = 0)
Input Sampling Rate, f_s	See Table III		
Reference Inputs			
REF IN(+) − REF IN(−) Voltage[11]	+2.5 to +5	V min to V max	For Specified Performance. Part Functions with Lower V_{REF} Voltages
Input Sampling Rate, f_S	$f_{CLK\ IN}/512$		
REFERENCE OUTPUT			
Output Voltage	2.5	V nom	
Initial Tolerance	±4	% max	
Drift	20	ppm/°C typ	
Output Noise	50	µV typ	pk–pk Noise 0.1 Hz to 10 Hz Bandwidth
Line Regulation (AV_{DD})	1	mV/V max	
Load Regulation	1.5	mV/mA max	Maximum Load Current 1 mA
External Current	1	mA max	

NOTES

[1]Temperature ranges are as follows: A Version, −40°C to +85°C; S Version −55°C to +125°C. See also Note 16.

[2]Applies after calibration at the temperature of interest.

[3]Positive full-scale error applies to both unipolar and bipolar input ranges.

[4]These errors will be of the order of the output noise of the part as shown in Table I.

[5]Recalibration at any temperature or use of the background calibration mode will remove these drift errors.

[6]This common-mode voltage range is allowed provided that the input voltage on AIN(+) and AIN(−) does not exceed AV_{DD} + 30 mV and V_{SS} − 30 mV.

[7]These numbers are guaranteed by design and/or characterization.

[8]The analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance depends on the selected gain (see Tables IV and V).

[9]The analog input voltage range on the AIN1(+) and AIN2(+) inputs is given here with respect to the voltage on the AIN1(−) and AIN2(−) inputs. The absolute voltage on the analog inputs should not go more positive than AV_{DD} + 30 mV or go more negative than V_{SS} − 30 mV.

[10]V_{REF} = REF IN(+) – REF IN(−).

[11]The reference input voltage range may be restricted by the input voltage range requirement on the V_{BIAS} input.

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Parameter	A, S Versions[1]	Units	Conditions/Comments
V_{BIAS} INPUT[12]			
Input Voltage Range	$AV_{DD} - 0.85 \times V_{REF}$		See V_{BIAS} Input Section
	or $AV_{DD} - 3$	V max	Whichever Is Smaller; +5 V/−5 V or +10 V/0 V Nominal AV_{DD}/V_{SS}
	or $AV_{DD} - 2.1$	V max	Whichever Is Smaller; +5 V/0 V Nominal AV_{DD}/V_{SS}
	$V_{SS} + 0.85 \times V_{REF}$		See V_{BIAS} Input Section
	or $V_{SS} + 3$	V min	Whichever Is Greater; +5 V/−5 V or +10 V/0 V Nominal AV_{DD}/V_{SS}
	or $V_{SS} + 2.1$	V min	Whichever Is Greater; +5 V/0 V Nominal AV_{DD}/V_{SS}
V_{BIAS} Rejection	65 to 85	dB typ	Increasing with Gain
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	$DV_{DD} - 1$	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[13]	9	pF typ	
TRANSDUCER BURN-OUT			
Current	100	nA nom	
Initial Tolerance	±10	% typ	
Drift	0.1	%/°C typ	
RTD EXCITATION CURRENT			
Output Current	400	μA nom	
Initial Tolerance	±20	μA max	
Drift	20	ppm/°C typ	
Line Regulation (AV_{DD})	400	nA/V max	AV_{DD} = +5 V
Load Regulation	400	nA/V max	
Output Compliance	$AV_{DD} - 2$	V max	
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[14]	$(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[14]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[15]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[15]	$0.8 \times V_{REF}/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(2.1 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)

NOTES

[12]The AD7711A is tested with the following V_{BIAS} voltages. With AV_{DD} = +5 V and V_{SS} = 0 V, V_{BIAS} = +2.5 V; with AV_{DD} = +10 V and V_{SS} = 0 V, V_{BIAS} = +5 V and with AV_{DD} = +5 V and V_{SS} = −5 V, V_{BIAS} = 0 V.

[13]Sample tested at +25°C to ensure compliance.

[14]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale then the device will output all 0s.

[15]These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed AV_{DD} + 30 mV or go more negative than V_{SS} − 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

PRELIMINARY TECHNICAL DATA

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AD7711A—SPECIFICATIONS

Parameter	A, S Versions[1]	Units	Conditions/Comments
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage[16]	+5 to +10	V nom	±5% for Specified Performance
DV_{DD} Voltage[17]	+5	V nom	±5% for Specified Performance
AV_{DD}-V_{SS} Voltage	+10.5	V max	For Specified Performance
Power Supply Currents			
AV_{DD} Current	4	mA max	
DV_{DD} Current	4.5	mA max	
V_{SS} Current	1.5	mA max	V_{SS} = −5 V
Power Supply Rejection[18]			Rejection w.r.t. AGND; Assumes V_{BIAS} Is Fixed
Positive Supply (AV_{DD})	See Note 19	dB typ	
Negative Supply (V_{SS})	90	dB typ	
Power Dissipation			
Normal Mode	45	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V; Typically 25 mW
Normal Mode	52.5	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = −5 V; Typically 30 mW
Standby (Power-Down) Mode	15	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V or −5 V; Typically 7 mW

NOTES

[16]The AD7711A is specified with a 10 MHz clock for AV_{DD} voltages of +5 V ±5%. It is specified with an 8 MHz clock for AV_{DD} voltages greater than 5.25 V and less than 10.5 V. Operation with AV_{DD} voltages in the range 5.25 V to 10.5 V is only guaranteed over the 0 to +70°C temperature range.

[17]The ±5% tolerance on the DV_{DD} input is allowed provided that DV_{DD} does not exceed AV_{DD} by more than 0.3 V.

[18]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 10 Hz, 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 10 Hz, 30 Hz or 60 Hz.

[19]PSRR depends on gain: Gain of 1: 70 dB typ; Gain of 2: 75 dB typ; Gain of 4: 80 dB typ; Gains of 8 to 128: 85 dB typ. These numbers can be improved (to 95 dB typ) by deriving the V_{BIAS} voltage (via Zener diode or reference) from the AV_{DD} supply.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C, unless otherwise noted)

AV_{DD} to DV_{DD} . . . . . −0.3 V to +12 V
AV_{DD} to V_{SS} . . . . . −0.3 V to +12 V
AV_{DD} to AGND . . . . . −0.3 V to +12 V
AV_{DD} to DGND . . . . . −0.3 V to +12 V
DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to DGND . . . . . −0.3 V to +6 V
V_{SS} to AGND . . . . . +0.3 V to −6 V
V_{SS} to DGND . . . . . +0.3 V to −6 V
Analog Input Voltage to AGND
. . . . . V_{SS} − 0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND
. . . . . V_{SS} − 0.3 V to AV_{DD} + 0.3 V
REF OUT to AGND . . . . . −0.3 V to AV_{DD}
Digital Input Voltage to DGND . . . −0.3 V to AV_{DD} + 0.3 V
Digital Output Voltage to DGND . . −0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Commercial (A Version) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates Above +75°C . . . . . 6 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD7711AAN	−40°C to +85°C	N-24
AD7711AAR	−40°C to +85°C	R-24

NOTES

[1]To order MIL-STD-883B, Class B processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.

[2]N = Plastic DIP; R = SOIC. For outline information see Package Information section.

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CONTROL REGISTER (24 BITS)

A write to the device with the A0 input low writes data to the control register. A read to the device with the A0 input low accesses the contents of the control register. The control register is 24-bits wide and when writing to the register 24 bits of data must be written otherwise the data will not be loaded to the control register. In other words, it is not possible to write just the first 12-bits of data into the control register. If more than 24 clock pulses are provided before $\overline{TFS}$ returns high, then all clock pulses after the 24th clock pulse are ignored. Similarly, a read operation from the control register should access 24 bits of data.

MSB

MD2	MD1	MD0	G2	G1	G0	CH	PD	WL	IO	BO	B/U

FS11*	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

LSB

*Must always be 0 to ensure correct operation of the device.

Operating Mode			
MD2	MD1	MD0	Operating Mode
0	0	0	Normal Mode. This is the normal mode of operation of the device whereby a read to the device with A0 high accesses data from the data register. This is the default condition of these bits after the internal power on reset.
0	0	1	Activate Self-Calibration. This activates self-calibration on the channel selected by CH. This is a one-step calibration sequence, and when complete, the part returns to normal mode (with MD2, MD1, MD0 of the control register returning to 0, 0, 0). The $\overline{DRDY}$ output indicates when this self-calibration is complete and valid data is available in the output register. For this calibration type, the zero scale calibration is done internally on shorted (zeroed) inputs and the full-scale calibration is done internally on V_{REF}.
0	1	0	Activate System Calibration. This activates system calibration on the channel selected by CH. This is a two-step calibration sequence, with the zero scale calibration done first on the selected input channel and $\overline{DRDY}$ indicating when this zero scale calibration is complete. The part returns to normal mode at the end of this first step in the two-step sequence.
0	1	1	Activate System Calibration. This is the second step of the system calibration sequence with full-scale calibration being performed on the selected input channel. Once again, $\overline{DRDY}$ indicates when the full-scale calibration is complete. When this calibration is complete, the part returns to normal mode.
1	0	0	Activate System Offset Calibration. This activates system offset calibration on the channel selected by CH. This is a one-step calibration sequence and, when complete, the part returns to normal mode with $\overline{DRDY}$ indicating when this system offset calibration is complete. For this calibration type, the zero scale calibration is done on the selected input channel and the full-scale calibration is done internally on V_{REF}.
1	0	1	Activate Background Calibration. This activates background calibration on the channel selected by CH. If the background calibration mode is on, then the AD7711A provides continuous self-calibration of the reference and shorted (zeroed) inputs. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the device when there is a change in the ambient temperature. In this mode, the shorted (zeroed) inputs and V_{REF}, as well as the analog input voltage, are continuously monitored and the calibration registers of the device are automatically updated.
1	1	0	Read/Write Zero Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the zero scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the zero scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Therefore, when writing to the calibration register 24 bits of data must be written, otherwise the new data will not be transferred to the calibration register.
1	1	1	Read/Write Full-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the full-scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the full-scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Therefore, when writing to the calibration register 24 bits of data must be written, otherwise the new data will not be transferred to the calibration register.

PRELIMINARY TECHNICAL DATA

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PGA Gain

G2	G1	G0	Gain	
0	0	0	1	(Default Condition After the Internal Power-On Reset)
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

Channel Selection

CH	Channel	
0	AIN1	(Default Condition After the Internal Power-On Reset)
1	AIN2	

Power-Down

PD		
0	Normal Operation	(Default Condition After the Internal Power-On Reset)
1	Power-Down	

Word Length

WL	Output Word Length	
0	16-Bit	(Default Condition After Internal Power-On Reset)
1	24-Bit	

RTD Excitation Current

IO		
0	Off	(Default Condition After Internal Power-On Reset)
1	On	

Burn-Out Current

BO		
0	Off	(Default Condition After Internal Power-On Reset)
1	On	

Bipolar/Unipolar Selection (Both Inputs)

B/U		
0	Bipolar	(Default Condition After Internal Power-On Reset)
1	Unipolar	

Filter Selection (FS11–FS0)

The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$) filter response. The 12 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device.

The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency = $(f_{CLK\ IN}/512)/code$ where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 2,000. With the nominal $f_{CLK\ IN}$ of 10 MHz, this results in a first notch frequency range from 9.76 Hz to 1.028 kHz. To ensure correct operation of the AD7711A, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I and II and Figure 2 show the effect of the filter notch frequency and gain on the effective resolution of the AD7711A. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1 kHz, a new word is available every 1 ms.

The settling time of the filter to a full-scale step input change is worst case 4 × 1/(output data rate). This settling time is to 100% of the final value. For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. If the first notch is at 1 kHz, the settling time of the filter to a full-scale input step is 4 ms max. This settling time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with $\overline{SYNC}$ low, the settling time will be 3 × 1/(output data rate). If a change of channels takes place, the settling time is 3 × 1/(output data rate) regardless of the $\overline{SYNC}$ input.

The −3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter −3 dB frequency = 0.262 × first notch frequency.

All other features and functions of the AD7711A are as per the AD7710. Refer to the AD7710/AD7712 data sheet for detailed description.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

3 V/5 V, CMOS, Low Cost, Low Power, Signal Conditioning ADC

AD7714*

FEATURES

Charge Balancing ADC
- **24 Bits No Missing Codes**
- **0.0015% Nonlinearity**

Five-Channel Programmable Gain Front End
- **Gains from 1 to 128**
- **Can be Configured as Three Fully Differential Inputs or Five Pseudo-Differential Inputs**

Three-Wire Serial Interface

3 V (AD7714-3) or 5 V (AD7714-5) Operation

Low Power (750 μW typ) with Power-Down (50 μW typ)

Low-Pass Filter with Programmable Filter Cutoffs

Ability to Read/Write Calibration Coefficients

APPLICATIONS

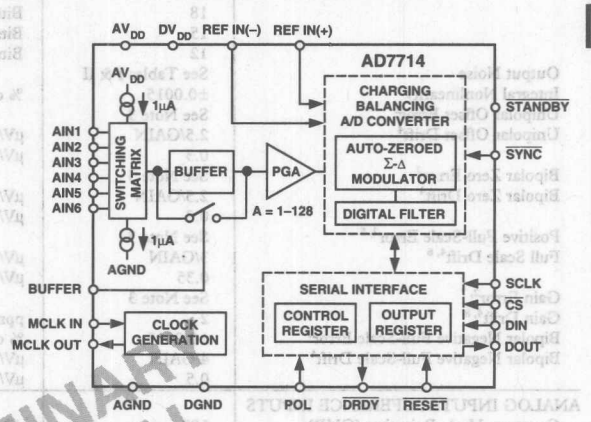
Portable Industrial Instruments

Portable Weigh Scales

Loop-Powered Systems

Smart Transmitters

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7714 is a complete analog front end for low frequency measurement applications. The device accepts low level signals directly from a transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The part features three differential analog inputs (which can also be configured as five pseudo-differential analog inputs) as well as a differential reference input. It operates from a single supply (+3 V or +5 V). The AD7714 thus performs all signal conditioning and conversion for a system consisting of up to five channels.

The AD7714 is ideal for use in smart, microcontroller- or DSP-based systems. It features a serial interface that can be configured for three-wire operation. Gain settings, signal polarity and channel selection can be configured in software using the input serial port. The AD7714 contains self-calibration, system calibration and background calibration options and also allows the user to read and write the on-chip calibration registers.

CMOS construction ensures very low power dissipation, and the power-down mode reduces the standby power consumption to 50 μW typ. The part is available in a 24-pin, 0.3 inch-wide, plastic and hermetic dual-in-line package (DIP); a 24 lead small outline (SOIC) package and a 28-lead shrink small outline package (SSOP).

PRODUCT HIGHLIGHTS

1. The AD7714 consumes less than 500 μA ($f_{CLK\ IN}$ = 1 MHz) or 1 mA ($f_{CLK\ IN}$ = 2.5 MHz) in total supply current, making it ideal for use in loop-powered systems.
2. The programmable gain channels allow the AD7714 to accept input signals directly from a strain gage or transducer removing a considerable amount of signal conditioning.
3. The AD7714 is ideal for microcontroller or DSP processor applications with a three-wire serial interface reducing the number of interconnect lines and reducing the number of opto-couplers required in isolated systems. The part contains on-chip registers that allow control over filter cutoff, input gain, channel selection, signal polarity and calibration modes.
4. The part features excellent static performance specifications with 24-bit no missing codes, ±0.0015% accuracy and low rms noise (<300 mV). End-point errors and the effects of temperature drift are eliminated by on-chip self-calibration, which removes zero-scale and full-scale errors.

*Protected by U.S. Patent No. 5,134,401.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7714-5—SPECIFICATIONS

(AV_{DD} = +5 V, DV_{DD} = +3 V or +5 V, REF IN(+) = +2.5 V; REF IN(–) = AGND; $f_{CLK\ IN}$ = 2.4576 MHz unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. For Filter Notches ≤ 60 Hz
	22	Bits min	For Filter Notch = 100 Hz
	18	Bits min	For Filter Notch = 250 Hz
	15	Bits min	For Filter Notch = 500 Hz
	12	Bits min	For Filter Notch = 1 kHz
Output Noise	See Tables I & II		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.0015	% of FSR max	Filter Notches ≤ 60 Hz
Unipolar Offset Error[2]	See Note 3		
Unipolar Offset Drift[4]	2.5/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.3	μV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Zero Error[2]	See Note 3		
Bipolar Zero Drift[4]	2.5/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.3	μV/°C typ	For Gains of 16, 32, 64, 128
Positive Full-Scale Error[2, 5]	See Note 3		
Full Scale Drift[4, 6]	3/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.35	μV/°C typ	For Gains of 16, 32, 64, 128
Gain Error[2, 7]	See Note 3		
Gain Drift[4, 8]	2	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error[2]	±0.0015	% of FSR max	Typically ±0.0004%
Bipolar Negative Full-Scale Drift[4]	4/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.5	μV/°C typ	For Gains of 16, 32, 64, 128
ANALOG INPUTS/REFERENCE INPUTS			
Common-Mode Rejection (CMR)	100	dB min	At DC. See Table VI
Absolute/Common-Mode Range[9]	AGND to AV_{DD}	V min to V max	
Absolute/Common-Mode Range[9]	AGND + 50 mV to AV_{DD} – 1.5 V	V min to V max	Analog Input with BUFFER = 1
Normal-Mode 50 Hz Rejection[10]	100	dB min	For Filter Notches of 10, 25, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Normal-Mode 60 Hz Rejection[10]	100	dB min	For Filter Notches of 10, 30, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 50 Hz Rejection[10]	150	dB min	For Filter Notches of 10, 25, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 60 Hz Rejection[10]	150	dB min	For Filter Notches of 10, 30, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Input Current[10]	1	nA max	BUFFER = 1
DC Input Leakage Current[10]			BUFFER = 0
@ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[10]	10	pF max	
Analog Inputs[11]			
Input Voltage Range[12]	0 to $+V_{REF}$/GAIN[13]	nom	Unipolar Input Range (B/U Bit of Filter High Register = 1)
	$\pm V_{REF}$/GAIN	nom	Bipolar Input Range (B/U Bit of Filter High Register = 0)
Input Sampling Rate, f_S	GAIN × $f_{CLK\ IN}$/128		For Gains of 1, 2, 4
	$f_{CLK\ IN}$/16		For Gains of 8, 16, 32, 64, 128
Reference Inputs			
REF IN(+) – REF IN(–) Voltage	+2.5	V nom	±5% for Specified Performance. Part Functions with Lower V_{REF} Voltages
Input Sampling Rate, f_S	$f_{CLK\ IN}$/128		
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = +5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = +3 V
V_{INH}, Input High Voltage	3.5	V min	DV_{DD} = +5 V
V_{INH}, Input High Voltage	2.5	V min	DV_{DD} = +3 V
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 800 μA.
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 μA. DV_{DD} = +5 V
V_{OH}, Output High Voltage	DV_{DD} – 0.4	V min	I_{SOURCE} = 200 μA. DV_{DD} = +3 V
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[14]	9	pF typ	

PRELIMINARY TECHNICAL DATA

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AD7714-3–SPECIFICATIONS

(AV_{DD} = +3 V, DV_{DD} = +3 V, REF IN(+) = +1.25 V; REF IN(–) = AGND; $f_{CLK\ IN}$ = 2.4576 MHz unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. For Filter Notches ≤ 60 Hz
	22	Bits min	For Filter Notch = 100 Hz
	18	Bits min	For Filter Notch = 250 Hz
	15	Bits min	For Filter Notch = 500 Hz
	12	Bits min	For Filter Notch = 1 kHz
Output Noise	See Tables III & IV		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.003	% of FSR max	Filter Notches ≤ 60 Hz
Unipolar Offset Error[2]	See Note 3		
Unipolar Offset Drift[4]	2.5/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.3	μV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Zero Error[2]	See Note 3		
Bipolar Zero Drift[4]	2.5/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.3	μV/°C typ	For Gains of 16, 32, 64, 128
Positive Full-Scale Error[2, 5]	See Note 3		
Full-Scale Drift[4, 6]	3/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.35	μV/°C typ	For Gains of 16, 32, 64, 128
Gain Error[2, 7]	See Note 3		
Gain Drift[4, 8]	2	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error[2]	±0.003	% of FSR max	Typically ±0.0004%
Bipolar Negative Full-Scale Drift[4]	4/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.5	μV/°C typ	For Gains of 16, 32, 64, 128
ANALOG INPUTS/REFERENCE INPUTS			
Common-Mode Rejection (CMR)	94	dB min	At DC. See Table VI
Absolute Common-Mode Range[6]	AGND to AV_{DD}	V min to V max	
Absolute Common-Mode Range[6]	AGND + 50 mV to AV_{DD} – 1.5 V	V min to V max	Analog Input with BUFFER = 1
Normal-Mode 50 Hz Rejection[7]	100	dB min	For Filter Notches of 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Normal-Mode 60 Hz Rejection[7]	100	dB min	For Filter Notches of 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode 50 Hz Rejection[7]	150	dB min	For Filter Notches of 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Common-Mode 60 Hz Rejection[7]	150	dB min	For Filter Notches of 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
Input Current[7]	1	nA max	BUFFER = 1
DC Input Leakage Current[7]			BUFFER = 0
@ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[7]	10	pF max	
Analog Inputs[8]			
Input Voltage Range[9]	0 to +V_{REF}/GAIN[13]	nom	Unipolar Input Range (B/U Bit of Filter High Register = 1)
	±V_{REF}/GAIN	nom	Bipolar Input Range (B/U Bit of Filter High Register = 0)
Input Sampling Rate, f_S	GAIN × $f_{CLK\ IN}$/128		For Gains of 1, 2, 4
	$f_{CLK\ IN}$/16		For Gains of 8, 16, 32, 64, 128
Reference Inputs			
REF IN(+) – REF IN(–) Voltage	+1.25	V nom	±5% for Specified Performance. Part Functions with Lower V_{REF} Voltages
Input Sampling Rate, f_S	$f_{CLK\ IN}$/128		
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.4	V max	
V_{INH}, Input High Voltage	2.5	V min	
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.2	V max	I_{SINK} = 800 μA
V_{OH}, Output High Voltage	DV_{DD} – 0.4	V min	I_{SOURCE} = 200 μA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[11]	9	pF typ	

PRELIMINARY TECHNICAL DATA

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Parameter	A, S Versions	Units	Conditions/Comments
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[15]	$(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[15]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[16]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[16]	$0.8 \times V_{REF}/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(2.1 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage (AD7714-3)	+2.7 to +3.6	V nom	For Specified Performance
AV_{DD} Voltage (AD7714-5)	+5	V nom	±5% for Specified Performance
DV_{DD} Voltage	+2.7 to +5.25	V nom	For Specified Performance
Power Supply Currents			
AV_{DD} Current			AV_{DD} = 3 V or 5 V. BST Bit of Filter High Register = 0[17]
	0.3	mA max	Typically 0.2 mA. BUFFER = 0 V. $f_{CLK\ IN}$ = 1 MHz or 2.4576 MHz
	0.6	mA max	Typically 0.4 mA. BUFFER = +5 V. $f_{CLK\ IN}$ = 1 MHz or 2.4576 MHz
			AV_{DD} = 3 V or 5 V. BST Bit of Filter High Register = 1[17]
	0.5	mA max	Typically 0.3 mA. BUFFER = 0 V. $f_{CLK\ IN}$ = 2.4576 MHz
	1	mA max	Typically 0.8 mA. BUFFER = +5 V. $f_{CLK\ IN}$ = 2.4576 MHz
DV_{DD} Current			Digital I/Ps = 0 V or DV_{DD}
	0.2	mA max	Typically 0.15 mA. DV_{DD} = 3 V. $f_{CLK\ IN}$ = 1 MHz
	0.4	mA max	Typically 0.3 mA. DV_{DD} = 5 V. $f_{CLK\ IN}$ = 1 MHz
	0.5	mA max	Typically 0.4 mA. DV_{DD} = 3 V. $f_{CLK\ IN}$ = 2.4576 MHz
	1	mA max	Typically 0.8 mA. DV_{DD} = 5 V. $f_{CLK\ IN}$ = 2.4576 MHz
Power Supply Rejection[18] (AVDD)	See Note 19	dB typ	
Normal Mode Power Dissipation			AV_{DD} = DV_{DD} = +3 V. Digital I/Ps = 0 V or DV_{DD}. BST Bit = 0
	1.5	mW max	Typically 1 mW. BUFFER = 0 V. $f_{CLK\ IN}$ = 1 MHz
	2.4	mW max	Typically 1.6 mW. BUFFER = +5 V. $f_{CLK\ IN}$ = 1 MHz
	3	mW max	Typically 2.1 mW. BUFFER = 0 V. $f_{CLK\ IN}$ = 2.4576 MHz
	4.5	mW max	Typically 3.6 mW. BUFFER = +5 V. $f_{CLK\ IN}$ = 2.4576 MHz
Normal Mode Power Dissipation			AV_{DD} = DV_{DD} = +5 V. Digital I/Ps = 0 V or DV_{DD}. BST Bit = 0
	3.5	mW max	Typically 2.5 mW. BUFFER = 0 V. $f_{CLK\ IN}$ = 1 MHz
	5	mW max	Typically 3.5 mW. BUFFER = +5 V. $f_{CLK\ IN}$ = 1 MHz
	7.5	mW max	Typically 5.5 mW. BUFFER = 0 V. $f_{CLK\ IN}$ = 2.4576 MHz
	10	mW max	Typically 8 mW. BUFFER = +5 V. $f_{CLK\ IN}$ = 2.4576 MHz
Standby (Power-Down) Dissipation	100	µW max	Typically 50 µW

NOTES

[1]Temperature ranges are as follows: A Version: –40°C to +85°C; S Version: –55°C to +125°C.

[2]Applies after calibration at the temperature of interest.

[3]These errors will be of the order of the output noise of the part as shown in Tables I to IV.

[4]Recalibration at any temperature will remove these drift errors.

[5]Positive Full-Scale Error includes Zero-Scale Errors (Unipolar Offset Error or Bipolar Zero Error) and applies to both unipolar and bipolar input ranges.

[6]Full-Scale Drift includes Zero-Scale Drift (Unipolar Offset Drift or Bipolar Zero Drift) and applies to both unipolar and bipolar input ranges.

[7]Gain Error does not include Zero-Scale Errors. It is calculated as Full-Scale Error—Unipolar Offset Error for unipolar ranges and Full-Scale Error—Bipolar Zero Error for bipolar ranges.

[8]Gain Drift does not include Unipolar Offset Drift/Bipolar Zero Drift. It is effectively the drift of the part if zero-scale calibrations only were performed as is the case with background calibration for gains of 64 and 128.

[9]This Common-Mode voltage range is allowed provided that the input voltage on the differential inputs does not go more positive than AV_{DD} + 30 mV or go more negative than AGND – 30 mV. The common-mode mode voltage applies to those inputs which form differential pairs (see Table VI).

[10]These numbers are guaranteed by design and/or characterization.

[11]The analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance depends on the selected gain.

[12]The analog input voltage range on the analog inputs is given here with respect to the voltage on the respective negative input of its differential or pseudo-differential pair (see Table V). The absolute voltage on the analog inputs should not go more positive than AV_{DD} + 30 mV or go more negative than AGND – 30 mV.

[13]V_{REF} = REF IN(+) – REF IN(–).

[14]Sample tested at +25°C to ensure compliance.

[15]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale, then the device will output all 0s.

[16]These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed AV_{DD} + 30 mV or go more negative than AGND – 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

[17]For higher gains (≥8) at $f_{CLK\ IN}$ = 2.4576 MHz, the BST bit of the Filter High Register must be set to 1. For other conditions, it can be set to 0.

[18]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 5, 10, 25 or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 6, 10, 30 or 60 Hz.

[19]PSRR depends on gain: Gain of 1: 70 dB typ; Gain of 2: 75 dB typ; Gain of 4: 80 dB typ; Gains of 8 to 128: 85 dB typ.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL

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TIMING CHARACTERISTICS[1, 2] (DV_{DD} = +3 V to +5 V, ± 5%; AV_{DD} = +3 V or +5 V, ± 5%; AGND = DGND = 0 V; f_{CLKIN} = 2.5 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	Master Clock Frequency: Crystal Oscillator or Externally Supplied
	2.5	MHz max	For Specified Performance
$t_{CLK\ IN\ LO}$	0.4 × $t_{CLK\ IN}$	ns min	Master Clock Input Low Time. $t_{CLK\ IN}$ = 1/$f_{CLK\ IN}$
$t_{CLK\ IN\ HI}$	0.4 × $t_{CLK\ IN}$	ns min	Master Clock Input High Time
t_r[5]	50	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	50	ns max	Digital Output Fall Time. Typically 20 ns
t_{DRDY}	500 × $t_{CLK\ IN}$	ns nom	$\overline{DRDY}$ High Time
t_1	1000	ns min	$\overline{SYNC}$ Pulse Width
t_2	1000	ns min	$\overline{RESET}$ Pulse Width
Read Operation			
t_3	0	ns min	$\overline{DRDY}$ to $\overline{CS}$ Setup Time
t_4	20	ns min	$\overline{CS}$ Falling Edge to SCLK Falling Edge (POL = 1) or SCLK Rising Edge (POL = 0) Setup Time
t_5[6]	0	ns min	SCLK Active Edge to Data Valid Delay[7]
	20	ns max	DV_{DD} = +5 V
	40	ns max	DV_{DD} = +3 V
t_6	200	ns min	SCLK High Pulse Width
t_7	200	ns min	SCLK Low Pulse Width
t_8	20	ns min	$\overline{CS}$ Rising Edge to SCLK Rising Edge (POL = 1) or SCLK Falling Edge (POL = 0) Hold Time
t_9[8]	10	ns min	Bus Relinquish Time after SCLK Rising Edge (POL = 1) or
	50	ns max	SCLK Falling Edge (POL = 0). DV_{DD} = +5 V
	100	ns max	SCLK Falling Edge (POL = 0). DV_{DD} = +3 V
t_{10}	50	ns max	SCLK Rising Edge (POL = 1) or SCLK Falling Edge (POL = 0) to $\overline{DRDY}$ High[9]
Write Operation			
t_{11}	20	ns min	$\overline{CS}$ Falling Edge to SCLK Falling Edge (POL = 1) or SCLK Rising Edge (POL = 0) Setup Time
t_{12}	30	ns min	Data Valid to SCLK Active Edge Setup Time[6]
t_{13}	20	ns min	Data Valid to SCLK Active Edge Hold Time[6]
t_{14}	200	ns min	SCLK High Pulse Width
t_{15}	200	ns min	SCLK Low Pulse Width
t_{16}	20	ns min	$\overline{CS}$ Rising Edge to SCLK Rising Edge (POL = 1) or SCLK Falling Edge (POL = 0) Hold Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.

[2]See Figures 2 and 3.

[3]CLKIN Duty Cycle range is 45% to 55%. CLKIN must be supplied whenever the AD7714 is not in standby mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7714 is production tested with f_{CLKIN} at 2.5 MHz (1 MHz for some I_{DD} tests). It is guaranteed by characterization to operate at 400 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

[7]SCLK active edge is falling edge of SCLK with POL = 1; SCLK active edge is rising edge of SCLK with POL = 0.

[8]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 100 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

[9]$\overline{DRDY}$ returns high after the first read from the device after an output update. The same data can be read again, if required, while $\overline{DRDY}$ is high although care should be taken that subsequent reads do not occur close to the next output update.

PRELIMINARY TECHNICAL DATA

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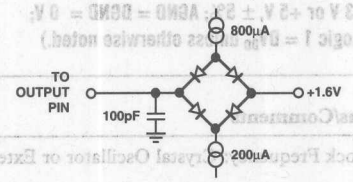


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

ORDERING GUIDE

Model	AV_{DD} Supply	Temperature Range	Package Option*
AD7714AN-5	5 V	–40°C to +85°C	N-24
AD7714AR-5	5 V	–40°C to +85°C	R-24
AD7714ARS-5	5 V	–40°C to +85°C	RS-28
AD7714SQ-5	5 V	–55°C to +125°C	Q-24
AD7714AN-3	3 V	–40°C to +85°C	N-24
AD7714AR-3	3 V	–40°C to +85°C	R-24
AD7714ARS-3	3 V	–40°C to +85°C	RS-28
AD7714SQ	3 V & 5 V	–55°C to +125°C	Q-24

*N = Plastic DIP; R = SOIC; RS = SSOP; Q = Cerdip. For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
AV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND ..... –0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND ... –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND ... –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
  Commercial (A Version) ..... –40°C to +85°C
  Extended (S Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 105°C/W
  Lead Temperature (Soldering, 10 sec) ..... +260°C
Cerdip Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 70°C/W
  Lead Temperature (Soldering, 10 sec) ..... +300°C
SOIC Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C
Power Dissipation (Any Package) to +75°C ..... 450 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

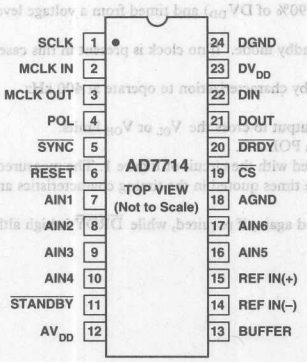
PRELIMINARY TECHNICAL DATA

CAUTION

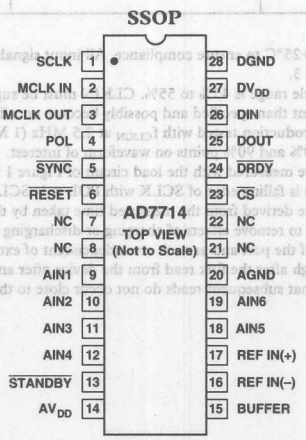
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7714 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

DIP & SOIC



SSOP



NC = NO CONNECT

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PIN FUNCTION DESCRIPTION

DIP/SOIC PIN NUMBERS

Pin No.	Mnemonic	Function
1	SCLK	Serial Clock. Logic Input. An external serial clock is applied to this input to access serial data from the AD7714. This serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7714 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal or external clock. A crystal can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The clock input frequency is nominally either 2.5 MHz or 1 MHz.
3	MCLK OUT	When the master clock for the device is a crystal, the crystal is connected between MCLK IN and MCLK OUT.
4	POL	Clock Polarity. Logic Input. With this input low, the first transition of the serial clock in a data transfer operation is from a low to a high. In microcontroller applications this means that the serial clock should idle low between data transfers. With this input high, the first transition of the serial clock in a data transfer operation is from a high to a low. In microcontroller applications, this means that the serial clock should idle high between data transfers.
5	$\overline{\text{SYNC}}$	Logic Input which allows for synchronization of the digital filters and analog modulators when using a number of AD7714s. While $\overline{\text{SYNC}}$ is low, the nodes of the digital filter, the filter control logic and the calibration control logic are reset and the analog modulator is also held in its reset state.
6	$\overline{\text{RESET}}$	Logic Input. Active low input which resets the control logic, interface logic, digital filter and analog modulator of the part to power-on status.
7	AIN1	Analog Input Channel 1. Programmable-gain analog input which can be used as a pseudo-differential input when used with AIN6 or as the positive input of a differential analog input pair when used with AIN2 (see Communications Register section).
8	AIN2	Analog Input Channel 2. Programmable-gain analog input which can be used as a pseudo-differential input when used with AIN6 or as the negative input of a differential analog input pair when used with AIN1 (see Communications Register section).
9	AIN3	Analog Input Channel 3. Programmable-gain analog input which can be used as a pseudo-differential input when used with AIN6 or as the positive input of a differential analog input pair when used with AIN4 (see Communications Register section).
10	AIN4	Analog Input Channel 4. Programmable-gain analog input which can be used as a pseudo-differential input when used with AIN6 or as the negative input of a differential analog input pair when used with AIN3 (see Communications Register section).
11	$\overline{\text{STANDBY}}$	Logic Input. Taking this pin low shuts down the analog and digital circuitry, reducing power consumption to typically 50 μW.
12	AV_{DD}	Analog Positive Supply Voltage, +3 V nominal (AD7714-3) or +5 V nominal (AD7714-5).
13	BUFFER	Buffer Option Select. Logic Input. With this input low, the on-chip buffer on the analog input (after the multiplexer and before the analog modulator) is shorted out. With the buffer shorted out the current flowing in the AV_{DD} line is reduced to 300 μA ($f_{CLK\ IN}$ = 1 MHz) or 500 μA ($f_{CLK\ IN}$ = 2.5 MHz). With this input high, the on-chip buffer is in series with the analog input allowing the inputs to handle higher source impedances.
14	REF IN(–)	Reference Input. Negative input of the differential reference input to the AD7714. The REF IN(–) can lie anywhere between AV_{DD} and AGND provided REF IN(+) is greater than REF IN(–).
15	REF IN(+)	Reference Input. Positive input of the differential reference input to the AD7714. The reference input is differential with the provision that REF IN(+) must be greater than REF IN(–). REF IN(+) can lie anywhere between AV_{DD} and AGND.
16	AIN5	Analog Input Channel 5. Programmable-gain analog input which is the positive input of a differential analog input pair when used with AIN6 (see Communications Register section).
17	AIN6	Analog Input Channel 6. Reference point for AIN1 through AIN4 in pseudo-differential mode or as the negative input of a differential analog input pair when used with AIN5 (see Communications Register section).
18	AGND	Ground reference point for analog circuitry.

PRELIMINARY TECHNICAL DATA

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Pin No.	Mnemonic	Function
19	$\overline{CS}$	Chip Select. Active low Logic Input used to select the AD7714. With this input hard-wired low, the AD7714 can operate in its three-wire interface mode with SCLK, DIN and DOUT used to interface to the device. $\overline{CS}$ can be used to select the device in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the AD7714.
20	$\overline{DRDY}$	Logic output. A logic low on this output indicates that a new output word is available from the AD7714 data register. The $\overline{DRDY}$ pin will return high upon completion of a read operation of a full output word. If no data read has taken place, after an output update, the $\overline{DRDY}$ line will return high for $500 \times t_{CLK\ IN}$ cycles prior to he next output update. This gives an indication of when a read operation should not be attempted to avoid reading from the data register as it is being updated. $\overline{DRDY}$ is also used to indicate when the AD7714 has completed its on-chip calibration sequence.
21	DOUT	Serial Data Output with serial data being read from the output shift register on the part. This output shift register can contain information from the calibration registers, mode register, communications register, filter selection registers or data register depending on the register selection bits of the Communications Register.
22	DIN	Serial Data Input with serial data being written to the input shift register on the part. Data from this input shift register is transferred to the calibration registers, mode register, communications register or filter selection registers depending on the register selection bits of the Communications Register.
23	DV_{DD}	Digital Supply Voltage, +3 V or +5 V nominal.
24	DGND	Ground reference point for digital circuitry.

TERMINOLOGY*

INTEGRAL NONLINEARITY

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero-scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and Full-Scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

POSITIVE FULL-SCALE ERROR

Positive Full-Scale Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal AIN(+) voltage (AIN(–) + V_{REF}/GAIN – 3/2 LSBs). It applies to both unipolar and bipolar analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(–) + 0.5 LSB) when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal AIN(+) voltage (AIN(–) – 0.5 LSB) when operating in the bipolar mode.

GAIN ERROR

This is a measure of the span error of the ADC. It includes full-scale errors but not zero-scale errors. For unipolar input ranges it is defined as (full-scale error–unipolar offset error) while for bipolar input ranges it is defined as (full-scale error–bipolar zero error).

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(–) – V_{REF}/GAIN + 0.5 LSB), when operating in the bipolar mode.

POSITIVE FULL-SCALE OVERRANGE

Positive Full-Scale Overrange is the amount of overhead available to handle input voltages on AIN(+) input greater than AIN(–) + V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages on AIN(+) below AIN(–) – V_{REF}/GAIN without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks even in the unipolar mode provided that AIN(+) is greater than AIN(–) and greater than AGND – 30 mV.

OFFSET CALIBRATION RANGE

In the system calibration modes, the AD7714 calibrates its offset with respect to the analog input. The Offset Calibration Range specification defines the range of voltages that the AD7714 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7714 can accept in the system calibration mode and still calibrate full-scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7714's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full-scale that the AD7714 can accept and still calibrate gain accurately.

*AIN(–) refers to the negative input of the differential input pairs or to AIN6 when referring to the pseudo-differential input configurations

PRELIMINARY TECHNICAL DATA

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AD7714-5 Output Noise

Table I shows the output rms noise and effective resolution for some typical notch and –3 dB frequencies for the AD7714-5 with $f_{CLK\ IN}$ = 2.4576 MHz while Table II gives the information for $f_{CLK\ IN}$ = 1 MHz. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V and with BUFFER = 0. These numbers are typical and are generated at an analog input voltage of 0 V. The numbers in brackets in each table are for the effective resolution of the part (rounded to the nearest 0.5 LSB). The effective resolution of the device is defined as the ratio of the output rms noise to the input full-scale (i.e., $2 \times V_{REF}$/GAIN). It should be noted that it is not calculated using peak-to-peak output noise numbers. Peak-to-peak noise numbers can be up to 6.6 times the rms numbers while effective resolution numbers based on peak-to-peak noise can be 2.5 bits below the effective resolution based on rms noise as quoted in the tables.

The output noise from the part comes from two sources. The first is the electrical noise in the semiconductor devices used in the implementation of the modulator (device noise). Secondly, when the analog input signal is converted into the digital domain, quantization noise is added. The device noise is at a low level and is largely independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. Consequently, lower filter notch settings (below 100 Hz approximately for $f_{CLK\ IN}$ = 2.4576 MHz and below 40 Hz approximately for $f_{CLK\ IN}$ = 1 MHz) tend to be device noise dominated while higher notch settings are dominated by quantization noise. Changing the filter notch and cutoff frequency in the quantization-noise dominated region results in a more dramatic improvement in noise performance than it does in the device-noise dominated region as shown in Tables I and II. Furthermore, quantization noise is added after the PGA, so effective resolution is largely independent of gain for the higher filter notch frequencies. Meanwhile, device noise is added in the PGA and, therefore, effective resolution reduces at high gains for lower notch frequencies. Additionally, in the device-noise dominated region, the output noise is largely independent of reference voltage while in the quantization-noise dominated region, the noise is proportional to the value of the reference. Noise numbers in the device noise dominated region will be higher than those in the Table I for BUFFER = 1 (at a gain of 128, 10 Hz notch rms noise will be 500 nV). It is possible to do post-filtering on the device to improve the output data rate for a given –3 dB frequency and also to further reduce the output noise.

At the lower filter notch settings (below 60 Hz for $f_{CLK\ IN}$ = 2.4576 MHz and below 25 Hz for $f_{CLK\ IN}$ = 1 MHz), the no missing codes performance of the device is at the 24-bit level. At the higher settings, more codes will be missed until at 1 kHz notch setting for $f_{CLK\ IN}$ = 2.4576 MHz (400 Hz for $f_{CLK\ IN}$ = 1 MHz), no missing codes performance is only guaranteed to the 12-bit level.

PRELIMINARY TECHNICAL DATA

Table I. Output Noise/Effective Resolution vs. Gain and First Notch Frequency for $f_{CLK\ IN}$ = 2.4576 MHz, BUFFER = 0

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in µV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
5 Hz	1.31 Hz	1.2	(22)	0.7	(22)	0.4	(21.5)	0.3	(21)	0.3	(20)	0.3	(19)	0.3	(18)	0.3	(17)
10 Hz	2.62 Hz	1.7	(21.5)	1.0	(21.5)	0.5	(21.5)	0.36	(20.5)	0.33	(20)	0.33	(19)	0.33	(18)	0.33	(17)
25 Hz	6.55 Hz	4.9	(20)	2.2	(20)	1.2	(20)	0.60	(20)	0.36	(19.5)	0.36	(18.5)	0.36	(17.5)	0.36	(16.5)
30 Hz	7.86 Hz	6.1	(19.5)	2.4	(20)	1.2	(20)	0.84	(19.5)	0.5	(19.5)	0.4	(18.5)	0.4	(17.5)	0.4	(16.5)
50 Hz	13.1 Hz	7.5	(19.5)	3.8	(19.5)	2.0	(19.5)	1.0	(19.5)	0.6	(19)	0.5	(18.5)	0.5	(17.5)	0.45	(16.5)
60 Hz	15.72 Hz	8.5	(19)	4.1	(19)	2.1	(19)	1.1	(19)	0.6	(19)	0.5	(18.5)	0.5	(17.5)	0.45	(16.5)
100 Hz	26.2 Hz	13	(18.5)	6.4	(18.5)	3.7	(18.5)	1.8	(18.5)	1.1	(18)	0.9	(17.5)	0.65	(17)	0.65	(16.5)
250 Hz	65.5 Hz	130	(15)	75	(15)	25	(15.5)	12	(15.5)	7.5	(15.5)	4.0	(15.5)	2.7	(15)	1.7	(14.5)
500 Hz	131 Hz	600	(13)	260	(13)	140	(13)	70	(13)	35	(13)	25	(12.5)	15	(12.5)	8	(12.5)
1 kHz	262 Hz	2,850	(11)	1,430	(11)	700	(11)	290	(11)	180	(11)	120	(11)	63	(10.5)	35	(10)

Table II. Output Noise/Effective Resolution vs. Gain and First Notch Frequency for $f_{CLK\ IN}$ = 1 MHz, BUFFER = 0

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in µV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
2 Hz	0.52 Hz	1.2	(22)	0.7	(22)	0.4	(21.5)	0.3	(21)	0.3	(20)	0.3	(19)	0.3	(18)	0.3	(17)
4 Hz	1.05 Hz	1.7	(21.5)	1.0	(21.5)	0.5	(21.5)	0.36	(20.5)	0.33	(20)	0.33	(19)	0.33	(18)	0.33	(17)
10 Hz	2.62 Hz	4.9	(20)	2.2	(20)	1.2	(20)	0.60	(20)	0.36	(19.5)	0.36	(18.5)	0.36	(17.5)	0.36	(16.5)
25 Hz	6.55 Hz	8.5	(19)	4.1	(19)	2.1	(19)	1.1	(19)	0.6	(19)	0.5	(18.5)	0.5	(17.5)	0.45	(16.5)
30 Hz	7.86 Hz	10.2	(19)	4.9	(19)	2.6	(19)	1.3	(19)	0.8	(18.5)	0.65	(18)	0.65	(17)	0.5	(16)
50 Hz	13.1 Hz	22.5	(18)	11.2	(18)	5.6	(18)	2.7	(18)	1.7	(17.5)	1.2	(17)	0.85	(16.5)	0.75	(15.5)
60 Hz	15.72 Hz	31	(17.5)	16	(17.5)	7.6	(17.5)	3.7	(17.5)	2.3	(17)	1.5	(16.5)	1.0	(16)	0.85	(15.5)
100 Hz	26.2 Hz	130	(15)	75	(15)	25	(15.5)	12	(15.5)	7.5	(15.5)	4.0	(15.5)	2.7	(15)	1.7	(14.5)
200 Hz	52.4 Hz	600	(13)	260	(13)	140	(13)	70	(13)	35	(13)	25	(12.5)	15	(12.5)	8	(12.5)
400 Hz	104.8 Hz	2,850	(11)	1,430	(11)	700	(11)	290	(11)	180	(11)	120	(11)	63	(10.5)	35	(10)

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AD7714-3 Output Noise

Table III shows the output rms noise and effective resolution for some typical notch and –3 dB frequencies for the AD7714-3 with $f_{CLK\,IN}$ = 2.4576 MHz while Table IV gives the information for $f_{CLK\,IN}$ = 1 MHz. The numbers given are for the bipolar input ranges with a V_{REF} of +1.25 V and BUFFER = 0. These numbers are typical and are generated at an analog input voltage of 0 V. The numbers in brackets in each table are for the effective resolution of the part (rounded to the nearest 0.5 LSB). The effective resolution of the device is defined as the ratio of the output rms noise to the input full-scale (i.e., $2 \times V_{REF}$/GAIN). It should be noted that it is not calculated using peak-to-peak output noise numbers. Peak-to-peak noise numbers can be up to 6.6 times the rms numbers while effective resolution numbers based on peak-to-peak noise can be 2.5 bits below the effective resolution based on rms noise as quoted in the tables.

The output noise from the part comes from two sources. The first is the electrical noise in the semiconductor devices used in the implementation of the modulator (device noise). Secondly, when the analog input signal is converted into the digital domain, quantization noise is added. The device noise is at a low level and is largely independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. Consequently, lower filter notch settings (below 100 Hz approximately for $f_{CLK\,IN}$ = 2.4576 MHz and below 40 Hz approximately for $f_{CLK\,IN}$ = 1 MHz) tend to be device noise dominated while higher notch settings are dominated by quantization noise. Changing the filter notch and cutoff frequency in the quantization noise dominated region results in a more dramatic improvement in noise performance than it does in the device-noise dominated region as shown in Tables III and IV. Furthermore, quantization noise is added after the PGA, so effective resolution is largely independent of gain for the higher filter notch frequencies. Meanwhile, device noise is added in the PGA and, therefore, effective resolution suffers a little at high gains for lower notch frequencies. Additionally, in the device-noise dominated region, the output noise is largely independent of reference voltage while in the quantization-noise dominated region, the noise is proportional to the value of the reference. Noise numbers in the device noise dominated region will be higher than those in the Table III for BUFFER = 1 (at a gain of 128, 10 Hz notch rms noise will be 500 nV). It is possible to do post-filtering on the device to improve the output data rate for a given –3 dB frequency and also to further reduce the output noise (see Digital Filtering section).

At the lower filter notch settings (below 60 Hz for $f_{CLK\,IN}$ = 2.4576 MHz and below 25 Hz for $f_{CLK\,IN}$ = 1 MHz), the no missing codes performance of the device is at the 24-bit level. At the higher settings, more codes will be missed until at 1 kHz notch setting for $f_{CLK\,IN}$ = 2.4576 MHz (400 Hz for $f_{CLK\,IN}$ = 1 MHz), no missing codes performance is only guaranteed to the 12-bit level.

PRELIMINARY TECHNICAL DATA

Table III. Output Noise/Effective Resolution vs. Gain and First Notch Frequency for $f_{CLK\,IN}$ = 2.4576 MHz, BUFFER = 0

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in µV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
5 Hz	1.31 Hz	1.2	(21)	0.7	(21)	0.4	(20.5)	0.3	(20)	0.3	(19)	0.3	(18)	0.3	(17)	0.3	(16)
10 Hz	2.62 Hz	1.7	(20.5)	1.0	(20.5)	0.5	(20.5)	0.36	(19.5)	0.33	(19)	0.33	(18)	0.33	(17)	0.33	(16)
25 Hz	6.55 Hz	4.9	(19)	2.2	(19)	1.2	(19)	0.60	(19)	0.36	(18.5)	0.36	(17.5)	0.36	(16.5)	0.36	(15.5)
30 Hz	7.86 Hz	5.6	(19)	2.4	(19)	1.2	(19)	0.84	(18.5)	0.5	(18.5)	0.4	(17.5)	0.4	(16.5)	0.4	(15.5)
50 Hz	13.1 Hz	7.5	(18.5)	3.8	(18.5)	2.0	(18.5)	1.0	(18.5)	0.6	(18)	0.5	(17.5)	0.5	(16.5)	0.45	(15.5)
60 Hz	15.72 Hz	8.5	(18)	4.1	(18)	2.1	(18)	1.1	(18)	0.6	(18)	0.5	(17.5)	0.5	(16.5)	0.45	(15.5)
100 Hz	26.2 Hz	13	(17.5)	6.4	(17.5)	2.9	(17.5)	1.5	(17.5)	1.1	(17)	0.7	(17)	0.65	(16)	0.65	(15)
250 Hz	65.5 Hz	53	(15.5)	28	(15.5)	12	(15.5)	8.6	(15)	3.9	(15)	3.7	(14)	1.9	(14)	1.4	(14)
500 Hz	131 Hz	240	(13.5)	150	(13)	80	(13)	35	(13)	22	(13)	14	(12.5)	8.7	(12)	8	(11.5)
1 kHz	262 Hz	1400	(11)	610	(11)	370	(10.5)	230	(10.5)	125	(10.5)	70	(10)	40	(10)	22	(10)

Table IV. Output Noise/Effective Resolution vs. Gain and First Notch Frequency for $f_{CLK\,IN}$ = 1 MHz, BUFFER = 0

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in µV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
2 Hz	0.52 Hz	1.2	(21)	0.7	(21)	0.4	(20.5)	0.3	(20)	0.3	(19)	0.3	(18)	0.3	(17)	0.3	(16)
4 Hz	1.05 Hz	1.7	(20.5)	1.0	(20.5)	0.5	(20.5)	0.36	(19.5)	0.33	(19)	0.33	(18)	0.33	(17)	0.33	(16)
10 Hz	2.62 Hz	4.9	(19)	2.2	(19)	1.2	(19)	0.60	(19)	0.36	(18.5)	0.36	(17.5)	0.36	(16.5)	0.36	(15.5)
25 Hz	6.55 Hz	7.8	(18.5)	4.1	(18)	2.1	(18)	1.1	(18)	0.6	(18)	0.5	(17.5)	0.5	(16.5)	0.45	(15.5)
30 Hz	7.86 Hz	10.2	(18)	4.9	(18)	2.1	(18)	1.1	(18)	0.8	(17.5)	0.65	(17)	0.65	(16)	0.5	(15)
50 Hz	13.1 Hz	22.5	(17)	11.2	(17)	4.4	(17)	2.3	(17)	1.7	(16.5)	1.2	(16)	0.85	(15.5)	0.75	(14.5)
60 Hz	15.72 Hz	31	(16.5)	16	(16.5)	6.0	(16.5)	3.2	(16.5)	2.3	(16)	1.5	(15.5)	1.0	(15)	0.85	(14.5)
100 Hz	26.2 Hz	53	(15.5)	28	(15.5)	12	(15.5)	8.6	(15)	3.9	(15)	3.7	(14)	1.9	(14)	1.4	(14)
200 Hz	52.4 Hz	240	(13.5)	150	(13)	80	(13)	35	(13)	22	(13)	14	(12.5)	8.7	(12)	8	(11.5)
400 Hz	104.8 Hz	1400	(11)	610	(11)	370	(10.5)	230	(10.5)	125	(10.5)	70	(10)	40	(10)	22	(10)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

On-Chip Registers

The AD7714 contains eight on-chip registers which can be accessed via the serial port of the part. The first of these is a Communications Register which controls the channel selection, decides whether the next operation is a read or write operation and also decides which register the next read or write operation accesses. The $\overline{DRDY}$ status is also available by reading from the Communications Register. The second register is a Mode Register which determines calibration mode and gain setting. The third register is labelled the Filter High Register and this determines the word length, bipolar/unipolar operation and contains the upper 4 bits of the filter selection word. The fourth register is labelled the Filter Low Register and contains the lower 8 bits of the filter selection word. The fifth register is a Test Register which is accessed when testing the device. The sixth register is the Data Register from which the output data from the part is accessed. The final two registers are calibration registers; one is the Calibration Zero-Scale Register and the other is the Calibration Full-Scale Register. The registers are discussed in more detail in the following sections.

Communications Register (RS2–RS0 = 0, 0, 0)

The Communications Register is an eight bit register from which data can either be read or to which data can be written. On power-up or after a $\overline{RESET}$, the AD7714 is waiting for a write operation to the Communications Register. This is the default state of the interface, and in situations where the interface sequence is lost, if enough writes to the device (at least four bytes) take place with DIN high, the AD7714 returns to its default state. Table V outlines the bit designations for the Communications Register.

Table V. Communications Register

0/$\overline{DRDY}$	RS2	RS1	RS0	R/$\overline{W}$	CH2	CH1	CH0

0/$\overline{DRDY}$

For a read operation, this bit provides the status of the $\overline{DRDY}$ flag from the part. The status of this bit is the same as the $\overline{DRDY}$ output pin. For a write operation, a 0 must be written to this bit so that the write operation will be recognized by the register. If a 1 is written to this bit, the part will not clock on to subsequent bits in the register.

RS2–RS0

Register Selection Bits. RS2 is the MSB of the three selection bits. The three bits select to which one of eight on-chip registers the next read or write operation takes place as follows:

RS2	RS1	RS0	Register	Register Size
0	0	0	Communications Register	8 Bits
0	0	1	Mode Register	8 Bits
0	1	0	Filter High Register	8 Bits
0	1	1	Filter Low Register	8 Bits
1	0	0	Test Register	8 Bits
1	0	1	Data Register	16 Bits or 24 Bits
1	1	0	Calibration Zero-Scale Register	24 Bits
1	1	1	Calibration Full-Scale Register	24 Bits

R/$\overline{W}$

Read/Write Select. This bit selects whether the next operation is a read or write operation to the selected register. A 0 indicates a write cycle for the next operation to the appropriate register, while a 1 indicates a read operation from the appropriate register.

CH2–CH0

Channel Select. These three bits select a channel for either conversion or for access to calibration coefficients as outlined in Table VI. There are three pairs of calibration registers on the part with some of the input channel combinations sharing calibration registers. With CH2, CH1 and CH0 at a logic 1, the part internally looks at shorted AIN6 inputs. This can be used as a test method to evaluate the noise performance of the part. The power-on or RESET status of these bits is 1, 0, 0 selecting the differential pair AIN1 and AIN2.

Table VI. Channel Selection

CH2	CH1	CH0	AIN(+)	AIN(–)	Type	Calibration Register Pair
0	0	0	AIN1	AIN6	Pseudo Differential	Register Pair 0
0	0	1	AIN2	AIN6	Pseudo Differential	Register Pair 1
0	1	0	AIN3	AIN6	Pseudo Differential	Register Pair 2
0	1	1	AIN4	AIN6	Pseudo Differential	Register Pair 2
1	0	0	AIN1	AIN2	Fully Differential	Register Pair 0
1	0	1	AIN3	AIN4	Fully Differential	Register Pair 1
1	1	0	AIN5	AIN6	Fully Differential	Register Pair 2
1	1	1	AIN6	AIN6	Test Mode	Register Pair 2

PRELIMINARY TECHNICAL DATA

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Mode Register (RS2-RS0 = 0, 0, 1); Power On/Reset Status: 00 Hex

The Mode Register is an eight bit register from which data can either be read or to which data can be written. Table VII outlines the bit designations for the Mode Register.

Table VII. Mode Register

MD2	MD1	MD0	G2	G1	G0	BO	FSYNC

MD2	MD1	MD0	Operating Mode
0	0	0	Normal Mode; this is the normal mode of operation of the device whereby the device is performing normal conversions. This is the default condition of these bits after Power-On or RESET.
0	0	1	Self-Calibration; this activates self-calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. This is a one step calibration sequence and when complete the part returns to Normal Mode. The $\overline{DRDY}$ output or bit indicates when this self-calibration is complete and when a new valid word is available in the data register. For this calibration type, the zero-scale calibration is done internally on shorted (zeroed) inputs and the full-scale calibration is done internally on V_{REF}.
0	1	0	Zero-Scale System Calibration; this activates zero-scale system calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. Calibration is performed on the analog input voltage provided at the analog input during this calibration sequence. The $\overline{DRDY}$ output or bit indicates when this zero-scale calibration is complete and the part returns to Normal Mode.
0	1	1	Full-Scale System Calibration; this activates full-scale system calibration on the selected input channel. Calibration is performed on the analog input voltage provided at the analog input during this calibration sequence. Once again, $\overline{DRDY}$ indicates when this full-scale calibration is complete. When this calibration is complete, the part returns to Normal Mode.
1	0	0	System-Offset Calibration; this activates system-offset calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. This is a one step calibration sequence and when complete the part returns to Normal Mode with $\overline{DRDY}$ indicating when this system offset calibration is complete. For this calibration type, the zero-scale calibration is done on the selected input channel and the full-scale calibration is done internally on V_{REF}.
1	0	1	Background Calibration; this activates background calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. If the background calibration mode is on, the AD7714 provides continuous self-calibration of the shorted (zeroed) inputs. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the offset of the device when there is a change in the ambient temperature or supplies. In this mode, the shorted (zeroed) inputs, as well as the analog input voltage, are continuously monitored and the calibration registers of the device are automatically updated. Because the background calibration does not perform full-scale calibrations, a full-scale self-calibration should be performed before placing the part in background calibration mode.
1	1	0	Zero-Scale Self-Calibration; this activates zero-scale self-calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. This zero-scale calibration is done internally on shorted (zeroed) inputs. This is a one step calibration sequence and when complete the part returns to Normal Mode. The $\overline{DRDY}$ output or bit indicates when this zero-scale self-calibration is complete.
1	1	1	Full-Scale Self-Calibration; this activates full-scale self-calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. This full-scale calibration is done internally on V_{REF}. This is a one step calibration sequence and when complete the part returns to Normal Mode. The $\overline{DRDY}$ output indicates when this full-scale self-calibration is complete.

G2	G1	G0	Gain Setting
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

BO — Burn Out Current. A 0 in this bit turns off the on-chip burn out currents. This is the default (Power-On or RESET) status of this bit. A 1 in this bit activates the burn out currents.

FSYNC — Filter Synchronization. When this bit is high, the nodes of the digital filter, the filter control logic and the calibration control logic are reset, and the analog modulator is also held in its reset state. When this bit goes low, valid data is available in 3 × 1/(output update rate), i.e., the settling time of the filter.

PRELIMINARY TECHNICAL

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Filter Registers. Power On/Reset Status: Filter High Register: 01 Hex. Filter Low Register: 40 Hex

There are two 8-bit Filter Registers on the AD7714 from which data can either be read or to which data can be written. Tables VIII and IX outline the bit designations for the Filter Registers.

Table VIII. Filter High Register (RS2–RS0 = 0, 1, 0)

$\overline{B}$/U	WL	BST	0	FS11	FS10	FS9	FS8

Table IX. Filter Low Register (RS2–RS0 = 0, 1, 1)

FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

$\overline{B}$/U	Bipolar/Unipolar Operation. A 0 in this bit selects Bipolar Operation. This is the default (Power-On or $\overline{RESET}$) status of this bit. A 1 in this bit selects unipolar operation.
WL	Word Length. A 0 in this bit selects 16-bit word length when reading from the data register (i.e., $\overline{DRDY}$ returns high after 16 serial clock cycles). This is the default (Power-On or RESET) status of this bit. A 1 in this bit selects 24-bit word length.
BST	Current Boost. A 0 in this bit reduces the current taken by the analog front-end. When the part is operated with $f_{CLK\ IN}$ = 1 MHz, this bit should be 0 to reduce the current drawn from AV_{DD}. When the AD7714 is operated from $f_{CLK\ IN}$ = 2.4576 MHz with gains of 8 to 128, this bit needs to be 1 to ensure correct operation of the device. The Power-On or $\overline{RESET}$ status of this bit is 0.
0	To ensure correct operation of the part, a 0 must be written to this bit.
FS11–FS0	Filter Selection. The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$) filter response. The 12-bits of data programmed into these bits determine the filter cut-off frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device. The first notch of the filter occurs at a frequency determined by the relationship: *filter first notch frequency = ($f_{CLK\ IN}$/128)/code* where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 4,000. With the nominal $f_{CLK\ IN}$ of 2.4576 MHz, this results in a first notch frequency range from 4.8 Hz to 1.01 kHz. To ensure correct operation of the AD7714, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device. Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I through IV show the effect of the filter notch frequency and gain on the effective resolution of the AD7714. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1 kHz, a new word is available every 1 ms. The settling-time of the filter to a full-scale step input change is worst case 4 × 1/(output data rate). For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. If the first notch is at 1 kHz, the settling time of the filter to a full-scale input step is 4 ms max. This settling-time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with the $\overline{SYNC}$ input low or the FSYNC bit high, the settling-time time will be 3 × 1/(output data rate) from when $\overline{SYNC}$ returns high or FSYNC returns low. If a change of channel takes place, the settling-time is 3 × 1/(output data rate) regardless of the $\overline{SYNC}$ or FSYNC status as the part issues an internal SYNC command when requested to change channels. The –3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter –3 dB frequency = 0.262 × first notch frequency.

Test Register (RS2–RS0 = 1, 0 , 0)

The part contains a Test Register which is used in testing the device. The user is advised not to change the status of any of the bits in this register from the default (Power-On or RESET) status of all 0s as the part will be placed in one of its test modes and will not operate correctly. If the part enters one of its test modes, exercising $\overline{RESET}$ will exit the part from the mode.

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Calibration Zero-Scale Register (RS2–RS0 = 1, 1, 0)

The AD7714 contains 3 zero-scale calibration registers, labelled Register 0 to Register 2. Each of these registers is a 24-bit read/write register and 24 bits must be written; otherwise no data will be transferred to the register. The register is used in conjunction with the associated full-scale calibration register to form a register pair. These register pairs are associated with input channel pairs as outlined in Table VI.

There is a possibility that after accessing the calibration registers (either read or write operation), the first output data read from the part contain incorrect data. In addition, a read or write operation to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking either the $\overline{\text{SYNC}}$ input low or the FSYNC bit of the Mode Register high before the calibration register operation and taking them either high or low respectively after the operation is complete.

Calibration Full-Scale Register (RS2–RS0 = 1, 1, 1)

The AD7714 contains 3 full-scale calibration registers, labelled Register 0 to Register 2. Each of these registers is a 24-bit read/write register and 24 bits must be written, otherwise no data will be transferred to the register. The register is used in conjunction with the associated zero scale calibration register to form a register pair. These register pairs are associated with input channel pairs as outlined in Table VI.

There is a possibility that after accessing the calibration registers (either read or write operation), the first output data read from the part will contain incorrect data. In addition, a read or write operation to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking either the $\overline{\text{SYNC}}$ input low or the FSYNC bit of the Mode Register high before the calibration register operation and taking them either high or low respectively after the operation is complete.

CIRCUIT DESCRIPTION

The AD7714 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, industrial control or process control applications. It contains a sigma-delta (or charge-balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bidirectional serial communications port. The part consumes only 500 μA of power supply current, making it ideal for battery-powered or loop-powered instruments. The part comes in two versions, the AD7714-5 which is specified for operation from a +5 V analog supply (AV_{DD}) and the AD7714-3 which is specified for operation from a +3 V analog supply. The AD7714-5 can be operated with a digital supply (DV_{DD}) voltage of +3 V or +5 V.

The part contains three programmable-gain fully differential analog input channels which can be reconfigured as five pseudo-differential inputs. The gain range on all channels is from 1 to 128 allowing the part to accept unipolar signals of between 0 mV to +20 mV and 0 V to +2.5 V or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals +2.5 V. With a reference voltage of +1.25 V, the input ranges are from 0 mV to +10 mV to 0 V to +1.25 V in unipolar mode and from ±10 mV to ±1.25 V in bipolar mode.

The input signal to the selected analog input channel is continuously sampled at a rate determined by the frequency of the master clock, MCLK IN, and the selected gain. A charge-balancing A/D converter (Sigma-Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma delta modulator with the input sampling frequency being modified to give the higher gains. A $Sinc^3$ digital low-pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and hence its –3 dB frequency) can be programmed via the filter high and filter low registers. With a master clock frequency of 2.4576 MHz, the programmable range for this first notch frequency is from 4.8 Hz to 1.01 kHz giving a programmable range for the –3 dB frequency of 1.26 Hz to 265 Hz.

The basic connection diagram for the part is shown in Figure 2. This shows both the AV_{DD} and DV_{DD} pins of the AD7714 being driven from the analog +3 V or +5 V supply. Some applications will have AV_{DD} and DV_{DD} driven from separate supplies. In the connection diagram shown, the AD7714's analog inputs are configured as three fully differential inputs. The part is set up for unbuffered mode on the these analog inputs. An AD780, precision +2.5 V reference, provides the reference source for the part. On the digital side, the part is configured for three-wire operation with $\overline{\text{CS}}$ tied to DGND. A quartz crystal or ceramic resonator provides the master clock source for the part.

The AD7714 provides a number of calibration options which can be programmed via the MD2, MD1 and MD0 bits of the Mode Register. A calibration cycle may be initiated at any time by writing to these bits of the Mode Register. The part can perform self-calibration using the on-chip calibration microcontroller and SRAM to store calibration parameters. Other system components may also be included in the calibration loop to remove offset and gain errors in the input channel using the system calibration mode. Another option is a background calibration mode where the part continuously performs internal zero-scale calibrations and updates the calibration coefficients. Using the part in this mode, the user does not have to worry

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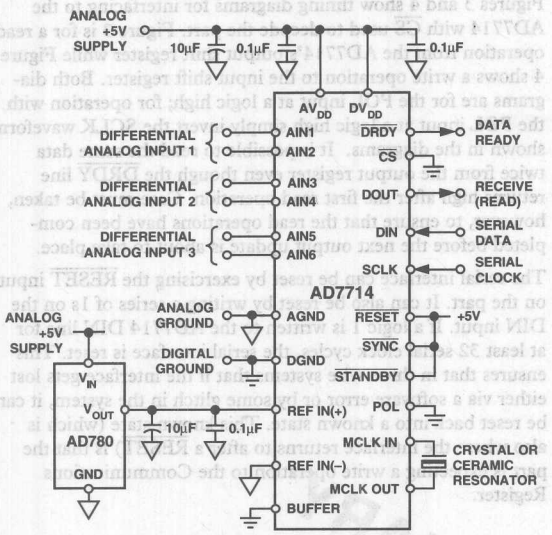

Figure 2. Basic Connection Diagram

about issuing periodic calibration commands to the device or ask the device to recalibrate when there is a change in the ambient temperature or power supply voltage. This automatic removal of offset errors is achieved at the expense of output update rate which is reduced by a factor of six. Using the part in background calibration mode automatically removes offset errors but not full-scale errors. A full-scale self-calibration should be performed before entering the background calibration mode. The residual gain drift in background calibration mode is 2 ppm/°C.

The AD7714 gives the user access to the on-chip calibration registers allowing the microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part from prestored values in E^2PROM. This gives the microprocessor much greater control over the AD7714's calibration procedure. It also means that the user can verify that the device has performed its calibration correctly by comparing the coefficients after calibration with prestored values in E^2PROM. Table X details the calibration options and sequences available on the AD7714. For the table, Sel Gain refers to the selected operating gain.

DIGITAL INTERFACE

The AD7714's serial interface consists of five signals, $\overline{CS}$, SCLK, DIN, DOUT and $\overline{DRDY}$. The DIN line is used for

Table X. Calibration Sequences

Calibration Type	MD2, MD1, MD0	Calibration Sequence	Duration
Self Calibration	0, 0, 1	Internal ZS Cal @ Sel Gain + Internal FS Cal @ Sel Gain	9 × 1/Output Rate
ZS System Calibration	0, 1, 0	ZS Cal on AIN @ Sel Gain	3 × 1/Output Rate
FS System Calibration	0, 1, 1	FS Cal on AIN @ Sel Gain	3 × 1/Output Rate
System-Offset Calibration	1, 0, 0	ZS Cal on AIN @ Sel Gain + Internal FS Cal @ Sel Gain	9 × 1/Output Rate
Background Calibration	1, 0, 1	Internal ZS Cal @ Sel Gain	6 × 1/Output Rate
ZS Self Calibration	1, 1, 0	Internal ZS Cal @ Sel Gain	3 × 1/Output Rate
FS Self Calibration	1, 1, 1	Internal FS Cal @ Sel Gain	3 × 1/Output Rate

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transferring data into the on-chip registers while the DOUT line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on DIN or DOUT) take place with respect to this SCLK signal. The $\overline{DRDY}$ line is used as a status signal to indicate when data is ready to be read from the AD7714's data register. $\overline{DRDY}$ goes low when a new data word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select the device. It can be used to decode the AD7714 in systems where a number of parts are connected to the serial bus.

The AD7714 serial interface can operate in three-wire mode by tying the $\overline{CS}$ input low. In this case, the SCLK, DIN and DOUT lines are used to communicate with the AD7714 and the status of $\overline{DRDY}$ can be obtained by interrogating the MSB of the Communications Register.

Figures 3 and 4 show timing diagrams for interfacing to the AD7714 with $\overline{CS}$ used to decode the part. Figure 3 is for a read operation from the AD7714's output shift register while Figure 4 shows a write operation to the input shift register. Both diagrams are for the POL input at a logic high; for operation with the POL input at a logic high simply invert the SCLK waveform shown in the diagrams. It is possible to read the same data twice from the output register even though the $\overline{DRDY}$ line returns high after the first read operation. Care must be taken, however, to ensure that the read operations have been completed before the next output update is about to take place.

The serial interface can be reset by exercising the $\overline{RESET}$ input on the part. It can also be reset by writing a series of 1s on the DIN input. If a logic 1 is written to the AD7714 DIN line for at least 32 serial clock cycles, the serial interface is reset. This ensures that in three-wire systems that if the interface gets lost either via a software error or by some glitch in the system, it can be reset back into a known state. This known state (which is also where the interface returns to after a $\overline{RESET}$) is that the part is expecting a write operation to the Communications Register.

PRELIMINARY TECHNICAL DATA

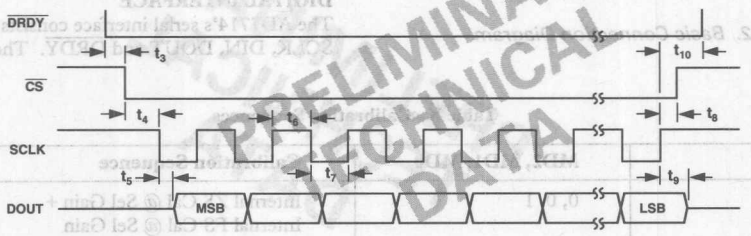

Figure 3. Read Cycle Timing Diagram (POL = 1)

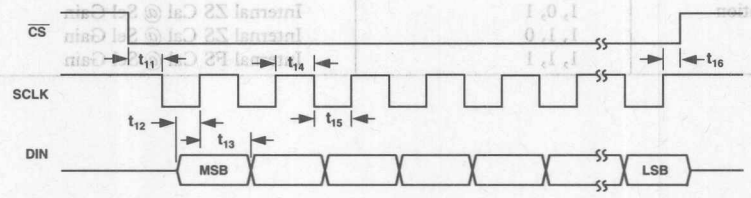

Figure 4. Write Cycle Timing Diagram (POL = 1)

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CMOS 12-Bit, 468 kHz, Sigma-Delta ADC

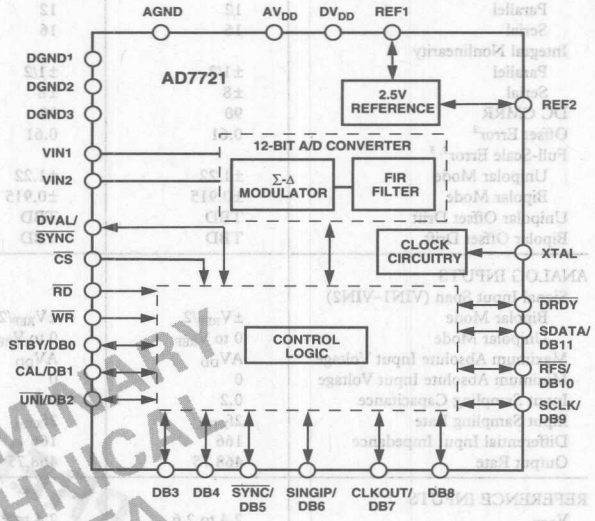
AD7721

FEATURES

12-Bit Sigma-Delta ADC
- **30 MHz Sampling Rate**
- **468.75 kHz Output Word Rate**
- **No Missing Codes**
- **Low-Pass Digital Filter**
- **Linear Phase**

210 kHz Input Bandwidth
On-Chip Voltage Reference
Power Supplies: AV_{DD}, DV_{DD}: +5 V ± 5%
Standby Mode
Flexible High Speed Serial Interface

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7721 is a complete low power, 12-bit, sigma-delta ADC. The part operates from a +5 V supply and accepts a differential input of 0 V to 2.5 V or ±1.25 V. The analog input is continuously sampled by an analog modulator at a 30 MHz rate eliminating the need for external sample-and-hold circuitry. The modulator output is processed by two finite impulse response (FIR) digital filters in series. The on-chip filtering reduces the external antialias requirements to first order in most cases. Settling-time for a step input is 98.74 µs while the group delay for the filter is 49.37 µs.

The AD7721 provides 12-bit performance for input bandwidths up to 210 kHz. The part provides data at an output word rate of 468.75 kHz. The sample rate, filter corner frequency and output word rate are set by an external clock or crystal that is nominally set to 15 MHz.

Use of a single bit DAC in the modulator guarantees excellent linearity and dc accuracy. Endpoint accuracy is ensured by on-chip calibration of offset and gain. This calibration procedure minimizes the part's zero-scale and full-scale errors.

The output data is accessed from the output register through a flexible serial port or a parallel port. This offers easy, high speed interfacing to modern microcontrollers and digital signal processors. The serial interface operates in external clocking (slave) mode. In this mode, an external serial clock and framing pulse must be provided to access the data from the output register.

The part provides an on-chip, accurate 2.5 V reference. A REFIN/REFOUT function is provided that allows either this internal reference or an external system reference to be used as the reference source for the part.

CMOS construction ensures low power dissipation while a power-down mode, initiated by the STBY pin, reduces the idle power consumption to only 100 µW.

ORDERING INFORMATION

Model	Temperature Range	Package Option*
AD7721AN	–40°C to +85°C	N-28
AD7721AR	–40°C to +85°C	R-28
AD7721SQ	–55°C to +125°C	Q-28

*N = Plastic DIP; R = 0.3" Small Outline IC (SOIC); Q = Cerdip. For outline information see Package Information section.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

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Resolution				
Parallel	12	12	Bits	
Serial	16	16	Bits	
Minimum Resolution for Which No Missing Codes is Guaranteed				
Parallel	12	12	Bits min	Guaranteed Monotonic
Serial	16	16	Bits min	Guaranteed Monotonic
Integral Nonlinearity				
Parallel	±1/2	±1/2	LSB max	
Serial	±8	±8	LSB max	
DC CMRR	90	90	dB min	Bipolar Mode
Offset Error[2]	0.61	0.61	mV max	Unipolar Mode
Full-Scale Error[2, 3]				
Unipolar Mode	±1.22	±1.22	mV max	
Bipolar Mode	±0.915	±0.915	mV max	
Unipolar Offset Drift	TBD	TBD		Excluding Reference
Bipolar Offset Drift	TBD	TBD		Excluding Reference
ANALOG INPUTS				
Signal Input Span (VIN1–VIN2)				
Bipolar Mode	$\pm V_{REF}/2$	$\pm V_{REF}/2$	V max	$\overline{UNI} = V_{IH}$
Unipolar Mode	0 to V_{REF}	0 to V_{REF}	V max	$\overline{UNI} = V_{IL}$
Maximum Absolute Input Voltage	AV_{DD}	AV_{DD}	V	
Minimum Absolute Input Voltage	0	0	V	
Input Sampling Capacitance	0.2	0.2	pF typ	
Input Sampling Rate	$2f_{XTAL}$	$2f_{XTAL}$	MHz	Guaranteed by Design
Differential Input Impedance	166	166	kΩ typ	With 15 MHz on XTAL Pin
Output Rate	468.75	468.75	kHz	
REFERENCE INPUTS				
V_{REF}	2.4 to 2.6	2.4 to 2.6	V min/V max	External Reference Applied to REF1 or REF2 Pin for Specified Performance
REF1 Input Current	–10 to +10	–10 to +10	µA typ	External Reference Applied to REF1 Pin
REF2 Input Current	33.75	33.75	µA typ	External Reference Applied to REF2 Pin
REF2 OUTPUT				
REF2 Voltage	2.5 ± 0.125	2.5 ± 0.125	V min/V max	Using Internal Reference
Output Current	±500	±500	µA max	All Reference Modes
DC Load Regulation	1	1	mV/mA	All Reference Modes
DC Line Regulation (AV_{DD})	1	1	mV/V max	Using Internal Reference
Offset Between REF1 and REF2	±5	±5	mV max	External Reference Applied to REF1 Pin
DYNAMIC SPECIFICATIONS				
Dynamic Range	72	72	dB min	
Signal to (Noise + Distortion)	70	70	dB min	Input Bandwidth 0 to 210 kHz
Total Harmonic Distortion	–80	–80	dB max	Input Bandwidth 0 to 210 kHz
Frequency Response				
0 to 210 kHz	±0.05	±0.05	dB max	
259 kHz to 14.741 MHz	–72	–72	dB min	
14.741 MHz to 15.259 MHz	–30	–30	dB min	50% Duty cycle on XTAL1 Pin
15.259 MHz to 29.741 MHz	–72	–72	dB min	
CLOCK				
XTAL1 Mark Space Ratio	45 to 55	45 to 55	% max	For Specified Operation
LOGIC INPUTS				
V_{INH}, Input High Voltage	2.0	2.0	V min	
V_{INL}, Input Low Voltage	0.8	0.8	V max	
I_{INH}, Input Current	10	10	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	4.0	4.0	V min	$\lvert I_{OUT} \rvert \leq 200$ µA
V_{OL}, Output Low Voltage	0.4	0.4	V max	$\lvert I_{OUT} \rvert \leq 1.6$ mA

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Parameter	A Version	S Version	Units	Test Conditions/Comments
POWER SUPPLIES				
AV_{DD}	4.75/5.25	4.75/5.25	V min/V max	
DV_{DD}	4.75/5.25	4.75/5.25	V min/V max	
I_{DD} (Total from AV_{DD}, DV_{DD})	70	80	mA max	
Power Consumption	350	400	mW max	STBY = 0 V
Power Consumption	100	100	µW max	STBY = +5 V

NOTES
[1]Operating temperature range is as follows: A Version: –40°C to +85°C; S Version: –55°C to +125°C.
[2]Applies after calibration at temperature of interest.
[3]Full-scale error applies to both positive and negative full-scale error. It excludes reference error. The ADC gain is calibrated w.r.t. the voltage on the REF2 pin.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND = DGND = 0 V, $f_{CLK\ IN}$ = 15 MHz, REFIN = +2.5 V)

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
Serial Interface			
t_1	$t_{CLK\ IN}$	ns min	$\overline{DRDY}$ High Time
t_2	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time
t_3	10	ns min	$\overline{RFS}$ Low to SCLK Falling Edge Setup Time
t_4	10	ns max	$\overline{RFS}$ Low to Data Valid Delay
t_5	25	ns min	SCLK High Pulse Width
t_6	25	ns min	SCLK Low Pulse Width
t_7[1]	25	ns max	SCLK Rising Edge to Data Valid Delay
t_8	0	ns min	$\overline{RFS}$ to SCLK Falling Edge Hold Time
t_9[2]	5	ns min	Bus Relinquish Time after Rising Edge of $\overline{RFS}$
	20	ns max	
Parallel Interface			
Read Operation			
t_{10}	2 × $t_{CLK\ IN}$	ns min	$\overline{DRDY}$ High Time
t_{11}	0	ns min	$\overline{DRDY}$ to $\overline{CS}$ Setup Time
t_{12}	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_{13}	25	ns min	$\overline{RD}$ Pulse Width
t_{14}[1]	25	ns min	Data Access Time after Falling Edge of $\overline{RD}$
t_{15}[2]	5	ns min	Bus Relinquish Time after Rising Edge of $\overline{RD}$
	20	ns max	
t_{16}	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{17}	$t_{CLK\ IN}$	ns max	$\overline{RD}$ to $\overline{DRDY}$ High Time
Write Operation			
t_{18}	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_{19}	35	ns min	$\overline{WR}$ Pulse Width
t_{20}	20	ns min	Data Valid to $\overline{WR}$ High Setup Time
t_{21}	0	ns min	Data Valid to $\overline{WR}$ High Hold Time
t_{22}	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time

NOTES
[1]t_7 and t_{14} are measured with the load circuit below and defined as the time required for an output to cross 0.4 V or 2 V.
[2]t_9 and t_{15} are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit shown below. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time quoted in the Timing Characteristics is the true bus relinquish time of the part and, as such, is independent of external bus loading capacitance.

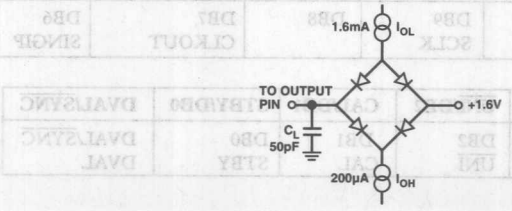

Figure 1. Load Circuit for Access Time and Bus Relinquish Time

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PIN FUNCTION DESCRIPTION

Mnemonic	Function
AV_{DD}	Analog Positive Supply Voltage, +5 V ± 5%.
AGND	Ground reference point for analog circuitry.
DV_{DD}	Digital Supply Voltage, +5 V ± 5%.
DGND	Ground reference point for digital circuitry.
VIN1 VIN2	Analog Input. In unipolar operation, the analog input range on VIN1 is VIN2 to (VIN2 + V_{REF}); for diffxerential (bipolar) operation, the analog input range on VIN1 is (VIN2 ± V_{REF}/2). Alternatively, VIN2 can be connected to the internal reference in bipolar mode to give a single-ended input on VIN1 of (VREF ± VREF/2). VIN2 can be connected to the internal reference on chip by taking SINGIP high in the serial mode or writing to bit SINGIP in the parallel mode. The absolute analog input range must lie between 0 and AV_{DD}. The analog input is continuously sampled and processed by the analog modulator.
REF1 REF2	Reference Pins. The AD7721 can operate with the on-board reference which has a nominal value of 2.5 V. Alternatively, an external reference can be used. There are three modes of operation: 1. Using the internal reference. REF2 is used as the REFOUT. A 10 nF capacitor is required on REF2. 2. Using an external reference. REF1 is used as REFIN with the external reference source being connected to this pin. This reference is internally buffered thus, the reference sees a high impedance static load. However, there will be an error added to this reference due to the offset voltage of the internal buffer amplifier, the offset having a value of ±5 mV maximum. A 10 nF capacitor is required from REF2 to ground. This method is useful when the external reference cannot drive a 10 nF load capacitor. 3. For system gain errors less than 0.02%, REF1 is grounded and the external reference is connected to REF2. REF2 is directly connected to the on-chip modulator. With this arrangement, a capacitor of value 10 nF is required between REF2 and ground.
XTAL	The AD7721 operates with a 15 MHz crystal or with a 15 MHz external clock which is connected to the XTAL pin. The modulator samples the analog input on both phases of the clock, increasing the sampling rate to 30 MHz.
$\overline{DRDY}$	Logic Output. In parallel mode, a falling edge indicates a new output word is available for transmission. $\overline{DRDY}$ will return high upon completion of a read operation. If a read operation does not occur between output updates, $\overline{DRDY}$ will become active for two clock cycles before the next output update. In serial mode, $\overline{DRDY}$ goes high for one SCLK cycle to indicate that data is available.
$\overline{CS}$	Chip Select. When the ADC is operated in parallel mode, this input selects the device. Note that serial mode operation is attained by tying $\overline{CS}$ along with $\overline{RD}$ and $\overline{WR}$ to DGND.
$\overline{RD}$	Read. This digital input is used in conjunction with $\overline{CS}$ to read data from the device when configured for parallel mode operation.
$\overline{WR}$	Write. This digital input is used in conjunction with $\overline{CS}$ to write data to the device when the part is configured for parallel mode operation.
SDATA/DB11 STBY/DB0 DVAL/$\overline{SYNC}$	The function of these pins depends on the status of $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$. Driving $\overline{CS}$ low along with $\overline{RD}$ or $\overline{WR}$ reads data or writes data to the device in the parallel mode. Tying $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ low together configures the part for serial mode operation. NOTE: All three pins must be low for a minimum of two clock cycles of the internal clock (15 MHz) before the part is configured for serial mode operation.

MODE	SDATA/DB11	$\overline{RFS}$/DB10	SCLK/DB9	DB8	CLKOUT/DB7	SINGIP/DB6	$\overline{SYNC}$/DB5
Parallel	DB11	DB10	DB9	DB8	DB7	DB6	DB5
Serial	SDATA	RFS	SCLK		CLKOUT	SINGIP	$\overline{SYNC}$

MODE	DB4	DB3	$\overline{UNI}$/DB2	CAL/DB1	STBY/DB0	DVAL/$\overline{SYNC}$
Parallel	DB4	DB3	DB2	DB1	DB0	DVAL/$\overline{SYNC}$
Serial			$\overline{UNI}$	CAL	STBY	DVAL

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SERIAL MODE ONLY

For serial mode operation, $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ must be tied to DGND.

SDATA/DB11	Serial Data Output. Output serial data becomes active after $\overline{RFS}$ goes low. Sixteen bits of data are clocked out starting with the MSB. Serial data is clocked out on the rising edge of SCLK and is valid on the subsequent falling edge of SCLK.
$\overline{RFS}$/DB10	Receive Frame Synchronization. Active low logic input. This is a logic input with $\overline{RFS}$ provided externally as a strobe or framing pulse to access serial data from the output register. Alternatively, $\overline{RFS}$ may be provided by connecting this input to $\overline{DRDY}$ which is active high in the serial mode. When $\overline{RFS}$ is high, SDATA is high impedance.
SCLK/DB9	Serial Clock. Logic Input. This input serial clock can be a continuous clock or, alternatively, it can be a non-continuous clock with the information being read from the AD7721 in smaller batches of data.
CLKOUT/DB7	Serial Clock. Logic Output. The internal digital clock is provided as an output on this pin. This buffered signal can alternatively be used as the clock input to SCLK in the serial mode.
SINGIP/DB6	Single-Ended Analog Input, Digital Input. The AD7721 can accept a single-ended analog input. A logic high on the logic input SINGIP causes the pin VIN2 to be connected to the reference internally, enabling the AD7721 to accept a single-ended analog input. When SINGIP is at a logic low, the AD7721 operates with a differential input.
$\overline{SYNC}$/DB5	Synchronization Input. The internal digital filter is reset on the rising edge of a $\overline{SYNC}$ pulse. The filter reset operation requires 2048 clock cycles, throughout which $\overline{DRDY}$ remains low. Should a $\overline{SYNC}$ be requested while the part is in calibration mode, the $\overline{SYNC}$ will be acted upon immediately and the calibration will be abandoned.
$\overline{UNI}$/DB2	Analog Input Range Select, Digital Input. The analog input range can be ±1.25 V or 0 V to 2.5 V. The $\overline{UNI}$ pin is used to select the input range required. A logic high on this pin selects the ±1.25 V range while a logic low selects the 0 V to 2.5 V analog input range.
CAL/DB1	Calibration Mode Pin. When this pin is pulsed high, the part is placed in its calibration mode and both the gain and offset are calibrated. At the end of calibration, new offset and gain calibration coefficients are loaded to the calibration registers.
STBY/DB0	Standby Mode Input. Logic input used to put the device into the power save (standby) mode. The STBY pin is low for normal operation and high for standby operation. When the part is placed in the standby mode, the values in the offset and gain registers are unaffected.
DVAL/$\overline{SYNC}$	Data Valid Digital Output. An excessive overload on the modulator inputs can cause the modulator to go unstable. Once this condition is detected by internal circuits, the modulator is reset into a stable state and DVAL goes low for 2048 clock cycles. This period allows sufficient time for the modulator and digital filter to settle. An overload on the input pins can also cause clipping in the digital filter. This will cause DVAL to remain low. As well as the AD7721 indicating an overload by taking DVAL low, the AD7721 also highlights an overload by loading the output register. A positive overload causes the output register to be reset to 111 . . . 11 (unipolar input) or 011 . . . 11 (bipolar input). A negative overload causes the output register to be set to 000 . . .00 (unipolar input) or 100 . . .00 (bipolar input). When DVAL goes low, data can still be read from the interface and $\overline{DRDY}$ will continue to indicate that there is data to be read.

PARALLEL MODE ONLY

DVAL/$\overline{SYNC}$	Data Valid Digital Output/Synchronization Input depending on the status of bit DB3 in the control register. When the AD7721 is powered up, bit DB3 will be set to "0," causing this pin to be programmed as DVAL. The pin can be placed in $\overline{SYNC}$ mode by writing a "1" to bit DB3 in the control register. When changing the function of this pin from $\overline{SYNC}$ mode to DVAL mode, a logic high must be applied to the pin. DVAL: An overload in the modulator is highlighted as in the serial mode. $\overline{SYNC}$: Operates as in the serial mode except $\overline{DRDY}$ remains high while the digital filter is being reset.
SDATA/DB11–STBY/DB0	Data Outputs DB11 to DB0, DB11 being the Most Significant Bit (MSB).

PRELIMINARY TECHNICAL DATA

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arrangement to allow easy interfacing to industry-standard microprocessors, microcontrollers and digital signal processors. The AD7721 can be operated in External-Clocking mode. This External-Clocking mode is designed for direct interface to systems that provide a serial clock output which is synchronized to the serial data output including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors. This external clock can have a frequency up to 20 MHz. Alternatively, the SCLK input can be provided by the master clock by connecting CLKOUT to SCLK. The $\overline{RFS}$ signal can also be provided by the AD7721 by connecting $\overline{RFS}$ to $\overline{DRDY}$.

Figure 2 shows the timing diagram for reading from the AD7721. $\overline{DRDY}$ goes high to indicate the presence of a new word in the output register. $\overline{DRDY}$ remains high for one internal clock (15 MHz) cycle. $\overline{RFS}$ is taken low to access data from the AD7721. The serial clock input does not have to be continuous. The serial data can be accessed in a number of bytes. However, $\overline{RFS}$ must remain low for the duration of the data transfer operation. Although the AD7721 has a 12-bit digital output in the parallel mode, sixteen bits of data are available for transmission in the serial mode, starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. $\overline{DRDY}$ rises for one internal clock cycle when a new word is available in the output register. Any earlier result still in the output register is lost at this time.

The device defaults to parallel mode if $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ are not tied to DGND together. Figure 3 shows a timing diagram for reading from the AD7721 in the parallel mode. When conversion is complete, $\overline{DRDY}$ goes low to indicate that new data is available in the AD7721's output register. When the data has been read from the register using the $\overline{CS}$ and $\overline{RD}$ inputs, the $\overline{DRDY}$ pin returns high. This $\overline{DRDY}$ pin can be used to drive an edge-triggered interrupt of a microprocessor. $\overline{CS}$ and $\overline{RD}$ going low accesses the 12-bit conversion result.

Write Operation

The write operation is used for self-calibration, selecting unipolar or bipolar analog input ranges, placing the part in power down mode (standby) or programming the function of pin DVAL/$\overline{SYNC}$. When the AD7721 is placed in the write mode, data bits DB0 to DB3 and DB6 function as control bits, DB0 becoming the Standby mode bit, DB1 becoming the Calibration mode bit, DB2 being used to select the analog input range and, DB3 being used to select the function of pin DVAL/$\overline{SYNC}$. Writing a logic "1" to DB2 selects bipolar operation while a logic low selects unipolar operation. For a single-ended input in bipolar mode, DB6 (SINGIP) is taken to a logic high. When SINGIP is at a logic low, VIN2 must be provided externally. The part powers up in unipolar mode. Calibration is performed by writing a logic "1" to DB1 while the part is put into the standby mode by inputting a logic high to DB0. Writing a "1" to bit DB3 places pin DVAL/$\overline{SYNC}$ in $\overline{SYNC}$ mode while

PRELIMINARY TECHNICAL DATA

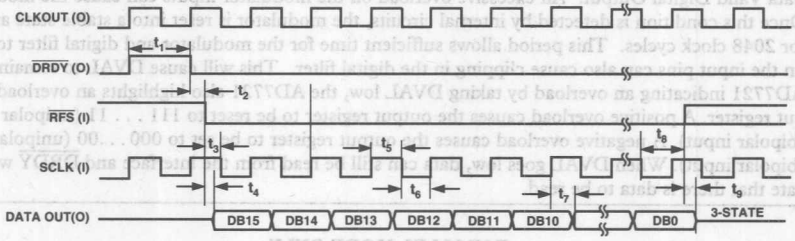

Figure 2. Serial Mode Output Register Read

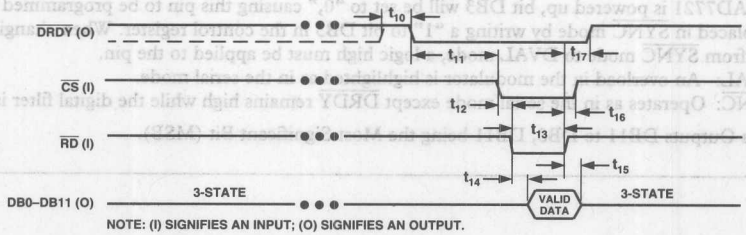

Figure 3. Parallel Mode Output Register Read

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writing a "0" places the pin in DVAL mode. $\overline{CS}$ and $\overline{WR}$ going low places this information in the control register. Figure 4 shows a timing diagram for the write operation. Bits DB4 to DB5 and bits DB7 to DB15 are used to test the AD7721 in parallel mode. Thus, for normal operation, a logic "0" is inputted to these bits.

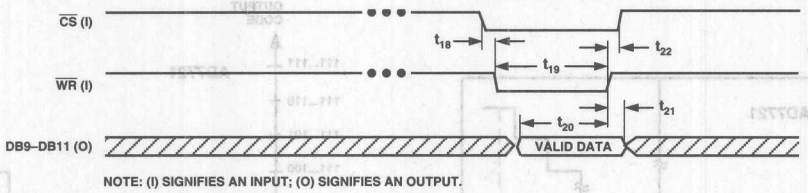

Figure 4. Write Timing Diagram

READ	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4
WRITE	0	0	0	0	0	SINGIP	0	0

READ	DB3	DB2	DB1	DB0
WRITE	DVAL/$\overline{SYNC}$	$\overline{UNI}$	CAL	STBY

Figure 5. Control Register

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ANALOG INPUT

In the bipolar mode configuration, the analog input range is ±1.25 V. The designed code transitions occur midway between successive integer LSB values. The output code is 2s complement binary with 1 LSB = 0.61 mV in parallel mode and 38 μV in serial mode. The ideal input/output transfer function is illustrated in Figure 6.

In the unipolar mode, the analog input range is 0 V to 2.5 V. Again, the designed code transitions occur midway between successive integer LSB values. The output code is straight binary with 1 LSB = 0.61 mV in parallel mode and 38 μV in serial mode. The ideal input/output transfer function is shown in Figure 7.

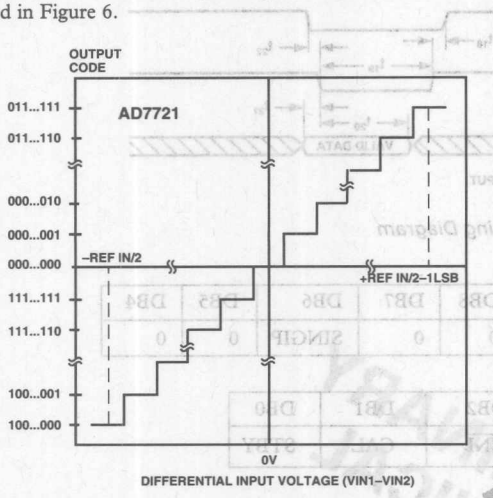

Figure 6. Bipolar Mode Transfer Function

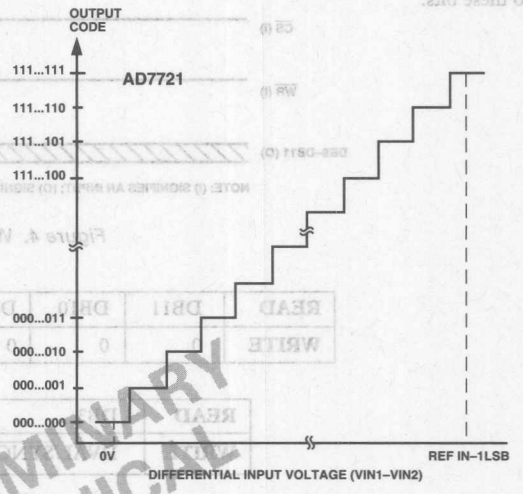

Figure 7. Unipolar Mode Transfer Function

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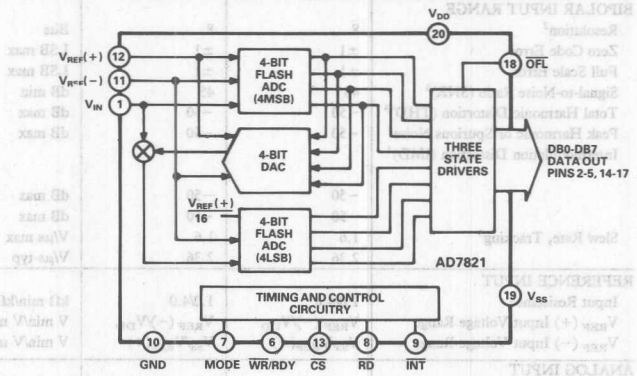
LC²MOS High Speed, µP-Compatible 8-Bit ADC with Track/Hold Function

AD7821

FEATURES

- Fast Conversion Time: 660 ns max
- 100 kHz Track-and-Hold Function
- 1 MHz Sample Rate
- Unipolar and Bipolar Input Ranges
- Ratiometric Reference Inputs
- No External Clock
- Extended Temperature Range Operation
- Skinny 20-Pin DIPs, SOIC and 20-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7821 is a high-speed, 8-bit, sampling, analog-to-digital converter that offers improved performance over the popular AD7820. It offers a conversion time of 660 ns (vs. 1.36 µs for the AD7820) and 100 kHz signal bandwidth (vs. 6.4 kHz). The sampling instant is better defined and occurs on the falling edge of $\overline{WR}$ or $\overline{RD}$. The provision of a V_{SS} pin (Pin 19) allows the part to operate from ±5 V supplies and to digitize bipolar input signals. Alternatively, for unipolar inputs, the V_{SS} pin can be grounded and the AD7821 will operate from a single +5 V supply, like the AD7820.

The AD7821 has a built-in track-and-hold function capable of digitizing full-scale signals up to 100 kHz max. It also uses a half-flash conversion technique that eliminates the need to generate a CLK signal for the ADC.

The AD7821 is designed with standard microprocessor control signals ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RDY, $\overline{INT}$) and latched, three-state data outputs capable of interfacing to high-speed data buses. An overflow output ($\overline{OFL}$) is also provided for cascading devices to achieve higher resolution.

The AD7821 is fabricated in Linear-Compatible CMOS (LC²MOS), an advanced, mixed technology process combining precision bipolar circuits with low-power CMOS logic. The part features a low power dissipation of 50 mW.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The half-flash conversion technique, coupled with fabrication on Analog Devices' LC²MOS process, enables a very fast conversion time. The conversion time for the WR-RD mode is 660 ns, with 700 ns for the RD mode.
2. Built-In Track-and-Hold
   This allows input signals with slew rates up to 1.6 V/µs to be converted to 8-bits without an external track-and-hold. This corresponds to a 5 V peak-to-peak, 100 kHz sine-wave signal.
3. Total Unadjusted Error
   The AD7821 features an excellent total unadjusted error figure of less than ±1 LSB over the full operating temperature range.
4. Unipolar/Bipolar Input Ranges
   The AD7821 is specified for single supply (+5 V) operation with a unipolar full-scale range of 0 to +5 V, and for dual supply (±5 V) operation with a bipolar input range of ±2.5 V. Typical performance characteristics are given for other input ranges.
5. Dynamic Specifications for DSP Users
   In addition to the traditional ADC specifications, the AD7821 is specified for ac parameters, including signal-to-noise ratio, distortion and slew rate.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7821—SPECIFICATIONS

V_{DD} = +5 V ± 5%, GND = 0 V. Unipolar Input Range: V_{SS} = GND, $V_{REF}(+)$ = 5 V, $V_{REF}(-)$ = GND. Bipolar Input Range: V_{SS} = −5 V ± 5%, $V_{REF}(+)$ = 2.5 V, $V_{REF}(-)$ = −2.5 V. These test conditions apply unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated. Specifications apply for RD Mode (Pin 7 = 0 V).

Parameter	K Version[1]	B, T Versions	Units	Comments
UNIPOLAR INPUT RANGE				
Resolution[2]	8	8	Bits	
Total Unadjusted Error[3]	±1	±1	LSB max	
Minimum Resolution for which				
No Missing Codes are Guaranteed	8	8	Bits	
BIPOLAR INPUT RANGE				
Resolution[2]	8	8	Bits	
Zero Code Error	±1	±1	LSB max	
Full Scale Error	±1	±1	LSB max	
Signal-to-Noise Ratio (SNR)[3]	45	45	dB min	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Total Harmonic Distortion (THD)[3]	−50	−50	dB max	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Peak Harmonic or Spurious Noise[3]	−50	−50	dB max	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Intermodulation Distortion (IMD)[3]				fa (84.72 kHz) and fb (94.97 kHz) Full-Scale Sine Waves with $f_{SAMPLING}$ = 500 kHz
	−50	−50	dB max	Second Order Terms
	−50	−50	dB max	Third Order Terms
Slew Rate, Tracking[3]	1.6	1.6	V/μs max	
	2.36	2.36	V/μs typ	
REFERENCE INPUT				
Input Resistance	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
V_{REF} (+) Input Voltage Range	V_{REF} (−)/V_{DD}	V_{REF} (−)/V_{DD}	V min/V max	
V_{REF} (−) Input Voltage Range	V_{SS}/V_{REF}(+)	V_{SS}/V_{REF}(+)	V min/V max	
ANALOG INPUT				
Input Voltage Range	$V_{REF}(-)/V_{REF}(+)$	$V_{REF}(-)/V_{REF}(+)$	V min/V max	
Input Leakage Current	±3	±3	μA max	−5 V ≤ V_{IN} ≤ +5 V
Input Capacitance	55	55	pF typ	
LOGIC INPUTS				
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$				
V_{INH}	2.4	2.4	V min	
V_{INL}	0.8	0.8	V max	
I_{INH} ($\overline{CS}$, $\overline{RD}$)	1	1	μA max	
I_{INH} ($\overline{WR}$)	3	3	μA max	
I_{INL}	−1	−1	μA max	
Input Capacitance[4]	8	8	pF max	Typically 5 pF
MODE				
V_{INH}	3.5	3.5	V min	
V_{INL}	1.5	1.5	V max	
I_{INH}	200	200	μA max	50 μA typ
I_{INL}	−1	−1	μA max	
Input Capacitance[4]	8	8	pF max	Typically 5 pF
LOGIC OUTPUTS				
DB0–DB7, $\overline{OFL}$, $\overline{INT}$				
V_{OH}	4.0	4.0	V min	I_{SOURCE} = 360 μA
V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
I_{OUT} (DB0–DB7)	±3	±3	μA max	Floating State Leakage
Output Capacitance[4] (DB0–DB7)	8	8	pF max	Typically 5 pF
RDY				
V_{OL}	0.4	0.4	V max	I_{SINK} = 2.6 mA
I_{OUT}	±3	±3	μA max	Floating State Leakage
Output Capacitance[4]	8	8	pF max	Typically 5 pF
POWER SUPPLY				
I_{DD}	15	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 0 V
I_{SS}	100	100	μA max	$\overline{CS}$ = $\overline{RD}$ = 0 V
Power Dissipation	50	50	mW typ	
Power Supply Sensitivity	±1/4	±1/4	LSB max	±1/16 LSB typ, V_{DD} = 4.75 V to 5.25 V, (V_{REF}(+) = 4.75 V max for Unipolar Mode)

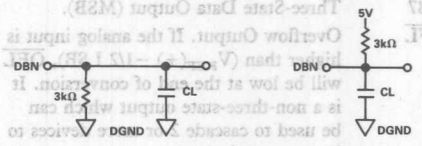
NOTES
[1]Temperature Ranges are as follows: K Version = −40°C to +85°C; B Version = −40°C to +85°C; T Version = −55°C to +125°C.
[2]1 LSB = 19.53 mV for both the unipolar (0 to +5 V) and bipolar (−2.5 V to +2.5 V) input ranges.
[3]See Terminology.
[4]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{SS} = 0 V or −5 V ± 5%; Unipolar or Bipolar Input Range)

Parameter	Limit at 25°C (All Versions)	Limit at T_{min}, T_{max} (K, B, Versions)	Limit at T_{min}, T_{max} (T Version)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Hold Time
t_{RDY}[2]	70	85	100	ns max	$\overline{CS}$ to RDY Delay. Pull-Up Resistor 5 kl.
t_{CRD}	700	875	975	ns max	Conversion Time (RD Mode)
t_{ACC0}[3]					Data Access Time (RD Mode)
	t_{CRD} +25	t_{CRD} +30	t_{CRD} +35	ns max	C_L = 20 pF
	t_{CRD} +50	t_{CRD} +65	t_{CRD} +75	ns max	C_L = 100 pF
t_{INTH}[2]	50	–	–	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)
	80	85	90	ns max	
t_{DH}[4]	15	15	15	ns min	Data Hold Time
	60	70	80	ns max	
t_P	350	425	500	ns min	Delay Time Between Conversions
t_{WR}	250	325	400	ns min	Write Pulse Width
	10	10	10	µs max	
t_{RD}	250	350	450	ns min	Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses
t_{READ1}	160	205	240	ns min	$\overline{RD}$ Pulse Width (WR–RD Mode, see Figure 12b) Determined by t_{ACC1}
t_{ACC1}[3]					Data Access Time (WR-RD Mode, see Figure 12b)
	160	205	240	ns max	C_L = 20 pF
	185	235	275	ns max	C_L = 100 pF
t_{RI}	150	185	220	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_{INTL}[2]	380	-	-	ns typ	$\overline{WR}$ to $\overline{INT}$ Delay
	500	610	700	ns max	
t_{READ2}	65	75	85	ns min	$\overline{RD}$ Pulse Width (WR–RD Mode, see Figure 12a) Determined by t_{ACC2}
t_{ACC2}[3]					Data Access Time (WR–RD Mode, see Figure 12a)
	65	75	85	ns max	C_L = 20 pF
	90	110	130	ns max	C_L = 100 pF
t_{IHWR}[2]	80	100	120	ns max	$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation)
t_{ID}[3]					Data Access Time after $\overline{INT}$ (Stand-Alone Operation)
	30	35	40	ns max	C_L = 20 pF
	45	60	70	ns max	C_L = 100 pF

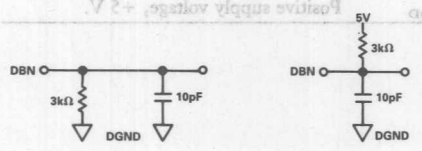
NOTES
[1]Sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[2]C_L = 50 pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]Defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

Test Circuits



a. High Z to V_{OH} *b. High Z to V_{OL}*

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High Z *b. V_{OL} to High Z*

Figure 2. Load Circuits for Data Hold Time Test

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7821KN	−40°C to +85°C	±1 max	N-20
AD7821KP	−40°C to +85°C	±1 max	P-20A
AD7821KR	−40°C to +85°C	±1 max	R-20
AD7821BQ	−40°C to +85°C	±1 max	Q-20
AD7821TQ	−55°C to +125°C	±1 max	Q-20
AD7821TE	−55°C to +125°C	±1 max	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

Digital Input Voltage to GND
(Pins 6-8, 13). . . . . −0.3 V, V_{DD} +0.3 V
Digital Output Voltage to GND
(Pins 2-5, 9, 14-18). . . . . −0.3 V, V_{DD} +0.3 V
V_{REF} (+) to GND . . . . . V_{SS} −0.3 V, V_{DD} +0.3 V
V_{REF} (−) to GND . . . . . V_{SS} −0.3 V, V_{DD} +0.3 V
V_{IN} to GND. . . . . V_{SS} −0.3 V, V_{DD} +0.3 V
Operating Temperature Range
Commercial (K Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 6 mW/°C

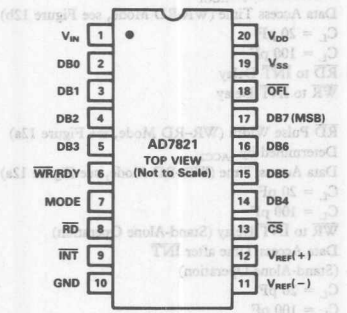
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

PIN CONFIGURATIONS

DIP AND SOIC



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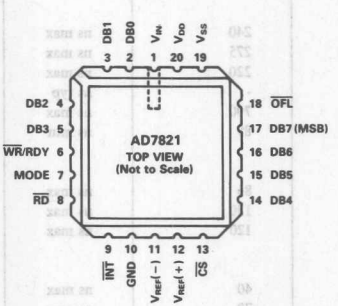

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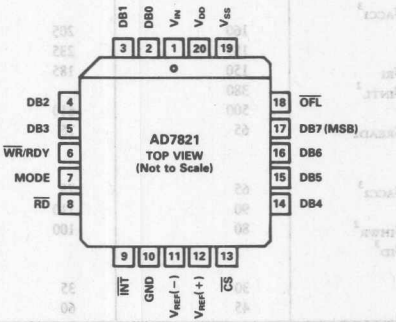


PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{IN}	Analog Input: Range $V_{REF}(-) \le V_{IN} \le V_{REF}(+)$.
2	DB0	Three-State Data Output (LSB).
3–5	DB1–DB3	Three-State Data Outputs.
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	MODE	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. This input is internally pulled low through a 50 μA current source. See Digital Interface section.
8	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data from the part. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT Output. $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$. See Digital Interface section.
10	GND	Ground.
11	$V_{REF}(-)$	Lower limit of reference span. Range: $V_{SS} \le V_{REF}(-) < V_{REF}(+)$.
12	$V_{REF}(+)$	Upper limit of reference span. Range: $V_{REF}(-) < V_{REF}(+) \le V_{DD}$.
13	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
14–16	DB4–DB6	Three-State Data Outputs.
17	DB7	Three-State Data Output (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than ($V_{REF}(+) - 1/2$ LSB), $\overline{OFL}$ will be low at the end of conversion. It is a non-three-state output which can be used to cascade 2 or more devices to increase resolution.
19	V_{SS}	Negative supply voltage. V_{SS} = 0 V; Unipolar Operation. V_{SS} = −5 V; Bipolar Operation.
20	V_{DD}	Positive supply voltage, +5 V.

3 V to 5 V Single Supply, 200 kSPS, Single/Multichannel 12-Bit Sampling ADCs

AD7853/AD7858

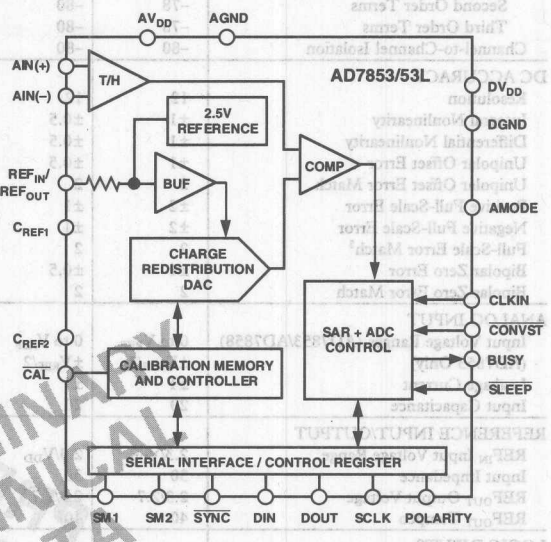
FEATURES

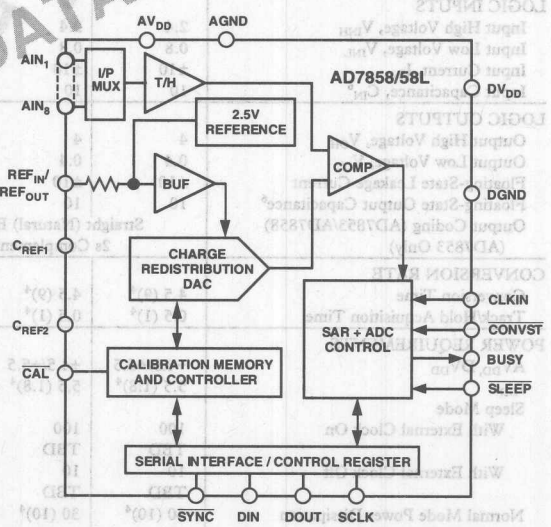
- Battery-Compatible Supply Voltage: Guaranteed Specs for V_{DD} of 3 V to 5.5 V
- AD7853/AD7858: 200 kSPS, AD7853L/AD7858L: 100 kSPS
- Pseudo-Differential Input with Two Input Ranges (AD7853)
- 8 Single Ended or 4 Pseudo-Differential Inputs (AD7858)
- Self and System Calibration
- Read/Write Capability of Calibration Data
- Low Power
  - AD7853/AD7858: 15 mW (V_{DD} = 3 V)
  - AD7853L/AD7858L: 5.5 mW (V_{DD} = 3 V)
- Power-Down Mode: 25 µW Power Consumption
- Flexible Serial Interface
  - Three-Wire SPI Compatible
  - Two-Wire 8051 Compatible
- 24-Pin DIP, SOIC and SSOP Packages

APPLICATIONS

- Battery-Powered Systems (Portable PCs, Personal Digital Assistants (PDAs))
- Pen Computers
- Instrumentation and Control Systems
- High Speed Modems

FUNCTIONAL BLOCK DIAGRAMS





PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7853/AD7858 are high speed, low power, 12-bit ADCs that operate from a single 3 V or 5 V power supply, the AD7853 being the single channel version and the AD7858 the multi-channel version. The ADCs contain self-calibration and system calibration options to ensure accurate operation over time and temperature.

The AD7853/AD7858 is capable of 200 kHz throughput rate. The input track-and-hold acquires a signal in 500 ns and features a pseudo-differential sampling scheme. The AD7853 has the added advantage of two input voltage ranges (0 V to V_{REF} and $-V_{REF}/2$ to $+V_{REF}/2$). Input signal range is to the supply and the part is capable of converting full power signals to 100 kHz.

CMOS construction ensures low power dissipation (18 mW typ) with power-down mode (25 µW typ). The part is available in 24-pin, 0.3 inch-wide DIP, 24-lead SOIC and 24-lead SSOP packages.

PRODUCT HIGHLIGHTS

1. Operation with either 3 V or 5 V power supplies.
2. Operates with reference voltages from 1.2 V to the supply.
3. Unipolar analog input range from 0 V to V_{SUPPLY}.
4. Self and System calibration including power-down mode.
5. Versatile serial I/O port.
6. Single channel (AD7853) or 8 channel (AD7858).

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7853/AD7858–5 V SPECIFICATIONS[1, 2]

(AV_{DD} = DV_{DD} = +5.0 V ± 10%, f_{CLKIN} = 4 MHz; f_{SAMPLE} = 200 kHz (AD7853/AD7858) 100 kHz (AD7853L/AD7858L); $\overline{SLEEP}$ = Logic High; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal-to-Noise Ratio[3] (SNR)	70	71	dB min	Typically SNR Is 72 dB
				V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (100 kHz)[4]
Total Harmonic Distortion (THD)	–78	–80	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (100 kHz)[4]
Peak Harmonic or Spurious Noise	–78	–80	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 200 kHz (100 kHz)[4]
Intermodulation Distortion (IMD)				
Second Order Terms	–78	–80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz (100 kHz)[4]
Third Order Terms	–78	–80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz (100 kHz)[4]
Channel-to-Channel Isolation	–80	–80	dB max	(AD7858 Only)
DC ACCURACY				(Any Channel AD7858 Only)
Resolution	12	12	Bits	
Integral Nonlinearity	±1	±0.5	LSB max	
Differential Nonlinearity	±1	±0.5	LSB max	Guaranteed No Missed Codes to 12 Bits
Unipolar Offset Error	±1	±0.5	LSB max	
Unipolar Offset Error Match	2	2	LSB max	(AD7858 Only)
Positive Full-Scale Error	±2	±1	LSB max	
Negative Full-Scale Error	±2	±1	LSB max	
Full-Scale Error Match[5]	2	2	LSB max	(AD7858 Only)
Bipolar Zero Error	±1	±0.5	LSB max	
Bipolar Zero Error Match	2	2	LSB max	(AD7858 Only)
ANALOG INPUT				
Input Voltage Ranges (AD7853/AD7858)	0 to V_{REF}	0 to V_{REF}	Volts	i.e., AIN(+) – AIN(–) = 0 V to V_{REF}
(AD7853 Only)	±V_{REF}/2	±V_{REF}/2	Volts	i.e., AIN(+) – AIN(–) = –V_{REF}/2 to +V_{REF}/2
Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT/OUTPUT				
REF_{IN} Input Voltage Range	2.3/V_{DD}	2.3/V_{DD}	V min/max	Functional from 1.2 V
Input Impedance	30	30	kΩ min	Resistor Connected to Internal Reference Node
REF_{OUT} Output Voltage	2.3/2.7	2.3/2.7	V min/max	
REF_{OUT} Tempco	40	40	ppm/°C typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[6]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	4	4	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 0.8 mA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[6]	10	10	pF max	
Output Coding (AD7853/AD7858)	Straight (Natural) Binary			Unipolar Input Range
(AD7853 Only)	2s Complement			Bipolar Input Range
CONVERSION RATE				
Conversion Time	4.5 (9)[4]	4.5 (9)[4]	µs max	(L Versions Only)
Track/Hold Acquisition Time	0.5 (1)[4]	0.5 (1)[4]	µs max	(L Versions Only)
POWER REQUIREMENTS				
AV_{DD}, DV_{DD}	+4.5/+5.5	+4.5/+5.5	V min/max	
I_{DD}	5.5 (1.8)[4]	5.5 (1.8)[4]	mA max	Typically 4.5 mA (1.5)[4]; $\overline{SLEEP}$ = V_{DD}
Sleep Mode				Logic Inputs @ 0 V or V_{DD}; $\overline{SLEEP}$ = 0 V
With External Clock On	100	100	µA max	Typically 70 µA. PMGT (Control Register) = 1
	TBD	TBD	µA max	PMGT (Control Register) = 0
With External Clock Off	10	10	µA max	Typically 7 µA. PMGT (Control Register) = 1
	TBD	TBD	µA max	PMGT (Control Register) = 0.
Normal Mode Power Dissipation	30 (10)[4]	30 (10)[4]	mW max	V_{DD} = 5.5 V: Typically 25 mW (8)[4]; $\overline{SLEEP}$ = V_{DD}
Save Mode Power Dissipation				
With External Clock On	0.55	0.55	mW max	V_{DD} = 5.5 V: Typically 0.4 mW; $\overline{SLEEP}$ = 0 V
With External Clock Off	55	55	µW max	V_{DD} = 5.5 V: Typically 30 µW; $\overline{SLEEP}$ = 0 V

NOTES

[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.

[2]Specifications apply after calibration.

[3]SNR calculation includes distortion and noise components.

[4]Specifications written within parentheses ( ) refer to the AD7853L/AD7858L.

[5]Full-scale error match is the worst case of the positive full-scale error match or the negative full-scale error match.

[6]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

3 V SPECIFICATIONS[1, 2]

(AV_{DD} = DV_{DD} = +3.0 V to +3.6 V, f_{CLKIN} = 5 MHz; (2.5 MHz for L versions); f_{SAMPLE} = 200 kHz (AD7853/AD7858) 100 kHz (AD7853L/AD7858L); $\overline{SLEEP}$ = Logic High; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal-to-Noise Ratio[3] (SNR)	70	71	dB min	Typically SNR Is 72 dB V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (100 kHz)[4]
Total Harmonic Distortion (THD)	–78	–80	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (100 kHz)[4]
Peak Harmonic or Spurious Noise	–78	–80	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 200 kHz (100 kHz)[4]
Intermodulation Distortion (IMD)				
Second Order Terms	–78	–80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz (100 kHz)[4]
Third Order Terms	–78	–80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz (100 kHz)[4]
Channel-to-Channel Isolation	–80	–80	dB max	(AD7858 Only)
DC ACCURACY				(Any Channel AD7858 Only)
Resolution	12	12	Bits	
Integral Nonlinearity	±1	±0.5	LSB max	
Differential Nonlinearity	±1	±0.5	LSB max	Guaranteed No Missed Codes to 12 Bits
Unipolar Offset Error	±1	±0.5	LSB max	
Unipolar Offset Error Match	2	2	LSB max	(AD7858 Only)
Positive Full-Scale Error	±2	±1	LSB max	
Negative Full-Scale Error	±2	±1	LSB max	
Full-Scale Error Match[5]	2	2	LSB max	(AD7858 Only)
Bipolar Zero Error	±1	±0.5	LSB max	
Bipolar Zero Error Match	2	2	LSB max	(AD7858 Only)
ANALOG INPUT				
Input Voltage Ranges (AD7853/AD7858)	0 to V_{REF}	0 to V_{REF}	Volts	i.e., AIN(+) – AIN(–) = 0 V to V_{REF}
(AD7853 Only)	±V_{REF}/2	±V_{REF}/2	Volts	i.e., AIN(+) – AIN(–) = –V_{REF}/2 to +V_{REF}/2
Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT/OUTPUT				
REF_{IN} Input Voltage Range	2.3/V_{DD}	2.3/V_{DD}	V min/max	Functional from 1.2 V
Input Impedance	30	30	kΩ min	Resistor Connected to Internal Reference Node
REF_{OUT} Output Voltage	2.3/2.7	2.3/2.7	V min/max	
REF_{OUT} Tempco	40	40	ppm/°C typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.1	2.1	V min	
Input Low Voltage, V_{INL}	0.6	0.6	V max	
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[6]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	2.4	2.4	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 0.8 mA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[6]	10	10	pF max	
Output Coding (AD7853/AD7858)	Straight (Natural) Binary			Unipolar Input Range
(AD7853 Only)	2s Complement			Bipolar Input Range
CONVERSION RATE				
Conversion Time	4.5 (9)[4]	4.5 (9)[4]	µs max	(L Versions Only)
Track/Hold Acquisition Time	0.5 (1)[4]	0.5 (1)[4]	µs max	(L Versions Only)
POWER REQUIREMENTS				
AV_{DD}, DV_{DD}	+3.0/+3.6	+3.0/+3.6	V min/max	
I_{DD}	5.0 (1.8)[4]	5.0 (1.8)[4]	mA max	Typically 4.0 mA (1.5)[4]; $\overline{SLEEP}$ = V_{DD}
Sleep Mode				Logic Inputs @ 0 V or V_{DD}; $\overline{SLEEP}$ = 0 V
With External Clock On	100	100	µA max	Typically 70 µA. PMGT (Control Register) = 1
	TBD	TBD	µA max	PMGT (Control Register) = 0
With External Clock Off	10	10	µA max	Typically 7 µA. PMGT (Control Register) = 1
	TBD	TBD	µA max	PMGT (Control Register) = 0.
Normal Mode Power Dissipation	18 (6.5)[4]	18 (6.5)[4]	mW max	V_{DD} = 3.6 V: Typically 15 mW (5.4)[4]; $\overline{SLEEP}$ = V_{DD}
Standby Mode Power Dissipation				
With External Clock On	0.36	0.36	mW max	V_{DD} = 3.6 V: Typically 0.3 mW; $\overline{SLEEP}$ = 0 V
With External Clock Off	36	36	µW max	V_{DD} = 3.6 V: Typically 25 µW; $\overline{SLEEP}$ = 0 V

NOTES

[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.

[2]Specifications apply after calibration.

[3]SNR calculation includes distortion and noise components.

[4]Specifications written within parentheses ( ) refer to the AD7853L/AD7858L.

[5]Full-scale error match is the worst case of the positive full-scale error match or the negative full-scale error match.

[6]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

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PRELIMINARY TECHNICAL DATA

AD7853/AD7858

TIMING SPECIFICATIONS[1, 2] (V_{DD} = +3.0 V to +5.5 V; f_{CLKIN} = 4 MHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (A, B, S Versions)	Units	Description
f_{CLKIN}	500 4	kHz min MHz max	Master Clock Frequency (2 MHz for the AD7853L/AD7858L)
f_{SCLK}	$f_{CLK\ IN}$	MHz max	Serial Clock Input Frequency
t_1	100[3]	ns min	$\overline{CONVST}$ Pulse Width
t_2	50	ns max	$\overline{CONVST}$ to BUSY Propagation Delay
$t_{CONVERT}$	4.5 (18 × t_{CLKIN})	µs max	Conversion Time
t_3	60 (60/0.4 × t_{SCLK})	ns min (min/max)	$\overline{SYNC}$ to SCLK falling Edge Setup Time (Continuous SCLK input).
t_{3A}	60	ns min	$\overline{SYNC}$ to SCLK falling Edge Setup Time (AD7853 only).
t_4	60[4]	ns max	Delay from $\overline{SYNC}$ until DOUT 3-state disabled.
t_{4A}	70[4]	ns max	Delay from $\overline{SYNC}$ until DIN 3-state disabled.
t_5	60[4]	ns max	Data Access time after falling edge of SCLK.
t_6	40	ns min	Data Setup Time Prior to rising edge of SCLK.
t_7	0	ns min	Data Valid to SCLK Hold Time.
t_8	0.4 × t_{SCLK}[5]	ns min	SCLK High Pulse Width
t_9	0.4 × t_{SCLK}[5]	ns min	SCLK Low Pulse Width
t_{10}	30 (30/0.4 × t_{SCLK})	ns min (min/max)	SCLK Rising Edge to $\overline{SYNC}$ Hold Time (Continuous SCLK).
t_{10A}	30	ns min	SCLK Rising Edge to $\overline{SYNC}$ Hold Time (AD7853 only).
t_{11}	60[4]	ns max	Delay from $\overline{SYNC}$ until DOUT 3-state enabled.
t_{11A}	70[4]	ns max	Delay from $\overline{SYNC}$ until DIN 3-state enabled.
t_{12}	80[4]	ns max	Delay from SCLK to DIN being configured as output.
t_{13}	60[4]	ns max	Delay from SCLK to DIN being configured as input.
t_{14}	100	ns max	$\overline{CAL}$ Rising Edge to BUSY delay.
t_{15}	50	ns max	$\overline{CONVST}$ to BUSY delay in calibration sequence.
t_{CAL}	N_2 × t_{CLKIN}		Full self calibration time, N_2 an integer.
t_{CAL1}	N_3 × t_{CLKIN}		Internal DAC plus system full-scale calibration time, N_3 an integer.
t_{CAL2}	N_4 × t_{CLKIN}		System offset calibration time, N_4 an integer.

NOTES

[1]Sample tested at +25°C to ensure compliance. The timing figures here are for the AD7853/AD7858 only and not for the AD7853L/AD7858L, so the timing figures for the AD7853L/AD7858L will reflect that the AD7853L/AD7858L operates at half the speed of the AD7853, and an example of this is given with the max master clock frequency of 2.5 MHz for the AD7853L/AD7858L. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

[2]See Table I and Figures 2, 4, 5, 6, 8 where all the timing diagrams are for ADC output data as distinct from calibration or control register data in which case there would not be the 4 leading zeros with the output data. Instead there would be 4 data bits DB15–DB12 in their place.

[3]The $\overline{CONVST}$ pulse width will depend on the way the part is being operated. For operation where the BUSY is not connected to the $\overline{SLEEP}$ pin then the $\overline{CONVST}$ pulse width is 100 ns min as stated above. If BUSY is connected to the $\overline{SLEEP}$ pin so that the part goes into sleep mode after conversion the conversion time will be different and will also be dependent on the PMGT bit in the control register.

[4]t_4 is measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

[5]SCLK mark/space ratio (measured from a voltage level of 1.6 V) is 40/60 to 60/40.

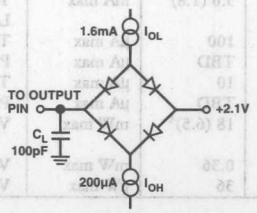


Figure 1. Load Circuit for Digital Output Timing Specifications

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

TYPICAL TIMING DIAGRAM

All the timing diagrams (Figures 2–9) are for ADC output data from the part, and this is why there are 4 leading zeros before the 12 bits of data. However for a control register or calibration register read, there will not be 4 leading zeros on the output data. These 4 leading zeros will be replaced by data bits DB15–DB12 for this read operations.

In Figure 2 below we have a typical read and write timing diagram with the $\overline{\text{CONVST}}$ and BUSY. The essence of this is to show exactly what most of the timing numbers relate to. Here the reading from and writing to the part is shown after the conversion so in this case the maximum conversion rate cannot be achieved. To achieve the maximum throughput rate of 100 kHz (AD7853L) or 200 kHz (AD7853) the user must read from and write to the part during conversion.

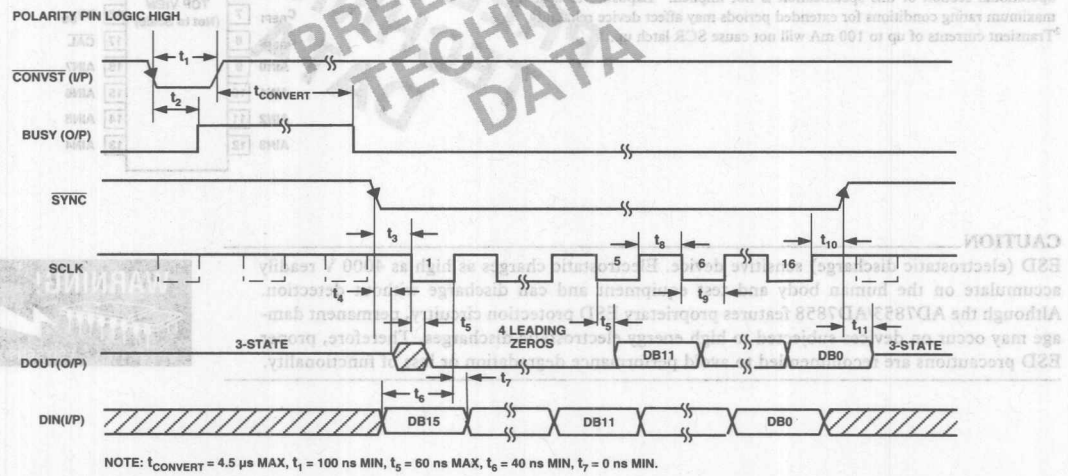
There is a very useful mode of operation for reducing power consumption. In this power save mode of operation the BUSY can be connected to the $\overline{\text{SLEEP}}$ pin so that at the end of conversion the part automatically goes into sleep mode. However on the next $\overline{\text{CONVST}}$ pulse, the part then must be allowed a reasonable time to "wake up" before converting the signal on the AIN pin. Thus the $\overline{\text{CONVST}}$ pulse width must be made longer and will extend well beyond the rising edge of the BUSY (see specification for $\overline{\text{CONVST}}$ pulse width) so that it caters for what is called "wake-up" time.

ORDERING GUIDE

Model	Linearity Error (LSB)	Power Dissipation (mW)	Package Option*
AD7853AN	±1	18	N-24
AD7853BN	±1/2	18	N-24
AD7853LAN	±1	6.5	N-24
AD7853LBN	±1/2	6.5	N-24
AD7853AR	±1	18	R-24
AD7853BR	±1/2	18	R-24
AD7853LAR	±1	6.5	R-24
AD7853LBR	±1/2	6.5	R-24
AD7853LARS	±1	6.5	RS-24
AD7858AN	±1	18	N-24
AD7858BN	±1/2	18	N-24
AD7858LAN	±1	6.5	N-24
AD7858LBN	±1/2	6.5	N-24
AD7858AR	±1	18	R-24
AD7858BR	±1/2	18	R-24
AD7858LAR	±1	6.5	R-24
AD7858LBR	±1/2	6.5	R-24
AD7858LARS	±1	6.5	RS-24

*For outline information see Package Information section.

PRELIMINARY TECHNICAL DATA



NOTE: $t_{CONVERT}$ = 4.5 µs MAX, t_1 = 100 ns MIN, t_5 = 60 ns MAX, t_6 = 40 ns MIN, t_7 = 0 ns MIN.

Figure 2. AD7853 Timing Diagram (Typical Read or Write Operation)

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ABSOLUTE MAXIMUM RATINGS[1]

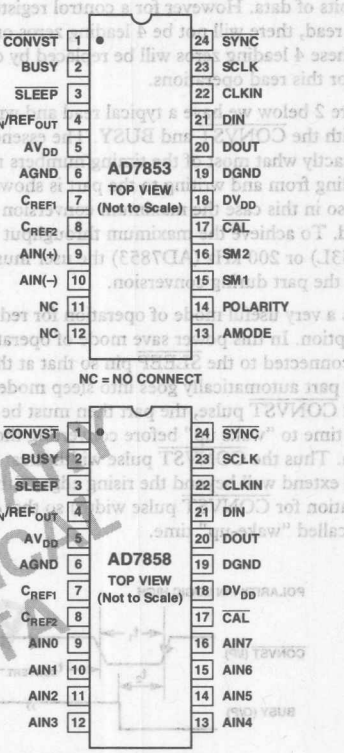
(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND ..... –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND .... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND ... –0.3 V to DV_{DD} + 0.3 V
REF_{IN}/REF_{OUT} to AGND ..... –0.3 V to AV_{DD} + 0.3 V
Input Current to any Pin except Supplies[2] ..... ±10 mA
Operating Temperature Range
  Commercial (A, B Versions) ..... –40°C to +85°C
  Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package Power, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 105°C/W
  θ_{JC} Thermal Impedance ..... 35°C/W
  Lead Temperature (Soldering, 10 sec) ..... +260°C
SOIC, SSOP Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance . 75°C/W (SOIC) 115°C/W (SSOP)
  θ_{JC} Thermal Impedance . 25°C/W (SOIC) 35°C/W (SSOP)
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

PIN CONFIGURATIONS

DIP, SOIC and SSOP



PRELIMINARY TECHNICAL DATA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7853/AD7858 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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AD7853 PIN DESCRIPTIONS

Pin	Mnemonic	Description
1	$\overline{\text{CONVST}}$	Convert start. Logic input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion.
2	BUSY	Busy output. The busy output goes high when conversion begins (note that BUSY goes high before $\overline{\text{CONVST}}$ goes high) and stays high until conversion is completed, at which time it goes low. BUSY is also used to indicate when the AD7853 has completed its on-chip calibration sequence.
3	$\overline{\text{SLEEP}}$	Sleep input/Low power mode. With this pin logic low all circuitry is powered down including the internal voltage reference. Calibration data is retained. With the pin logic high normal operation results.
4	REF_{IN}/REF_{OUT}	Reference input/output. This pin is connected to the internal reference via a resistor so that the reference voltage appears at this pin from the internal reference. An external reference can be applied to overdrive this pin. This pin is the reference source for the analog-to-digital converter, and the nominal reference voltage is 2.5 V but can be as high as AV_{DD} to give a larger reference for the analog-to-digital converter.
5	AV_{DD}	Analog positive supply voltage, +3.0 V to +5.5 V.
6	AGND	Analog ground. Ground reference for track/hold, reference and DAC.
7	C_{REF1}	Reference capacitor (0.1 μF multilayer ceramic). This external capacitor is used as a charge source for the internal DAC.
8	C_{REF2}	Reference capacitor (0.01 μF ceramic disc). This external capacitor is used in conjunction with the on-chip reference.
9	AIN(+)	Analog input. Positive input of the differential analog input.
10	AIN(–)	Analog input. Negative input of the differential analog input.
11, 12	NC	No Connect pins.
13	AMODE	Analog mode pin. This pin allows two different analog input ranges to be selected: A logic 0 selects range 0 to V_{REFIN} (i.e., AIN(+) – AIN(–) = 0 to V_{REFIN}). A logic 1 selects range $-V_{REFIN}/2$ to $+V_{REFIN}/2$ (i.e., AIN(+) – AIN(–) = $-V_{REFIN}/2$ to $+V_{REFIN}/2$).
14	POLARITY	This pin determines the edge of the serial clock (SCLK) on which the data is latched and transferred to the DOUT pin or latched from the DIN pin. Depending on the mode of operation then the output data can be clocked out on the rising or falling edge of the serial clock (SCLK). The data input is always latched on the rising edge of the serial clock (SCLK) regardless of the state of the POLARITY pin. It is best to see the timing diagrams for each of the operating modes to see which edges of the SCLK are critical for the output data and for the input data. All the timing diagrams are with the POLARITY pin high, so bringing the POLARITY pin low will reverse the edge of the SCLK that the data input is latched in on and will also reverse the edge of the SCLK that the output data is clocked out on.
15	SM1	Serial mode select pin. When this pin is high, the device is in its self-clocking mode; when it is low, the device is in its external clocking mode. This pin is used in conjunction with SM2 to give different modes of operation as shown in Table III.
16	SM2	Serial mode select pin. This pin is used in conjunction with the SM1 pin in order to give the different modes of operation as shown in Table III.
17	$\overline{\text{CAL}}$	Calibration input. A logic 0 on this input resets all logic and initiates a calibration on its rising edge. This input overrides all other internal operations.
18	DV_{DD}	Digital supply voltage, +3.0 V to +5.5 V.
19	DGND	Digital ground. Ground reference point for digital circuitry.
20	DOUT	Serial data output. The data output is supplied to this pin as a 16-bit serial word.
21	DIN	Serial data input. The data to be loaded to the control register is applied to this pin in serial form (16-bit word). This pin can act as an input pin or as a I/O pin depending on the mode the part is in (see Table III).
22	CLKIN	Master clock signal for the device (4 MHz). Sets the conversion and calibration times.
23	SCLK	Serial port clock. Logic input/output. The SCLK pin is configured as an input or output, dependent on the type of serial data transmission (self-clocking or external-clocking) that has been selected by the SM1 and SM2 pins. The data is latched on the rising or falling edge of SCLK depending on the POLARITY input logic level.
24	$\overline{\text{SYNC}}$	This pin can be an input level triggered active low (similar to a chip select in one case and to a frame sync in the other case) or an output (similar to a frame sync) pin depending on SM1 and SM2 (see Table III).

PRELIMINARY TECHNICAL DATA

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Pin	Mnemonic	Description
1	$\overline{\text{CONVST}}$	Convert start. Logic input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. If the $\overline{\text{CONVST}}$ is tied to the BUSY pin, then the part will go into sleep mode once conversion is complete and on the next conversion cycle the part needs to "wake-up" before a conversion can take place.
2	BUSY	Busy output. The busy output goes high when conversion begins (note that BUSY goes high before $\overline{\text{CONVST}}$ goes high) and stays high until conversion is completed, at which time it goes low. BUSY is also used to indicate when the AD7858 has completed its on-chip calibration sequence.
3	$\overline{\text{SLEEP}}$	Sleep input/low power mode. With this pin logic low all circuitry is powered down including the internal voltage reference. Calibration data is retained. With the pin logic high normal operation results.
4	REF_{IN}/REF_{OUT}	Reference input/output. This pin is connected to the internal reference via a resistor so that the reference voltage appears at this pin from the internal reference. An external reference can be applied to overdrive this pin. This pin is the reference source for the analog-to-digital converter and the nominal reference voltage is 2.5 V. However this pin can be taken as high as AV_{DD} to give a larger reference for the analog-to-digital converter.
5	AV_{DD}	Analog positive supply voltage, +3.0 V to +5.5 V.
6	AGND	Analog ground. Ground reference for track/hold, reference and DAC.
7	C_{REF1}	Reference capacitor (0.1 µF multilayer ceramic). This external capacitor is used as a charge source for the internal DAC.
8	C_{REF2}	Reference capacitor (0.01 µF ceramic disc). This external capacitor is used in conjunction with the on-chip reference.
9–16	AIN_1–AIN_8	Analog inputs. Eight analog inputs which can be used as eight single ended inputs (referenced to AGND) or four pseudo differential inputs where AIN_1 would be the positive input and AIN_2 would be the negative input and similarly for pairs AIN_3 AIN_4, AIN_5 AIN_6, and AIN_7 AIN_8. Pseudo differential means that the negative input cannot be taken below AGND. The selection of single ended or pseudo differential channels can be programmed via the SGL/$\overline{\text{DIFF}}$ bit in the control register, and also the channel to be selected for conversion can be programmed by the bits CHSLT0, CHSLT1, CHSLT2 in the control register.
17	$\overline{\text{CAL}}$	Calibration input. A logic 0 on this input resets all logic and initiates a calibration on its rising edge. This input overrides all other internal operations (see Figure 5).
18	DV_{DD}	Digital supply voltage, +3.0 V to +5.5 V.
19	DGND	Digital ground. Ground reference point for digital circuitry.
20	DOUT	Serial data output. The data output is supplied to this pin as a 16-bit serial word.
21	DIN	Serial data input. The data to be loaded to the control register is applied to this pin in serial form (16-bit word). This pin can act as an input pin or as a I/O pin depending on the mode the part is in (see Operating Modes).
22	CLKIN	Master clock signal for the device (4 MHz). Sets the conversion and calibration times.
23	SCLK	Serial port clock. The SCLK pin is configured as an input pin, and the user must provide 16 clock pulses at this pin for correct operation. The input data is latched on the rising edge of SCLK, and the output data is clocked out on the falling edge of SCLK (see timing diagrams).
24	$\overline{\text{SYNC}}$	The user must provide a frame sync signal at this pin and this signal is level triggered active low. This pin can be tied permanently low. When this input is high then the part will not read in the input data and output data will also be disabled.

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CONTROL/STATUS REGISTER

The power-up/default state of all bits in the control/status register is 0.

When writing to the control register, the first two bits are used in determining whether it is the control/status register or the calibration register that is being written to. A 11 in the first two bits ensures that it is the control/status register that you are writing to, and a 10 tells the part that it is the calibration register that is being written to. Also a 00 in the first two bits does not have any effect and a 01 is not allowed.

Bit	Mnemonic	Comment
0	STCAL	Start calibration bit. The type of calibration is determined by the setting of CALSLT1 and CALSLT2 and also whether it is a system or device calibration is set by the calibration mode (CALMD) bit. The default/Power up setting is for full device calibration (*i.e., calibration of DAC, Offset, and Gain*).
1 2	CALSLT1 CALSLT2	These two bits are for calibration control so that one can select the type of calibration that is to be performed depending on the value of the bits. A 00 will give a full DAC + Offset + Gain calibration, a 01 will give an Offset + Gain calibration, a 10 combination will give just an Offset calibration, and a 11 will give a Gain calibration. The calibration can be a system or device calibration depending on the setting of the calibration mode bit (see Table I).
3	CALMD	This is the calibration mode bit. A 0 here selects the device itself for calibration and a 1 selects a system calibration. The default/power-up state is a 0 so that it is a device calibration is selected unless this bit is changed (see Table I).
4	$\overline{\text{CONVST}}$	This is the conversion start bit. This is used for initiating a conversion start and it is also used in conjunction with system calibration as shown in the calibration timing diagram of Figure 6.
5	2/$\overline{3}$ MODE	The interface mode select bit. With this bit set to 1 the two-wire interface mode is enabled where DIN is used as an output as well as an input.
6 7	RDSLT1 RDSLT2	Theses two bits determine what data is going to be read from the part. ADC data will be read when the bits are set to 00, a 01 combination is used for test purposes and contains no useful user information, a 10 combination allows reading of the calibration register data, and a 11 ensures reading of control register data.
8	$\overline{\text{SLEEP}}$	This is the sleep bit which puts the device into sleep mode when 1 and the extent of the power down is determined by the power management bit.
9	PMGT	Power management bit. With this set to 0 then when put into sleep mode there will be a full power down whereas if set to 1 there will only be a selective power down.
10 11 12	*CHSLT0 *CHSLT1 *CHSLT2	(AD7858 only, should be 0 for AD7853.) These three bits are used to select the channel to be converted. With three bits then we can address all the eight channels. One should refer to Table II for the combinations of these three bits for different channel selections. The default selection is the pseudo differential mode with positive channel AIN_1 and negative channel AIN_2.
13	*SGL/$\overline{\text{DIFF}}$	(AD7858 only, should be 0 for AD7853) This is the bit which determines whether the input channels are in the single ended mode or in the pseudo differential mode. With this bit set to 1 then the singled ended mode is enabled. The default setting of this bit is 0 so that the input channels are in the pseudo differential mode. This bit is used in conjunction with the three channel selection bits CHSLT0, CHSLT1, CHSLT2 and one should refer to Table II for the bit combinations for different selections.
14	BUSY	This is the conversion/calibration busy bit which is read only and tells you when the part is finished conversion or calibration.

It is important to note that in writing to the control register it is Bit 15 (the MSB) that is the first bit in the data stream and not Bit 0, so that the first bit to be written to the control register will be Bit 15 then Bit 14, Bit 13 and so on down to Bit 0.

*These bits for the channel selection and the channel configuration are only valid for the AD7858 and for the AD7853 these bits must all be made 0 when writing to the control register.

PRELIMINARY TECHNICAL DATA

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Shown below are the tables for the different types of calibration and the different types of configurations for the analog inputs (AD7858 only) that can be selected in the control register.

Table I. Calibration Selection in the Control Register (AD7853/AD7858)

CALSLT2	CALSLT1	CALMD	Calibration Type
0	0	0	A full internal calibration is initiated where the internal DAC is calibrated then the Internal Offset Error is calibrated out and finally the Internal Gain Error is calibrated out.
0	0	1	A full system calibration is initiated here where firstly the Internal DAC is calibrated and then the System Offset Error is calibrated out and finally the System Gain Error is calibrated out.
0	1	0	Here the Internal Offset Error is calibrated out and then the Internal Gain Error is calibrated out.
0	1	1	Here the System Offset Error is calibrated out and then the System Gain Error is calibrated out.
1	0	0	This calibrates out the Internal Offset Error only.
1	0	1	This calibrates out the System Offset Error only.
1	1	0	This calibrates out the Internal Gain Error only.
1	1	1	This calibrates out the System Gain Error only.

NOTE
There is more information on the calibration features of the part under the Calibration section of this data sheet.

Table II. Multichannel Selection in the Control Register for the AD7858

SGL/$\overline{DIFF}$	CHSLT2	CHSLT1	CHSLT0	CH(+)	CH(–)
0	0	0	0	AIN_1	AIN_2
0	0	0	1	AIN_3	AIN_4
0	0	1	0	AIN_5	AIN_6
0	0	1	1	AIN_7	AIN_8
0	1	0	0	AIN_2	AIN_1
0	1	0	1	AIN_4	AIN_3
0	1	1	0	AIN_6	AIN_5
0	1	1	1	AIN_8	AIN_7
1	0	0	0	AIN_1	AGND
1	0	0	1	AIN_3	AGND
1	0	1	0	AIN_5	AGND
1	0	1	1	AIN_7	AGND
1	1	0	0	AIN_2	AGND
1	1	0	1	AIN_4	AGND
1	1	1	0	AIN_6	AGND
1	1	1	1	AIN_8	AGND

NOTE
The four selection bits are in the control register.

PRELIMINARY TECHNICAL DATA

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TERMINOLOGY[1]

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (*which is AIN(+) = AIN(–) –1/2 LSB in unipolar mode (AD7853/AD7858), and AIN(+) = AIN(–) –V_{REF}/2 – 1/2 LSB in bipolar mode (AD7853 only)*), a point 1/2 LSB below the first code transition (00 . . . 000 to 00 . . . 001) and full scale (*which is AIN(+) = AIN(–) + V_{REF} + 1/2 LSB in unipolar range (AD7853/AD7858), and AIN(+) = AIN(–) +V_{REF}/2 + 1/2 LSB in bipolar mode (AD7853 only)*), a point 1/2 LSB above the last code transition (11 . . . 110 to 11 . . . 111).

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Unipolar Offset Error
This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal AIN(+) voltage (AIN(–) + 1/2 LSB) when operating in the unipolar mode.

Positive Full-Scale Error
This applies to the unipolar and bipolar modes and is the deviation of the last code transition (11 . . . 110 to 11 . . . 111 (*for unipolar mode (AD7853/AD7858)*) and 01 . . . 110 to 01 . . . 111 (*for bipolar mode (AD7853 only)*) from the ideal (AIN(+) = AIN(–) + Full Scale – 1.5 LSB) after the offset error (*unipolar offset error or bipolar offset error*) has been adjusted out.

Negative Full-Scale Error
This applies to the bipolar mode only and is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal (AIN(+) = AIN(–) – V_{REF}/2 + 0.5 LSB (*bipolar mode (AD7853 only)*)).

Bipolar Zero Error
This is the deviation of the midscale transition (all 0s to all 1s) from the ideal AIN(+) voltage (AIN(–) – 1/2 LSB).

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 1 kHz signal to the other seven inputs and determining how much that signal is attenuated in the channel of interest. The figure given is the worst case for all channels.

Track/Hold Acquisition Time
Track/hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (*the point at which the track/hold returns into track mode*). It also applies to a situation where a change in the selected input channel takes place (AD7858 only) or where there is a step input change on the input voltage applied to the selected V_{IN} input of the AD7853/AD7858. It means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a channel change/step input change to V_{IN} before starting another conversion, to ensure the part operates to specification.

[1]AIN(–) refers to the negative input of the pseudo differential input pairs or to AGND for the AD7858 depending on the channel configuration, and AIN(–) refers to the negative input for the AD7853.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f_S/2), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7853, it is defined as:

$$THD\ (dB) = 20 \log \sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)/V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to f_S/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7853 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

PRELIMINARY TECHNICAL DATA

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No.	SM1	SM2	SYNC	DIN	DOUT	SCLK	Comment
1 (AD7853/AD7858)	0	0	I/P[1]	I/O	(O/P)[2]	I/P	**TWO-WIRE MODE (8051).** In this mode of operation the user must supply the serial clock (SCLK with a total of 16 clock cycles). This mode can only be entered by programming the interfaced mode select (2/3 MODE) bit in the control register. The SYNC pin must also be provided by the user; it is level triggered and can be tied low permanently in this mode. The DIN pin is used for inputting the data (in serial form) as well as providing the output data in serial form.
2 (AD7853/AD7858)	0	0	I/P[1]	I/P	O/P	I/P	**THREE-WIRE MODE (SPI).** In this mode of operation the user must supply the frame sync signal (SYNC) and serial clock (SCLK with a total of 16 clock cycles). This is the default mode. Here the DOUT pin is used for the output data and DIN pin is used for the input data only.
3 (AD7853 Only)	0	1	I/P[3]	I/P	O/P	I/P	**DSP MASTER MODE.** In this mode of operation a frame sync input is needed at the SYNC pin and a serial clock SCLK is needed with a continuous clock or 16 clock cycles from when the SYNC goes low.
4 (AD7853 Only)	1	0	O/P[3]	I/P	O/P	O/P[4]	**DSP SLAVE MODE.** This mode of operation is where the part provides a noncontinuous serial clock (SCLK with a total of 16 clock cycles) and the frame sync (SYNC).
5 (AD7853 Only)	1	1	O/P[3]	I/P	O/P	O/P[5]	This another DSP slave mode of operation where the part provides a **CONTINUOUS CLOCK (TMS)** signal (SCLK) and frame sync output (SYNC).

NOTES
I/P: Input, I/O: Input/Output, O/P: Output
[1]SYNC pin is an input pin which is level triggered active low.
[2]Output data may appear at the DOUT pin but the pin is not used and should be left unconnected.
[3]A frame sync signal (input or output) which is edge triggered (high to low).
[4]Noncontinuous serial clock.
[5]Continuous serial clock.

PRELIMINARY TECHNICAL DATA

OPERATING SETUPS

From Table III it is clear that all the interface modes apply to the AD7853 (*and AD7853L*) but that only interface modes 1 and 2 apply to the AD7858 (*and AD7858L*). In all the timing diagrams the reference to the Polarity, SM1 and SM2 pins only applies to the AD7853. Next, before describing the operating modes in more detail, the different arrangements for reading, writing and starting conversions will be described.

The most useful arrangement is where the writing and reading takes place during conversion as shown in Figure 3. This allows for the maximum throughput rate (200 kHz AD7853/AD7858, 100 kHz AD7853L/AD7858L). It is clear from Figure 3 that the read on the DOUT pin is for the previous conversion and the write on the DIN pin is for the next conversion.

The arrangement in Figure 3 is only valid for the three-wire mode and the DSP Master Mode (AD7853 only) of operation. The different arrangements for the other modes of operation are shown under the respective operating mode section.

There are other less common arrangements that can be used. These involve initiating a write in synchronization with the start of conversion and then waiting for the conversion to be complete before reading from the part. The reverse of this can also be used where a read is initiated in synchronization with the start of conversion, and writing to the part once the conversion is complete. Alternatively the conversion can be initiated by setting the CONVST bit in the control register to 1 when writing to the part. These arrangements are similar to the arrangements shown in Figures 4c, 4d, and 4e for the two-wire mode of operation, but both the reading and writing would not take place on the DIN pin.

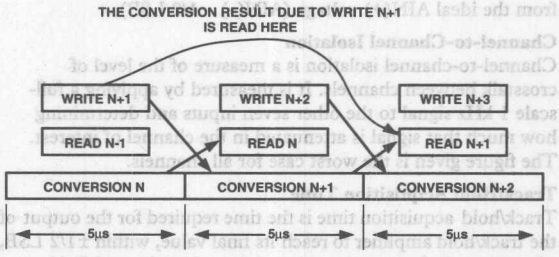

Figure 3.

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Timing

The two timing figures t_3 and t_{10} need to be explained due to their complexity. Theses times apply to Figures 4d, 4e, 5a, 5b, and 6 only where the $\overline{SYNC}$ and the SCLK are both inputs to the part. For Figure 8 where $\overline{SYNC}$ and SCLK are outputs from the part, t_{3A} and t_{10A} are used and these are explained under the DSP Slave Mode section.

Taking t_3 first and a continuous SCLK situation (*which only applies for Figures 4d, 5a and 6*), t_3 has a minimum spec of 60 ns so that the part will have enough time to prepare for the first SCLK edge. The max spec for t_3 (*which only applies with a continuous SCLK*) is 0.4 t_{SCLK} which ensures that the $\overline{SYNC}$ does not go low before the rising edge A of the dashed SCLK (*shown in the timing diagrams*). This ensures that the part does not clock in an incorrect data bit from the DIN pin as DB15.

Next take the time t_{10} and a continuous SCLK situation (*again this only applies to Figures 4d, 5a and 6*), t_{10} has a minimum spec of 30 ns which is so that the part will have enough time to prepare for the rising edge of $\overline{SYNC}$. The max spec for t_{10} (*which only applies with a continuous SCLK*) is 0.4 t_{SCLK} which ensures that the SYNC goes high before the falling edge B of the dashed SCLK (*shown in the timing diagrams*). This ensures that the part does not offset the next write sequence and also so that an extra bit will not be clocked out onto the DOUT pin.

Both t_3 and t_{10} only have a minimum spec when there is a noncontinuous SCLK to allow the part enough time to prepare for the following edge of the relevant signal. There is no maximum spec for t_3 and t_{10} as there is no danger of getting an extra clock edge to upset the operation of the part.

Two-Wire Mode (AD7853 and AD7858)

The different setup arrangements for reading and writing to the part in the two-wire mode are shown in Figures 4a, 4b, and 4c. The read and writing takes place on the DIN line and the conversion start take place on the $\overline{CONVST}$ line. (Note that the write to the part must set the $2/\overline{3}$ MODE bit in the control register to 1 for all cases 4a, 4b, 4c. Also the conversion can be started by setting the $\overline{CONVST}$ bit in the control register to 1, and so the $\overline{CONVST}$ pin does not need to be used in cases 4b and 4c.)

In Figure 4a a write is initiated in synchronization with the start of a conversion cycle (*thus with this setup the write cannot initiate the start of conversion via the control register, but the $2/\overline{3}$ MODE bit must be set to 1 in all the write sequences to the part*). Then after the conversion is finished, a read operation is started and the data read here is from conversion N-1 and does not correspond to the previous write. You must wait until the next conversion (conversion N) before reading data corresponding to the initial write (write N). The very first read from the part here will not contain a result from a conversion under the two-wire mode due to the fact that the write sequence is one sequence behind the conversion sequence. The time for the read and write operation given is for a serial clock of 4 MHz (*2 MHz is max for L versions*), but is still only an approximate time. Thus the 9.5 µs shown is the fastest throughput time for the two-wire interface operating mode which corresponds to a frequency of 105 kHz (*52 kHz for L versions*).

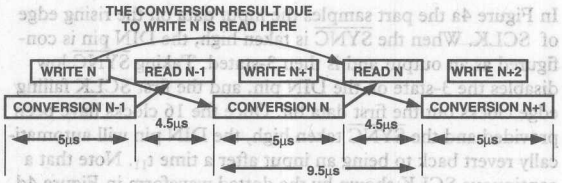

Figure 4a.

Figure 4b is the same as Figure 4a except that the conversion is initiated in synchronizations with a read operation instead of a write operation. Again the data read from the part is one conversion behind the corresponding write operation. (The *write to the part must enable the two-wire mode and may also initiate a conversion, and so the hardware* $\overline{CONVST}$ *signal is not needed.*)

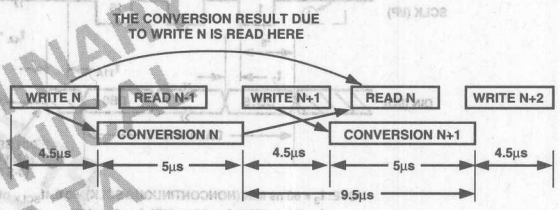

Figure 4b.

Figure 4c shows another way of operating the part in the two-wire mode where getting the fastest throughput rate is not essential. It is the most basic way to operate the part. A write is initiated (*which enables the two-wire mode and may also initiate the start of conversion*). After this a conversion is started, and when conversion is complete, the result is read back. From these diagrams it can be seen that the part cannot be run at its max throughput rate in the two-wire mode due to the time taken to read and write data on the same pin.

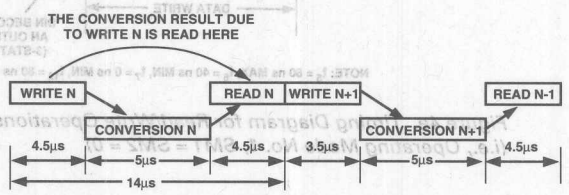

Figure 4c.

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Below in Figure 4d and in Figure 4e are the timing diagrams for operating mode No. 1 in Table I where we are in the 2-wire interface mode. Here the DIN pin is used for both input and output as shown. The $\overline{SYNC}$ input is level triggered active low and can be pulsed (Figure 4d) or can be constantly low (Figure 4e).

In Figure 4a the part samples the input data on the rising edge of SCLK. When the $\overline{SYNC}$ is taken high, the DIN pin is configured as an output and is then 3-stated. Taking $\overline{SYNC}$ low disables the 3-state on the DIN pin, and the first SCLK falling edge clocks out the first data bit. Once the 16 clocks have been provided and the $\overline{SYNC}$ taken high, the DIN pin will automatically revert back to being an input after a time t_{11}. Note that a continuous SCLK shown by the dotted waveform in Figure 4d can be used provided that the $\overline{SYNC}$ is low for only 16 clock pulses in each of the read and write cycles.

In Figure 4e the $\overline{SYNC}$ line is tied low permanently, and this results in a different timing arrangement for the DIN pin. The difference between $\overline{SYNC}$ being tied low and being pulsed is that the DIN pin will never be 3-stated in this mode, and it is also the last rising edge of the SCLK that causes the DIN pin to go from being an input to an output and back to an input pin. Here a continuous SCLK cannot be used as the $\overline{SYNC}$ is tied low permanently.

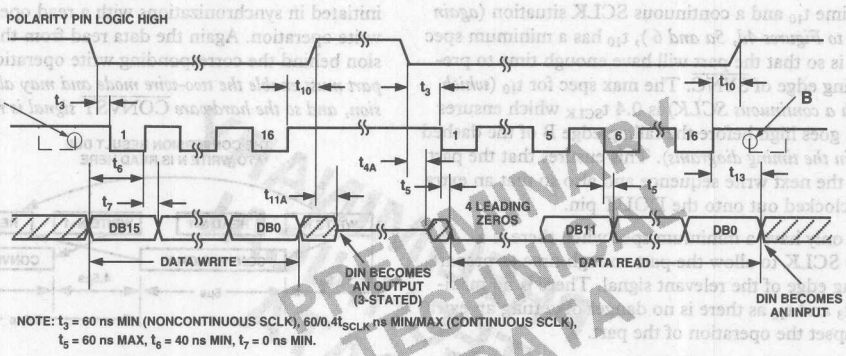

Figure 4d. Timing Diagram for Read/Write Operations with DIN as an Input/Output (i.e., Operating Mode No. 1, SM1 = SM2 = 0)

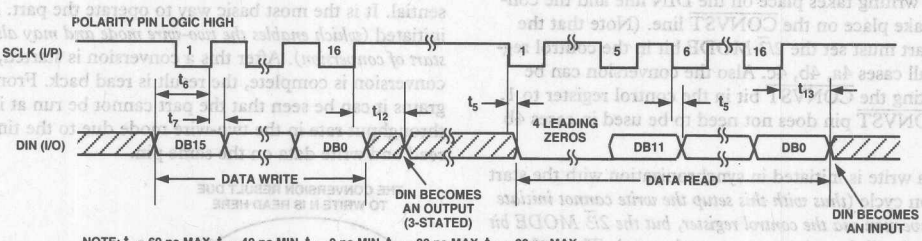

Figure 4e. Timing Diagram for Read/Write Operations with DIN as an Input/Output and $\overline{SYNC}$ Input Tied Low (i.e., Operating Mode No. 1, SM1 = SM2 = 0)

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Three-Wire Mode (AD7853 and AD7858)

In Figure 5a and Figure 5b we have the timing diagrams for operating mode No. 2 in Table I which is the three-wire interface mode. Here the $\overline{SYNC}$ input is active low and can be pulsed (Figure 5a) or can be constantly low, (Figure 5b). If $\overline{SYNC}$ is constantly low, the serial clock input (SCLK) must supply 16 clock pulses for the part to operate correctly; otherwise with a pulsed $\overline{SYNC}$ input, a continuous SCLK can be used provided $\overline{SYNC}$ is low for only 16 clock cycles. In Figure 5a the $\overline{SYNC}$ going low disables the 3-state on the DOUT pin. The first falling edge of the SCLK after the $\overline{SYNC}$ going low clocks out the first leading zero on the DOUT pin. The DOUT pin is 3-stated again a time t_{11} after the $\overline{SYNC}$ goes high. With the DIN pin the data input has to be set up a time t_6 before the SCLK rising edge as the part samples the input data on the SCLK rising edge.

Figure 5b shows the timing diagram for the three-wire interface mode where the $\overline{SYNC}$ input has been tied permanently low. The only difference between this timing diagram and the one in Figure 5a is that the DOUT pin is never 3-stated since the $\overline{SYNC}$ input is never brought high. Also the LSB of the output data will remain on the DOUT pin until the next read cycle where the first SCLK falling edge will clock out the first leading zero of the next conversion.

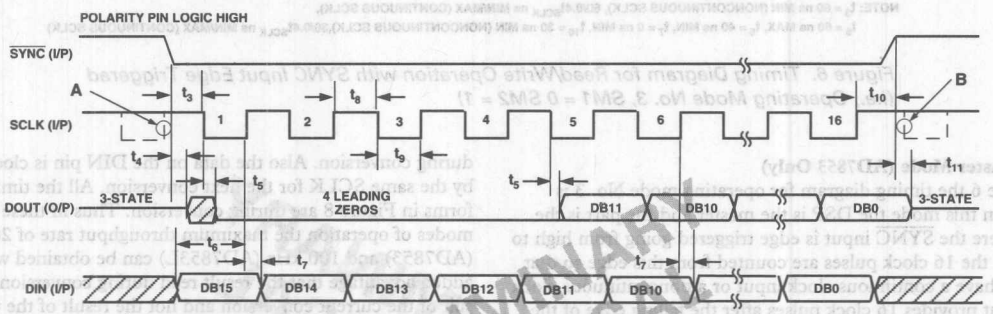

Figure 5a. Timing Diagram for Read/Write Operations with DIN as an Input and DOUT as Output and $\overline{SYNC}$ Input Pulsed (i.e., Operating Mode No. 2, SM1 = SM2 = 0)

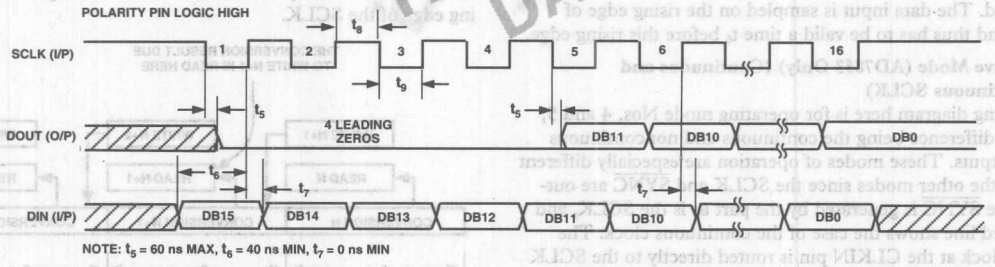

Figure 5b. Timing Diagram for Read/Write Operations with DIN as an Input and DOUT as Output and $\overline{SYNC}$ Input Tied Low (i.e., Operating Mode No. 2, SM1 = SM2 = 0)

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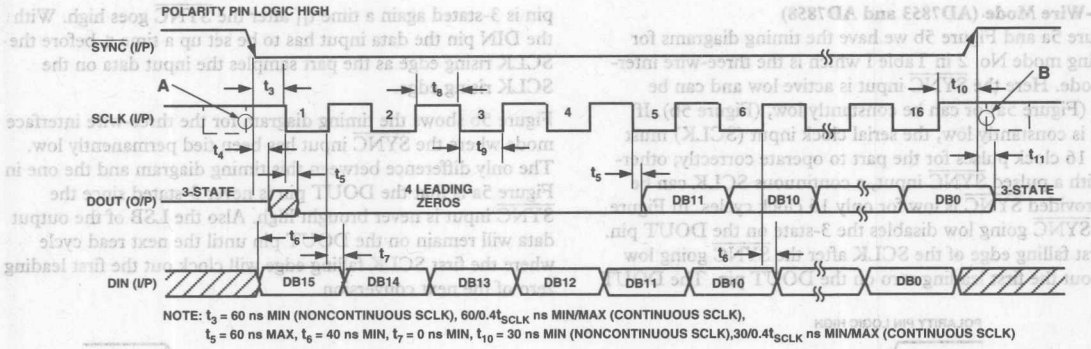

Figure 6. Timing Diagram for Read/Write Operation with $\overline{SYNC}$ Input Edge Triggered (i.e., Operating Mode No. 3, SM1 = 0 SM2 = 1)

DSP Master Mode (AD7853 Only)

In Figure 6 the timing diagram for operating mode No. 3 is shown. In this mode the DSP is the master and the part is the slave. Here the $\overline{SYNC}$ input is edge triggered going from high to low, and the 16 clock pulses are counted from this edge so that you can have a continuous clock input or a noncontinuous clock input that provides 16 clock pulses after the falling edge of the $\overline{SYNC}$ input. If a continuous clock is being used, the $\overline{SYNC}$ must go high after 16 clock pulses to disable the effect of any more clocks. The falling edge of $\overline{SYNC}$ disables the 3-state on the DOUT pin, and the data is clocked out on the falling edge of SCLK. Once $\overline{SYNC}$ goes high, the 3-state on the DOUT pin is enabled. The data input is sampled on the rising edge of SCLK and thus has to be valid a time t_6 before this rising edge.

DSP Slave Mode (AD7853 Only) (Continuous and Noncontinuous SCLK)

The timing diagram here is for operating mode Nos. 4 and 5, the only difference being the continuous and noncontinuous clock outputs. These modes of operation are especially different from all the other modes since the SCLK and $\overline{SYNC}$ are outputs. The $\overline{SYNC}$ is generated by the part as is the SCLK, and the dotted line shows the case of the continuous clock. The master clock at the CLKIN pin is routed directly to the SCLK pin for operating mode No. 5 (Continuous SCLK), and the CLKIN input is gated with the $\overline{SYNC}$ to give the SCLK in operating mode No. 4 (Noncontinuous SCLK).

The most important point about these two operation modes is that the result of the current conversion is clocked out during the same conversion, and a write to the part during this conversion is for the next conversion. The arrangement is shown in Figure 7. First the conversion is initiated with the $\overline{CONVST}$ signal going low, and then when part is ready, the $\overline{SYNC}$ will go low and the SCLK will clock out the data on the DOUT pin during conversion. Also the data on the DIN pin is clocked in by the same SCLK for the next conversion. All the timing waveforms in Figure 8 are during conversion. Thus in these two modes of operation the maximum throughput rate of 200 kHz (AD7853) and 100 kHz (AD7853L) can be obtained with the added advantage that the result read during conversion is the result of the current conversion and not the result of the previous as in the other modes of operation.

In these modes the part is now the master and the DSP is the slave. The output data is clocked out from the part to the DOUT pin on the rising edge of SCLK, and the input data to the part on the DIN pin is also clocked in to the part on the rising edge of the SCLK.

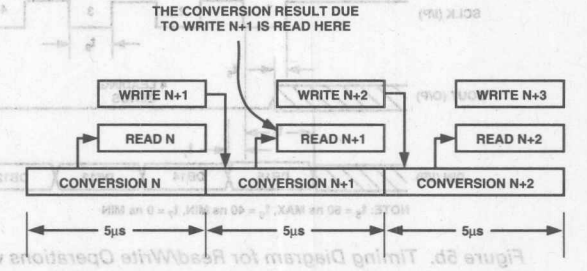

Figure 7.

Some of the timing numbers for the timing diagram of Figure 8 need explaining due to their complexity. First, t_{3A} has only a min spec and no max spec as the part will ensure that the $\overline{SYNC}$

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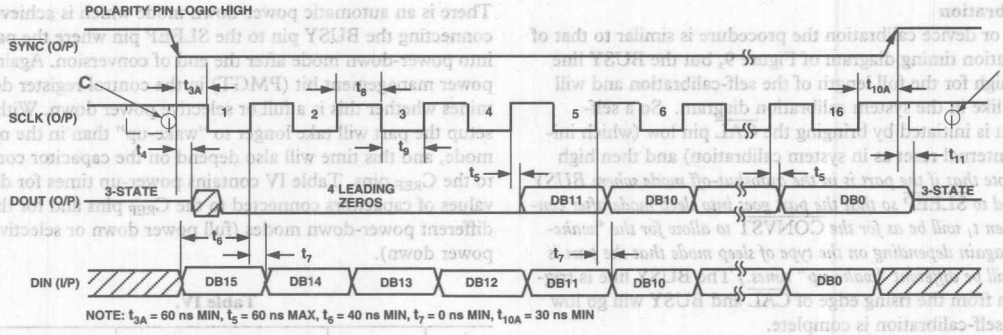

Figure 8. Timing Diagram for Read/Write with $\overline{SYNC}$ Output and SCLK Output (Continuous and Noncontinuous) (i.e., Operating Mode Nos. 4 and 5, SM1 = 1, SM2 = 1 and 0)

goes low after the rising edge C of the dashed SCLK in Figure 8 (if there is a continuous SCLK) so that the part will not clock in an incorrect data bit from the DIN pin as DB15. The other time is t_{10A} which again only has a min spec and no max spec as the part will again ensure that the SYNC has gone high before the rising edge D of the dashed SCLK in Figure 8 (if there is a continuous SCLK). This ensures both that the SCLK will not clock in an extra bit from the DIN pin which would offset the next write sequence, and also that another bit will not be clocked out of the part onto the DOUT pin.

CALIBRATION

There are two main calibration features on the AD7853/AD7858; these are a self or device calibration and a system calibration. For both system and self-calibrations there are a number of different types of calibration that can be selected depending on the setting of various bits in the control register. These options are covered by Table I.

There are a number of points that are useful to state before describing the procedure for initiating a system calibration. The first point is that the maximum calibration range is approximately ±3% of V_{REF} for both the system offset and gain errors. Also, if the errors are outside this range, the system calibration algorithm will reduce the errors as much as the trim range allows. Large system errors can be reduced in an incremental fashion by doing multiple system (gain + offset) calibrations. This is possible due to the way that the system calibration algorithm works. In bipolar mode (*AD7853 only*) it is the midscale error and the positive full-scale error that are adjusted; in unipolar mode it is the zero-scale error and the positive full-scale error that are adjusted.

System Calibration

The calibration timing diagram in Figure 9 is for a system calibration where the falling edge of $\overline{CAL}$ initiates an internal reset before starting a calibration. (*Note that if the part is in the autoshut-off mode where BUSY is connected to* $\overline{SLEEP}$ *so that the part goes into sleep mode after conversion, then* t_1 *will be as for the* $\overline{CONVST}$ *to allow for the "wake-up" time; again depending on the type of sleep mode that the part is in, there will be different "wake-up" times.*) Then the rising edge of $\overline{CAL}$ starts calibration of the internal DAC. Then if the control register is set for a full calibration, the $\overline{CONVST}$ must be used also. The full-scale system voltage should be applied to the analog input pins from the start of calibration. Then the offset voltage due to the system must be present on the AIN pin (after the full-scale system offset is completed) for a minimum setup time (t_{SETUP}) of 100 ns before the rising edge of the $\overline{CONVST}$.

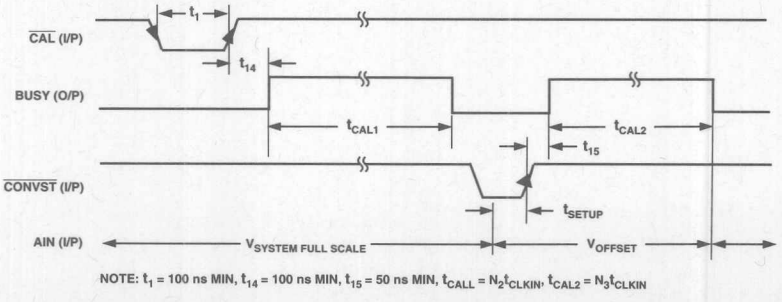

Figure 9. Calibration Timing Diagram for Full System Calibration

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not pulse like in the system calibration diagram. So a self-calibration is initiated by bringing the $\overline{CAL}$ pin low (which initiates an internal reset as in system calibration) and then high again. (*Note that if the part is in the autoshut-off mode where BUSY is connected to $\overline{SLEEP}$ so that the part goes into sleep mode after conversion, then t_1 will be as for the $\overline{CONVST}$ to allow for the "wake-up" time; again depending on the type of sleep mode that the part is in, there will be different "wake-up" times.*) The BUSY line is triggered high from the rising edge of $\overline{CAL}$ and BUSY will go low when the self-calibration is complete.

POWER-DOWN MODES

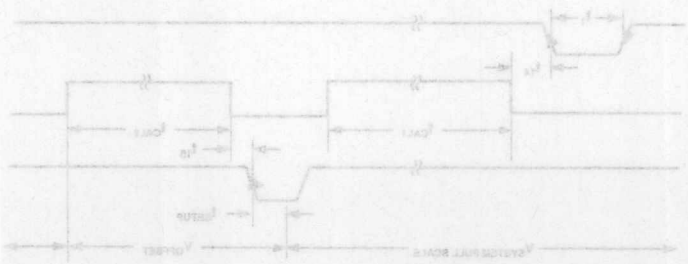
There are two power-down modes on the part, one being a full power down, the other a selective power down where only certain internal circuitry is powered down. The advantage of the selective power down is that the part will not require as much time to "wake up" as for the full power down. The type of power down is selected by programming the power management bit (PMGT) in the control register, 0 for a full power down and 1 for a selective power down.

power management bit (PMGT) in the control register determines whether this is a full or selective power down. With this setup the part will take longer to "wake-up" than in the normal mode, and this time will also depend on the capacitor connected to the C_{REF} pins. Table IV contains power-up times for different values of capacitors connected to the C_{REF} pins and for the two different power-down modes (full power down or selective power down).

Table IV.

C_{REF1} (μF)	C_{REF2} (μF)	Power-Down Mode	Power-Up Delay (sec)
0.1	0.01	Full	TBD
0.1	0.01	Selective	TBD
1.0	0.1	Full	TBD
1.0	0.1	Selective	TBD

PRELIMINARY TECHNICAL DATA



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LC²MOS Complete, 12-Bit, 100 kHz, Sampling ADCs

AD7870/AD7870A/AD7875/AD7876

FEATURES

Complete Monolithic 12-Bit ADC with:
- 2 µs Track/Hold Amplifier
- 8 µs A/D Converter
- On-Chip Reference
- Laser-Trimmed Clock
- Parallel, Byte and Serial Digital Interface

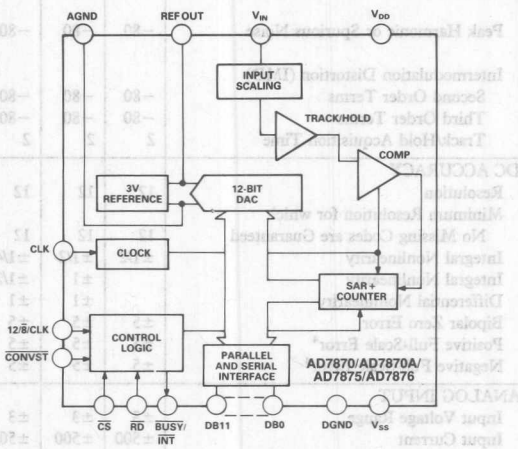
72 dB SNR at 10 kHz Input Frequency (AD7870, AD7870A, AD7875)

57 ns Data Access Time

Low Power −60 mW typ

Variety of Input Ranges:
- ±3 V for AD7870/AD7870A
- 0 to +5 V for AD7875
- ±10 V for AD7876

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7870/AD7870A/AD7875/AD7876 is a fast, complete, 12-bit A/D converter. It consists of a track/hold amplifier, 8 µs successive-approximation ADC, 3 V buried Zener reference and versatile interface logic. The ADC features a self-contained internal clock which is laser trimmed to guarantee accurate control of conversion time. No external clock timing components are required; the on-chip clock may be overridden by an external clock if required.

The parts offer a choice of three data output formats: a single, parallel, 12-bit word; two 8-bit bytes, or serial data. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

All parts operate from ±5 V power supplies. The AD7870 and AD7876 accept input signal ranges of ±3 V and ±10 V, respectively, while the AD7875 accepts a unipolar 0 to +5 V input range. The parts can convert full power signals up to 50 kHz.

The AD7870/AD7870A/AD7875/AD7876 feature dc accuracy specifications such as linearity, full-scale and offset error. In addition, the AD7870/AD7870A and AD7875 are fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

The parts are fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low-power CMOS logic. The parts are available in a 24-pin, 0.3 inch-wide, plastic or hermetic dual-in-line package (DIP). The AD7870/AD7870A and AD7875 are available in a 28-pin plastic leaded chip carrier (PLCC), while the AD7876 is available and in a 24-pin small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit ADC on a Chip.
   The AD7870/AD7870A/AD7875/AD7876 provides all the functions necessary for analog-to-digital conversion and combines a 12-bit ADC with internal clock, track/hold amplifier and reference on a single chip.
2. Dynamic Specifications for DSP Users.
   The AD7870/AD7870A and AD7875 are fully specified and tested for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion.
3. Fast Microprocessor Interface.
   Data access times of 57 ns make the parts compatible with modern 8- and 16-bit microprocessors and digital signal processors. Key digital timing parameters are tested and guaranteed over the full operating temperature range.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7870/AD7870A/AD7875/AD7876—SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2.5 MHz external, unless otherwise stated. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	AD7870/AD7870A J, A[1]	K, B[1]	L, C[1]	S[1]	T[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]							
Signal to Noise Ratio[3] (SNR)							
@ +25°C	70	70	72	69	69	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{min} to T_{max}	70	70	71	69	69	dB min	Typically 71.5 dB for 0 < V_{IN} < 50 kHz
Total Harmonic Distortion (THD)	−80	−80	−80	−78	−78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 < V_{IN} < 50 kHz
Peak Harmonic or Spurious Noise	−80	−80	−80	−78	−78	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 < V_{IN} < 50 kHz
Intermodulation Distortion (IMD)							
Second Order Terms	−80	−80	−80	−78	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	−80	−80	−78	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	2	2	2	µs max	
DC ACCURACY							
Resolution	12	12	12	12	12	Bits	
Minimum Resolution for which							
No Missing Codes are Guaranteed	12	12	12	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	±1/4	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1/2		±1	LSB max	
Differential Nonlinearity		±1	±1		±1	LSB max	
Bipolar Zero Error	±5	±5	±5	±5	±5	LSB max	
Positive Full-Scale Error[4]	±5	±5	±5	±5	±5	LSB max	
Negative Full-Scale Error[4]	±5	±5	±5	±5	±5	LSB max	
ANALOG INPUT							
Input Voltage Range	±3	±3	±3	±3	±3	Volts	
Input Current	±500	±500	±500	±500	±500	µA max	
REFERENCE OUTPUT							
REF OUT @ +25°C	2.99	2.99	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	3.01	3.01	V max	
REF OUT Tempco	±60	±60	±35	±60	±35	ppm/°C max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	±1	±1	±1	±1	±1	mV max	Reference Load Current Change (0–500 µA) Reference Load Should Not Be Changed During Conversion.
LOGIC INPUTS							
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current (12/8/CLK Input Only)	±10	±10	±10	±10	±10	µA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	10	10	pF max	
LOGIC OUTPUTS							
Output High Voltage, V_{OH}	4.0	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0							
Floating-State Leakage Current	±10	±10	±10	±10	±10	µA max	
Floating-State Output Capacitance[5]	15	15	15	15	15	pF max	
CONVERSION TIME							
External Clock (f_{CLK} = 2.5 MHz)	8	8	8	8	8	µs max	
Internal Clock	7/9	7/9	7/9	7/9	7/9	µs min/µs max	
POWER REQUIREMENTS							
V_{DD}	+5	+5	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	13	13	mA max	Typically 8 mA
I_{SS}	6	6	6	6	6	mA max	Typically 4 mA
Power Dissipation	95	95	95	95	95	mW max	Typically 60 mW

NOTES

[1]Temperature ranges are as follows: J, K, L Versions; 0 to +70°C: A, B, C Versions; −25°C to +85°C: S, T Versions; −55°C to +125°C. AD7870A has only J Version.

[2]V_{IN} (pk–pk) = ±3 V.

[3]SNR calculation includes distortion and noise components.

[4]Measured with respect to internal reference and includes bipolar offset error.

[5]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

Parameter	AD7875/AD7876 K, B[1]	L, C[1]	T[1]	Units	Test Conditions/Comments
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1/2	±1	LSB max	
T_{min} to T_{max} (AD7875 Only)	±1	±1	±1	LSB max	
T_{min} to T_{max} (AD7876 Only)	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	−1, +1.5	LSB max	
Unipolar Offset Error (AD7875 Only)	±5	±5	±5	LSB max	
Bipolar Zero Error (AD7876 Only)	±6	±2	±6	LSB max	
Full-Scale Error at +25°C[2]	±8	±8	±8	LSB max	Typical full-scale error is ±1 LSB
Full-Scale TC[2]	±60	±35	±60	ppm/°C max	Typical TC is ±20 ppm/°C
Track/Hold Acquisition Time	2	2	2	µs max	
DYNAMIC PERFORMANCE[3] (AD7875 ONLY)					
Signal-to-Noise Ratio[4] (SNR)					
@ +25°C	70	72	69	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{min} to T_{max}	70	71	69	dB min	Typically 71.5 dB for $0 < V_{IN} < 50$ kHz
Total Harmonic Distortion (THD)	−80	−80	−78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically −86 dB for $0 < V_{IN} < 50$ kHz
Peak Harmonic or Spurious Noise	−80	−80	−78	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz Typically −86 dB for $0 < V_{IN} < 50$ kHz
Intermodulation Distortion (IMD)					
Second Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
ANALOG INPUT					
AD7875 Input Voltage Range	0 to +5	0 to +5	0 to +5	Volts	
AD7875 Input Current	500	500	500	µA max	
AD7876 Input Voltage Range	±10	±10	±10	Volts	
AD7876 Input Current	±600	±600	±600	µA max	
REFERENCE OUTPUT					
REF OUT @ +25°C	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	V max	
REF OUT Tempco	±60	±35	±60	ppm/°C max	Typical Tempco is ±20 ppm/°C
Reference Load Sensitivity (ΔREF OUT/ΔI)	−1	−1	−1	mV max	Reference Load Current Change (0–500 µA) Reference Load Should Not Be Changed During Conversion.
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current (12/8/CLK Input Only)	±10	±10	±10	µA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	10	10	10	µA max	
Floating-State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME					
External Clock (f_{CLK} = 2.5 MHz)	8	8	8	µs max	
Internal Clock	7/9	7/9	7/9	µs min/µs max	
POWER REQUIREMENTS	As per AD7870/AD7870A				

NOTES

[1]Temperature ranges are as follows: AD7875: K, L Versions, 0 to +70°C; B, C Versions, −40°C to +85°C; T Version, −55°C to +125°C. AD7876: B, C Versions, −40°C to +85°C; T Version, −55°C to +125°C.

[2]Includes internal reference error and is calculated after unipolar offset error (AD7875) or bipolar zero error (AD7876) has been adjusted out. Full-scale error refers to both positive and negative full-scale error for the AD7876.

[3]Dynamic performance parameters are not tested on the AD7876 but these are typically the same as for the AD7875.

[4]SNR calculation includes distortion and noise components.

[5]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

Parameter	(J, K, L, A, B, C Versions)	(S, T Versions)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 1)
t_3	**60**	**75**	ns min	$\overline{RD}$ Pulse Width
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 1)
t_5	70	70	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_6[3]	**57**	**70**	ns max	Data Access Time after $\overline{RD}$
t_7[4]	5	**5**	ns min	Bus Relinquish Time after $\overline{RD}$
	50	**50**	ns max	
t_8	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	100	100	ns min	$\overline{SSTRB}$ to SCLK Falling Edge Setup Time
t_{11}[5]	370	370	ns min	SCLK Cycle Time
t_{12}[6]	135	150	ns max	SCLK to Valid Data Delay. C_L=35 pF
t_{13}	20	20	ns min	SCLK Rising Edge to $\overline{SSTRB}$
	100	100	ns max	
t_{14}	10	10	ns min	Bus Relinquish Time after SCLK
	100	100	ns max	
t_{15}	60	60	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 2)
t_{16}	120	120	ns max	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay
t_{17}	200	200	ns min	Data Setup Time Prior to $\overline{BUSY}$
t_{18}	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 2)
t_{19}	0	0	ns min	HBEN to $\overline{CS}$ Setup Time
t_{20}	0	0	ns min	HBEN to $\overline{CS}$ Hold Time

NOTES

[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and $\overline{SSTRB}$ and a 2 kΩ pull-up on SCLK. The capacitance on all three outputs is 35 pF.

[3]t_6 is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[4]t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

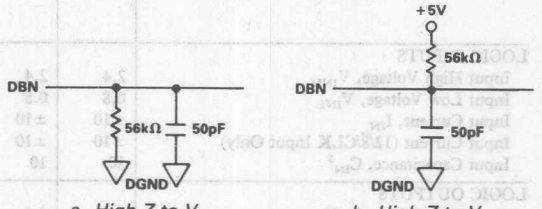
[5]SCLK mark/space ratio (measured from a voltage level of 1.6 V) is 40/60 to 60/40.

[6]SDATA will drive higher capacitive loads but this will add to t_{12} since it increases the external RC time constant (4.7 kΩ||C_L) and hence the time to reach 2.4 V. Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

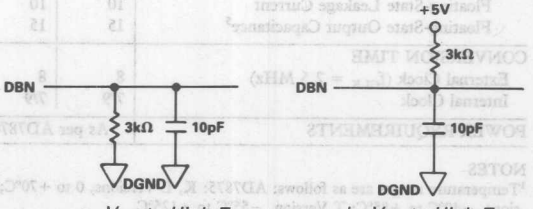
V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
V_{IN} to AGND . . . . . −15 V to +15 V
REF OUT to AGND . . . . . 0 V to V_{DD}
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, K, L Versions – AD7870) . . . . . 0 to +70°C
Commercial (K, L Versions – AD7875) . . . . . 0 to +70°C
Industrial (A, B, C Versions – AD7870) . . . −25°C to +85°C
Industrial (B, C Versions – AD7875/AD7876)
. . . . . −40°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



a. High-Z to V_{OH} b. High-Z to V_{OL}

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 2. Load Circuits for Output Float Delay

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

Model[1, 2]	Temperature Range	V_{IN} Voltage Range (V)	SNR (dBs)	Nonlinearity (LSB)	Package Option[3]
AD7870AJN	0 to +70°C	±3	70 min	±1/2 typ	N-24
AD7870JN	0 to +70°C	±3	70 min	±1/2 typ	N-24
AD7870KN	0 to +70°C	±3	70 min	±1 max	N-24
AD7870LN	0 to +70°C	±3	72 min	±1/2 max	N-24
AD7870JP	0 to +70°C	±3	70 min	±1/2 typ	P-28A
AD7870KP	0 to +70°C	±3	70 min	±1 max	P-28A
AD7870LP	0 to +70°C	±3	72 min	±1/2 max	P-28A
AD7870AQ	−25°C to +85°C	±3	70 min	±1/2 typ	Q-24
AD7870BQ	−25°C to +85°C	±3	70 min	±1 max	Q-24
AD7870CQ	−25°C to +85°C	±3	72 min	±1/2 max	Q-24
AD7870SQ[4]	−55°C to +125°C	±3	69 min	±1/2 typ	Q-24
AD7870TQ[4]	−55°C to +125°C	±3	69 min	±1 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]Contact local sales office for LCCC (Leadless Ceramic Chip Carrier) availability.
[3]N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.
[4]Available to /883B processing only.

AD7875 ORDERING GUIDE

Model[1]	Temperature Range	V_{IN} Voltage Range (V)	SNR (dBs)	Integral Nonlinearity (LSB)	Package Option[2]
AD7875KN	0 to +70°C	0 to +5	70 min	±1 max	N-24
AD7875LN	0 to +70°C	0 to +5	72 min	±1/2 max	N-24
AD7875KR	0 to +70°C	0 to +5	70 min	±1 max	R-24
AD7875KP	0 to +70°C	0 to +5	70 min	±1 max	P-28A
AD7875LP	0 to +70°C	0 to +5	72 min	±1/2 max	P-28A
AD7875BQ	−40°C to +85°C	0 to +5	70 min	±1 max	Q-24
AD7875CQ	−40°C to +85°C	0 to +5	72 min	±1/2 max	Q-24
AD7875TQ[3]	−55°C to +125°C	0 to +5	69 min	±1 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[3]Available to /883B processing only.

AD7876 ORDERING GUIDE

Model[1]	Temperature Range	V_{IN} Voltage Range (V)	Integral Nonlinearity (LSB)	Package Option[2]
AD7876BN	−40°C to +85°C	±10	±1 max	N-24
AD7876CN	−40°C to +85°C	±10	±1/2 max	N-24
AD7876BR	−40°C to +85°C	±10	±1 max	R-24
AD7876CR	−40°C to +85°C	±10	±1/2 max	R-24
AD7876BQ	−40°C to +85°C	±10	±1 max	Q-24
AD7876CQ	−40°C to +85°C	±10	±1/2 max	Q-24
AD7876TQ[3]	−55°C to +125°C	±10	±1 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]N = Narrow Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[3]Available to /883B processing only.

PIN FUNCTION DESCRIPTION

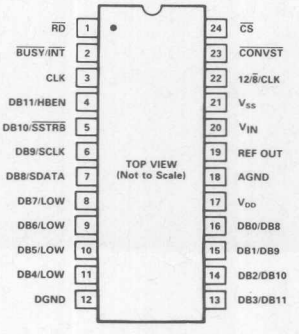
DIP Pin No.	Pin Mnemonic	Function
1	$\overline{RD}$	Read. Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs.
2	$\overline{BUSY}/\overline{INT}$	Busy/Interrupt, Active low logic output indicating converter status. See timing diagrams.
3	CLK	Clock input. An external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to V_{SS} enables the internal laser-trimmed clock oscillator.
4	DB11/HBEN	Data Bit 11 (MSB)/High Byte Enable. The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input (see below). When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table I).
5	DB10/$\overline{SSTRB}$	Data Bit 10/Serial Strobe. When 12-bit parallel data is selected, this pin provides the DB10 output. $\overline{SSTRB}$ is an active low open-drain output that provides a strobe or framing pulse for serial data. An external 4.7 kΩ pull-up resistor is required on $\overline{SSTRB}$.
6	DB9/SCLK	Data Bit 9/Serial Clock. When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If the 12/8/CLK input is at −5 V, then SCLK runs continuously. If 12/8/CLK is at 0 V, then SCLK is gated off after serial transmission is complete. SCLK is an open-drain output and requires an external 2 kΩ pull-up resistor.
7	DB8/SDATA	Data Bit 8/Serial Data. When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is an open-drain serial data output which is used with SCLK and $\overline{SSTRB}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{SSTRB}$ is low. An external 4.7 kΩ pull-up resistor is required on SDATA.
8–11	DB7/LOW–DB4/LOW	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With 12/8/CLK high, they are always DB7-DB4. With 12/8/CLK low or −5 V, their function is controlled by HBEN (see Table I).
12	DGND	Digital Ground. Ground reference for digital circuitry.
13–16	DB3/DB11–DB0/DB8	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With/12/8/CLK high, they are always DB3-DB0. With 12/8/CLK low or −5 V, their function is controlled by HBEN (see Table I).
17	V_{DD}	Positive Supply, +5 V ±5%.
18	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
19	REF OUT	Voltage Reference Output. The internal 3 V reference is provided at this pin. The external load capability is 500 μA.
20	V_{IN}	Analog Input. The analog input range is ±3 V for the AD7870, ±10 V for the AD7876 and 0 to +5 V for the AD7875.
21	V_{SS}	Negative Supply, −5 V ±5%.
22	12/$\overline{8}$/CLK	Three Function Input. Defines the data format and serial clock format. With this pin at +5 V, the output data format is 12-bit parallel only. With this pin at 0 V, either byte or serial data is available and SCLK is not continuous. With this pin at −5 V, byte or serial data is again available but SCLK is now continuous.
23	$\overline{CONVST}$	Convert Start. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. This input is asynchronous to the CLK input.
24	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active. With $\overline{CONVST}$ tied low, a new conversion is initiated when $\overline{CS}$ goes low.

HBEN	DB7/LOW	DB6/LOW	DB5/LOW	DB4/LOW	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
HIGH	LOW	LOW	LOW	LOW	DB11 (MSB)	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)

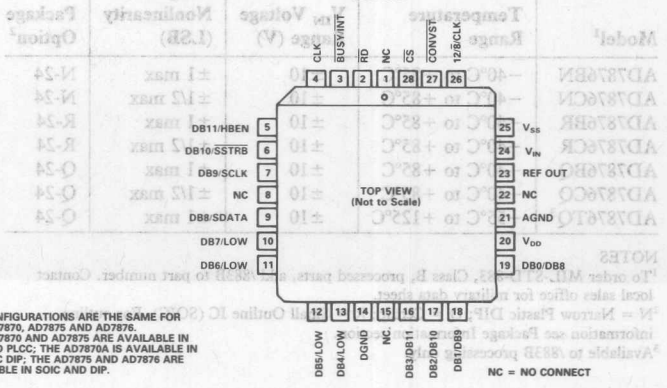
Table I. Output Data for Byte Interfacing

PIN CONFIGURATIONS[1]

DIP and SOIC[2]



PLCC[2]



[1]PIN CONFIGURATIONS ARE THE SAME FOR THE AD7870, AD7875 AND AD7876.
[2]THE AD7870 AND AD7875 ARE AVAILABLE IN DIP AND PLCC; THE AD7870A IS AVAILABLE IN PLASTIC DIP; THE AD7875 AND AD7876 ARE AVAILABLE IN SOIC AND DIP.

LC²MOS Complete 14-Bit Sampling ADCs

AD7871/AD7872

FEATURES

Complete Monolithic 14-Bit ADC
2s Complement Coding
Parallel, Byte and Serial Digital Interface
80 dB SNR at 10 kHz Input Frequency
57 ns Data Access Time
Low Power—50 mW typ
83 kSPS Throughput Rate
16-Lead SOIC (AD7872)

APPLICATIONS

Digital Signal Processing
High Speed Modems
Speech Recognition and Synthesis
Spectrum Analysis
DSP Servo Control

GENERAL DESCRIPTION

The AD7871 and AD7872 are fast, complete, 14-bit analog-to-digital converters. They consist of a track/hold amplifier, successive-approximation ADC, 3 V buried Zener reference and versatile interface logic. The ADC features a self-contained, laser trimmed internal clock, so no external clock timing components are required. The on-chip clock may be overridden to synchronize ADC operation to the digital system for minimum noise.

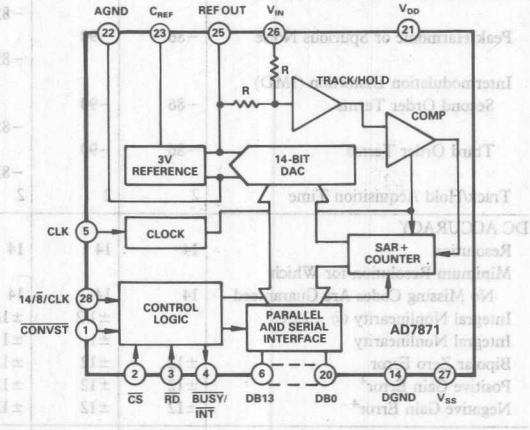
The AD7871 offers a choice of three data output formats: a single, parallel, 14-bit word; two 8-bit bytes or a 14-bit serial data stream. The AD7872 is a serial output device only. The two parts are capable of interfacing to all modern microprocessors and digital signal processors.

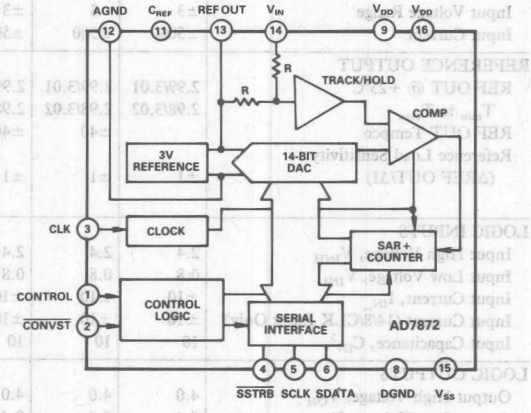
The AD7871 and AD7872 operate from ±5 V power supplies, accept bipolar input signals of ±3 V and can convert full power signals up to 41.5 kHz.

In addition to the traditional dc accuracy specifications, the AD7871 and AD7872 are also fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

Both devices are fabricated in Analog Devices' LC²MOS mixed technology process. The AD7871 is available in 28-pin plastic DIP, hermetic DIP and PLCC packages. The AD7872 is available in 16-pin plastic and hermetic DIP packages or 16-lead SOIC.

FUNCTIONAL BLOCK DIAGRAMS





PRODUCT HIGHLIGHTS

1. Complete 14-Bit ADC on a Chip.
2. Dynamic Specifications for DSP Users.
3. Low Power.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7871/AD7872—SPECIFICATIONS

(V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2 MHz external, f_{SAMPLE} = 83 kHz unless otherwise stated.)All Specifications T_{min} to T_{max} unless otherwise noted.

Parameter	J, A Versions[1]	K, B Versions[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal to Noise Ratio[3] (SNR) @ +25°C	80	80	79	dB min	V_{IN} = 10 kHz Sine Wave
T_{min} to T_{max}	80	80	79	dB min	SNR is Typically 82 dB for <V_{IN}<41.5 kHz;
Total Harmonic Distortion (THD)	−86	−90		dB max	V_{IN} = 10 kHz Sine Wave;
			−85	dB typ	
Peak Harmonic or Spurious Noise	−86	−90		dB max	V_{IN} = 10 kHz.
			−85	dB typ	
Intermodulation Distortion (IMD)					
Second Order Terms	−86	−90		dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
			−85	dB typ	
Third Order Terms	−86	−90		dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
			−85	dB typ	
Track/Hold Acquisition Time	2	2	2	μs max	
DC ACCURACY					
Resolution	14	14	14	Bits	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	14	14	14	Bits	
Integral Nonlinearity @ +25°C		±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1	LSB max	
Bipolar Zero Error	±12	±12	±12	LSB max	
Positive Gain Error[4]	±12	±12	±12	LSB max	
Negative Gain Error[4]	±12	±12	±12	LSB max	
ANALOG INPUT					
Input Voltage Range	±3	±3	±3	Volts	
Input Current	±500	±500	±500	μA max	
REFERENCE OUTPUT					
REF OUT @ +25°C	2.99/3.01	2.99/3.01	2.99/3.01	V min/V max	
T_{min} to T_{max}	2.98/3.02	2.98/3.02	2.98/3.02	V min/V max	
REF OUT Tempco		±40	±40	ppm/°C max	Typically 35 ppm
Reference Load Sensitivity					
(ΔREF OUT/ΔI)	±1	±1	±1	mV max	Reference Load Current Change (0–500 μA); Reference Load Should Not Be Changed During Conversion
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Current (14/8/CLK Input Only)	±10	±10	±10	μA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB13 – DB0					
Floating-State Leakage Current	10	10	10	μA max	
Floating-State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME					
External Clock	10	10	10	μs max	
Internal Clock	10.5	10.5	10.5	μs max	The Internal Clock Has a Nominal Value of 2 MHz
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	mA max	Typically 6 mA
I_{SS}	6	6	6	mA max	Typically 4 mA
Power Dissipation	95	95	95	mW max	Typically 50 mW

NOTES

[1]Temperature ranges are as follows: J, K versions, 0°C to +70°C; A, B versions, −40°C to +85°C; T version; −55°C to +125°C.

[2]V_{IN} = ±3 V.

[3]SNR calculation includes distortion and noise components.

[4]Measured with respect to internal reference.

[5]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V. See Figures 3, 4, 5 and 6.)

Parameter	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (T Version)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 1)
t_3	**60**	**75**	ns min	$\overline{RD}$ Pulse Width
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 1)
t_5	70	70	ns min	$\overline{RD}$ to $\overline{INT}$ Delay
t_6[3]	57	**70**	ns max	Data Access Time after $\overline{RD}$
t_7[4]	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	50	**50**	ns max	
t_8	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	100	100	ns min	$\overline{SSTRB}$ to SCLK Falling Edge Setup Time
t_{11}[5]	440	440	ns min	SCLK Cycle Time
t_{12}[6]	155	155	ns max	SCLK to Valid Data Delay. C_L = 35 pF
t_{13}	140	150	ns max	SCLK Rising Edge to $\overline{SSTRB}$
	20	20	ns min	
t_{14}	4	4	ns min	Bus Relinquish Time after SCLK
	100	100	ns max	
t_{15}	60	60	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 2)
t_{16}	120	120	ns max	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay
t_{17}[3]	200	200	ns min	Data Setup Time Prior to BUSY
t_{18}	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 2)
t_{19}	0	0	ns min	HBEN to $\overline{CS}$ Setup Time
t_{20}	0	0	ns min	HBEN to $\overline{CS}$ Hold Time

NOTES
[1]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and $\overline{SSTRB}$ and a 2 kΩ pull-up resistor on SCLK. The capacitance on all three outputs is 35 pF.
[3]t_6 and t_{17} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7, quoted in the Timing Characteristics is the true bus relinquish time of the part and is independent of bus loading.
[5]SCLK mark/space ratio (measured from a voltage level of 1.6 V) is 40/60 to 60/40.
[6]SDATA will drive higher capacitive loads, but this will add to t_{12} since it increases the external RC time constant (4.7 kΩ//C_L) and hence the time to reach 2.4 V.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
V_{IN} to AGND . . . . . V_{SS} − 0.3 V to V_{DD} + 0.3 V
REF OUT, C_{REF} to AGND . . . . . 0 V to V_{DD}
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0°C to +70°C
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 6 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

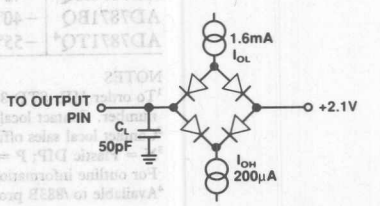


Figure 1. Load Circuit for Access Time

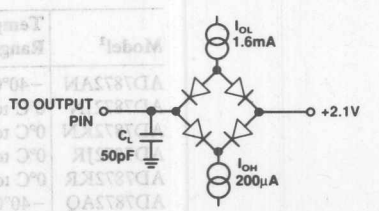
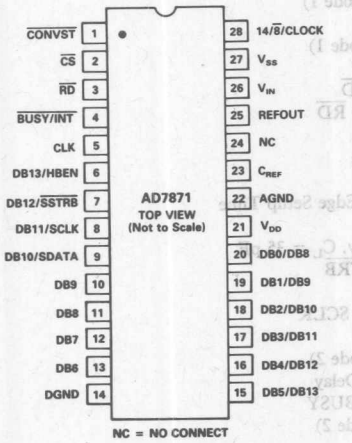


Figure 2. Load Circuit for Output Float Delay

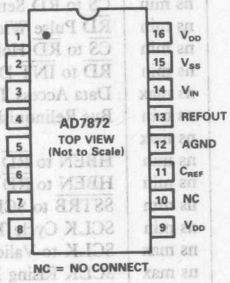
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

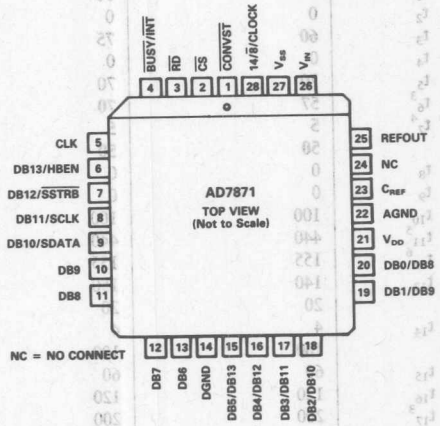
DIP



DIP, SOIC



PLCC



AD7871 ORDERING GUIDE

Model[1, 2]	Temperature Range	SNR	Relative Accuracy	Package Option[3]
AD7871JN	0°C to +70°C	80 dBs min		N-28
AD7871KN	0°C to +70°C	80 dBs min	±1 max	N-28
AD7871JP	0°C to +70°C	80 dBs min		P-28A
AD7871KP	0°C to +70°C	80 dBs min	±1 max	P-28A
AD7871AQ	−40°C to +85°C	80 dBs min		Q-28
AD7871BQ	−40°C to +85°C	80 dBs min	±1 max	Q-28
AD7871TQ[4]	−55°C to +125°C	79 dBs min	±1 max	Q-28

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]Contact local sales office for LCCC availability.
[3]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.
[4]Available to /883B processing only.

AD7872 ORDERING GUIDE

Model[1]	Temperature Range	SNR	Relative Accuracy	Package Option[2]
AD7872AN	−40°C to +85°C	80 dBs min		N-16
AD7872JN	0°C to +70°C	80 dBs min		N-16
AD7872KN	0°C to +70°C	80 dBs min	±1 max	N-16
AD7872JR	0°C to +70°C	80 dBs min		R-16
AD7872KR	0°C to +70°C	80 dBs min	±1 max	R-16
AD7872AQ	−40°C to +85°C	80 dBs min		Q-16
AD7872BQ	−40°C to +85°C	80 dBs min	±1 max	Q-16
AD7872TQ[3]	−55°C to +125°C	79 dBs min	±1 max	Q-16

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[3]Available to /883B processing only.

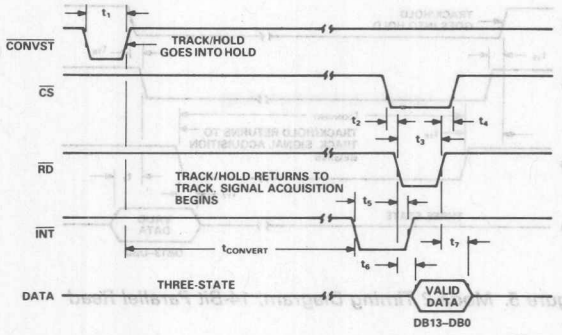
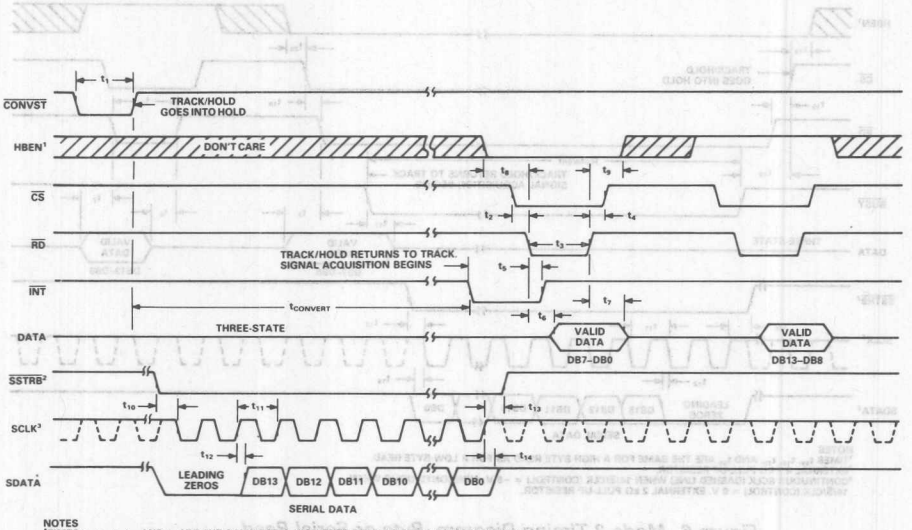


Figure 3. Mode 1 Timing Diagram, 14-Bit Parallel Read



NOTES
[1]TIMES t_2, t_3, t_4, t_8, AND t_9 ARE THE SAME FOR A HIGH BYTE READ AS FOR A LOW BYTE READ.
[2]EXTERNAL 4.7 kΩ PULL-UP RESISTOR.
[3]EXTERNAL 2 kΩ PULL-UP RESISTOR. CONTINUOUS SCLK (DASHED LINE) WHEN 14/$\overline{8}$/CLK (CONTROL) = −5 V; NONCONTINUOUS WHEN 14/$\overline{8}$/CLK (CONTROL) = 0V.

Figure 4. Mode 1 Timing Diagram, Byte or Serial Read

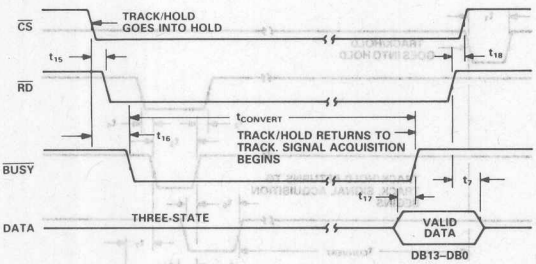
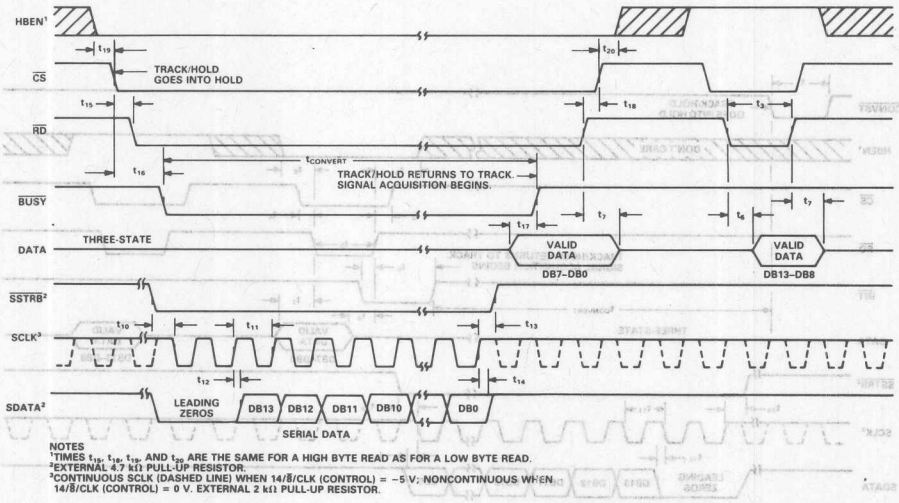


Figure 5. Mode 2 Timing Diagram, 14-Bit Parallel Read



NOTES
1TIMES t_{19}, t_{16}, t_{19}, AND t_{20} ARE THE SAME FOR A HIGH BYTE READ AS FOR A LOW BYTE READ.
2EXTERNAL 4.7 kΩ PULL-UP RESISTOR.
3CONTINUOUS SCLK (DASHED LINE) WHEN 14/8/CLK (CONTROL) = –5 V; NONCONTINUOUS WHEN 14/8/CLK (CONTROL) = 0 V. EXTERNAL 2 kΩ PULL-UP RESISTOR.

Figure 6. Mode 2 Timing Diagram, Byte or Serial Read

LC²MOS 4-Channel, 12-Bit Simultaneous Sampling Data Acquisition System

AD7874

2

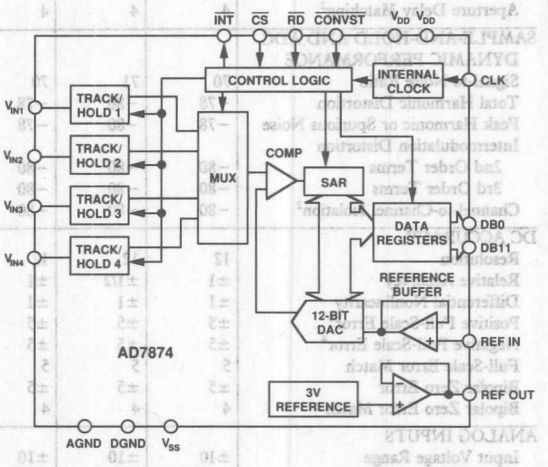
FEATURES

Four On-Chip Track/Hold Amplifiers
Simultaneous Sampling of 4 Channels
Fast 12-Bit ADC with 8 µs Conversion Time/Channel
29 kHz Sample Rate for All Four Channels
On-Chip Reference
±10 V Input Range
±5 V Supplies

APPLICATIONS

Sonar
Motor Controllers
Adaptive Filters
Digital Signal Processing

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7874 is a four-channel simultaneous sampling, 12-bit data acquisition system. The part contains a high speed 12-bit ADC, on-chip reference, on-chip clock and four track/hold amplifiers. This latter feature allows the four input channels to be sampled simultaneously, thus preserving the relative phase information of the four input channels, which is not possible if all four channels share a single track/hold amplifier. This makes the AD7874 ideal for applications such as phased-array sonar and ac motor controllers where the relative phase information is important.

The aperture delay of the four track/hold amplifiers is small and specified with minimum and maximum limits. This allows several AD7874s to sample multiple input channels simultaneously without incurring phase errors between signals connected to several devices. A reference output/reference input facility also allows several AD7874s to be driven from the same reference source.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7874 is also fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

The AD7874 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low-power CMOS logic. The part is available in a 28-pin, 0.6" wide, plastic or hermetic dual-in-line package (DIP), in a 28-terminal leadless ceramic chip carrier (LCCC) and in a 28-pin SOIC.

PRODUCT HIGHLIGHTS

1. Simultaneous Sampling of Four Input Channels.
   Four input channels, each with its own track/hold amplifier, allow simultaneous sampling of input signals. Track/hold acquisition time is 2 µs, and the conversion time per channel is 8 µs, allowing 29 kHz sample rate for all four channels.
2. Tight Aperture Delay Matching.
   The aperture delay for each channel is small and the aperture delay matching between the four channels is less than 4 ns. Additionally, the aperture delay specification has upper and lower limits allowing multiple AD7874s to sample more than four channels.
3. Fast Microprocessor Interface.
   The high speed digital interface of the AD7874 allows direct connection to all modern 16-bit microprocessors and digital signal processors.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7874—SPECIFICATIONS (V_{DD} = +5 V, V_{SS} = −5 V, AGND = DGND = 0 V, REF IN = +3 V, f_{CLK} = 2.5 MHz external. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	A Version	B Version	S Version	Units	Test Conditions/Comments
SAMPLE-AND-HOLD					
Acquisition Time[2] to 0.01%	2	2	2	µs max	
Droop Rate[2, 3]	1	1	2	mV/ms max	
−3 dB Small Signal Bandwidth[3]	500	500	500	kHz typ	V_{IN} = 500 mV p–p
Aperture Delay[2]	0	0	0	ns min	
	40	40	40	ns max	
Aperture Jitter[2, 3]	200	200	200	ps typ	
Aperture Delay Matching[2]	4	4	4	ns max	
SAMPLE-AND-HOLD AND ADC DYNAMIC PERFORMANCE					
Signal-to-Noise Ratio	70	71	70	dB min	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 29 kHz
Total Harmonic Distortion	−78	−80	−78	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 29 kHz
Peak Harmonic or Spurious Noise	−78	−80	−78	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 29 kHz
Intermodulation Distortion					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 29 kHz
2nd Order Terms	−80	−80	−80	dB max	
3rd Order Terms	−80	−80	−80	dB max	
Channel-to-Channel Isolation[2]	−80	−80	−80	dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	No Missing Codes Guaranteed
Positive Full-Scale Error[4]	±5	±5	±5	LSB max	Any Channel
Negative Full-Scale Error[4]	±5	±5	±5	LSB max	Any Channel
Full-Scale Error Match	5	5	5	LSB max	Between Channels
Bipolar Zero Error	±5	±5	±5	LSB max	Any Channel
Bipolar Zero Error Match	4	4	4	LSB max	Between Channels
ANALOG INPUTS					
Input Voltage Range	±10	±10	±10	Volts	
Input Current	±600	±600	±600	µA max	
REFERENCE OUTPUT[5]					
REF OUT	3	3	3	V nom	
REF OUT Error @ +25°C	±0.33	±0.33	±0.33	% max	
T_{min} to T_{max}	±1	±1	±1	% max	
REF OUT Temperature Coefficient	±35	±35	±35	ppm/°C typ	
Reference Load Change	±1	±1	±2	mV max	Reference Load Current Change (0–500 µA)
					Reference Load Should Not Be Changed During Conversion
REFERENCE INPUT					
Input Voltage Range	2.85/3.15	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	±1	±1	±1	µA max	
Input Capacitance[3]	10	10	10	pF max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ±5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ±5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	V_{DD} = 5 V ±5%; I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	V_{DD} = 5 V ±5%; I_{SINK} = 1.6 mA
DB0–DB11					
Floating-State Leakage Current	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Floating-State Output Capacitance	10	10	10	pF max	
Output Coding	2s COMPLEMENT				
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	18	18	18	mA max	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = +5 V; Typically 12 mA
I_{SS}	12	12	12	mA max	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = +5 V; Typically 8 mA
Power Dissipation	150	150	150	mW max	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = +5 V; Typically 100 mW

NOTES
[1]Temperature ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.
[2]See Terminology.
[3]Sample tested @ +25°C to ensure compliance.
[4]Measured with respect to the REF IN voltage and includes bipolar offset error.
[5]For capacitive loads greater than 50 pF a series resistor is required.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2.5 MHz external unless otherwise stated.)

Parameter	A, B Versions	S Version	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_3	**60**	**70**	ns min	$\overline{RD}$ Pulse Width
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_5	60	60	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_6[2]	**57**	**70**	ns max	Data Access Time after $\overline{RD}$
t_7[3]	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	45	**50**	ns max	
t_8	130	150	ns min	Delay Time between Reads
t_{CONV}	31	31	µs min	$\overline{CONVST}$ to $\overline{INT}$, External Clock
	32.5	32.5	µs max	$\overline{CONVST}$ to $\overline{INT}$, External Clock
	31	31	µs min	$\overline{CONVST}$ to $\overline{INT}$, Internal Clock
	35	35	µs max	$\overline{CONVST}$ to $\overline{INT}$, Internal Clock
t_{CLK}	10	10	µs max	Minimum Input Clock Period

NOTES

[1]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]t_6 is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice.

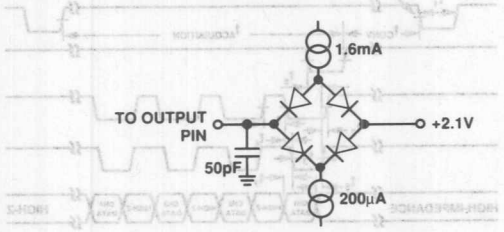


Figure 1. Load Circuit for Access Time

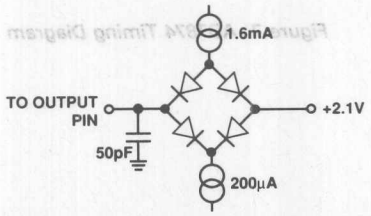


Figure 2. Load Circuit for Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	−0.3 V to +7 V
V_{DD} to DGND	−0.3 V to +7 V
V_{SS} to AGND	+0.3 V to −7 V
AGND to DGND	−0.3 V to V_{DD}+0.3 V
V_{IN} to AGND	−15 V to +15 V
REF OUT to AGND	0 V to V_{DD}
Digital Inputs to DGND	−0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND	−0.3 V to V_{DD} +0.3 V
Operating Temperature Range	
Commercial (A, B Versions)	−40°C to +85°C
Extended (S Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Any Package) to +75°C	1,000 mW
Derates above +75°C by	10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

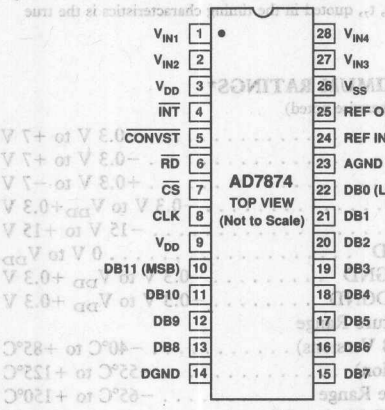
ORDERING GUIDE

Model[1]	Temperature Range	SNR (dBs)	Relative Accuracy (LSB)	Package Option[2]
AD7874AN	−40°C to +85°C	70 min	±1 max	N-28
AD7874BN	−40°C to +85°C	72 min	±1/2 max	N-28
AD7874AR	−40°C to +85°C	70 min	±1 max	R-28
AD7874BR	−40°C to +85°C	72 min	±1/2 max	R-28
AD7874AQ	−40°C to +85°C	70 min	±1 max	Q-28
AD7874BQ	−40°C to +85°C	72 min	±1/2 max	Q-28
AD7874SQ[3]	−55°C to +125°C	70 min	±1 max	Q-28
AD7874SE[3]	−55°C to +125°C	70 min	±1 max	E-28A

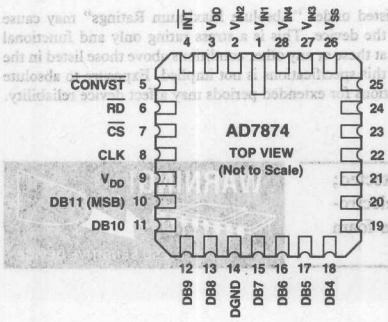
NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.
[2]E = Leaded Ceramic Chip Carrier; N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[3]Available to /883B processing only.

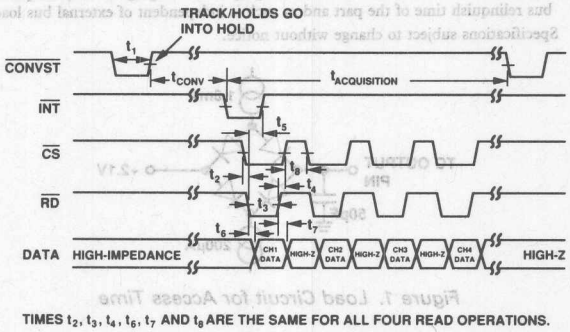
PIN CONFIGURATIONS

DIP and SOIC



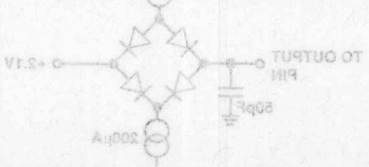
LCCC





TIMES t_2, t_3, t_4, t_6, t_7 AND t_8 ARE THE SAME FOR ALL FOUR READ OPERATIONS.

Figure 7. AD7874 Timing Diagram



LC²MOS Complete 12-Bit 100 kHz Sampling ADC with DSP Interface

AD7878

FEATURES

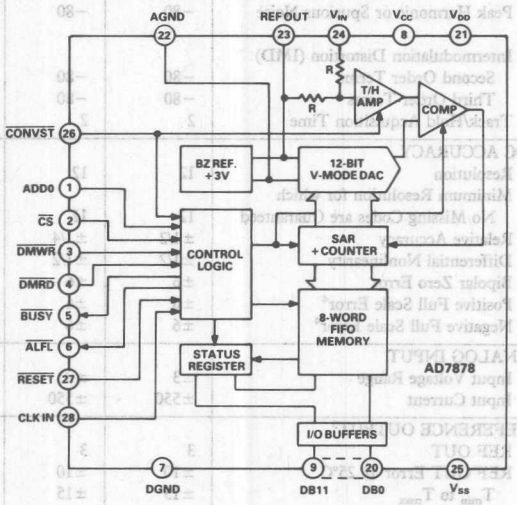
Complete ADC with DSP Interface, Comprising:
- Track/Hold Amplifier with 2 μs Acquisition Time
- 7 μs A/D Converter
- 3 V Zener Reference
- 8-Word FIFO and Interface Logic

72 dB SNR at 10 kHz Input Frequency
Interfaces to High Speed DSP Processors, e.g., ADSP-2100, TMS32010, TMS32020
41 ns max Data Access Time
Low Power, 60 mW typ

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7878 is a fast, complete 12-bit A/D converter with a versatile DSP interface consisting of an 8-word, first-in, first-out (FIFO) memory and associated control logic.

The FIFO memory allows up to eight samples to be digitized before the microprocessor is required to service the A/D converter. The eight words can then be read out of the FIFO at maximum microprocessor speed. A fast data access time of 41 ns allows direct interfacing to DSP processors and high speed 16-bit microprocessors.

An on-chip status/control register allows the user to program the effective length of the FIFO and contains the FIFO out of range, FIFO empty and FIFO word count information.

The analog input of the AD7878 has a bipolar range of ±3 V. The AD7878 can convert full power signals up to 50 kHz and is fully specified for dynamic parameters such as signal-to-noise ratio and harmonic distortion.

The AD7878 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in four package styles, 28-pin plastic and hermetic dual-in-line package (DIP), leadless ceramic chip carrier (LCCC) or plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. Complete A/D Function with DSP Interface
   The AD7878 provides the complete function for digitizing ac signals to 12-bit accuracy. The part features an on-chip track/hold, on-chip reference and 12-bit A/D converter. The additional feature of an 8-word FIFO reduces the high software overheads associated with servicing interrupts in DSP processors.
2. Dynamic Specifications for DSP Users
   The AD7878 is fully specified and tested for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion. Key digital timing parameters are also tested and specified over the full operating temperature range.
3. Fast Microprocessor Interface
   Data access time of 41 ns is the fastest ever achieved in a monolithic A/D converter and makes the AD7878 compatible with all modern 16-bit microprocessors and digital signal processors.

ORDERING GUIDE

Model[1, 2]	Temperature Range	Signal-to-Noise Ratio	Data Access Time	Package Options[3]
AD7878JN	0°C to +70°C	70 dB	57 ns	N-28
AD7878AQ	−25°C to +85°C	70 dB	57 ns	Q-28
AD7878SQ	−55°C to +125°C	70 dB	57 ns	Q-28
AD7878KN	0°C to +70°C	72 dB	57 ns	N-28
AD7878BQ	−25°C to +85°C	72 dB	57 ns	Q-28
AD7878LN	0°C to +70°C	72 dB	41 ns	N-28
AD7878SE[4]	−55°C to +125°C	70 dB	57 ns	E-28A
AD7878JP	0°C to +70°C	70 dB	57 ns	P-28A
AD7878KP	0°C to +70°C	72 dB	57 ns	P-28A
AD7878LP	0°C to +70°C	72 dB	41 ns	P-28A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact our local sales office for military data sheet.
[2]Analog Devices reserves the right to ship either ceramic (D-28) packages or cerdip (Q-28) hermetic packages.
[3]For outline information see Package Information section.
[4]Available to /883B processing only.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter	Versions[1]	Versions	Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio (SNR)[3] @ 25°C	70	72	70	dB min	V_{IN} = 10 kHz Sine Wave , f_{SAMPLE} = 100 kHz
T_{min} to T_{max}	70	71	70	dB min	Typically 71.5 dB for 0<V_{IN}<50 kHz
Total Harmonic Distortion (THD)	−80	−80	−78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically −86 dB for 0<V_{IN}<50 kHz
Peak Harmonic or Spurious Noise	−80	−80	−78	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz Typically −86 dB for 0<V_{IN}<50 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	2	μs max	See Throughput Rate Section.
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for which					
No Missing Codes are Guaranteed	12	12	12	Bits	
Relative Accuracy	±1/2	±1/4	±1/2	LSB typ	
Differential Nonlinearity	±1/2	±1/2	±1/2	LSB typ	
Bipolar Zero Error	±6	±6	±6	LSB max	
Positive Full Scale Error[4]	±6	±6	±6	LSB max	
Negative Full Scale Error[4]	±6	±6	±6	LSB max	
ANALOG INPUT					
Input Voltage Range	±3	±3	±3	Volts	
Input Current	±550	±550	±550	μA max	
REFERENCE OUTPUT[5]					
REF OUT	3	3	3	V nom	
REF OUT Error @ 25°C	±10	±10	±10	mV max	
T_{min} to T_{max}	±15	±15	±15	mV max	
Reference Load Sensitivity					
(ΔREF OUT/ΔI)	±1	±1	±1	mV max	Reference Load Current Change (0–500 μA). Reference Load Should Not Be Changed During Conversion.
LOGIC INPUTS					
Input High Voltage, V_{INH}	+2.4	+2.4	+2.4	V min	V_{CC} = +5 V ± 5%
Input Low Voltage, V_{INL}	+0.8	+0.8	+0.8	V max	V_{CC} = +5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 to V_{CC}
Input Capacitance, C_{IN}[6]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	+2.7	+2.7	+2.7	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating State Leakage Current	±10	±10	±10	μA max	
Floating State Output Capacitance[6]	15	15	15	15	pF max
CONVERSION TIME					
	7/7.125	7/7.125	7/7.125	μs min/μs max	Assuming No External Read/Write Operations
	7/9.250	7/9.250	7/9.250	μs min/μs max	Assuming 17 External Read/Write Operations
					See Internal Comparator Timing Section
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{CC}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	mA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5 V
I_{CC}	100	100	100	μA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5 V
I_{SS}	6	6	6	mA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5 V
Power Dissipation	95.5	95.5	95.5	mW max	Typically 60 mW

NOTES

[1]Temperature range as follows: J, K, L versions: 0 to +70°C; A, B versions: −25°C to +85°C; S version: −55°C to +125°C.

[2]V_{IN} = ±3 V. See Dynamic Specifications section.

[3]SNR calculation includes distortion and noise components.

[4]Measured with respect to the Internal Reference.

[5]For Capacitive Loads greater than 50 pF a series resistor is required (see Internal Reference section).

[6]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = 5 V ± 5%, V_{CC} = 5 V ± 5%, V_{SS} = −5 V ± 5%)

Parameter	Limit at T_{min}, T_{max} (L Grade)	Limit at T_{min}, T_{max} (J, K, A, B Grades)	Limit at T_{min}, T_{max} (S Grade)	Units	Conditions/Comments
t_1	65	65	75	ns max	CLK IN to $\overline{BUSY}$ Low Propagation Delay
t_2	65	65	75	ns max	CLK IN to $\overline{BUSY}$ High Propagation Delay
t_3	2 CLK IN cycles	2 CLK IN cycles	2 CLK IN cycles	min	$\overline{CONVST}$ Pulse Width
t_4	0	0	0	ns min	$\overline{CS}$ to $\overline{DMRD}$/REGISTER ENABLE Setup Time
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{DMRD}$/REGISTER ENABLE Hold Time
t_6	45	60	60	ns min	$\overline{DMRD}$ Pulse Width
	50	50	50	µs max	
t_7	16	16	16	ns min	ADD0 to $\overline{DMRD}$/REGISTER ENABLE Setup Time
t_8	0	0	0	ns min	ADD0 to $\overline{DMRD}$/REGISTER ENABLE Hold Time
t_9[2]	41	57	57	ns min	Data Access Time after $\overline{DMRD}$
t_{10}[3]	5	5	5	ns min	Bus Relinquish Time
	45	45	45	ns max	
t_{11}	42	42	55	ns min	REGISTER ENABLE Pulse Width
	50	50	50	µs max	
t_{12}	20	20	30	ns min	Data Valid to REGISTER ENABLE Setup Time
t_{13}	10	10	10	ns min	Data Hold Time after REGISTER ENABLE
t_{14}[2]	41	57	57	ns min	Data Access Time after BUSY
t_{RESET}	2 CLK IN cycles	2 CLK IN cycles	2 CLK IN cycles	min	RESET Pulse Width

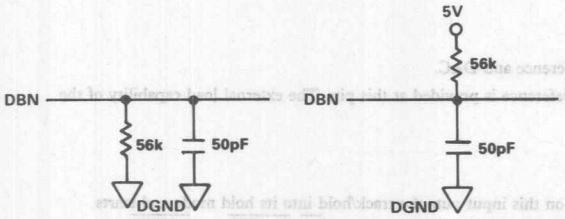
NOTES

[1]Timing Specifications in **bold** print are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_9 and t_{14} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

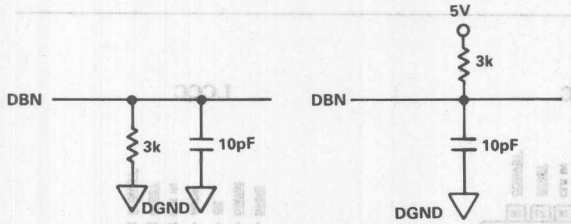
[3]t_{10} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND . . . . . −0.3 V to +7 V
V_{CC} to DGND . . . . . −0.3 V to +7 V
V_{SS} to DGND . . . . . +0.3 V to −7 V
V_{DD} to V_{CC} . . . . . −0.3 V to +0.3 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
V_{IN} to AGND . . . . . −15 V to +15 V
REF OUT to AGND . . . . . 0 to V_{DD}
Digital Inputs to DGND
$\overline{CLK\ IN}$, $\overline{DMWR}$, $\overline{DMRD}$, $\overline{RESET}$, $\overline{CS}$, $\overline{CONVST}$, ADD0 . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND
$\overline{ALFL}$, $\overline{BUSY}$ . . . . . −0.3 V to V_{DD} +0.3 V
Data Pins
DB11–DB0 . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
J, K, L Versions . . . . . 0 to +70°C
A, B Versions . . . . . −25°C to +85°C
S Version . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

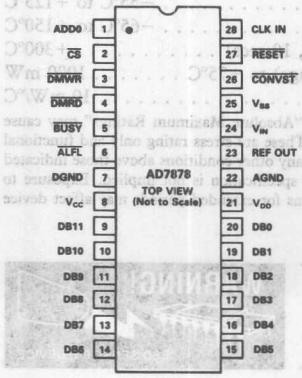
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN FUNCTION DESCRIPTION

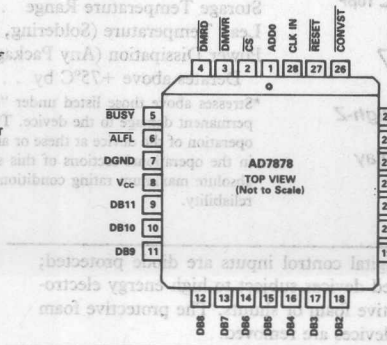
Pin Number	Pin Mnemonic	Function
1	ADD0	Address Input. This control input determines whether the word placed on the output data bus during a read operation is a data word from the FIFO RAM or the contents of the status/control register. A logic low accesses the data word from Location 0 of the FIFO while a logic high selects the contents of the register (see Status/Control Register section).
2	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
3	$\overline{DMWR}$	Data Memory Write. Active low logic input. $\overline{DMWR}$ is used in conjunction with $\overline{CS}$ low and ADD0 high to write data to the status/control register. Corresponds to $\overline{DMWR}$ (ADSP-2100), R/$\overline{W}$ (MC68000, TMS32020), $\overline{WE}$ (TMS32010).
4	$\overline{DMRD}$	Data Memory READ. Active low logic input. $\overline{DMRD}$ is used in conjunction with $\overline{CS}$ low to enable the three-state output buffers. Corresponds directly to $\overline{DMRD}$ (ADSP-2100), $\overline{DEN}$ (TMS32010).
5	$\overline{BUSY}$	Active low logic output. This output goes low when the ADC receives a $\overline{CONVST}$ pulse and remains low until the track/hold has gone into its hold mode. The three-state drivers of the AD7878 can be disabled while the $\overline{BUSY}$ signal is low (see Extended READ/WRITE section). This is achieved by writing a logic 0 to DB5 ($\overline{DISO}$) of the status/control register. Writing a logic 1 to DB5 of the status/control register allows data to be accessed from the AD7878 while $\overline{BUSY}$ is low.
6	$\overline{ALFL}$	FIFO Almost Full. A logic low indicates that the word count (i.e., number of conversion results) in the FIFO memory has reached the programmed word count in the status/control register. $\overline{ALFL}$ is updated at the end of each conversion. The $\overline{ALFL}$ output is reset to a logic high when a word is read from the FIFO memory and the word count is less than the preprogrammed word count. It can also be set high by writing a logic 1 to DB7 ($\overline{ENAF}$) of the status/control register.
7	DGND	Digital Ground. Ground reference for digital circuitry.
8	V_{CC}	Digital supply voltage, +5 V ±5%. Positive supply voltage for digital circuitry.
9	DB11	Data Bit 11 (MSB). Three-state TTL output. Coding for the data words in FIFO RAM is 2s complement.
10–15	DB10–DB5	Data Bit 10 to Data Bit 5. Three-state TTL input/outputs.
16–19	DB4–DB1	Data Bit 4 to Data Bit 1. Three-state TTL outputs.
20	DB0	Data Bit 0 (LSB). Three-state TTL output.
21	V_{DD}	Analog positive supply voltage, +5 V ±5%.
22	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
23	REF OUT	Voltage Reference Output. The internal 3 V analog reference is provided at this pin. The external load capability of the reference is 500 μA.
24	V_{IN}	Analog Input. Analog input range is ±3 V.
25	V_{SS}	Analog negative supply voltage, −5 V ±5%.
26	$\overline{CONVST}$	Convert Start. Logic input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. The $\overline{CONVST}$ input is asynchronous to CLK IN and is independent of $\overline{CS}$, $\overline{DMWR}$ and $\overline{DMRD}$.
27	$\overline{RESET}$	Reset. Active low logic input. A logic low sets the words in FIFO memory to 1000 0000 0000 and resets the $\overline{ALFL}$ output and status/control register.
28	CLK IN	Clock Input. TTL-compatible logic input. Used as the clock source for the A/D converter. The mark-space ratio of this clock can vary from 35/65 to 65/35.

PIN CONFIGURATIONS

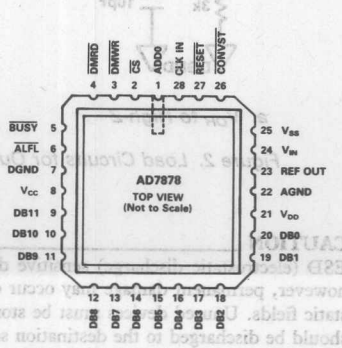
DIP



PLCC



LCCC



LC²MOS Single +5 V Supply, Low Power, 12-Bit Sampling ADC

AD7880

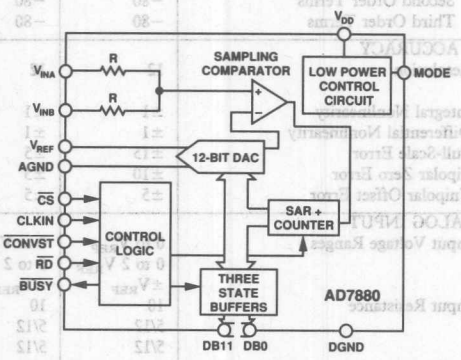
FEATURES

- 12-Bit Monolithic A/D Converter
- 66 kHz Throughput Rate
  - 12 μs Conversion Time
  - 3 μs On-Chip Track/Hold Amplifier
- Low Power
  - Power Save Mode: 2 mW typ
  - Normal Operation: 25 mW typ
- 70 dB SNR
- Fast Data Access Time: 57 ns
- Small 24-Lead SOIC and 0.3″ DIP Packages

APPLICATIONS

- Battery Powered Portable Systems
- Digital Signal Processing
- Speech Recognition and Synthesis
- High Speed Modems
- Control and Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7880 is a high speed, low power, 12-bit A/D converter which operates from a single +5 V supply. It consists of a 3 μs track/hold amplifier, a 12 μs successive-approximation ADC, versatile interface logic and a multiple-input-range circuit. The part also includes a power save feature.

An internal resistor network allows the part to accept both unipolar and bipolar input signals while operating from a single +5 V supply. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

The AD7880 features a total throughput time of 15 μs and can convert full power signals up to 33 kHz with a sampling frequency of 66 kHz.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7880 is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7880 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3 inch-wide, plastic or hermetic dual-in-line package (DIP) as well as a small 24-lead SOIC package.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time.
   12 μs conversion time and 3 μs acquisition time allow for large input signal bandwidth. This performance is ideally suited for applications in areas such as telecommunications, audio, sonar and radar signal processing.
2. Low Power Consumption.
   2 mW power consumption in the power-down mode makes the part ideally suited for portable, hand held, battery powered applications.
3. Multiple Input Ranges.
   The part features three user-determined input ranges, 0 to +5 V, 0 to 10 V and ±5 V. These unipolar and bipolar ranges are achieved with a 5 V only power supply.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7880—SPECIFICATIONS

(V_{DD} = +5 V ± 5%, V_{REF} = V_{DD}, AGND = DGND = 0 V, f_{CLKIN} = 2.5 MHz, MODE = V_{DD} unless otherwise noted. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	B Versions[1]	C Versions[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio[3] (SNR)	70	70	dB min	Typically SNR Is 72 dB V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 66 kHz
Total Harmonic Distortion (THD)	−80	−80	dB typ	V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 66 kHz
Peak Harmonic or Spurious Noise	−80	−80	dB typ	V_{IN} = 1 kHz, f_{SAMPLE} = 66 kHz
Intermodulation Distortion (IMD)				
Second Order Terms	−80	−80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 66 kHz
Third Order Terms	−80	−80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 66 kHz
DC ACCURACY				
Resolution	12	12	Bits	All DC ACCURACY Specifications Apply for the Three Analog Input Ranges
Integral Nonlinearity	±1	±1	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±15	±5	LSB max	
Bipolar Zero Error	±10	±5	LSB max	
Unipolar Offset Error	±5	±5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	See Figure 5
	0 to 2 V_{REF}	0 to 2 V_{REF}	Volts	See Figure 6
	±V_{REF}	±V_{REF}	Volts	See Figure 7
Input Resistance	10	10	MΩ min	0 to V_{REF} Range
	5/12	5/12	kΩ min/max	8 kΩ typical: 0 to 2V_{REF} Range
	5/12	5/12	kΩ min/max	8 kΩ typical: ±V_{REF} Range
REFERENCE INPUT				
V_{REF} (For Specified Performance)	5	5	V	±5%: Normally V_{REF} = V_{DD} (See Reference Input Section)
I_{REF}	1.5	1.5	mA max	
Nominal Reference Range	2.5/V_{DD}	2.5/V_{DD}	V min/max	See Figure 3 for Degradation in Performance Down to 2.5 V
LOGIC INPUTS				
$\overline{CONVST}$, $\overline{RD}$, $\overline{CS}$, CLKIN				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
MODE INPUT				
Input High Voltage, V_{INH}	4	4	V min	
Input Low Voltage, V_{INL}	1	1	V max	
Input Current, I_{IN}	±125	±125	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
DB11–DB0, $\overline{BUSY}$				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0				
Floating-State Leakage Current	±10	±10	μA max	
Floating-State Output Capacitance[4]	10	10	pF max	
CONVERSION				
Conversion Time	12	12	μs max	f_{CLKIN} = 2.5 MHz
Track/Hold Acquisition Time	3	3	μs max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
I_{DD}				
Normal Power Mode @ +25°C	7.5	7.5	mA max	Typically 4 mA; MODE = V_{DD}
T_{min} to T_{max}	10	10	mA max	Typically 5 mA; MODE = V_{DD}
Power Save Mode @ +25°C	750	750	μA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V
T_{min} to T_{max}	1	1	mA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V
Power Dissipation				
Normal Power Mode @ +25°C	37.5	37.5	mW max	V_{DD} = 5 V: Typically 20 mW; MODE = V_{DD}
T_{min} to T_{max}	50	50	mW max	V_{DD} = 5 V: Typically 25 mW; MODE = V_{DD}
Power Save Mode @ +25°C	3.75	3.75	mW max	V_{DD} = 5 V: Typically 2 mW; MODE = 0 V
T_{min} to T_{max}	5	5	mW max	V_{DD} = 5 V: Typically 2.5 mW; MODE = 0 V

NOTES

[1]Temperature Ranges are as follows: B/C Versions, −40°C to +85°C.

[2]V_{IN} = 0 to V_{REF}.

[3]SNR calculation includes distortion and noise components.

[4]Sample tested @25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{REF} = V_{DD}, AGND = DGND = 0 V)

Parameter	Limit at 25°C (All Versions)	Limit at T_{min}, T_{max} (All Versions)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	130	130	ns min	$\overline{CONVST}$ to $\overline{BUSY}$ Falling Edge
t_3	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Setup Time
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_5	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6	60	75	ns min	$\overline{RD}$ Pulse Width
t_7[2]	57	70	ns max	Data Access Time after $\overline{RD}$
t_8[3]	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	50	50	ns max	

NOTES

[1]Timing specifications in **bold** print are 100% production tested. All other times are sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_7 is measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_8 is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

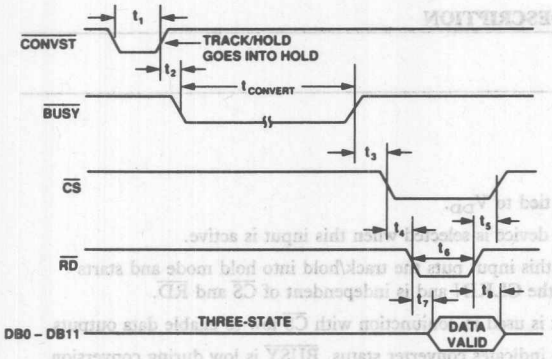


Figure 1. Timing Diagram

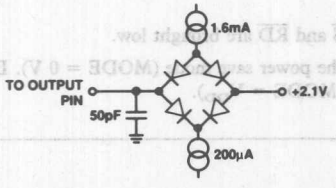


Figure 2. Load Circuit for Access and Relinquish Time

Table I. AD7880 Truth Table

$\overline{CS}$	$\overline{CONVST}$	$\overline{RD}$	Function
1	1	X	Not Selected
1	↓	1	Start Conversion ↓
0	1	0	Enable ADC Data
0	1	1	Data Bus Three Stated

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND ..... −0.3 V to +7 V
V_{DD} to DGND ..... −0.3 V to +7 V
AGND to DGND ..... −0.3 V to V_{DD} +0.3 V
V_{INA}, V_{INB} to AGND (Fig 5) ..... −0.3 V to V_{DD} +0.3 V
V_{INA} to AGND (Fig 6) ..... −0.6 V to 2 V_{DD} +0.6 V
V_{INA} to AGND(Fig 7) ..... $-V_{DD}$−0.3 V to V_{DD}+0.3 V
V_{REF} to AGND ..... 0.3 V to V_{DD}
Digital Inputs to DGND ..... −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND ..... −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Industrial (B, C Versions) ..... −40°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Power Dissipation (Any Package) to +75°C ..... 450 mW
Derates above +75°C by ..... 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

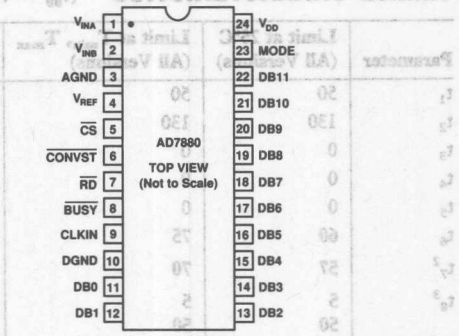
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

Model	Temperature Range	Full-Scale Error (LSBs)	Bipolar Zero Error (LSBs)	Package Option*
AD7880BN	−40°C to +85°C	±15	±10	N-24
AD7880BQ	−40°C to +85°C	±15	±10	Q-24
AD7880CN	−40°C to +85°C	±5	±5	N-24
AD7880CQ	−40°C to +85°C	±5	±5	Q-24
AD7880BR	−40°C to +85°C	±15	±10	R-24
AD7880CR	−40°C to +85°C	±5	±5	R-24

*N = Plastic DIP; Q = Cerdip; R = SOIC (Small Outline Integrated Circuit). For outline information see Package Information section.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
1	V_{INA}	Analog Input.
2	V_{INB}	Analog Input.
3	AGND	Analog Ground.
4	V_{REF}	Voltage Reference Input. This is normally tied to V_{DD}.
5	$\overline{CS}$	Chip Select. Active Low Logic input. The device is selected when this input is active.
6	$\overline{CONVST}$	Convert Start. A low to high transition on this input puts the track/hold into hold mode and starts conversion. This input is asynchronous to the CLKIN and is independent of $\overline{CS}$ and $\overline{RD}$.
7	$\overline{RD}$	Read. Active Low Logic Input. This input is used in conjunction with $\overline{CS}$ low to enable data outputs.
8	$\overline{BUSY}$	Active Low Logic Output. This status line indicates converter status. $\overline{BUSY}$ is low during conversion.
9	CLKIN	Clock Input. TTL-compatible logic input. Used as the clock source for the A/D converter. The mark/space ratio of the clock can vary from 40/60 to 60/40.
10	DGND	Digital Ground.
11 . . . 22	DB0–DB11	Three-State Data Outputs. These become active when $\overline{CS}$ and $\overline{RD}$ are brought low.
23	MODE	MODE Input. This input is used to put the device into the power save mode (MODE = 0 V). During normal operation, the MODE input will be a logic high (MODE = V_{DD}).
24	V_{DD}	Power Supply. This is nominally +5 V.

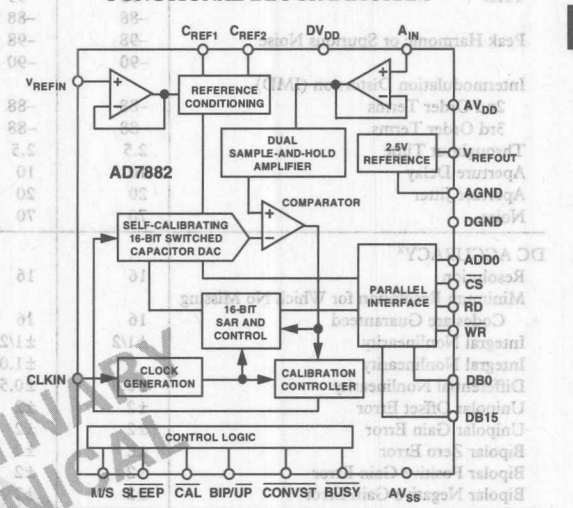
LC²MOS 16-Bit, 2.5 µs, Sampling ADC

AD7882

FEATURES
- 2.5 µs Throughput Time
- 16-Bit Sampling ADC
- Self-Calibration
- High Speed Parallel Interface
- 92 dB Signal-to-Noise Ratio
- Low Power: 200 mW typ
  - 1 mW in Power-Down Mode
- Unipolar and Bipolar Input Signal Ranges
- On-Chip 2.5 V Reference
- Operates from ±5 V Supplies

APPLICATIONS
- Data Acquisition Systems
- Digital Signal Processing
- Spectrum Analysis
- DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7882 is a fast, 16-bit self-calibrating A/D converter. It consists of a sample-and-hold amplifier, a self-calibrating 16-bit ADC, a 2.5 V reference and versatile interface logic. An on-chip controller manages the self-calibrating algorithm that reduces linearity, offset and gain errors to ±0.0015%. System offset and gain errors, caused by external conditioning circuitry, can also be included in the calibration procedure. Throughput time is minimized at 2.5 µs by the use of a dual sample-and-hold amplifier. The ADC also has a self-contained internal clock which is laser trimmed to guarantee accurate control of conversion time; alternatively, an external clock may be used.

Another feature of the AD7882 is a power-down mode that reduces power dissipation from its normal operating value of 200 mW to 1 mW.

The AD7882 operates from ±5 V supplies. Analog input ranges can be unipolar, 0 to 2.5 V or bipolar, ±2.5 V. The analog input bandwidth is 200 kHz.

In addition to traditional dc accuracy specifications such as linearity, the AD7882 is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio (SNR).

The AD7882 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power high-speed CMOS logic. The part is available in a 44-pin plastic quad flatpack (PQFP) and 40-pin cerdip.

PRODUCT HIGHLIGHTS

1. Fast 2.5 µs Throughput Time
   A fast 2.5 µs throughput time makes the AD7882 suitable for a wide range of data acquisition applications.
2. Self-Calibration Achieves High Accuracy
   A self-calibrating algorithm minimizes linearity, offset and gain errors. The calibration procedure can also include external offset and gain errors.
3. Dynamic Specifications for DSP Users
   In addition to traditional dc specifications, the AD7882 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
4. Fast, Versatile Microprocessor Interface
   Fast bus access times and standard control signals make the AD7882 easy to interface to microprocessors.
5. Low Power
   Low power monolithic solution allows ease of application. The AD7882 also has a power down facility.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7882–SPECIFICATIONS (AV_{DD} = 5 V ± 5%, DV_{DD} = 5 V ± 5%, AV_{SS} = –5 V ± 5%, V_{REFIN} = 2.5 V, AGND = DGND = 0 V, f_{CLKIN} = 10 MHz, f_{SAMPLE} = 400 kHz. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A, S Versions[1]	B, T Versions[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal to (Noise + Distortion Ratio)	90	90	dB min	A_{IN} = 10 kHz, Typical SNR = 92 dB
	85	85	dB min	A_{IN} = 100 kHz, Typical SNR = 87 dB
THD	–95	–95	dB max	A_{IN} = 10 kHz, Typical THD = –100 dB
	–88	–88	dB max	A_{IN} = 100 kHz, Typical THD = –90 dB
Peak Harmonic or Spurious Noise	–98	–98	dB max	A_{IN} = 10 kHz, Typical Peak Harmonic = –100 dB
	–90	–90	dB max	A_{IN} = 100 kHz, Typical Peak Harmonic = –92 dB
Intermodulation Distortion (IMD)				
2nd Order Terms	–88	–88	dB max	f_A = 98 kHz, f_B = 100 kHz
3rd Order Terms	–88	–88	dB max	
Throughput Time	2.5	2.5	µs max	
Aperture Delay	10	10	ns typ	
Aperture Jitter	20	20	ps typ	
Noise	70	70	µV rms typ	
DC ACCURACY[2]				
Resolution	16	16	Bits	
Minimum Resolution for Which No Missing Codes are Guaranteed	16	16	Bits	
Integral Nonlinearity	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1.0	LSB max	
Differential Nonlinearity	±0.9	±0.5	LSB max	
Unipolar Offset Error	±2	±2	LSB max	
Unipolar Gain Error	±2	±2	LSB max	
Bipolar Zero Error	±2	±2	LSB max	
Bipolar Positive Gain Error	±2	±2	LSB max	
Bipolar Negative Gain Error	±2	±2	LSB max	
POWER SUPPLY REJECTION				
AV_{DD} Only	84	84	dB typ	
AV_{SS} Only	84	84	dB typ	
ANALOG I/P				
Input Current	±1	±1	µA max	Input Range = 0 V to +2.5 V or ±2.5 V
Input Capacitance[3]	20	20	pF max	
REFERENCE OUTPUT				
V_{REFOUT} @ +25°C	2.5	2.5	Volts Nominal	±1%
V_{REFOUT} Tempco	20	20	ppm/°C typ	
REFERENCE INPUT				
V_{REFIN} Range	2.5	2.5	Volts	±2%
V_{REFIN} Current	±1	±1	µA max	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	Volts min	
Input Low Voltage, V_{INL}	0.8	0.8	Volts max	
Input Current	±10	±10	µA max	
Input Capacitance[3]	10	10	pF max	
$\overline{SLEEP}$ INPUT				
Input High Voltage, V_{INH}	V_{DD} – 0.2	V_{DD} – 0.2	Volts min	
Input Low Voltage, V_{INL}	0.2	0.2	Volts max	
CLKIN INPUT				
Negative Trigger Level	–2	–2	Volts min	This is the Trigger Level for Choosing Internal Clock Operation of the Device

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	A, S Versions[1]	B, T Versions[1]	Units	Test Conditions/Comments
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	2.4	2.4	Volts min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	Volts max	I_{SINK} = 1.6 mA
DB15–DB0				
Floating-State Leakage Current	±10	±10	μA max	
Floating-State Output Capacitance[3]	20	20	pF max	
POWER REQUIREMENTS				
DV_{DD}	+5	+5	Volts	±5%
AV_{DD}	+5	+5	Volts	±5%
AV_{SS}	–5	–5	Volts	±5%
Normal Mode				
DI_{DD}	1	1	mA max	
AI_{DD}	29	29	mA max	
AI_{SS}	27	27	mA max	
Power Dissipation	300	300	mW max	Typically 200 mW, CLKIN not Running
Sleep Mode				
DI_{DD}	40	40	μA max	
AI_{DD}	50	50	μA max	
AI_{SS}	40	40	μA max	
Power Dissipation	1	1	mW max	Typically 500 μW, Input Logic Levels of 0.2 V and V_{DD} – 0.2 V, CLKIN Not Running. Typically 1.5 mW with CLKIN Running

NOTES
[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S, T Versions: –55°C to +125°C.
[2]Specifications apply after calibration.
[3]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	(All Versions)	(A, B Versions)	(S, T Versions)	Units	Conditions/Comments
t_1	10	15	20	ns min	ADD0 to $\overline{WR}$ Setup Time
t_2	5	5	10	ns min	ADD0 to $\overline{WR}$ Hold Time
t_3	10	15	20	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_4	5	5	10	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_5	30	40	50	ns min	$\overline{WR}$ Pulse Width
t_6	30	40	50	ns min	Data Setup Time
t_7	5	5	10	ns min	Data Hold Time
$t_{CONVERT}$	**22 t_{CLKIN}**	**22 t_{CLKIN}**	**22 t_{CLKIN}**		Conversion Time: Synchronous Operation
	2.3	**2.3**	**2.3**	µs max	Conversion Time: Internal Clock Operation
t_{SAMPLE}	**25 t_{CLKIN}**	**25 t_{CLKIN}**	**25 t_{CLKIN}**		Time Between Samples: Synchronous Operation
	2.6	**2.6**	**2.6**	µs max	Time Between Samples: Internal Clock Operation
t_8	30	40	50	ns min	$\overline{CONVST}$ Pulse Width
t_9	20	30	40	ns max	$\overline{CONVST}$ High to BUSY Low Delay
t_{10}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_{11}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{12}	40	50	60	ns min	$\overline{RD}$ Pulse Width
t_{13}[2]	40	50	60	ns max	$\overline{RD}$ Low to Data Valid Delay (Data Access Time)
t_{14}[3]	10	10	10	ns min	Data Hold Time After $\overline{RD}$ (Bus Relinquish Time)
	75	75	75	ns max	
t_{15}	10	15	20	ns min	ADD0 to $\overline{RD}$ Setup Time
t_{16}	5	5	10	ns min	ADD0 to $\overline{RD}$ Hold Time
t_{17}	40	40	50	ns min	New Data Valid before Rising Edge of $\overline{BUSY}$
t_{18}	20	30	40	ns max	CLKIN Falling Edge to $\overline{BUSY}$ Low Delay
t_{19}	10	20	30	ns min	$\overline{CS}$ to $\overline{CAL}$ Setup Time
t_{20}	0	0	0	ns min	$\overline{CS}$ to $\overline{CAL}$ Hold Time
t_{21}	30	40	50	ns min	$\overline{CAL}$ Pulse Width
t_{22}	20	30	40	ns max	$\overline{CAL}$ High to $\overline{BUSY}$ Low Delay
t_{23}	20	30	40	ns max	$\overline{CONVST}$ High to $\overline{BUSY}$ Low Delay: System CAL Mode
$t_{CAL\,1}$	9276744 t_{CLKIN}				Device Calibration Time: Device CAL Mode
$t_{CAL\,2}$	6359324 t_{CLKIN}				DAC Calibration Time: System CAL Mode
$t_{CAL\,3}$	1475104 t_{CLKIN}				Offset Calibration Time: System CAL Mode
$t_{CAL\,4}$	1442324 t_{CLKIN}				Gain Calibration Time: System CAL Mode

NOTES

[1]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_{13} is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_{14} is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time, t_{14}, quoted in the Timing Specifications is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice

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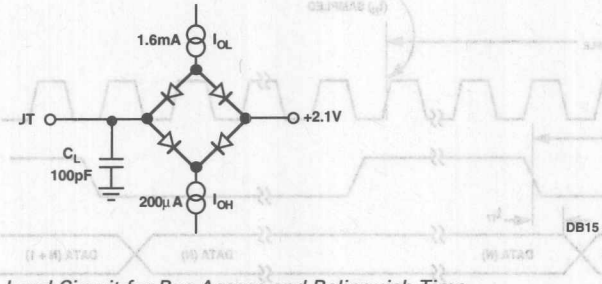


Figure 1. Load Circuit for Bus Access and Relinquish Time

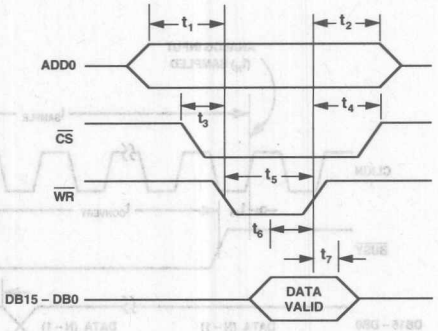


Figure 2. Write Timing Diagram

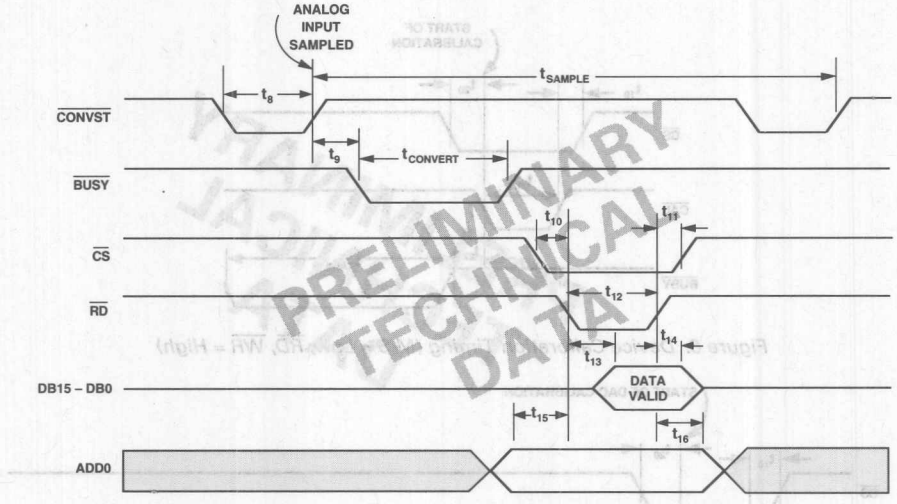


Figure 3. Read Timing Diagram, Asynchronous Operation (M/S = Low; $\overline{CAL}$ = High)

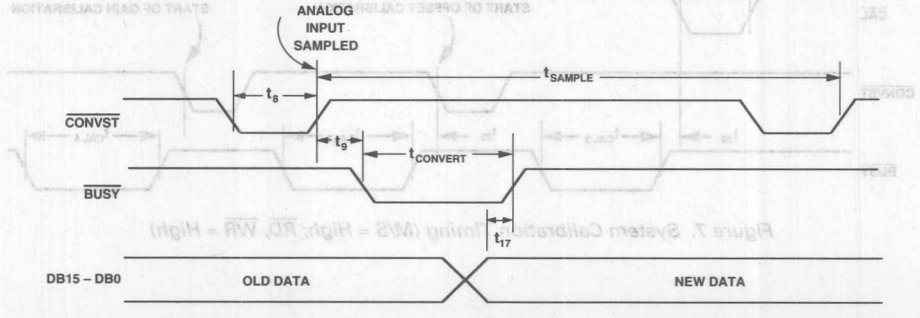


Figure 4. Read Timing Diagram, Asynchronous Operation (M/S, $\overline{CS}$, $\overline{RD}$, ADD0 = Low; $\overline{CAL}$ = High)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

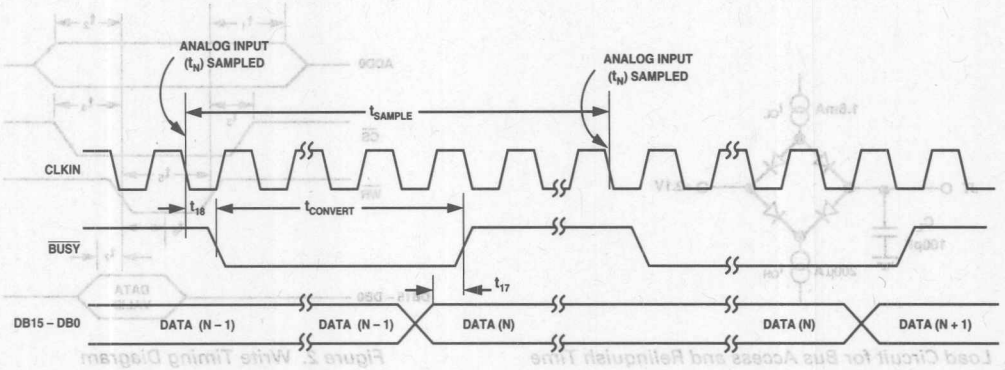


Figure 5. Read Timing Diagram, Synchronous Operation ($\overline{CS}$, $\overline{RD}$ = Low: M/S, $\overline{CAL}$ = High)

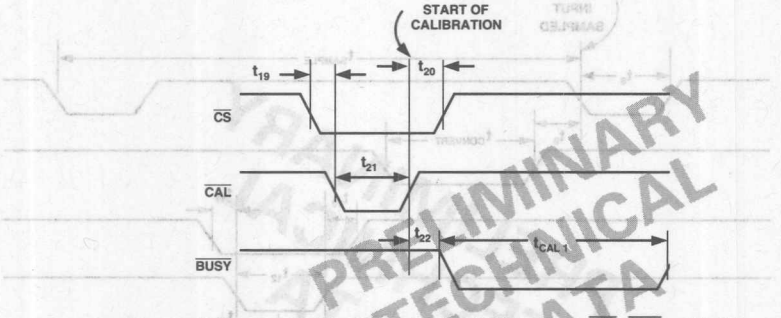


Figure 6. Device Calibration Timing (M/S = Low; $\overline{RD}$, $\overline{WR}$ = High)

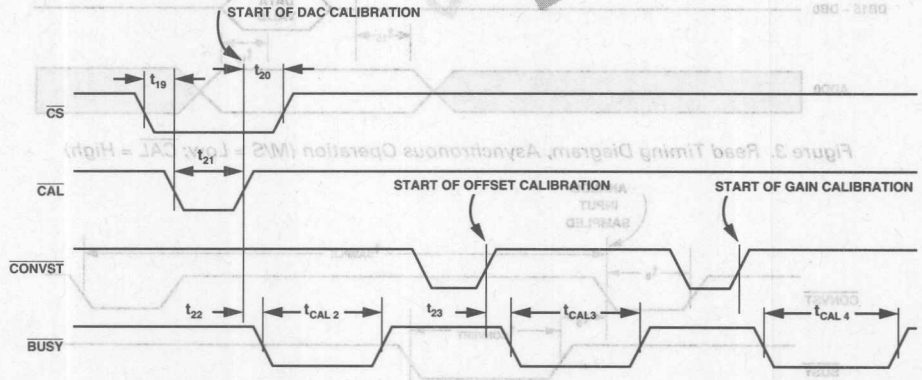


Figure 7. System Calibration Timing (M/S = High; $\overline{RD}$, $\overline{WR}$ = High)

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

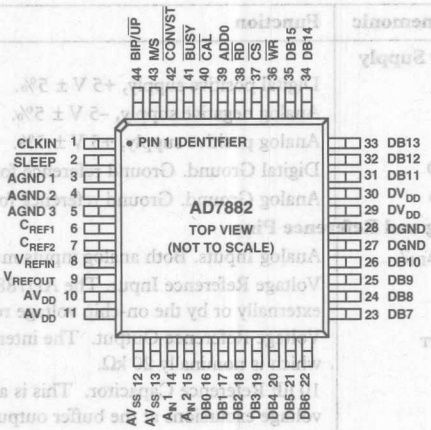
AV_{DD} to AGND ..... –0.3 V to +7 V
AV_{SS} to AGND ..... +0.3 V to –7 V
AGND to DGND ..... –0.3 V to +0.3 V
AV_{DD} to DV_{DD} ..... –0.3 V to +0.3 V
Analog Inputs to AGND ..... AV_{SS} – 0.3 V to AV_{DD} + 0.3 V
Reference Inputs to AGND ... AV_{SS} – 0.3 V to AV_{DD} + 0.3 V
Digital Inputs to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Digital Outputs to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
  Commercial Plastic (A, B Versions) ..... –40°C to +85°C
  Extended Hermetic (S, T Versions) ..... –55°C to +125°C
Storage Temperature Range. ..... –65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Cerdip Package, Power Dissipation ..... 1000 mW
  θ_{JA} Thermal Impedance ..... 50°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C
PQFP Package, Power Dissipation ..... .875 mW
  θ_{JA} Thermal Impedance ..... 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C

NOTES

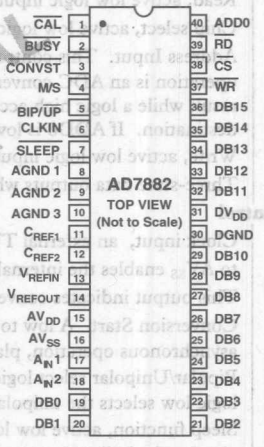
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

PQFP Pinout



Cerdip Pinout



PRELIMINARY TECHNICAL DATA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7882 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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Power Supply	
DV_{DD}	Digital positive supply, +5 V ± 5%.
AV_{SS}	Analog negative supply, –5 V ± 5%.
AV_{DD}	Analog positive supply, +5 V ± 5%.
DGND	Digital Ground. Ground reference for digital circuitry.
AGND	Analog Ground. Ground reference for analog circuitry.
Analog and Reference Pins	
$A_{IN}1$, $A_{IN}2$	Analog Inputs. Both analog inputs must be tied together. The input ranges are; 0 V to 2.5 V and ±2.5 V.
V_{REFIN}	Voltage Reference Input. The AD7882 is specified with a voltage reference of 2.5 V, which can be provided externally or by the on-chip voltage reference.
V_{REFOUT}	Voltage Reference Output. The internal 2.5 V reference is provided at this pin. It has an output impedance which is nominally 20 kΩ.
C_{REF1}	10 µF Reference Capacitor. This is a charge reservoir for the coarse internal reference buffer, and it damps voltage excursions at the buffer output. This must be a high quality, low series inductance capacitor.
C_{REF2}	0.2 µF Reference Capacitor. This is a charge reservoir for the fine internal reference buffer, and it damps voltage excursions at the buffer output. This must be a high quality, low series inductance capacitor.
Interface	
$\overline{RD}$	Read, active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the three-state data outputs.
$\overline{CS}$	Chip select, active low logic input. The device is selected when this input is active.
ADD0	Address Input. This control input determines whether the word placed on the output data bus during a read operation is an ADC conversion result or the contents of the control register. A logic low accesses a conversion result while a logic high accesses the control register. When writing, if ADD0 is high, the control register is the destination. If ADD0 is low, the calibration data memory is the destination.
$\overline{WR}$	Write, active low logic input. This input is used in conjunction with $\overline{CS}$ and ADD0 to write data to the AD7882.
DB15–DB0	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Data output coding is 2s complement binary.
Timing and Control	
CLKIN	Clock input, an external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to AV_{SS} enables the internal clock oscillator.
$\overline{BUSY}$	This output indicates converter status. $\overline{BUSY}$ is low during conversion and calibration.
$\overline{CONVST}$	Conversion Start. A low to high transition on this logic input pin, when the AD7882 is configured for asynchronous operation, places the sample-and-hold amplifier in the hold mode and starts conversion.
BIP/$\overline{UP}$	Bipolar/Unipolar select logic input. A logic high selects the bipolar input range (A_{IN} Range = $\pm V_{REFIN}$), and a logic low selects the unipolar range (A_{IN} Range = 0 to V_{REFIN}).
$\overline{SLEEP}$	Sleep function, active low logic input. Once asserted, the AD7882 enters the low power mode. All internal circuitry including the internal voltage reference is powered down. Calibration data is retained.
$\overline{CAL}$	Active low logic input. A logic low on this input resets all internal logic and initiates a calibration. Initiating a calibration overrides all other internal operations and if a conversion is in progress, it will be terminated.
M/S	Mode/Sync Logic Input. This is a dual function pin. When the device is in the CAL mode ($\overline{CAL}$ input low), it determines the calibration mode. When the device is in the normal operating mode, it determines whether conversion is synchronous or asynchronous. Synchronous operation means that the device continuously converts the input in synchronism with the clock. Asynchronous operation means that the device converts the analog input in response to the application of a $\overline{CONVST}$ signal. See Table I for the $\overline{CAL}$, M/S Truth Table. Note that the control register can be used to disable this input pin. See Control Register Section.

Table I. AD7882 Operating Modes

$\overline{CAL}$	M/S	Function
1	0	Asynchronous Operation
1	1	Synchronous Operation
0	0	Device Calibration
0	1	System Calibration

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TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed in LSBs.

Differential Nonlinearity/No Missed Codes
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC. Differential linearity error is expressed in LSBs. A differential linearity error of ±0.9 LSB or less guarantees no missed codes to the full resolution of the device. Thus, the AD7882 has no missed codes guaranteed to 16 bits.

Unipolar Offset Error
When the device is operating in the 0 to $+V_{REFIN}$ range, the deviation of the first code transition from the ideal (+0.5 LSB) is the unipolar offset error. It is expressed in LSBs.

Unipolar Gain Error
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal (V_{REFIN} – 1.5 LSB) after bipolar zero error has been adjusted out.

Bipolar Zero Error
This is the deviation of the midscale transition (all 0s to all 1s) from the ideal (AGND).

Positive Gain Error
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal (V_{REFIN} – 1.5 LSB) after bipolar zero error has been adjusted out.

Negative Gain Error
This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal ($-V_{REFIN}$ + 0.5 LSB) after bipolar zero error has been adjusted out.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise +distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ \text{dB}$$

Thus for a 16-bit converter, this is 98 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7882, it is defined as

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

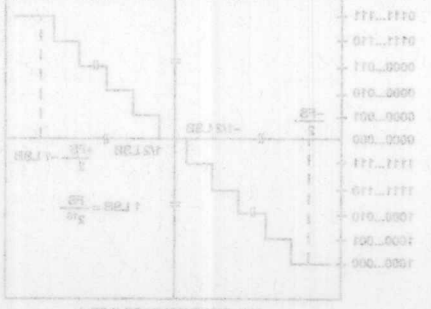
where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7882 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Power Supply Rejection Ratio
This is the ratio, in dBs, of the change in positive gain error to the change in AV_{DD}, DV_{DD} or AV_{SS}. It is a dc measurement.



PRELIMINARY TECHNICAL DATA

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CIRCUIT DESCRIPTION

Analog Input

The analog input circuitry includes two SHAs in a ping-pong configuration as in Figure 8. The SHAs alternatively acquire the analog input and hold the output constant for the ADC conversions. During conversion, one of the SHAs is in the hold mode while the other is in the sample mode. The sample and

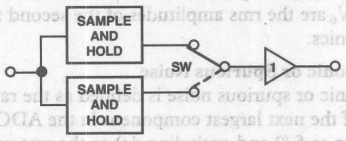

Figure 8. Input SHA Configuration

hold states are then switched after every conversion. The benefit of this configuration is to eliminate the need for acquisition time between conversions. The throughput time is now effectively equal to the conversion time which is 2.5 µs. The analog input range can be either unipolar or bipolar depending on the status of the BIP/$\overline{UP}$ input. The transfer function for the unipolar range is straight binary while the transfer function for the bipolar input is 2s complement. These are shown in Figures 9 and 10.

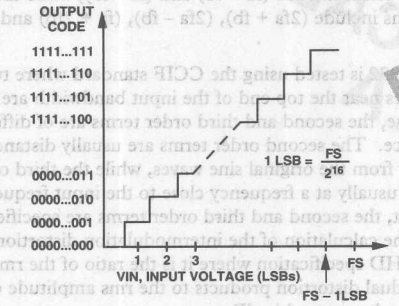

Figure 9. Unipolar Transfer Function

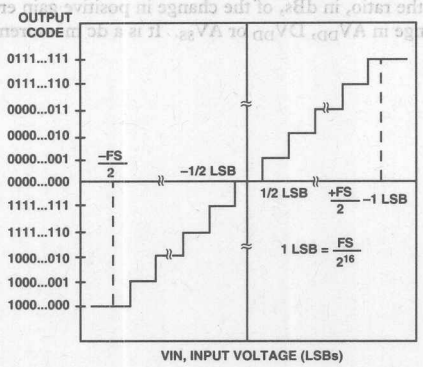

Figure 10. Bipolar Transfer Function

Calibration

The AD7882 conversion procedure is based on the successive approximation algorithm. Accuracy of the individual components, such as the DAC and comparator, is critical to achieve 16-bit performance. The comparator uses an autozero technique to null both internal and external offsets. Another advantage of this scheme is that it nulls 1/f noise. The autozero switching occurs well above the 1/f roll-off frequency, thus the noise appears as a dc offset which gets cancelled.

The internal DAC uses binary weighted capacitors instead of the traditional R-2 R ladder type. This allows the AD7882 to employ a calibration routine that nulls the errors of the individual DAC segments along with offset and gain errors. Each segment of the capacitor DAC contains multiple capacitors that are used to trim for absolute accuracy. During a calibration routine, the DAC segments are compared against other segments and trimmed to 1/4 LSB accuracy. Offset and gain errors are then calibrated either against the device AGND and V_{REFIN} inputs or external reference voltages that are applied at the A_{IN} input.

Calibration Routine

The AD7882 is capable of two calibration methods; system calibration and device calibration. Both modes calibrate the internal DAC linearity along with offset and gain errors. A system calibration is where the device calibrates its full scale and offset voltages against externally applied voltages. For a device calibration, full scale and offset are calibrated against the V_{REFIN} and AGND inputs. Note that a calibration must always be initiated after power on to meet the device performance specifications.

Calibration may be initiated in hardware by asserting the $\overline{CAL}$ pin or in software by writing the appropriate word to the control register. The AD7882 will always perform a full calibration if initiated in hardware. However, under software control, partial calibration options including only offset and gain, can be performed. These options are shown in Table III.

Device Calibration

Device calibration is initiated by pulsing $\overline{CAL}$ low; see Figure 6. Offset and gain are calibrated against the AGND and V_{REFIN} inputs respectively. This calibration procedure takes 928 ms, when using a 10 MHz clock.

System Calibration

System calibration is initiated by a positive edge on $\overline{CAL}$ as shown in Figure 7. $\overline{BUSY}$ goes low three times during the calibration procedure corresponding to the DAC, offset and gain calibrations respectively. The rising edge of the first $\overline{BUSY}$ pulse indicates that the DAC calibration is complete and the AD7882 is now ready to calibrate the offset. This is achieved by applying an external 0 V input at the A_{IN} input and asserting the $\overline{CONVST}$ input. Note, the external 0 V input must be within ±1.5% of AGND. The rising edge of the second $\overline{BUSY}$ pulse indicates that the part is ready to calibrate full scale. This time, the full scale input voltage must be applied to the analog input, and $\overline{CONVST}$ must be asserted once again. The full-scale input voltage must be within ±1.5% of the reference input voltage. Complete calibration time is 928 ms plus the width of the two $\overline{CONVST}$ start pulses, when using a 10 MHz clock for the device.

PRELIMINARY TECHNICAL DATA

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Configuring the M/S Input

The M/S input with conjunction with the $\overline{CAL}$ input determines the type of calibration initiated when $\overline{CAL}$ is taken low. It also determines whether the conversion is asynchronous (controlled by the $\overline{CONVST}$ input) or synchronous (with CLKIN). In all, they can be configured in four different ways as shown in Figure 11. The $\overline{CAL}$ input is asserted by a positive edge, when calibration is required. Then, for example if synchronous operation and device calibration is required, M/S is tied to $\overline{CAL}$. Note, an inverter can be used between the $\overline{CAL}$ and the M/S inputs when asynchronous operation and system calibration is required.

If $\overline{CAL}$ is high, then the user can start a Calibration from the Control Register.

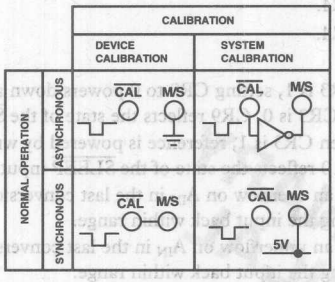

Figure 11. M/S Input Configuration

Timing and Control

Data communication with the AD7882 is controlled by four control inputs: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ and ADD0. The data transfer consists of reading and writing to the control register or coefficients register and reading the conversion result from the output data register.

Conversion Control and Data Reads

Conversion can be controlled in hardware by asserting the $\overline{CONVST}$ input (Asynchronous Mode) or the device can be set up for continuous "back-to-back" conversions (Synchronous Mode). The M/S input controls these as outlined above. In synchronous mode, a power-up, CAL or CONVST will initiate operation.

The data outputs are controlled by the $\overline{CS}$ and $\overline{RD}$ inputs. The possible timing configurations are shown in Figures 3, 4 and 5. If $\overline{CS}$ and $\overline{RD}$ are tied permanently low, then the data bus will always be active. However, it will change state at the end of conversion to reflect the most recent result. Reading the data bus must be avoided at this time.

Control Register

The control register serves the dual function of providing control and monitoring the status of the AD7882. This register is directly accessible through the data bus with a read or write operation while ADD0 is high. One of the option settings in the control register is to set up the coefficients register for reading or writing. The coefficient registers contain the calibration coefficients. Loading the coefficients to the register consists of writing forty 16-bit words. This activity is considerably shorter for almost any processor than performing a calibration. Thus, a typical application might read all the coefficients after calibration, store them in the backup memory and rewrite them to the AD7882 in future power-up initialization routines. Reading the calibration coefficients consists of forty read cycles to the AD7882. This will return forty 16-bit words to the microprocessor.

Writing to the AD7882

Data can be written to either the control register or the coefficients register. A typical timing diagram is shown in Figure 12.

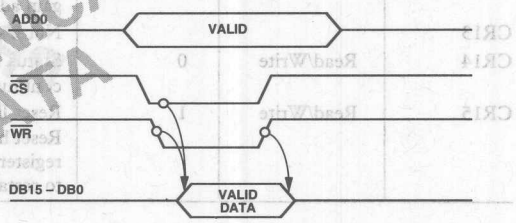

Figure 12. Typical Write Timing

PRELIMINARY TECHNICAL DATA

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Table II. Control Register Bit Functions

Bit Location	I/O Option	Power-Up Default	Function
CR0	Read Only	0	Conversion status. This bit is high during conversion.
CR1	Read Only	0	Calibration status. This bit is high during calibration.
CR2	Read/Write	BIP/$\overline{UP}$	BIP/$\overline{UP}$ Select. Unipolar operation is selected when CR2 is 0; bipolar operation is selected when CR2 is 1. This assumes that CR3 is 1. When CR3 is 0, CR2 reflects the BIP/$\overline{UP}$ input.
CR3	Read/Write	0	If CR3 = 1, then Control Register bits CR2, CR9 and CR10 have priority. Otherwise external pins, $\overline{SLEEP}$ and BIP/$\overline{UP}$, have priority.
CR4	Read/Write	0	CR4 to CR7 determine the calibration function, see Table III.
CR5	Read/Write	1	Calibration function, See CR4.
CR6	Read/Write	1	Calibration function, See CR4.
CR7	Read/Write	1	Calibration function, See CR4.
CR8			Not Used
CR9	Read/Write	$\overline{SLEEP}$	Sleep Control Bit. When CR3 is 1, setting CR9 to 0 powers down all circuitry except the reference. When CR3 is 0, CR9 reflects the state of the $\overline{SLEEP}$ input.
CR10	Read/Write	$\overline{SLEEP}$	Reference power down. When CR3 is 1, reference is powered by writing a 0 to CR10. When CR3 is 0, CR10 reflects the state of the $\overline{SLEEP}$ input.
CR11	Read	0	A 1 in this location indicates an overflow on A_{IN} in the last conversion and a gain adjust is required to bring the input back within range.
CR12	Read	0	A 1 in this location indicates an underflow on A_{IN} in the last conversion and a gain adjust is required to bring the input back within range.
CR13			Not Used
CR14	Read/Write	0	Status Bit. If this is 1, it means that the calibration is halted. Calibration can be continued by writing a 0 to this location.
CR15	Read/Write	1	Reset Bit. All memory and logic is reset when a 0 is written to this location. Reset happens on the rising edge of $\overline{WR}$. If there is a subsequent control register read all bits except CR15 will have power-up default setting. Therefore, to restart after a software reset, it is necessary to write a 1 back into CR15.

Table III. Calibration Options Using the Control Register

CR7	CR6	CR5	CR4	Function
0	0	0	0	Normal Conversion, No Calibration
0	0	0	1	Normal Conversion, No Calibration
0	0	1	0	Gain Error Only–Device Calibration
0	0	1	1	Gain Error Only–System Calibration
0	1	0	0	Offset Error Only–Device Calibration
0	1	0	1	Offset Error Only–System Calibration
0	1	1	0	Offset and Gain Error Only–Device Calibration
0	1	1	1	Offset and Gain Error Only–System Calibration
1	0	0	0	Read All Calibration Coefficients
1	0	0	1	Write All Calibration Coefficients
1	0	1	0	Read Gain Calibration Coefficients Only
1	0	1	1	Write Gain Calibration Coefficients Only
1	1	0	0	Read Offset Calibration Coefficients Only
1	1	0	1	Write Offset Calibration Coefficients Only
1	1	1	0	Full Device Calibration
1	1	1	1	Full System Calibration

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LC²MOS 12-Bit, 3.3 V Sampling ADC

AD7883

FEATURES

Battery-Compatible Supply Voltage: Guaranteed Specs for V_{DD} of 3 V to 3.6 V
12-Bit Monolithic A/D Converter
50 kHz Throughput Rate
15 µs Conversion Time
5 µs On-Chip Track/Hold Amplifier
Low Power
Power Save Mode: 1 mW typ
Normal Operation: 8 mW typ
70 dB SNR
Small 24-Lead SOIC and 0.3" DIP Packages

APPLICATIONS

Battery Powered Portable Systems
Laptop Computers

GENERAL DESCRIPTION

The AD7883 is a high speed, low power, 12-bit A/D converter which operates from a single +3 V to +3.6 V supply. It consists of a 5 µs track/hold amplifier, a 15 µs successive-approximation ADC, versatile interface logic and a multiple-input-range circuit. The part also includes a power save feature.

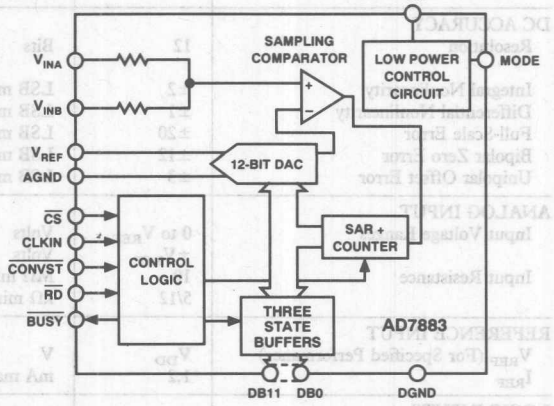
Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

The AD7883 features a total throughput time of 20 µs and can convert full power signals up to 25 kHz with a sampling frequency of 50 kHz.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7883 is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7883 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3 inch-wide, plastic dual-in-line package (DIP) as well as a small 24-lead SOIC package.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. 3 V Operation
   The AD7883 is guaranteed and tested with a supply voltage of 3 V to 3.6 V. This makes it ideal for battery-powered applications where 12-bit A/D conversion is required.
2. Fast Conversion Time
   15 µs conversion time and 5 µs acquisition time allow for large input signal bandwidth. This performance is ideally suited for applications in areas such as telecommunications, audio, sonar and radar signal processing.
3. Low Power Consumption
   1 mW power consumption in the power-down mode makes the part ideally suited for portable, hand held, battery powered applications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

DYNAMIC PERFORMANCE[2]			
Signal-to-Noise Ratio[3] (SNR)	69	dB min	Typically SNR Is 71 dB V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 50 kHz
Total Harmonic Distortion (THD)	−80	dB typ	V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 50 kHz
Peak Harmonic or Spurious Noise	−80	dB typ	V_{IN} = 1 kHz, f_{SAMPLE} = 50 kHz
Intermodulation Distortion (IMD)			
Second Order Terms	−80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 50 kHz
DC ACCURACY			
Resolution	12	Bits	All DC ACCURACY Specifications Apply for the Two Analog Input Ranges
Integral Nonlinearity	±2	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±20	LSB max	
Bipolar Zero Error	±12	LSB max	
Unipolar Offset Error	±3	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{REF}	Volts	See Figure 4
	±V_{REF}	Volts	See Figure 5
Input Resistance	10	MΩ min	0 to V_{REF} Range
	5/12	kΩ min/max	8 kΩ typical: ±V_{REF} Range
REFERENCE INPUT			
V_{REF} (For Specified Performance)	V_{DD}	V	
I_{REF}	1.2	mA max	
LOGIC INPUTS			
$\overline{CONVST}$, RD, $\overline{CS}$, CLKIN			
Input High Voltage, V_{INH}	2.1	V min	
Input Low Voltage, V_{INL}	0.6	V max	
Input Current, I_{IN}	±10	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	pF max	
MODE INPUT			
Input High Voltage, V_{INH}	V_{DD} −0.2	V	
Input Low Voltage, V_{INL}	0.2	V	
Input Current, I_{IN}	±100	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	pF max	
LOGIC OUTPUTS			
DB11–DB0, $\overline{BUSY}$			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 0.8 mA
DB11–DB0			
Floating-State Leakage Current	±10	μA max	
Floating-State Output Capacitance[4]	10	pF max	
CONVERSION			
Conversion Time	15	μs max	f_{CLKIN} = 2 MHz
Track/Hold Acquisition Time	5	μs max	
POWER REQUIREMENTS			
V_{DD}	+3.3	V nom	+3 V to +3.6 V for Specified Performance
I_{DD}			
Normal Power Mode @ +25°C	3	mA max	Typically 2 mA; MODE = V_{DD}
T_{MIN} to T_{MAX}	4	mA max	Typically 2.5 mA; MODE = V_{DD}
Power Save Mode @ +25°C	400	μA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V; Typically 250 μA
T_{MIN} to T_{MAX}	800	μA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V; Typically 300 μA
Power Dissipation			
Normal Power Mode @ +25°C	11	mW max	V_{DD} = 3.6 V: Typically 8 mW; MODE = V_{DD}
T_{MIN} to T_{MAX}	15	mW max	V_{DD} = 3.6 V: Typically 9 mW; MODE = V_{DD}
Power Save Mode @ +25°C	1.5	mW max	V_{DD} = 3.6 V: Typically 1 mW; MODE = 0 V
T_{MIN} to T_{MAX}	3	mW max	V_{DD} = 3.6 V: Typically 1 mW; MODE = 0 V

NOTES
[1]Temperature range is as follows: B Versions: −40°C to +85°C.
[2]V_{IN} = 0 to V_{REF}.
[3]SNR calculation includes distortion and noise components.
[4]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +3 V to +3.6 V, V_{REF} = V_{DD}, AGND = DGND = 0 V)

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (All Versions)	Units	Conditions/Comments
t_1	50	60	ns min	$\overline{CONVST}$ Pulse Width
t_2	200	200	ns max	$\overline{CONVST}$ to $\overline{BUSY}$ Falling Edge
t_3	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Setup Time
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_5	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6	110	150	ns min	$\overline{RD}$ Pulse Width
t_7[2]	100	140	ns max	Data Access Time after $\overline{RD}$
t_8[3]	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	90	90	ns max	

NOTES

[1]Timing specifications in bold print are 100% production tested. All other times are sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_7 is measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_8 is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

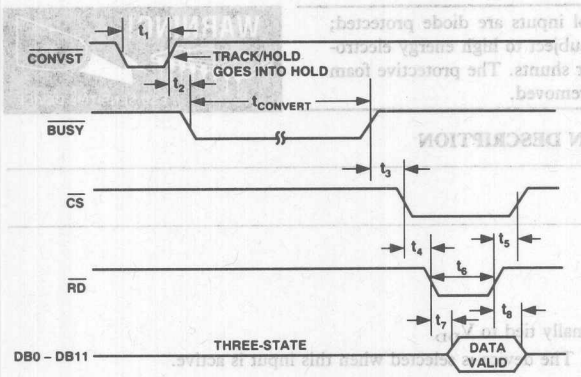


Figure 1. Timing Diagram

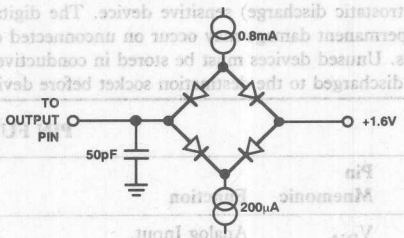


Figure 2. Load Circuit for Access and Relinquish Time

Table I. AD7883 Truth Table

$\overline{CS}$	$\overline{CONVST}$	$\overline{RD}$	Function
1	1	X	Not Selected
1	↓	1	Start Conversion
0	1	0	Enable ADC Data
0	1	1	Data Bus Three Stated

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7883BN	−40°C to +85°C	N-24
AD7883BR	−40°C to +85°C	R-24

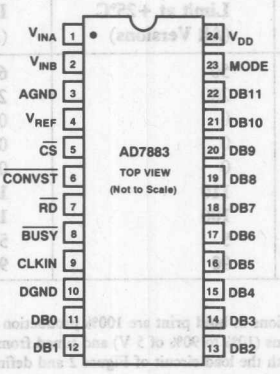
*N = Plastic DIP; R = SOIC (Small Outline Integrated Circuit).
For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{DD} to DGND . . . . . −0.3 V to +7 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
V_{INA}, V_{INB} to AGND (Fig 4) . . . . . −0.3 V to V_{DD} +0.3 V
V_{INA} to AGND (Fig 5) . . . . . $-V_{DD}$−0.3 V to V_{DD}+0.3 V
V_{REF} to AGND . . . . . 0.3 V to V_{DD}
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Industrial (B Version) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
1	V_{INA}	Analog Input.
2	V_{INB}	Analog Input.
3	AGND	Analog Ground.
4	V_{REF}	Voltage Reference Input. This is normally tied to V_{DD}.
5	$\overline{CS}$	Chip Select. Active Low Logic input. The device is selected when this input is active.
6	$\overline{CONVST}$	Convert Start. A low to high transition on this input puts the track/hold into hold mode and starts conversion. This input is asynchronous to the CLKIN and is independent of $\overline{CS}$ and $\overline{RD}$.
7	$\overline{RD}$	Read. Active Low Logic Input. This input is used in conjunction with $\overline{CS}$ low to enable data outputs.
8	$\overline{BUSY}$	Active Low Logic Output. This status line indicates converter status. $\overline{BUSY}$ is low during conversion.
9	CLKIN	Clock Input. TTL-compatible logic input. Used as the clock source for the A/D converter. The mark/space ratio of the clock can vary from 40/60 to 60/40.
10	DGND	Digital Ground.
11 . . . 22	DB0–DB11	Three-State Data Outputs. These become active when $\overline{CS}$ and $\overline{RD}$ are brought low.
23	MODE	MODE Input. This input is used to put the device into the power save mode (MODE = 0 V). During normal operation, the MODE input will be a logic high (MODE = V_{DD}).
24	V_{DD}	Power Supply. This is nominally +3.3 V.

ANALOG DEVICES

LC²MOS 16-Bit, High Speed Sampling ADCs

AD7884/AD7885

FEATURES
Monolithic Construction
Fast Conversion: 5.3 μs
High Throughput: 166 kSPS
Low Power: 250 mW

APPLICATIONS
Automatic Test Equipment
Medical Instrumentation
Industrial Control
Data Acquisition Systems
Robotics

GENERAL DESCRIPTION

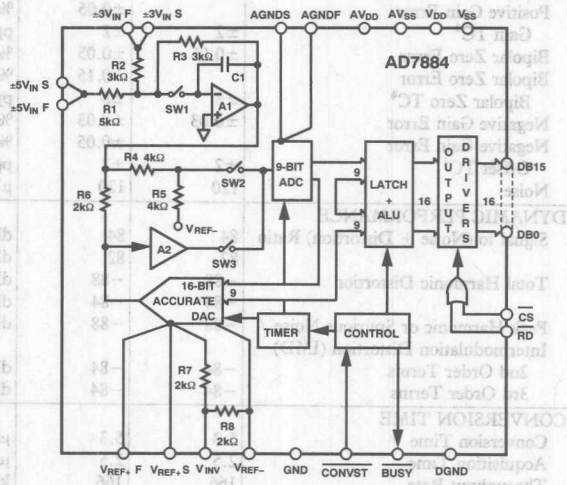
The AD7884/AD7885 is a 16-bit monolithic analog-to-digital converter with internal sample-and-hold and a conversion time of 5.3 μs. The maximum throughput rate is 166 kSPS. It uses a two pass flash architecture to achieve this speed. Two input ranges are available: ±5 V and ±3 V. Conversion is initiated by the $\overline{\text{CONVST}}$ signal. The result can be read into a microprocessor using the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs on the device. The AD7884 has a 16-bit parallel reading structure while the AD7885 has a byte reading structure. The conversion result is in 2s complement code.

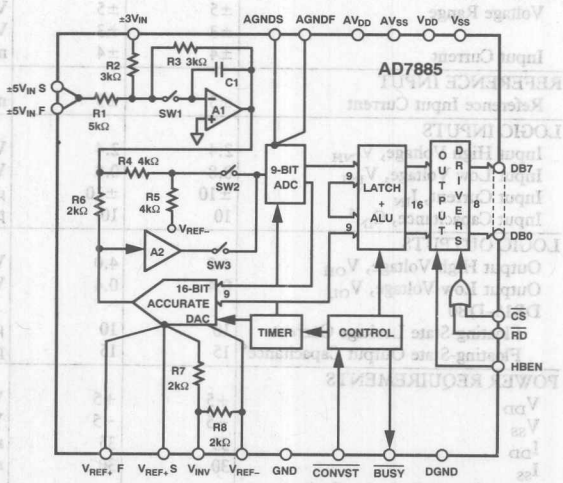
The AD7884/AD7885 has its own internal oscillator which controls conversion. It runs from ±5 V supplies and needs a V_{REF+} of +3 V.

The AD7884 is available in a 40-pin plastic DIP package and in a 44-pin PLCC package.

The AD7885 is available in a 28-pin plastic DIP package and the AD7885A is available in a 44-pin PLCC package.

FUNCTIONAL BLOCK DIAGRAMS





This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter	A Version[1, 2, 3]	B Version[1, 2, 3]	Units	Test Conditions/Comments
DC ACCURACY				
Resolution	16	16	Bits	
Minimum Resolution for Which				
No Missing Codes Are Guaranteed	16	16	Bits	
Integral Nonlinearity		±0.006	% FSR max	Typically 0.003% FSR
Positive Gain Error	±0.03	±0.03	% FSR typ	AD7885AN/BN: 0.1% typ
Positive Gain Error		±0.05	% FSR max	AD7885BN: 0.2% max
Gain TC[4]	±2	±2	ppm FSR/°C typ	
Bipolar Zero Error	±0.05	±0.05	% FSR typ	
Bipolar Zero Error		±0.15	% FSR max	
Bipolar Zero TC[4]	±8	±8	ppm FSR/°C typ	
Negative Gain Error	±0.03	±0.03	% FSR typ	AD7885AN/BN: 0.1% typ
Negative Gain Error		±0.05	% FSR max	AD7885BN: 0.2% max
Offset TC[4]	±2	±2	ppm FSR/°C typ	
Noise	120	120	μV rms typ	78 μV rms typical in ±3 V Input Range
DYNAMIC PERFORMANCE				
Signal to (Noise + Distortion) Ratio	84	84	dB min	Input Signal: ±5 V, 1 kHz Sine Wave, Typically 86 dB
	82	82	dB typ	Input Signal: ±5 V, 12 kHz Sine Wave
Total Harmonic Distortion	−88	−88	dB max	Input Signal: ±5 V, 1 kHz Sine Wave
	−84	−84	dB typ	Input Signal: ±5 V, 12 kHz Sine Wave
Peak Harmonic or Spurious Noise	−88	−88	dB max	Input Signal: ±5 V, 1 kHz Sine Wave
Intermodulation Distortion (IMD)				
2nd Order Terms	−84	−84	dB typ	f_A = 11.5 kHz, f_B = 12 kHz, f_{SAMPLE} = 166 kHz
3rd Order Terms	−84	−84	dB typ	f_A = 11.5 kHz, f_B = 12 kHz, f_{SAMPLE} = 166 kHz
CONVERSION TIME				
Conversion Time	5.3	5.3	μs max	
Acquisition Time	2.5	2.5	μs max	
Throughput Rate	166	166	kSPS max	There is an overlap between conversion and acquisition.
ANALOG INPUT				
Voltage Range	±5	±5	Volts	
	±3	±3	Volts	
Input Current	±4	±4	mA max	
REFERENCE INPUT				
Reference Input Current	±5	±5	mA max	V_{REF} + S = +3 V
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V± 5%
Input Current, I_{IN}	±10	±10	μA max	Input Level = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB15–DB0				
Floating-State Leakage Current	10	10	μA max	
Floating-State Output Capacitance[4]	15	15	pF max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	35	35	mA max	Typically 25 mA
I_{SS}	30	30	mA max	Typically 25 mA
Power Supply Rejection Ratio				
$\Delta Gain/\Delta V_{DD}$	86	86	dB typ	
$\Delta Gain/\Delta V_{SS}$	86	86	dB typ	
Power Dissipation	325	325	mW max	Typically 250 mW

NOTES

[1]Temperature Ranges are as follows: A, B Versions: −40°C to +85°C.

[2]V_{IN} = ±5 V.

[3]The AD7885AAP has the same specs as the AD7884AP.
The AD7885ABP has the same specs as the AD7884BP.

[4]Sample tested to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = GND = 0 V. See Figures 2, 3, 4 and 5.)

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (A, B Versions)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	100	100	ns max	$\overline{CONVST}$ to $\overline{BUSY}$ Low Delay
t_3	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_4	60	60	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	57	57	ns max	Data Access Time after $\overline{RD}$
t_7[3]	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	50	50	ns max	
t_8	40	40	ns min	New Data Valid before Rising Edge of $\overline{BUSY}$
t_9	10	80	ns min	HBEN to $\overline{RD}$ Setup Time
t_{10}	25	25	ns min	HBEN to $\overline{RD}$ Hold Time
t_{11}	60	60	ns min	HBEN Low Pulse Duration
t_{12}	60	60	ns min	HBEN High Pulse Duration
t_{13}	55	70	ns max	Propagation Delay from HBEN Falling to Data Valid
t_{14}	55	70	ns max	Propagation Delay from HBEN Rising to Data Valid

NOTES

[1]Timing specifications in **bold** print are 100% production tested. All other times are sample tested at +5°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_6 is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time, t_7, quoted in the Timing Characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice.

ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error (% FSR)	SNR (dB)	Package Option[2]
AD7884AN	−40°C to +85°C		84	N-40A
AD7884BN	−40°C to +85°C	±0.006	84	N-40A
AD7884AP	−40°C to +85°C		84	P-44A
AD7884BP	−40°C to +85°C	±0.006	84	P-44A
AD7885AN	−40°C to +85°C		84	N-28A
AD7885BN	−40°C to +85°C	±0.006	84	N-28A
AD7885ABP	−40°C to +85°C		84	P-44A
AD7885AAP	−40°C to +85°C	±0.006	84	P-44A

NOTES

[1]Analog Devices reserves the right to ship cerdip (Q) in lieu of plastic DIP.

[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

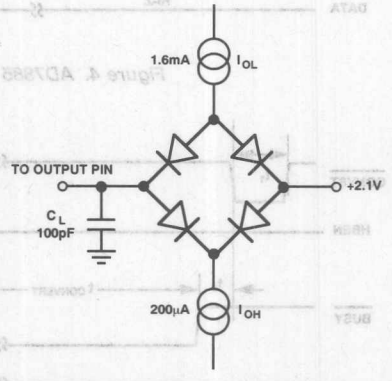


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

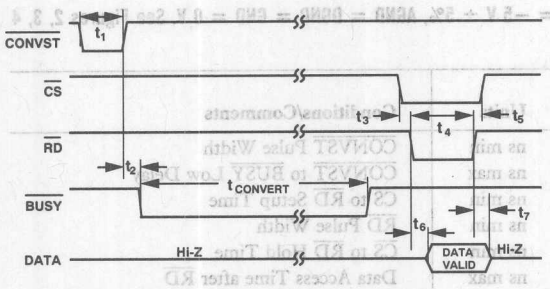


Figure 2. AD7884 Timing Diagram, Using $\overline{CS}$ and $\overline{RD}$

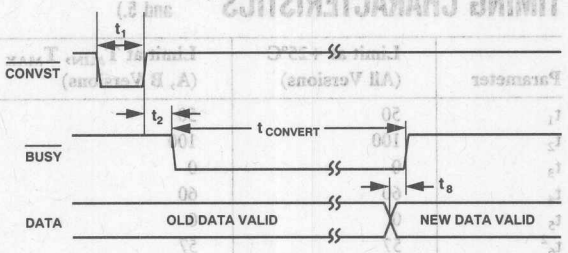


Figure 3. AD7884 Timing Diagram, with $\overline{CS}$ and $\overline{RD}$ Permanently Low

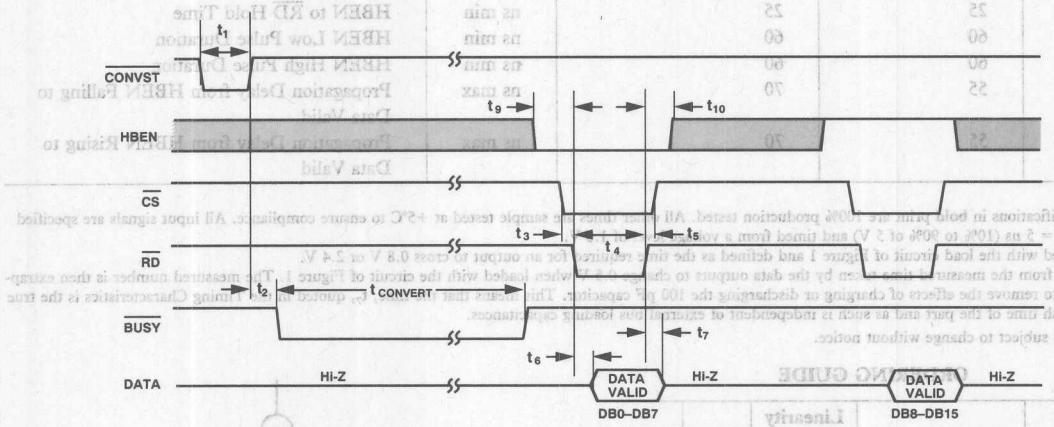


Figure 4. AD7885 Timing Diagram, Using $\overline{CS}$ and $\overline{RD}$

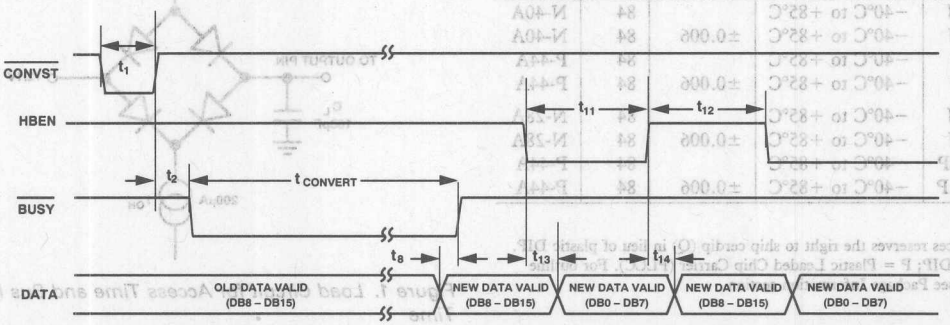


Figure 5. AD7885 Timing Diagram, with $\overline{CS}$ and $\overline{RD}$ Permanently Low

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to AGND . . . . . −0.3 V to +7 V
AV_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AV_{SS} to AGND . . . . . −0.3 V to −7 V
AGND Pins to DGND . . . . . −0.3 V to V_{DD} +0.3 V
AV_{DD} to V_{DD}[2] . . . . . −0.3 V to +7 V
AV_{SS} to V_{SS}[2] . . . . . +0.3 V to −7 V
GND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
$V_{IN}S$, $V_{IN}F$ to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
V_{REF+} to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
V_{REF-} to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
V_{INV} to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V

Operating Temperature Range
Commercial Plastic (A, B Versions) . . . . . −40°C to +85°C
Industrial Cerdip (A, B Versions) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

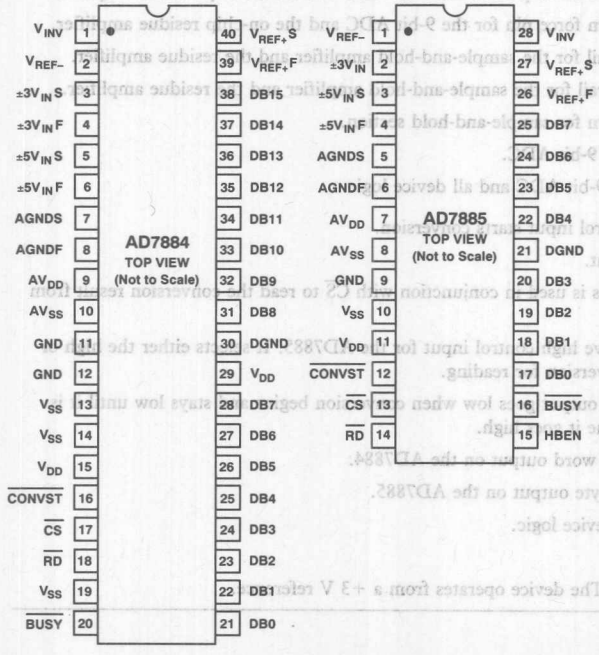
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]If the AD7884/AD7885 is being powered from separate analog and digital supplies, AV_{SS} should always come up before V_{SS}. See Figure 13 for a recommended protection circuit using Schottky diodes.

CAUTION

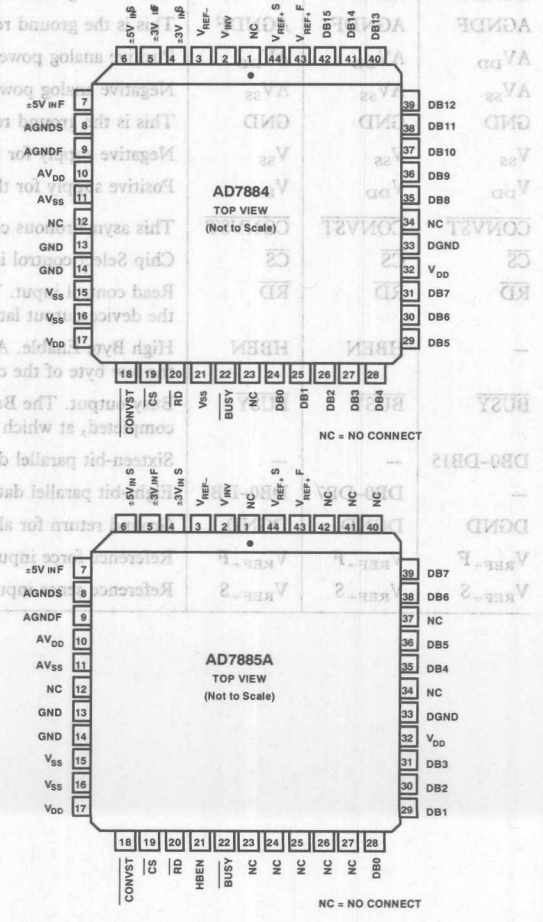
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

DIP



PLCC



PIN FUNCTION DESCRIPTION

AD7884	AD7885	AD7885A	Description
V_{INV}	V_{INV}	V_{INV}	This pin is connected to the inverting terminal of an op amp, as in Figure 6, and allows the inversion of the supplied +3 V reference.
V_{REF-}	V_{REF-}	V_{REF-}	This is the negative reference input, and it can be obtained by using an external amplifier to invert the positive reference input. In this case, the amplifier output is connected to V_{REF-}. See Figure 6.
$\pm 3V_{IN}S$	—	$\pm 3V_{IN}S$	This is the analog input sense pin for the ±3 volt analog input range on the AD7884 and AD7885A.
$\pm 3V_{IN}F$	—	$\pm 3V_{IN}F$	This is the analog input force pin for the ±3 volt analog input range on the AD7884 and AD7885A. When using this input range, the ±5 $V_{IN}F$ and ±5 $V_{IN}S$ pins should be tied to AGND.
—	$\pm 3V_{IN}$	—	This is the analog input pin for the ±3 volt analog input range on the AD7885. When using this input range, the ±5 $V_{IN}F$ and ±5 $V_{IN}S$ pins should be tied to AGND.
$\pm 5V_{IN}S$	$\pm 5V_{IN}S$	$\pm 5V_{IN}S$	This is the analog input sense pin for the ±5 volt analog input range on both the AD7884, AD7885 and AD7885A.
$\pm 5V_{IN}F$	$\pm 5V_{IN}F$	$\pm 5V_{IN}F$	This is the analog input force pin for the ±5 volt analog input range on both the AD7884, AD7885 and AD7885A. When using this input range, the ±3 $V_{IN}F$ and ±3 $V_{IN}S$ pins should be tied to AGND.
AGNDS	AGNDS	AGNDS	This is the ground return sense pin for the 9-bit ADC and the on-chip residue amplifier.
AGNDF	AGNDF	AGNDF	This is the ground return force pin for the 9-bit ADC and the on-chip residue amplifier.
AV_{DD}	AV_{DD}	AV_{DD}	Positive analog power rail for the sample-and-hold amplifier and the residue amplifier.
AV_{SS}	AV_{SS}	AV_{SS}	Negative analog power rail for the sample-and-hold amplifier and the residue amplifier.
GND	GND	GND	This is the ground return for sample-and-hold section.
V_{SS}	V_{SS}	V_{SS}	Negative supply for the 9-bit ADC.
V_{DD}	V_{DD}	V_{DD}	Positive supply for the 9-bit ADC and all device logic.
$\overline{CONVST}$	$\overline{CONVST}$	$\overline{CONVST}$	This asynchronous control input starts conversion.
$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	Chip Select control input.
$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	Read control input. This is used in conjunction with $\overline{CS}$ to read the conversion result from the device output latch.
—	HBEN	HBEN	High Byte Enable. Active high control input for the AD7885. It selects either the high or the low byte of the conversion for reading.
$\overline{BUSY}$	$\overline{BUSY}$	$\overline{BUSY}$	Busy output. The Busy output goes low when conversion begins and stays low until it is completed, at which time it goes high.
DB0–DB15	—	—	Sixteen-bit parallel data word output on the AD7884.
—	DB0–DB7	DB0–DB7	Eight-bit parallel data byte output on the AD7885.
DGND	DGND	DGND	Ground return for all device logic.
$V_{REF+}F$	$V_{REF+}F$	$V_{REF+}F$	Reference force input.
$V_{REF+}S$	$V_{REF+}S$	$V_{REF+}S$	Reference sense input. The device operates from a +3 V reference.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Error
This is the deviation of the midscale transition (all 0s to all 1s) from the ideal (AGND).

Positive Gain Error
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal ($+V_{REF+}$ S − 1 LSB), after Bipolar Zero Error has been adjusted out.

Negative Gain Error
This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal ($-V_{REF+}$S + 1 LSB), after Bipolar Zero Error has been adjusted out.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02N + 1.76)\ dB$$

Thus for an ideal 16-bit converter, this is 98 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7884/AD7885, it is defined as:

$$THD\ (dB) = 20\ log\ \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

The AD7884/AD7885 is tested using the CCIFF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Power Supply Rejection Ratio
This is the ratio, in dBs, of the change in positive gain error to the change in V_{DD} or V_{SS}. It is a dc measurement.

OPERATIONAL DIAGRAM

An operational diagram for the AD7884/AD7885 is shown in Figure 6. It is set up for an analog input range of ±5 V. If a ±3 V input range is required, A1 should drive ±3 V_{IN}S and ±3 V_{IN}F with ±5 V_{IN}S, ±5 V_{IN}F being tied to system AGND.

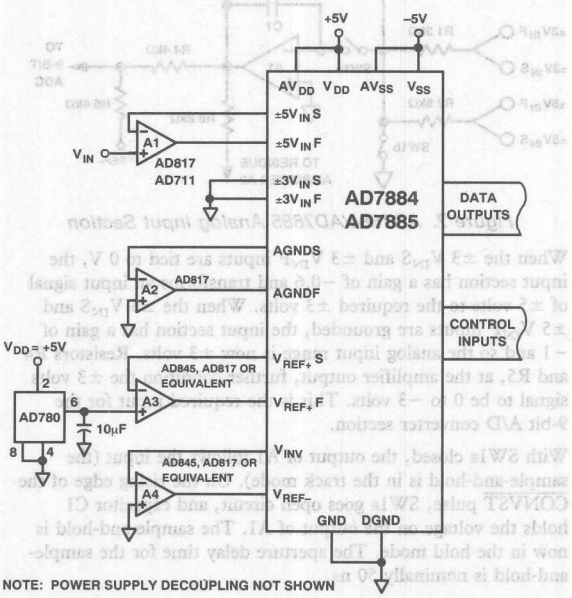


Figure 6. AD7884/AD7885 Operational Diagram

The chosen input buffer amplifier (A1) should have low noise and distortion and fast settling time for high bandwidth applications. Both the AD711 and the AD845 are suitable amplifiers.

A2 is the force, sense amplifier for AGND. The AGNDS pin should be at zero potential. Therefore, the amplifier must have a low input offset voltage and good noise performance. It must also have the ability to deal with fast current transients on the AGNDS pin. The AD817 has the required performance and is the recommended amplifier.

If AGNDS and AGNDF are simply tied together to Star Ground instead of buffering, the SNR and THD are not significantly degraded. However, dc specifications like INL, Bipolar Zero and Gain Error will be degraded.

The required +3 V reference is derived from the AD780 and buffered by the high-speed amplifier A3 (AD845, AD817 or equivalent). A4 is a unity gain inverter which provides the −3 V negative reference. The gain setting resistors are on-chip and are factory trimmed to ensure precise tracking of V_{REF+}. Figure 6 shows A3 and A4 as AD845s or AD817s. These have the ability to respond to the rapidly changing reference input impedance.

CIRCUIT DESCRIPTION

Analog Input Section

The analog input section of the AD7884/AD7885 is shown in Figure 7. It contains both the input signal conditioning and sample-and-hold amplifier. Note that the analog input is truly benign. When SW1a goes open circuit to put the SHA into the hold mode, SW1b is closed. This means that the input resistors, R1 and R2 are always connected to either virtual ground or true ground.

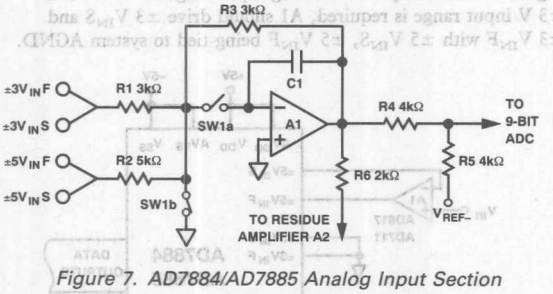


Figure 7. AD7884/AD7885 Analog Input Section

When the ±3 V_{IN}S and ±3 V_{IN}F inputs are tied to 0 V, the input section has a gain of −0.6 and transforms an input signal of ±5 volts to the required ±3 volts. When the ±5 V_{IN}S and ±5 V_{IN}F inputs are grounded, the input section has a gain of −1 and so the analog input range is now ±3 volts. Resistors R4 and R5, at the amplifier output, further condition the ±3 volts signal to be 0 to −3 volts. This is the required input for the 9-bit A/D converter section.

With SW1a closed, the output of A1 follows the input (the sample-and-hold is in the track mode). On the rising edge of the $\overline{\text{CONVST}}$ pulse, SW1a goes open circuit, and capacitor C1 holds the voltage on the output of A1. The sample-and-hold is now in the hold mode. The aperture delay time for the sample-and-hold is nominally 50 ns.

A/D Converter Section

The AD7884/AD7885 uses a two-pass flash technique in order to achieve the required speed and resolution. When the $\overline{\text{CONVST}}$ control input goes from low to high, the sample-and-hold amplifier goes into the hold mode and a 0 V to −3 V signal is presented to the input of the 9-bit ADC. The first phase of conversion generates the 9 MSBs of the 16-bit result and transfers these to the latch and ALU combination. They are also fed back to the 9 MSBs of the 16-bit DAC. The 7 LSBs of the DAC are permanently loaded with 0s. The DAC output is subtracted from the analog input with the result being amplified and offset in the Residue Amplifier Section. The signal at the output of A2 is proportional to the error between the first phase result and the actual analog input signal and is digitized in the second conversion phase. This second phase begins when the 16-bit DAC and the Residue Error Amplifier have both settled. First, SW2 is turned off and SW3 is turned on. Then, the SHA section of the Residue Amplifier goes into hold mode. Next SW2 is turned off and SW3 is turned on. The 9-bit result is transferred to the output latch and ALU. An error correction algorithm now compensates for the offset inserted in the Residue Amplifier Section and errors introduced in the first pass conversion and combines both results to give the 16-bit answer.

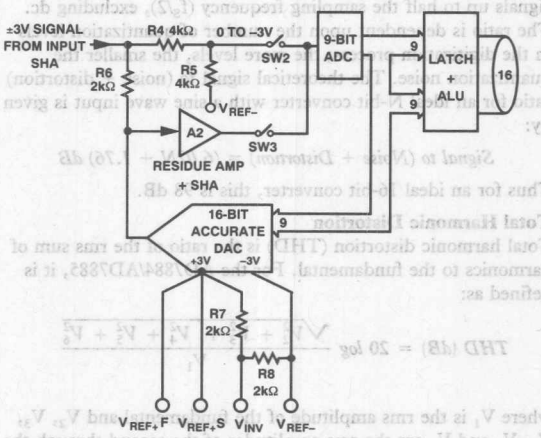


Figure 8. A/D Converter Section

Timing and Control Section

Figure 9 shows the timing and control sequence for the AD7884/AD7885. When the part receives a $\overline{\text{CONVST}}$ pulse, the conversion begins. The input sample-and-hold goes into the hold mode 50 ns after the rising edge of $\overline{\text{CONVST}}$ and $\overline{\text{BUSY}}$ goes low. This is the first phase of conversion and takes 3.35 μs to complete. The second phase of conversion begins when SW2 is turned off and SW3 turned on. The Residue Amplifier and SHA section (A2 in Figure 8) goes into hold mode at this point and allows the input sample-and-hold to go back into sample mode. Thus, while the second phase of conversion is ongoing, the input sample-and-hold is also acquiring the input signal for the next conversion. This overlap between conversion and acquisition allows throughput rates of 166 kSPS to be achieved.

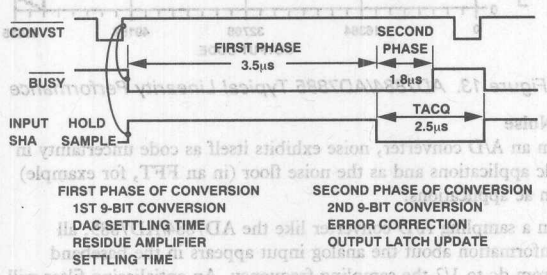


Figure 9. Timing and Control Sequence

USING THE AD7884/AD7885

Analog Input Ranges

The AD7884/AD7885 can be set up to have either a ±3 volts analog input range or a ±5 volts analog input range. Figures 10 and 11 show the necessary corrections for each of these. The output code is 2s complement and the ideal code table for both input ranges is shown in Table I.

Reference Considerations

The AD7884/AD7885 operates from a ±3 volt reference. This can be derived simply using the AD780 as shown in Figure 6.

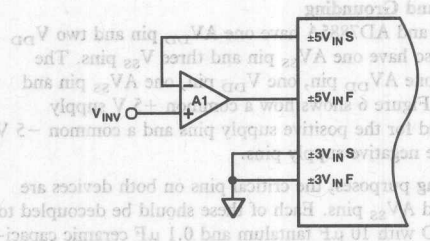


Figure 10. ±5 V Input Range Connection

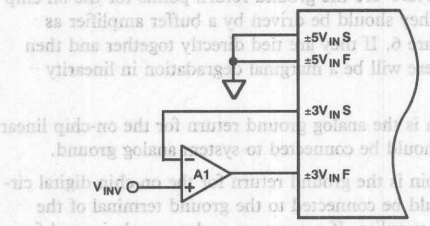


Figure 11. ±3 V Input Range Connections

The critical performance specification for a reference in a 16-bit application is noise. The reference pk-pk noise should be insignificant in comparison to the ADC noise. The AD7884/AD7885 has a typical rms noise of 120 μV. For example a reasonable target would be to keep the total rms noise less than 125 μV. To do this the reference noise needs to be less than 35 μV rms. In the 100 kHz band, the AD780 noise is less than 30 μV rms, making it a very suitable reference.

The buffer amplifier used to drive the device V_{REF+} should have low enough noise performance so as not to affect the overall system noise requirement. The AD845 and AD817 achieve this.

Table I. Ideal Output Code Table for the AD7884/AD7885

Analog Input			Digital Output
In Terms of FSR[2]	±3 V Range[3]	±5 V Range[4]	Code Transition[1]
+FSR/2 − 1 LSB	2.999908	4.999847	011 . . . 111 to 011 . . . 110
+FSR/2 − 2 LSBs	2.999817	4.999695	011 . . . 110 to 011 . . . 101
+FSR/2 − 3 LSBs	2.999726	4.999543	011 . . . 101 to 011 . . . 100
AGND + 1 LSB	0.000092	0.000153	000 . . . 001 to 000 . . . 000
AGND	0.000000	0.000000	000 . . . 000 to 111 . . . 111
AGND − 1 LSB	−0.000092	−0.000153	111 . . . 111 to 111 . . . 110
−(FSR/2 − 3 LSBs)	−2.999726	−4.999543	100 . . . 011 to 100 . . . 010
−(FSR/2 − 2 LSBs)	−2.999817	−4.999695	100 . . . 010 to 100 . . . 001
−(FSR/2 − 1 LSB)	−2.999908	−4.999847	100 . . . 001 to 100 . . . 000

NOTES
[1]This table applies for $V_{REF+}S$ = +3 V.
[2]FSR (Full-Scale Range) is 6 volts for the ±3 V input range and 10 volts for the ±5 V input range.
[3]1 LSB on the ±3 V range is FSR/2^{16} and is equal to 91.5 μV.
[4]1 LSB on the ±5 V range is FSR/2^{16} and is equal to 152.6 μV.

Decoupling and Grounding

The AD7884 and AD7885A have one AV_{DD} pin and two V_{DD} pins. They also have one AV_{SS} pin and three V_{SS} pins. The AD7885 has one AV_{DD} pin, one V_{DD} pin, one AV_{SS} pin and one V_{SS} pin. Figure 6 shows how a common +5 V supply should be used for the positive supply pins and a common −5 V supply for the negative supply pins.

For decoupling purposes, the critical pins on both devices are the AV_{DD} and AV_{SS} pins. Each of these should be decoupled to system AGND with 10 μF tantalum and 0.1 μF ceramic capacitors right at the pins. With the V_{DD} and V_{SS} pins, it is sufficient to decouple each of these with ceramic 1 μF capacitors.

AGNDS, AGNDF are the ground return points for the on-chip 9-bit ADC. They should be driven by a buffer amplifier as shown in Figure 6. If they are tied directly together and then to ground, there will be a marginal degradation in linearity performance.

The GND pin is the analog ground return for the on-chip linear circuitry. It should be connected to system analog ground.

The DGND pin is the ground return for the on-chip digital circuitry. It should be connected to the ground terminal of the V_{DD} and V_{SS} supplies. If a common analog supply is used for AV_{DD} and V_{DD} then DGND should be connected to the common ground point.

Power Supply Sequencing

AV_{DD} and V_{DD} are connected to a common substrate and there is typically 17 Ω resistance between them. If they are powered by separate +5 V supplies, then these should come up simultaneously. Otherwise, the one that comes up first will have to drive +5 V into a 17 Ω load for a short period of time. However, the standard short-circuit protection on regulators like the 7800 series will ensure that there is no possibility of damage to the driving device.

AV_{SS} should always come up either before or at the same time as V_{SS}. If this cannot be guaranteed, Schottky diodes should be used to ensure that V_{SS} never exceeds AV_{SS} by more than 0.3 V. Arranging the power supplies as in Figure 6 and using the recommended decoupling ensures that there are no power supply sequencing issues as well as giving the specified noise performance.

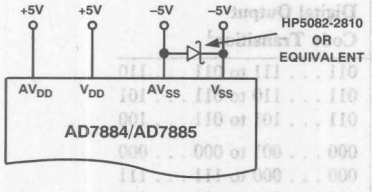


Figure 12. Schottky Diodes Used to Protect Against Incorrect Power Supply Sequencing

AD7884/AD7885 PERFORMANCE

Linearity

The linearity of the AD7884/AD7885 is determined by the on-chip 16-bit D/A converter. This is a segmented DAC which is laser trimmed for 16-bit DNL performance to ensure that there are no missing codes in the ADC transfer function. Figure 13 shows a typical INL plot for the AD7884/AD7885.

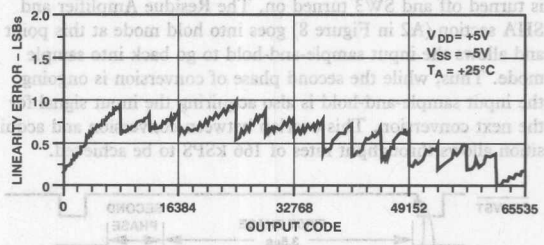


Figure 13. AD7884/AD7885 Typical Linearity Performance

Noise

In an A/D converter, noise exhibits itself as code uncertainty in dc applications and as the noise floor (in an FFT, for example) in ac applications.

In a sampling A/D converter like the AD7884/AD7885, all information about the analog input appears in the baseband from dc to 1/2 the sampling frequency. An antialiasing filter will remove unwanted signals above $f_S/2$ in the input signal but the converter wideband noise will alias into the baseband. In the AD7884/AD7885, this noise is made up of sample-and-hold noise and a/d converter noise. The sample-and-hold section contributes 51 μV rms and the ADC section contributes 59 μV rms. These add up to a total rms noise of 78 μV. This is the input referred noise in the ±3 V analog input range. When operating in the ±5 V input range, the input gain is reduced to −0.6. This means that the input referred noise is now increased by a factor of 1.66 to 120 μV rms.

Figure 14 shows a histogram plot for 5000 conversions of a dc input using the AD7884/AD7885 in the ±5 V input range. The analog input was set as close as possible to the center of a code transition. All codes other than the center code are due to the ADC noise. In this case, the spread is six codes.

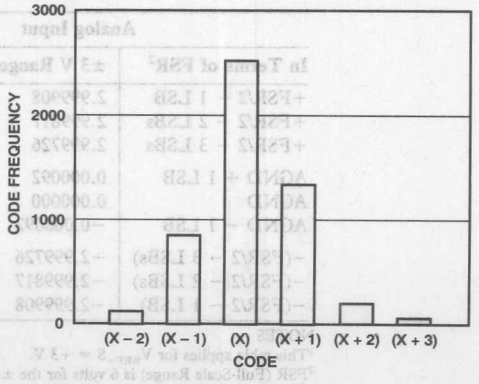


Figure 14. Histogram of 5000 Conversions of a DC Input

If the noise in the converter is too high for an application, it can be reduced by oversampling and digital filtering. This involves sampling the input at higher than the required word rate and then averaging to arrive at the final result. The very fast conversion time of the AD7884/AD7885 makes it very suitable for oversampling. For example, if the required input bandwidth is 40 kHz, the AD7884/AD7885 could be oversampled by a factor of 2. This yields a 3 dB improvement in the effective SNR performance. The noise performance in the ±5 volt input range is now effectively 85 μV rms and the resultant spread of codes for 2500 conversions will be four. This is shown in Figure 15.

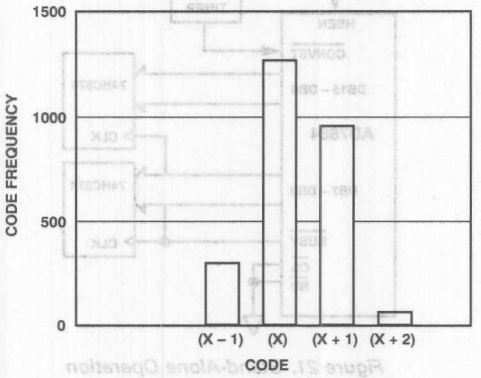


Figure 15. Histogram of 2500 Conversions of a DC Input Using a ×2 Oversampling Ratio

Dynamic Performance

With a combined conversion and acquisition time of 6 μs, the AD7884/AD7885 is ideal for wide bandwidth signal processing applications. Signal to (Noise + Distortion), Total Harmonic Distortion, Peak Harmonic or Spurious Noise and Intermodulation Distortion are all specified. Figure 16 shows a typical FFT plot of a 1.8 kHz, ±5 V input after being digitized by the AD7884/AD7885.

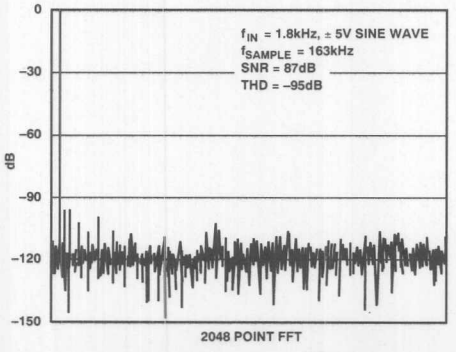


Figure 16. AD7884/AD7885 FFT Plot

Effective Number of Bits

The formula for SNR (see Terminology Section) is related to the resolution or number of bits in the converter. Rewriting the formula, below, gives a measure of performance expressed in effective number of bits (N).

$$N = (SNR - 1.76)/6.02$$

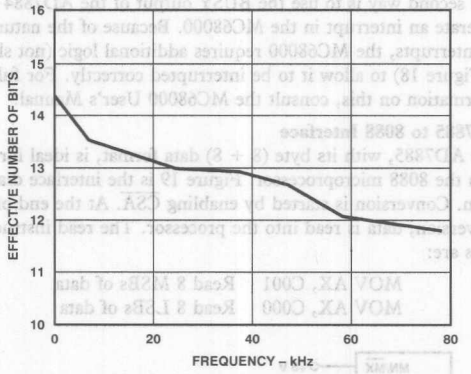


Figure 17. Effective Number of Bits vs. Frequency

The effective number of bits for a device can be calculated from its measured SNR. Figure 17 shows a typical plot of effective number of bits versus frequency for the AD7884. The sampling frequency is 166 kHz.

MICROPROCESSOR INTERFACING

The AD7884/AD7885 is designed on a high speed process which results in very fast interfacing timing (Data Access Time of 57 ns max). The AD7884 has a full 16-bit parallel bus, and the AD7885 has an 8-bit wide bus. The AD7884, with its parallel interface, is suited to 16-bit parallel machines whereas the AD7885, with its byte interface, is suited to 8-bit machines. Some examples of typical interface configurations follow.

AD7884 to MC68000 Interface

Figure 18 shows a general interface diagram for the MC68000, 16-bit microprocessor to the AD7884. In Figure 18, conversion is initiated by bringing $\overline{CSA}$ low (i.e., writing to the appropriate address). This allows the processor to maintain control over the complete conversion process. In some cases it may be more desirable to control conversion independent from the processor. This can be done by using an external sampling timer.

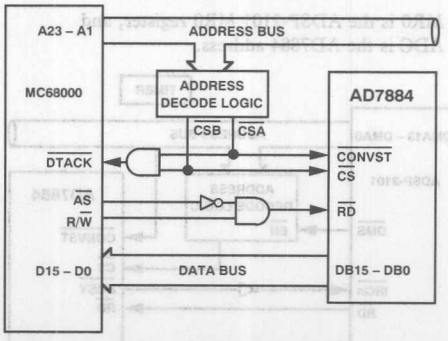


Figure 18. AD7884 to MC68000 Interface

Once conversion has been started, the processor must wait until it is completed before reading the result. There are two ways of ensuring this. The first way is to simply use a software delay to wait for 6.5 μs before bringing $\overline{CS}$ and $\overline{RD}$ low to read the data.

The second way is to use the $\overline{BUSY}$ output of the AD7884 to generate an interrupt in the MC68000. Because of the nature of its interrupts, the MC68000 requires additional logic (not shown in Figure 18) to allow it to be interrupted correctly. For full information on this, consult the MC68000 User's Manual.

AD7885 to 8088 Interface

The AD7885, with its byte (8 + 8) data format, is ideal for use with the 8088 microprocessor. Figure 19 is the interface diagram. Conversion is started by enabling $\overline{CSA}$. At the end of conversion, data is read into the processor. The read instructions are:

```
MOV AX, C001    Read 8 MSBs of data
MOV AX, C000    Read 8 LSBs of data
```

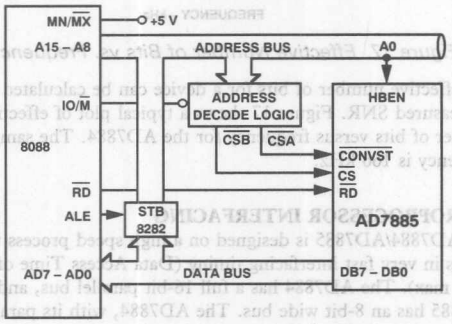


Figure 19. AD7885 to 8088 Interface

AD7884 to ADSP-2101 Interface

Figure 20 shows an interface between the AD7884 and the ADSP-2101. Conversion is initiated using a timer which allows very accurate control of the sampling instant. The AD7884 $\overline{BUSY}$ line provides an interrupt to the ADSP-2101 when conversion is completed. The $\overline{RD}$ pulse width of the processor can be programmed using the Data Memory Wait State Control Register. The result can then be read from the ADC using the following instruction:

$$MR0 = DM (ADC)$$

where MR0 is the ADSP-2101 MR0 register, and
ADC is the AD7884 address.

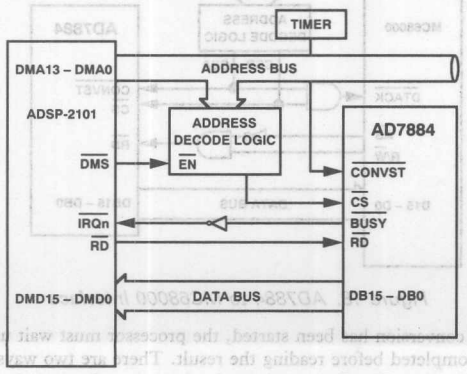


Figure 20. AD7884 to ADSP-2101 Interface

Stand-Alone Operation

If $\overline{CS}$ and $\overline{RD}$ are tied permanently low on the AD7884, then, when a conversion is completed, output data will be valid on the rising edge of $\overline{BUSY}$. This makes the device very suitable for stand-alone operation. All that is required to run the device is an external $\overline{CONVST}$ pulse which can be supplied by a sample timer. Figure 21 shows the AD7884 set up in this mode with the $\overline{BUSY}$ signal providing the clock for the 74HC574 3-state latches.

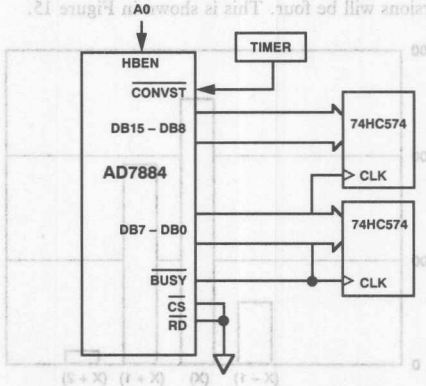
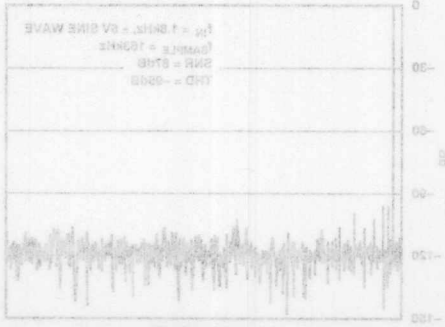


Figure 21. Stand-Alone Operation

Digital Feedthrough from an Active Bus

It is very important when using the AD7884/AD7885 in a microprocessor-based system to isolate the ADC data bus from the active processor bus while a conversion is being executed. This will yield the best noise performance from the ADC. Latches like the 74HC574 can be used to do this. If the device is connected directly to an active bus then the converter noise will typically increase by a factor of 30%.



ANALOG DEVICES

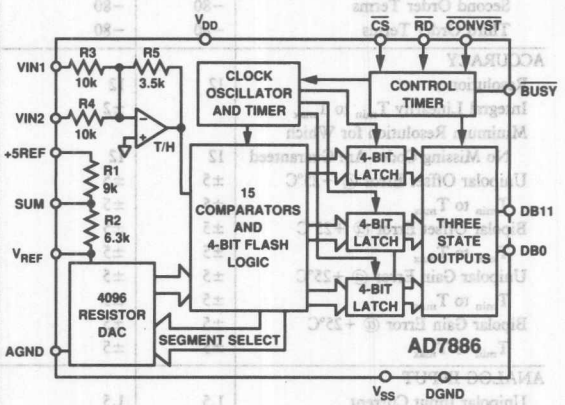
LC²MOS 12-Bit, 750 kHz/1 MHz, Sampling ADC

AD7886

FEATURES
750 kHz/1 MHz Throughput Rate
1 μs/750 ns Conversion Time
12-Bit No Missed Codes Over Temperature
67 dB SNR at 100 kHz Input Frequency
Low Power—250 mW typ
Fast Bus Access Time—57 ns max

APPLICATIONS
Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7886 is 12-bit ADC with a sample-and-hold amplifier offering high speed performance combined with low power dissipation. The AD7886 is a triple pass flash ADC, which uses 15 comparators in a 4-bit flash technique to achieve 12-bit accuracy in 1 μs/750 ns conversion time. An on-chip clock oscillator provides the appropriate timing for each of the three conversion stages eliminating the need for any external clocks. Acquisition time of the sample-and-hold amplifier gives a resulting throughput rate of 750 kHz/1 MHz.*

The AD7886 operates from ±5 V power supplies. Pin-strappable inputs offer a choice of three analog input ranges; 0 to 5 V, 0 to 10 V or ±5 V.

In addition to the traditional dc accuracy specifications such as linearity, offset and full-scale errors, the AD7886 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7886 has a high speed digital interface with three-state data outputs. Conversion control is provided by a $\overline{\text{CONVST}}$ input. Data access is controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs, standard microprocessor signals. The data access time of less than 57 ns means that the AD7886 can interface directly to most modern microprocessors including DSP processors.

***Contact your local salesperson for further information on the 1 MHz version.**

The AD7886 is fabricated in Analog Devices' Linear Compatible CMOS process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic.

The AD7886 is available in both a 28-pin DIP and in a 28-pin leaded chip carrier.

PRODUCT HIGHLIGHTS

1. Fast 1.33 μs/1 μs Throughput Time.
   Fast throughput time makes the AD7886 suitable for a wide range of data acquisition applications.
2. Dynamic Specifications for DSP Users.
   The AD7886 is specified for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion. Key digital timing parameters are also tested and guaranteed over the full operating temperature range.
3. Fast Microprocessor Interface.
   Standard control signals, $\overline{\text{CS}}$ and $\overline{\text{RD}}$, and fast bus access times make the AD7886 easy to interface to microprocessors.
4. Low Power.
   LC²MOS fabrication process gives low power dissipation of 250 mW.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio[3] (SNR)	65	67	65	dB min	VIN = 100 kHz Sine Wave, f_{SAMPLE} = 750 kHz
Total Harmonic Distortion (THD)	−75	−75	−75	dB typ	VIN = 100 kHz Sine Wave, f_{SAMPLE} = 750 kHz
Peak Harmonic or Spurious Noise	−77	−77	−77	dB typ	VIN = 100 kHz Sine Wave, f_{SAMPLE} = 750 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	−80	−80	−80	dB typ	f_a = 96 kHz, f_b = 103 kHz, f_{SAMPLE} = 750 kHz
Third Order Terms	−80	−80	−80	dB typ	
ACCURACY					
Resolution	12	12	12	Bits	
Integral Linearity T_{min} to T_{max}		±2	±2	LSB max	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	12	12	12	Bits	
Unipolar Offset Error @ +25°C	±5	±5	±5	LSB max	Input Range: 0 to 5 V or 0 to 10 V
T_{min} to T_{max}	±5	±5	±5	LSB max	
Bipolar Offset Error @ +25°C	±5	±5	±5	LSB max	Input Range: ±5 V
T_{min} to T_{max}	±5	±5	±5	LSB max	
Unipolar Gain Error @ +25°C	±5	±5	±5	LSB max	Input Range: 0 to 5 V or 0 to 10 V
T_{min} to T_{max}	±5	±5	±5	LSB max	
Bipolar Gain Error @ +25°C	±5	±5	±5	LSB max	Input Range: ±5 V
T_{min} to T_{max}	±5	±5	±5	LSB max	
ANALOG INPUT					
Unipolar Input Current	1.5	1.5	1.5	mA max	Input Ranges: 0 to 5 V or 0 to 10 V
Bipolar Input Current	±0.75	±0.75	±0.75	mA max	Input Range: ±5 V
REFERENCE INPUT					
V_{REF}	−3.5	−3.5	−3.5	Volts	±2% For Specified Performance
Input Reference Current	−10	−10	−10	mA max	
R1, Resistance	9	9	9	kΩ nom	±25%
R2, Resistance	6.3	6.3	6.3	kΩ nom	±25%
R2/R1 Ratio	0.7	0.7	0.7	nom	±0.1%
POWER SUPPLY REJECTION					
V_{DD} Only, (FS Change)	0.5	0.5	0.5	LSB typ	V_{SS} = −5 V, V_{DD} = +4.75 V to +5.25 V
V_{SS} Only, (FS Change)	0.5	0.5	0.5	LSB typ	V_{DD} = +5 V, V_{SS} = −4.75 V to −5.25 V
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	10	pF max	
LOGIC OUTPUTS					
DB11–DB0, $\overline{BUSY}$					
Output High Voltage, V_{OH}	4	4	4	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	±10	±10	±10	μA max	
Floating-State Output Capacitance[4]	15	15	15	pF max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	35	35	35	mA max	Typically 25 mA, $\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = V_{DD}
I_{SS}	−35	−35	−35	mA max	Typically 25 mA, $\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = V_{DD}
Power Dissipation	250	250	250	mW typ	$\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = V_{DD}
	350	350	350	mW max	

NOTES

[1]Temperature ranges are as follows: J, K Versions: 0°C to +70°C; B Version: −40°C to +85°C; T Version: −55°C to +125°C.

[2]Applies to all three input ranges, VIN = 0 to FS, pk-to-pk V.

[3]SNR calculation includes distortion and noise components.

[4]Sample tested @+25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V)

Parameter	Limit at T_{min}, T_{max} (J, K Versions)	Limit at T_{min}, T_{max} (B Version)	Limit at T_{min}, T_{max} (T Version)	Units	Conditions/Comments
t_1	50	50	50	ns min	$\overline{CONVST}$ Pulse Width
	1	1	1	µs max	
t_2	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_4	**60**	**60**	**75**	ns min	$\overline{RD}$ Pulse Width
t_5	100	100	100	ns max	$\overline{CONVST}$ to $\overline{BUSY}$ Propagation Delay, (C_L = 10 pF)
t_6[2]	**57**	**57**	**70**	ns max	Data Access Time After $\overline{RD}$
t_7[3]	**10**	**10**	**10**	ns min	Bus Relinquish Time After $\overline{RD}$
	50	**50**	**60**	ns max	
t_8	20	20	14	ns min	Data Setup Time Prior to $\overline{BUSY}$, (C_L = 20 pF)
	10	10	0	ns min	Data Setup Time Prior to $\overline{BUSY}$, (C_L = 100 pF)
t_9[3]	10	10	10	ns min	Bus Relinquish Time After $\overline{CONVST}$
	100	100	100	ns max	
t_{10}	0	0	0	ns min	$\overline{CS}$ High to $\overline{CONVST}$ Low
t_{11}	0	0	0	ns min	$\overline{BUSY}$ High to $\overline{RD}$ Low
t_{12}	250	250	250	ns typ	$\overline{BUSY}$ High to $\overline{CONVST}$ Low, SHA Acquisition Time
t_{13}	1.333	1.333	1.333	µs min	Sampling Interval
t_{CONV}	950	950	950	ns typ	Conversion Time
	1000	**1000**	**1000**	ns max	

NOTES

[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_6 is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_7 and t_9 are derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the load capacitor, C_L. This means that the times, t_7 and t_9, quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

Specifications subject to change without notice.

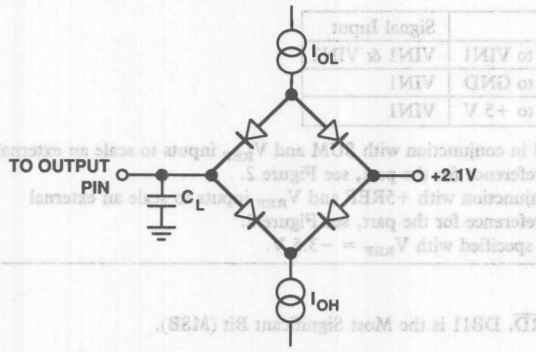


Figure 1. Load Circuit for Bus Access and Relinquish Time

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
VIN1, VIN2, SUM, +5REF to AGND . . . . −15 V to +15 V
V_{REF} to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND
$\overline{CS}$, $\overline{RD}$, $\overline{CONVST}$ . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND
DB0 to DB11, $\overline{BUSY}$ . . . . . −0.3 V to V_{DD} +0.3V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0°C to +70°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]If V_{SS} is open circuited with V_{DD} and AGND applied, the V_{SS} pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V_{SS} to DGND (cathode end to GND) ensures that the Absolute Maximum Ratings will be observed.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

Model[1, 2]	Temperature Range	SNR (dBs)	Integral Nonlinearity (LSBs)	Package Option[3]
AD7886JD	0°C to +70°C	65		D-28
AD7886KD	0°C to +70°C	67	±2.0	D-28
AD7886JP	0°C to +70°C	65		P-28A[2]
AD7886KP	0°C to +70°C	67	±2.0	P-28A[2]
AD7886BD	−40°C to +85°C	67	±2.0	D-28
AD7886TD	−55°C to +125°C	65	±2.0	D-28

NOTES
[1]Contact your sales office for availability of AD7886BD, AD7886TD and 1 MHz version.
[2]Analog Devices reserves the right to ship J-Leaded Ceramic Chip Carrier (JLCCC) in lieu of PLCC packages.
[3]D = Ceramic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN FUNCTION DESCRIPTION

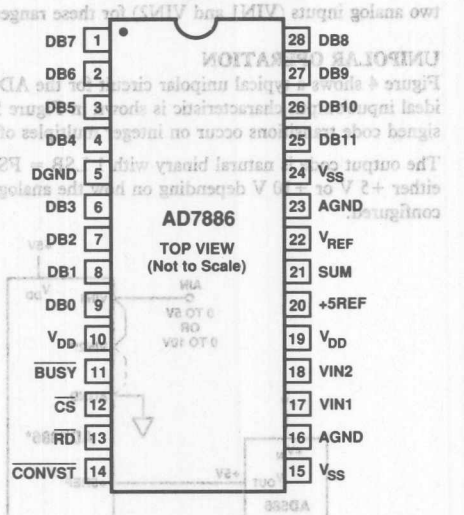
DIP Pin Number	Mnemonic	Description
Power Supply		
10 & 19	V_{DD}	Positive Power Supply, +5 V ± 5%. Both V_{DD} pins must be tied together.
15 & 24	V_{SS}	Negative Power Supply, −5 V ± 5%. Both V_{SS} pins must be tied together.
16 & 23	AGND	Analog Ground. Both AGND pins must be tied together.
5	DGND	Digital Ground.
Analog and Reference Inputs		
17 & 18	VIN	Analog Inputs, VIN1 and VIN2. The part can be pin strapped for any one of three analog input ranges;

Range	Pin Strap	Signal Input
0 to 5 V	Connect VIN2 to VIN1	VIN1 & VIN2
0 to 10 V	Connect VIN2 to GND	VIN1
±5 V	Connect VIN2 to +5 V	VIN1

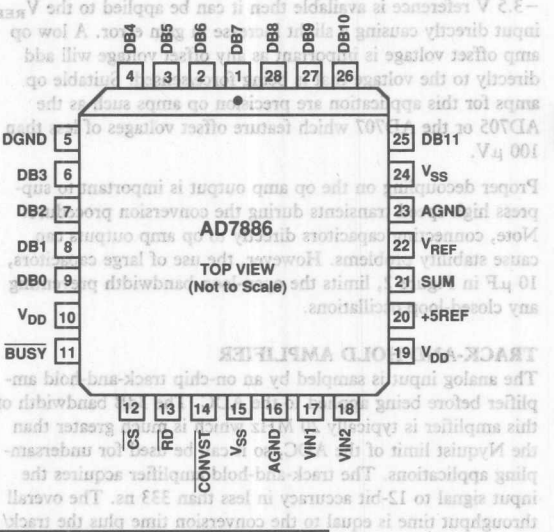
20	+5REF	+5 V Reference input. This input is used in conjunction with SUM and V_{REF} inputs to scale an external +5 V reference to −3.5 V, the required reference for the part, see Figure 2.
21	SUM	Summing Point. This input is used in conjunction with +5REF and V_{REF} inputs to scale an external +5 V reference to −3.5 V, the required reference for the part, see Figure 2.
22	V_{REF}	Voltage Reference Input. The AD7886 is specified with V_{REF} = −3.5 V.
Interface and Control		
1–4,	DB7–DB4	Three-state data outputs.
6–9,	DB3–DB0	These outputs are controlled by $\overline{CS}$ and $\overline{RD}$. DB11 is the Most Significant Bit (MSB).
25–28	DB11–DB8	
11	$\overline{BUSY}$	$\overline{BUSY}$ Output indicates converter status. $\overline{BUSY}$ is low during conversion.
12	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
13	$\overline{RD}$	Read Input. This active low signal, in conjunction with $\overline{CS}$, is used to enable the output data three-state drivers.
14	$\overline{CONVST}$	Conversion Start Input. This input is used to start conversion.

PIN CONFIGURATIONS

DIP



PLCC



TERMINOLOGY

Unipolar Offset Error

The ideal first code transition should occur when the analog input is 1 LSB above AGND. The deviation of the actual transition from that point is termed the offset error.

Bipolar Zero Error

The ideal midscale transition (i.e., 0111 1111 1111 to 1000 0000 0000 for the ±5 V range should occur when the analog input is at zero volts. Bipolar zero error is the deviation of the actual transition from that point.

Gain Error

In the unipolar mode, gain error is measured with respect to the first and last code transition points. The ideal difference between these points if FS−2 LSBs. For bipolar applications, the gain error is measured from the midscale transition to both the first and last code transitions. The ideal difference in this case is FS/2−1 LSB. The gain error is defined as the deviation between the ideal difference, given above, and the measured difference. For the bipolar case, there are two gain errors, the figure in the specification page represents the worst case. Ideal FS depends on the +5REF input; for the 0 to 5 V input, ideal FS = +5REF and for the 0 to 10 V and ±5 V ranges, ideal FS = 2 × +5REF.

CONVERTER DETAILS

The AD7886 is a triple-pass flash ADC which uses 15 comparators in a 4-bit flash technique to perform the 12-bit conversion procedure. Each of the 4096 quantization levels is realized internally with a precision resistor DAC.

The fifteen comparators first compare the analog input voltage to the V_{REF}/16 voltages of the resistor array. This determines the four most significant bits and selects 1 out of 16 voltage segments. The comparators are then switched to 15 subvoltages on that segment to determine the next four bits and select 1 out of 256 voltage segments. A further switching of the comparators to another 15 subvoltages produces the complete 12-bit conversion result. The 12 bits of data are then stored internally in a three-state output latch.

REFERENCE INPUT

The AD7886 operates from a +3.5 V reference which must be provided at the V_{REF} input. Two on-chip resistors for use with an external amplifier can be used for deriving −3.5 V from standard 5 V references. Figure 2 shows an example with the AD586 which a is a high performance voltage reference which exhibits excellent stability performance, 5 ppm/°C max. The external amplifier serves a second function of force/sensing the V_{REF} input. Force/sensing minimizes error contributions from

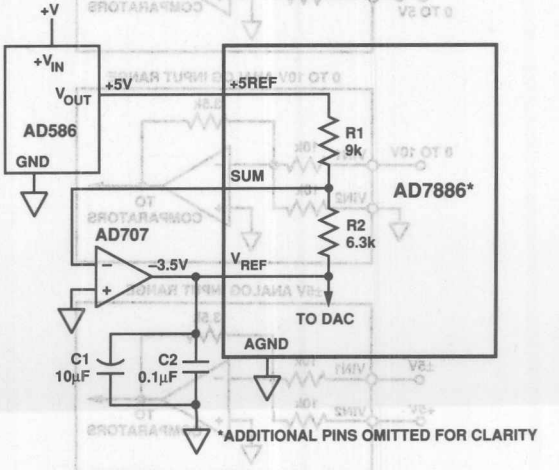


Figure 2. Typical Reference Circuitry

voltage or IR drops along the internal conductors. IR drops in the reference path cause a gain error, and typically the external amplifier reduces this error by 2 LSBs. In systems where a −3.5 V reference is available then it can be applied to the V_{REF} input directly causing a slight increase in gain error. A low op amp offset voltage is important as any offset voltage will add directly to the voltage that is being force/sensed. Suitable op amps for this application are precision op amps such as the AD705 or the AD707 which feature offset voltages of less than 100 μV.

Proper decoupling on the op amp output is important to suppress high speed transients during the conversion procedure. Note, connecting capacitors directly to op amp outputs can cause stability problems. However, the use of large capacitors, 10 μF in Figure 2, limits the open-loop bandwidth preventing any closed-loop oscillations.

TRACK-AND-HOLD AMPLIFIER

The analog input is sampled by an on-chip track-and-hold amplifier before being applied to the ADC. The 3dB bandwidth of this amplifier is typically 20 MHz which is much greater than the Nyquist limit of the ADC, so it can be used for undersampling applications. The track-and-hold amplifier acquires the input signal to 12-bit accuracy in less than 333 ns. The overall throughput time is equal to the conversion time plus the track/hold amplifier acquisition time which is 1.333 μs for the AD7886.

The operation of the track/hold amplifier is essentially transparent to the user. The track-to-hold transition occurs at the start of conversion on the falling edge of $\overline{\text{CONVST}}$. The conversion procedure does not start until the rising edge of $\overline{\text{CONVST}}$. The width of the $\overline{\text{CONVST}}$ pulse low time determines the track-to-hold settling time. The track/hold reverts back to the track mode at the end of conversion when $\overline{\text{BUSY}}$ has returned high.

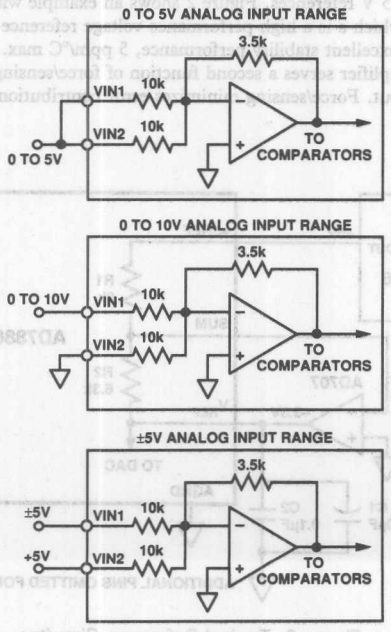


Figure 3. Analog Input Range Configurations

ANALOG INPUT RANGES

The AD7886 has three user selectable analog input ranges: 0 to 5 V, 0 to 10 V and ±5 V. Figure 3 shows how to configure the two analog inputs (VIN1 and VIN2) for these ranges.

UNIPOLAR OPERATION

Figure 4 shows a typical unipolar circuit for the AD7886. The ideal input/output characteristic is shown in Figure 5. The designed code transitions occur on integer multiples of 1 LSB.

The output code is natural binary with 1 LSB = FS/4096. FS is either +5 V or +10 V depending on how the analog inputs are configured.

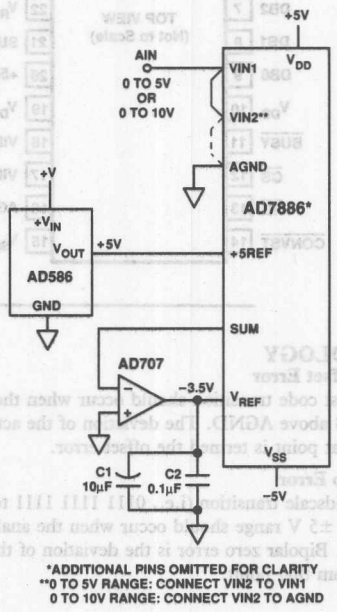


Figure 4. Unipolar Operation

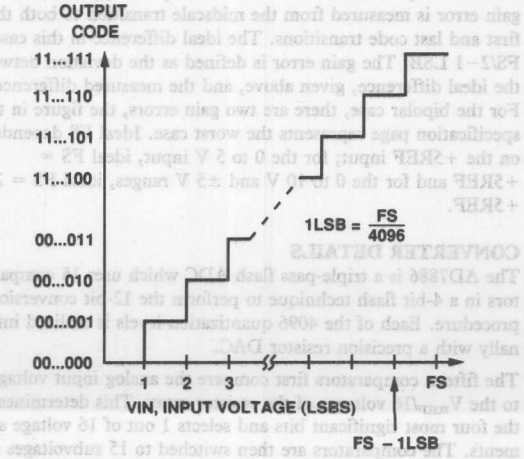


Figure 5. Ideal Input/Output Transfer Characteristic for Unipolar Operation

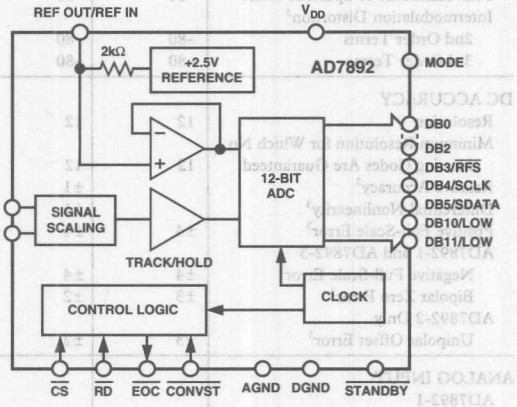
LC²MOS Single Supply, 12-Bit 600 kSPS ADC

AD7892

FEATURES

Fast 12-Bit ADC with 1.3 μs Conversion Time
600 kSPS Throughput Rate (AD7892-3)
500 kSPS Throughput Rate (AD7892-1, AD7892-2)
Single Supply Operation
On-Chip Track/Hold Amplifier
Selection of Input Ranges:
±10 V or ±5 V for AD7892-1
0 V to +2.5 V for AD7892-2
±2.5 V for AD7892-3
High Speed Serial and Parallel Interface
Low Power, 60 mW typ
Overvoltage Protection on Analog Inputs (AD7892-1 and AD7892-3)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7892 is a high speed, low power, 12-bit A/D converter that operates from a single +5 V supply. The part contains a 1.3 μs successive approximation ADC, an on-chip track/hold amplifier, an internal +2.5 V reference and on-chip versatile interface structures that allow both serial and parallel connection to a microprocessor. The part accepts an analog input range of ±10 V or ±5 V (AD7892-1), 0 V to +2.5 V (AD7892-2) and ±2.5 V (AD7892-3). Overvoltage protection on the analog inputs for the AD7892-1 and AD7892-3 allows the input voltage to go to ±17 V or ±7 V respectively without damaging the ports.

The AD7892 offers a choice of two data output formats: a single, parallel, 12-bit word or serial data. Fast bus access times and standard control inputs ensure easy parallel interface to microprocessors and digital signal processors. A high speed serial interface allows direct connection to the serial ports of microcontrollers and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the part is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7892 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low-power CMOS logic. It is available in a 24-pin, 0.3" wide, plastic or hermetic DIP or in a 24-pin SOIC.

PRODUCT HIGHLIGHTS

1. The AD7892-3 features a conversion time of 1.3 μs and a track/hold acquisition time of 0.35 μs. This allows a throughput rate for the part up to 600 ksps. The AD7892-1 and AD7892-2 operate with throughput rates of 500 ksps.
2. The AD7892 operates from a single +5 V supply and consumes 60 mW typ making it ideal for low power and portable applications.
3. The part offers a high speed, flexible interface arrangement with parallel and serial interfaces for easy connection to microprocessors, microcontrollers and digital signal processors.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

DYNAMIC PERFORMANCE					f_{IN} = 100 kHz. f_{SAMPLE} = 500 ksps (AD7892-1 and AD7892-2) and 600 ksps (AD7892-3)
Signal to (Noise + Distortion) Ratio[3]	70	70	70	dB min	
Total Harmonic Distortion[3]	–80	–80	–80	dB max	
Peak Harmonic or Spurious Noise[3]	–81	–81	–81	dB max	
Intermodulation Distortion[3]					fa = 49 kHz, fb = 50 kHz
2nd Order Terms	–80	–80	–80	dB max	
3rd Order Terms	–80	–80	–80	dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	12	Bits	
Relative Accuracy[3]		±1	±1	LSB max	
Differential Nonlinearity[3]		±1	±1	LSB max	
Positive Full-Scale Error[3]	±4	±4	±4	LSB max	
AD7892-1 and AD7892-3					
Negative Full-Scale Error[3]	±4	±4	±4	LSB max	
Bipolar Zero Error[3]	±3	±2	±3	LSB max	
AD7892-2 Only					
Unipolar Offset Error[3]	±3	±2	±3	LSB max	
ANALOG INPUT					
AD7892-1					
Input Voltage Range	±10	±10	±10	Volts	Input Applied to V_{IN1} with V_{IN2} Grounded
Input Voltage Range	±5	±5	±5	Volts	Input Applied to V_{IN1} and V_{IN2}
Input Resistance	8	8	8	kΩ min	Input Applied to V_{IN1} with V_{IN2} Grounded
AD7892-2					
Input Voltage Range on V_{IN1}	0 to +2.5	0 to +2.5	0 to +2.5	Volts	Input Applied to V_{IN1} and Referenced to V_{IN2}
Input Current	50	50	50	nA max	
Input Voltage Range on V_{IN2}	±50	±50	±50	mV max	
AD7892-3					
Input Voltage Range on V_{IN1}	±2.5	±2.5	±2.5	Volts	Input Applied to V_{IN1} with V_{IN2} Unconnected
Input Resistance	2	2	2	kΩ min	
REFERENCE OUTPUT/INPUT					
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Impedance	1.6	1.6	1.6	kΩ min	Resistor Connected to Internal Reference Node
Input Capacitance[4]	10	10	10	pF max	
REF OUT Output Voltage	2.5	2.5	2.5	V nom	
REF OUT Error @ +25°C	±10	±10	±10	mV max	
T_{MIN} to T_{MAX}	±20	±20	±25	mV max	
REF OUT Temperature Coefficient	25	25	25	ppm/°C typ	
REF OUT Output Impedance	5.5	5.5	5.5	kΩ nom	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	±10	±10	±10	μA max	
Floating-State Capacitance[4]	15	15	15	pF max	
Output Coding					
AD7892-1 and AD7892-3	2s Complement				
AD7892-2	Straight (Natural) Binary				

Parameter	A Versions[1]	B Versions	S Version[2]	Units	Test Conditions/Comments
CONVERSION RATE					
Conversion Time	1.3	1.3		µs max	AD7892-3
Track/Hold Acquisition Time[3]	0.35	0.35		µs max	AD7892-3
Conversion Time	1.6	1.6	1.6	µs max	AD7892-1 and AD7892-2
Track/Hold Acquisition Time[3]	0.4	0.4	0.4	µs max	AD7892-1 and AD7892-2
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD}					
Normal Operation	18	18	18	mA max	
Standby Mode[5]	250	250	250	µA typ	
Power Dissipation					
Normal Operation	90	90	90	mW max	V_{DD} = +5 V. Typically 60 mW
Standby Mode[5]	1.25	1.25	1.25	mW typ	

NOTES
[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S Version: –55°C to +125°C.
[2]S Version available on AD7892-1 and AD7892-2.
[3]See Terminology.
[4]Sample tested @ +25°C to ensure compliance.
[5]This standby current is achieved with resistors to either DGND or V_{DD} on Pins 8, 9, 16 and 17. A conversion should not be initiated on the part within 30 µs of exiting standby mode.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A= +25°C unless otherwise noted)

V_{DD} to AGND ..... –0.3 V to +7 V
V_{DD} to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND
AD7892-1 ..... ±17 V
AD7892-2 ..... –0.3 V, V_{DD}
AD7892-3 ..... ±7 V
Reference Input Voltage to AGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Commercial (A, B Versions) ..... –40°C to +85°C
Extended (S Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 105°C/W
Lead Temperature (Soldering, 10 sec) ..... +260°C
Cerdip Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 70°C/W
Lead Temperature (Soldering, 10 sec) ..... +300°C
SOIC Package, Power Dissipation. ..... 450 mW
θ_{JA} Thermal Impedance ..... 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Input Range	Sample Rate	Relative Accuracy	Temperature Range	Package Option*
AD7892AN-1	±5 V or ±10 V	500 ksps		–40°C to +85°C	N-24
AD7892BN-1	±5 V or ±10 V	500 ksps	±1 LSB	–40°C to +85°C	N-24
AD7892AR-1	±5 V or ±10 V	500 ksps		–40°C to +85°C	R-24
AD7892BR-1	±5 V or ±10 V	500 ksps	±1 LSB	–40°C to +85°C	R-24
AD7892SQ-1	±5 V or ±10 V	500 ksps	±1 LSB	–55°C to +125°C	Q-24
AD7892AN-2	0 V to +2.5 V	500 ksps		–40°C to +85°C	N-24
AD7892BN-2	0 V to +2.5 V	500 ksps	±1 LSB	–40°C to +85°C	N-24
AD7892AR-2	0 V to +2.5 V	500 ksps		–40°C to +85°C	R-24
AD7892BR-2	0 V to +2.5 V	500 ksps	±1 LSB	–40°C to +85°C	R-24
AD7892SQ-2	0 V to +2.5 V	500 ksps	±1 LSB	–55°C to +125°C	Q-24
AD7892AN-3	±2.5 V	600 ksps		–40°C to +85°C	N-24
AD7892BN-3	±2.5 V	600 ksps	±1 LSB	–40°C to +85°C	N-24
AD7892AR-3	±2.5 V	600 ksps		–40°C to +85°C	R-24
AD7892BR-3	±2.5 V	600 ksps	±1 LSB	–40°C to +85°C	R-24

*N = Plastic DIP; R = SOIC; Q = Cerdip. For outline information see Package Information section.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, AGND = DGND = 0 V, REF IN = +2.5 V)

Parameter	A, B Versions	S Version	Units	Test Conditions/Comments
t_{CONV}	1.3		µs max	Conversion Time for AD7892-3
	1.6	1.6	µs max	Conversion Time for AD7892-1, AD7892-2
t_{ACQ}	350		ns min	Acquisition Time for AD7892-3
	400	400	ns min	Acquisition Time for AD7892-1, AD7892-2
Parallel Interface				
t_1	35	45	ns min	$\overline{CONVST}$ Pulse Width
t_2	60	60	ns min	$\overline{EOC}$ Pulse Width
t_3	0	0	ns min	$\overline{EOC}$ Falling Edge to $\overline{CS}$ Falling Edge Setup Time
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_5	35	45	ns min	Read Pulse Width
t_6[3]	35	40	ns max	Data Access Time After Falling Edge of $\overline{RD}$
t_7[4]	5	5	ns min	Bus Relinquish Time After Rising Edge of $\overline{RD}$
	30	40	ns max	
t_8	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_9[5]	100	100	ns min	$\overline{RD}$ to $\overline{CONVST}$ Setup Time
Serial Interface				
t_{10}	30	35	ns min	$\overline{RFS}$ Low to SCLK Falling Edge Setup Time
t_{11}[3]	25	30	ns max	$\overline{RFS}$ Low to Data Valid Delay
t_{12}	25	25	ns min	SCLK High Pulse Width
t_{13}	25	25	ns min	SCLK Low Pulse Width
t_{14}[3]	5	5	ns min	SCLK Rising Edge to Data Valid Hold Time
t_{15}[3]	25	30	ns max	SCLK Rising Edge to Data Valid Delay
t_{16}	20	30	ns min	$\overline{RFS}$ to SCLK Falling Edge Hold Time
t_{17}[4]	0	0	ns min	Bus Relinquish Time after Rising Edge of $\overline{RFS}$
	30	30	ns max	
t_{17A}[4]	0	0	ns min	Bus Relinquish Time after Rising Edge of SCLK
	30	30	ns max	

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are measured with tr = tf = 1 ns (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.

[2]See Figures 2 and 3.

[3]Measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[4]These times are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

[5]Assumes CMOS loads on data bits. With TTL loads, more current is drawn from the data lines and the $\overline{RD}$ to $\overline{CONVST}$ time needs to be extended to 300 ns min.

Specifications subject to change without notice.

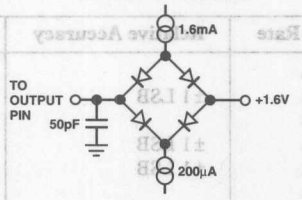


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7892 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

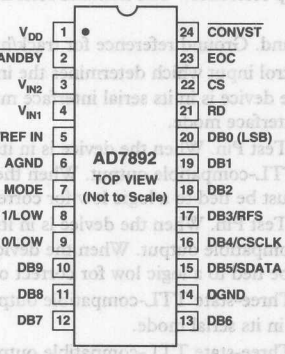
PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1	V_{DD}	Positive supply voltage, +5 V ± 5%.
2	STANDBY	Standby Input. Logic Input. With this input at a logic high, the part is in its normal operating mode; with this input at a logic low, the part is placed in its standby or power-down mode, which reduces power consumption to 5 mW typical.
3	V_{IN2}	Analog Input 2. For the AD7892-1, this input either connects to AGND or to V_{IN1} to determine the analog input voltage range. With V_{IN2} connected to AGND on the AD7892-1, the analog input range at the V_{IN1} input is ±10 V. With V_{IN2} connected to V_{IN1} on the AD7892-1, the analog input range to the part is ±5 V. For the AD7892-2, the voltage range at the V_{IN1} input is referenced to the voltage applied to the V_{IN2} input. The allowable span for the V_{IN2} voltage is ±50 mV. With V_{IN2} at AGND on the AD7892-2, the analog input voltage range at the V_{IN1} input is 0 to +2.5 V. For the AD7892-3, this input should be connected to AGND.
4	V_{IN1}	Analog Input 1. The analog input voltage to be converted by the AD7892 is applied to this input. For the AD7892-1, the input voltage range is either ±5 V or ±10 V depending on where the V_{IN2} input is connected. For the AD7892-2, the voltage range on the V_{IN1} input is 0 V to +2.5 V with respect to the voltage appearing at the V_{IN2} input. For the AD7892-3, the voltage range on the V_{IN1} input is ±2.5 V.
5	REF OUT/REF IN	Voltage Reference Output/Input. The part can be used with either its own internal reference or with an external reference source. The on-chip +2.5 V reference is provided at this pin. When using this internal reference as the reference source for the part, REF OUT should be decoupled to AGND with a 0.1 µF disc ceramic capacitor. The output impedance of this reference source is typically 5.5 kΩ. When using an external reference source as the reference voltage for the part, the reference source should be connected to this pin. This overdrives the internal reference and provides the reference source for the part. The REF IN input is buffered on-chip but must be able to sink or source current through the resistor to the output of the on-chip reference. The nominal reference voltage for correct operation of the AD7892 is +2.5 V.
6	AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
7	MODE	Mode. Control input which determines the interface mode for the AD7892. With this pin at a logic low, the device is in its serial interface mode; with this pin at a logic high, the device is in its parallel interface mode.
8	DB11/LOW	Data Bit 11/Test Pin. When the device is in its parallel mode, this pin is Data Bit 11 (MSB), a three-state TTL-compatible output. When the device is in its serial mode, this is used as a test pin which must be tied to a logic low for correct operation of the AD7892
9	DB10/LOW	Data Bit 10/Test Pin. When the device is in its parallel mode, this pin is Data Bit 10, a three-state TTL-compatible output. When the device is in its serial mode, this is used as a test pin which must be tied to a logic low for correct operation of the AD7892.
10	DB9	Data Bit 9. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
11	DB8	Data Bit 8. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
12	DB7	Data Bit 7. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
13	DB6	Data Bit 6. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
14	DGND	Digital Ground. Ground reference for digital circuitry.
15	DB5/SDATA	Data Bit 5/Serial Data. When the device is in its parallel mode, this pin is Data Bit 5, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the serial data output line. Sixteen bits of serial data are provided with four leading zeros preceding the 12-bits of valid data. Serial data is valid on the falling edge of SCLK for sixteen edges after $\overline{RFS}$ goes low. Output coding is 2s complement for AD7892-1 and AD7892-3 and straight (natural) binary for AD7892-2.

Pin No.	Mnemonic	Description
16	DB4/SCLK	Data Bit 4/Serial Clock. When the device is in its parallel mode, this pin is Data Bit 4, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the serial clock pin, SCLK. SCLK is an input and an external serial clock must be provided at this pin to obtain serial data from the AD7892. Serial data is clocked out from the output shift register on the rising edges of SCLK after $\overline{RFS}$ goes low.
17	DB3/$\overline{RFS}$	Data Bit 3/Receive Frame Synchronization. When the device is in its parallel mode, this pin is Data Bit 3, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the receive frame synchronization input with $\overline{RFS}$ provided externally to obtain serial data from the AD7892.
18	DB2	Data Bit 2. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
19	DB1	Data Bit 1. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
20	DB0	Data Bit 0 (LSB). Three-state TTL-compatible output. Output coding is 2s complement for AD7892-1 and AD7892-3 and straight (natural) binary for AD7892-2. This output should be left unconnected when the device is in its serial mode.
21	$\overline{RD}$	Read. Active low logic input which is used in conjunction with $\overline{CS}$ low to enable the data outputs.
22	$\overline{CS}$	Chip Select. Active low logic input which is used in conjunction with $\overline{RD}$ to enable he data outputs.
23	$\overline{EOC}$	End-of-Conversion. Active low logic output indicating converter status. The end of conversion is signified by a low-going pulse on this line. The duration of this $\overline{EOC}$ pulse is nominally 100 ns.
24	$\overline{CONVST}$	Convert Start. Logic Input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion.

PIN CONFIGURATION

DIP and SOIC



CIRCUIT DESCRIPTION

The AD7892 is a fast, 12-bit single supply A/D converter. It provides the user with signal scaling, track/hold, reference, A/D converter and versatile interface logic functions on a single chip. The signal scaling on the AD7892-1 allows the part to handle either ±5 V or ±10 V input signals while operating from a single +5 V supply. The AD7892-2 handles a 0 to +2.5 V analog input range, while signal scaling on the AD7892-3 allows it to handle ±2.5 V input signals when operating from a single supply. The part requires a +2.5 V reference which can be provided from the part's own internal reference or from an external reference source.

Conversion is initiated on the AD7892 by pulsing the $\overline{\text{CONVST}}$ input. On the rising edge of $\overline{\text{CONVST}}$, the track/hold goes from track mode to hold mode and the conversion sequence is started. At the end of conversion (falling edge of $\overline{\text{EOC}}$), the track/hold returns to tracking mode and the acquisition time begins. Conversion time for the part is 1.3 µs (AD7892-3) and the track/hold acquisition time is 350 ns (AD7892-3). This allows the AD7892-3 to operate at throughput rates up to 600 ksps. The AD7892-1 and AD7892-2 are specified with a 1.6 µs conversion and 400 ns acquisition time allowing a throughput rate of 500 ksps.

Track/Hold Section

The track/hold amplifier on the AD7892 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the track/hold is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate of 600 kHz (i.e., the track/hold can handle input frequencies in excess of 300 kHz).

The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 350 ns. The operation of the track/hold is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode on the rising edge of $\overline{\text{CONVST}}$. The aperture time for the track/hold (i.e., the delay time between the external $\overline{\text{CONVST}}$ signal and the track/hold actually going into hold) is typically 15 ns. At the end of conversion, the part returns to its tracking mode. The acquisition time of the track/hold amplifier begins at this point.

Reference Section

The AD7892 contains a single reference pin, labelled REF OUT/REF IN, which either provides access to the part's own +2.5 V reference or to which an external +2.5 V reference can be connected to provide the reference source for the part. The part is specified with a +2.5 V reference voltage. Errors in the reference source will result in gain errors in the AD7892's transfer function and will add to the specified full-scale errors on the part. On the AD7892-1 and AD7892-3, it will also result in an offset error injected in the attenuator stage.

The AD7892 contains an on-chip +2.5 V reference. To use this reference as the reference source for the AD7892, simply connect a 0.1 µF disc ceramic capacitor from the REF OUT/REF IN pin to AGND. The voltage that appears at this pin is internally buffered before being applied to the ADC. If this reference is required for use external to the AD7892, it should be buffered as the part has a FET switch in series with the reference output resulting in a source impedance for this output of 5.5 kΩ nominal. The tolerance on the internal reference is ±10 mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error over temperature of ±25 mV.

If the application requires a reference with a tighter tolerance or the AD7892 needs to be used with a system reference, then the user has the option of connecting an external reference to this REF OUT/REF IN pin. The external reference will effectively overdrive the internal reference and thus provide the reference source for the ADC. The reference input is buffered before being applied to the ADC with the maximum input current is ±100 µA. Suitable reference sources for the AD7892 include the AD680, AD780 and REF43 precision +2.5 V references.

INTERFACING

The part provides two interface options, a 12-bit parallel interface and a three-wire serial interface. The required interface mode is selected via the MODE pin. The two interface modes are discussed in the following sections.

Parallel Interface Mode

The parallel interface mode is selected by tying the MODE input to a logic high. Figure 2 shows a timing diagram illustrating the operational sequence of the AD7892. The on-chip track/hold goes into hold mode, and conversion is initiated on the rising edge of the $\overline{\text{CONVST}}$ signal. When conversion is complete, the end of conversion line ($\overline{\text{EOC}}$) pulses low to indicate that new data is available in the AD7892's output register. This $\overline{\text{EOC}}$ line can be used to drive an edge-triggered interrupt of a microprocessor. The read operation should be completed 200 ns prior to the next rising edge of $\overline{\text{CONVST}}$. $\overline{\text{CS}}$ and $\overline{\text{RD}}$

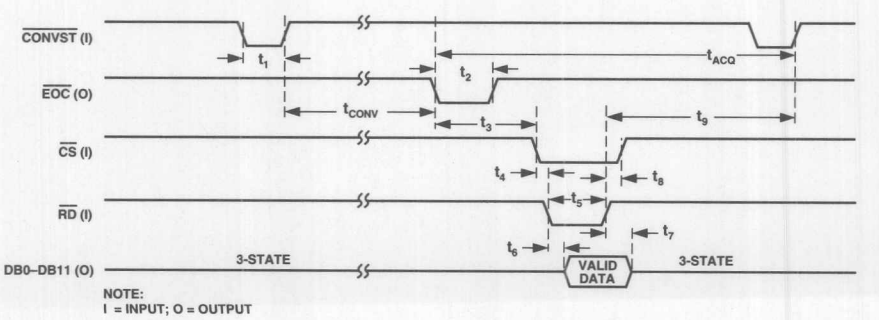


Figure 2. Parallel Mode Timing Diagram

going low accesses the 12-bit conversion result. In systems where the part is interfaced to a gate array or ASIC, this $\overline{EOC}$ pulse can be applied to the $\overline{CS}$ and $\overline{RD}$ inputs to latch data out of the AD7892 and into the gate array or ASIC. This eliminates the logic required in the gate array or ASIC to recognize the end of conversion and generate the read signal for the AD7892. To obtain optimum performance from the AD7892, it is not recommended to tie $\overline{CS}$ and $\overline{RD}$ permanently low as this keeps the three-state active during conversion.

Serial Interface Mode

The AD7892 is configured for serial mode interfacing by tying the MODE input low. It provides for a three-wire, serial link between the AD7892 and industry-standard microprocessors, microcontrollers and digital signal processors. SCLK and $\overline{RFS}$ of the AD7892 are inputs, and the AD7892's serial interface is designed for direct interface to systems that provide a serial clock input that is synchronized to the serial data output including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

Figure 3 shows the timing diagram for reading from the AD7892 in the serial interface mode. $\overline{RFS}$ goes low to access data from the AD7892. The serial clock input does not have to be continuous. The serial data can be accessed in a number of bytes. However, $\overline{RFS}$ must remain low for the duration of the data transfer operation. Sixteen bits of data are transmitted with four leading zeros followed by the 12-bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK. Old data is guaranteed to be valid for 5 ns after this edge. This is useful for high speed serial clocks where the access time of the part would not allow sufficient set-up time for the data to be accepted on the falling edge of the clock. In this case, care must be taken that $\overline{RFS}$ does not go just prior to a rising edge of SCLK. For slower serial clocks data is valid on the falling edge of SCLK. At the end of the read operation, the SDATA line is three-stated by a rising edge on either the SCLK of $\overline{RFS}$ inputs, whichever occurs first. Serial data cannot be read during conversion to avoid feedthrough problems from the serial clock to the conversion process. For optimum performance, a serial read should also be avoided within 400 ns of the rising edge of $\overline{CONVST}$ to avoid feedthrough into the track/hold during its acquisition time. The serial read should, therefore, occur between the end of conversion ($\overline{EOC}$ falling edge) and 400 ns prior to the next rising edge of $\overline{CONVST}$. This limits the maximum achievable throughput rate in serial mode (assuming 20 MHz serial clock) to 400 ksps for the AD7892-3 and 357 ksps for the AD7892-1 and AD7892-2.

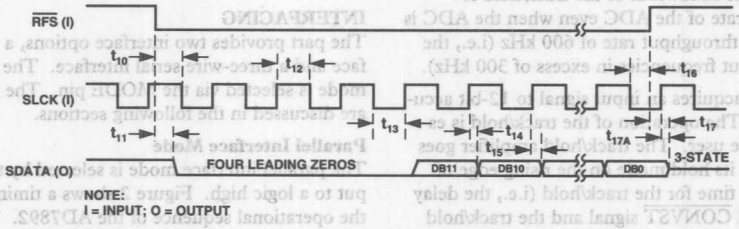


Figure 3. Serial Mode Timing Diagram

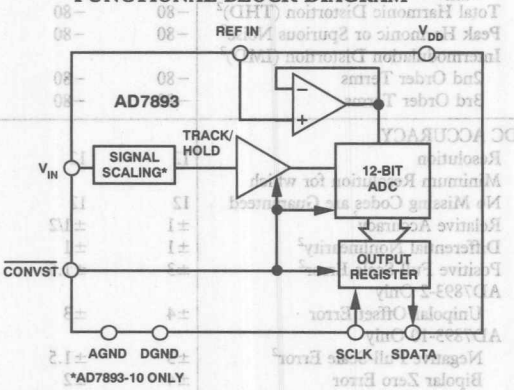
LC²MOS 12-Bit, Serial 6 µs ADC in 8-Pin Package

AD7893

FEATURES

- **Fast 12-Bit ADC with 6 µs Conversion Time**
- **8-Pin Mini-DIP and SOIC**
- **Single Supply Operation**
- **High Speed, Easy-to-Use, Serial Interface**
- **On-Chip Track/Hold Amplifier**
- **Selection of Input Ranges**
  - **±10 V for AD7893-10**
  - **0 V to +2.5 V for AD7893-2**
- **Low Power: 25 mW typ**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7893 is a fast, 12-bit ADC which operates from a single +5 V supply and is housed in a small 8-pin mini-DIP and 8-pin SOIC. The part contains a 6 µs successive approximation A/D converter, an on-chip track/hold amplifier, an on-chip clock and a high speed serial interface.

Output data from the AD7893 is provided via a high speed, serial interface port. This two-wire serial interface has a serial clock input and a serial data output with the external serial clock accessing the serial data from the part.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7893 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The part accepts an analog input range of ±10 V (AD7893-10) or 0 V to +2.5 V (AD7893-2) and operates from a single +5 V supply consuming only 25 mW typical.

The AD7893 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a small, 8-pin, 0.3″ wide, plastic or hermetic dual-in-line package (mini-DIP) and in an 8-pin, small-outline IC (SOIC).

PRODUCT HIGHLIGHTS

1. Fast, 12-Bit ADC in 8-Pin Package
   The AD7893 contains a 6 µs ADC, a track/hold amplifier, control logic and a high speed serial interface, all in an 8-pin package. This offers considerable space saving over alternative solutions.
2. Low Power, Single Supply Operation
   The AD7893 operates from a single +5 V supply and consumes only 25 mW. This low power, single supply operation makes it ideal for battery-powered or portable applications.
3. High Speed Serial Interface
   The part provides high speed serial data and serial clock lines allowing for an easy, two-wire serial interface arrangement.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7893—SPECIFICATIONS (V_{DD} = +5 V, AGND = DGND = 0 V, REF IN = +2.5 V. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	B Versions	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Signal to (Noise + Distortion) Ratio[2]					
@ +25°C	70	70	70	dB min	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 117 kHz
T_{MIN} to T_{MAX}		70		dB min	
Total Harmonic Distortion (THD)[2]	−80	−80	−80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 117 kHz
Peak Harmonic or Spurious Noise[2]	−80	−80	−80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 117 kHz
Intermodulation Distortion (IMD)[2]					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 117 kHz
2nd Order Terms	−80	−80	−80	dB max	
3rd Order Terms	−80	−80	−80	dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for which No Missing Codes are Guaranteed	12	12	12	Bits	
Relative Accuracy[2]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[2]	±1	±1	±1	LSB max	
Positive Full-Scale Error[2]	±3	±1.5	±3	LSB max	
AD7893-2 Only					
Unipolar Offset Error	±4	±3	±4	LSB max	
AD7893-10 Only					
Negative Full-Scale Error[2]	±3	±1.5	±3	LSB max	
Bipolar Zero Error	±4	±2	±4	LSB max	
ANALOG INPUT					
AD7893-10					
Input Voltage Range	±10	±10	±10	Volts	
Input Resistance	16	16	16	kΩ min	
AD7893-5					
Input Voltage Range	0 to +5	0 to +5	0 to +5	Volts	
Input Resistance	9	9	9	kΩ min	
AD7893-2					
Input Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Input Current	500	500	500	nA max	
REFERENCE INPUT					
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Current	2	2	10	μA max	
Input Capacitance[3]	10	10	10	pF max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
Output Coding					
AD7893-10	2s Complement				
AD7893-2	Straight (Natural) Binary				
CONVERSION RATE					
Conversion Time	6	6	6	μs max	
Track/Hold Acquisition Time[2]	1.5	1.5	1.5	μs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD}	9	9	9	mA max	
Power Dissipation	45	45	45	mW max	Typically 25 mW

NOTES
[1]Temperature Ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.
[2]See Terminology.
[3]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V, AGND = DGND = 0 V, REF IN = +2.5 V)

Parameter	A, B Versions	S Version	Units	Test Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	60	70	ns min	SCLK High Pulse Width
t_3	30	40	ns min	SCLK Low Pulse Width
t_4[3]	50	60	ns max	SCLK Rising Edge to Data Valid Delay
t_5[4]	10	10	ns min	Bus Relinquish Time after Falling Edge of SCLK
	100	100	ns max	

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are measured with tr = tf = 1 ns (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.
[2]See Figure 5.
[3]Measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_5, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{DD} to DGND . . . . . −0.3 V to +7 V
Analog Input Voltage to AGND
  AD7893-10, AD7893-5 . . . . . ±17 V
  AD7893-2 . . . . . −5 V, +10 V
Reference Input Voltage to AGND . . −0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . −0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Commercial (A, B Versions) . . . . . −40°C to +85°C
  Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +150°C
Plastic DIP Package, Power Dissipation . . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . . 130°C/W
  Lead Temperature, (Soldering, 10 sec) . . . . . +260°C
Cerdip Package, Power Dissipation . . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . . 125°C/W
  Lead Temperature, (Soldering, 10 secs) . . . . . +300°C
SOIC Package, Power Dissipation . . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . . 170°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . +215°C
    Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

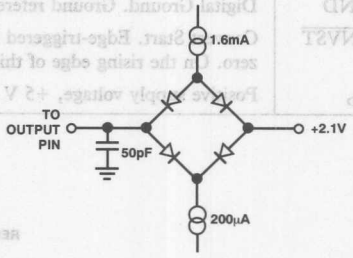


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

CAUTION

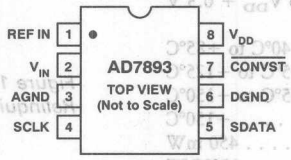
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7893 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Description
1	REF IN	Voltage Reference Input. An external reference source should be connected to this pin to provide the reference voltage for the AD7893's conversion process. The REF IN input is buffered on-chip. The nominal reference voltage for correct operation of the AD7893 is +2.5 V.
2	V_{IN}	Analog Input Channel. The analog input range is ±10 V (AD7893-10), 0 to +5 V (AD7893-5) and 0 to +2.5 V (AD7893-2).
3	AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
4	SCLK	Serial Clock Input. An external serial clock is applied to this input to obtain serial data from the AD7893. A new serial data bit is clocked out on the rising edge of this serial clock and data is valid on the falling edge. The serial clock input should be taken low at the end of the serial data transmission.
5	SDATA	Serial Data Output. Serial data from the AD7893 is provided at this output. The serial data is clocked out by the rising edge of SCLK and is valid on the falling edge of SCLK. Sixteen bits of serial data are provided with four leading zeros followed by the 12-bits of conversion data. On the sixteenth falling edge of SCLK, the SDATA line is disabled (three-stated). Output data coding is twos complement for the AD7893-10 and straight binary for the AD7893-2 and AD7893-5.
6	DGND	Digital Ground. Ground reference for digital circuitry.
7	$\overline{\text{CONVST}}$	Convert Start. Edge-triggered logic input. On the falling edge of this input, the serial clock counter is reset to zero. On the rising edge of this input, the track/hold goes into its hold mode and conversion is initiated.
8	V_{DD}	Positive supply voltage, +5 V ± 5%.

PIN CONFIGURATION

DIP and SOIC



ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)	SNR (dB)	Package Option*
AD7893AN-2	−40°C to +85°C	±1 LSB	70 dB	N-8
AD7893BN-2	−40°C to +85°C	±1/2 LSB	72 dB	N-8
AD7893AR-2	−40°C to +85°C	±1 LSB	70 dB	SO-8
AD7893BR-2	−40°C to +85°C	±1/2 LSB	72 dB	SO-8
AD7893SQ-2	−55°C to +125°C	±1 LSB	70 dB	Q-8
AD7893AN-5	−40°C to +85°C	±1 LSB	70 dB	N-8
AD7893BN-5	−40°C to +85°C	±1/2 LSB	72 dB	N-8
AD7893AR-5	−40°C to +85°C	±1 LSB	70 dB	SO-8
AD7893BR-5	−40°C to +85°C	±1/2 LSB	72 dB	SO-8
AD7893SQ-5	−55°C to +125°C	±1 LSB	70 dB	Q-8
AD7893AN-10	−40°C to +85°C	±1 LSB	70 dB	N-8
AD7893BN-10	−40°C to +85°C	±1/2 LSB	72 dB	N-8
AD7893AR-10	−40°C to +85°C	±1 LSB	70 dB	SO-8
AD7893BR-10	−40°C to +85°C	±1/2 LSB	72 dB	SO-8
AD7893SQ-10	−55°C to +125°C	±1 LSB	70 dB	Q-8

*N = Plastic DIP, Q = Cerdip, SO = SOIC. For outline information see Package Information section.

TERMINOLOGY

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7893, it is defined as:

$$THD(dB) = 20\ log\ \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither *m* or *n* are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), while the third order terms include (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb).

The AD7893 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Relative Accuracy
Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Positive Full-Scale Error (AD7893-10)
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal (4 × REF IN − 1 LSB) after the Bipolar Zero Error has been adjusted out.

Positive Full-Scale Error (AD7893-5)
This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111) from the ideal (2 × REF IN − 1 LSB) after the Unipolar Offset Error has been adjusted out.

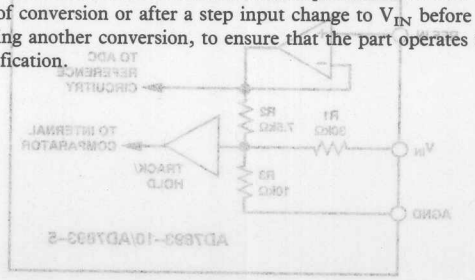
Positive Full-Scale Error (AD7893-2)
This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111) from the ideal (REF IN − 1 LSB) after the Unipolar Offset Error has been adjusted out.

Bipolar Zero Error (AD7893-10)
This is the deviation of the midscale transition (all 0s to all 1s) from the ideal 0 V (AGND).

Unipolar Offset Error (AD7893-2, AD7893-5)
This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal 1 LSB.

Negative Full-Scale Error (AD7893-10)
This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal (−4 × REF IN + 1 LSB) after Bipolar Zero Error has been adjusted out.

Track/Hold Acquisition Time
Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where there is a step input change on the input voltage applied to the V_{IN} input of the AD7893. This means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a step input change to V_{IN} before starting another conversion, to ensure that the part operates to specification.



CONVERTER DETAILS

The AD7893 is a fast, 12-bit single supply A/D converter. It provides the user with signal scaling (AD7893-10), track/hold, A/D converter and serial interface logic functions on a single chip. The A/D converter section of the AD7893 consists of a conventional successive-approximation converter based around an R-2R ladder structure. The signal scaling on the AD7893-10 and AD7893-5 allows the part to handle ±10 V and 0 to +5 V input signals respectively while operating from a single +5 V supply. The AD7893-2 accepts an analog input range of 0 V to +2.5 V. The part requires an external +2.5 V reference. The reference input to the part is buffered on-chip.

A major advantage of the AD7893 is that it provides all of the above functions in an 8-pin package, either 8-pin mini-DIP or SOIC. This offers the user considerable spacing saving advantages over alternative solutions. The AD7893 consumes only 25 mW typical making it ideal for battery-powered applications.

Conversion is initiated on the AD7893 by pulsing the $\overline{\text{CONVST}}$ input. On the rising edge of $\overline{\text{CONVST}}$, the on-chip track/hold goes from track to hold mode and the conversion sequence is started. The conversion clock for the part is generated internally using a laser-trimmed clock oscillator circuit. Conversion time for the AD7893 is 6 μs and the track/hold acquisition time is 1.5 μs. To obtain optimum performance from the part, the read operation should not occur during the conversion or during 600 ns prior to the next conversion. This allows the part to operate at throughput rates up to 117 kHz and achieve data sheet specifications. The part can operate at higher throughput rates (up to 133 kHz) with slightly degraded performance (see Timing and Control section).

CIRCUIT DESCRIPTION

Analog Input Section

The AD7893 is offered as three part types, the AD7893-10 which handles a ±10 V input voltage range, the AD7893-5 which handles a 0 to +5 V input range and the AD7893-2 which handles a 0 V to +2.5 V input voltage range.

Figure 2 shows the analog input section for the AD7893-10 and AD7893-5. The analog input range of the AD7893-10 is ±10 V into an input resistance of typically 33 kΩ. The input range on the AD7893-5 is 0 to +5 V into an input resistance of typically 11 kΩ. This input is benign with no dynamic charging currents as the resistor stage is followed by a high input impedance stage

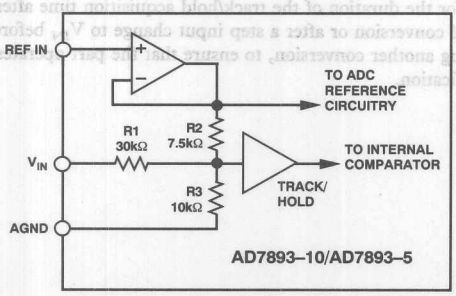


Figure 2. AD7893-10/AD7893-5 Analog Input Structure

of the track/hold amplifier. For the AD7893-10, R1 = 30 kΩ, R2 = 7.5 kΩ and R3 = 10 kΩ. For the AD7893-5, R1 and R3 = 5 kΩ while R2 is open-circuit.

For the AD7893-10, the designed code transitions occur on successive integer LSB values (i.e., 1 LSB, 2 LSBs, 3 LSBs ...). Output coding is 2s complement binary with 1 LSB = FS/4096 = 20 V/4096 = 4.88 mV. The ideal input/output transfer function for the AD7893-10 is shown in Table I.

Table I. Ideal Input/Output Code Table for the AD7893-10

Analog Input[1]	Digital Output Code Transition
+FSR/2 − 1 LSB[2] (9.995117)	011 . . . 110 to 011 . . . 111
+FSR/2 − 2 LSBs (9.990234)	011 . . . 101 to 011 . . . 110
+FSR/2 − 3 LSBs (9.985352)	011 . . . 100 to 011 . . . 101
AGND + 1 LSB (0.004883)	000 . . . 000 to 000 . . . 001
AGND (0.000000)	111 . . . 111 to 000 . . . 000
AGND − 1 LSB (−0.004883)	111 . . . 110 to 111 . . . 111
−FSR/2 + 3 LSBs (−9.985352)	100 . . . 010 to 100 . . . 011
−FSR/2 + 2 LSBs (−9.990234)	100 . . . 001 to 100 . . . 010
−FSR/2 + 1 LSB (−9.995117)	100 . . . 000 to 100 . . . 001

NOTES
[1]FSR is full-scale range and is 20 V with REF IN = +2.5 V.
[2]1 LSB = FSR/4096 = 4.883 mV with REF IN = +2.5 V.

For the AD7893-5, the designed code transitions again occur on successive integer LSB values. Output coding is straight (natural) binary with 1 LSB = FS/4096 = 5 V/4096 = 1.22 mV. The ideal input/output transfer function for the AD7893-5 is shown in Table II.

The analog input section for the AD7893-2 contains no biasing resistors and the V_{IN} pin drives the input to the track/hold amplifier directly. The analog input range is 0 V to +2.5 V into a high impedance stage with an input current of less than 500 nA. This input is benign with no dynamic charging currents. Once again, the designed code transitions occur on successive integer LSB values. Output coding is straight (natural) binary with 1 LSB = FS/4096 = 2.5 V/4096 = 0.61 mV. Table II also shows the ideal input/output transfer function for the AD7893-2.

Table II. Ideal Input/Output Code Table for AD7893-2/AD7893-5

Analog Input[1]	Digital Output Code Transition
+FSR − 1 LSB[2]	111 . . . 110 to 111 . . . 111
+FSR − 2 LSB	111 . . . 101 to 111 . . . 110
+FSR − 3 LSB	111 . . . 100 to 111 . . . 101
AGND + 3 LSB	000 . . . 010 to 000 . . . 011
AGND + 2 LSB	000 . . . 001 to 000 . . . 010
AGND + 1 LSB	000 . . . 000 to 000 . . . 001

NOTES
[1]FSR is Full Scale Range and is 5 V for AD7893-5 and 2.5 V for AD7893-2 with REF IN = +2.5 V.
[2]1 LSB = FSR/4096 and is 1.22 mV for AD7893-5 and 0.61 mV for AD7893-2 with REF IN = +2.5 V.

Track/Hold Section

The track/hold amplifier on the analog input of the AD7893 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the track/hold is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate of 117 kHz (i.e., the track/hold can handle input frequencies in excess of 58 kHz).

The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 1.5 μs. The operation of the track/hold is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion (i.e., the rising edge of $\overline{\text{CONVST}}$). The aperture time for the track/hold (i.e. the delay time between the external $\overline{\text{CONVST}}$ signal and the track/hold actually going into hold) is typically 15 ns. At the end of conversion (6 μs after the rising edge of $\overline{\text{CONVST}}$) the part returns to its tracking mode. The acquisition time of the track/hold amplifier begins at this point.

Reference Input

The reference input to the AD7893 is buffered on-chip with a maximum reference input current of 1 μA. The part is specified with a +2.5 V reference input voltage. Errors in the reference source will result in gain errors in the AD7893's transfer function and will add to the specified full-scale errors on the part. On the AD7893-10 it will also result in an offset error injected in the attenuator stage. Suitable reference sources for the AD7893 include the AD780 and AD680 precision +2.5 V references.

Timing and Control Section

Figure 4 shows the timing and control sequence required to obtain optimum performance from the AD7893. In the sequence shown, conversion is initiated on the rising edge of $\overline{\text{CONVST}}$ and new data from this conversion is available in the output register of the AD7893 6 μs later. Once the read operation has taken place, a further 600 ns should be allowed before the next rising edge of $\overline{\text{CONVST}}$ to optimize the settling of the track/hold amplifier before the next conversion is initiated. With the serial clock frequency at its maximum of 8.33 MHz, the achievable throughput rate for the part is 6 μs (conversion time) plus 1.92 μs (read time) plus 0.6 μs (acquisition time). This results in a minimum throughput time of 8.52 μs (equivalent to a throughput rate of 117 kHz).

The read operation consists of sixteen serial clock pulses to the output shift register of the AD7893. After sixteen serial clock pulses the shift register is reset and the SDATA line is three-stated. If there are more serial clock pulses after the sixteenth clock, the shift register will be moved on past its reset state. However, the shift register will be reset again on the falling edge of the $\overline{\text{CONVST}}$ signal to ensure that the part returns to a known state every conversion cycle. As a result, a read operation from the output register should not straddle across the falling edge of $\overline{\text{CONVST}}$ as the output shift register will be reset in the middle of the read operation and the data read back into the microprocessor will appear invalid.

The throughput rate of the part can be increased by reading data during conversion or during the acquisition time. If the data is read during conversion, a throughput time of 6 μs (conversion time) plus 1.5 μs is achieved. This minimum throughput time of 7.5 μs is achieved with a slight reduction in performance from the AD7893. The signal to (noise + distortion) number is likely to degrade by approximately 1.5 dB while the code flicker from the part will also increase (see AD7893 PERFORMANCE section).

Because the AD7893 is provided in an 8-pin package to minimize board space, the number of pins available for interfacing is very limited. As a result, no status signal is provided from the AD7893 to indicate when conversion is complete. In many applications this will not be a problem as the data can be read from the AD7893 during conversion or after conversion. However, applications which want to achieve optimum performance from the AD7893 will have to ensure that the data read does not occur during conversion or during 600 ns prior to the rising edge of $\overline{\text{CONVST}}$. This can be achieved in either of two ways. The first is to ensure in software that the read operation is not initiated until 6 μs after the rising edge of $\overline{\text{CONVST}}$. This will only be possible if the software knows when the $\overline{\text{CONVST}}$ command is issued. The second scheme would be to use the $\overline{\text{CONVST}}$ signal as both the conversion start signal and an interrupt signal. The simplest way to do this would be to generate a square wave signal for $\overline{\text{CONVST}}$ with high and low times of 6 μs (see Figure 4). Conversion is initiated on the rising edge of $\overline{\text{CONVST}}$. The falling edge of $\overline{\text{CONVST}}$ occurs 6 μs later and can be used as either an active low or falling edge-triggered interrupt signal to tell the processor to read the data from the

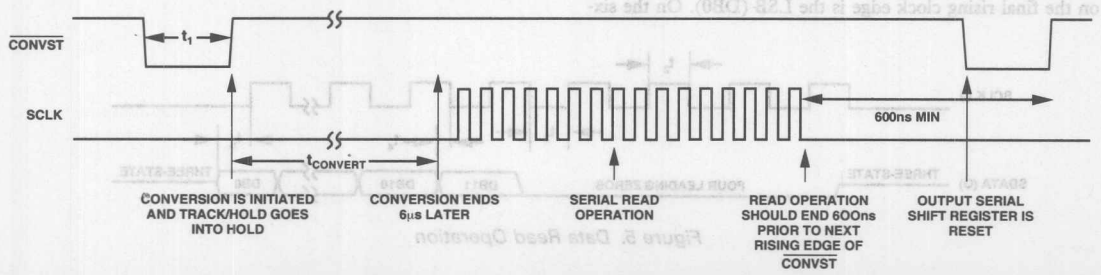


Figure 3. Timing Sequence for Optimum Performance from the AD7893

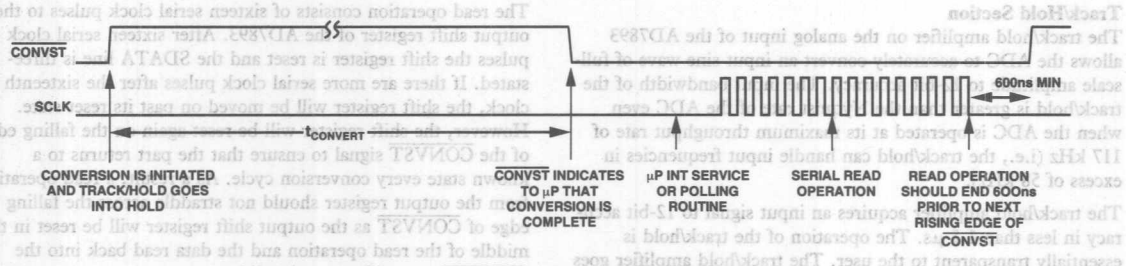


Figure 4. CONVST Used as Status Signal

AD7893. Provided the read operation is completed 600 ns before the rising edge of CONVST, the AD7893 will operate to specification.

This scheme limits the throughput rate to 12 µs minimum. However, depending upon the response time of the microprocessor to the interrupt signal and the time taken by the processor to read the data, this may the fastest which the system could have operated. In any case, the CONVST signal does not have to have a 50:50 duty cycle. This can be tailored to optimize the throughput rate of the part for a given system.

Alternatively, the CONVST signal can be used as a normal narrow pulse width. The rising edge of CONVST can be used as an active high or rising edge-triggered interrupt. A software delay of 6 µs can then be implemented before data is read from the part.

Serial Interface

The serial interface to the AD7893 consists of just two wires, a serial clock input (SCLK) and the serial data output (SDATA). This allows for an easy-to-use interface to most microcontrollers, DSP processors and shift registers.

Figure 5 shows the timing diagram for the read operation to the AD7893. The serial clock input (SCLK) provides the clock source for the serial interface. Serial data is clocked out from the SDATA line on the rising edge of this clock and is valid on the falling edge of SCLK. Sixteen clock pulses must be provided to the part to access to full conversion result. The AD7893 provides four leading zeros followed by the 12-bit conversion result starting with the MSB (DB11). The last data bit to be clocked out on the final rising clock edge is the LSB (DB0). On the sixteenth falling edge of SCLK, the SDATA line is disabled (three-stated). After this last bit has been clocked out, the SCLK input should return low and remain low until the next serial data read operation. If there are extra clock pulses after the sixteenth clock, the AD7893 will start over again with outputting data from its output register and the data bus will no longer be three-stated even when the clock stops. Provided the serial clock has stopped before the next falling edge of CONVST, the AD7893 will continue to operate correctly with the output shift register being reset on the falling edge of CONVST. However, the SCLK line must be low when CONVST goes low in order to reset the output shift register correctly.

The serial clock input does not have to be continuous during the serial read operation. The sixteen bits of data (four leading zeros and 12 bit conversion result) can be read from the AD7893 in a number of bytes. However, the SCLK input must remain low between the two bytes.

Normally, the output register is updated at the end of conversion. However, if a serial read from the output register is in progress when conversion is complete, the updating of the output register is deferred. In this case, the output register is updated when the serial read is completed. If the serial read has not been completed before the next falling edge of CONVST, then the output register will be updated on the falling edge of CONVST and the output shift register count is reset. In applications where the data read has been started and not completed before the falling edge of CONVST, the user must provide a CONVST pulse width of greater than 1.5 µs to ensure correct setup of the AD7893 before the next conversion is initiated. In

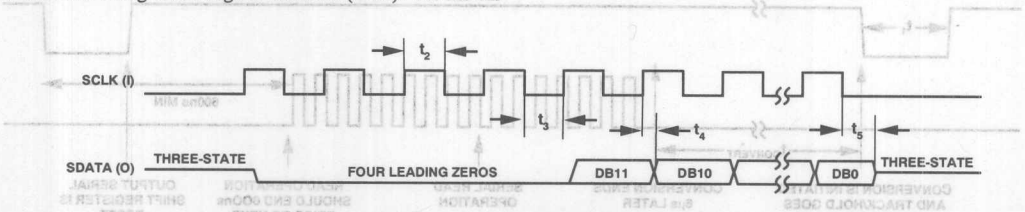


Figure 5. Data Read Operation

applications where the output update takes place either at the end of conversion or at the end of a serial read which is completed 1.5 μs before the rising edge of $\overline{\text{CONVST}}$, the normal pulse width of 50 ns minimum applies to $\overline{\text{CONVST}}$.

The AD7893 counts the serial clock edges to know which bit from the output register should be placed on the SDATA output. To ensure that the part does not lose synchronization, the serial clock counter is reset on the falling edge of the $\overline{\text{CONVST}}$ input provided the SCLK line is low. The user should ensure that a falling edge on the $\overline{\text{CONVST}}$ input does not occur, while a serial data read operation is in progress.

MICROPROCESSOR/MICROCONTROLLER INTERFACE

The AD7893 provides a two-wire serial interface which can be used for connection to the serial ports of DSP processors and microcontrollers. Figures 6 through 9 show the AD7893 interfaced to a number of different microcontrollers and DSP processors. The AD7893 accepts an external serial clock and as a result, in all interfaces shown here, the processor/controller is configured as the master, providing the serial clock, with the AD7893 configured as the slave in the system.

AD7893–8051 Interface

Figure 6 shows an interface between the AD7893 and the 8XC51 microcontroller. The 8XC51 is configured for its Mode 0 serial interface mode. The diagram shows the simplest form of the interface where the AD7893 is the only part connected to the serial port of the 8XC51 and, therefore, no decoding of the serial read operations is required. It also makes no provisions for monitoring when conversion is complete on the AD7893.

Either of these two tasks can readily be accomplished with minor modifications to the interface. To chip select the AD7893 in systems where more than one device is connected to the 8XC51's serial port, a port bit, configured as an output, from one of the 8XC51's parallel ports can be used to gate on or off the serial clock to the AD7893. A simple AND function on this port bit and the serial clock from the 8XC51 will provide this function. The port bit should be high to select the AD7893 and low when it is not selected.

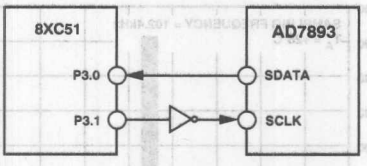


Figure 6. AD7893 to 8XC51 Interface

To monitor the conversion time on the AD7893 a scheme such as outlined previously with $\overline{\text{CONVST}}$ can be used. This can be implemented in two ways. One is to connect the $\overline{\text{CONVST}}$ line to another parallel port bit which is configured as an input. This port bit can then be polled to determine when conversion is complete. An alternative is to use an interrupt driven system in which case the $\overline{\text{CONVST}}$ line should be connected to the INT1 input of the 8XC51.

The serial clock rate from the 8XC51 is limited to significantly less than the allowable input serial clock frequency with which the AD7893 can operate. As a result, the time to read data from the part will actually be longer than the conversion time of the part. This means that the AD7893 cannot run at its maximum throughput rate when used with the 8XC51.

AD7893–68HC11 Interface

An interface circuit between the AD7893 and the 68HC11 microcontroller is shown in Figure 7. For the interface shown, the 68HC11 SPI port is used and the 68HC11 is configured in its single-chip mode. The 68HC11 is configured in the master mode with its CPOL bit set to a logic zero and its CPHA bit set to a logic one. As with the previous interface, the diagram shows the simplest form of the interface where the AD7893 is the only part connected to the serial port of the 68HC11 and, therefore, no decoding of the serial read operations is required. It also makes no provisions for monitoring when conversion is complete on the AD7893.

Once again, either of these two tasks can readily be accomplished with minor modifications to the interface. To chip select the AD7893 in systems where more than one device is connected to the 68HC11's serial port, a port bit, configured as an output, from one of the 68HC11's parallel ports can be used to gate on or off the serial clock to the AD7893. A simple AND function on this port bit and the serial clock from the 68HC11 will provide this function. The port bit should be high to select the AD7893 and low when it is not selected.

To monitor the conversion time on the AD7893 a scheme, such as outlined in the previous interface with $\overline{\text{CONVST}}$, can be used. This can be implemented in two ways. One is to connect the $\overline{\text{CONVST}}$ line to another parallel port bit which is configured as an input. This port bit can then be polled to determine when conversion is complete. An alternative is to use an interrupt driven system in which case the $\overline{\text{CONVST}}$ line should be connected to the $\overline{\text{IRQ}}$ input of the 68HC11.

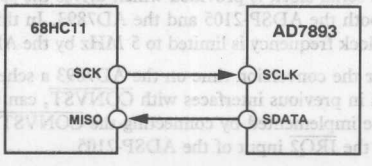


Figure 7. AD7893 to 68HC11 Interface

The serial clock rate from the 68HC11 is limited to significantly less than the allowable input serial clock frequency with which the AD7893 can operate. As a result, the time to read data from the part will actually be longer than the conversion time of the part. This means that the AD7893 cannot run at its maximum throughput rate when used with the 68HC11.

AD7893–ADSP-2105 Interface

An interface circuit between the AD7893 and the ADSP-2105 DSP processor is shown in Figure 8. In the interface shown, the RFS1 output from the ADSP-2105's SPORT1 serial port is used to gate the serial clock (SCLK1) of the ADSP-2105 before it is applied to the SCLK input of the AD7893. The RFS1 output is configured for active high operation. The interface ensures a noncontinuous clock for the AD7893's serial clock input, with only sixteen serial clock pulses provided and the serial clock line of the AD7893 remaining low between data transfers. The SDATA line from the AD7893 is connected to the DR1 line of the ADSP-2105's serial port.

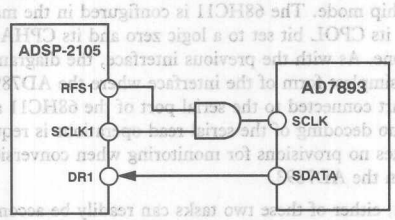


Figure 8. AD7893 to ADSP-2105 Interface

The timing relationship between the SCLK1 and RFS1 outputs of the ADSP-2105 are such that the delay between the rising edge of the SCLK1 and the rising edge of an active high RFS1 is up to 25 ns. There is also a requirement that data must be setup 10 ns prior to the falling edge of the SCLK1 to be read correctly by the ADSP-2105. The data access time for the AD7893 is 50 ns from the rising edge of its SCLK input. Assuming a 10 ns propagation delay through the external AND gate, the high time of the SCLK1 output of the ADSP-2105 must be $\geq (50 + 25 + 10 + 10)$ ns, i.e., ≥ 95 ns. This means that the serial clock frequency with which the interface of Figure 13 can work with is limited to 5.26 MHz.

An alternative scheme is to configure the ADSP-2105 such that it accepts an external serial clock. In this case, an external noncontinuous serial clock is provided which drives the serial clock inputs of both the ADSP-2105 and the AD7893. In this scheme, the serial clock frequency is limited to 5 MHz by the ADSP-2105.

To monitor the conversion time on the AD7893 a scheme, such as outlined in previous interfaces with $\overline{\text{CONVST}}$, can be used. This can be implemented by connecting the $\overline{\text{CONVST}}$ line directly to the $\overline{\text{IRQ2}}$ input of the ADSP-2105.

AD7893–DSP56000 Interface

Figure 9 shows an interface circuit between the AD7893 and the DSP56000 DSP processor. The DSP5600 is configured for normal mode asynchronous operation with gated clock. It is also set up for a 16-bit word with the gated serial clock being generated by the DSP56000 and appears on the SC0 pin. The SC0 pin should be configured as an output by setting bit SCD0 to 1. In this mode, the DSP56000 provides sixteen serial clock pulses to the AD7893 in a serial read operation. The DSP56000 assumes valid data on the first falling edge of SCK so the interface is simply two-wire as shown in Figure 9.

To monitor the conversion time on the AD7893 a scheme, such as outlined in previous interface examples with $\overline{\text{CONVST}}$, can be used. This can be implemented by connecting the $\overline{\text{CONVST}}$ line directly to the $\overline{\text{IRQA}}$ input of the DSP56000.

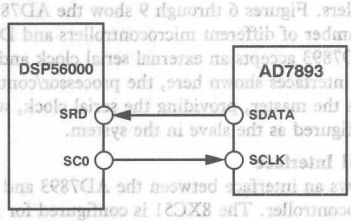


Figure 9. AD7893 to DSP56000 Interface

AD7893 PERFORMANCE

Figure 10 shows a histogram plot for 8192 conversions of a dc input using the AD7893. The analog input was set at the center of a code transition. The timing and control sequence used was as per Figure 3 where the optimum performance of the ADC was achieved. It can be seen that almost all the codes appear in the one output bin indicating very good noise performance from the ADC. The rms noise performance for the AD7893-2 for the above plot was 87 μV. Since the analog input range, and hence LSB size, on the AD7893-10 is eight times what it is for the AD7893-2, the same output code distribution results in an output rms noise of 700 μV for the AD7893-10.

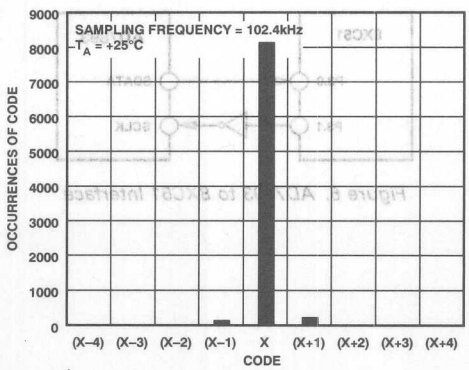


Figure 10. Histogram of 8192 Conversions of a DC Input

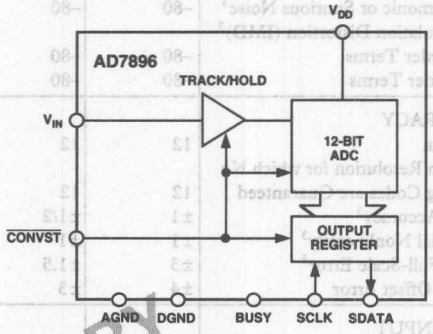
3 V, LC²MOS 12-Bit, Serial 8 µs ADC in 8-Pin Package

AD7896*

FEATURES

- Fast 12-Bit ADC with 8 µs Conversion Time
- 8-Pin Mini-DIP and SOIC
- Single 3 V Supply Operation
- High Speed, Easy-to-Use, Serial Interface
- On-Chip Track/Hold Amplifier
- Analog Input Range is 0 V to V_{DD}
- High Input Impedance
- Low Power: 10 mW typ

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7896 is a fast, 12-bit ADC which operates from a single +3 V supply and is housed in a small 8-pin mini-DIP and 8-pin SOIC. The part contains an 8 µs successive approximation A/D converter, an on-chip track/hold amplifier, an on-chip clock and a high speed serial interface.

Output data from the AD7896 is provided via a high speed, serial interface port. This two-wire serial interface has a serial clock input and a serial data output with the external serial clock accessing the serial data from the part.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7896 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The part accepts an analog input range of 0 V to V_{DD} and operates from a single +3 V supply consuming only 10 mW typical. The V_{DD} input is also used as the reference for the part so that no external reference is required.

The AD7896 features a high sampling rate mode and, for low power applications, a proprietary automatic power down mode where the part automatically goes into power down once conversion is complete and "wakes up" before the next conversion cycle.

The AD7896 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a small, 8-pin, 0.3" wide, plastic or hermetic dual-in-line package (mini-DIP) and in an 8-pin, small outline IC (SOIC).

PRODUCT HIGHLIGHTS

1. Complete, 12-bit ADC in 8-Pin Package
   The AD7896 contains an 8 µs ADC, a track/hold amplifier, control logic and a high speed serial interface, all in an 8-pin DIP. The V_{DD} input is used as the reference for the part so no external reference is needed. This offers considerable space saving over alternative solutions.
2. Low Power, Single Supply Operation
   The AD7896 operates from a single +3 V supply and consumes only 10 mW typical. The automatic power down mode, where the part goes into power down once conversion is complete and "wakes up" before the next conversion cycle, makes the AD7896 ideal for battery powered or portable applications.
3. High Speed Serial Interface
   The part provides high speed serial data and serial clock lines allowing for an easy, two-wire serial interface arrangement.

*Patent pending.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7896–SPECIFICATIONS

(V_{DD} = +3.0 V to +3.6 V, AGND = DGND = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	A Versions[1]	B Versions	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE [2]					
Signal to (Noise + Distortion) Ratio[3]					
@ +25°C	70	70	70	dB min	f_{IN} =10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{MIN} to T_{MAX}		70		dB min	
Total Harmonic Distortion (THD)[3]	–80	–80	–80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
Peak Harmonic or Spurious Noise[3]	–80	–80	–80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
Intermodulation Distortion (IMD)[3]					fa = 9 Hz, fb = 9.5 kHz, f_{SAMPLE} = 100 kHz
2nd Order Terms	–80	–80	–80	dB max	
3rd Order Terms	–80	–80	–80	dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for which No Missing Codes are Guaranteed	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[3]	±1	±1	±1	LSB max	
Positive Full-Scale Error[3]	±3	±1.5	±3	LSB max	
Unipolar Offset Error	±4	±3	±4	LSB max	
ANALOG INPUT					
Input Voltage Range	0 V to +V_{DD}	0 V to +V_{DD}	0 V to +V_{DD}	Volts	
Input Current	50	50	50	µA max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.0	2.0	2.0	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 3.0 V to 3.6 V
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	2.4	2.4	2.4	V min	I_{SOURCE} = 2 mA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 2 mA
Output Coding	Straight (Natural) Binary				
CONVERSION RATE					
Conversion Time:					
Mode 1 Operation	8	8	8	µs max	
Mode 2 Operation[5]	13	13	13	µs max	
Track/Hold Acquisition Time[3]	1.5	1.5	1.5	µs max	
POWER REQUIREMENTS					
V_{DD}	+3.0/+3.6	+3.0/+3.6	+3.0/+3.6	V min/max	
I_{DD}	4.5	4.5	4.5	mA max	
Power Dissipation	15	15	15	mW max	V_{DD} = 3.3 V, Typically 10 mW
Power-Down Mode					
I_{DD}	10	10	10	µA max	
Power Dissipation	36	36	36	µW max	

NOTES

[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S Version: –55°C to +125°C.

[2]Applies to Mode 1 operation. See section on operating modes.

[3]See Terminology.

[4]Sample tested @ +25°C to ensure compliance.

[5]This 13 µs includes the "wake-up" time from standby. This "wake-up" time is timed from the rising edge of $\overline{\text{CONVST}}$, whereas conversion is timed from the falling edge of $\overline{\text{CONVST}}$, for narrow $\overline{\text{CONVST}}$ pulse width the conversion time is effectively the "wake-up" time plus conversion time hence 13 µs. This can be seen from Figure 3. Note that if the $\overline{\text{CONVST}}$ pulse width is greater than 5 µs then the effective conversion time will increase beyond 13 µs.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

TIMING CHARACTERISTICS[1] (V_{DD} = +3.0 V to +3.6 V, AGND = DGND = 0 V)

Parameter	A, B Versions	S Version	Units	Test Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	50	50	ns min	SCLK High Pulse Width
t_3	50	50	ns min	SCLK Low Pulse Width
t_4	80[2]	80[2]	ns max	Data Access Time After Falling Edge of SCLK
t_5	15	15	ns min	Data Hold Time After Falling Edge of SCLK
t_6	100[3]	100[3]	ns max	Bus Relinquish Time After Falling Edge of SCLK

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are measured with tr = tf = 1 ns (10% to 90% of +3.3 V) and timed from a voltage level of +1.6 V.
[2]Measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.0 V.
[3]Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_6, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND ..... –0.3 V to +7 V
V_{DD} to DGND. ..... –0.3 V to +7 V
Analog Input Voltage to AGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Commercial (A, B Versions) ..... –40°C to +85°C
  Extended (S Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 125°C/W
  θ_{JC} Thermal Impedance. ..... 50°C/W
  Lead Temperature (Soldering, 10 sec) ..... +260°C
SOIC Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 160°C/W
  θ_{JC} Thermal Impedance ..... 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

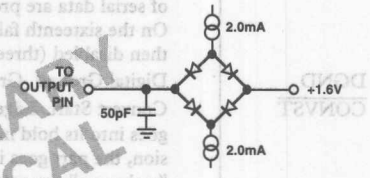


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

PRELIMINARY TECHNICAL DATA

CAUTION

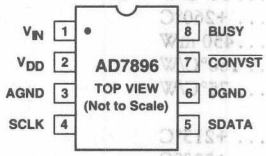
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7896 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Description
1	V_{IN}	Analog Input. The analog input range is 0 V to V_{DD}.
2	V_{DD}	Positive supply voltage, +3.0 V to 3.6 V.
3	AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
4	SCLK	Serial Clock Input. An external serial clock is applied to this input to obtain serial data from the AD7896. A new serial data bit is clocked out on the falling edge of this serial clock. Data is guaranteed valid for 15 ns after this falling edge so the µP can accept data on the either the falling edge or the rising edge. The serial clock input should be taken low at the end of the serial data transmission.
5	SDATA	Serial Data Output. Serial data from the AD7896 is provided at this output. The serial data is clocked out by the falling edge of SCLK, but the data can also be read on the falling edge of the SCLK. This is possible because data bit N is valid for a specified time after the falling edge of the SCLK (data hold time) and can be read before data bit N+1 becomes valid a specified time after the falling edge of SCLK (data access time) (see Figure 4). Sixteen bits of serial data are provided with four leading zeros followed by the 12-bits of conversion data. On the sixteenth falling edge of SCLK, the SDATA line is held for the data hold time and then disabled (three-stated). Output data coding is straight binary.
6	DGND	Digital Ground. Ground reference for digital circuitry.
7	$\overline{\text{CONVST}}$	Convert Start. Edge-triggered logic input. On the falling edge of this input, the track/hold goes into its hold mode and conversion is initiated. If $\overline{\text{CONVST}}$ is low at the end of conversion, the part goes into power down mode. In this case, the rising edge of $\overline{\text{CONVST}}$ "wakes up" the part.
8	BUSY	The BUSY pin is used to indicate when the part is doing a conversion. The BUSY pin will go high on the falling edge of $\overline{\text{CONVST}}$ and will return low when the conversion is complete.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)	SNR (dB)	Package Option*
AD7896AN	–40°C to +85°C	±1 LSB	70 dB	N-8
AD7896BN	–40°C to +85°C	±1/2 LSB	72 dB	N-8
AD7896AQ	–40°C to +85°C	±1 LSB	70 dB	Q-8
AD7896BQ	–40°C to +85°C	±1/2 LSB	72 dB	Q-8
AD7896AR	–40°C to +85°C	±1 LSB	70 dB	R-8
AD7896BR	–40°C to +85°C	±1/2 LSB	72 dB	R-8
AD7896SQ	–55°C to +125°C	±1 LSB	70 dB	Q-8

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

TERMINOLOGY

Relative Accuracy
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (*which is V_{IN} = AGND + 1/2 LSB*) a point 1/2 LSB below the first code transition (00 . . . 000 to 00 . . . 001) and full scale (*which is V_{IN} = AGND + V_{DD} – 1/2 LSB*), a point 1/2 LSB above the last code transition (11 . . . 110 to 11 . . . 111).

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Unipolar Offset Error
This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal V_{IN} voltage (AGND + 1 LSB).

Positive Full-Scale Error
This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111 from the ideal (V_{IN} = AGND + V_{DD} – 1 LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time
Track/hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (*the point at which the track/hold returns into track mode*). It also applies to a situation where there is a step input change on the input voltage applied to the selected V_{IN} input of the AD7896. It means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a step input change to V_{IN} before starting another conversion, to ensure the part operates to specification.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7896, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

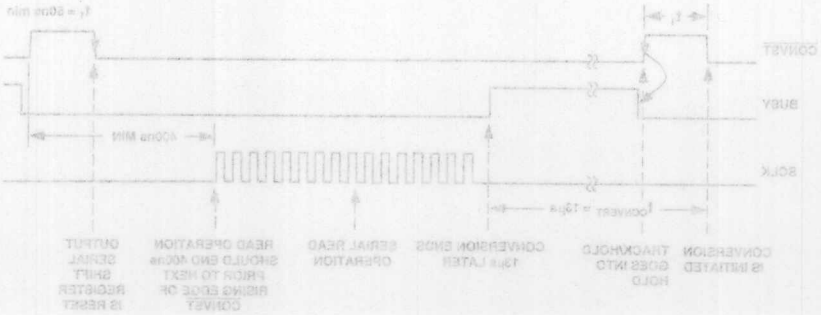
where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7896 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

PRELIMINARY TECHNICAL DATA



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OPERATING MODES

Mode 1 Operation (High Sampling Performance)

The timing diagram in Figure 2 is for optimum performance in Operating Mode 1 where the falling edge of $\overline{CONVST}$ starts conversion and puts the Track/Hold amplifier into its hold mode. This falling edge of $\overline{CONVST}$ also causes the BUSY signal to go high to indicate that a conversion is taking place. The BUSY signal goes low when the conversion is complete which is 8 µs max after the falling edge of $\overline{CONVST}$, and new data from this conversion is available in the output register of the AD7896. A read operation accesses this data. This read operation consists of 16 clock cycles, and the length of this read operation will depend on the serial clock frequency. For the fastest throughput rate (with a serial clock of 10 MHz) the read operation will take 1.6 µs. The read operation must be complete at least 400 ns before the falling edge of the next $\overline{CONVST}$, and this gives a total time of 10 µs for the full throughput time (equivalent to 100 kHz). This mode of operation should be used for high sampling applications.

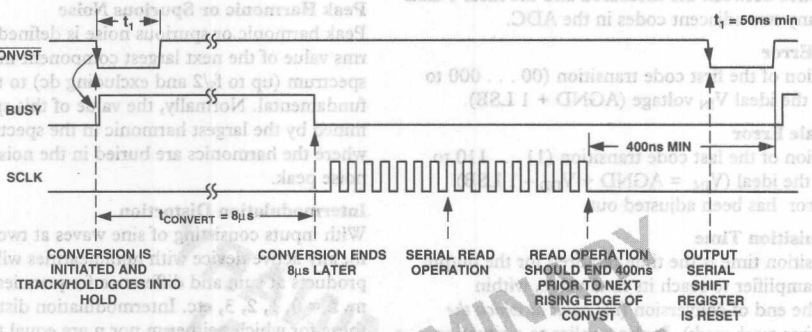


Figure 2. Mode 1 Timing Operation Diagram for High Sampling Performance

Mode 2 Operation (Auto Sleep After Conversion)

The timing diagram in Figure 3 is for optimum performance in Operating Mode 2 where the part automatically goes into sleep mode once BUSY goes low after conversion and "wakes up" before the next conversion takes place. This is achieved by keeping $\overline{CONVST}$ low at the end of conversion whereas it was high at the end of conversion for Mode 1 operation. The rising edge of $\overline{CONVST}$ "wakes up" the part. This wake-up time is 5 µs at which point the Track/Hold amplifier goes into its hold mode. The conversion takes 8 µs after this, provided the $\overline{CONVST}$ has gone low, giving a total of 13 µs from the rising edge of $\overline{CONVST}$ to the conversion being complete which is indicated by the BUSY going low. Note that since the wake-up time from the rising edge of $\overline{CONVST}$ is 5 µs, when the $\overline{CONVST}$ pulse width is greater than 5 µs the conversion will take more than the 13 µs shown in diagram from the rising edge of $\overline{CONVST}$. This is because the Track/Hold amplifier goes into its hold mode on the falling edge of $\overline{CONVST}$ and then the conversion will not be complete for a further 8 µs. In this case the BUSY will be the best indicator for when the conversion is complete. Even though the part is in sleep mode, data can still be read from the part. The read operation consists of 16 clock cycles as in Mode 1 operation. For the fastest serial clock of 10 MHz the read operation will take 1.6 µs, and this must be complete at least 400 ns before the falling edge of the next $\overline{CONVST}$ to allow the Track/Hold amplifier to have enough time to settle. This mode is very useful when the part is converting at a slow rate as the power consumption will be significantly reduced from that of Mode 1 operation.

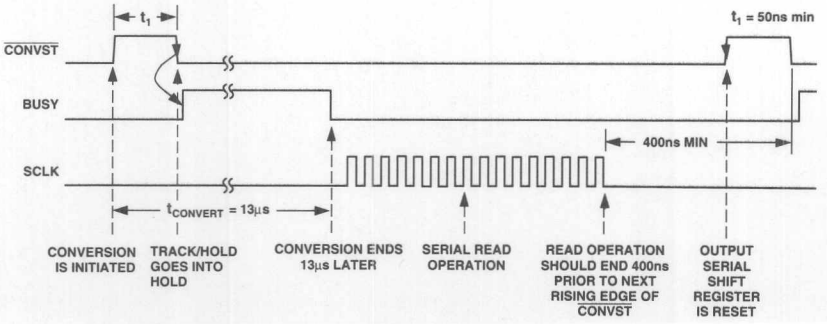


Figure 3. Mode 2 Timing Diagram Where Automatic Sleep Function Is Initiated

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

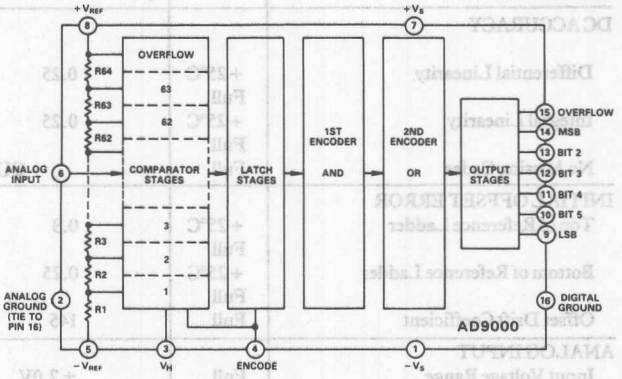
High Speed 6-Bit A/D Converter

AD9000

FEATURES
- 77MSPS Encode Rate
- Bipolar Input Range
- Low Error Rate
- Overflow Bit
- MIL-STD-883 Compliant Versions Available

APPLICATIONS
- QAM Telecommunications
- Electronic Warfare (ECM, ECCM, ESM)
- Radar Guidance Digitizers

FUNCTIONAL BLOCK DIAGRAM



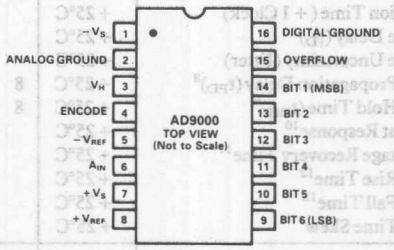
GENERAL DESCRIPTION

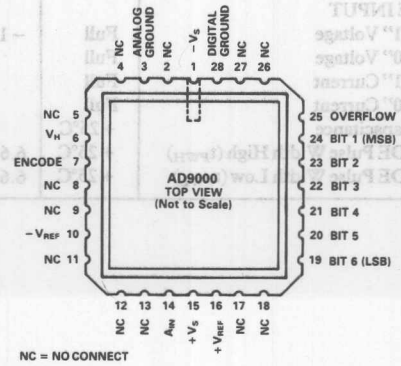
The AD9000 is a 6-bit, high speed, analog-to-digital converter with ECL compatible outputs and a bipolar input stage. The AD9000 is fabricated in a high-performance bipolar process which allows encode rates up to 77MSPS.

The AD9000 employs the standard flash converter architecture based on 64 individual comparators which simultaneously determine the precise analog signal level. The comparators are followed by two stages of decoding logic, allowing the AD9000 to operate with a very low error rate. The low 35pF input capacitance of the AD9000 greatly simplifies the analog driver stage. Also incorporated into the AD9000 design is an overflow output bit as well as a hysteresis control pin to modify comparator sensitivity.

The AD9000 is offered as both an commercial temperature range device 0 to +70°C, and as an extended temperature range device −55°C to +125°C. Both versions are available packaged in a 16-pin ceramic DIP. The extended temperature range device is also available in a 28-pin ceramic LCC package. The extended temperature range versions are offered as fully compliant MIL-STD-883 Class B devices.

PIN DESIGNATIONS





NC = NO CONNECT

ORDERING GUIDE

Model[1]	Temperature Range	Description	Package Option[2]
AD9000JD	0 to +70°C	16-Pin DIP, Industrial	D-16
AD9000SD	−55°C to +125°C	16-Pin DIP	D-16
AD9000SE	−55°C to +125°C	28-Pin LCC	E-28A

NOTES
[1]MIL-STD-883 versions available, contact factory.
[2]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier. For outline information see Package Information section.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9000—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (Supply Voltages = −5.2V and +5.0V; Differential Reference Voltage = 2.0V unless otherwise stated)

		Commercial 0 to +70°C AD9000JD			Military −55°C to +125°C AD9000SD/SE			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
RESOLUTION		6			6			Bits
DC ACCURACY								
Differential Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Integral Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
No Missing Codes	Full		GUARANTEED			GUARANTEED		
INITIAL OFFSET ERROR								
Top of Reference Ladder	+25°C		0.3	7/8		0.3	7/8	LSB
	Full			1.5			1.5	LSB
Bottom of Reference Ladder	+25°C		0.25	7/8		0.25	7/8	LSB
	Full			1.5			1.5	LSB
Offset Drift Coefficient	Full		145			145		µV/°C
ANALOG INPUT								
Input Voltage Range	Full		±2.0V			±2.0V		V
Input Bias Current (Sampling)[5]	Full			800			800	µA
Input Bias Current (Latched)[5]	Full			20			20	µA
Input Resistance	+25°C		3.0			3.0		kΩ
Input Capacitance	+25°C		35	50		35	50	pF
Full Power Bandwidth[6]	+25°C		20			20		MHz
REFERENCE INPUT[2, 3]								
Reference Ladder Resistance	+25°C	80		200	80		200	Ω
Ladder Temperature Coefficient			0.275			0.275		Ω/°C
Reference Input Bandwidth	+25°C		20			20		MHz
DYNAMIC PERFORMANCE[7]								
Conversion Rate	+25°C	50	70		75	77		MHz
Conversion Time (+1 Clock)	+25°C			20			13.3	ns
Aperture Delay (t_D)	+25°C		2			2		ns
Aperture Uncertainty (Jitter)	+25°C		25			25		ps
Output Propagation Delay (t_{PD})[8]	+25°C	8		12	8		12	ns
Output Hold Time (t_{OH})[9]	+25°C	8		14	8		14	ns
Transient Response[10]	+25°C		13			13		ns
Overvoltage Recovery Time[11]	+25°C		11			11		ns
Output Rise Time[12]	+25°C			5.0			4.5	ns
Output Fall Time[12]	+25°C			5.0			4.5	ns
Output Time Skew	+25°C		0.4			0.4		ns
ENCODE INPUT								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
Logic "1" Current	Full			100			100	µA
Logic "0" Current	Full			100			100	µA
Input Capacitance	+25°C		2.5	5.0		2.5	5.0	pF
ENCODE Pulse Width High (t_{PWH})	+25°C	6.6			6.6			ns
ENCODE Pulse Width Low (t_{PWL})	+25°C	6.6			6.6			ns

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Temp	Commercial 0 to +70°C AD9000JD Min	Typ	Max	Military −55°C to +125°C AD9000SD/SE Min	Typ	Max	Units
AC LINEARITY[11]								
Dynamic Linearity[12]	+25°C		0.5			0.5		LSB
In-Band Harmonics								
(DC to 1MHz)	+25°C		44			44		dBc
(1MHz to 5MHz)	+25°C		42			42		dBc
(5MHz to 8MHz)	+25°C		38			38		dBc
Signal to Noise Ratio[13]	+25°C	31	33		31	33		dB
Signal to Noise Ratio[14]	+25°C	40	42		40	42		dB
Two Tone Intermodulation Rejection[15]	+25°C		46			46		dBc
Noise Power Ratio (NPR)[16]	+25°C		30			30		dBc
DIGITAL OUTPUTS[5]								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
POWER SUPPLY[17]								
Positive Supply Current (+5.0V)	+25°C		60	70		60	70	mA
	Full			75			75	mA
Negative Supply Current (−5.2V)	+25°C		68	80		68	80	mA
	Full			85			85	mA
Nominal Power Dissipation	+25°C		675			675		mW
Reference Ladder Dissipation	+25°C		20			20		mW

NOTES
[1] $A_{IN} = +V_{REF}$.
[2] Determined by 3dB reduction in reconstructed output at 75MSPS.
[3] Under normal operating conditions, the analog input voltages should not exceed nominal ±2V operating range, nor the supply voltages ($+V_S$ and $-V_S$), whichever is smaller.
[4] Under normal operating conditions the differential reference voltage may range from ±0.5V to ±2V; $+V_{REF} \geq -V_{REF}$.
[5] Output terminated with 100Ω resistors to −2.0V.
[6] Measured from the leading edge of ENCODE to data out on Bit 1 (MSB).
[7] Measured from the trailing edge of ENCODE to data out on Bit 1 (MSB).
[8] For full-scale step input, 6-bit accuracy is attained in specified time.
[9] Recovers to 6-bit accuracy in specified time, after 150% full-scale input overvoltage.
[10] Measured on Bit 1 (MSB) only.
[11] Measured at 50MSPS encode rate.
[12] Analog input frequency = 15MHz.
[13] RMS signal to RMS noise, with 540kHz analog input signal.
[14] Peak-to-peak signal to rms noise, with 540kHz analog input signal.
[15] $f_1 = 9.3$MHz; $f_2 = 7.6$MHz; Encode = 42MHz.
[16] DC to 8.2MHz noise bandwidth with 3.886MHz slot.
[17] Supply voltage should remain stable within ±5% for normal operation.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

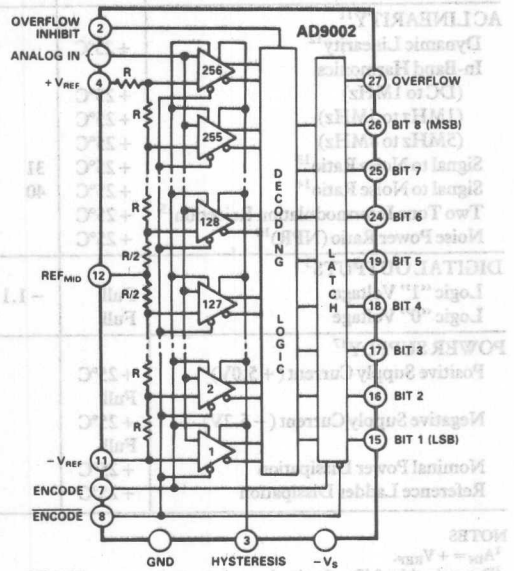
Positive Supply Voltage . . . . . −0.3V to +6V
Negative Supply Voltage . . . . . −6.0V to +0.3V
Analog-to-Digital Ground Voltage Differential 0.5
Analog Input Voltages (A_{IN}, $+V_{REF}$, $-V_{REF}$)[2] . . . . . ±3V
Differential Reference Voltage ($+V_{REF}$ to $-V_{REF}$)[3] 6V
ENCODE Input Voltage . . . . . $-V_S$ to 0V
HYSTERESIS Control Voltage . . . . . 0V to +3.0V
Digital Output Current 20mA
Power Dissipation (+25°C Free Air)[4] 745mW
Operating Temperature Range
AD9000JD . . . . . 0 to +70°C
AD9000SD/SE . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

NOTES
[1] Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] Under normal operating conditions, the analog input voltages should not exceed nominal ±2V operating range, nor the supply voltages ($+V_S$ and $-V_S$), whichever is smaller.
[3] Under normal operating conditions the differential reference voltage may range from ±0.5V to ±2V; $+V_{REF} \geq -V_{REF}$.
[4] Typical thermal impedances . . .
16-Pin Ceramic $\theta_{ja} = 67°C/W$; $\theta_{jc} = 7°C/W$
28-Pin LCC $\theta_{ja} = 62°C/W$; $\theta_{jc} = 14°C/W$

FEATURES
150MSPS Encode Rate
Low Input Capacitance: 17pF
Low Power: 750mW
−5.2V Single Supply
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Radar Systems
Digital Oscilloscopes/ATE Equipment
Laser/Radar Warning Receivers
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)
Communication/Signal Intelligence

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9002 is an 8-bit, high speed, analog-to-digital converter. The AD9002 is fabricated in an advanced bipolar process which allows operation at sampling rates in excess of 150 megasamples/second. Functionally, the AD9002 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the ECL compatible output latches.

An exceptionally wide large signal analog input bandwidth of 160MHz is due to an innovative comparator design and very close attention to device layout considerations. The wide input bandwidth of the AD9002 allows very accurate acquisition of high speed pulse inputs, without an external track-and-hold. The comparator output decoding scheme minimizes false codes which is critical to high speed linearity.

The AD9002 provides an external hysteresis control pin which can be used to optimize comparator sensitivity to further improve performance. Additionally, the AD9002's low power dissipation of 750mW makes it usable over the full extended temperature range. The AD9002 also incorporates an overflow bit to indicate overrange inputs. This overflow output can be disabled with the overflow inhibit pin.

The AD9002 is available in two grades, one with 0.5LSB linearity and one with 0.75LSB linearity. Both versions are offered in an industrial grade, −25°C to +85°C, packaged in a 28-pin DIP and a 28-pin JLCC. The military temperature range devices, −55°C to +125°C, are available in ceramic DIP and LCC packages and are compliant to MIL-STD-883 Class B.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($-V_S$) . . . . . −6V
Analog-to-Digital Supply Voltage Differential 0.5V
Analog Input Voltage . . . . . $-V_S$ to $+0.5V$
Digital Input Voltage . . . . . $-V_S$ to 0V
Reference Input Voltage ($+V_{REF} - V_{REF}$)[2] . . . −3.5V to 0.1V
Differential Reference Voltage 2.1V
Reference Midpoint Current . . . . . ±4mA
ENCODE to $\overline{\text{ENCODE}}$ Differential Voltage 4V
Digital Output Current 20mA
Operating Temperature Range
AD9002AD/BD/AJ/BJ . . . . . −25°C to +85°C
AD9002SE/SD/TD/TE . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

2

Electrical Characteristics ($-V_S = -5.2V$; Differential Reference Voltage = 2.0V, unless otherwise stated)

Parameter	Temp	Test Level	AD9002AD/AJ Min	AD9002AD/AJ Typ	AD9002AD/AJ Max	AD9002BD/BJ Min	AD9002BD/BJ Typ	AD9002BD/BJ Max	AD9002SD/SE Min	AD9002SD/SE Typ	AD9002SD/SE Max	AD9002TD/TE Min	AD9002TD/TE Typ	AD9002TD/TE Max	Units
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Linearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
Integral Linearity	+25°C	I		0.6	1.0		0.4	0.5		0.6	1.0		0.4	0.5	LSB
	Full	VI			1.2			1.2			1.2			1.2	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR															
Top of Reference Ladder	+25°C	I		8	14		8	14		8	14		8	14	mV
	Full	VI			17			17			17			17	mV
Bottom of Reference Ladder	+25°C	I		4	10		4	10		4	10		4	10	mV
	Full	VI			12			12			12			12	mV
Offset Drift Coefficient	Full	V		20			20			20			20		µV/°C
ANALOG INPUT															
Input Bias Current[4]	+25°C	I		60	100		60	100		60	100		60	100	µA
	Full	VI			200			200			200			200	µA
Input Resistance	+25°C	III	100	200		100	200		100	200		100	200		kΩ
Input Capacitance	+25°C	III		17	22		17	22		17	22		17	22	pF
Large Signal Bandwidth[5]	+25°C	V		160			160			160			160		MHz
Input Slew Rate[6]	+25°C	V		440			440			440			440		V/µs
REFERENCE INPUT															
Reference Ladder Resistance	+25°C	VI	64	80	110	64	80	110	64	80	110	64	80	110	Ω
Ladder Temperature Coefficient		V		0.25			0.25			0.25			0.25		Ω/°C
Reference Input Bandwidth	+25°C	V		10			10			10			10		MHz
DYNAMIC PERFORMANCE															
Conversion Rate	+25°C	I	125	150		125	150		125	150		125	150		MSPS
Aperture Delay	+25°C	V		1.3			1.3			1.3			1.3		ns
Aperture Uncertainty (Jitter)	+25°C	V		15			15			15			15		ps
Output Delay (t_{PD})[7,8]	+25°C	I	2.5	3.7	5.5	2.5	3.7	5.5	2.5	3.7	5.5	2.5	3.7	5.5	ns
Transient Response[9]	+25°C	V		6			6			6			6		ns
Overvoltage Recovery Time[10]	+25°C	V		6			6			6			6		ns
Output Rise Time[7]	+25°C	I			3.0			3.0			3.0			3.0	ns
Output Fall Time[7]	+25°C	I			2.5			2.5			2.5			2.5	ns
Output Time Skew[7,11]	+25°C	V		0.6			0.6			0.6			0.6		ns
ENCODE INPUT															
Logic "1" Voltage[7]	Full	VI	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage[7]	Full	VI			−1.5			−1.5			−1.5			−1.5	V
Logic "1" Current	Full	VI			150			150			150			150	µA
Logic "0" Current	Full	VI			120			120			120			120	µA
Input Capacitance	+25°C	V		3			3			3			3		pF
Encode Pulse Width (Low)[12]	+25°C	I	1.5			1.5			1.5			1.5			ns
Encode Pulse Width (High)[12]	+25°C	I	1.5			1.5			1.5			1.5			ns
OVERFLOW INHIBIT INPUT															
0V Input Current	Full	VI		144	300		144	300		144	300		144	300	µA
AC LINEARITY[13]															
Effective Bits[14]	+25°C	V		7.6			7.6			7.6			7.6		Bits
In-Band Harmonics															
dc to 1.23MHz	+25°C	I	48	55		48	55		48	55		48	55		dB
dc to 9.3MHz	+25°C	V		50			50			50			50		dB
dc to 19.3MHz	+25°C	V		44			44			44			44		dB
Signal-to-Noise Ratio[15]	+25°C	I	46	47.6		46	47.6		46	47.6		46	47.6		dB
Two Tone Intermod Rejection[16]	+25°C	V		60			60			60			60		dB
DIGITAL OUTPUTS[7]															
Logic "1" Voltage	Full	VI	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5			−1.5			−1.5	V
POWER SUPPLY[17]															
Supply Current (−5.2V)	+25°C	I		145	175		145	175		145	175		145	175	mA
	Full	VI			200			200			200			200	mA
Nominal Power Dissipation	+25°C	V		750			750			750			750		mW
Reference Ladder Dissipation	+25°C	V		50			50			50			50		mW
Power Supply Rejection Ratio[18]	+25°C	I		0.8	1.5		0.8	1.5		0.8	1.5		0.8	1.5	mV/V

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
[2]$+V_{REF} \geq -V_{REF}$ under all circumstances.
[3]Maximum junction temperature (t_J max) should not exceed 175°C for ceramic packages, and 150°C for plastic packages:

$t_J = PD\ (\theta_{JA}) + t_A$
$PD\ (\theta_{JC}) + t_C$

where
PD = power dissipation
θ_{JA} = thermal impedance from junction to ambient (°C/W)
θ_{JC} = thermal impedance from junction to case (°C/W)
t_A = ambient temperature (°C)
t_C = case temperature (°C)
typical thermal impedances are:
Ceramic DIP $\theta_{JA} = 56°C/W$; $\theta_{JC} = 20°C/W$
Plastic DIP $\theta_{JA} = 60°C/W$; $\theta_{JC} = 20°C/W$
Ceramic LCC $\theta_{JA} = 69°C/W$; $\theta_{JC} = 23°C/W$
PLCC $\theta_{JA} = 60°C/W$, $\theta_{JC} = 19°C/W$.

[4]Measured with AIN = 0V.
[5]Measured by FFT analysis where fundamental is −3dB FS.
[6]Input slew rate derived from rise time (10 to 90%) of full scale input.
[7]Outputs terminated through 100Ω to −2V.
[8]Measured from ENCODE in to data out for LSB only.
[9]For full-scale step input, 8-bit accuracy is attained in specified time.
[10]Recovers to 8-bit accuracy in specified time after 150% full-scale input overvoltage.
[11]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.
[12]ENCODE signal rise/fall times should be less than 10ns for normal operation.
[13]Measured at 125MSPS encode rate.
[14]Analog input frequency = 1.23MHz.
[15]RMS signal to rms noise, with 1.23MHz analog input signal.
[16]Input signals 1V p-p @1.23MHz and 1V p-p @2.30MHz.
[17]Supplies should remain stable within ±5% for normal operation.
[18]Measured at −5.2V ±5%.

Specifications subject to change without notice.

Recommended Operating Conditions

Parameter	Input Voltage Min	Nominal	Max
$-V_S$	−5.46	−5.20	−4.94
$+V_{REF}$	$-V_{REF}$	0.0V	+0.1
$-V_{REF}$	−2.1	−2.0	$+V_{REF}$
Analog Input	$-V_{REF}$		$+V_{REF}$

EXPLANATION OF TEST LEVELS

Test Level I	–	100% production tested.
Test Level II	–	100% production tested at +25°C, and sample tested at specified temperatures.
Test Level III	–	Sample tested only.
Test Level IV	–	Parameter is guaranteed by design and characterization testing.
Test Level V	–	Parameter is a typical value only.
Test Level VI	–	All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Linearity	Temperature Range	Package Option[1]
AD9002AD	0.75LSB	−25°C to +85°C	D-28
AD9002BD	0.50LSB	−25°C to +85°C	D-28
AD9002AJ	0.75LSB	−25°C to +85°C	J-28
AD9002BJ	0.50LSB	−25°C to +85°C	J-28
AD9002SD[2]	0.75 LSB	−55°C to +125°C	D-28
AD9002SE[2]	0.75 LSB	−55°C to +125°C	E-28A
AD9002TD[2]	0.50 LSB	−55°C to +125°C	D-28
AD9002TE[2]	0.50 LSB	−55°C to +125°C	E-28A

NOTES
[1]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; J = Ceramic Leaded Chip Carrier. For outline information see Package Information section.
[2]MIL-STD-883 versions.

FUNCTIONAL DESCRIPTION

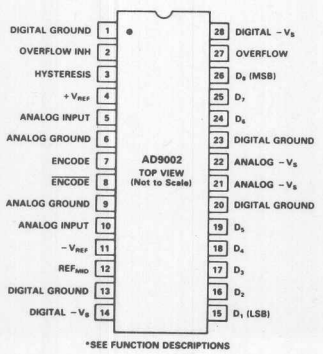
Pin #	Name	Description
1	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
2	OVERFLOW INH	OVERFLOW INHIBIT controls the data output polarity for overvoltage inputs.

ANALOG INPUT	OVERFLOW ENABLED (FLOATING OR −5.2V) OF	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	OVERFLOW INHIBITED (GND) OF	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8
$V_{IN} > +V_{REF}$	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$V_{IN} \leq +V_{REF}$	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X

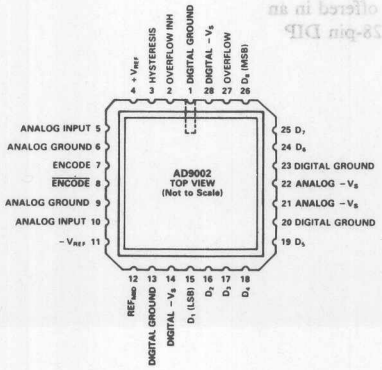
Pin #	Name	Description
3	HYSTERESIS	The Hysteresis control voltage varies the comparator hysteresis from 0mV to 10mV, for a change from −5.2V to −2.2V at the Hysteresis control pin. Normally connected to −5.2V.
4	$+V_{REF}$	The most positive reference voltage for the internal resistor ladder.
5	ANALOG INPUT	One of two analog input pins. Both analog input pins should be connected together.
6	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
7	ENCODE	Noninverted input of the differential encode input. This pin is driven in conjunction with $\overline{\text{ENCODE}}$. Data is latched on the rising edge of the ENCODE signal.
8	$\overline{\text{ENCODE}}$	Inverted input of the differential encode input. This pin is driven in conjunction with ENCODE.
9	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
10	ANALOG INPUT	One of two analog input pins. Both analog inputs should be connected together.
11	$-V_{REF}$	The most negative reference voltage for the internal resistor ladder.
12	REF_{MID}	The midpoint tap on the internal resistor ladder.
13	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
14	DIGITAL $-V_S$	One of two negative digital supply pins (nominally −5.2V). Both digital supply pins should be connected together.
15	D1	Digital data output (LSB).
16-19	D2-D5	Digital data output.
20	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
21, 22	ANALOG $-V_S$	One of two negative analog supply pins (nominally −5.2V). Both analog supply pins should be connected together.
23	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
24, 25	D6, D7	Digital data output.
26	D8	Digital data output (MSB).
27	OVERFLOW	Overflow data output. Logic high indicates an input overvoltage ($V_{IN} > +V_{REF}$) if OVERFLOW INHIBIT is enabled (overflow enabled, −5.2V). See OVERFLOW INHIBIT.
28	DIGITAL $-V_S$	One of two negative digital supply pins (nominally −5.2V). Both digital supply pins should be connected together.

PIN DESIGNATIONS

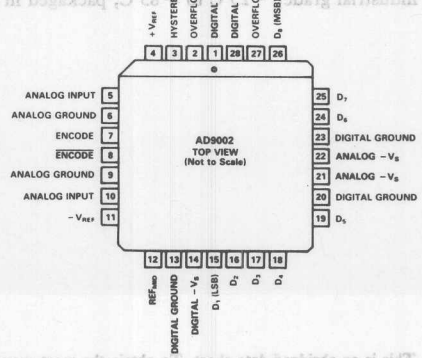
DIP



LCC



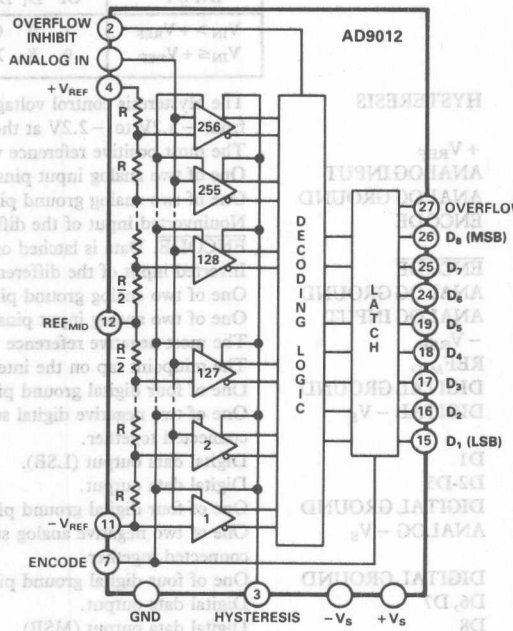
JLCC



FEATURES
100MSPS Encode Rate
Very Low Input Capacitance – 16pF
Low Power – 1W
TTL Compatible Outputs
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Radar Guidance
Digital Oscilloscopes/ATE Equipment
Laser/Radar Warning Receivers
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)
Communication/Signal Intelligence

FUNCTIONAL BLOCK DIAGRAM



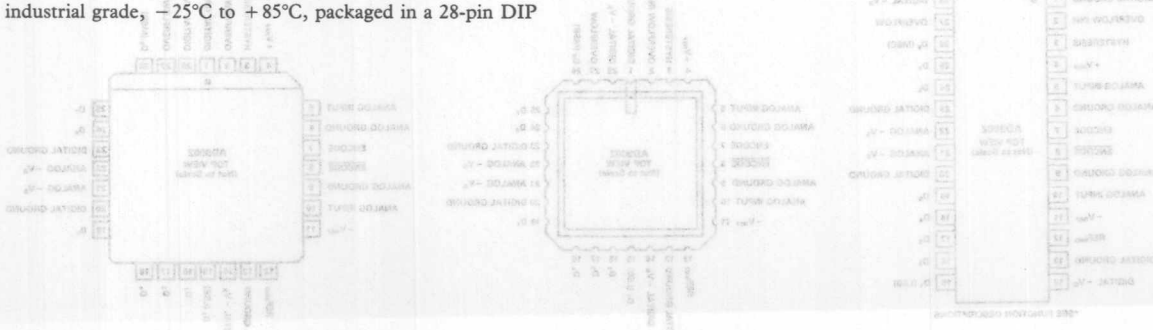
GENERAL DESCRIPTION

The AD9012 is an 8-bit, ultrahigh speed, analog-to-digital converter. The AD9012 is fabricated in an advanced bipolar process, which allows operation at sampling rates up to 100 megasamples/second. Functionally, the AD9012 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the TTL compatible output latches.

The exceptionally wide large signal analog input bandwidth of 160MHz is due to an innovative comparator design and very close attention to device layout considerations. The wide input bandwidth of the AD9012 allows very accurate acquisition of high speed pulse inputs without an external track-and-hold. The comparator output decoding scheme minimizes false codes, which is critical to high speed linearity.

The AD9012 is available in two grades, one with 0.5LSB linearity and one with 0.75LSB linearity. Both versions are offered in an industrial grade, −25°C to +85°C, packaged in a 28-pin DIP and a 28-pin JLCC. The military temperature range devices, −55°C to +125°C, are available in ceramic DIP and LCC packages and are compliant to MIL-STD-883 Class B.

The AD9012 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD9012/883B data sheet for detailed specifications.



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +6V
Analog to Digital Supply Voltage Differential ($-V_S$) . . . 0.5V
Negative Supply Voltage ($-V_S$) . . . . . −6V
Analog Input Voltage . . . . . $-V_S$ to +0.5V
ENCODE Input Voltage . . . . . −0.5V to +5V
OVERFLOW INH Input Voltage . . . . . −5.2V to 0V
Reference Input Voltage ($+V_{REF} - V_{REF}$)[2] . . −3.5V to +0.1V
Differential Reference Voltage 2.1V
Reference Midpoint Current . . . . . ±4mA
Digital Output Current 30mA
Operating Temperature Range
AD9012AQ/BQ/AJ/BJ . . . . . −25°C to +85°C
AD9012SE/SQ/TE/TQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

2

ELECTRICAL CHARACTERISTICS ($+V_S = +5.0V$; $-V_S = -5.2V$; Differential Reference Voltage = 2.0V, unless otherwise noted)

Parameter	Temp	Test Level	AD9012AQ/AJ Min	Typ	Max	AD9012BQ/BJ Min	Typ	Max	AD9012SQ/SE Min	Typ	Max	AD9012TQ/TE Min	Typ	Max	Units
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Linearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
Integral Linearity	+25°C	I		0.6	1.0		0.4	0.5		0.6	1.0		0.4	0.5	LSB
	Full	VI			1.2			1.2			1.2			1.2	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR															
Top of Reference Ladder	+25°C	I		7	15		7	15		7	15		7	15	mV
	Full	VI			18			18			18			18	mV
Bottom of Reference Ladder	+25°C	I		6	10		6	10		6	10		6	10	mV
	Full	VI			13			13			13			13	mV
Offset Drift Coefficient	Full	V		25			25			25			25		µV/°C
ANALOG INPUT															
Input Bias Current[4]	+25°C	I		60	100		60	100		60	100		60	100	µA
	Full	VI			200			200			200			200	µA
Input Resistance	+25°C	I	150	200		150	200		150	200		150	200		kΩ
Input Capacitance	+25°C	III		16	18		16	18		16	18		16	18	pF
Large Signal Bandwidth[5]	+25°C	V		160			160			160			160		MHz
Analog Input Slew Rate[6]	+25°C	V		440			440			440			440		V/µs
REFERENCE INPUT															
Reference Ladder Resistance	+25°C	VI	64	80	110	64	80	110	64	80	110	64	80	110	Ω
Ladder Temperature Coefficient		V		0.25			0.25			0.25			0.25		Ω/°C
Reference Input Bandwidth	+25°C	V		10			10			10			10		MHz
DYNAMIC PERFORMANCE															
Conversion Rate	+25°C	I	75	100		75	100		75	100		75	100		MSPS
Aperture Delay	+25°C	V		3.8			3.8			3.8			3.8		ns
Aperture Uncertainty (Jitter)	+25°C	V		15			15			15			15		ps
Output Delay (t_{PD})[7, 8]	+25°C	I	4	4.9	11	4	4.9	11	4	4.9	11	4	4.9	11	ns
Transient Response[9]	+25°C	V		8			8			8			8		ns
Overvoltage Recovery Time[10]	+25°C	V		8			8			8			8		ns
Output Rise Time[7]	+25°C	I		6.6	8.0		6.6	8.0		6.6	8.0		6.6	8.0	ns
Output Fall Time[7]	+25°C	I		3.3	4.3		3.3	4.3		3.3	4.3		3.3	4.3	ns
Output Time Skew[7, 11]	+25°C	V		3.0			3.0			3.0			3.0		ns
ENCODE INPUT															
Logic "1" Voltage[7]	Full	VI	2.0			2.0			2.0			2.0			V
Logic "0" Voltage[7]	Full	VI			0.8			0.8			0.8			0.8	V
Logic "1" Current	Full	VI			250			250			250			250	µA
Logic "0" Current	Full	VI			400			400			400			400	µA
Input Capacitance	+25°C	V		2.5			2.5			2.5			2.5		pF
Encode Pulse Width (Low)[12]	+25°C	I	2.5			2.5			2.5			2.5			ns
Encode Pulse Width (High)[12]	+25°C	I	2.5			2.5			2.5			2.5			ns
OVERFLOW INHIBIT INPUT															
0V Input Current	Full	VI		200	250		200	250		200	250		200	250	µA
AC LINEARITY[13]															
Effective Bits[14]	+25°C	V		7.5			7.5			7.5			7.5		Bits
In-Band Harmonics															
dc to 1.23MHz	+25°C	I	48	55		48	55		48	55		48	55		dBc
dc to 9.3MHz	+25°C	V		50			50			50			50		dBc
dc to 19.3MHz	+25°C	V		44			44			44			44		dBc
Signal-to-Noise Ratio[15]	+25°C	I	46	47.6		46	47.6		46	47.6		46	47.6		dBc
Noise Power Ratio[16]	+25°C	V		37			37			37			37		dBc
DIGITAL OUTPUT															
Logic "1" Voltage	Full	VI	2.4			2.4			2.4			2.4			V
Logic "0" Voltage	Full	VI			0.4			0.4			0.4			0.4	V
POWER SUPPLY[17]															
Positive Supply Current (+5.0V)	+25°C	I		33	45		33	45		33	45		33	45	mA
	Full	VI			48			48			48			48	mA
Supply Current (−5.2V)	+25°C	I		152	179		152	179		152	179		152	179	mA
	Full	VI			191			191			191			191	mA
Nominal Power Dissipation	+25°C	V		955			955			955			955		mW
Reference Ladder Dissipation	+25°C	V		44			44			44			44		mW
Power Supply Rejection Ratio[18]	+25°C	I		0.85	2.5		0.85	2.5		0.8	2.5		0.8	2.5	mV/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]$+V_{REF} \geq -V_{REF}$ under all circumstances.

[3]Maximum junction temperature (t_J max) should not exceed +175°C for ceramic packages, and +150°C for plastic packages:

$t_J = PD\ (\theta_{JA}) + t_A$

$PD\ (\theta_{JC}) + t_C$

where

PD = power dissipation

θ_{JA} = thermal impedance from junction to ambient (°C/W)

θ_{JC} = thermal impedance from junction to case (°C/W)

t_A = ambient temperature (°C)

t_C = case temperature (°C)

typical thermal impedances are:

Ceramic DIP $\theta_{JA} = 42°C/W$; $\theta_{JC} = 10°C/W$

Ceramic LCC $\theta_{JA} = 50°C/W$; $\theta_{JC} = 15°C/W$

JLCC $\theta_{JA} = 59°C/W$; $\theta_{JC} = 15°C/W$.

[4]Measured with Analog Input = 0V.

[5]Measured by FFT analysis where fundamental is −3dBc.

[6]Input slew rate derived from rise time (10% to 90%) of full-scale step input.

[7]Outputs terminated with two equivalent 'LS00 type loads. (See load circuit.)

[8]Measured from ENCODE into data out for LSB only.

[9]For full-scale step input, 8-bit accuracy is attained in specified time.

[10]Recovers to 8-bit accuracy in specified time, after 150% full-scale input overvoltage.

[11]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.

[12]ENCODE signal rise/fall times should be less than 30ns for normal operation.

[13]Measured at 75MSPS encode rate. Harmonic data based on worst case harmonics.

[14]Analog input frequency = 1.23MHz.

[15]RMS signal to rms noise, including harmonics with 1.23MHz analog input signal.

[16]NPR measured @ 0.5MHz. Noise Source is 250mW (rms) from 0.5MHz to 8MHz.

[17]Supplies should remain stable within ±5% for normal operation.

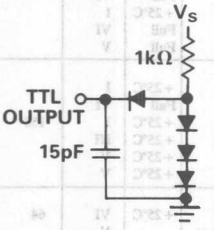
[18]Measured at −5.2V ±5% and +5.0V ±5%.

Specifications subject to change without notice.

Recommended Operating Conditions

Parameter	Input Voltage		
	Min	Nominal	Max
$-V_S$	−5.46	−5.20	−4.94
$+V_S$	+4.75	5.00	+5.25
$+V_{REF}$	$-V_{REF}$	0.0V	+0.1
$-V_{REF}$	−2.1	−2.0	$+V_{REF}$
Analog Input	$-V_{REF}$		$+V_{REF}$

LOAD CIRCUIT



EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.

Test Level II – 100% production tested at +25°C, and sample tested at specified temperatures.

Test Level III – Sample tested only.

Test Level IV – Parameter is guaranteed by design and characterization testing.

Test Level V – Parameter is a typical value only.

Test Level VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Device	Linearity	Temperature Range	Package Option*
AD9012AQ	0.75LSB	−25°C to +85°C	Q-28
AD9012BQ	0.50LSB	−25°C to +85°C	Q-28
AD9012AJ	0.75LSB	−25°C to +85°C	J-28
AD9012BJ	0.50LSB	−25°C to +85°C	J-28
AD9012SQ	0.75LSB	−55°C to +125°C	Q-28
AD9012SE	0.75LSB	−55°C to +125°C	E-28A
AD9012TQ	0.50LSB	−55°C to +125°C	Q-28
AD9012TE	0.50LSB	−55°C to +125°C	E-28A

*E = Leadless Ceramic Chip Carrier; J = Ceramic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

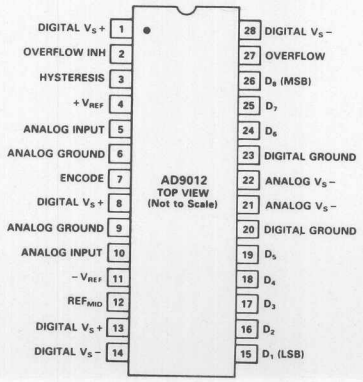
FUNCTIONAL DESCRIPTION

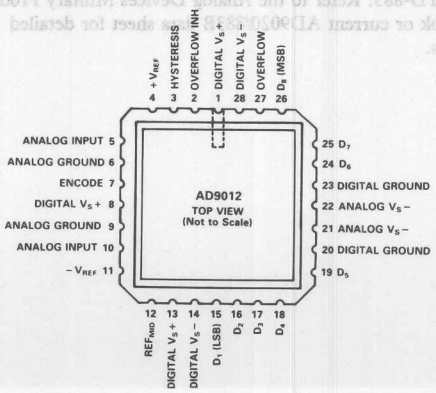
Pin #	Name	Description
1	DIGITAL $+V_S$	One of three positive digital supply pins (nominally $+5.0$V).
2	OVERFLOW INH	OVERFLOW INHIBIT controls the data output coding for overvoltage inputs (AIN$\geq +V_{REF}$).

ANALOG INPUT	OVERFLOW ENABLED (FLOATING OF D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8	OVERFLOW INHIBITED (GND) OF D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8
$V_{IN} \geq +V_{REF}$	1 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1
$V_{IN} < +V_{REF}$	0 X X X X X X X X	0 X X X X X X X X

3	HYSTERESIS	The Hysteresis control voltage varies the comparator hysteresis from 0mV to 10mV, for a change from -5.2V to -2.2V at the Hysteresis control pin.
4	$+V_{REF}$	The most positive reference voltage for the internal resistor ladder.
5	ANALOG INPUT	One of two analog input pins. Both analog input pins should be connected together.
6	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
7	ENCODE	TTL level encode command input. ENCODE is rising edge sensitive.
8	DIGITAL $+V_S$	One of three positive digital supply pins (nominally $+5.0$V).
9	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
10	ANALOG INPUT	One of two analog input pins. Both analog inputs should be connected together.
11	$-V_{REF}$	The most negative reference voltage for the internal resistor ladder.
12	REF_{MID}	The midpoint tap on the internal resistor ladder.
13	DIGITAL $+V_S$	One of three positive digital supply pins (nominally $+5.0$V)
14	DIGITAL $-V_S$	One of two negative digital supply pins (nominally -5.2V). Both digital supply pins should be connected together.
15	D_1 (LSB)	Digital data output. D_1 (LSB) is the least significant bit of the digital output word.
16-19	D_2-D_5	Digital data output.
20	DIGITAL GROUND	One of two digital ground pins. Both digital grounds pins should be connected together.
21, 22	ANALOG $-V_S$	One of two negative analog supply pins (nominally -5.2V). Both analog supply pins should be connected together.
23	DIGITAL GROUND	One of two digital ground pins. Both digital ground pins should be connected together.
24, 25	D_6, D_7	Digital data output.
26	D_8 (MSB)	Digital data output D_8 (MSB) is the most significant bit of the digital output word.
27	OVERFLOW	Overflow data output. Logic HIGH indicates an input overvoltage ($V_{IN} > +V_{REF}$), if OVERFLOW INHIBIT is enabled (overflow enabled, floating). See OVERFLOW INHIBIT.
28	DIGITAL $-V_S$	One of two negative digital supply pins (nominally -5.2V). Both digital supply pins should be connected together.

PIN DESIGNATIONS





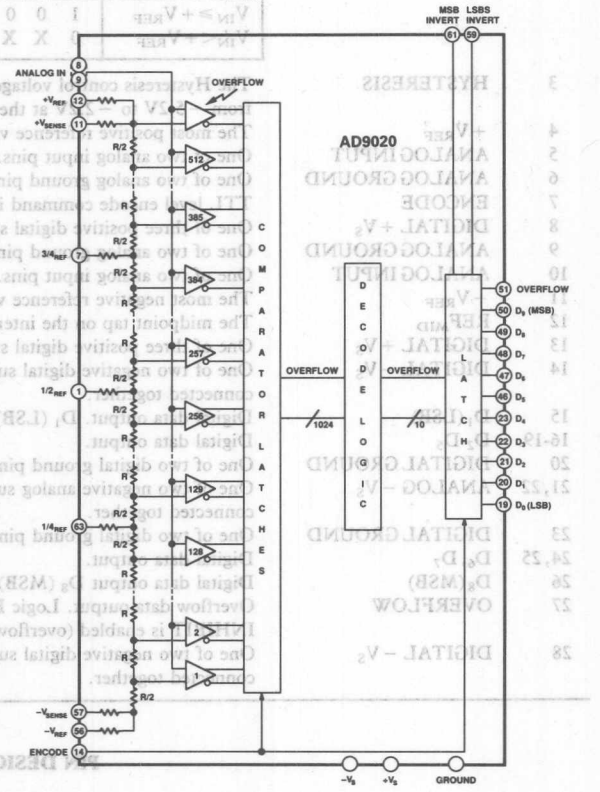
10-Bit 60 MSPS A/D Converter

AD9020

FEATURES
Monolithic 10-Bit/60 MSPS Converter
TTL Outputs
Bipolar (±1.75 V) Analog Input
56 dB SNR @ 2.3 MHz Input
Low (45 pF) Input Capacitance
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Digital Oscilloscopes
Medical Imaging
Professional Video
Radar Warning/Guidance Systems
Infrared Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

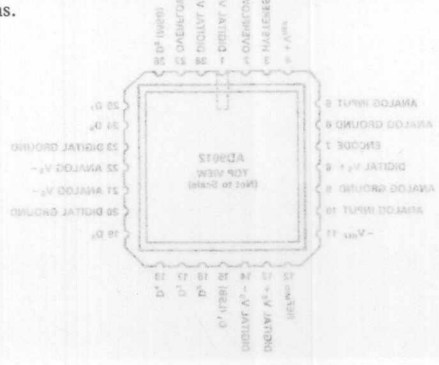
The AD9020 A/D converter is a 10-bit monolithic converter capable of word rates of 60 MSPS and above. Innovative architecture using 512 input comparators instead of the traditional 1024 required by other flash converters reduces input capacitance and improves linearity.

Encode and outputs are TTL-compatible, making the AD9020 an ideal candidate for use in low power systems. An overflow bit is provided to indicate analog input signals greater than $+V_{SENSE}$.

Voltage sense lines are provided to insure accurate driving of the $\pm V_{REF}$ voltages applied to the units. Quarter-point taps on the resistor ladder help optimize the integral linearity of the unit.

Either 68-pin ceramic leaded (gull wing) packages or ceramic LCCs are available and are specifically designed for low thermal impedances. Two performance grades for temperatures of both 0 to +70°C and −55°C to +125°C ranges are offered to allow the user to select the linearity best suited for each application. Dynamic performance is fully characterized and production tested at +25°C. MIL-STD-883 units are available.

The AD9020 A/D Converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD9020/883B data sheet for detailed specifications.



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6 V
$-V_S$	−6 V
ANALOG IN	−2 V to +2 V
$+V_{REF}$, $-V_{REF}$, $3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$	−2 V to +2 V
$+V_{REF}$ to $-V_{REF}$	4.0 V
DIGITAL INPUTS	−0.5 V to $+V_S$
$3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$ Current	±10 mA
Digital Output Current	20 mA
Operating Temperature	
AD9020JE/KE/JZ/KZ	0 to +70°C
Storage Temperature	−65°C to +150°C
Maximum Junction Temperature[2]	+175°C
Lead Soldering Temp (10 sec)	+300°C

2

ELECTRICAL CHARACTERISTICS ($\pm V_S$ = ±5 V; $\pm V_{SENSE}$ = ±1.75 V; ENCODE = 40 MSPS unless otherwise noted)[3]

Parameter (Conditions)	Temp	Test Level	AD9020JE/JZ Min	AD9020JE/JZ Typ	AD9020JE/JZ Max	AD9020KE/KZ Min	AD9020KE/KZ Typ	AD9020KE/KZ Max	Units
RESOLUTION			10			10			Bits
DC ACCURACY[3]									
Differential Nonlinearity	+25°C	I		1.0	1.25		0.75	1.0	LSB
	Full	VI			1.5			1.25	LSB
Integral Nonlinearity	+25°C	I		1.25	2.0		1.0	1.5	LSB
	Full	VI			2.5			2.0	LSB
No Missing Codes	Full	VI					Guaranteed		
ANALOG INPUT									
Input Bias Current[4]	+25°C	I		0.4	1.0		0.4	1.0	mA
	Full	VI			2.0			2.0	mA
Input Resistance	+25°C	I	2.0	7.0		2.0	7.0		kΩ
Input Capacitance[4]	+25°C	V		45			45		pF
Analog Bandwidth	+25°C	V		175			175		MHz
REFERENCE INPUT									
Reference Ladder Resistance	+25°C	I	22	37	56	22	37	56	Ω
	Full	VI	14		66	14		66	Ω
Ladder Tempco	Full	V		0.1			0.1		Ω/°C
Reference Ladder Offset									
Top of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Bottom of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Offset Drift Coefficient	Full	V		50			50		µV/°C
SWITCHING PERFORMANCE									
Conversion Rate	+25°C	I	60			60			MSPS
Aperture Delay (t_A)	+25°C	V		1			1		ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5		ps, rms
Output Delay (t_{OD})[5]	+25°C	I	6	10	13	6	10	13	ns
Output Time Skew[5]	+25°C	I		3	5		3	5	ns
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		10			10		ns
Overvoltage Recovery Time	+25°C	V		10			10		ns
Effective Number of Bits (ENOB)									
f_{IN} = 2.3 MHz	+25°C	I	8.6	9.0		8.6	9.0		Bits
f_{IN} = 10.3 MHz	+25°C	IV	8.0	8.4		8.0	8.4		Bits
f_{IN} = 15.3 MHz	+25°C	IV	7.5	8.0		7.5	8.0		Bits
Signal-to-Noise Ratio[6]									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	I	50	53		50	53		dB
f_{IN} = 15.3 MHz	+25°C	I	47	50		47	50		dB
Signal-to-Noise Ratio[6] (Without Harmonics)									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	I	51	54		51	54		dB
f_{IN} = 15.3 MHz	+25°C	I	48	52		48	52		dB

(CONTINUED)									
Harmonic Distortion									
f_{IN} = 2.3 MHz	+25°C	I	61	67		61	67		dBc
f_{IN} = 10.3 MHz	+25°C	I	55	59		55	59		dBc
f_{IN} = 15.3 MHz	+25°C	I	49	53		49	53		dBc
Two-Tone Intermodulation Distortion Rejection[7]	+25°C	V		70			70		dBc
Differential Phase	+25°C	V		0.5			0.5		Degree
Differential Gain	+25°C	V		1			1		%
ENCODE INPUT									
Logic "1" Voltage	Full	VI	2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			20			20	μA
Logic "0" Current	Full	VI			800			800	μA
Input Capacitance	+25°C	V		5			5		pF
Pulse Width (High)	+25°C	I	6			6			ns
Pulse Width (Low)	+25°C	I	6			6			ns
DIGITAL OUTPUTS									
Logic "1" Voltage (I_{OH} = 2 mA)	Full	VI	2.4			2.4			V
Logic "0" Voltage (I_{OL} = 10 mA)	Full	VI			0.4				V
POWER SUPPLY									
$+V_S$ Supply Current	+25°C	I		440	530		440	530	mA
	Full	VI			542			542	mA
$-V_S$ Supply Current	+25°C	I		140	170		140	170	mA
	Full	VI			177			177	mA
Power Dissipation	+25°C	I		2.8	3.3		2.8	3.3	W
	Full	VI			3.4			3.4	W
Power Supply Rejection Ratio (PSRR)[8]	Full	VI		6	10		6	10	mV/V

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances (part soldered onto board): 68-pin leaded ceramic chip carrier: θ_{JC} = 1°C/W; θ_{JA} = 17°C/W (no air flow); θ_{JA} = 15°C/W (air flow = 500 LFM). 68-pin ceramic LCC: θ_{JC} = 2.6°C/W; θ_{JA} = 15°C/W (no air flow); θ_{JA} = 13°C/W (air flow = 500 LFM).

[3]$3/4_{REF}$, $1/2_{REF}$, and $1/4_{REF}$ reference ladder taps are driven from dc sources at +0.875 V, 0 V, and −0.875 V, respectively. Accuracy of the overflow comparator is not tested and not included in linearity specifications.

[4]Measured with ANALOG IN = $+V_{SENSE}$.

[5]Output delay measured as worst-case time from 50% point of the rising edge of ENCODE to 50% point of the slowest rising or falling edge of D_0–D_9. Output skew measured as worst-case difference in output delay among D_0–D_9.

[6]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

[7]Intermodulation measured with analog input frequencies of 2.3 MHz and 3.0 MHz at 7 dB below full scale.

[8]Measured as the ratio of the worst-case change in transition voltage of a single comparator for a 5% change in $+V_S$ or $-V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

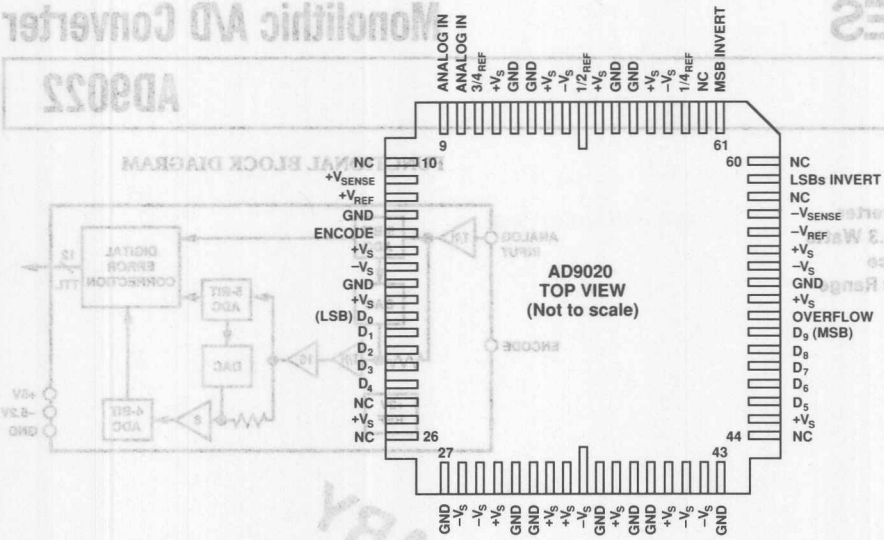
V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Device	Temperature Range	Description	Package Option*
AD9020JZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9020JE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9020KZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9020KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9020SZ/883	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9020SE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9020TZ/883	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9020TE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9020/PCB	0 to +70°C	Evaluation Board	

*E = Ceramic Leadless Chip Carrier; Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.



AD9020 Pin Designations

AD9020 PIN DESCRIPTIONS

Pin No.	Name	Function
1	$1/2_{REF}$	Midpoint of internal reference ladder.
2, 16, 28, 29, 35, 41, 42, 54, 64	$-V_S$	Negative supply voltage; nominally −5.0 V ±5%.
3, 6, 15, 18, 25, 30, 33, 34, 37, 40, 45, 52, 55, 65, 68	$+V_S$	Positive supply voltage; nominally +5 V ±5%.
4, 5, 13, 17, 27, 31, 32 36, 38, 39, 43, 53, 66, 67	GROUND	All ground pins should be connected together and to low-impedance ground plane.
7	$3/4_{REF}$	Three-quarter point of internal reference ladder.
8, 9	ANALOG IN	Analog input; nominally between ±1.75 V.
11	$+V_{SENSE}$	Voltage sense line to most positive point on internal resistor ladder. Normally +1.75 V.
12	$+V_{REF}$	Voltage force connection for top of internal reference ladder. Normally driven to provide +1.75 V at $+V_{SENSE}$.
14	ENCODE	TTL-compatible convert command used to begin digitizing process.
19–23, 46–50	D_0–D_9	TTL-compatible digital output data.
51	OVERFLOW	TTL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
56	$-V_{REF}$	Voltage force connection for bottom of internal reference ladder. Normally driven to provide −1.75 V at $-V_{SENSE}$.
57	$-V_{SENSE}$	Voltage sense line to most negative point on internal resistor ladder. Normally −1.75 V.
59	LSBs INVERT	Normally grounded. When connected to $+V_S$, lower order bits (D_0–D_8) are inverted.
61	MSB INVERT	Normally grounded. When connected to $+V_S$, most significant bit (MSB; D_9) is inverted.
63	$1/4_{REF}$	One-quarter point of internal reference ladder.

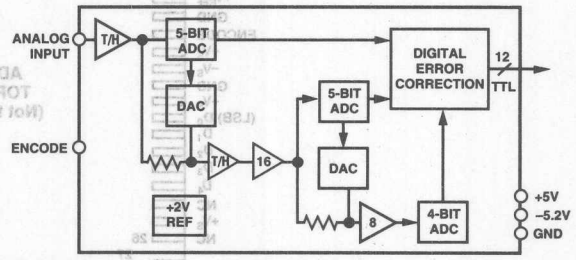
12-Bit 20 MSPS Monolithic A/D Converter

AD9022

FEATURES
Monolithic
12-Bit 20 MSPS A/D Converter
Low Power Dissipation: 1.3 Watts
On-Chip T/H and Reference
High-Spurii Free Dynamic Range
TTL Logic

APPLICATIONS
Radar Receivers
Digital Communications
Digital Instrumentation
Electro-Optics

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD9022 is a high speed, high performance, monolithic 12-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference, are included on chip to provide a complete conversion solution. It is a companion unit to the AD9023; the primary difference between the two is that all logic for the AD9022 is TTL compatible, while the AD9023 utilizes ECL logic for digital inputs and outputs. Pinouts for the two parts are nearly identical.

Operating from +5 V and –5.2 V supplies, the AD9022 provides excellent dynamic performance. Sampling at 20 Msps with A_{IN} = 1 MHz, the spurious free dynamic range (SFDR) is typically 80 dB; with A_{IN} = 9.6 MHz, SFDR is 74 dB. SNR is typically 65 dB.

The on-board T/H has a 100 MHz bandwidth and, more importantly, is designed to provide excellent dynamic performance for analog input frequencies above Nyquist. This feature is necessary in many under-sampling signal processing applications, such as in direct IF to digital conversion.

To maintain dynamic performance at higher IFs, monolithic RF track-and-holds (such as the AD9100 and AD9101 Samplifier™) can be used with the AD9022 to process signals up to and beyond 70 MHz.

Samplifier is a trademark of Analog Devices, Inc.

With DNL typically less than 0.5 LSB and 20 ns transient response settling time, the AD9022 provides excellent results when low-frequency analog inputs must be oversampled (such as CCD digitization). The full scale analog input is ±1 V with a 300 Ω input impedance. The analog input can be driven directly from the signal source, or can be buffered by the AD96xx series of low noise, low distortion buffer amplifiers.

All timing is internal to the AD9022; the clock signal initiates the conversion cycle. For best results, the encode command should contain as little jitter as possible. High speed layout practices must be followed to ensure optimum A/D performance.

The AD9022 is built on a trench isolated bipolar process and utilizes an innovative multipass architecture (see the block diagram). The unit is packaged in 28-pin ceramic DIPs and gullwing surface mount packages. The AD9022 is specified to operate over the industrial (–25°C to +85°C) and military (–55°C to +125°C) temperature ranges.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = −5.2 V; Encode = 20 MSPS, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9022AQ/AZ Min	AD9022AQ/AZ Typ	AD9022AQ/AZ Max	AD9022BQ/BZ Min	AD9022BQ/BZ Typ	AD9022BQ/BZ Max	AD9022SQ/SZ Min	AD9022SQ/SZ Typ	AD9022SQ/SZ Max	Units
RESOLUTION			12			12			12			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		0.4	0.75		0.25	0.5		0.4	0.75	LSB
	Full	VI			1.0			0.75			1.0	LSB
Integral Nonlinearity	+25°C	I		1.2	2.5		1.2	2.0		1.2	2.5	LSB
	Full	VI		1.25	3.0		1.25	3.0		1.25	3.0	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed			Guaranteed		
Offset Error	+25°C	I		5	25		5	25		5	25	mV
	Full	VI		15	35		15	35		15	35	mV
Gain Error	+25°C	I		±0.5	±2.5		±0.5	±2.5		±0.5	±2.5	% FS
	Full	VI		0.5	3.5		0.5	3.5		0.5	3.5	% FS
Thermal Noise	+25°C	V		0.5			0.5			0.5		LSB, rms
ANALOG INPUT												
Input Voltage Range				±1.024			±1.024			±1.024		V
Input Resistance	Full	IV	250	300	375	250	300	375	250	300	375	Ω
Input Capacitance	+25°C	V		7			7			7		pF
Analog Bandwidth	+25°C	IV		115			115			115		MHz
SWITCHING PERFORMANCE[1]												
Minimum Conversion Rate	+25°C	IV			2			2			2	Msps
Maximum Conversion Rate	Full	VI	20			20			20			Msps
Aperture Delay (t_A)	+25°C	IV	0.82	1.12	1.42	0.82	1.12	1.42	0.82	1.12	1.42	ns
Aperture Uncertainty (Jitter)	+25°C	IV										ps, rms
Output Delay (t_{OD})	Full	IV	14.5		33.5	14.5		33.5	14.5		33.5	ns
ENCODE INPUT												
Logic Compatibility				TTL			TTL			TTL		
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8			0.8	V
Logic "1" Current	Full	VI		7	20		7	20		7	20	µA
Logic "0" Current	Full	VI		7	20		7	20		7	20	µA
Input Capacitance	+25°C	V		4			4			4		pF
Pulse Width (High)	+25°C	IV	25		250	25		250	25		250	ns
Pulse Width (Low)	+25°C	IV	17.5		250	17.5		250	17.5		250	ns
DYNAMIC PERFORMANCE												
Transient Response	+25°C	V		20			20			20		ns
Overvoltage Recovery Time	+25°C	V		20			20			20		ns
Harmonic Distortion												
Analog Input @ 1.2 MHz	+25°C	I	65	73		70	75		65	73		dBc
@ 1.2 MHz	Full	VI	65	70		70	75		65	70		dBc
@ 4.3 MHz	+25°C	V		75			75			75		dBc
@ 9.6 MHz	+25°C	I	63	74		70	74		63	74		dBc
@ 9.6 MHz	Full	VI	61	70		70	72		61	70		dBc
Signal-to-Noise Ratio[2]												
Analog Input @ 1.2 MHz	+25°C	I	62	65		65	67		62	65		dB
@ 1.2 MHz	Full	VI	61	64		64	66		61	64		dB
@ 4.3 MHz	+25°C	V		65			65			65		dB
@ 9.6 MHz	+25°C	I	61	64		64	66		61	64		dB
@ 9.6 MHz	Full	VI	60	63		63	65		60	63		dB
Signal-to-Noise Ratio[2] (Without Harmonics)												
Analog Input @ 1.2 MHz	+25°C	I	65	66		66	67		65	66		dB
@ 1.2 MHz	Full	VI	63	64		65	66		63	64		dB
@ 4.3 MHz	+25°C	V		66			66			66		dB
@ 9.6 MHz	+25°C	I	62	65		65	66		62	65		dB
@ 9.6 MHz	Full	VI	60	63		64	65		60	63		dB

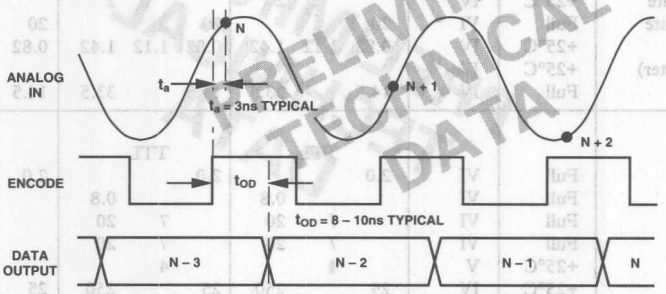
PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Two-Tone Intermodulation Distortion Rejection[3]	+25°C	V	76			76			76			dBc
DIGITAL OUTPUTS[1]												
Logic Compatibility				TTL			TTL			TTL		
Logic "1" Voltage	Full	VI	2.4			2.4			2.4			V
Logic "0" Voltage	Full	VI			0.5			0.5			0.5	V
Output Coding				Offset Binary			Offset Binary			Offset Binary		
POWER SUPPLY												
$+V_S$ Supply Voltage	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	mA
$+V_S$ Supply Current	Full	VI		100	120		100	120		100	120	mA
$-V_S$ Supply Voltage	Full	VI	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	mA
$-V_S$ Supply Current	Full	VI		160	190		160	190		160	190	mA
Power Dissipation	Full	VI		1.3	1.6		1.3	1.6		1.3	1.6	W
Power Supply Rejection Ratio (PSRR)[4]	Full	IV		28			28			28		mV/V

NOTES
[1]AD9022 load is a single LS latch.
[2]RMS signal-to-rms noise with analog input signal 1 dB below full scale at specified frequency.
[3]Intermodulation measured with analog input frequencies of 9.3 MHz and 9.6 MHz at 7 dB below full scale.
[4]PSRR is sensitivity of offset error to power supply variations within the 5% limits shown.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA



AD9022 Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ ..... +6 V
$-V_S$ ..... –6 V
Analog Input ..... $-V_S$ to $+V_S$
Digital Inputs ..... $-V_S$ to 0 V
Digital Output Current ..... 20 mA
Gain Adjust ..... $-V_S$ to $+V_S$
Offset Adjust ..... $-V_S$ to $+V_S$
Operating Temperature Range (Case)
AD9022AQ/AZ/BQ/BZ ..... –25°C to +85°C
AD9022SQ/SZ ..... –55°C to +125°C
Maximum Junction Temperature[2] ..... +175°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Storage Temperature Range ..... –65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: "Q" Package (Ceramic DIP): θ_{JC} = 10°C/W; θ_{JA} = 35°C/W. "Z" Package (Gullwing Surface Mount): θ_{JC} = 13°C/W; θ_{JA} = 45°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9022AQ/BQ	–25°C to +85°C	28-Pin Ceramic DIP	Q-28
AD9022AZ/BZ	–25°C to +85°C	28-Pin Ceramic Leaded Chip Carrier	Z-28
AD9022SQ	–55°C to +125°C	28-Pin Ceramic DIP	Q-28
AD9022SZ	–55°C to +125°C	28-Pin Ceramic Leaded Chip Carrier	Z-28

*For outline information see Package Information section.

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I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; guaranteed by design and characterization testing for industrial devices.

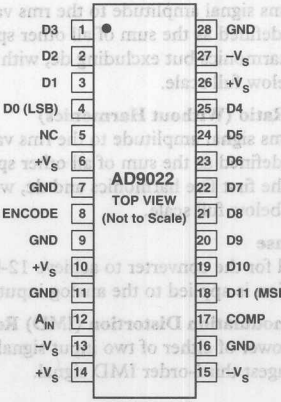
DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions	205 × 228 × 21 (±1) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Transistor Count	4,080
Passivation	Oxynitride
Die Attach	Silver Glass
Bond Wire	Aluminum

PRELIMINARY TECHNICAL DATA

Pin No.	Name	Function
1–3	D3–D1	Digital output bits of ADC; TTL/CMOS compatible.
4	D0 (LSB)	Least significant bit of ADC output; TTL/CMOS compatible.
5	NC	No Connection Internally
6	$+V_S$	+5 V Power Supply
7	GND	Ground
8	ENCODE	Encode clock input to ADC. Internal T/H is placed in hold mode (ADC is encoding) on rising edge of encode signal.
9	GND	Ground
10	$+V_S$	+5 V Power Supply
11	GND	Ground
12	A_{IN}	Noninverting input to T/H amplifier.
13	$-V_S$	–5.2 V Power Supply
14	$+V_S$	+5 V Power Supply
15	$-V_S$	–5.2 V Power Supply
16	GND	Ground
17	COMP	Should be connected to $-V_S$ through 0.1 µF capacitor.
18	D11 (MSB)	Most significant bit of ADC output; TTL/CMOS compatible.
19–25	D10–D4	Digital output bits of ADC; TTL/CMOS compatible.
26	$+V_S$	+5 V Power Supply
27	$-V_S$	–5.2 V Power Supply
28	GND	Ground

PIN DESIGNATIONS



NC = NO CONNECT
COMPENSATION (PIN 17) SHOULD BE CONNECTED TO $-V_S$ THROUGH 0.01µF

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DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Harmonic Distortion
The rms value of the fundamental divided by the rms value of the worst harmonic component.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency tested drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between the 50% point of the rising edge of the ENCODE command and the time when all output data bits are within valid logic levels.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 12-bit accuracy after an analog input signal 150% of full scale is reduced to the full-scale range of the converter.

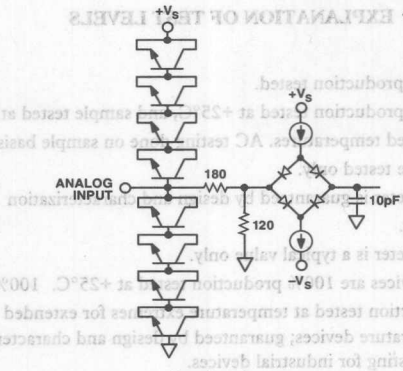
Power Supply Rejection Ratio (PSRR)
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1 dB below full scale.

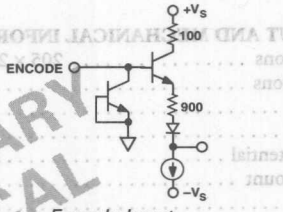
Signal-to-Noise Ratio (Without Harmonics)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, excluding the first five harmonics and dc, with an analog input signal 1 dB below full scale.

Transient Response
The time required for the converter to achieve 12-bit accuracy when a step function is applied to the analog input.

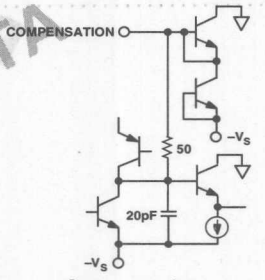
Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of either of two input signals to the power of the strongest third-order IMD signal.



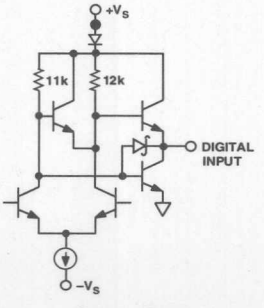
Analog Input



Encode Input



Compensation



Output Stage

Figure 1. Equivalent Circuits

PRELIMINARY TECHNICAL DATA

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THEORY OF OPERATION

Refer to the block diagram.

The AD9022 employs a three pass subranging architecture and digital error correction. This combination of design techniques ensures 12-bit accuracy at relatively low power.

Analog input signals are immediately attenuated through a resistor divider and applied directly to the sampling bridge of the track-and-hold (T/H). The T/H holds whatever analog value is present when the unit is strobed with an ENCODE command. The conversion process begins on the rising edge of this pulse, which should conform to the minimum and maximum pulse width requirements shown in the specifications. Operation below the recommended encode rate (2 Msps) may result in excessive droop in the internal T/H devices–leading to large dc and ac errors.

The held analog value of the first track-and-hold is applied to a 5-bit flash converter and a second T/H. The 5-bit flash converter resolves the most significant bits (MSBs) of the held analog voltage. These 5 bits are reconstructed via a 5-bit DAC and subtracted from the original T/H output signal to form a residue signal.

A second T/H holds the amplified residue signal while it is encoded with a second 5-bit flash ADC. Again the 5 bits are reconstructed and subtracted from the second T/H output to form a residue signal. This residue is amplified and encoded with a 4-bit flash ADC to provide the 3 least significant bits (LSBs) of the digital output and one bit of error correction.

Digital Error Correction logic aligns the data from the three flash converters and presents the result as a 12-bit parallel digital word. The output stage of the AD9022 is TTL. Output data may be strobed on the rising edge of the ENCODE command.

AD9022 IN RECEIVER APPLICATIONS

Advances in semiconductor processes have resulted in low cost digital signal processing (DSP) and analog signal processing which can help create cost effective alternative receiver designs. Today, an all-digital receiver allows tuning, demodulation, and detection of receiver signals in the digital domain. By digitizing IF signals directly and utilizing digital techniques, it becomes possible to make significant improvements in receiver design. For high frequency IFs, the ADC is the key to the receiver's performance. Unfortunately, the specifications frequently used by receiver designers and analog-to-digital (ADC) manufacturers are often very different. Noise Figure and Intercept Point are common measures of noise and linearity in analog RF system design. ADCs are more frequently specified in terms of SNR and harmonic distortion.

Noise

Noise figure (NF) is a measure of receiver sensitivity and is defined as the degradation of signal-to-noise ratio (SNR) as a signal passes through a device. In equation form:

$$NF = SNR\ (in) - SNR\ (out)$$

Noise figure is a bandwidth invariant parameter for reasonably narrow bandwidths in most devices. The system noise figure for a combination of amplifiers and mixers, for instance, can be analyzed without regard to the information bandwidth.

Thermal noise contribution from the ADC behaves in a similar fashion; however, the spectral density of quantization noise is a function of the sample rate. In addition, the spectral density of the quantization noise is flat only in an ADC with perfect linearity, i.e., perfect 1 LSB step sizes.

To analyze the system noise performance, ADC noise figure is calculated by normalizing the SNR of the ADC output to a 1 Hz bandwidth. This result is given by:

$$SNR\ (/Hz) = SNR + 10\ log_{10}\ (Fs/2)$$

where Fs is the sample rate.

This will be true only for converters in which perfect quantization noise dominates. There may be an upper sample rate, above which the thermal noise of the converter is the dominant source of noise. In this case, normalization would be based on the noise bandwidth of the ADC. For an AD9022 with a typical SNR of 64 dB and a sample rate of 20 Msps, the normalized SNR is equal to 134 dB (64 + 70). Both thermal and quantization noise contribute to this number.

The SNR of the input is assumed to be limited by the thermal noise of the input resistance, or –174 dBm/Hz. The input signal level is +10 dBm (2 V p-p into 50 Ω). Noise figure of the ADC can be calculated by:

$$NF = SNR\ (in) - SNR\ (out) = [+10 - (174)] - 134 = 50\ dB$$

Most ADCs detect input voltage levels, not power. Consequently, the input SNR can be determined more accurately by determining the ratio of the signal voltage to the noise voltage of the terminating resistor. However, both the input signal and noise voltage delivered to the ADC are also a function of the source impedance. The dependence of NF on sample rate, linearity, source and terminating impedances, and the number of assumptions that are required highlight the weakness of using NF as a figure of merit for an ADC. The rather large number that results bolsters this belief by indicating the ADC is often the weakest link in the signal processing path.

Linearity

The Third Order intercept point for a linear device (with some nonlinearity) is a good way to predict 3rd order spurious signals as a function of input signal level. For an ADC, however, this in an invalid concept except with signals near full scale. As the input signal is reduced, the performance burden shifts from the input track-and-hold (T/H) to the encoder. This creates a nonlinear function, as contrasted with the third order intercept behavior, which predicts an improvement in dynamic range as the signal level is decreased.

For signals near full scale, the intercept point is calculated the same as any device:

$$Intercept\ Point = [Harmonic\ Suppression/(N-1)] + Input\ Power$$

where N = the order of the IMD (3 in this case)

$$AD9022\ Intercept\ Point = 80/2 + 3\ dBm\ (7\ dBm\ below\ full\ scale)$$
$$= 43\ dBm$$

For signals below this level, the spurious free dynamic range (SFDR) curves shown in the data sheet are a more accurate predictor of dynamic range. The SFDR curve is generated by measuring the ratio of the signal (either tone in the two-tone measurement) to the worst spurious signal which is observed as the analog input signal amplitude is swept.

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The worst spurious signal is usually the second harmonic or 3rd order IMD. Actual results are shown on several plots. The straightline with a slope of one is constructed at the point where the worst SFDR touches the line. This line, extrapolated to full scale, gives the SFDR of the ADC. This value can then be used to predict the dynamic range by simply subtracting the input level from the SFDR. As shown on the two-tone SFDR plot, for example, a signal 20 dB below full scale will always have a dynamic range of at least 67 dB (87 dB – 20 dB).

It should be noted that all SFDR lines are constructed to be valid only below a certain level below full scale. Above these points, the linearity of the device is dominated by the nonlinearities of the front end and best predicted by the intercept point.

AD9022 NOISE PERFORMANCE

High speed, wide bandwidth ADCs such as the AD9022 are optimized for dynamic performance over a wide range of analog input frequencies. However, there are many applications (Imaging, Instrumentation, etc.) where dc precision is also important. Due to the wide input bandwidth of the AD9022 for a given input voltage, there will be a range of output codes which may occur. This is caused by unavoidable circuit noise within the wideband circuits in the ADC. If a dc signal is applied to the ADC and several thousand outputs are recorded, a distribution of codes such as that shown in the histogram below may result.

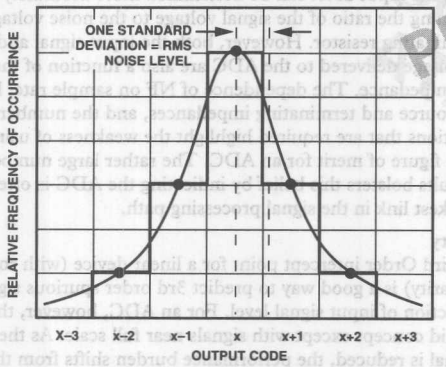

Figure 2. ADC Equivalent Input Noise

The correct code appears most of the time, but adjacent codes also appear with reduced probability. If a normal probability density curve is fitted to this Gaussian distribution of codes, the standard deviation will be equal to the equivalent input rms noise of the ADC. The rms noise may also be approximated by converting the SNR, as measured by a low frequency FFT, to an equivalent input noise. This method is accurate only if the SNR performance is dominated by random thermal noise (the low frequency SNR without harmonics is the best measure). Sixty-three dB equates to 1 LSB rms for a 2 V p-p (0.707 V rms) input signal. The AD9022 has approximately 0.5 LSB of rms noise or a noise limited SNR of 69 dB, indicating that noise alone does not limit the SNR performance of the device (quantization noise and linearity are also major contributors).

This thermal noise may come from several sources. The drive source impedance should be kept low to minimize resistor thermal noise. Some of the internal ADC noise is generated in the wideband T/H. Sampling ADCs generally have input bandwidths which exceed the Nyquist frequency of one-half the sampling rate. (The AD9022 has an input bandwidth of over 100 MHz, even though the sampling rate is limited to 20 Msps.)

Wide bandwidth is required to minimize gain and phase distortion and to permit adequate settling times in the internal amplifiers and T/Hs. But a certain amount of unavoidable noise is generated in the T/H and other wideband circuits within the ADC; this causes variation in output codes for dc inputs. Good layout, grounding, and decoupling techniques are essential to prevent external noise from coupling into the ADC and further corrupting performance.

USING THE AD9022

Layout Information

Preserving the accuracy and dynamic performance of the AD9022 requires that designers pay special attention to the layout of the printed circuit board.

Analog paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input connection should be kept away from digital signals paths; this reduces the amount of digital switching noise which is capacitively coupled into the analog section. Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch. The AD9022 digital outputs should be buffered or latched close to the device (<2 cm). This prevents load transients which may feed back into the device.

In high speed circuits, layout of the ground is critical. A single, low impedance ground plane on the component side of the board is recommended. Power supplies should be capacitively coupled to the ground plane with high quality 0.1 µF chip capacitors to reduce noise in the circuit. All power pins of the AD9022 should be bypassed individually. The compensation pin (COMP Pin 17) should be bypassed directly to the $-V_S$ supply (Pin 15) as close to the part as possible using a 0.1 µF chip capacitor.

Multilayer boards allow designers to lay out signal traces without interrupting the ground plane, and provide low impedance ground planes. In systems with dedicated analog and digital grounds, all grounds for the AD9022 should be connected to the analog ground plane.

In systems using multilayer boards, dedicated power planes are recommended to provide low impedance connections for device power. Sockets limit dynamic performance and are not recommended for use with the AD9022.

Timing

Conversion by the AD9022 is initiated by the rising edge of the ENCODE clock (Pin 8). All required timing is generated internal to the ADC. Care should be taken to ensure that the encode clock to the AD9022 is free from jitter that can degrade dynamic performance. The clock driver should be compatible with TTL LS logic series devices. Drivers with excessive slew rate or overdrive will degrade the dynamic performance of the AD9022.

PRELIMINARY TECHNICAL DATA

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Pulse width of the ADC encode clock must be controlled to ensure the best possible performance. Dynamic performance is guaranteed with a clock pulse HIGH minimum of 25 ns. Operation with narrower pulses will degrade SNR and dynamic performance. From a system perspective, this is generally not a problem, because a simple inverter can be used to generate a suitable clock if the system clock is less than 25 ns wide.

The AD9022 provides latched data outputs. Data outputs are available two pipeline delays and one propagation delay after the rising edge of the encode clock (refer to the AD9022 Timing Diagram). The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9022; these transients can detract from the converter's dynamic performance.

Operation at encode rates less than 2 Msps is not recommended. The internal track-and-hold saturates, causing erroneous conversions. This T/H saturation precludes clocking the AD9022 in a burst mode.

The duty cycle of the encode clock for the AD9022 is critical for obtaining rated performance of the ADC. Internal pulse widths within the track-and-hold are established by the encode command pulse width; to ensure rated performance, minimum and maximum pulse width restrictions should be observed. Operation at 20 Msps is optimized when the duty cycle is held at 50%. Duty cycle variations of less than ±5% will cause no degradation in performance at 20 Msps.

Analog Input
The analog input (Pin 12) voltage range is nominally ±1.024 volts. The range is set with an internal voltage reference and cannot be adjusted by the user. The input resistance is 300 Ω and the analog bandwidth is 100 MHz, making the AD9022 useful in undersampling applications.

The AD9022 should be driven from a low impedance source. The noise and distortion of the amplifier should be considered to preserve the dynamic range of the AD9022.

Power Supplies
The power supplies of the AD9022 should be isolated from the supplies used for noisy devices (digital logic especially) to reduce the amount of noise coupled into the ADC. For optimum performance, linear supplies ensure that switching noise from the supplies does not introduce distortion products during the encoding process. If switching supplies must be used, decoupling recommendations above are critically important. The PSRR of the AD9022 as a function of the ripple frequency present on the supplies is shown in the performance graphs. Clearly, power supplies with the lowest possible frequency should be selected.

AD9022 EVALUATION BOARD
The evaluation board for the AD9022 (AD9022/PCB) provides an easy and flexible method for evaluating the ADC's performance without (or prior to) developing a user-specific printed circuit board. The two-sided board includes a reconstruction DAC and digital output interface; and uses the layout and applications suggestions outlined above. It is available from Analog Devices at nominal cost.

Generous space is provided near the analog input and digital outputs to support additional signal processing components the user may wish to add. This prototyping area includes through holes with 100 mil centers to support a variety of component additions.

Input/Output/Supply Information
Power supply, analog input, clock connections, and reconstructed output (RC OUTPUT) are identified by labels on the evaluation board.

Operation of the evaluation board will conform to the following characteristics:

Parameter	Typical	Units
Supply Current		
+5 V	150	mA
–5 V	300	mA
A_{IN}		
Impedance	51	Ω
Voltage Range	±1.024	V
CLOCK		
Impedance	51	Ω
Frequency	20	Msps
RC OUTPUT		
Impedance	51	Ω
Voltage Range	0 to –1	V

Analog Input
Analog input signals can be fed directly into the device under test input (A_{IN}). The A_{IN} input is terminated at the device with a 62 Ω resistor to give a parallel equivalent of 51 Ω (62 Ω‖300 Ω).

DAC Reconstruction
The AD9022 evaluation board provides an on-board AD9713B reconstruction DAC for observing the digitized analog input signal. The AD9713B is terminated into 51 Ω to provide a 1 V p-p signal at the output (RC Output).

Output Data
The output data bits are latched with two 74LS574 latches which drive a 40-pin connector (AMP p/n 102153-09). The data and clock signals are available at the connector per the pin assignments shown on the schematic of the evaluation board. Data is latched on the rising edge of the encode clock.

PRELIMINARY TECHNICAL DATA

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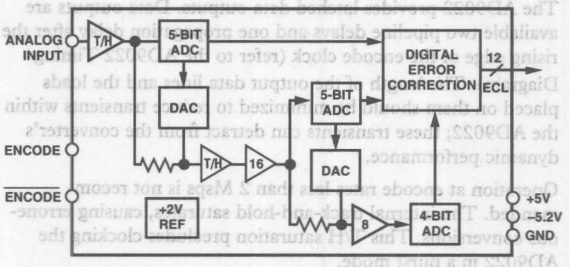
12-Bit 20 MSPS Monolithic A/D Converter

AD9023

FEATURES
Monolithic
12-Bit 20 MSPS A/D Converter
Low Power Dissipation: 1.3 Watts
On-Chip T/H and Reference
High-Spurii Free Dynamic Range
ECL Logic

APPLICATIONS
Radar Receivers
Digital Communications
Digital Instrumentation
Electro-Optic
Medical Imaging
Digital Filters

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9023 is a high speed, high performance, monolithic 12-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference, are included on chip to provide a complete conversion solution. It is a companion unit to the AD9023; the primary difference between the two is that all logic for the AD9022 is TTL compatible, while the AD9023 utilizes ECL logic for digital inputs and outputs. Pinouts for the two parts are nearly identical.

Operating from +5 V and –5.2 V supplies, the AD9023 provides excellent dynamic performance. Sampling at 20 Msps with A_{IN} = 1 MHz, the spurious free dynamic range (SFDR) is typically 80 dB; with A_{IN} = 9.6 MHz, SFDR is 74 dB. SNR is typically 65 dB.

The on-board T/H has a 100 MHz bandwidth and, more importantly, is designed to provide excellent dynamic performance for analog input frequencies above Nyquist. This feature is necessary in many undersampling signal processing applications, such as in direct IF to digital conversion.

To maintain dynamic performance at higher IFs, monolithic RF track-and-holds (such as the AD9100 and AD9101 Samplifier™) can be used with the AD9023 to process signals up to and beyond 70 MHz.

Samplifier is a trademark of Analog Devices, Inc.

With DNL typically less than 0.5 LSB and 20 ns transient response settling time, the AD9023 provides excellent results when low frequency analog inputs must be over-sampled (such as CCD digitization). The full-scale analog input is ±1 V with a 300 Ω input impedance. The analog input can be driven directly from the signal source, or can be buffered by the AD96xx series of low noise, low distortion buffer amplifiers.

All timing is internal to the AD9023; the clock signal initiates the conversion cycle. For best results, the encode command should contain as little jitter as possible. High speed layout practices must be followed to ensure optimum A/D performance.

The AD9023 is built on a trench isolated bipolar process and utilizes an innovative multipass architecture (see the block diagram). The unit is packaged in 28-pin ceramic DIPs and gullwing surface mount packages. The AD9023 is specified to operate over the industrial (–25°C to +85°C) and extended (–55°C to +125°C) temperature ranges.

PRELIMINARY DATA

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S = +5$ V; $-V_S = -5.2$ V; Encode = 20 MSPS, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9023AQ/AZ Min	Typ	Max	AD9023BQ/BZ Min	Typ	Max	AD9023SQ/SZ Min	Typ	Max	Units
RESOLUTION			12			12			12			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		0.4	0.75		0.25	0.5		0.4	0.75	LSB
	Full	VI			1.0			0.75			1.0	LSB
Integral Nonlinearity	+25°C	I		1.2	2.5		1.2	2.0		1.2	2.5	LSB
	Full	VI		1.25	3.0		1.25	3.0		1.25	3.0	LSB
No Missing Codes	Full	VI	Guaranteed			Guaranteed			Guaranteed			
Offset Error	+25°C	I		5	25		5	25		5	25	mV
	Full	VI		15	35		15	35		15	35	mV
Gain Error	+25°C	I		±0.5	±2.5		±0.5	±2.5		±0.5	±2.5	% FS
	Full	VI		0.5	3.5		0.5	3.5		0.5	3.5	% FS
Thermal Noise	+25°C	V		0.5			0.5			0.5		LSB, rms
ANALOG INPUT												
Input Voltage Range				±1.024			±1.024			±1.024		V
Input Resistance	Full	IV	250	300	375	250	300	375	250	300	375	Ω
Input Capacitance	+25°C	V		7			7			7		pF
Analog Bandwidth	+25°C	IV		115			115			115		MHz
SWITCHING PERFORMANCE[1]												
Minimum Conversion Rate	+25°C	IV			2			2			2	Msps
Maximum Conversion Rate	Full	VI	20			20			20			Msps
Aperture Delay (t_A)	+25°C	IV	0.82	1.12	1.42	0.82	1.12	1.42	0.82	1.12	1.42	ns
Aperture Uncertainty (Jitter)	+25°C	IV										ps, rms
Output Delay (t_{OD})	Full	IV	14.5		33.5	14.5		33.5	14.5		33.5	ns
ENCODE INPUT												
Logic Compatibility				ECL			ECL			ECL		
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8			0.8	V
Logic "1" Current	Full	VI		150			150			150		µA
Logic "0" Current	Full	VI		150			150			150		µA
Input Capacitance	+25°C	V		4			4			4		pF
Pulse Width (High)	+25°C	IV	25		250	25		250	25		250	ns
Pulse Width (Low)	+25°C	IV	17.5		250	17.5		250	17.5		250	ns
DYNAMIC PERFORMANCE												
Transient Response	+25°C	V		20			20			20		ns
Overvoltage Recovery Time	+25°C	V		20			20			20		ns
Harmonic Distortion												
Analog Input @ 1.2 MHz	+25°C	I	65	73		70	75		65	73		dBc
@ 1.2 MHz	Full	VI	65	70		70	75		65	70		dBc
@ 4.3 MHz	+25°C	V		75			75			75		dBc
@ 9.6 MHz	+25°C	I	63	74		70	74		63	74		dBc
@ 9.6 MHz	Full	VI	61	70		70	72		61	70		dBc
Signal-to-Noise Ratio[2]												
Analog Input @ 1.2 MHz	+25°C	I	62	65		65	67		62	65		dB
@ 1.2 MHz	Full	VI	61	64		64	66		61	64		dB
@ 4.3 MHz	+25°C	V		65			65			65		dB
@ 9.6 MHz	+25°C	I	61	64		64	66		61	64		dB
@ 9.6 MHz	Full	VI	60	63		63	65		60	63		dB
Signal-to-Noise Ratio[2] (Without Harmonics)												
Analog Input @ 1.2 MHz	+25°C	I	65	66		66	67		65	66		dB
@ 1.2 MHz	Full	VI	63	64		65	66		63	64		dB
@ 4.3 MHz	+25°C	V		66			66			66		dB
@ 9.6 MHz	+25°C	I	62	65		65	66		62	65		dB
@ 9.6 MHz	Full	VI	60	63		64	65		60	63		dB

PRELIMINARY TECHNICAL DATA

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Parameter (Conditions)	Temp	Test Level	AD9023AQ/AZ Min	Typ	Max	AD9023BQ/BZ Min	Typ	Max	AD9023SQ/SZ Min	Typ	Max	Units
DYNAMIC PERFORMANCE												
Transient Response	+25°C											V ns
Overvoltage Recovery Time	+25°C											V ns
Harmonic Distortion												
Analog Input @ 1.2 MHz	+25°C	I	65	73		70	75		65	73		dBc
@ 1.2 MHz	Full	VI	65	70		70	75		65	70		dBc
@ 4.3 MHz	+25°C	V		75			75			75		dBc
@ 9.6 MHz	+25°C	I	63	74		70	74		63	74		dBc
@ 9.6 MHz	Full	VI	61	70		70	72		61	70		dBc
Signal-to-Noise Ratio[2]												
Analog Input @ 1.2 MHz	+25°C	I	62	65		65	67		62	65		dB
@ 1.2 MHz	Full	VI	61	64		64	66		61	64		dB
@ 4.3 MHz	+25°C	V		65			65			65		dB
@ 9.6 MHz	+25°C	I	61	64		64	66		61	64		dB
@ 9.6 MHz	Full	VI	60	63		63	65		60	63		dB
Signal-to-Noise Ratio[2] (Without Harmonics)												
Analog Input @ 1.2 MHz	+25°C	I	65	66		66	67		65	66		dB
@ 1.2 MHz	Full	VI	63	64		65	66		63	64		dB
@ 4.3 MHz	+25°C	V		66			66			66		dB
@ 9.6 MHz	+25°C	I	62	65		65	66		62	65		dB
@ 9.6 MHz	Full	VI	60	63		64	65		60	63		dB
Two-Tone Intermodulation Distortion Rejection[3]	+25°C	V	76			76				76		dBc
DIGITAL OUTPUTS[1]												
Logic Compatibility				ECL			ECL			ECL		
Logic "1" Voltage	Full	VI	2.4			2.4			2.4			V
Logic "0" Voltage	Full	VI			0.5			0.5			0.5	V
Output Coding				Offset Binary			Offset Binary			Offset Binary		
POWER SUPPLY												
$+V_S$ Supply Voltage	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	mA
$+V_S$ Supply Current	Full	VI		100	120		100	120		100	120	mA
$-V_S$ Supply Voltage	Full	VI	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	mA
$-V_S$ Supply Current	Full	VI		160	190		160	190		160	190	mA
Power Dissipation	Full	VI		1.3	1.6		1.3	1.6		1.3	1.6	W
Power Supply Rejection Ratio (PSRR)[4]	Full	IV		28			28			28		mV/V

NOTES
[1]AD9023 load is a single LS latch.
[2]RMS signal-to-rms noise with analog input signal 1 dB below full scale at specified frequency.
[3]Intermodulation measured with analog input frequencies of 9.3 MHz and 9.6 MHz at 7 dB below full scale.
[4]PSRR is sensitivity of offset error to power supply variations within the 5% limits shown.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ ..... +6 V
$-V_S$ ..... –6 V
Analog Input ..... $-V_S$ to $+V_S$
Digital Inputs ..... $-V_S$ to 0 V
Digital Output Current ..... 20 mA
Gain Adjust ..... $-V_S$ to $+V_S$
Offset Adjust ..... $-V_S$ to $+V_S$
Operating Temperature Range (Case)
AD9023AQ/AZ/BQ/BZ ..... –25°C to +85°C
AD9023SQ/SZ/TQ/TZ ..... –55°C to +125°C
Maximum Junction Temperature[2] ..... +175°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Storage Temperature Range ..... –65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: "Q" Package (Ceramic DIP): θ_{JC} = 10°C/W; θ_{JA} = 35°C/W. "Z" Package (Gullwing Surface Mount): θ_{JC} = 13°C/W; θ_{JA} = 45°C/W.

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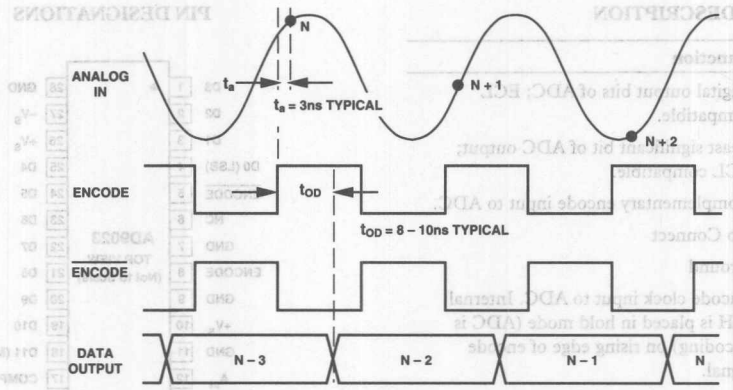


Timing Diagram

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9023AQ/BQ	–25°C to +85°C	28-Pin Ceramic DIP	Q-28
AD9023AZ/BZ	–25°C to +85°C	28-Pin Ceramic Leaded Chip Carrier	Z-28
AD9032SQ	–55°C to +125°C	28-Pin Ceramic DIP	Q-28
AD9023SZ	–55°C to +125°C	28-Pin Ceramic Leaded Chip Carrier	Z-28

*For outline information see Package Information section.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III – Sample tested only.

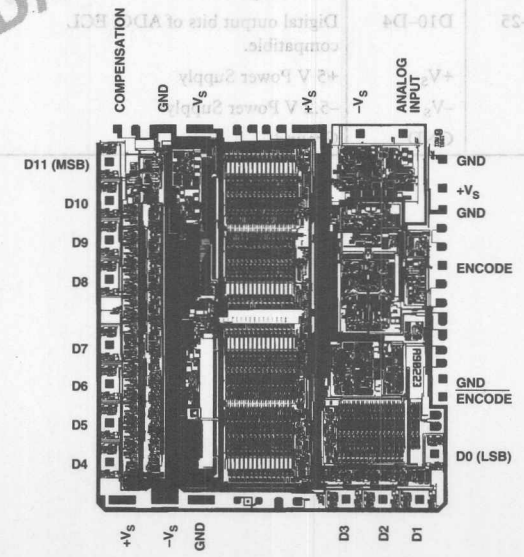
IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C; guaranteed by design and characterization testing at temperature extremes for industrial devices.

DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions	205 × 228 × 21 (±1) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Transistor Count	4,128
Passivation	Oxynitride
Die Attach	Silver Glass
Bond Wire	Aluminum



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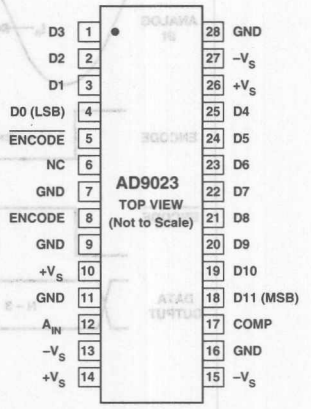
PIN DESCRIPTION

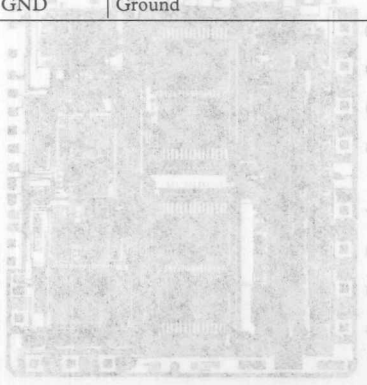
Pin No.	Name	Function
1–3	D3–D1	Digital output bits of ADC; ECL compatible.
4	D0 (LSB)	Least significant bit of ADC output; ECL compatible.
5	$\overline{\text{ENCODE}}$	Complementary encode input to ADC.
6	NC	No Connect
7	GND	Ground
8	ENCODE	Encode clock input to ADC. Internal T/H is placed in hold mode (ADC is encoding) on rising edge of encode signal.
9	GND	Ground
10	$+V_S$	+5 V Power Supply
11	GND	Ground
12	A_{IN}	Noninverting input to T/H amplifier.
13	$-V_S$	–5.2 V Power Supply
14	$+V_S$	+5 V Power Supply
15	$-V_S$	–5.2 V Power Supply
16	GND	Ground
17	COMP	Should be connected to $-V_S$ through 0.1 μF capacitor.
18	D11 (MSB)	Most significant bit of ADC output; ECL compatible.
19–25	D10–D4	Digital output bits of ADC; ECL compatible.
26	$+V_S$	+5 V Power Supply
27	$-V_S$	–5.2 V Power Supply
28	GND	Ground

PIN DESIGNATIONS



NC = NO CONNECT
COMPENSATION (PIN 17) SHOULD BE CONNECTED TO $-V_S$ THROUGH 0.01μF

PRELIMINARY TECHNICAL DATA



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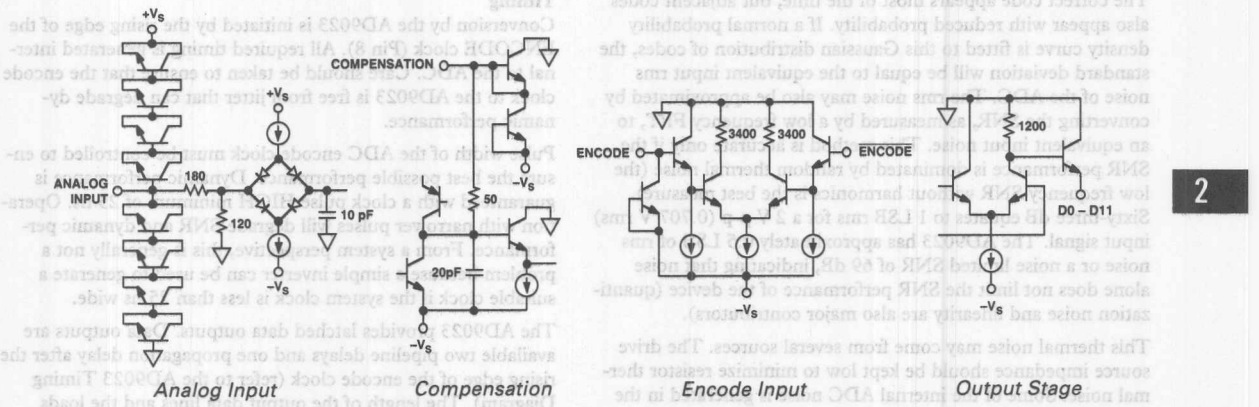

Figure 1. Equivalent Circuits

THEORY OF OPERATION

Refer to the block diagram. The AD9023 employs a three pass subranging architecture and digital error correction. This combination of design techniques insures 12-bit accuracy at relatively low power.

Analog input signals are immediately attenuated through a resistor divider and applied directly to the sampling bridge of the track-and-hold (T/H). The T/H holds whatever analog value is present when the unit is strobed with an ENCODE command. The conversion process begins on the rising edge of this pulse, which should conform to the minimum and maximum pulse width requirements shown in the specifications. Operation below the recommended encode rate (2 Msps) may result in excessive droop in the internal T/H devices–leading to large dc and ac errors.

The held analog value of the first track-and-hold is applied to a 5-bit flash converter and a second T/H. The 5-bit flash converter resolves the most significant bits (MSBs) of the held analog voltage. These 5 bits are reconstructed via a 5-bit DAC and subtracted from the original T/H output signal to form a residue signal.

A second T/H holds the amplified residue signal while it is encoded with a second 5-bit flash ADC. Again the 5 bits are reconstructed and subtracted from the second T/H output to form a residue signal. This residue is amplified and encoded with a 4-bit flash ADC to provide the 3 least significant bits (LSBs) of the digital output and one bit of error correction.

Digital Error Correction logic aligns the data from the three flash converters and presents the result as a 12-bit parallel digital word. The output stage of the AD9023 is TTL. Output data may be strobed on the rising edge of the ENCODE command.

AD9023 Noise Performance

High speed, wide bandwidth ADCs such as the AD9023 are optimized for dynamic performance over a wide range of analog input frequencies. However, there are many applications (Imaging, Instrumentation, etc.) where dc precision is also important. Due to the wide input bandwidth of the AD9023 for a given input voltage, there will be a range of output codes which may occur. This is caused by unavoidable circuit noise within the wideband circuits in the ADC. If a dc signal is applied to the ADC and several thousand outputs are recorded, a distribution of codes such as that shown in the histogram below may result.

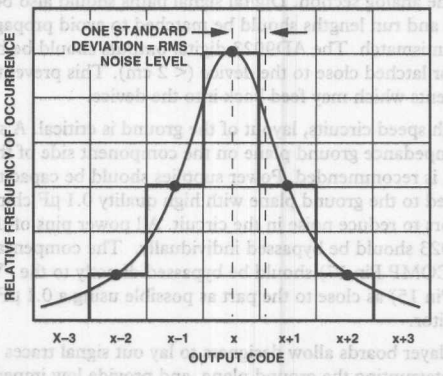

Figure 2. Equivalent Input Noise

PRELIMINARY TECHNICAL DATA

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The correct code appears most of the time, but adjacent codes also appear with reduced probability. If a normal probability density curve is fitted to this Gaussian distribution of codes, the standard deviation will be equal to the equivalent input rms noise of the ADC. The rms noise may also be approximated by converting the SNR, as measured by a low frequency FFT, to an equivalent input noise. This method is accurate only if the SNR performance is dominated by random thermal noise (the low frequency SNR without harmonics is the best measure). Sixty-three dB equates to 1 LSB rms for a 2 V p-p (0.707 V rms) input signal. The AD9023 has approximately 0.5 LSB of rms noise or a noise limited SNR of 69 dB, indicating that noise alone does not limit the SNR performance of the device (quantization noise and linearity are also major contributors).

This thermal noise may come from several sources. The drive source impedance should be kept low to minimize resistor thermal noise. Some of the internal ADC noise is generated in the wideband T/H. Sampling ADCs generally have input bandwidths which exceed the Nyquist frequency of one-half the sampling rate. (The AD9023 has an input bandwidth of over 100 MHz, even though the sampling rate is limited to 20 Msps.)

USING THE AD9023

Layout Information

Preserving the accuracy and dynamic performance of the AD9023 requires that designers pay special attention to the layout of the printed circuit board.

Analog paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input connection should be kept away from digital signals paths; this reduces the amount of digital switching noise which is capacitively coupled into the analog section. Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch. The AD9023 digital outputs should be buffered or latched close to the device (< 2 cm). This prevents load transients which may feed back into the device.

In high speed circuits, layout of the ground is critical. A single, low impedance ground plane on the component side of the board is recommended. Power supplies should be capacitively coupled to the ground plane with high quality 0.1 µF chip capacitors to reduce noise in the circuit. All power pins of the AD9023 should be bypassed individually. The compensation pin (COMP Pin 17) should be bypassed directly to the $-V_S$ supply (Pin 15) as close to the part as possible using a 0.1 µF chip capacitor.

Multilayer boards allow designers to lay out signal traces without interrupting the ground plane, and provide low impedance ground planes. In systems with dedicated analog and digital grounds, all grounds for the AD9023 should be connected to the analog ground plane.

In systems using multilayer boards, dedicated power planes are recommended to provide low impedance connections for device power. Sockets limit dynamic performance and are not recommended for use with the AD9023.

Timing

Conversion by the AD9023 is initiated by the rising edge of the ENCODE clock (Pin 8). All required timing is generated internal to the ADC. Care should be taken to ensure that the encode clock to the AD9023 is free from jitter that can degrade dynamic performance.

Pulse width of the ADC encode clock must be controlled to ensure the best possible performance. Dynamic performance is guaranteed with a clock pulse HIGH minimum of 25 ns. Operation with narrower pulses will degrade SNR and dynamic performance. From a system perspective, this is generally not a problem because a simple inverter can be used to generate a suitable clock if the system clock is less than 25 ns wide.

The AD9023 provides latched data outputs. Data outputs are available two pipeline delays and one propagation delay after the rising edge of the encode clock (refer to the AD9023 Timing Diagram). The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9023; these transients can detract from the converter's dynamic performance. Operation at encode rates less than 2 Msps is not recommended. The internal track-and-hold saturates, causing erroneous conversions. This T/H saturation precludes clocking the AD9023 in a burst mode.

The duty cycle of the encode clock for the AD9023 is critical for obtaining rated performance of the ADC. Internal pulse widths within the track-and-hold are established by the encode command pulse width; to ensure rated performance, minimum and maximum pulse width restrictions should be observed. Operation at 20 Msps is optimized when the duty cycle is held at 50%. Duty cycle variations of less than ±5% will cause no degradation in performance at 20 Msps.

Analog Input

The analog input (Pin 12) voltage range is nominally ±1.024 volts. The range is set with an internal voltage reference and cannot be adjusted by the user. The input resistance is 300 Ω and the analog bandwidth is 100 MHz, making the AD9023 useful in undersampling applications.

The AD9023 should be driven from a low impedance source. The noise and distortion of the amplifier should be considered to preserve the dynamic range of the AD9023.

Power Supplies

The power supplies of the AD9023 should be isolated from the supplies used for noisy devices (digital logic especially) to reduce the amount of noise coupled into the ADC. For optimum performance, linear supplies ensure that switching noise from the supplies does not introduce distortion products during the encoding process. If switching supplies must be used, decoupling recommendations above are critically important. The PSRR of the AD9023 as a function of the ripple frequency present on the supplies is shown in the performance graphs. Clearly, power supplies with the lowest possible frequency should be selected.

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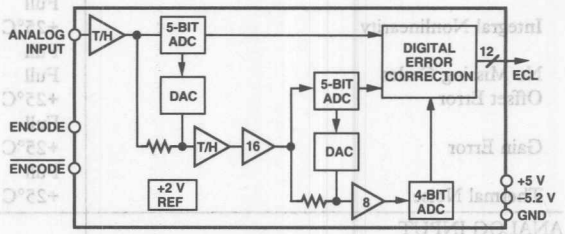
12-Bit, 31 MSPS Monolithic A/D Converter

AD9027

FEATURES
- 12-Bit 31 MSPS A/D Converter
- Low Power Dissipation: 1.5 Watts
- On-Chip T/H and Reference
- Wide Spurious-Free Dynamic Range
- ECL Logic

APPLICATIONS
- Cellular Base Stations
- Communications Receivers
- Radar Receivers
- Spectrum Analyzers
- Electro-Optics
- Medical Imaging

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD9027 is a high speed, high performance, monolithic 12-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference, are included on chip to provide a complete conversion solution.

It is a companion unit to the AD9026; the primary difference between the two is that all logic for the AD9026 is TTL compatible, while the AD9027 utilizes ECL logic for digital inputs and outputs. Pinouts for the two parts are nearly identical.

The on-board T/H has a 200 MHz bandwidth and, more importantly, is designed to provide excellent dynamic performance for analog input frequencies above Nyquist. This feature is necessary in many undersampling signal processing applications, such as in direct IF-to-digital conversion. In addition, wide spurious-free dynamic range (SFDR) over the entire Nyquist bandwidth makes the AD9027 well suited for multichannel transceiver applications which need to digitize bandwidths up to 15 MHz.

All timing is internal to the AD9027; the clock signal initiates the conversion cycle. For best results, the encode command should contain as little jitter as possible. High speed layout practices must be followed to ensure optimum A/D performance.

The AD9027 is built on a trench isolated bipolar process and utilizes an innovative multipass architecture (see the block diagram). The unit is packaged in a 28-pin ceramic DIP; the custom cofired ceramic package forms a multilayer substrate to which are attached internal bypass capacitors and the AD9027 die. The AD9027 is specified to operate over the industrial (–25°C to +85°C) temperature range.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

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Parameter (Conditions)	Temp	Test Level	AD9027AD Min	Typ	Max	Units
RESOLUTION		12				Bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		0.4	0.75	LSB
	Full	VI			1.0	LSB
Integral Nonlinearity	+25°C	I		1.2	2.5	LSB
	Full	VI		1.25	3.0	LSB
No Missing Codes	Full	VI		Guaranteed		
Offset Error	+25°C	I		5	25	mV
	Full	VI		15	35	mV
Gain Error	+25°C	I		±0.5	±2.5	% FS
	Full	VI		0.5	3.5	% FS
Thermal Noise	+25°C	V		0.7		LSB, rms
ANALOG INPUT						
Input Voltage Range				±1.024		V
Input Resistance	Full	IV	250	300	375	Ω
Input Capacitance	+25°C	V		7		pF
Analog Bandwidth	+25°C	IV		200		MHz
SWITCHING PERFORMANCE[1]						
Conversion Rate	+25°C	I	4		31	Msps
Aperture Delay (t_A)	+25°C	V		3		ns
Aperture Uncertainty (Jitter)	+25°C	V		TBD		ps, rms
Output Delay (t_{OD})	Full	IV	TBD		TBD	ns
ENCODE INPUT						
Logic Compatibility				Differential ECL		
Logic "1" Voltage	Full	VI	−1.1			V
Logic "0" Voltage	Full	VI			−1.5	V
Logic "1" Current	Full	VI		5		µA
Logic "0" Current	Full	VI		5		µA
Input Capacitance	+25°C	V		4		pF
Pulse Width (High)	+25°C	IV	TBD		TBD	ns
Pulse Width (Low)	+25°C	IV	TBD		TBD	ns
DYNAMIC PERFORMANCE						
Transient Response	+25°C	V				ns
Overvoltage Recovery Time	+25°C	V				ns
Harmonic Distortion[2]						
Analog Input @ 1.2 MHz	+25°C	I		73		dBc
@ 1.2 MHz	Full	VI		70		dBc
@ 9.6 MHz	+25°C	I		72		dBc
@ 13.4 MHz	+25°C	I		72		dBc
@ 13.4 MHz	Full	VI		70		dBc
Signal-to-Noise-and-Distortion[2] (SINAD)						
Analog Input @ 1.2 MHz	+25°C	I		65		dB
@ 1.2 MHz	Full	VI		64		dB
@ 9.6 MHz	+25°C	I		64		dB
@ 13.4 MHz	+25°C	I		63		dB
@ 13.4 MHz	Full	VI		62		dB
Signal-to-Noise Ratio[2] (SNR) (Without Harmonics)						
Analog Input @ 1.2 MHz	+25°C	I		66		dB
@ 1.2 MHz	Full	VI		65		dB
@ 9.6 MHz	+25°C	I		65		dB
@ 13.4 MHz	+25°C	I		64		dB
@ 13.4 MHz	Full	VI		63		dB
Two-Tone Intermodulation Distortion Rejection[3]	+25°C	V		75		dBc

PRELIMINARY TECHNICAL DATA

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Parameter (Conditions)	Test Temp	Level	AD9027AD Min	Typ	Max	Units
DIGITAL OUTPUTS[1]						
Logic Compatibility				ECL		
Logic "1" Voltage	Full	VI	–1.1			V
Logic "0" Voltage	Full	VI			–1.5	V
Output Coding				Offset Binary		
POWER SUPPLY						
$+V_S$ Supply Voltage	Full	VI	4.75	5.0	5.25	V
$+V_S$ Supply Current	Full	VI		112		mA
$-V_S$ Supply Voltage	Full	VI	5.45	–5.2	–4.95	V
$-V_S$ Supply Current	Full	VI		180		mA
Power Dissipation	Full	VI		1.5		W
Power Supply Rejection Ratio (PSRR)[4]	Full	IV		12		mV/V

NOTES
[1]AD9027 is terminated into 5.2 V through 2,000 ohms.
[2]Analog input signal is 1 dB below full scale at specified frequency.
[3]Intermodulation measured with analog input frequencies of 9.6 MHz and 11.3 MHz at 7 dB below full scale.
[4]PSRR is sensitivity of offset error to power supply variations within the 5% limits shown.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ . . . . . +6 V
$-V_S$ . . . . . –6 V
Analog Input . . . . . ±2.5 V
Digital Inputs . . . . . $-V_S$ to 0 V
Digital Output Current . . . . . 20 mA
Operating Temperature Range (Case) . . . . . –25°C to +85°C
Maximum Junction Temperature[2] . . . . . +175°
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Storage Temperature Range . . . . . –65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: "Q" Package (Ceramic DIP): θ_{JC} = x°C/W; θ_{JA} = x°C/W.

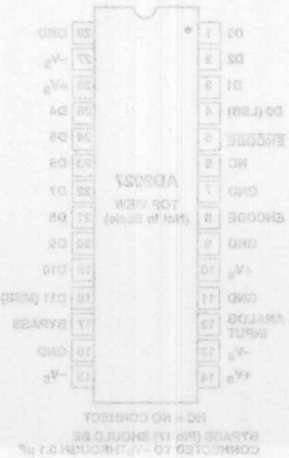
ORDERING GUIDE

Device	Temperature Range	Package Option*
AD9027AD	–25°C to +85°C	DH-28

*For outline information see Package Information section.

EXPLANATION OF TEST LEVELS

Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C; 100% production tested at temperature extremes for extended temperature devices; guaranteed by design and characterization testing for industrial devices.



PRELIMINARY TECHNICAL DATA

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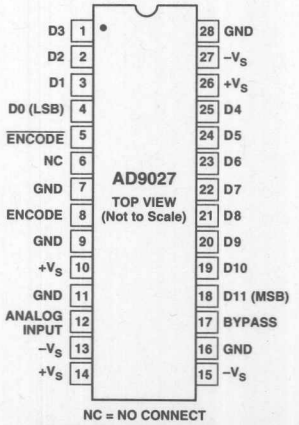
PIN DESCRIPTION

Pin No.	Name	Function
1–3	D3–D1	Digital output bits of ADC; ECL compatible.
4	D0 (LSB)	Least significant bit of ADC output; ECL compatible.
5	$\overline{\text{ENCODE}}$	Complement of encode clock input.
6	NC	No connection internally.
7	GND	Ground.
8	ENCODE	Encode clock input to ADC. Internal T/H is placed in hold mode (ADC is encoding) on rising edge of encode signal.
9	GND	Ground.
10	$+V_S$	+5 V power supply.
11	GND	Ground.
12	A_{IN}	Noninverting input to T/H amplifier.
13	$-V_S$	–5.2 V power supply.
14	$+V_S$	+5 V power supply.
15	$-V_S$	–5.2 V power supply.
16	GND	Ground.
17	BYPASS	Should be connected to $-V_S$ through 0.1 µF capacitor.
18	D11 (MSB)	Most significant bit of ADC output; ECL compatible.
19–25	D10–D4	Digital output bits of ADC; ECL compatible.
26	$+V_S$	+5 V power supply.
27	$-V_S$	–5.2 V power supply.
28	GND	Ground.

PIN DESIGNATIONS

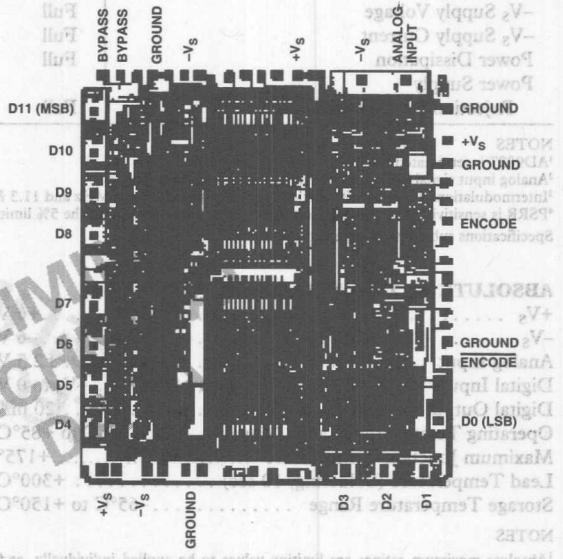


NC = NO CONNECT

BYPASS (Pin 17) SHOULD BE CONNECTED TO $-V_S$ THROUGH 0.1 µF

DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions	205 × 228 × 21 (±1) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Transistor Count	4,336
Passivation	Oxynitride
Die Attach	Silver Filled
Bond Wire	Gold



AD9027 Chip Pinouts

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DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Harmonic Distortion
The rms value of the fundamental divided by the rms value of the worst harmonic component.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency tested drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between the 50% point of the rising edge of the ENCODE command and the time when all output data bits are within valid logic levels.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 12-bit accuracy after an analog input signal 150% of full scale is reduced to midscale.

Power Supply Rejection Ratio (PSRR)
The ratio of a change in input offset voltage to a change in power supply voltage.

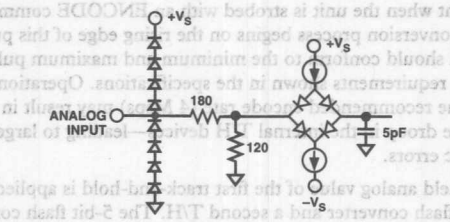
Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1 dB below full scale.

Signal-to-Noise Ratio (Without Harmonics)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, excluding the first five harmonics and dc, with an analog input signal 1 dB below full scale.

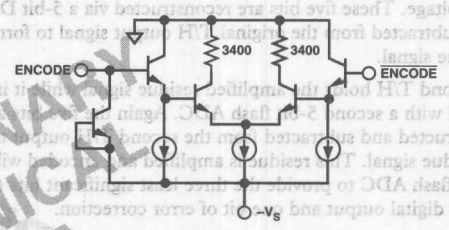
Transient Response
The time required for the converter to achieve 12-bit accuracy when a one-half full-scale step function is applied to the analog input.

Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of either of two input signals to the power of the strongest third-order IMD signal.

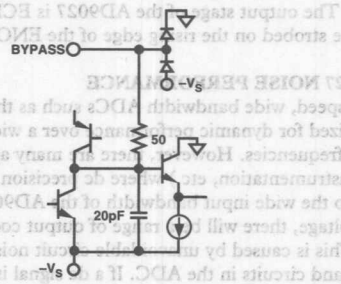
PRELIMINARY TECHNICAL DATA



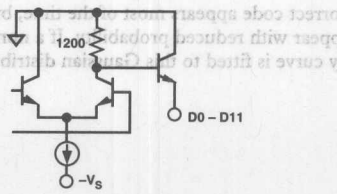
Analog Input



Encode Input



Bypass



Output Stage

Equivalent Circuits

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The AD9027 employs a three-pass subranging architecture and digital error correction. This combination of design techniques ensures 12-bit accuracy at relatively low power.

Analog input signals are immediately attenuated through a resistor divider and applied directly to the sampling bridge of the track-and-hold (T/H). The T/H holds whatever analog value is present when the unit is strobed with an ENCODE command. The conversion process begins on the rising edge of this pulse, which should conform to the minimum and maximum pulse width requirements shown in the specifications. Operation below the recommended encode rate (4 Msps) may result in excessive droop in the internal T/H devices—leading to large dc and ac errors.

The held analog value of the first track-and-hold is applied to a 5-bit flash converter and a second T/H. The 5-bit flash converter resolves the most significant bits (MSBs) of the held analog voltage. These five bits are reconstructed via a 5-bit DAC and subtracted from the original T/H output signal to form a residue signal.

A second T/H holds the amplified residue signal while it is encoded with a second 5-bit flash ADC. Again the five bits are reconstructed and subtracted from the second T/H output to form a residue signal. This residue is amplified and encoded with a 4-bit flash ADC to provide the three least significant bits (LSBs) of the digital output and one bit of error correction.

Digital error correction logic aligns the data from the three flash converters and presents the result as a 12-bit parallel digital word. The output stage of the AD9027 is ECL. Output data may be strobed on the rising edge of the ENCODE command.

AD9027 NOISE PERFORMANCE

High speed, wide bandwidth ADCs such as the AD9027 are optimized for dynamic performance over a wide range of analog input frequencies. However, there are many applications (imaging, instrumentation, etc.) where dc precision is also important. Due to the wide input bandwidth of the AD9027 for a given input voltage, there will be a range of output codes that may occur. This is caused by unavoidable circuit noise within the wideband circuits in the ADC. If a dc signal is applied to the ADC and several thousand outputs are recorded, a distribution of codes such as that shown in the histogram may result.

The correct code appears most of the time, but adjacent codes also appear with reduced probability. If a normal probability density curve is fitted to this Gaussian distribution of codes, the noise of the ADC. The rms noise may also be approximated by converting the SNR, as measured by a low frequency FFT, to an equivalent input noise. This method is accurate only if the SNR performance is dominated by random thermal noise (the low frequency SNR without harmonics is the best measure); 63 dB equates to 1 LSB rms for a 2 V p-p (0.707 V rms) input signal.

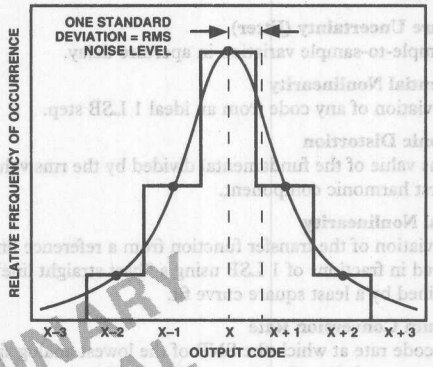

Figure 1. ADC Equivalent Input Noise

The AD9027 has approximately 0.7 LSB of rms noise or a noise limited SNR of 66 dB, indicating that thermal noise alone does not limit the SNR performance of the device (quantization noise and linearity are also major contributors).

This thermal noise may come from several sources. The drive source impedance should be kept low to minimize resistor thermal noise. Some of the internal ADC noise is generated in the wideband T/H. Sampling ADCs generally have input bandwidths which exceed the Nyquist frequency of one-half the sampling rate. (The AD9027 has an input bandwidth of approximately 200 MHz, even though the sampling rate is limited to 31 Msps.)

Wide bandwidth is required to minimize gain and phase distortion and to permit adequate settling times in the internal amplifiers and T/Hs. But a certain amount of unavoidable noise is generated in the T/H and other wideband circuits within the ADC; this causes variation in output codes for dc inputs. Good layout, grounding, and decoupling techniques are essential to prevent external noise from coupling into the ADC and further corrupting performance.

PRELIMINARY TECHNICAL DATA

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USING THE AD9027

Layout Information

Preserving the accuracy and dynamic performance of the AD9027 requires that designers pay special attention to the layout of the printed circuit board.

Analog paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input connection should be kept away from digital signals paths; this reduces the amount of digital switching noise which is capacitively coupled into the analog section. Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch. The AD9027 digital outputs should be buffered or latched close to the device (< 2 cm). This prevents load transients which may feed back into the device.

In high speed circuits, layout of the ground is critical. A single, low impedance ground plane on the component side of the board is recommended. Power supplies should be capacitively coupled to the ground plane with high quality 0.1 µF chip capacitors to reduce noise in the circuit. All power pins of the AD9027 should be bypassed individually. The bypass pin (BYPASS Pin 17) should be bypassed directly to the $-V_S$ supply (Pin 15) as close to the part as possible using a 0.1 µF chip capacitor.

Multilayer boards allow designers to lay out signal traces without interrupting the ground plane, and provide low impedance ground planes. In systems with dedicated analog and digital grounds, all grounds for the AD9027 should be connected to the analog ground plane.

In systems using multilayer boards, dedicated power planes are recommended to provide low impedance connections for device power. Sockets limit dynamic performance and are not recommended for use with the AD9027.

Timing

Conversion by the AD9027 is initiated by the rising edge of the ENCODE clock (Pin 8). All required timing is generated internal to the ADC. Care should be taken to ensure that the encode clock to the AD9027 is free from jitter that can degrade dynamic performance. The clock driver should be differential ECL. Drivers with excessive slew rate or overdrive will degrade the dynamic performance of the AD9027.

Pulse width of the ADC encode clock must be controlled to insure the best possible performance. The duty cycle of the encode clock for the AD9027 is critical for obtaining rated performance of the ADC. Internal pulse widths within the track-and-hold are established by the encode command pulse width; to ensure rated performance, minimum and maximum pulse width restrictions should be observed. Operation at 31 Msps is optimized when the duty cycle is held at 50%. Duty cycle variations of less than ±5% will cause no degradation in performance at 31 Msps.

The AD9027 provides latched data outputs. Data outputs are available two pipeline delays and one propagation delay after the rising edge of the encode clock (refer to the AD9027 Timing Diagram). The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9027; these transients can detract from the converter's dynamic performance.

Operation at encode rates less than 4 Msps is not recommended. The internal track-and-hold saturates, causing erroneous conversions. This T/H saturation precludes clocking the AD9027 in a burst mode.

Analog Input

The Analog Input (Pin 12) voltage range is nominally ±1.024 V. The range is set with an internal voltage reference and can not be adjusted by the user. The input resistance is 300 Ω and the analog bandwidth is 200 MHz, making the AD9027 useful in undersampling applications.

The AD9027 should be driven from a low impedance source. The noise and distortion of the amplifier should be considered to preserve the dynamic range of the AD9027.

Power Supplies

The power supplies of the AD9027 should be isolated from the supplies used for noisy devices (digital logic especially) to reduce the amount of noise coupled into the ADC. For optimum performance, linear supplies ensure that switching noise from the supplies does not introduce distortion products during the encoding process. If switching supplies *must* be used, decoupling recommendations above are critically important. The PSRR of the AD9027 as a function of the ripple frequency present on the supplies is shown in the performance graphs. Clearly, power supplies with the lowest possible frequency should be selected.

PRELIMINARY TECH DATA

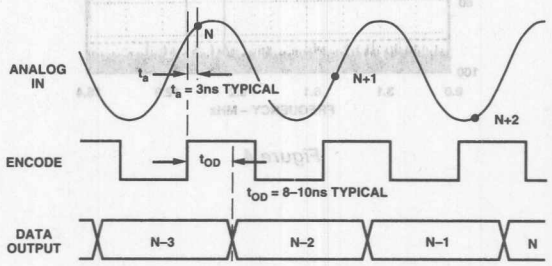

Figure 2. Timing Diagram

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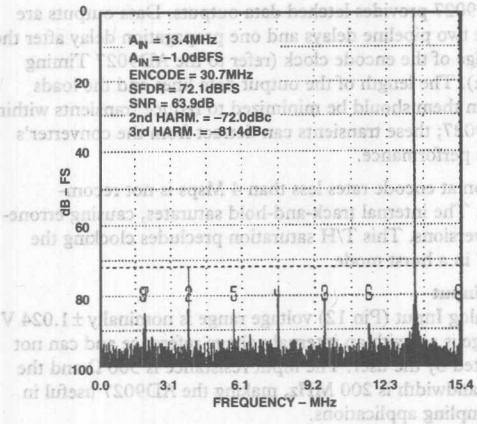

Figure 3.

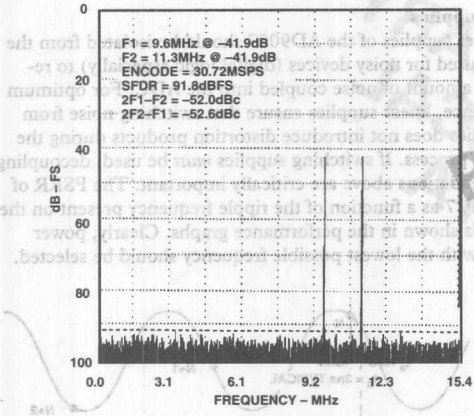

Figure 4.

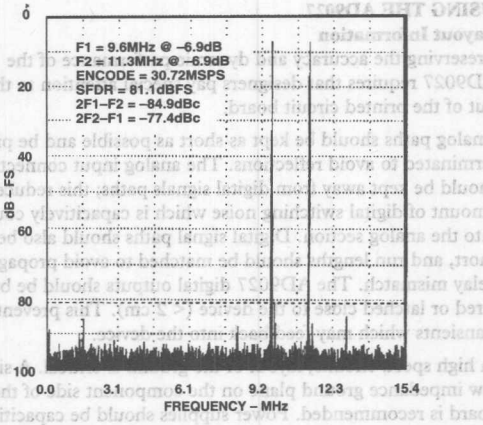

Figure 5.

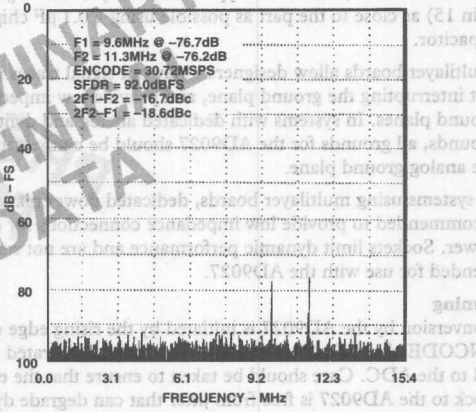

Figure 6.

PRELIMINARY TECHNICAL DATA

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12-Bit 25 MSPS A/D Converter

AD9032

2

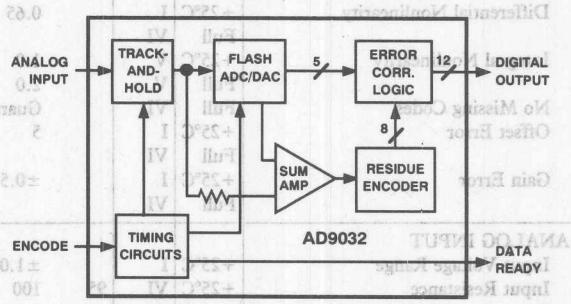
FEATURES

- 25.6 MSPS Conversion Speeds
- On-Board T/H, References, Timing
- Low Power: 3.8 W
- Single 40-Pin Package
- 74 dB Spurious-Free Dynamic Range to 12 MHz A_{IN}
- Bipolar Input: ±1.024 V

APPLICATIONS

- Radar
- Signal Intelligence
- Digital Spectrum Analyzers
- Medical Imaging
- Electro-Optics

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9032 is the world's fastest 12-bit analog-to-digital converter (ADC) that includes on-board T/H, voltage references, and timing circuits. The AD9032 uses a subranging converter architecture to achieve sample rates from dc to 25.6 Msps. Packaged in a single 40-pin hybrid, the AD9032 is pin-compatible with the AD9034, which operates at word rates up to 20 Msps.

This ECL-compatible ADC requires only +5 V and −5.2 V supplies, an analog input, and a stable ECL clock to obtain the best dynamic performance available in a 12-bit ADC. This kind of performance is achieved with advanced bipolar circuits, custom designed and manufactured by Analog Devices. The latest in monolithic track-and-hold technology ensures accurate sampling of high frequency analog inputs.

Dynamic performance has been optimized to achieve SNR of 64 dB and a spurious-free dynamic range (SFDR) of 74 dB for analog bandwidths up to 12 MHz. All units are tested for dynamic performance at a sample rate of 25.6 Msps.

The AD9032 is available in either a 40-pin ceramic DIP or leaded flatpack. The two versions operate over an industrial (−25°C to +85°C) or military (−55°C to +125°C) temperature range.

EVALUATION BOARD

An evaluation board which is available for the AD9032 (part number AD9034/PCB) provides an easy and flexible method for evaluating the ADC's performance without (or prior to) developing a user-specified printed circuit board. The evaluation board was originally designed and used for evaluating the AD9034 A/D converter, but is equally useful for the pin-compatible AD9032.

The board includes a reconstruction DAC, analog input amplifier, and digital output interface. Physically, it is 7.25 inches × 6 inches in size and uses the layout and applications information contained in the AD9034 data sheet.

Generous space is provided near the analog input and digital outputs of the evaluation board to support additional signal processing components the user may wish to add. These two prototyping areas include through holes with 100-mil centers to support a variety of component additions.

For additional operating details, a schematic of the evaluation board, and complete layout information, consult the data sheet on the AD9034 A/D converter.

AD9032–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = −5.2 V; Encode = 25.6 Msps, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9032AD/AZ Min	AD9032AD/AZ Typ	AD9032AD/AZ Max	AD9032BD/BZ Min	AD9032BD/BZ Typ	AD9032BD/BZ Max	AD9032TD/TZ Min	AD9032TD/TZ Typ	AD9032TD/TZ Max	Units
RESOLUTION			12			12			12			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		0.65	1.25		0.5	1.0		0.5	1.0	LSB
	Full	VI			1.75			1.5			1.5	LSB
Integral Nonlinearity	+25°C	V		1.0			1.0			1.0		LSB
	Full	V		2.0			2.0			2.0		LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed			Guaranteed		
Offset Error	+25°C	I		5	15		5	15		5	15	mV
	Full	VI			25			25			30	mV
Gain Error	+25°C	I		±0.5	±1.0		±0.5	±1.0		±0.5	±1.0	% FS
	Full	VI			±2.5			±2.5			±2.5	% FS
ANALOG INPUT												
Input Voltage Range	+25°C	I		±1.024			±1.024			±1.024		V
Input Resistance	+25°C	VI	95	100	105	95	100	105	95	100	105	Ω
Input Capacitance	+25°C	IV		7	10		7	10		7	10	pF
Analog Bandwidth	+25°C	IV	150	220		150	220		150	220		MHz
SWITCHING PERFORMANCE[1]												
Conversion Rate	Full	VI	dc		25.6	dc		25.6	dc		25.6	Msps
Aperture Delay (t_A)	Full	IV	1	3	5	1	3	5	1	3	5	ns
Aperture Uncertainty (jitter)	Full	IV		4	8		4	8		4	8	ps, rms
Output Delay (t_{OD})	Full	IV	9	13	17	9	13	17	9	13	17	ns
Data Ready Delay (t_{DR})	Full	IV	3.5	7.5	10.5	3.5	7.5	10.5	3.5	7.5	10.5	ns
Output Time Skew	Full	IV		1	2		1	2		1	2	ns
ENCODE INPUT												
Logic "1" Voltage	Full	IV	−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	IV			−1.5			−1.5			−1.5	V
Logic "1" Current	Full	VI		150	300		150	300		150	300	μA
Logic "0" Current	Full	VI		150	300		150	300		150	300	μA
Input Capacitance	+25°C	V		10			10			10		pF
Pulse Width (High)	+25°C	IV	10			10			10			ns
Pulse Width (Low)	+25°C	IV	10			10			10			ns
DYNAMIC PERFORMANCE												
Transient Response	+25°C	IV		12	27		12	27		12	27	ns
Overvoltage Recovery Time	+25°C	IV		25	37		25	37		25	37	ns
Harmonic Distortion												
Analog Input @ 1.2 MHz	+25°C	I	70	80		75	82		75	82		dBc
@ 1.2 MHz	Full	VI	67			70			70			dBc
@ 4.3 MHz	+25°C	V		76			77			77		dBc
@ 9.6 MHz	+25°C	I	68	75		72	76		72	76		dBc
@ 9.6 MHz	Full	VI	64			68			64			dBc
@ 12.1 MHz	+25°C	V		72			74			74		dBc
Signal-to-Noise Ratio[2]												
Analog Input @ 1.2 MHz	+25°C	I	63	66		64	67		64	67		dB
@ 1.2 MHz	Full	VI	61			63			61			dB
@ 4.3 MHz	+25°C	V		64			65			65		dB
@ 9.6 MHz	+25°C	I	62	64		62	64		62	64		dB
@ 9.6 MHz	Full	VI	60			61			58			dB
@ 12.1 MHz	+25°C	V		64			64			64		dB
Two-Tone Intermodulation Distortion Rejection[3]	+25°C	V		66			68			68		dBc

Parameter (Conditions)	Temp	Test Level	AD9032AD/AZ Min	Typ	Max	AD9032BD/BZ Min	Typ	Max	AD9032TD/TZ Min	Typ	Max	Units
DIGITAL OUTPUTS (10K ECL)												
Logic "1" Voltage	Full	VI	−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5			−1.5	V
Output Coding			2s Complement			2s Complement			2s Complement			
POWER SUPPLY												
$+V_S$ Supply Voltage	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	mA
$+V_S$ Supply Current	Full	VI		133	160		133	160		133	160	mA
$-V_S$ Supply Voltage	Full	VI	−5.45	−5.2	−4.95	−5.45	−5.2	−4.95	−5.45	−5.2	−4.95	mA
$-V_S$ Supply Current	Full	VI		610	672		610	672		610	672	mA
Power Dissipation	Full	VI		3.8	4.5		3.8	4.5		3.8	4.5	W
Power Supply Rejection Ratio (PSRR)[4]	Full	VI		4.0	10		4.0	10		4.0	10	mV/V

NOTES
[1]Outputs terminated through 510 Ω to −5.2 V; C_L < 4 pF. Typical values are valid for +25°C ambient.
[2]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.
[3]Intermodulation measured with analog input frequencies of 9.3 MHz and 9.6 MHz at 7 dB below full scale.
[4]PSRR is sensitivity of offset error to power supply variations within the 5% limits shown.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ . . . . . +7 V
$-V_S$ . . . . . −7 V
Analog Input . . . . . $-V_S$ to $+V_S$
Digital Inputs . . . . . $-V_S$ to 0 V
Digital Output Current . . . . . 20 mA
Operating Temperature Range
AD9032AD/BD/AZ/BZ . . . . . −25°C to +85°C
AD9032TD/TZ . . . . . −55°C to +125°C
Maximum Junction Temperature[2] . . . . . +175°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: θ_{CA} = 13°C/W; $T_J - T_C$ = 10°C max (worst case die junction temperature rise). See Thermal Management section.

EXPLANATION OF TEST LEVELS

Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. Devices are 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD9032AD	−25°C to +85°C	40-Pin Ceramic DIP	DH-40A
AD9032AZ[2]	−25°C to +85°C	40-Pin Ceramic Leaded Chip Carrier	Z-40
AD9032BD	−25°C to +85°C	40-Pin Ceramic DIP	DH-40A
AD9032BZ[2]	−25°C to +85°C	40-Pin Ceramic Leaded Chip Carrier	Z-40
AD9032TD	−55°C to +125°C	40-Pin Ceramic DIP	DH-40A
AD9032TZ[2]	−55°C to +125°C	40-Pin Ceramic Leaded Chip Carrier	Z-40
AD9034/PWB	Printed Circuit Board (only) of Evaluation Circuit		
AD9034/PCB	Complete Evaluation Board, Assembled and Tested (Order AD9032 DIP separately)		

NOTES
[1]For outline information see Package Information section.
[2]Ceramic leaded chip carrier packages are tested and shipped with unformed leads. Consult the factory for availability.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay (t_A)
The delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Data Ready Delay (t_{DR})
The delay between the 50% point of the change in output data and the 50% point of the rising edge of DATA READY.

Differential Nonlinearity (DNL)
The deviation of any code width from an ideal 1 LSB step, as determined by a histogram.

Harmonic Distortion
The rms value of the fundamental divided by the rms value of the worst harmonic.

Integral Nonlinearity (INL)
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit, as determined by a histogram.

Output Delay (t_{OD})
The delay between the 50% point of the rising edge of the ENCODE command and the 50% point of the next change in output data.

Output Time Skew
Bit-to-bit time variations among D_0 to D_{11} outputs. Time skew includes HIGH-to-LOW and LOW-to-HIGH transitions of the digital output bits.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 12-bit accuracy after an analog input signal 150% of full scale is reduced to the midscale of the converter.

Power Supply Rejection Ratio
The ratio of a change in power supply voltage which results in a change in input offset voltage.

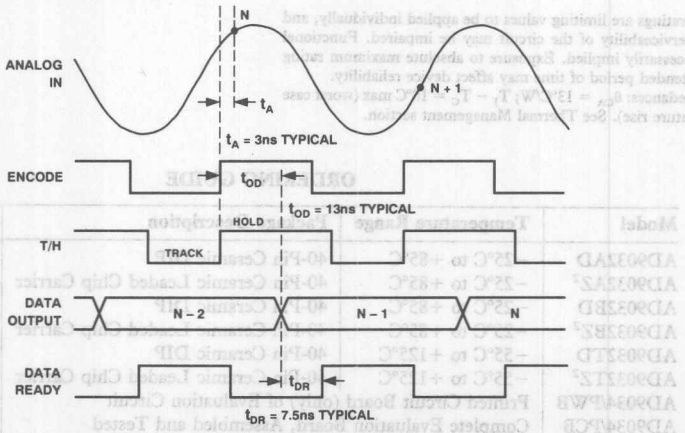
Pulse Width (High and Low)
Rated performance of the ADC is assured when stated restrictions on ENCODE pulse width shown in Specifications table are observed.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1 dB below full scale.

Spurious Free Dynamic Range (SFDR)
The rms value of the fundamental divided by the rms value of the highest spurious signal. This is generally specified as a function of input signal level.

Transient Response
The time required for the converter to achieve 12-bit accuracy when a full-scale step function is applied to the analog input.

Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of either of two input signals to the power of the strongest third-order IMD signal.

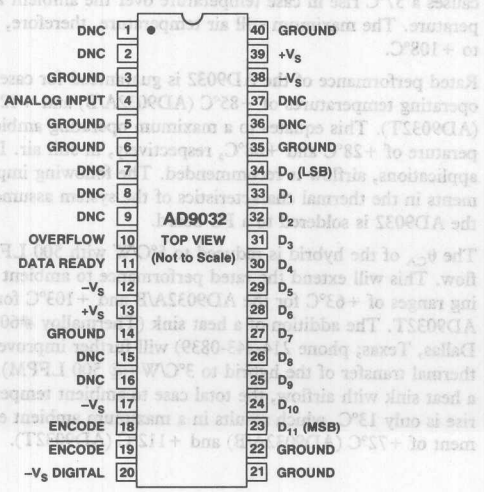


Timing Diagram

PIN DESCRIPTIONS

Pin	Name	Description
1	GAIN ADJUST	Can be used to null out initial gain error of ADC. Normally open.
2	OFFSET ADJUST	Can be used to null out initial offset error of ADC. Normally open.
3, 5, 6, 14, 21, 22, 35, 40	GROUND	All ground pins should be connected together and to low-impedance ground plane near AD9034.
4	ANALOG INPUT	Analog input to ADC, ±1.024 V input range; 100 Ω input resistance; 7 pF input capacitance.
7, 8, 9, 15 16, 36, 37	DNC	Do not connect. Internal test points.
10	OVERFLOW	ECL-compatible output; normally low. High when analog input > +FS.
11	DATA READY	ECL-compatible output. Rising edge of signal suitable, for externally latching $D_0 - D_{11}$.
12, 17, 20, 38	$-V_S$	−5.2 V supply voltage.
13, 39	$+V_S$	+5.0 V supply voltage.
18	ENCODE	Differential ECL convert command.
19	$\overline{\text{ENCODE}}$	Sampling occurs on rising edge; no internal terminations.
23–34	D_0–D_{11}	ECL-compatible digital outputs; 2s complement coding.

PIN DESIGNATIONS



THEORY OF OPERATION

The AD9032 is a digitally corrected subranging analog-to-digital converter (ADC) optimized for fast sampling rates and dynamic range. Refer to the block diagram on the first page. The AD9032 is a vertically integrated structure consisting of a track-and-hold (T/H) amplifier, a combined flash ADC and digital-to-analog (DAC), a summation amplifier, digital error correction logic, and timing circuits. Reference circuits to generate stable DC voltages and currents that maintain the static accuracy of the device are also included, but are not shown on the block diagram.

Internally, the monolithic T/H (AD9101) provides fast settling and acquisition times while minimizing distortion introduced by the sampling process. The unique design of the sampling bridge allows accurate sampling of high slew rate signals with negligible distortion. The effects of jitter and other aperture errors have been reduced to provide dynamic performance previously unavailable in monolithic and discrete designs.

At the output of the T/H amplifier, the analog input is converted by the first (5-bit) ADC. This 5-bit representation of the input value is stored in the digital error correction logic. It is also converted back to an analog signal by the 14-bit-accurate DAC on the same chip with the ADC. The 32 DAC current sources are steered directly by the outputs of the 32 input comparators on the 5-bit ADC. This minimizes propagation delay through the DAC, and allows the summation of the DAC signal and the held output of the T/H to settle quickly. The hold time of the T/H is optimized to allow sufficient settling time without sacrificing the acquisition time necessary to acquire the next sample.

The residue signal, representing the difference between the 5-bit conversion (DAC output) and the input signal held by the T/H, is amplified by the summation amplifier. During the tracking period of the T/H, this residue signal can be much larger than the input range of the 8-bit ADC and would saturate the output stage of a normal amplifier. To protect the ADC and maintain fast settling times under all conditions, the summation amplifier is a custom design with clamping circuits that prevent saturation, limit the output voltage, and preserve settling time.

The 8-bit flash ADC determines the 7 least significant bits (LSBs) of the 12-bit conversion and generates a correction bit for any small errors created by inaccuracies in the first 5-bit conversion. This 8-bit signal and the 5-bit quantization are combined to obtain a 12-bit-accurate representation of the analog input voltage.

USING THE AD9032

Layout Information

Preserving the accuracy and dynamic performance of the AD9032 requires that designers pay special attention to the layout of the printed circuit board. Signal paths should be impedance matched and properly terminated at or near the package connections. Analog signal paths should be isolated from digital signal paths. Capacitive and inductive coupling of digital signals into analog signal sections can degrade the overall performance of the A/D converter.

Analog Input

The analog input pin of the AD9032 is terminated with a 100 Ω load. The analog input range of the AD9032 is factory trimmed for a ±1.024 V input for compatibility with the AD9034. The signal presented to the monolithic T/H is divided in half to optimize dynamic performance.

When the amplitude, bandwidth, or dc level of the analog input requires external signal conditioning, the selection of the input amplifier is of particular concern. The noise and distortion of the amplifier must be taken into account to preserve the dynamic range of the AD9032. The AD9617 wideband, current feedback amplifier is an excellent choice for most applications.

Timing

Internal timing for the AD9032 is trimmed at the factory to simplify use. Care should be taken to ensure that the encode command to the AD9032 is free from jitter that can degrade dynamic performance. Differential ECL inputs to the AD9032 can be derived from a single-ended source using a fast comparator such as the AD96685. The encode source should be located and terminated as close to the AD9032 as possible.

The ECL-compatible digital outputs are latched to provide valid data for the entire conversion period (less the transition region of latch). This data should be latched into external ECL registers located near the AD9032. External termination resistors are required (510 Ω recommended). The data are latched with either the encode command or the data ready signal provided on the AD9032. The rising edge of the data ready signal occurs typically 7.5 ns after the data changes.

Gain and Offset Adjustment

Gain and offset pins are normally not connected. Rated performance is guaranteed without any external connection to these pins. In most applications, wide variations in input signal range and offset can be accommodated using external amplifiers. However, in those applications where a vernier adjustment is required (such as nulling out factory trim limits), the gain and offset pins will provide sufficient adjustment range.

Both inputs offer a 20 kΩ input resistance that can be driven from a voltage source (DAC, amplifier) or the center tap of a potentiometer. The offset pin provides a 195 mV/V sensitivity to input offset, while the gain pin offers 120 mV/V adjustment of the full-scale input range of the ADC. The adjustment range for offset is limited to 10 mV and for gain is 20 mV without introducing potential dynamic errors or restricting the operating temperature range of the part.

Power Supplies

The unique design of the AD9032 provides excellent dynamic performance without a need for high voltage power supplies. Two supplies (+5 V and −5.2 V) are all that are required to achieve rated performance. Careful layout and decoupling of power supplies used in conjunction with a low impedance analog ground plane will reduce supply-related noise components.

Separate analog and digital supplies are not required. In applications with only limited analog supply current, a separate digital supply source can be used for the −5.2 V supply on Pin 20. This supply typically requires 310 mA (330 mA max) and may be shared with other ECL logic devices when isolated with bypass capacitors and/or ferrite bead inductors (Fair-Rite Products Corporation part # 2743001111, Wallkill, NY). Each power supply pin should be capacitively decoupled to the ground plane through a good high frequency ceramic capacitor (0.1 μF) and a single large value capacitor (tantalum 10 μF).

For optimum performance, "clean" linear supplies ensure that switching noise on the supplies does not introduce distortion products during the encoding process. Recognizing, however, that switching power supplies may be required in power-sensitive applications, decoupling recommendations outlined above are critically important for using switching supplies effectively. Elsewhere in this data sheet, a graph shows the PSRR of the AD9032 as a function of the ripple frequency present on the AD9032 supplies. Clearly, if they must be used, switching power supplies with the lowest possible frequency should be selected.

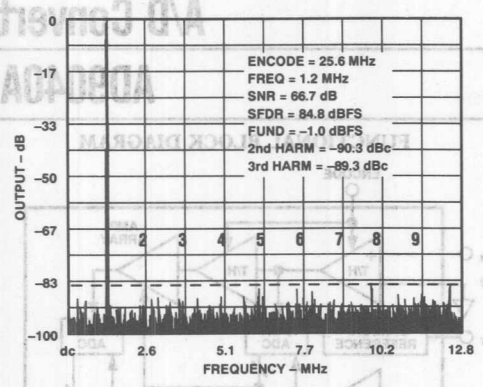
Thermal Management

The AD9032 design minimizes power dissipation; however, the ADC does typically require 3.8 W (4.5 W max) to operate. To ensure long life and reliable operation, the maximum junction temperature in the AD9032 must be limited to +175°C.

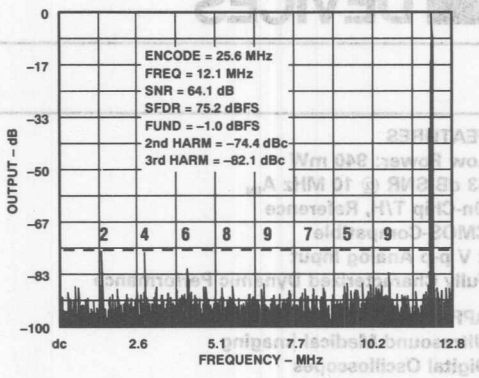
Within the hybrid, the hottest discrete die has a case to junction temperature rise of 10°C (max). Therefore, the case temperature of the AD9032 should not exceed +165°C under worst case operating conditions. Without airflow, the θ_{CA} of the hybrid package is 13°C/W. Assuming maximum power dissipation, this causes a 57°C rise in case temperature over the ambient air temperature. The maximum still air temperature, therefore, is equal to +108°C.

Rated performance of the AD9032 is guaranteed for case operating temperatures of +85°C (AD9032A/B) and +125°C (AD9032T). This equates to a maximum operating ambient temperature of +28°C and +68°C, respectively, in still air. In most applications, airflow is recommended. The following improvements in the thermal characteristics of the system assume that the AD9032 is soldered to a PC board.

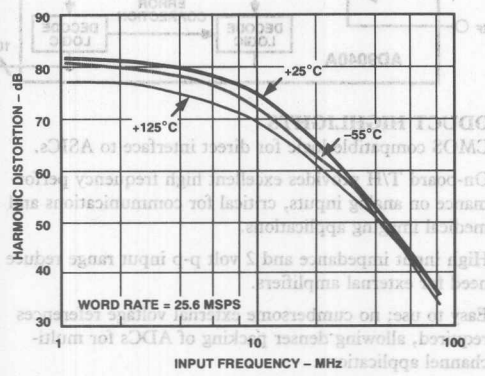
The θ_{CA} of the hybrid is reduced to 5°C/W with 500 LFPM airflow. This will extend the rated performance to ambient operating ranges of +63°C for the AD9032A/B and +103°C for the AD9032T. The addition of a heat sink (Thermalloy #6087B, Dallas, Texas; phone 214-243-0839) will further improve the thermal transfer of the hybrid to 3°C/W (@ 500 LFPM). Using a heat sink with airflow, the total case to ambient temperature rise is only 13°C, which results in a maximum ambient environment of +72°C (AD9032A/B) and +112°C (AD9032T).



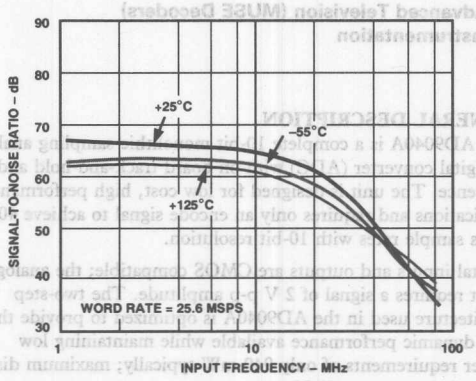
AD9032 A/D Converter FFT



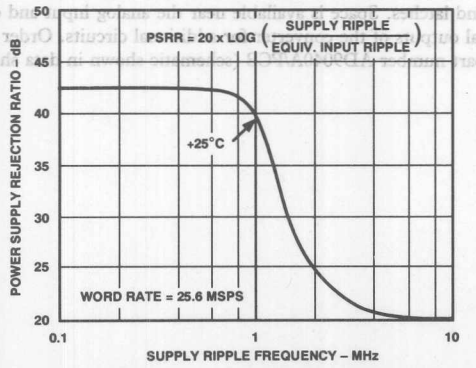
AD9032 A/D Converter FFT



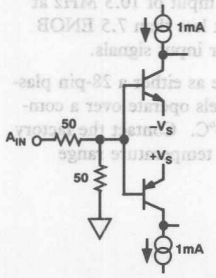
AD9032 Harmonic Distortion vs. Analog Input



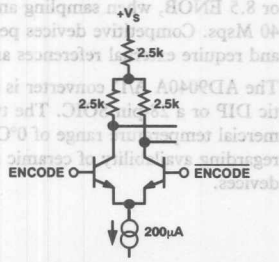
AD9032 SNR vs. Analog Input



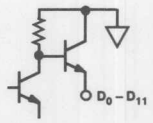
AD9032 PSRR vs. Supply Ripple Frequency



Equivalent Analog Input Circuit



Equivalent Encode Input Circuit

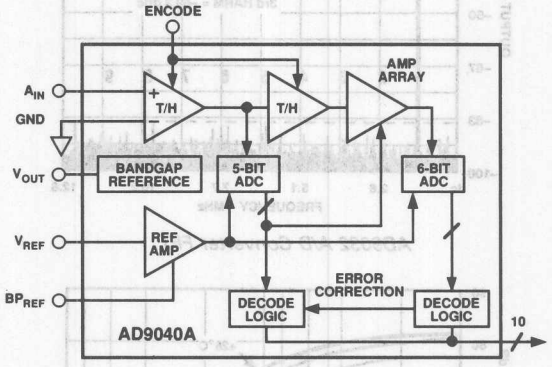


Equivalent Digital Output Circuit

FEATURES
Low Power: 940 mW
53 dB SNR @ 10 MHz A_{IN}
On-Chip T/H, Reference
CMOS-Compatible
2 V p-p Analog Input
Fully Characterized Dynamic Performance

APPLICATIONS
Ultrasound Medical Imaging
Digital Oscilloscopes
Professional Video
Digital Communications
Advanced Television (MUSE Decoders)
Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9040A is a complete 10-bit monolithic sampling analog-to-digital converter (ADC) with on-board track-and-hold and reference. The unit is designed for low cost, high performance applications and requires only an encode signal to achieve 40 Msps sample rates with 10-bit resolution.

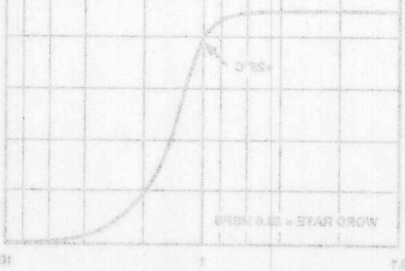
Digital inputs and outputs are CMOS compatible; the analog input requires a signal of 2 V p-p amplitude. The two-step architecture used in the AD9040A is optimized to provide the best dynamic performance available while maintaining low power requirements of only 940 mW typically; maximum dissipation is 1.1 watt at 40 Msps.

The signal-to-noise ratio (SNR), including harmonics, is 53 dB, or 8.5 ENOB, when sampling an analog input of 10.3 MHz at 40 Msps. Competitive devices perform at less than 7.5 ENOB and require external references and larger input signals.

The AD9040A A/D converter is available as either a 28-pin plastic DIP or a 28-pin SOIC. The two models operate over a commercial temperature range of 0°C to +70°C. Contact the factory regarding availability of ceramic military temperature range devices.

PRODUCT HIGHLIGHTS

1. CMOS compatible logic for direct interface to ASICs.
2. On-board T/H provides excellent high frequency performance on analog inputs, critical for communications and medical imaging applications.
3. High input impedance and 2 volt p-p input range reduce need for external amplifiers.
4. Easy to use; no cumbersome external voltage references required, allowing denser packing of ADCs for multichannel applications.
5. Available in 28-lead plastic DIP and SOIC packages.
6. Evaluation board includes AD9040AJR, reconstruction DAC, and latches. Space is available near the analog input and digital outputs of the converter for additional circuits. Order as part number AD9040A/PCB (schematic shown in data sheet).



Parameter (Conditions)	Temp	Test Level	AD9040AJN/JR Min	Typ	Max	Units
RESOLUTION				10		Bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		1.0	2.0	LSB
	Full	VI			2.5	LSB
Integral Nonlinearity	+25°C	I		1.0	2.0	LSB
	Full	VI			2.5	LSB
No Missing Codes	Full	VI		Guaranteed		
Gain Error	+25°C	I		±0.5	±1.5	% FS
	Full	VI			±2	% FS
Gain Tempco[1]	Full	V		±70		ppm/°C
ANALOG INPUT						
Input Voltage Range	+25°C	V		2		V p-p
Input Offset Voltage	+25°C	I		±2	±25	mV
	Full	VI			±30	mV
Input Bias Current	+25°C	I		7	15	μA
	Full	VI			25	μA
Input Resistance	+25°C	I	200	350		kΩ
Input Capacitance	+25°C	V		5		pF
Analog Bandwidth	+25°C	V		48		MHz
BANDGAP REFERENCE						
Output Voltage	Full	VI	2.4		2.6	V
Temperature Coefficient[1]	Full	V		±40		ppm/°C
SWITCHING PERFORMANCE						
Maximum Conversion Rate	+25°C	I	40			Msps
Minimum Conversion Rate	+25°C	IV		2	10	Msps
Aperture Delay (t_A)	+25°C	V		1.9		ns
Aperture Uncertainty (Jitter)	+25°C	V		7		ps, rms
Output Propagation Delay (t_{PD})[2]	+25°C	I	7.5	10	12	ns
	Full	IV	6		14	ns
DYNAMIC PERFORMANCE						
Transient Response	+25°C	V		25		ns
Overvoltage Recovery Time	+25°C	V		40		ns
Signal-to-Noise Ratio[3]						
f_{IN} = 2.3 MHz	+25°C	I	51	54		dB
f_{IN} = 10.3 MHz	+25°C	I	50	53		dB
Signal-to-Noise Ratio[3] (Without Harmonics)						
f_{IN} = 2.3 MHz	+25°C	I	52	55		dB
f_{IN} = 10.3 MHz	+25°C	I	51	54		dB
Signal-to-Noise Ratio[3, 4]						
f_{IN} = 2.3 MHz	+25°C	I	52	56		dB
f_{IN} = 10.3 MHz	+25°C	I	51	55		dB
Signal-to-Noise Ratio[3, 4] (Without Harmonics)						
f_{IN} = 2.3 MHz	+25°C	I	53	57		dB
f_{IN} = 10.3 MHz	+25°C	I	53	56		dB
2nd Harmonic Distortion						
f_{IN} = 2.3 MHz	+25°C	I	56	67		dBc
f_{IN} = 10.3 MHz	+25°C	I	56	65		dBc
3rd Harmonic Distortion						
f_{IN} = 2.3 MHz	+25°C	I	58	73		dBc
f_{IN} = 10.3 MHz	+25°C	I	58	70		dBc
Two-Tone Intermodulation Distortion Rejection[5]	+25°C	V		62		dBc
Differential Phase	+25°C	III		0.15	0.5	Degrees
Differential Gain	+25°C	III		0.25	1.0	%

AD9040A—SPECIFICATIONS

Parameter (Conditions)	Temp	Test Level	AD9040AJN/JR Min	Typ	Max	Units
ENCODE INPUT						
Logic "1" Voltage	Full	VI	4.0			V
Logic "0" Voltage	Full	VI			1.0	V
Logic "1" Current	Full	VI			±1	μA
Logic "0" Current	Full	VI			±1	μA
Input Capacitance	+25°C	V		14		pF
Encode Pulse Width (High) (t_{EH})[6]	+25°C	IV	10		100	ns
Encode Pulse Width (Low) (t_{EL})[6]	+25°C	IV	10		100	ns
DIGITAL OUTPUTS						
Logic "1" Voltage	Full	VI	4.95			V
Logic "0" Voltage	Full	VI			0.05	V
Output Coding				Offset Binary		
POWER SUPPLY						
V_D Supply Current	Full	VI		13	20	mA
$+V_S$ Supply Current	Full	VI		89	105	mA
$-V_S$ Supply Current	Full	VI		87	100	mA
Power Dissipation	Full	VI		0.94	1.1	W
Power Supply Rejection Ratio (PSRR)[7]	+25°C	I			±15	mV/V

NOTES

[1]"Gain Tempco" is for converter using internal reference; "Temperature Coefficient" is for bandgap reference only.

[2]Output propagation delay (t_{PD}) is measured from the 50% point of the falling edge of the encode command to the min/max voltage levels of the digital outputs with 10 pF maximum loads.

[3]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

[4]ENCODE = 32 Msps.

[5]3rd order intermodulation measured with analog input frequencies of 2.3 MHz and 2.4 MHz at 7 dB below full scale.

[6]For rated performance at 40 Msps, duty cycle of encode command should be 50% ±10%.

[7]Measured as the ratio of the change in offset voltage for a 5% change in $+V_S$ or $-V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I — 100% Production Tested.

II — 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III — Sample Tested Only.

IV — Parameter is guaranteed by design and characterization testing.

V — Parameter is a typical value only.

VI — All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

ABSOLUTE MAXIMUM RATINGS[1]

$\pm V_S$ . . . . . ±7 V

V_D . . . . . +7 V

ANALOG IN . . . . . $-V_S$ to $+V_S$

DIGITAL INPUTS . . . . . 0 V to $+V_S$

V_{REF} Input . . . . . 0 V to $+V_S$

Digital Output Current . . . . . 20 mA

Operating Temperature

AD9040AJN/JR . . . . . 0°C to +70°C

Storage Temperature . . . . . −65°C to +150°C

Maximum Junction Temperature[2] (JN/JR Suffixes) . . . +150°C

Lead Soldering Temp (10 sec) . . . . . +300°C

NOTES

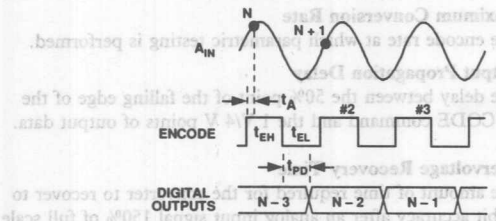
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances (parts soldered to board):
N Package (Plastic DIP): θ_{JA} = 42°C/W; θ_{JC} = 10°C/W.
R Package (SOIC): θ_{JA} = 47°C/W; θ_{JC} = 10°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9040AJN	0°C to +70°C	28-Pin Plastic DIP	N-28
AD9040AJR	0°C to +70°C	28-Pin SOIC Package	R-28
AD9040A/PWB	Printed Circuit Board (Only) of Evaluation Circuit		
AD9040A/PCB	Complete Evaluation Board, Assembled and Tested, Including AD9040AJR		

*For outline information see Package Information section.

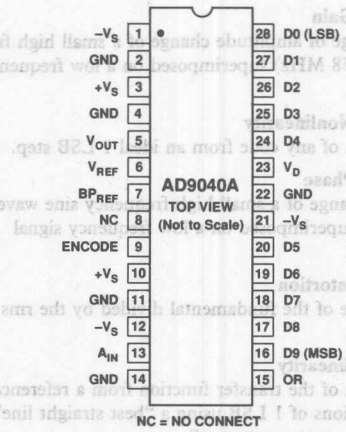


		MIN	TYP	MAX
t_A	APERTURE DELAY		1.9	
t_{EH}	PULSE WIDTH HIGH	10		100
t_{EL}	PULSE WIDTH LOW	10		100
t_{PD}	OUTPUT PROP DELAY	7.5	10ns	12

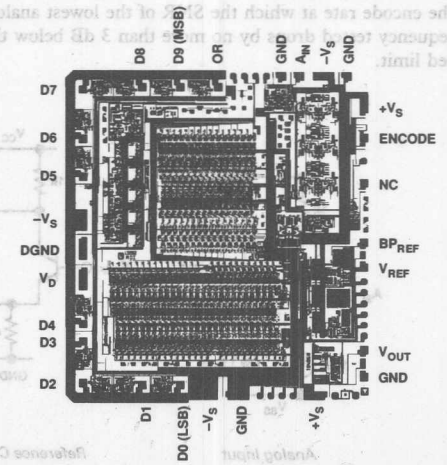
Timing Diagram

PIN DESCRIPTIONS

Pin No.	Name	Function
1, 12, 21	$-V_S$	−5 V Power Supply
2, 4, 11, 14, 22	GND	Ground
3, 10	$+V_S$	Analog +5 V Power Supply
5	V_{OUT}	Internal Bandgap Voltage Reference (Nominally +2.5 V)
6	V_{REF}	Noninverting Input to Reference Amplifier. Voltage reference for ADC is connected here.
7	BP_{REF}	External Connection for (0.1 μF) Reference Bypass Capacitor
8	NC	No Connection Internally
9	ENCODE	Encode Clock Input to ADC. Internal T/H placed in hold mode (ADC is encoding) on rising edge.
13	A_{IN}	Noninverting Input to T/H Amplifier
15	OR	Out-of-Range Condition Output. Active high when analog input exceeds input range of ADC by 1 LSB (<FS − 1 LSB or >+FS + 1 LSB).
16	D9 (MSB)	Most Significant Bit of ADC Output; TTL/CMOS Compatible
17–20	D8–D5	Digital Output Bits of ADC; TTL/CMOS Compatible
23	V_D	Digital +5 V Power Supply
24–27	D4–D1	Digital Output Bits of ADC; TTL/CMOSL Compatible
28	D0 (LSB)	Least Significant Bit of ADC Output; TTL/CMOS Compatible



PDIP and SOIC Pinouts



DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions . . . . . 204 × 185 × 21 (±1) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Aluminum
Backing . . . . . None
Substrate Potential . . . . . $-V_S$
Transistor Count 5,070
Passivation . . . . . Oxynitride
Die Attach (JN/JR) . . . . . Epoxy
Bond Wire (JN/JR) . . . . . Gold

Analog input frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Gain
The percentage of amplitude change of a small high frequency sine wave (3.58 MHz) superimposed on a low frequency signal (15.734 kHz).

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Differential Phase
The phase change of a small high frequency sine wave (3.58 MHz) superimposed on a low frequency signal (15.734 kHz).

Harmonic Distortion
The rms value of the fundamental divided by the rms value of the harmonic.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency tested drops by no more than 3 dB below the guaranteed limit.

The delay between the 50% point of the falling edge of the ENCODE command and the 1 V/4 V points of output data.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 10-bit accuracy after an analog input signal 150% of full scale is reduced to the full-scale range of the converter.

Power Supply Rejection Ratio (PSRR)
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1 dB below full scale.

Signal-to-Noise Ratio (Without Harmonics)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, excluding the first eight harmonics and dc, with an analog input signal 1 dB below full scale.

Transient Response
The time required for the converter to achieve 10-bit accuracy when a step function is applied to the analog input.

Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of either of two input signals to the power of the strongest third-order IMD signal.

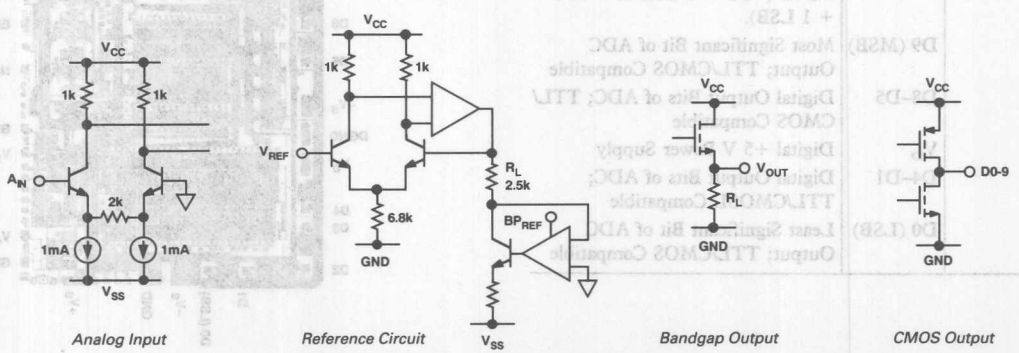


Figure 1. Equivalent Circuits

THEORY OF OPERATION

Refer to the block diagram.

The AD9040A employs subranging architecture and digital error correction. This combination of design techniques insures true 10-bit accuracy at the digital outputs of the converter.

At the input, the analog signal is applied to a track-and-hold (T/H) that holds the analog value which is present when the unit is strobed with an ENCODE command. The conversion process begins on the rising edge of this pulse, which should have a 50% (±10%) duty cycle. Minimum encode rate of the AD9040A is 10 Msps because of the use of three internal T/H devices.

The held analog value of the first track-and-hold is applied to a 5-bit flash converter and a pair of internal T/Hs (shown in the block diagram as a single unit). The T/Hs pipeline the analog signal to the amplifier array through a residue ladder and switch ing circuit while the 5-bit flash converter resolves the most significant bits (MSBs) of the held analog voltage.

When the 5-bit flash converter has completed its cycle, its output activates 1-of-32 ladder switches; these, in turn, cause the correct residue signal to be applied to the error amplifier array.

The output of the error amplifier is applied to a 6-bit flash converter whose output supplies the five least significant bits (LSBs) of the digital output along with one bit of error correction for the 5-bit main range converter.

Decode logic aligns the data from the two converters and presents the result as a 10-bit parallel digital word. The output stage of the AD9040A is CMOS. Output data are strobed on the trailing edge of the ENCODE command.

Full-scale range of the AD9040A is determined by the reference voltage applied to the V_{REF} (Pin 6) input. This voltage sets the internal flash and residue ladder voltage drops; these establish the value of the LSB. Because of headroom restraints, the full-scale range cannot be increased by applying a higher-than-specified reference voltage. Conversely, a lower reference voltage will reduce the full-scale range of the converter, but will also decrease its performance. An internal bandgap reference voltage of +2.5 V is provided to assure optimum performance over the operating temperature range.

USING THE AD9040A

Timing

The duty cycle of the encode clock for the AD9040A is critical for obtaining rated performance of the ADC. Internal pulse widths within the track-and-hold are established by the encode command pulse width; to ensure rated performance, the duty cycle should be held at 50%. Duty cycle variations of less than ±10% will cause no degradation in performance.

Operation at encode rates less than 10 Msps is not recommended. The internal track-and-hold saturates, causing erroneous conversions. This T/H saturation precludes clocking the AD9040A in burst mode. The 50% duty cycle must be maintained even for sample rates down to 10 Msps.

The AD9040A provides latched data outputs, with 2 1/2 pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the falling edge of the encode command (refer to AD9040A Timing Diagram). The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9040A; these transients can detract from the converter's dynamic performance.

Voltage Reference

A stable voltage reference is required to establish the 2-V p-p range of the AD9040A. There are two options for creating this reference. The easiest and least expensive way to implement it is to use the (+2.5 V) bandgap voltage reference which is internal to the ADC. Figure 2 illustrates the connections for using the internal reference. The internal reference has 500 μA of extra drive current which can be used for other circuits.

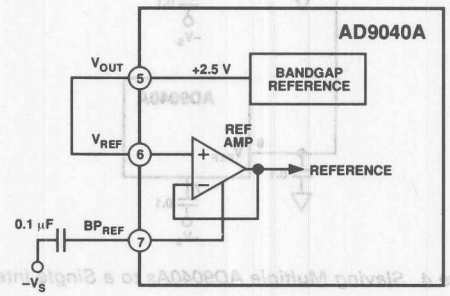


Figure 2. AD9040A Using Internal Reference

Some applications may require greater accuracy, improved temperature performance, or adjustment of the gain (input range) of the AD9040A which cannot be obtained by using the internal reference. For these applications, an external +2.5 V reference can be used, as shown in Figure 3. The V_{REF} input requires 5 μA of drive current.

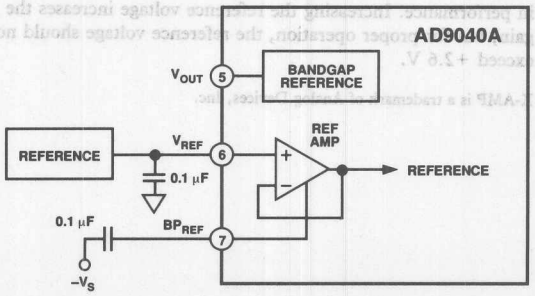


Figure 3. AD9040A Using External Reference

In applications using multiple AD9040As, slaving the reference inputs to a single reference output will improve gain tracking among the ADCs, as shown in Figure 4.

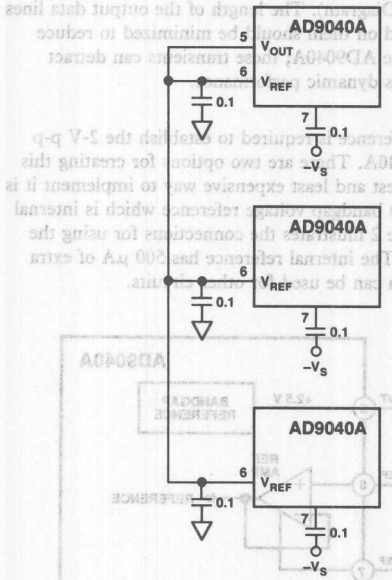


Figure 4. Slaving Multiple AD9040As to a Single Internal Reference

In the specifications table, the Gain Tempco parameter under DC ACCURACY applies to the ADC when the internal reference is being used. If an external reference is used, its temperature coefficient must be taken into account to determine overall temperature performance.

The input range can be varied by adjusting the reference voltage applied to the AD9040A. By decreasing the reference voltage, the gain can be reduced approximately 10% with no degradation in performance. Increasing the reference voltage increases the gain; but for proper operation, the reference voltage should not exceed +2.6 V.

X-AMP is a trademark of Analog Devices, Inc.

Time-Gain Control ADC

Ultrasound and sonar systems require an increase in gain versus time. This allows the system to correct for attenuation of return pulses. Figure 5 shows the AD600/602 amplifier and the AD9040A ADC configured as a time-gain control analog-to-digital converter. The control voltage ramps from −625 mV to +625 mV, permitting 40 dB of gain-control range. The voltage used for gain control can be either a linear ramp, or the output of a voltage-output DAC such as the AD7242.

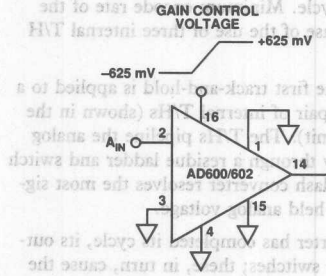


Figure 5. Ultrasound/Sonar Time-Gain Control ADC Using X-AMPs™

Transient Response

Figure 6 illustrates the method for evaluating ADC transient performance. Two synthesizers are locked in synchronization, but tuned to frequencies which are slightly offset from a 2-to-1 submultiple.

One synthesizer clocks a flat pulse network at a frequency of 19.9609375 MHz to provide the analog input signal; the other synthesizer output is shaped to provide a CMOS 40 MHz sampling clock. At the output of the AD9040A, output data reflects an interleaved alias of the input pulse. The repetitive sampling allows the measurement of ADC transient response as shown in performance graphs elsewhere in this data sheet.

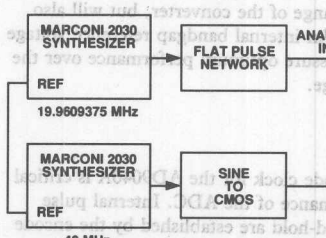


Figure 6. AD9040A Transient Response Test

Layout Information

Preserving the accuracy and dynamic performance of the AD9040A requires that designers pay special attention to the layout of the printed circuit board.

Analog paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input and reference voltage connections should be kept away from digital signal paths; this reduces the amount of digital switching noise which is capacitively coupled into the analog section. Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch. The AD9040A digital outputs should be buffered or latched close to the device (<2 cm). This prevents load transients which may feedback into the device.

In high speed circuits, layout of the ground is critical. A single, low impedance ground plane on the component side of the board is recommended. Power supplies should be capacitively coupled to the ground plane with high quality chip capacitors to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane, and provide low impedance ground planes. In systems with dedicated analog and digital grounds, all grounds of the AD9040A should be connected to the analog ground plane.

The power supplies of the AD9040A should be isolated from the supplies used for external devices; this reduces the amount of noise coupled into the ADC. The digital +5 volt connection of the device (V_D, Pin 23) powers the digital outputs and should be connected to the same supply as $+V_S$ (Pins 3 and 10). Connecting V_D to a system digital supply may couple noise into the device. Sockets limit dynamic performance and are not recommended for use with the AD9040A.

AD9040A EVALUATION BOARD

The evaluation board for the AD9040A (AD9040A/PCB) provides an easy and flexible method for evaluating the ADC's performance without (or prior to) developing a user-specific printed circuit board. The two-sided board includes a reconstruction DAC and digital output interface, and uses the layout and applications suggestions outlined above. It is available from Analog Devices at nominal cost.

Generous space is provided near the analog input and digital outputs to support additional signal processing components the user may wish to add. This prototyping area includes through holes with 100-mil centers to support a variety of component additions.

Input/Output/Supply Information

Power supply, analog input, clock connections, and reconstructed output (RC OUTPUT) are identified by labels on the evaluation board. Operation of the evaluation board should conform to the following characteristics:

Table I. Evaluation Board Characteristics

Parameter	Typical	Units
Supply Current		
+5 V	250	mA
−5.2 V	300	mA
A_{IN}		
Impedance	51	Ω
Voltage Range	±1.0	V
CLOCK		
Impedance	51	Ω
Frequency	40	Msps
RC OUTPUT		
Impedance	51	Ω
Voltage Range	0 to −1 V	V

Analog Input

Analog input signals can be fed directly into the Device Under Test input (A_{IN}). The A_{IN} input is terminated at the device with a 51 Ω resistor.

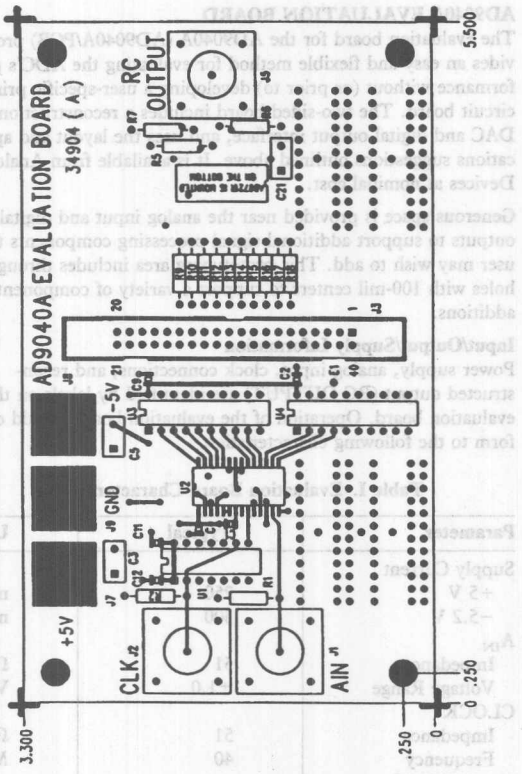


Figure 7. AD9040A/PCB Top View

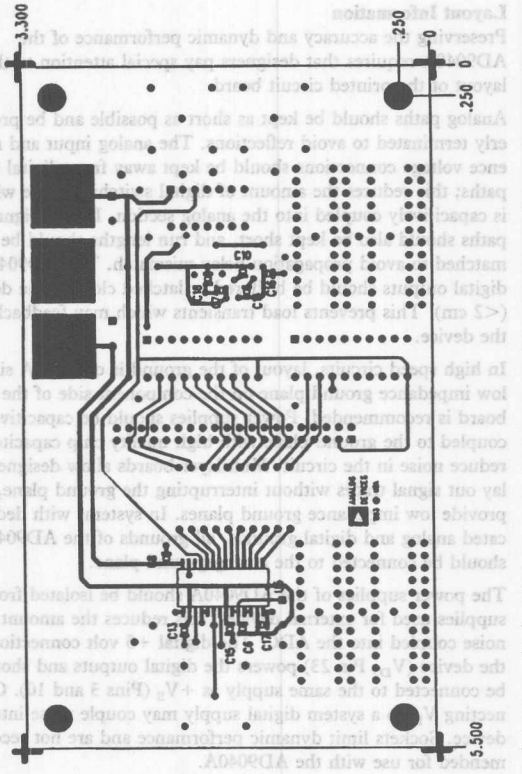


Figure 8. AD9040A/PCB Bottom View

DAC Reconstruction

The AD9040A evaluation board provides an on-board AD9721 reconstruction DAC for observing the digitized analog input signal. The AD9721 is terminated into 51 ohms to provide a 1 V p-p signal at the output (RC OUTPUT).

Output Data

The output data bits are latched with a CMOS 74AC574 which drives a 40-pin connector (AMP p/n 102153-9). The data and clock signals are available on the connector per the pin assignments shown on the schematic of the evaluation board. Output data are available on the falling edge of the clock.

Table II. AD9040A Digital Coding

Analog Input	Voltage Level	Out-of-Range	Digital Output
			MSB . . . LSB
+1.002 V	Positive Full Scale + 1 LSB	1	1111111111
+1 V	*Positive Full Scale*	0	1111111111
	Full Scale − 1 LSB	0	1111111110
+1/2 V	*Positive 1/2 Scale*	0	1100000000
	1/2 Scale − 1 LSB	0	1011111111
0 V	Bipolar Zero	0	10000000000
		0	01111111111
−1/2 V	*1/2 Scale +1 LSB*	0	0100000000
	Negative 1/2 Scale	0	0011111111
−1 V	*Full Scale + 1 LSB*	0	0000000001
	Negative Full Scale	0	0000000000
−1.002 V	Negative Full Scale − 1 LSB	1	0000000000

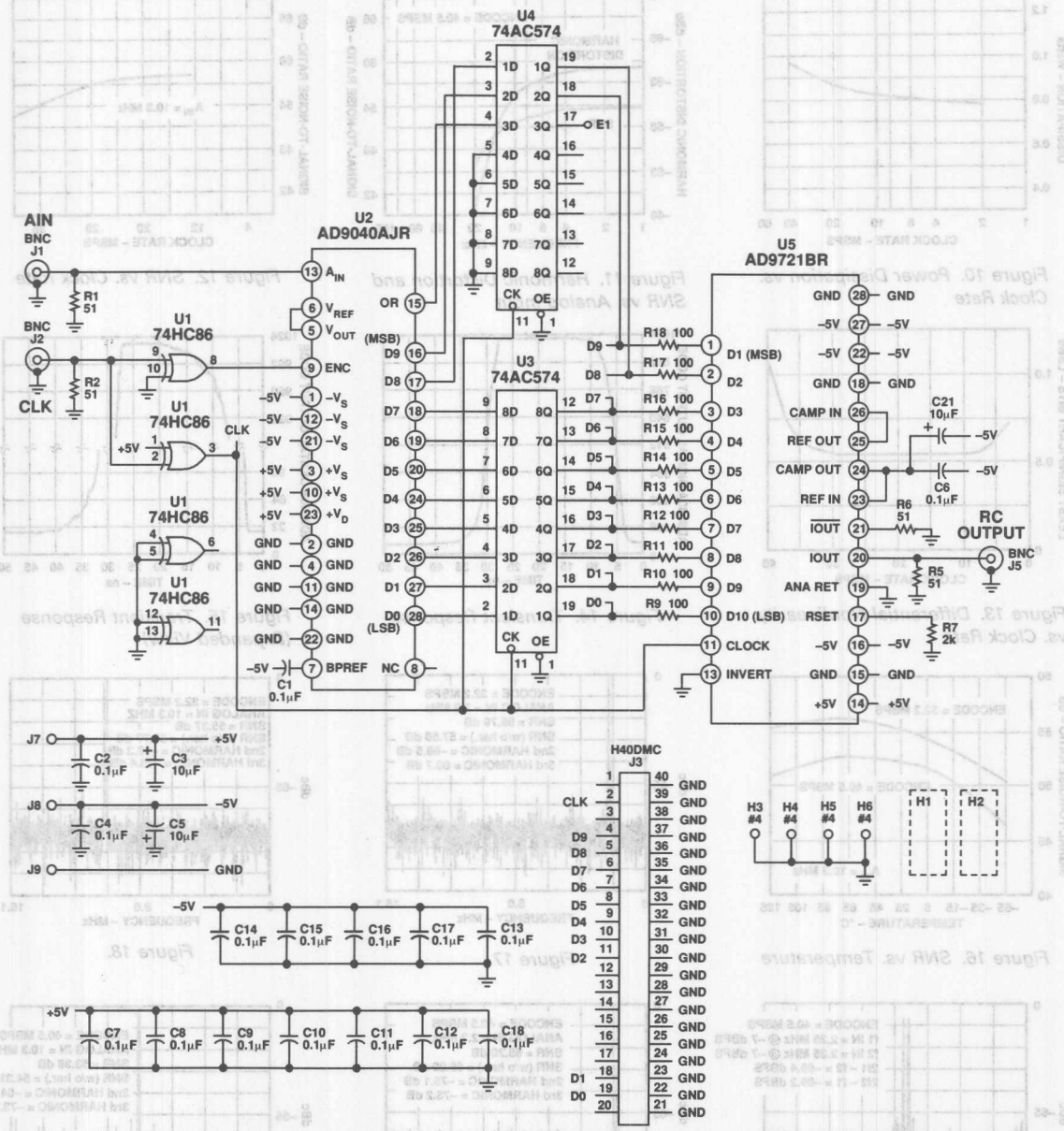


Figure 9. AD9040A/PCB Schematic

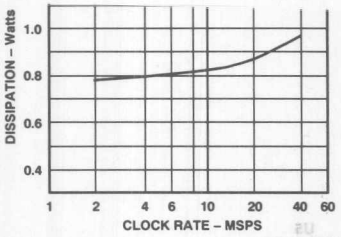


Figure 10. Power Dissipation vs. Clock Rate

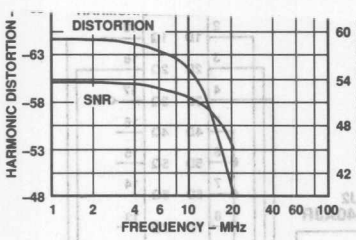


Figure 11. Harmonic Distortion and SNR vs. Analog Input

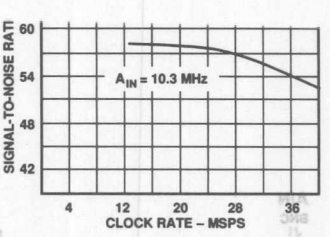


Figure 12. SNR vs. Clock Rate

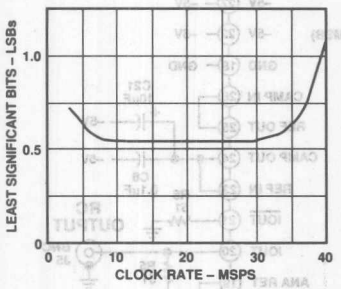


Figure 13. Differential Nonlinearity vs. Clock Rate

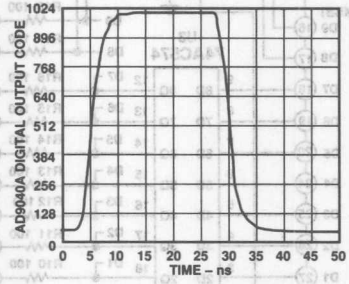


Figure 14. Transient Response

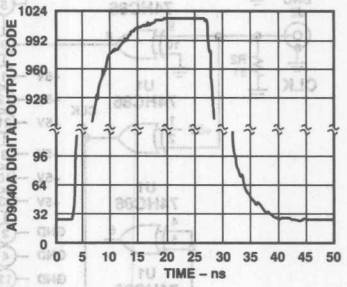


Figure 15. Transient Response (Expanded View)

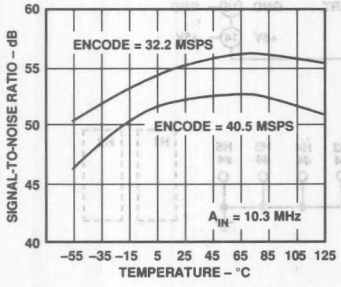


Figure 16. SNR vs. Temperature

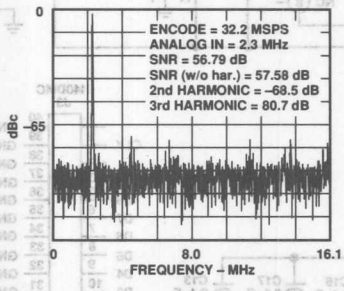


Figure 17.

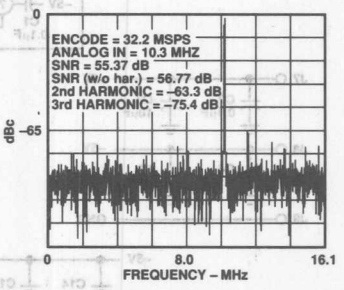


Figure 18.

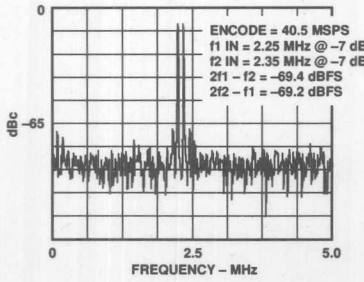


Figure 19.

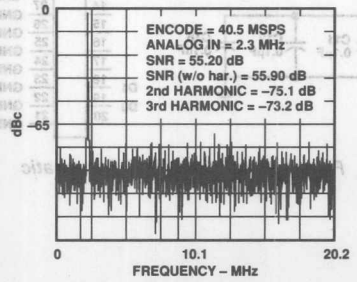


Figure 20.

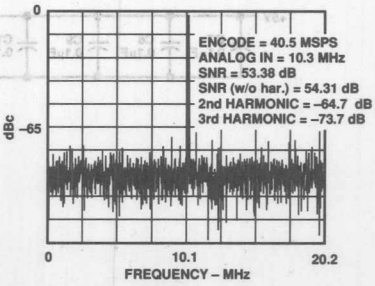


Figure 21.

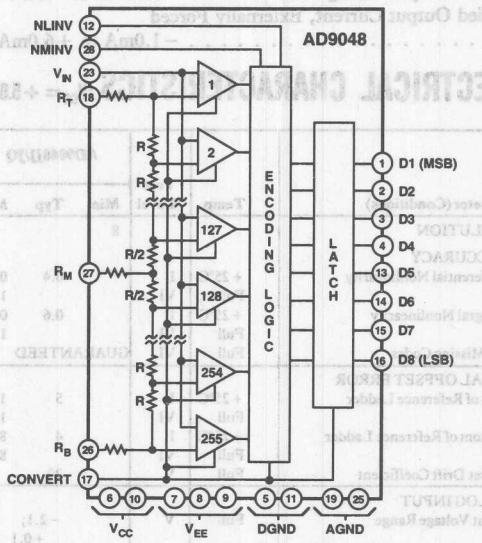
Monolithic 8-Bit Video A/D Converter

AD9048

FEATURES
- 35MSPS Encode Rate
- 16pF Input Capacitance
- 550mW Power Dissipation
- Industry-Standard Pinouts
- MIL-STD-883 Compliant Versions Available

APPLICATIONS
- Professional Video Systems
- Special Effects Generators
- Electro-Optics
- Digital Radio
- Electronic Warfare (ECM, ECCM, ESM)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9048 is an 8-bit, 35MSPS flash converter, made on a high speed bipolar process, which is an alternate source for the TDC1048 unit but offers enhancements over its predecessor. Lower power dissipation makes the AD9048 attractive for a variety of system designs.

Because of its wide bandwidth, it is an ideal choice for real-time conversion of video signals. Input bandwidth is flat with no missing codes.

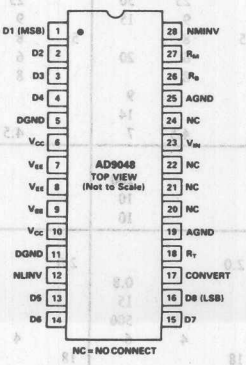
Clocked latching comparators, encoding logic and output buffer registers operating at minimum rates of 35MSPS preclude a need for a sample-and-hold (S/H) or track-and-hold (T/H) in most system designs using the AD9048. All digital control inputs and outputs are TTL compatible.

Devices operating over two ambient temperature ranges and with two grades of linearity are available. Linearities of either 0.5LSB or 0.75LSB can be ordered for a commercial range of 0 to +70°C, or extended case temperatures of −55°C to +125°C. Commercial versions are packaged in 28-pin DIPs; extended temperature versions are available in ceramic DIP and ceramic LCC packages. Both commercial units and MIL-STD-883 units are standard products.

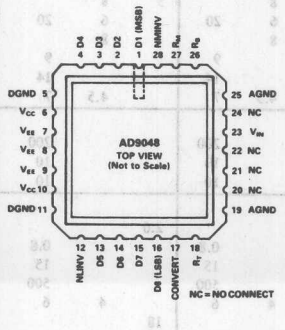
The AD9048 A/D converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9048/883B data sheet for detailed specifications.

PIN DESIGNATIONS

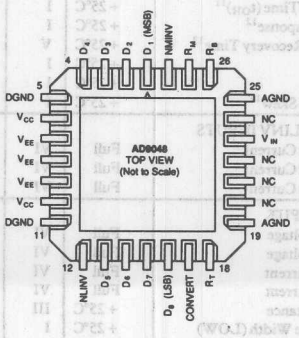
DIP



LCC



J-Leaded Ceramic



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9048–SPECIFICATIONS (typical with nominal supplies unless otherwise noted.)

ABSOLUTE MAXIMUM RATINGS[1]

V_{CC} to DGND . . . . . −0.5V dc to +7.0V dc
AGND to DGND . . . . . −0.5V dc to +0.5V dc
V_{EE} to AGND . . . . . +0.5V dc to −7.0V dc
V_{IN}, V_{RT} or V_{RB} to AGND . . . . . +0.5V to V_{EE}
V_{RT} to V_{RB} . . . . . −2.2V dc to +2.2V dc
CONV, NMINV or NLINV to DGND . −0.5V dc to +5.5V dc
Applied Output Voltage to DGND . −0.5V dc to +5.5V dc[2]
Applied Output Current, Externally Forced
. . . . . −1.0mA to +6.0mA[3, 4]
Output Short-Circuit Duration . . . . . 1.0sec[5]
Operating Temperature Range (Ambient)
AD9048JJ/KJ/JQ/KQ . . . . . 0 to +70°C
AD9048SE/SQ/TE/TQ . . . . . −55°C to +125°C
Maximum Junction Temperature (Plastic) . . . . . +150°C[6]
Maximum Junction Temperature (Hermetic) . . . . . +175°C[6]
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0V; V_{EE} = −5.2V; Differential Reference Voltage = 2.0V, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9048JJ/JQ			AD9048KJ/KQ			AD9048SE/SQ			AD9048TE/TQ			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I		0.4	0.75		0.3	0.5		0.4	0.75		0.3	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
Integral Nonlinearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR															
Top of Reference Ladder	+25°C	I		5	12		5	12		5	12		5	12	mV
	Full	VI			12			12			12			12	mV
Bottom of Reference Ladder	+25°C	I		4	8		4	8		4	8		4	8	mV
	Full	VI			8			8			8			8	mV
Offset Drift Coefficient	Full	V		20			20			20			20		µV/°C
ANALOG INPUT															
Input Voltage Range	Full	V		−2.1; +0.1			−2.1; +0.1			−2.1; +0.1			−2.1; +0.1		V
Input Bias Current[7]	+25°C	I		36	60		36	60		36	60		36	60	µA
	Full	VI			100			100			100			100	µA
Input Resistance	+25°C	I	200	300		200	300		200	300		200	300		kΩ
	Full	VI	40			40			40			40			kΩ
Input Capacitance	+25°C	III		16	20		16	20		16	20		16	20	pF
Full Power Bandwidth[8]	+25°C	III	10	15		10	15		10	15		10	15		MHz
REFERENCE INPUT															
Positive Reference Voltage[9]	Full	V		0.0			0.0			0.0			0.0		V
Negative Reference Voltage[9]	Full	V		−2.0			−2.0			−2.0			−2.0		V
Differential Reference Voltage	Full	V		2.0			2.0			2.0			2.0		V
Reference Ladder Resistance	Full	VI	50	90	125	50	90	125	50	90	125	50	90	125	Ω
Ladder Temperature Coefficient	Full	V		0.22			0.22			0.22			0.22		Ω/°C
Reference Ladder Current	Full	VI		23	40		23	40		23	40		23	40	mA
Reference Input Bandwidth	+25°C	V		10			10			10			10		MHz
DYNAMIC PERFORMANCE[10]															
Conversion Rate	+25°C	I	35	38		35	38		35	38		35	38		MHz
Aperture Delay	+25°C	III		2.4	5		2.4	5		2.4	5		2.4	5	ns
Aperture Uncertainty (Jitter)	+25°C	III		25	50		25	50		25	50		25	50	ps
Output Delay (t_{PD})	+25°C	I		13	15		9	15		9	15		9	15	ns
Output Hold Time (t_{OH})[11]	+25°C	I	5	8		5	8		5	8		5	8		ns
Transient Response[12]	+25°C	I		6	20		6	20		6	20		6	20	ns
Overvoltage Recovery Time[13]	+25°C	V		8			8			8			8		ns
Rise Time	+25°C	I			9			9			9			9	ns
Fall Time	+25°C	I			14			14			14			14	ns
Output Time Skew[14]	+25°C	I		4.5	7		4.5	7		4.5	7		4.5	7	ns
NMINV and NLINV INPUTS															
+0.4V Input Current	Full	VI			200			200			200			200	µA
+2.4V Input Current	Full	VI			10			10			10			10	µA
+5.5V Input Current	Full	VI			10			10			10			10	µA
CONVERT INPUT															
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8			0.8			0.8	V
Logic "1" Current	Full	VI			15			15			15			15	µA
Logic "0" Current	Full	VI			500			500			500			500	µA
Input Capacitance	+25°C	III		4	6		4	6		4	6		4	6	pF
Convert Pulse Width (LOW)	+25°C	I	18			18			18			18			ns
Convert Pulse Width (HIGH)	+25°C	I	10			10			10			10			ns

Parameter (Conditions)	Temp	Test Level	AD9048JJ/JQ Min	AD9048JJ/JQ Typ	AD9048JJ/JQ Max	AD9048KJ/KQ Min	AD9048KJ/KQ Typ	AD9048KJ/KQ Max	AD9048SE/SQ Min	AD9048SE/SQ Typ	AD9048SE/SQ Max	AD9048TE/TQ Min	AD9048TE/TQ Typ	AD9048TE/TQ Max	Units
AC LINEARITY															
In-Band Harmonics															
dc to 2.438MHz[15]	+25°C	I	47	50		49	55		47	50		49	55		dBc
dc to 9.35MHz[16]	+25°C	V		48			48			48			48		dBc
Signal-to-Noise Ratio (SNR)[15]															
1.248MHz Input Frequency[17]	+25°C	I	43.5	44		45	46		43.5	44		45	46		dB
2.438MHz Input Frequency[17]	+25°C	I	43	44		44	46		43	44		44	46		dB
1.248MHz Input Frequency[18]	+25°C	I	52.5	53		54	55		52.5	53		54	55		dB
2.438MHz Input Frequency[18]	+25°C	I	52	53		53	55		52	53		53	55		dB
Signal-to-Noise Ratio (SNR)[16]															
1.248MHz Input Frequency[17]	+25°C	I	43.5	44		45	46		43.5	44		45	46		dB
9.35MHz Input Frequency[17]	+25°C	V		40.5			40.5			40.5			40.5		dB
Noise Power Ratio (NPR)[19]	+25°C	III	36.5	39		36.5	39		36.5	39		36.5	39		dB
Differential Phase[20]	+25°C	III			1			1			1			1	Degree
Differential Gain[20]	+25°C	III			2			2			2			2	%
DIGITAL OUTPUTS															
Logic "1" Voltage	Full	VI	2.4			2.4			2.4			2.4			V
Logic "0" Voltage	Full	VI			0.5			0.5			0.5			0.5	V
Short Circuit Current[5]	Full	VI			30			30			30			30	mA
POWER SUPPLY															
Positive Supply Current	+25°C	I		34	46		34	46		34	46		34	46	mA
	Full	VI			48			48			48			48	mA
Negative Supply Current	+25°C	I		90	110		90	110		90	110		90	110	mA
	Full	VI			120			120			120			120	mA
Nominal Power Dissipation	+25°C	V		550			550			550			550		mW
Reference Ladder Dissipation	+25°C	V		45			45			45			45		mW

NOTES

[1]Maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the device may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

[2]Applied voltage must be current-limited to specified range.

[3]Forcing voltage must be limited to specified range.

[4]Current is specified as negative when flowing into the device.

[5]Output High; one pin to ground; one second duration.

[6]Typical thermal impedances (no air flow) are as follows:
Ceramic DIP: $\theta_{JA} = 49°C/W$; $\theta_{JC} = 15°C/W$ LCC: $\theta_{JA} = 69°C/W$; $\theta_{JC} = 21°C/W$
JLCC: $\theta_{JA} = 59°C/W$; $\theta_{JC} = 19°C/W$
To calculate junction temperature (T_J), use power dissipation (PD) and thermal impedance:
$T_J = PD(\theta_{JA}) + T_{AMBIENT} = PD(\theta_{JC}) = + T_{CASE}$

[7]Measured with V_{IN} = 0V and CONVERT low (sampling mode).

[8]Determined by beat frequency testing for no missing codes.

[9]$V_{RT} \geq V_{RB}$ under all circumstances.

[10]Outputs terminated with 40pF and 810Ω pull-up resistors.

[11]Interval from 50% point of leading edge CONVERT pulse to change in output data.

[12]For full scale step input, 8-bit accuracy attained in specified time.

[13]Recovers to 8-bit accuracy in specified time after −3V input overvoltage.

[14]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.

[15]Measured at 20MHz encode rate with analog input 1dB below full scale.

[16]Measured at 35MHz encode rate with analog input 1dB below full scale.

[17]RMS signal to rms noise.

[18]Peak signal to rms noise.

[19]DC to 8MHz noise bandwidth with 1.248MHz slot; four sigma loading; 20MHz encode.

[20]Clock frequency = 4 × NTSC = 14.32MHz. Measured with 40-IRE modulated ramp.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature	Package Option[1]
AD9048JJ	0 to +70°C	J-28
AD9048KJ	0 to +70°C	J-28
AD9048JQ	0 to +70°C	Q-28
AD9048KQ	0 to +70°C	Q-28
AD9048SE[2]	−55°C to +125°C	E-28A
AD9048TE[2]	−55°C to +125°C	E-28A
AD9048SQ[2]	−55°C to +125°C	Q-28
AD9048TQ[2]	−55°C to +125°C	Q-28

NOTES

[1]E = Leadless Ceramic Chip Carrier; J = J-Leaded Ceramic; Q = Cerdip. For outline information see Package Information section.

[2]For specifications, refer to Analog Devices *Military Products Databook*.

EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.

Test Level II – 100% production tested at +25°C and sample tested at specified temperatures.

Test Level III – Sample tested only.

Test Level IV – Parameter is guaranteed by design and characterization testing.

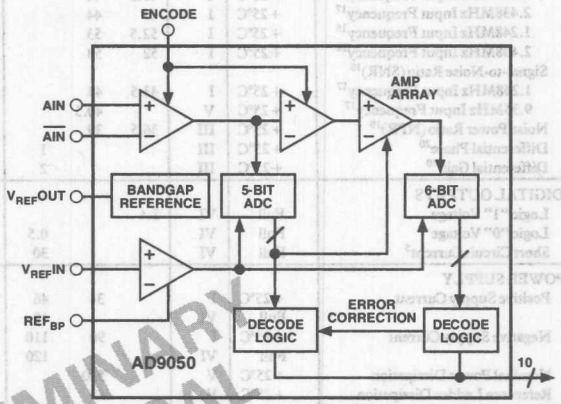
Test Level V – Parameter is a typical value only.

Test Level VI – All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for military temperature devices; sample tested at temperature extremes for commercial/industrial devices.

FEATURES
Low Power: 300 mW
On-Chip T/H, Reference
Single +5 V Power Supply Operation
Selectable 5 V/3 V Outputs
Wide Dynamic Performance

APPLICATIONS
Medical Imaging
Instrumentation
Digital Communications
Professional Video

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

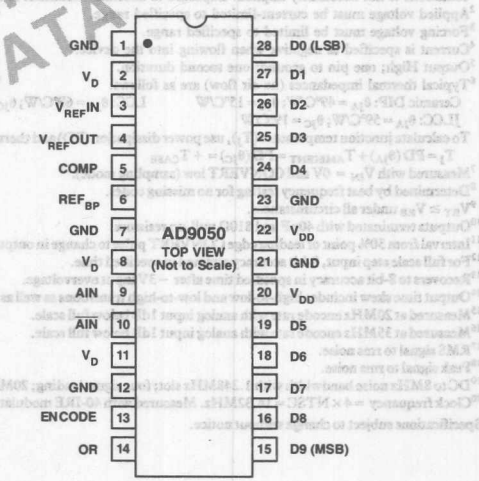
The AD9050 is a complete 10-bit monolithic sampling analog-to-digital converter (ADC) with on-board track-and-hold and reference. The unit is designed for low cost, high performance applications and requires only +5 V and an encode clock to achieve 40 Msps sample rates with 10-bit resolution.

The encode clock is TTL compatible and the digital outputs are 5 V/3 V, selected by the user. The two-step architecture used in the AD9050 is optimized to provide the best dynamic performance available while maintaining low power requirements.

The 2.5 V reference is included on-board, or the user can provide an external reference voltage for gain control, or matching of multiple devices. Fabricated on an advanced BiCMOS process, the AD9050 is packaged in space saving surface mount packages and will be specified over the commercial (0°C to +85°C) temperature range.

PRELIMINARY TECHNICAL DATA

PIN CONNECTIONS



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This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_D, V_{DD} = +5 V; internal reference; ENCODE = 40 Msps unless otherwise noted)

Parameter	Temp	Test Level	AD9050JR/J Min	Typ	Max	Units
RESOLUTION				10		Bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		0.5		LSB
	Full	VI		1.0		LSB
Integral Nonlinearity	+25°C	I		0.5		LSB
	Full	VI		1.0		LSB
No Missing Codes	Full	VI		GNT		
Gain Error	+25°C	I		±0.5		% FS
	Full	VI				% FS
Gain Tempco	Full	V		±70		ppm/°C
ANALOG INPUT						
Input Voltage Range	+25°C	V		1		V p-p
Input Offset Voltage	+25°C	I		±2		mV
	Full	VI				mV
Input Bias Current	+25°C	I		±100		µA
	Full	VI				µA
Input Resistance	+25°C	I	4.0	5.0	6.0	kΩ
Input Capacitance	+25°C	V		5		pF
Analog Bandwidth	+25°C	V		40		MHz
BANDGAP REFERENCE						
Output Voltage	Full	VI	2.4	2.5	2.6	V
Temperature Coefficient	Full	V		±10		ppm/°C
SWITCHING PERFORMANCE						
Maximum Conversion Rate	+25°C	I	40			Msps
Minimum Conversion Rate	+25°C	V		2	10	Msps
Aperture Delay (t_A)	+25°C	V		2		ns
Aperture Uncertainty (Jitter)	+25°C	V		5		ps, rms
Output Propagation Delay (t_{PD})	+25°C	I	2	5		ns
	Full	VI	2			ns
DYNAMIC PERFORMANCE						
Transient Response	+25°C	V		15		ns
Overvoltage Recovery Time	+25°C	V		25		ns
Signal-to-Noise Ratio (SINAD)						
f_{IN} = 2.3 MHz	+25°C	I		57		dB
f_{IN} = 10.3 MHz	+25°C	I		56		dB
Signal-to-Noise Ratio (Without Harmonics)						
f_{IN} = 2.3 MHz	+25°C	I		58		dB
f_{IN} = 10.3 MHz	+25°C	I		57		dB
2nd Harmonic Distortion						
f_{IN} = 2.3 MHz	+25°C	I		67		dBc
f_{IN} = 10.3 MHz	+25°C	I		65		dBc
3rd Harmonic Distortion						
f_{IN} = 2.3 MHz	+25°C	I		75		dBc
f_{IN} = 10.3 MHz	+25°C	I		70		dBc
Two-Tone Intermodulation Distortion (IMD)	+25°C	V		65		dBc
Differential Phase	+25°C	III		0.15		Degrees
Differential Gain	+25°C	III		0.25		%

PRELIMINARY TECHNICAL DATA

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AD9050–SPECIFICATIONS

Parameter	Temp	Test Level	AD9050JR/J Min	Typ	Max	Units
ENCODE INPUT						
Logic "1" Voltage	Full	VI	2.4			V
Logic "0" Voltage	Full	VI			0.4	V
Logic "1" Current	Full	VI			20	μA
Logic "0" Current	Full	VI	–0.4			mA
Input Capacitance	+25°C	V		10		pF
Encode Pulse Width High (t_{EH})	+25°C	IV	10		100	ns
Encode Pulse Width Low (t_{EL})	+25°C	IV	10		100	ns
DIGITAL OUTPUTS						
Logic "1" Voltage	Full	VI	4.95			V
Logic "0" Voltage	Full	VI			0.05	V
Logic "1" Voltage (3.0 V)	Full	VI	2.95			V
Logic "0" Voltage (3.0 V)	Full	VI			0.05	V
Output Coding			Offset	Binary	Code	
POWER SUPPLY						
V_D, V_{DD} Supply Current	Full	VI		60		mA
Power Dissipation	Full	VI		300		mW
Power Supply Rejection Ratio (PSRR)	+25°C	I		±12		mV/V

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

EXPLANATION OF TEST LEVELS

Test Level

I – 100% Production Tested.

III – Sample Tested Only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C.
100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

ABSOLUTE MAXIMUM RATINGS

V_D, V_{DD} ..... +7 V
ANALOG IN ..... –0.5 V to V_D + 0.5 V
Digital Inputs ..... –0.5 V to V_D
V_{REF} Input ..... –0.5 V to V_D
Digital Output Current ..... 20 mA
Operating Temperature
AD9050JR ..... 0°C to +85°C
Storage Temperature ..... –65°C to +150°C

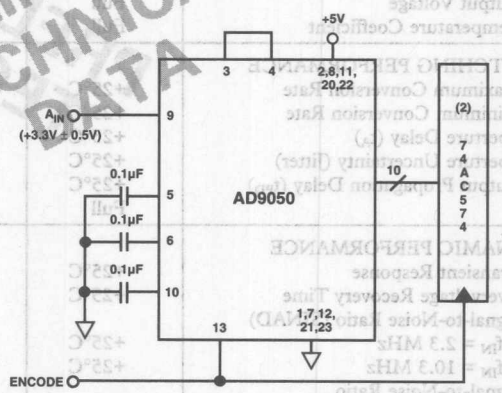


Figure 1. Typical Connections

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9050 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Dual 8-Bit 50 MSPS A/D Converter

AD9058

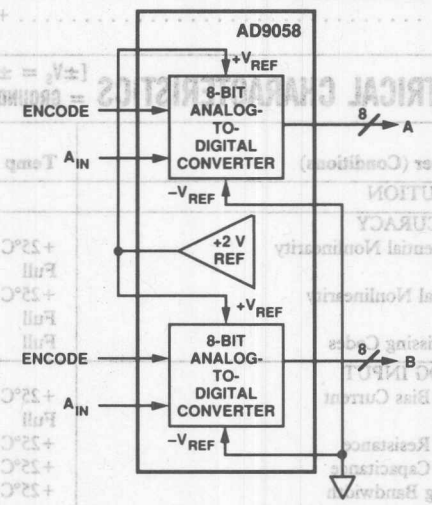
FEATURES

Two Matched ADCs on Single Chip
50 MSPS Conversion Speed
On-Board Voltage Reference
Low Power (<1W)
Low Input Capacitance (10 pF)
±5 V Power Supplies
Flexible Input Range

APPLICATIONS

Quadrature Demodulation for Communications
Digital Oscilloscopes
Electronic Warfare
Radar

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

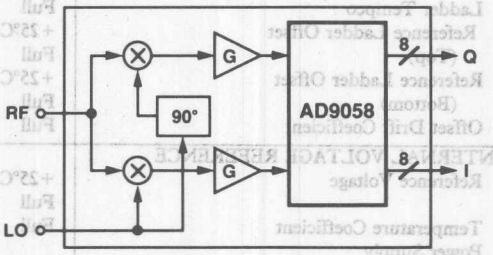
The AD9058 combines two independent high performance 8-bit analog-to-digital converters (ADCs) on a single monolithic IC. Combined with an optional on-board voltage reference, the AD9058 provides a cost effective alternative for systems requiring two or more ADCs.

Dynamic performance (SNR, ENOB) is optimized to provide up to 50 MSPS conversion rates. The unique architecture results in low input capacitance while maintaining high performance and low power (<0.5 watt/channel). Digital inputs and outputs are TTL compatible.

Performance has been optimized for an analog input of 2 V p–p (±1 V; 0 to +2 V). Using the on-board +2 V voltage reference, the AD9058 can be set up for unipolar positive operation (0 to +2 V). This internal voltage reference can drive both ADCs.

Commercial (0°C to +70°C) and military (−55°C to +125°C) temperature range parts are available. Parts are supplied in hermetic 48-pin DIP and 44-pin "J" lead packages.

QUADRATURE RECEIVER



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9058—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Analog Input . . . . . −1.5 V to +2.5 V
$+V_S$ . . . . . +6 V
$-V_S$ . . . . . +0.8 V to −6 V[2]
Digital Inputs . . . . . −0.5 V to $+V_S$
Digital Output Current . . . . . 20 mA
Voltage Reference Current . . . . . 53 mA
$+V_{REF}$ . . . . . +2.5 V
$-V_{REF}$ . . . . . −1.5
Operating Temperature Range
AD9058JD/JJ/KD/KJ . . . . . 0°C to +70°C
Maximum Junction Temperature[3]
AD9058JD/JJ/KD/KJ . . . . . +175°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS

[$\pm V_S = \pm 5$ V; $V_{REF} = +2$ V (internal); ENCODE = 40 MSPS; $A_{IN} = 0$ V to +2 V; $-V_{REF}$ = GROUND, unless otherwise noted.][2] All specifications apply to either of the two ADCs.

Parameter (Conditions)	Temp	Test Level	AD9058JD/JJ Min	AD9058JD/JJ Typ	AD9058JD/JJ Max	AD9058KD/KJ Min	AD9058KD/KJ Typ	AD9058KD/KJ Max	Units
RESOLUTION			8			8			Bits
DC ACCURACY									
Differential Nonlinearity	+25°C	I		0.25	0.65		0.25	0.5	LSB
	Full	VI			0.8			0.7	LSB
Integral Nonlinearity	+25°C	I		0.5	1.3		0.5	1.0	LSB
	Full	VI			1.4			1.25	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			
ANALOG INPUT									
Input Bias Current	+25°C	I		75	170		75	170	μA
	Full	VI			340			340	μA
Input Resistance	+25°C	I	12	28		12	28		kΩ
Input Capacitance	+25°C	IV		10	15		10	15	pF
Analog Bandwidth	+25°C	V		175			175		MHz
REFERENCE INPUT									
Reference Ladder Resistance	+25°C	I	120	170	220	120	170	220	Ω
	Full	VI	80		270	80		270	Ω
Ladder Tempco	Full	V		0.45			0.45		Ω/°C
Reference Ladder Offset	+25°C	I		8	16		8	16	mV
(Top)	Full	VI			24			24	mV
Reference Ladder Offset	+25°C	I		8	23		8	23	mV
(Bottom)	Full	VI			33			33	mV
Offset Drift Coefficient	Full	V		50			50		μV/°C
INTERNAL VOLTAGE REFERENCE									
Reference Voltage	+25°C	I	1.95	2.0	2.20	1.95	2.0	2.20	V
	Full	VI	1.90		2.25	1.90		2.25	V
Temperature Coefficient	Full	V		150			150		μV/°C
Power Supply									
Rejection Ratio (PSRR)	+25°C	I		10	25		10	25	mV/V
SWITCHING PERFORMANCE									
Maximum Conversion Rate[4]	+25°C	I		50		50	60		MSPS
Aperture Delay (t_A)	+25°C	IV	0.1	0.8	1.5	0.1	0.8	1.5	ns
Aperture Delay Matching	+25°C	IV		0.2	0.5		0.2	0.5	ns
Aperture Uncertainty (Jitter)	+25°C	V		10			10		ps, rms
Output Delay (Valid) (t_V)[4]	+25°C	I		8		5	8		ns
Output Delay (t_V) Tempco	Full	V		16			16		ps/°C
Propagation Delay (t_{PD})[4]	+25°C	I		12			12	19	ns
Propagation Delay (t_{PD}) Tempco	Full	V		−16			−16		ps/°C
Output Time Skew	+25°C	V		1			1		ns
ENCODE INPUT									
Logic "1" Voltage	Full	VI	2			2			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			600			600	μA
Logic "0" Current	Full	VI			1000			1000	μA
Input Capacitance	+25°C	V		5			5		pF
Pulse Width (High)	+25°C	I		8		8			ns
Pulse Width (Low)	+25°C	I		8		8			ns

Parameter (Conditions)	Temp	Test Level	AD9058JD/JJ Min	AD9058JD/JJ Typ	AD9058JD/JJ Max	AD9058KD/KJ Min	AD9058KD/KJ Typ	AD9058KD/KJ Max	Units
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		2			2		ns
Overvoltage Recovery Time	+25°C	V		2			2		ns
Effective Number of Bits (ENOB)[5]									
Analog Input @ 2.3 MHz	+25°C	I		7.7		7.2	7.7		Bits
@ 10.3 MHz	+25°C	I		7.4		7.1	7.4		Bits
Signal-to-Noise Ratio[5]									
Analog Input @ 2.3 MHz	+25°C	I		48		45	48		dB
@ 10.3 MHz	+25°C	I		46		44	46		dB
Signal-to-Noise Ratio[5] (Without Harmonics)									
Analog Input @ 2.3 MHz	+25°C	I		48		46	48		dB
@ 10.3 MHz	+25°C	I		47		45	47		dB
2nd Harmonic Distortion									
Analog Input @ 2.3 MHz	+25°C	I		58		48	58		dBc
@ 10.3 MHz	+25°C	I		58		48	58		dBc
3rd Harmonic Distortion									
Analog Input @ 2.3 MHz	+25°C	I		58		50	58		dBc
@ 10.3 MHz	+25°C	I		58		50	58		dBc
Crosstalk Rejection[6]	+25°C	IV		60		48	60		dBc
DIGITAL OUTPUTS									
Logic "1" Voltage (I_{OH} = 2 mA)	Full	VI	2.4			2.4			V
Logic "0" Voltage (I_{OL} = 2 mA)	Full	VI			0.4			0.4	V
POWER SUPPLY[7]									
$+V_S$ Supply Current	Full	VI		127	154		127	154	mA
$-V_S$ Supply Current	Full	VI		27	38		27	38	mA
Power Dissipation	Full	VI		770	960		770	960	mW

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]For applications in which $+V_S$ may be applied before $-V_S$, or $+V_S$ current is not limited to 500 mA, a reverse biased clamping diode should be inserted between ground and $-V_S$ to prevent destructive latch up. See section entitled "Using the AD9058."

[3]Typical thermal impedances: 44-pin hermetic J-Leaded ceramic package: θ_{JA} = 86.4°C/W; θ_{JC} = 24.9°C/W; 48-pin hermetic DIP θ_{JA} = 40°C/W; θ_{JC} = 12°C/W.

[4]To achieve guaranteed conversion rate, connect each data output to ground through a 2 kΩ pull-down resistor.

[5]SNR performance limits for the 48-pin DIP "D" package are 1 dB less than shown. ENOB limits are degraded by 0.3 dB. SNR and ENOB measured with analog input signal 1 dB below full scale at specified frequency.

[6]Crosstalk rejection measured with full-scale signals of different frequencies (2.3 MHz and 3.5 MHz) applied to each channel. With both signals synchronously encoded at 40 MSPS, isolation of the undesired frequency is measured with an FFT.

[7]Applies to both A/Ds and includes internal ladder dissipation.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD9058JJ	0°C to +70°C	44-Pin J-Leaded Ceramic†	J-44
AD9058KJ	0°C to +70°C	44-Pin J-Leaded Ceramic, AC Tested	J-44
AD9058TJ/883#	−55°C to +125°C	44-Pin J-Leaded Ceramic, AC Tested	J-44
AD9058JD	0°C to +70°C	48-Pin Ceramic DIP	D-48
AD9058KD	0°C to +70°C	48-Pin Ceramic DIP, AC Tested	D-48
AD9058TD/883#	−55°C to +125°C	48-Pin Ceramic DIP, AC Tested	D-48
AD9058/PCB	0°C to +70°C	AD9058 Evaluation Board (J-Lead)	

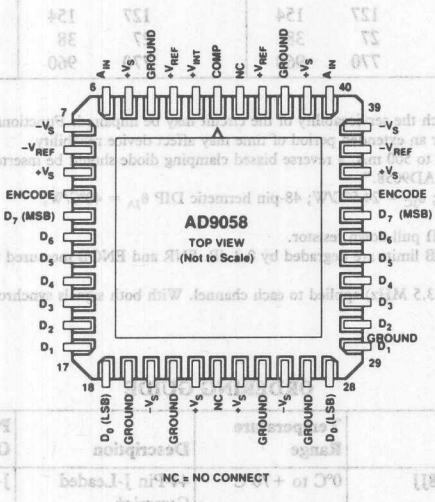
*D = Hermetic Ceramic DIP Package; J = Leaded Ceramic Package. For outline information see Package Information section.

†Hermetically sealed ceramic package; footprint equivalent to PLCC.

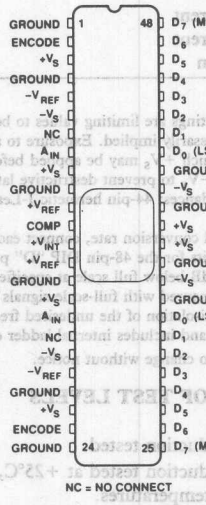
#For specifications, refer to Analog Devices Military Products Databook.

PIN DESCRIPTIONS

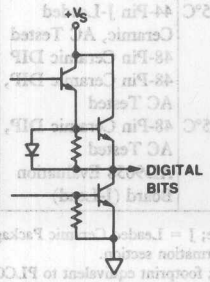
J-Lead Pin Number ADC-A	J-Lead Pin Number ADC-B	Name	Function	Ceramic DIP Pin Number ADC-A	Ceramic DIP Pin Number ADC-B
3	43	$+V_{REF}$	Top of internal voltage reference ladder.	14	11
4	42	GROUND	Analog ground return.	15	10
5	41	$+V_S$	Positive 5 V analog supply voltage.	16	9
6	40	AIN	Analog input voltage.	17	8
7	39	$-V_S$	Negative 5 V supply voltage.	19	6
8	38	$-V_{REF}$	Bottom of internal voltage reference ladder.	20	5
9	37	$+V_S$	Positive 5 V digital supply voltage.	22	3
10	36	ENCODE	TTL compatible convert command.	23	2
11	35	D7 (MSB)	Most significant bit of TTL digital output.	25	48
12–17	34–29	D6–D1	TTL compatible digital output bits.	26–31	47–42
18	28	D0 (LSB)	Least significant bit of TTL digital output.	32	41
19	27	GROUND	Digital ground return.	21, 24, 33	1, 4, 40
20	26	$-V_S$	Negative 5 V supply voltage.	34	39
21	25	GROUND	Analog ground return.	35	38
22	24	$+V_S$	Positive 5 V analog supply voltage.	36	37
COMMON PINS				COMMON PINS	
1		COMP	Connection for external (0.1 μF) compensation capacitor.	12	
2		$+V_{INT}$	Internal +2 V reference; can drive $+V_{REF}$ for both ADCs.	13	



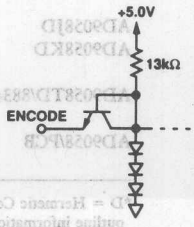
AD9058JJ/KJ Pinouts



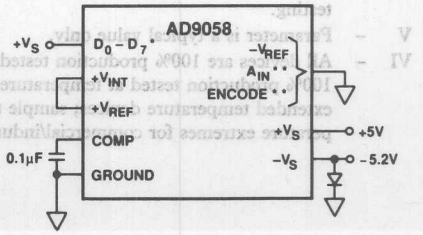
AD9058JD/KD Pinouts



AD9058 Equivalent Digital Outputs



AD9058 Equivalent Encode Circuit



*INDICATES EACH PIN IS CONNECTED THRU 2 kΩ
**INDICATES EACH PIN IS CONNECTED THROUGH 100 Ω

AD9058 Burn-In Connections

10-Bit 75 MSPS A/D Converter

AD9060

2

FEATURES

- Monolithic 10-Bit/75 MSPS Converter
- ECL Outputs
- Bipolar (±1.75 V) Analog Input
- 57 dB SNR @ 2.3 MHz Input
- Low (45 pF) Input Capacitance
- MIL-STD-883 Compliant Versions Available

APPLICATIONS

- Digital Oscilloscopes
- Medical Imaging
- Professional Video
- Radar Warning/Guidance Systems
- Infrared Systems

GENERAL DESCRIPTION

The AD9060 A/D converter is a 10-bit monolithic converter capable of word rates of 75 MSPS and above. Innovative architecture using 512 input comparators instead of the traditional 1024 required by other flash converters reduces input capacitance and improves linearity.

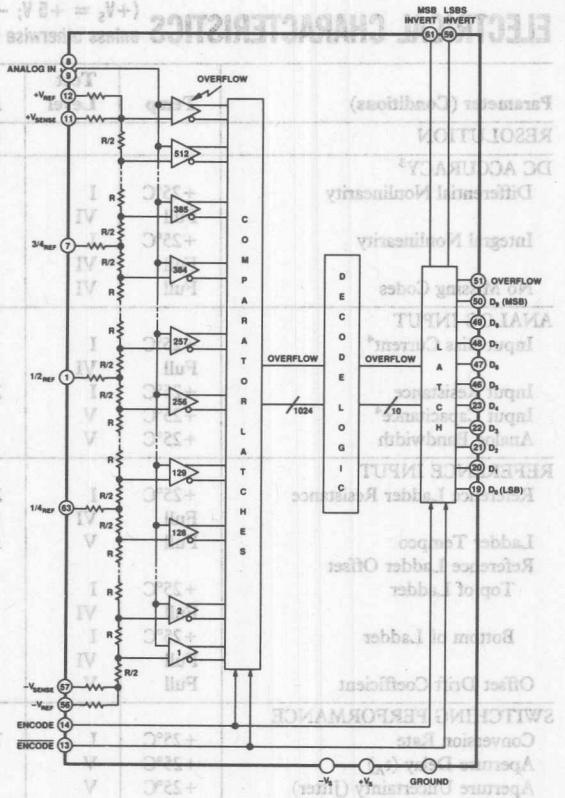
Inputs and outputs are ECL-compatible, which makes the AD9060 the recommended choice for systems with conversion rates >30 MSPS, to minimize system noise. An overflow bit is provided to indicate analog input signals greater than $+V_{SENSE}$.

Voltage sense lines are provided to insure accurate driving of the $\pm V_{REF}$ voltages applied to the units. Quarter-point taps on the resistor ladder help optimize the integral linearity of the unit.

Either 68-pin ceramic leaded (gull wing) packages or ceramic LCCs are available and are specifically designed for low thermal impedances. Two performance grades for temperatures of both 0 to +70°C and −55°C to +125°C ranges are offered to allow the user to select the linearity best suited for each application. Dynamic performance is fully characterized and production tested at +25°C. MIL-STD-883 units are available.

The AD9060 A/D converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9060/883B data sheet for detailed specifications.

FUNCTIONAL BLOCK DIAGRAM



ORDERING GUIDE

Device	Temperature Range	Package Option[1]
AD9060JZ	0 to +70°C	Z-68
AD9060JE	0 to +70°C	E-68A
AD9060KZ	0 to +70°C	Z-68
AD9060KE	0 to +70°C	E-68A
AD9060SZ[2]	−55°C to +125°C	Z-68
AD9060SE[2]	−55°C to +125°C	E-68A
AD9060TZ[2]	−55°C to +125°C	Z-68
AD9060TE[2]	−55°C to +125°C	E-68A
AD9060/PCB	0 to +70°C	Evaluation Board

NOTES
[1]E = Ceramic Leadless Chip Carrier; Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9060—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6 V
$-V_S$	−6 V
ANALOG IN	−2 V to +2 V
$+V_{REF}$, $-V_{REF}$, $3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$	−2 V to +2 V
$+V_{REF}$ to $-V_{REF}$	4.0 V
ENCODE, $\overline{\text{ENCODE}}$	0 V to $-V_S$
$3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$ Current	±10 mA
Digital Output Current	20 mA
Operating Temperature	
AD9060JE/KE/JZ/KZ	0 to +70°C
Storage Temperature	−65°C to +150°C
Maximum Junction Temperature[2]	+175°C
Lead Soldering Temp (10 sec)	+300°C

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = −5.2 V; $\pm V_{SENSE}$ = ±1.75 V; ENCODE = 60 MSPS unless otherwise noted)[3]

Parameter (Conditions)	Temp	Test Level	AD9060JE/JZ Min	AD9060JE/JZ Typ	AD9060JE/JZ Max	AD9060KE/KZ Min	AD9060KE/KZ Typ	AD9060KE/KZ Max	Units
RESOLUTION			10			10			Bits
DC ACCURACY[3]									
Differential Nonlinearity	+25°C	I		1.0	1.25		0.75	1.0	LSB
	Full	VI			1.5			1.25	LSB
Integral Nonlinearity	+25°C	I		1.25	2.0		1.0	1.5	LSB
	Full	VI			2.5			2.0	LSB
No Missing Codes	Full	VI					Guaranteed		
ANALOG INPUT									
Input Bias Current[4]	+25°C	I		0.4	1.0		0.4	1.0	mA
	Full	VI			2.0			2.0	mA
Input Resistance	+25°C	I	2.0	7.0		2.0	7.0		kΩ
Input Capacitance[4]	+25°C	V		45			45		pF
Analog Bandwidth	+25°C	V		175			175		MHz
REFERENCE INPUT									
Reference Ladder Resistance	+25°C	I	22	37	56	22	37	56	Ω
	Full	VI	14		66	14		66	Ω
Ladder Tempco	Full	V		0.1			0.1		Ω/°C
Reference Ladder Offset									
Top of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Bottom of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Offset Drift Coefficient	Full	V		50			50		µV/°C
SWITCHING PERFORMANCE									
Conversion Rate	+25°C	I	75			75			MSPS
Aperture Delay (t_A)	+25°C	V		1			1		ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5		ps, rms
Output Delay (t_{OD})[5]	+25°C	I	2	4	9	2	4	9	ns
Output Rise Time	+25°C	I		1	3		1	3	ns
Output Fall Time	+25°C	I		1	3		1	3	ns
Output Time Skew[5]	+25°C	I		1.5	3		1.5	3	ns
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		10			10		ns
Overvoltage Recovery Time	+25°C	V		10			10		ns
Effective Number of Bits (ENOB)									
f_{IN} = 2.3 MHz	+25°C	I	8.7	9.1		8.7	9.1		Bits
f_{IN} = 10.3 MHz	+25°C	IV	8.0	8.6		8.0	8.6		Bits
f_{IN} = 29.3 MHz	+25°C	IV	7.0	7.4		7.0	7.4		Bits
Signal-to-Noise Ratio[6]									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	I	51	54		51	54		dB
f_{IN} = 29.3 MHz	+25°C	I	44	47		44	47		dB

Parameter (Conditions)	Temp	Test Level	AD9060JE/JZ Min	AD9060JE/JZ Typ	AD9060JE/JZ Max	AD9060KE/KZ Min	AD9060KE/KZ Typ	AD9060KE/KZ Max	Units
DYNAMIC PERFORMANCE (CONTINUED)									
Signal-to-Noise Ratio[6] (Without Harmonics)									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	58		dB
f_{IN} = 10.3 MHz	+25°C	I	51	55		51	55		dB
f_{IN} = 29.3 MHz	+25°C	I	46	48		46	48		dB
Harmonic Distortion									
f_{IN} = 2.3 MHz	+25°C	I	61	65		61	65		dBc
f_{IN} = 10.3 MHz	+25°C	I	55	58		55	58		dBc
f_{IN} = 29.3 MHz	+25°C	I	47	50		47	50		dBc
Two-Tone Intermodulation Distortion Rejection[7]	+25°C	V		70			70		dBc
Differential Phase	+25°C	V		0.5			0.5		Degree
Differential Gain	+25°C	V		1			1		%
ENCODE INPUT									
Logic "1" Voltage	Full	VI	−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5	V
Logic "1" Current	Full	VI		150	300		150	300	μA
Logic "0" Current	Full	VI		150	300		150	300	μA
Input Capacitance	+25°C	V		5			5		pF
Pulse Width (High)	+25°C	I	6			6			ns
Pulse Width (Low)	+25°C	I	6			6			ns
DIGITAL OUTPUTS									
Logic "1" Voltage	Full	VI	−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5	V
POWER SUPPLY									
$+V_S$ Supply Current	+25°C	VI		420	500		420	500	mA
	Full	VI			500			500	mA
$-V_S$ Supply Current	+25°C	VI		150	180		150	180	mA
	Full	VI			190			190	mA
Power Dissipation	+25°C	VI		2.8	3.3		2.8	3.3	W
	Full	VI			3.5			3.5	W
Power Supply Rejection Ratio (PSRR)[8]	Full	VI		6	10		6	10	mV/V

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances (part soldered onto board): 68-pin leaded ceramic chip carrier: θ_{JC} = 1°C/W; θ_{JA} = 17°C/W (no air flow); θ_{JA} = 15°C/W (air flow = 500 LFM). 68-pin ceramic LCC: θ_{JC} = 2.6°C/W; θ_{JA} = 15°C/W (no air flow); θ_{JA} = 13°C/W (air flow = 500 LFM).

[3]$3/4_{REF}$, $1/2_{REF}$, and $1/4_{REF}$ reference ladder taps are driven from dc sources at +0.875 V, 0 V, and −0.875 V, respectively. Outputs terminated through 100 Ω to −2.0 V; C_L < 4 pF. Accuracy of the overflow comparator is not tested and not included in linearity specifications.

[4]Measured with ANALOG IN = $+V_{SENSE}$.

[5]Output delay measured as worst-case time from 50% point of the rising edge of ENCODE to 50% point of the slowest rising or falling edge of D_0–D_9. Output skew measured as worst-case difference in output delay among D_0–D_9.

[6]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

[7]Intermodulation measured with analog input frequencies of 2.3 MHz and 3.0 MHz at 7 dB below full scale.

[8]Measured as the ratio of the worst-case change in transition voltage of a single comparator for a 5% change in $+V_S$ or $-V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

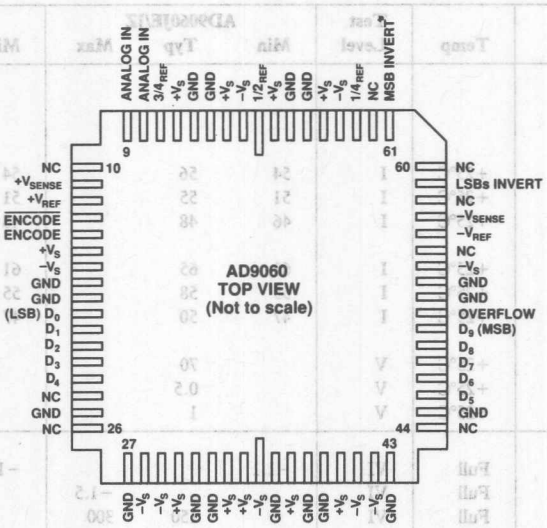
II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



AD9060 Pin Designations

AD9060 PIN DESCRIPTIONS

Pin No.	Name	Function
1	$1/2_{REF}$	Midpoint of internal reference ladder.
2, 16, 28, 29, 35, 41, 42, 54, 64	$-V_S$	Negative supply voltage; nominally −5.2 V ±5%.
3, 6, 15, 30, 33, 34, 37, 40, 65, 68	$+V_S$	Positive supply voltage; nominally +5 V ±5%.
4, 5, 17, 18, 25, 27, 31, 32, 36, 38, 39, 43, 45, 52, 53, 66, 67	GROUND	All ground pins should be connected together and to low-impedance ground plane.
7	$3/4_{REF}$	Three-quarter point of internal reference ladder.
8, 9	ANALOG IN	Analog input; nominally between ±1.75 V.
11	$+V_{SENSE}$	Voltage sense line to most positive point on internal resistor ladder. Normally +1.75 V.
12	$+V_{REF}$	Voltage force connection for top of internal reference ladder. Normally driven to provide +1.75 V at $+V_{SENSE}$.
13	$\overline{\text{ENCODE}}$	Differential ECL convert signal which starts digitizing process.
14	ENCODE	ECL-compatible convert command used to begin digitizing process.
19–23, 46–50	D_0–D_9	ECL-compatible digital output data.
51	OVERFLOW	ECL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
56	$-V_{REF}$	Voltage force connection for bottom of internal reference ladder. Normally driven to provide −1.75 V at $-V_{SENSE}$.
57	$-V_{SENSE}$	Voltage sense line to most negative point on internal resistor ladder. Normally −1.75 V.
59	LSBs INVERT	Normally grounded. When connected to $+V_S$, lower order bits (D_0–D_8) are inverted. Not ECL-compatible.
61	MSB INVERT	Normally grounded. When connected to $+V_S$, most significant bit (MSB; D_9) is inverted. Not ECL-compatible.
63	$1/4_{REF}$	One-quarter point of internal reference ladder.

D/A Converters
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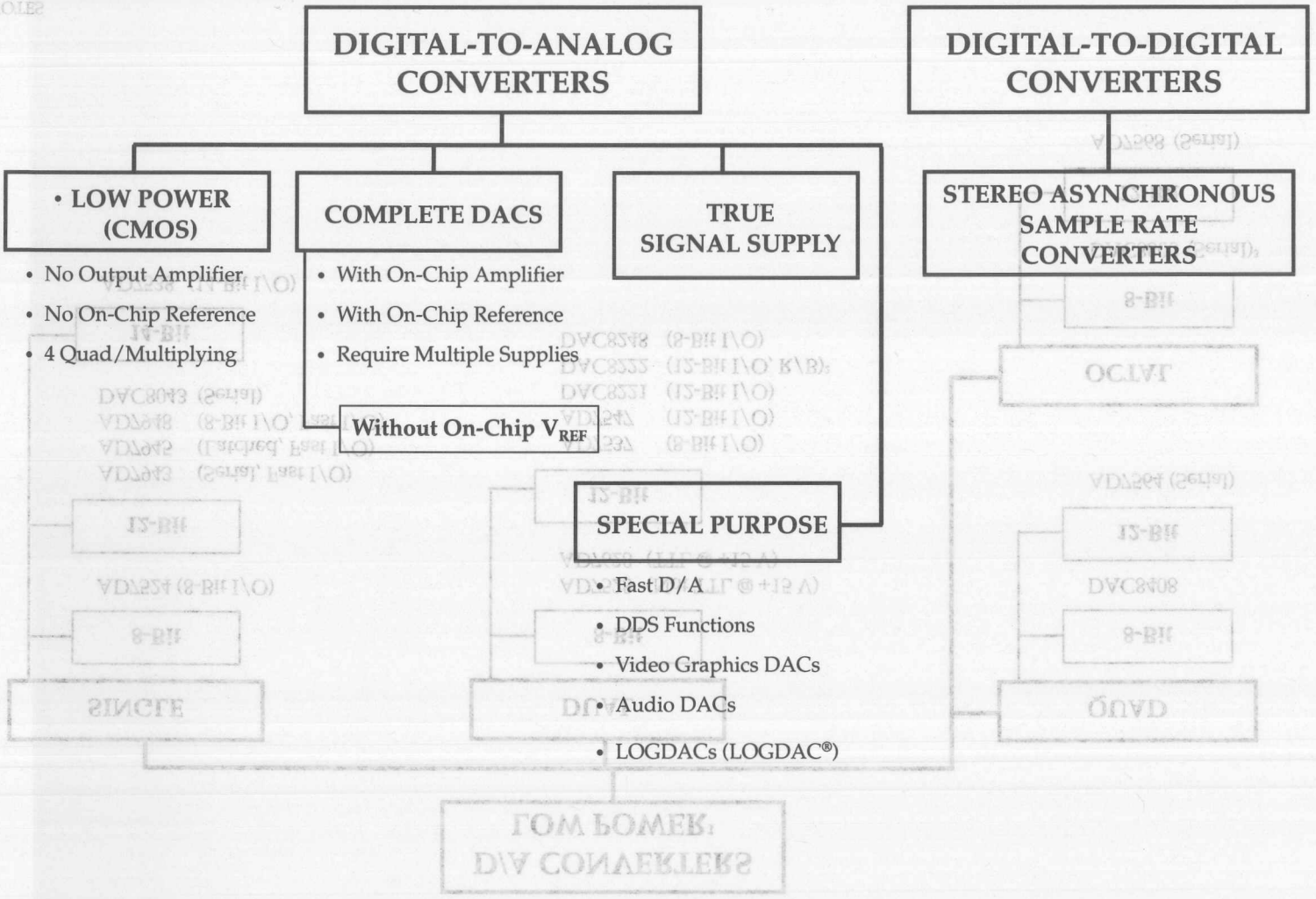
Selection Trees — Digital-to-Analog Converters



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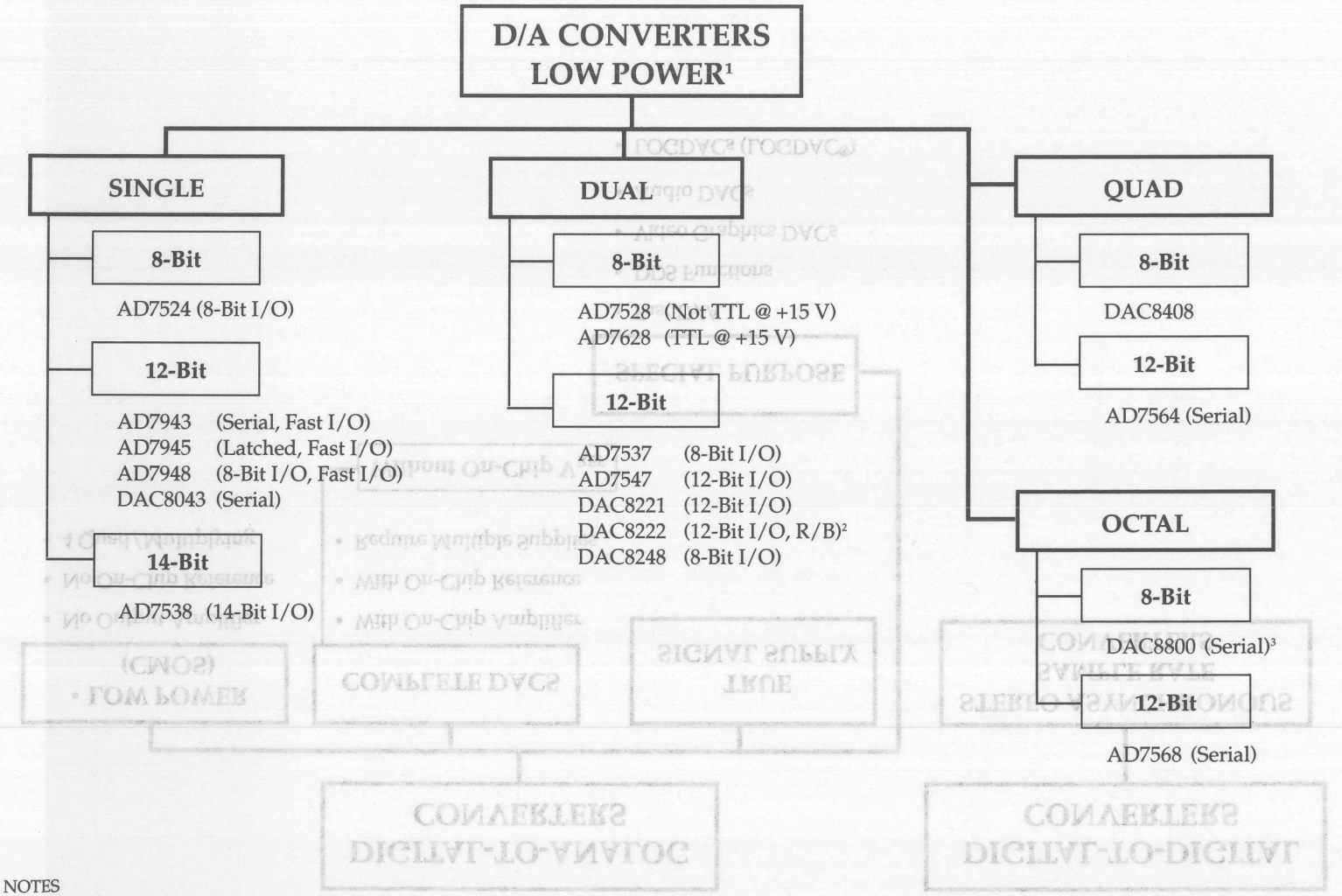
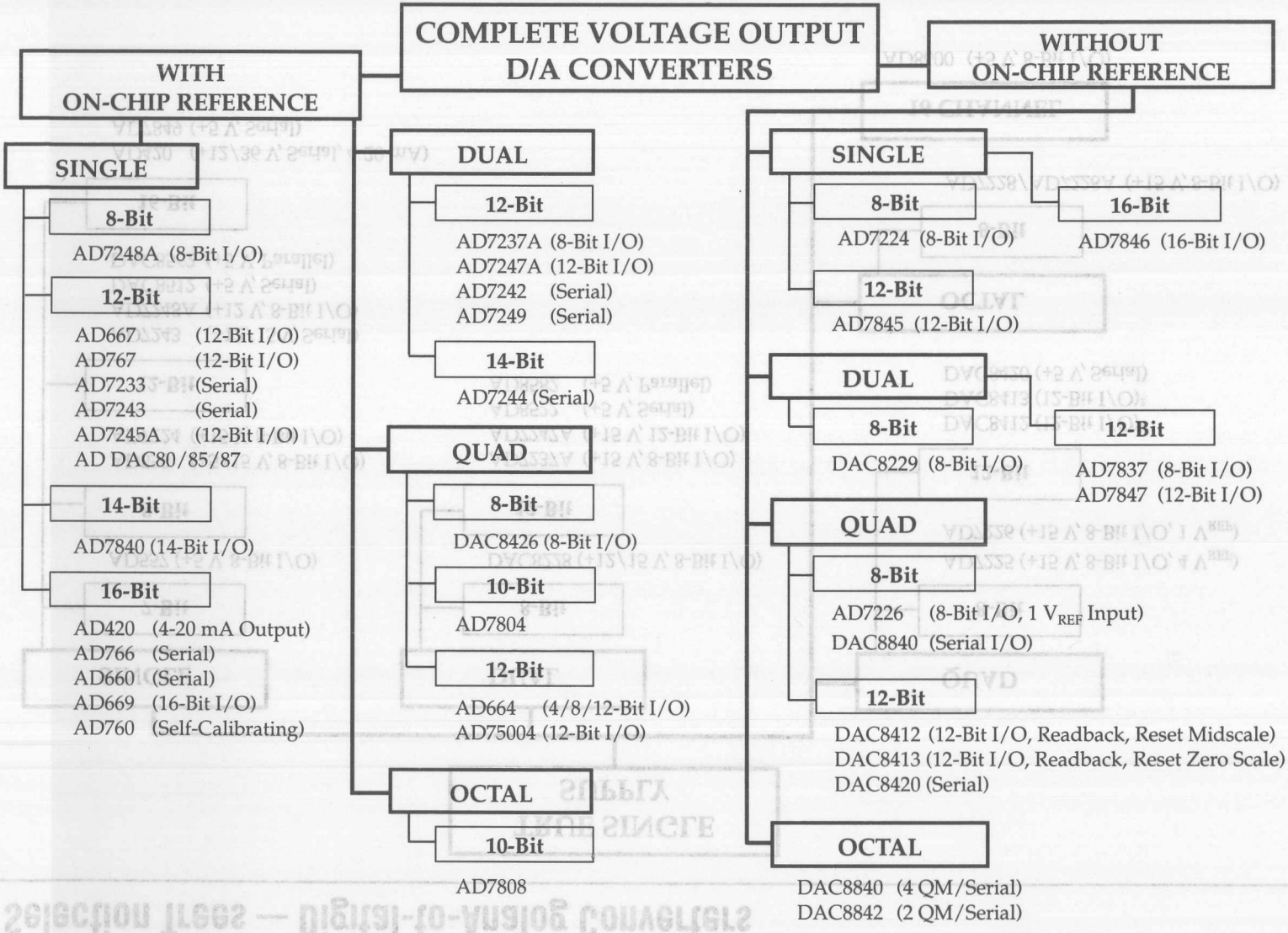
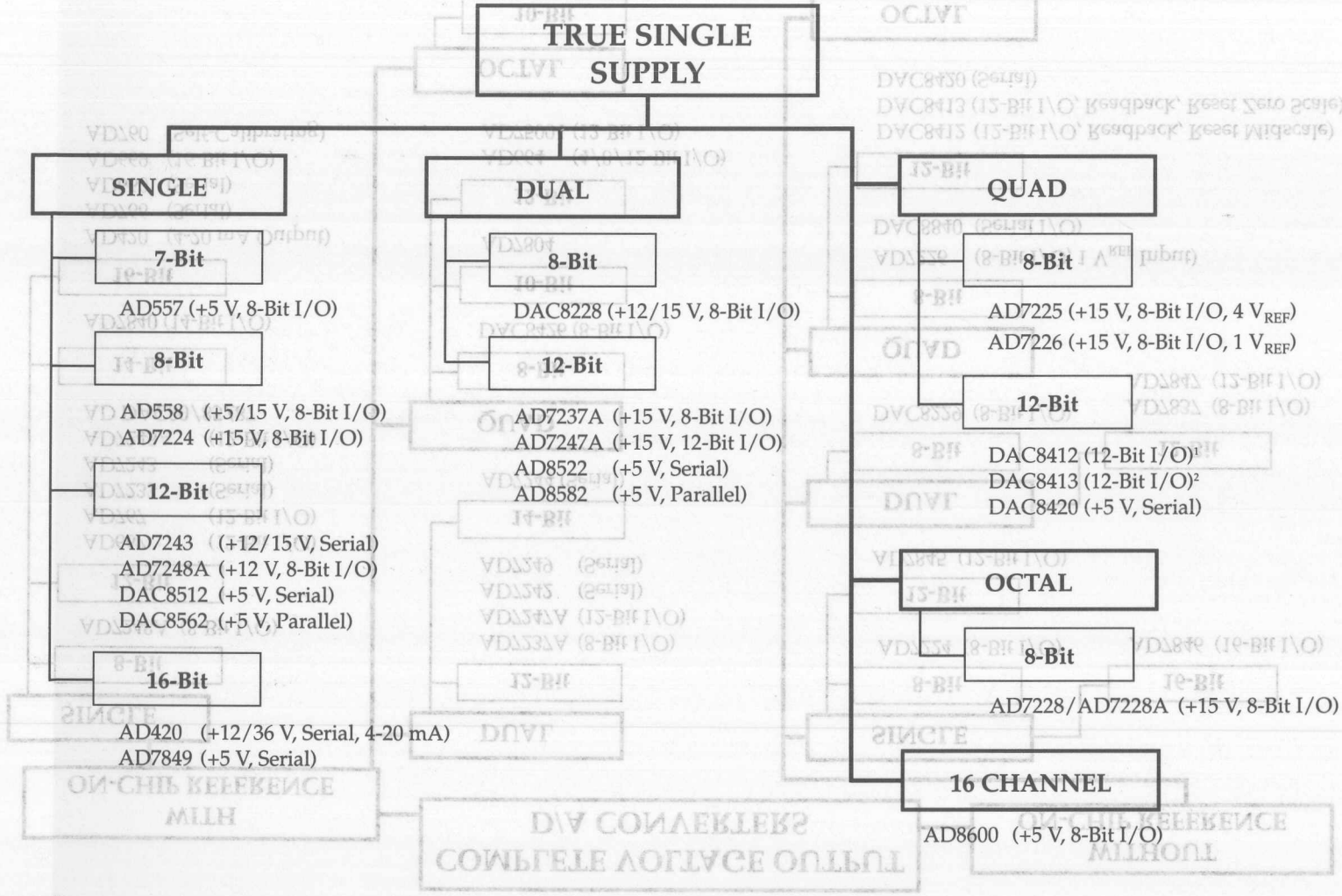
Selection Trees — Digital-to-Analog Converters



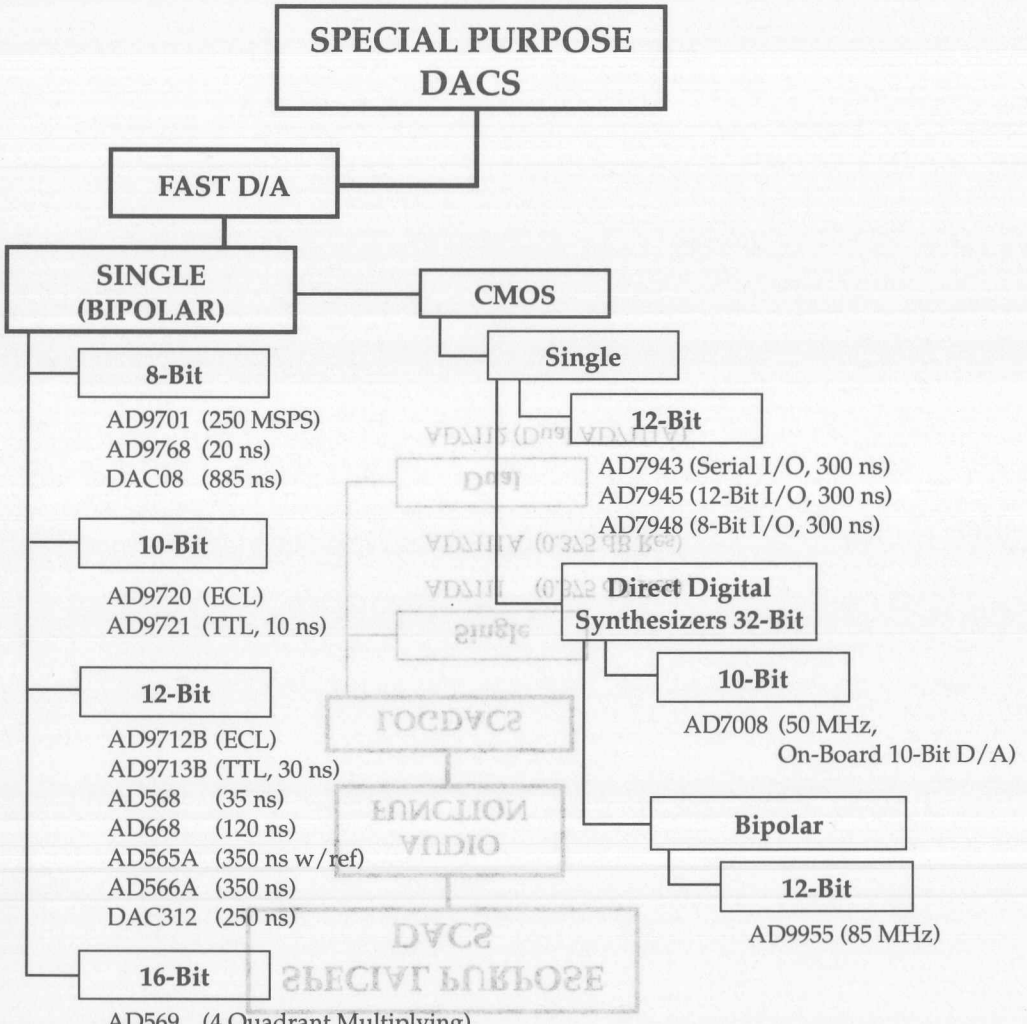
NOTES
[1]All are inverted R/2R ladders, except as noted.
[2]R/B = Readback feature.
[3]Voltage switching ladder.


COMPLETE VOLTAGE OUTPUT D/A CONVERTERS
WITH ON-CHIP REFERENCE
SINGLE
8-Bit
AD7248A (8-Bit I/O)
12-Bit
AD667 (12-Bit I/O)
AD767 (12-Bit I/O)
AD7233 (Serial)
AD7243 (Serial)
AD7245A (12-Bit I/O)
AD DAC80/85/87
14-Bit
AD7840 (14-Bit I/O)
16-Bit
AD420 (4-20 mA Output)
AD766 (Serial)
AD660 (Serial)
AD669 (16-Bit I/O)
AD760 (Self-Calibrating)
DUAL
12-Bit
AD7237A (8-Bit I/O)
AD7247A (12-Bit I/O)
AD7242 (Serial)
AD7249 (Serial)
14-Bit
AD7244 (Serial)
QUAD
8-Bit
DAC8426 (8-Bit I/O)
10-Bit
AD7804
12-Bit
AD664 (4/8/12-Bit I/O)
AD75004 (12-Bit I/O)
OCTAL
10-Bit
AD7808
WITHOUT ON-CHIP REFERENCE
SINGLE
8-Bit
AD7224 (8-Bit I/O)
16-Bit
AD7846 (16-Bit I/O)
12-Bit
AD7845 (12-Bit I/O)
DUAL
8-Bit
DAC8229 (8-Bit I/O)
12-Bit
AD7837 (8-Bit I/O)
AD7847 (12-Bit I/O)
QUAD
8-Bit
AD7226 (8-Bit I/O, 1 V_{REF} Input)
DAC8840 (Serial I/O)
12-Bit
DAC8412 (12-Bit I/O, Readback, Reset Midscale)
DAC8413 (12-Bit I/O, Readback, Reset Zero Scale)
DAC8420 (Serial)
OCTAL
DAC8840 (4 QM/Serial)
DAC8842 (2 QM/Serial)

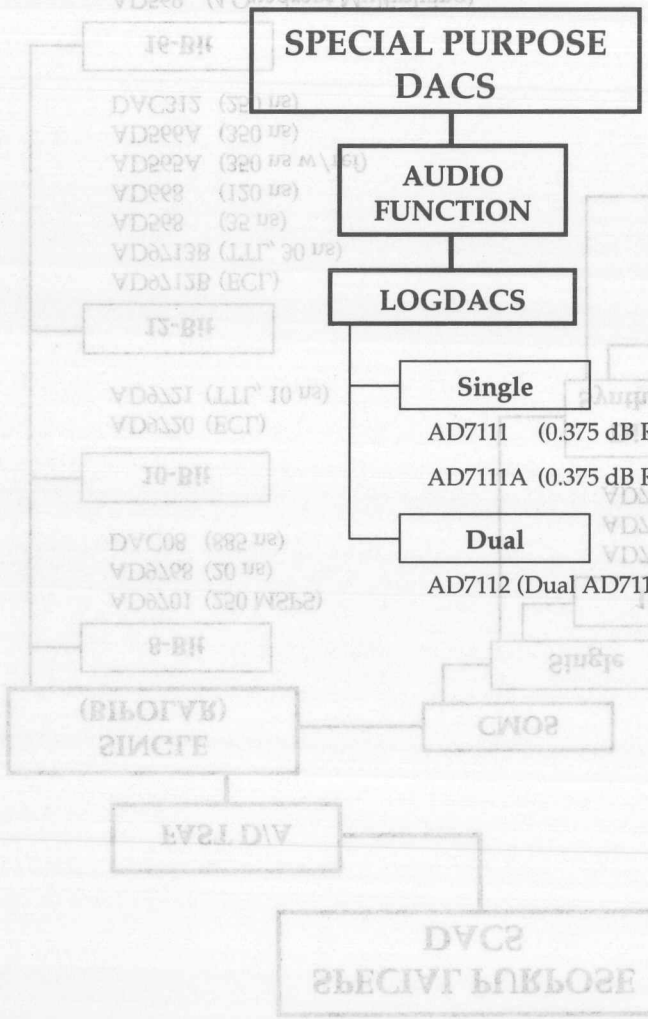
Selection Trees — Digital-to-Analog Converters



NOTES
[1]Readback, reset to midscale
[2]Readback, reset to zero scale


SPECIAL PURPOSE DACS
FAST D/A
SINGLE (BIPOLAR)
CMOS
8-Bit
AD9701 (250 MSPS)
AD9768 (20 ns)
DAC08 (885 ns)
10-Bit
AD9720 (ECL)
AD9721 (TTL, 10 ns)
12-Bit
AD9712B (ECL)
AD9713B (TTL, 30 ns)
AD568 (35 ns)
AD668 (120 ns)
AD565A (350 ns w/ref)
AD566A (350 ns)
DAC312 (250 ns)
16-Bit
AD569 (4 Quadrant Multiplying)
AD768 (35 MSPS, Low Glitch)
DAC16 (300 ns)
Single
12-Bit
AD7943 (Serial I/O, 300 ns)
AD7945 (12-Bit I/O, 300 ns)
AD7948 (8-Bit I/O, 300 ns)
Direct Digital Synthesizers 32-Bit
10-Bit
AD7008 (50 MHz, On-Board 10-Bit D/A)
Bipolar
12-Bit
AD9955 (85 MHz)

Selection Trees — Digital-to-Analog Converters



Selection Guides—Digital-to-Analog Converters

Single DACs, Voltage Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Ranges[4]	Comments	Page[5]
AD557	**8**	**0.8**	**8, µP**	**Int**	**N, P**	**C**	**Lowest Cost 8-Bit DACPORT®; Single +5 V Supply**	**3–24**
AD7569	8	1.0	8, µP	Int	E, N, P, Q, R	C, I, $M/_D$	CMOS, Complete 8-Bit DAC/ADC/SHA/Reference	CII 8–7
AD558	**8**	**3.0**	**8, µP**	**Int**	**D, E, N, P**	**C, $M/_D$**	**10 V Out DACPORT, Single or Dual Supply**	**3–26**
AD7224	**8**	**5.0 (max)**	**8, µP**	**2–12.5 V, Ext**	**E, N, P, Q, R**	**C, I, $M/_S$**	**CMOS, Low Cost 8-Bit DAC**	**3–107**
AD7848	12	2.5	12, µP	Int (+3 V), Ext	N, P, Q	C, I	CMOS, Complete 12-Bit DAC with 8-Word FIFO	CI 2–735
AD7845	**12**	**2.5**	**12, µP**	**Ext (M)**	**E, N, P, Q, R**	**C, I, $M/_D$**	**CMOS, 12-Bit Multiplying DAC with Output Amplifier**	**3–213**
AD667	**12**	**3.0**	**4/8/12, µP**	**10 V, Int**	**D, E, N, P**	**C, I, $M/_{DS}$**	**Highest Accuracy Complete 12-Bit DAC**	**3–59**
AD767	**12**	**3.0**	**12, µP**	**10 V, Int**	**D, N**	**C, I, $M/_{DS}$**	**Fastest Interface Complete 12-Bit DAC**	**3–86**
AD DAC80/85/87	**12**	**3**	**12**	**Int (6.3 V), Ext**	**D, N**	**C, I, M**	**General Purpose 12-Bit DAC**	**3–285**
AD7233	**12**	**10 (max)**	**Serial, µP**	**Int**	**N**	**I**	**Smallest 12-Bit Serial DACPORT (8-Pin) Bipolar ±5 V Output Range**	**3–123**
AD7243	**12**	**10 (max)**	**Serial**	**Int (+5 V), Ext**	**N, Q, R**	**I, $M/_D$**	**Low Cost 12-Bit Serial DACPORT in 16-Pin SOP**	**3–137**
AD7245A	**12**	**10 (max)**	**12, µP**	**5 V, Int**	**E, N, P, Q, R**	**C, I, $M/_D$**	**Faster Interface, 12 V and 15 V AD7245**	**3–141**
AD7248A	**12**	**10 (max)**	**8, µP**	**5 V, Int**	**N, P, Q, R**	**C, I, $M/_D$**	**Faster Interface, 12 V and 15 V AD7248**	**3–141**
DAC8512	**12**	**16**	**Serial, µP**	**Int**	**N, R**	**I**	**5 Volt Supply, Complete 12-Bit DAC, Serial Input**	**3–356**
DAC8562	**12**	**16**	**12, µP**	**Int (2.5 V)**	**N, R**	**I, M**	**5 Volt Supply, Complete 12-Bit DAC, Parallel Input**	**3–375**
AD7840	**14**	**2.0**	**14/Serial, µP**	**Int (+3 V), Ext**	**N, P, Q**	**C, I, $M/_D$**	**CMOS, 14-Bit Complete DAC, Parallel or Serial Load**	**3–209**
AD7849	**14/16**	**7 (max)**	**Serial, µP**	**Ext (M)**	**N, Q, R**	**I, M**	**High Accuracy Multiplying DAC, Serial Input**	**3–221**
AD766	**16**	**1.5**	**Serial, µP**	**Int**	**D, N**	**C, I, M**	**Zero-Chip Interface 16-Bit DSP DACPORT**	**3–83**
AD1851	16	1.5	Serial, µP	Int	N, R	C	16-Bit, 16 × F_S PCM Audio DAC	CI 2–173
AD760	**16**	**8**	**8/Serial, µP**	**Int (+10 V), Ext**	**N, P, Q**	**I, M**	**16-Bit Self-Calibrating High Accuracy DACPORT**	**3–71**
AD569	**16**	**3.0**	**8/16, µP**	**±5 V, Ext (M)**	**D, N**	**I, M**	**Monolithic, 16-Bit Monotonic DAC**	**3–38**
AD7846	**16**	**6**	**16, µP**	**Ext (M)**	**D, E, N, P**	**C, I, $M/_D$**	**CMOS, 16-Bit Multiplying DAC with Readback Capability**	**3–217**
AD660	**16**	**8**	**Serial, 8**	**10 V, Int**	**N, Q, R**	**I, M**	**Monolithic, Complete Serial/Byte I/P 16-Bit DAC**	**3–42**
AD669	**16**	**8**	**16, µP**	**10 V, Int**	**N, Q, R**	**I, M**	**Monolithic, Complete 16-Bit DAC**	**3–67**
AD1861	18	1.5	Serial	Int	N, R	C	18-Bit, 16 × F_S PCM Audio DAC	CI 2–173
AD1139	18	40	18, µP	–10 V, Int	D	C	True 18-Bit Accuracy	CI 2–167

[1]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.

[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.

[3]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.

[4]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, –40°C to +85°C (Some older products –25°C to +85°C); M = Military, –55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.

[5]CI = *Data Converter Reference Manual, Volume I*; CII = *Data Converter Reference Manual, Volume II*. All other entries refer to this volume.

Boldface type: data sheet information in this volume.

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Selection Guides—Digital-to-Analog Converters

Single DACs, Current Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Ranges[4]	Comments	Page[5]
AD9768	**8**	**0.005**	**8, µP**	**−1.26 V, Int**	**D, E**	**C, M**	**Ultrahigh Speed, ECL Compatible, 20 mA Output Current**	**3–279**
AD9701	**8**	**0.008**	**8, µP**	**Int**	**E, Q**	**I, M**	**250 MSPS Video DAC**	**3–261**
DAC08	**8**	**0.085**	**8**	**Ext (M)**	**E, N, Q, R**	**C, I, M/$_{JDS}$**	**8-Bit High Speed Multiplying DAC**	**3–290**
AD7524	**8**	**0.10**	**8, µP**	**Ext (M)**	**E, N, P, Q, R**	**C, I, M/$_{D}$**	**CMOS, Low Cost, 8-Bit Multiplying DAC with Latch**	**3–159**
AD9720	**10**	**0.01**	**10**	**Int**	**E, N, Q, R**	**C, M**	**Ultrahigh Speed, ECL Compatible, Low Power, 10 pV–s Glitch**	**3–272**
AD9721	**10**	**0.01**	**10**	**Int**	**E, N, Q, R**	**C, M**	**Ultrahigh Speed, TTL Compatible, Low Power, 10 pV–s Glitch**	**3–272**
AD561	10	0.25	10	Int	D, N	C, M/$_{J}$	Industry Standard 10-Bit DAC, JAN Part Available	CI 2–55
DAC100	10	0.300	10	6.6 V, Int	Q	C, I, M/$_{S}$	10-Bit Current Output DAC	CI 2–945
DAC86	10	0.500	10	Ext (M)	Q	I	COMDAC Companding DAC (U-255 Law)	D
AD7533	10	0.60	10	Ext (M)	E, N, P, Q, R	C, I, M/	CMOS, Low Cost, 10-Bit Multiplying DAC	CI 2–439
AD9712B	**12**	**0.022**	**12**	**Int**	**E, N, P, Q**	**C, M**	**ECL Compatible, 25 pV–s Glitch, 0.5 LSB DNL Typ**	**3–264**
AD9713B	**12**	**0.027**	**12**	**Int**	**E, N, P, Q**	**C, M**	**TTL Compatible, 25 pV–s Glitch, 0.5 LSB DNL Typ**	**3–264**
AD568	**12**	**0.035**	**12**	**Int**	**E, Q**	**C, M/$_{D}$**	**Highest Accuracy 12-Bit Ultrahigh Speed DAC**	**3–35**
AD668	**12**	**0.05**	**12**	**Ext (M)**	**Q**	**C, M/**	**Multiplying 12-Bit Ultrahigh Speed DAC**	**3–63**
AD565A	**12**	**0.25**	**12**	**10 V, Int**	**D, R**	**C, M/$_{JS}$**	**Industry Workhorse High Speed, JAN Part Available**	**3–29**
DAC8043	**12**	**0.25**	**Serial, µP**	**Ext (M)**	**N, Q**	**C, I, M/**	**8-Pin DIP Serial Input 12-Bit CMOS Multiplying DAC**	**3–308**
AD7542	12	0.25	4, µP	Ext (M)	E, N, P, Q	C, I, M/	CMOS, Nibble Load 12-Bit Multiplying DAC	CI 2–525
DAC312	**12**	**0.25**	**12**	**Ext (M)**	**N, Q, R**	**C, M/$_{S}$**	**Low Cost, High Speed 12-Bit Multiplying DAC**	**3–305**
AD566A	**12**	**0.35**	**12**	**10 V, Ext**	**D**	**C, M/**	**High Speed DAC**	**3–29**
AD7543	12	0.35	Serial, µP	Ext (M)	D, E, N, P, Q, R	C, I, M/	CMOS, Serial Load 12-Bit Multiplying DAC	CI 2–545
DAC8143	12	0.38	Serial, µP	Ext (M)	N, Q, R	I, M/$_{S}$	CMOS, Serial Load 12-Bit Multiplying DAC, Daisy Chain	CI 2–987
AD7943	**12**	**0.6**	**Serial**	**Ext (M)**	**N, R, RS**	**I**	**3 to 5 Volt Supply Multiplying DAC, Serial**	**3–227**
AD7945	**12**	**0.6**	**12, µP**	**Ext (M)**	**N, Q, R, RS**	**I, M**	**3 to 5 Volt Supply Multiplying DAC, 12-Bit Bus**	**3–227**
AD7948	**12**	**0.6**	**8, µP**	**Ext (M)**	**N, R, RS**	**I**	**3 to 5 Volt Supply Multiplying DAC, 8-Bit Bus**	**3–227**
AD7541A	12	0.60	12	Ext (M)	E, N, P, Q	C, I, M/$_{D}$	CMOS, 12-Bit Multiplying DAC	CI 2–507
DAC8012	12	1.0	12, µP	Ext (M)	N, P, Q	C, I, M/	12-Bit CMOS DAC with Memory and Readback	CI 2–967
AD7548	12	1.0	8, µP	Ext (M)	E, N, P, Q, R	C, I, M/	CMOS, Byte Load 12-Bit DAC, Single or Dual Supply	CI 2–601
AD562	12	1.5	12	Ext	D	C, I, M/$_{JS}$	Industry Standard, JAN Part Available	CI 2–59
AD563	12	1.5	12	2.5 V, Int	D	C, M/$_{S}$	Industry Standard	CI 2–59
AD7545A	12	1.0	12, µP	Ext (M)	E, N, P, Q	C, I, M/	CMOS, Improved AD7545	CI 2–585
AD7534	14	1.5	8, µP	Ext (M)	N, P, Q	C, I, M/	CMOS, Byte Load	CI 2–455
AD7535	14	1.5	8/14, µP	Ext (M)	E, N, P, Q	C, I, M/$_{D}$	CMOS, Parallel or Byte Load	CI 2–467
AD7536	14	1.5	8/14, µP	Ext (M)	E, N, P, Q	C, I, M/	CMOS, Parallel or Byte Load, Bipolar Output	CI 2–479
AD7538	**14**	**1.5**	**14, µP**	**Ext (M)**	**N, Q, R**	**C, I, M**	**CMOS, Parallel Load**	**3–173**

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Ranges[4]	Comments	Page[5]
AD768	**16**	**0.025**	**16, µP**	**Int (+2.5 V)**	**R**	**I**	**32 MSPS, 16-Bit, Low Glitch for Waveform Synthesis**	**3–89**
AD1851	16	1.5	Serial	Int	N, R	C	16-Bit 16 × F_S PCM Audio DAC	CI 2–173
DAC16	**16**	**0.5**	**16**	**Ext (M)**	**D, E, N, R**	**I, M**	**16-Bit High Speed Multiplying DAC**	**3–293**
AD420	**16**	**2500**	**Serial**	**Int (+5 V), Ext**	**N, R**	**I**	**Complete Digital to 4–20 mA Loop Controller**	**3–15**
AD1861	18	1.5	Serial	Int	N, R	C	18-Bit 16 × F_S PCM Audio DAC	CI 2–173
AD1862	20	0.35	Serial	Int	N	C	20-Bit Audio DAC	CI 2–203

[1]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.

[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.

[3]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.

[4]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.

[5]CI = *Data Converter Reference Manual, Volume I*; D = Data Sheet. All other entries refer to this volume.

Boldface Type: Data sheet information in this volume.

Selection Guides—Digital-to-Analog Converters

Multiple DACs, Voltage Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Voltage Int/Ext[2]	# of DACs	Package Options[3]	Temp Ranges[4]	Comments	Pa
AD7669	8	1.0	8, µP	Int	2	N, P, R	C, I, M	CMOS, Complete 8-Bit Dual DAC/ADC/SHA/Reference	Cl
AD8600	**8**	**2**	**8, µP**	**Ext, 2.5 V**	**16**	**P**	**I**	**16-Channel, 8-Bit Multiplying DAC**	**3–**
DAC8229	**8**	**2.0**	**8, µP**	**Ext (M)**	**2**	**N, P, R**	**I, M/**	**CMOS, Single or Dual Supply Operation**	**3–**
AD7769	8	2.5	8, µP	Ext	2	N, P	C, I	CMOS, Complete 8-Bit Dual DAC/ 2-Channel ADC	Cl
DAC8426	**8**	**3.0**	**8, µP**	**10 V, Int**	**4**	**N, Q, R**	**I, M**	**CMOS, Complete with 10 V Reference, Improved Timing**	**3–**
PM7226A	8	3.0	8, µP	Ext (M)	4	N, Q, R	I, M	CMOS, Improved Timing, Specified for +5 V to +15 V Operation	C
AD7226	**8**	**3.0**	**8, µP**	**2–12.5 V, Ext**	**8**	**E, N, P, Q, R**	**C, I, M/$_D$**	**CMOS, No User Trims, Specified with Single or Dual Supplies**	**3–**
AD7225	**8**	**5.0 (max)**	**8, µP**	**2–12.5 V, Ext**	**4**	**E, N, P, Q, R**	**C, I, M/$_D$**	**CMOS, Separate References for Each DAC**	**3–**
DAC8800	**8**	**0.8**	**8, Serial**	**DC, Ext**	**8**	**N, Q, R**	**C, I, M/**	**Octal 8-Bit CMOS DAC (TrimDAC®)**	**3–**
DAC8840	**8**	**3.5**	**Serial**	**Ext (M)**	**8**	**N, Q, R**	**I, M**	**CMOS, Four-Quadrant Multiplying TrimDACs with Op Amps, 8 Channel**	**3–**
DAC8841	8	3.5	Serial	Ext (M)	8	N, Q, R	I, M	Octal 8-Bit, Two Quadrant, Multiplying TrimDAC, +5 V Operation	C
AD7228A	**8**	**5.0 (max)**	**8, µP**	**2–10 V, Ext**	**8**	**N, P, Q, R**	**C, I, M**	**CMOS, Specified for Single or Dual Supply, 5 V to 15 V Skinny 24-Pin SOP/DIP**	**3**
DAC8228	**8**	**2**	**8, µP**	**Ext (M)**	**2**	**N, Q, R**	**I**	**Dual 8-Bit Multiplying DAC**	**3**
AD8842	**8**	**4**	**Serial, µP**	**Ext (M)**	**8**	**N, R**	**I**	**Octal 8-Bit Multiplying TrimDAC**	**3**
AD75004	**12**	**2**	**8, µP**	**5 V, Int**	**4**	**N, P**	**C**	**Fastest Quad 12-Bit Voltage Output DACPORT**	**3**
AD7242	**12**	**2**	**Serial, µP**	**3 V, Int**	**2**	**N, Q, R**	**C, I**	**Complete ±5 V 12-Bit Dual DAC**	**3**
AD390	12	4	12, µP	10 V, Int	4	D	C, M/$_D$	Double Buffered, Simultaneous Update	(
AD7249	**12**	**10 (max)**	**Serial, µP**	**Int (+5 V), Ext**	**2**	**N, Q, R**	**I, M**	**Complete 12-Bit Dual DAC, Serial Input**	**3**
AD7837	**12**	**5**	**8, µP**	**Ext (M)**	**2**	**N, Q, R**	**C, I, M**	**CMOS, MDAC, Byte Load, Double Buffered**	**3**
AD7847	**12**	**5**	**12, µP**	**Ext (M)**	**2**	**N, Q, R**	**C, I, M**	**CMOS, MDAC, Parallel Load**	**3**
DAC8412	**12**	**6**	**12, µP**	**Ext**	**4**	**D, E, N, P, Q**	**I, M/**	**Readback, Reset to Midscale, Low Power Quad DAC, +5 V to ±15 V Operation**	**3**
DAC8413	**12**	**6**	**12, µP**	**Ext**	**4**	**D, E, N, P, Q**	**I, M/**	**Equivalent to DAC8412 with Reset to Zero Scale**	**3**
DAC8420	**12**	**6**	**Serial**	**Ext**	**4**	**N, Q, R**	**I, M**	**BiCMOS, Equivalent to 8412/8413 with Serial Interface in 16-Pin Package**	**3**
AD75089	12	8	12	5 V, Int	8	P	C	Monolithic Octal 12-Bit Voltage Output DACPORT	(

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Voltage Int/Ext[2]	# of DACs	Package Options[3]	Temp Ranges[4]	Comments	Page[5]
AD7237A	**12**	**10 (max)**	**8, µP**	**Int (+5 V), Ext**	**2**	**N, Q, R**	**C, I**	**CMOS, Complete 12-Bit Dual DAC, 12 V–15 V Supplies**	**3–127**
AD7247A	**12**	**10 (max)**	**12, µP**	**Int (+5 V), Ext**	**2**	**N, Q, R**	**C, I**	**Same as AD7237A, Except 8+4 Interface**	**3–127**
AD8522	**12**	**16**	**Serial, µP**	**Int (+2.5 V)**	**2**	**N, R**	**I**	**Complete 12-Bit Dual DAC, 5 V Supply, Serial**	**3–241**
AD8582	**12**	**16**	**12, µP**	**Int (+2.5 V)**	**2**	**N, R**	**I**	**Complete 12-Bit Dual DAC, 5 V Supply, Parallel**	**3–245**
AD664	**12**	**10**	**12, µP**	**Ext (M)**	**4**	**D, E, N, P**	**C, I, $M/_D$**	**Readback, Reset, Low Power Quad DAC**	**3–54**
AD394	12	10	12, µP	Ext (M)	4	D	C, $M/_D$	Four Independent Reference Inputs, Bipolar Outputs	CI 2–31
AD7244	**14**	**2**	**Serial, µP**	**+3 V, Int**	**2**	**N, Q, R**	**C, I, M**	**Complete ±5 V 14-Bit Dual DAC**	**3–107**
AD1866	16	1.5	Serial	Int	2	N, R	I	Dual 16-Bit Audio DAC, +5 V Single Supply	CI 2–235
AD1865	18	1.5	Serial	Int	2	N, R	C	Dual 18-Bit, 16 × F_S PCM Audio DAC	CI 2–225
AD1868	18	1.5	Serial	Int	2	N, R	C	Dual 18-Bit Audio DAC, +5 V Single Supply	CI 2–237

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[4]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.

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Boldface type: Data sheet information in this volume.

TrimDAC is a registered trademark of Analog Devices, Inc.

Selection Guides—Digital-to-Analog Converters

Multiple DACs, Current Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Voltage Int/Ext[2]	# of DACs	Package Options[3]	Temp Ranges[4]	Comments	Page[5]
AD7528	**8**	**0.18**	**8, µP**	**Ext (M)**	**2**	**E, N, P, Q, R**	**C, I, M/$_D$**	**CMOS, +5 V to +15 V Operation, TTL Compatible at V_{DD} = +5 V**	**3–163**
DAC8408	**8**	**0.19**	**8, µP**	**Ext (M)**	**4**	**N, P, Q, R**	**C, I, M/$_D$**	**CMOS, Data Readback Memory Function, Separate V_{REF}**	**3–329**
PM7628	8	0.20	8, µP	Ext (M)	2	E, N, P, Q, R	I, M/	CMOS, +5 V or +15 V Operation, Improved Timing	CI 2–665
AD7628	**8**	**0.35**	**8, µP**	**Ext (M)**	**2**	**E, N, P, Q, R**	**C, I, M/**	**CMOS, +12 V to +15 V Operation, TTL Compatible at V_{DD} = 12 V to 15 V**	**3–191**
DAC8221	**12**	**0.45**	**12, µP**	**Ext (M)**	**2**	**E, N, Q, R**	**C, I, M/$_{DS}$**	**CMOS, Buffered Inputs, +5 V Operation**	**3–311**
AD7568	**12**	**0.2**	**Serial, µP**	**Ext (M)**	**8**	**P, S**	**I**	**Single +5 V Supply, Separate References, 44-Pin PQFP and PLCC**	**3–185**
AD7564	**12**	**0.5**	**Serial, µP**	**Ext (M)**	**4**	**N, R**	**I**	**Quad 12-Bit Multiplying DAC, 5 V Supply**	**3–177**
DAC8222	**12**	**1.0 (max)**	**12, µP**	**Ext (M)**	**2**	**E, N, Q, R**	**C, I, M/$_{DS}$**	**CMOS, Double Buffered Inputs, Parallel Load**	**3–315**
DAC8248	**12**	**1.0 (max)**	**8, µP**	**Ext (M)**	**2**	**N, Q, R**	**C, I, M/**	**CMOS, Double Buffered Inputs, Byte Load**	**3–325**
AD7537	**12**	**1.5 (max)**	**8, µP**	**Ext (M)**	**2**	**E, N, P, Q, R**	**C, I, M/$_D$**	**CMOS, Byte Load, Double Buffered**	**3–167**
AD7547	**12**	**1.5 (max)**	**12, µP**	**Ext (M)**	**2**	**E, N, P, Q, R**	**C, I, M/$_D$**	**CMOS, Parallel Load**	**3–167**
AD7549	12	1.5 (max)	4, µP	Ext (M)	2	E, N, P, Q	C, I, M/$_D$	CMOS, Nibble Load, Double Buffered	CI 2–629
AD1865	18		Serial, µP	Int	2	N	C	Dual 18-Bit, 16 × F_S PCM Audio DAC	CI 2–225

LOGDACs®

Model	Res dB	Full-Scale Range dB	Accuracy dB	Package Options[3]	Temp Ranges[4]	Comments	Page[5]
AD7111	**0.375**	**88.5**	**0.17**	**E, N, Q, R**	**C, I, M/**	**Low Distortion**	**3–93**
AD7111A	**0.375**	**88.5**	**0.17**	**N, R**	**I**	**Low Glitch, Pin Compatible with AD7524**	**3–93**
AD7112	**0.375**	**88.5**	**0.17**	**N, R**	**I**	**Low Glitch, Pin Compatible with AD7528**	**3–99**
AD7118	1.5	88.5	0.35	E, N, P, Q, R	C, I, M/	CMOS	CI 2–253

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[4]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.

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Boldface Type: Data sheet information in this volume.

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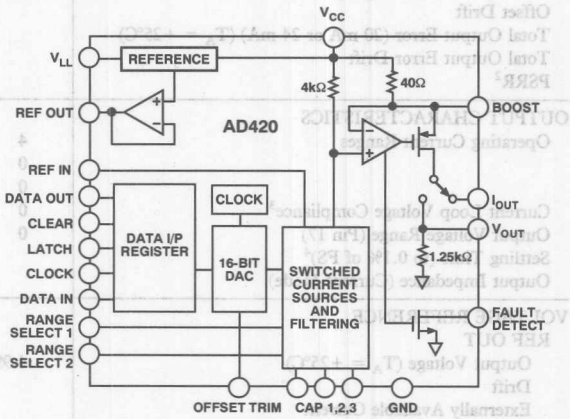
Serial Input 16-Bit 4–20 mA, 0–20 mA DAC

AD420

FEATURES

4–20 mA, 0–20 mA or 0–24 mA Current Output
16-Bit Resolution and Monotonicity
±0.012% max Integral Nonlinearity
±0.05% max Offset (Trimmable)
±0.15% max Total Output Error (Trimmable)
Flexible Serial Digital Interface (3.3 Mbps)
On-Chip Loop Fault Detection
On-Chip 5 V Reference (25 ppm/°C max)
Asynchronous CLEAR Function
Power Supply Range of 12 V–36 V
Output Loop Compliance of 0 V–33.5 V
24-Pin SOIC and PDIP Packages

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD420 is a complete digital to current loop output converter, designed to meet the needs of the industrial control market. It provides a high precision, fully integrated, low cost single-chip solution for generating current loop signals, in a compact 24-pin SOIC or PDIP package.

The output current range can be programmed to 4–20 mA, 0–20 mA or an overrange function of 0–24 mA. The AD420 can alternatively provide a voltage output from a separate pin that can be configured to provide 0 V–5 V, 0 V–10 V, ±5 V or ±10 V with the addition of a single external buffer amplifier.

The 3.3M Baud serial input logic design minimizes the cost of galvanic isolation and allows for simple connection to commonly used microprocessors. It can be used in three-wire or asynchronous mode and a serial-out pin is provided to allow daisy chaining of multiple DACs on the current loop side of the isolation barrier.

The AD420 uses sigma-delta (ΣΔ) DAC technology to achieve 16-bit monotonicity at very low cost. Full-scale settling to 0.1% occurs within 3 ms. The only external components that are required (in addition to normal transient protection circuitry) are three low cost capacitors which are used in the DAC output filter.

If the AD420 is going to be used at extreme temperatures and supply voltages, an external output transistor can be used to minimize power dissipation on the chip via the "BOOST" pin.

The FAULT DETECT pin signals when an open circuit occurs in the loop. The on-chip voltage reference can be used to supply a precision +5 V to external components in addition to the AD420 or, if the user desires temperature stability exceeding 25 ppm/°C, an external precision reference such as the AD586 can be used as the reference.

The AD420 is available in a 24-pin SOIC and PDIP over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. The AD420 is a single chip solution for generating 4–20 mA or 0–20 mA signals at the "controller end" of the current loop.
2. The AD420 operates on +12 V to +36 V supplies, with an output loop compliance of 0 V to V_{CC} – 2.5 V.
3. The flexible serial input can be used in Three-Wire Mode with SPI* or MICROWIRE† microcontrollers, or in Asynchronous Mode which minimizes the number of control signals required.
4. The Serial Data Out pin can be used to daisy chain any number of AD420s together in Three-Wire Mode.
5. At Power-Up the AD420 initializes its output to the low end of the selected range.
6. The AD420 has an asynchronous CLEAR pin which sends the output to the low end of the selected range (0 mA, 4 mA, or 0 V).
7. The AD420 BOOST pin accommodates an external transistor to off-load power dissipation from the chip.
8. The offset of ±0.05% and total output error of ±0.15% can be trimmed if desired, using two external potentiometers.

*SPI is a registered trademark of Motorola.
†MICROWIRE is a registered trademark of National Semiconductor.

AD420—SPECIFICATIONS ($T_A = T_{MIN} - T_{MAX}$, $V_{CC} = +24$ V, $R_L = 500\ \Omega$ unless otherwise noted)

Parameter	AD420AN/AR Min	Typ	Max	Units
RESOLUTION	16			Bits
ACCURACY[1]				
Monotonicity	16			Bits
Integral Nonlinearity		±0.002	±0.012	%
Offset (0 mA or 4 mA) ($T_A = +25°C$)			±0.05	%
Offset Drift		20	50	ppm/°C
Total Output Error (20 mA or 24 mA) ($T_A = +25°C$)			±0.15	%
Total Output Error Drift		20	50	ppm/°C
PSRR[2]		5	10	μA/V
OUTPUT CHARACTERISTICS				
Operating Current Ranges	4		20	mA
	0		20	mA
	0		24	mA
Current Loop Voltage Compliance[3]	0		$V_{CC} - 2.5$ V	V
Output Voltage Range (Pin 17)	0		5	V
Settling Time (to 0.1% of FS)[4]		2.5	3	ms
Output Impedance (Current Mode)		25		MΩ
VOLTAGE REFERENCE				
REF OUT				
Output Voltage ($T_A = +25°C$)	4.995	5.0	5.005	V
Drift			±25	ppm/°C
Externally Available Current		5		mA
Short Circuit Current		7		mA
REFIN				
Resistance		30		kΩ
V_{LL}				
Output Voltage		4.5		V
Externally Available Current		5		mA
Short Circuit Current		20		mA
DIGITAL INPUTS				
V_{IH} (Logic 1)	2.4			V
V_{IL} (Logic 0)			0.8	V
I_{IH} ($V_{IN} = 5.0$ V)			±10	μA
I_{IL} ($V_{IN} = 0$ V)			±10	μA
Data Input Rate ("3-Wire" Mode)	No Minimum		3.3	Mbps
Data Input Rate ("Asynchronous" Mode)	No Minimum		150	kbps
DIGITAL OUTPUTS				
FAULT DEFECT				
V_{OH} (10 kΩ Pull-Up Resistor to V_{LL})	3.6	4.5		V
V_{OL} (10 kΩ Pull-Up Resistor to V_{LL})		0.2	0.4	V
V_{OL} @ 2.5 mA		0.6		V
DATA OUT				
V_{OH} ($I_{OH} = -0.8$ mA)	3.6	4.3		V
V_{OL} ($I_{OL} = 1.6$ mA)		0.3	0.4	V
POWER SUPPLY				
Operating Range V_{CC}	12		36	V
Quiescent Current		4.2	5.0	mA
Quiescent Current (External V_{LL})		3		mA
TEMPERATURE RANGE				
Specified Performance	−40		+85	°C

NOTES

[1]Total Output Error includes Offset and Gain Error. Total Output Error and Offset Error are with respect to the Full-Scale Output and are measured with an ideal +5 V reference. If the internal reference is used, the reference errors must be added to the Offset and Total Output Errors.

[2]PSRR is measured by varying V_{CC} from 12 V to 36 V.

[3]When V_{CC} is greater than 32 V the Minimum R_L is 200 Ω.

[4]External capacitor selection must be as described in Figure 5.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to GND . . . . . 36 V
IOUT to GND . . . . . V_{CC}
Digital Inputs to GND . . . . . −0.5 V to +7 V
Digital Outputs to GND . . . . . −0.5 V to V_{LL} + 0.3 V
V_{LL} and REFOUT: Outputs safe for indefinite short to ground.
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Thermal Impedance:
SOIC (R) Package . . . . . θ_{JA} = 75°C/W
PDIP (N) Package . . . . . θ_{JA} = 50°C/W

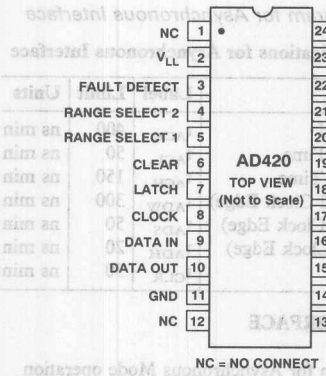
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational specification is not implied. Exposure to absolute maximum specifications for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD420AN	−40°C to +85°C	24-Pin Plastic DIP	N-24
AD420AR	−40°C to +85°C	24-Pin SOIC	R-24

*For outline information see Package Information section.

PIN DESIGNATIONS



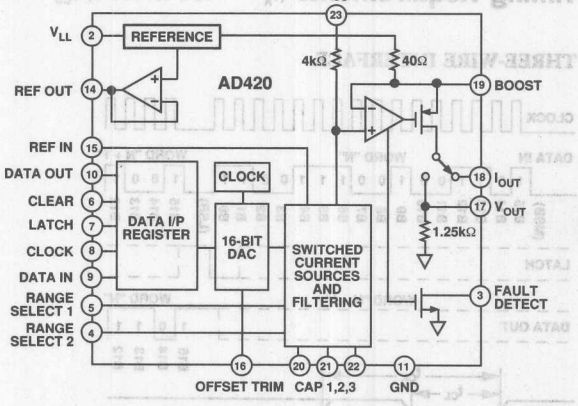


Figure 1. Functional Block Diagram

Table I. Truth Table

Inputs			
CLEAR	Range Select 2	Range Select 1	Operation
0	X	X	Normal Operation
1	X	X	Output at Bottom of Span
X	0	0	0 V–5 V Range
X	0	1	4–20 mA Range
X	1	0	0–20 mA Range
X	1	1	0–24 mA Range

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD420 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Timing Requirements (T_A = −40°C to +85°C, V_{CC} = +12 V to +36 V)

THREE-WIRE INTERFACE

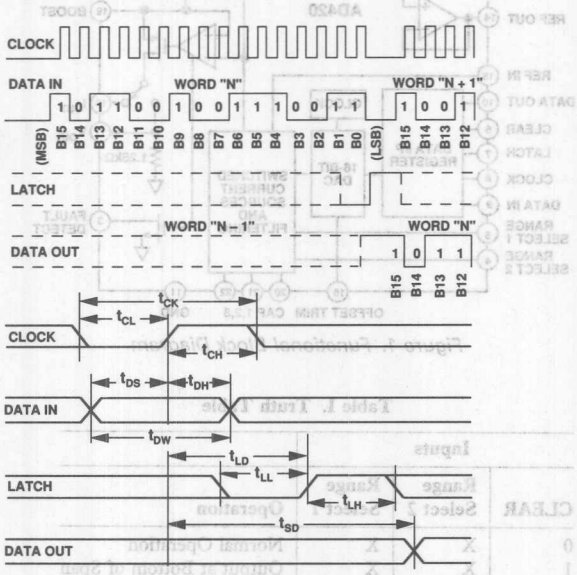


Figure 2. Timing Diagram for Three-Wire Interface

Table II. Timing Specification for Three-Wire Interface

Parameter	Label	Limit	Units
Data Clock Period	t_{CK}	300	ns min
Data Clock Low Time	t_{CL}	80	ns min
Data Clock High Time	t_{CH}	80	ns min
Data Stable Width	t_{DW}	125	ns min
Data Setup Time	t_{DS}	40	ns min
Data Hold Time	t_{DH}	5	ns min
Latch Delay Time	t_{LD}	80	ns min
Latch Low Time	t_{LL}	80	ns min
Latch High Time	t_{LH}	80	ns min
Serial Output Delay Time	t_{SD}	225	ns max
Clear Pulse Width	t_{CLR}	50	ns min

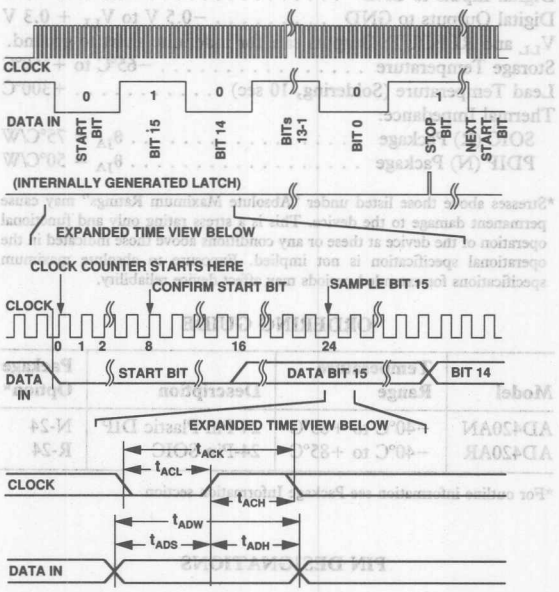


Figure 3. Timing Diagram for Asynchronous Interface

Table III. Timing Specifications for Asynchronous Interface

Parameter	Label	Limit	Units
Asynchronous Clock Period	t_{ACK}	400	ns min
Asynchronous Clock Low Time	t_{ACL}	50	ns min
Asynchronous Clock High Time	t_{ACH}	150	ns min
Data Stable Width (Critical Clock Edge)	t_{ADW}	300	ns min
Data Setup Time (Critical Clock Edge)	t_{ADS}	50	ns min
Data Hold Time (Critical Clock Edge)	t_{ADH}	20	ns min
Clear Pulse Width	t_{CLR}	50	ns min

ASYNCHRONOUS INTERFACE

Note in the timing diagram for Asynchronous Mode operation each data word is "framed" by a START (0) bit and a STOP (1) bit. The data timing is with respect to the rising edge of the CLOCK at the center of each bit cell. Bit cells are 16 clocks long, and the first cell (the START bit) begins at the first clock following the leading (falling) edge of the START bit. Thus the MSB (D15) is sampled 24 clock cycles after the beginning of the START bit, D14 is sampled at clock number 40, and so on. During any "dead time" before writing the next word the DATA IN pin must remain at logic 1.

The DAC output updates when the STOP bit is received. In the case of a "framing error" (the STOP bit sampled as a 0) the AD420 will output a pulse at the DATA OUT pin one clock period wide during the clock period subsequent to sampling the STOP bit. The DAC output will not update if a "framing error" is detected.

PIN DESCRIPTION

Pin #	Symbol	Type	Function
2	V_{LL}	P	Auxiliary buffered +4.5 V digital logic voltage. This pin is the internal supply voltage for the digital circuitry and can be used as a termination for pull-up resistors. An external +5 V power supply can be connected to V_{LL}. It will override this buffered voltage, thus reducing the internal power dissipation.
3	FAULT DETECT	DO	FAULT DETECT, connected to a pull-up resistor, is asserted low when the output current does not match the DAC's programmed value. For example, in case the current loop is broken.
4 5	RANGE SELECT 2 RANGE SELECT 1	DI	Selects the converters output operating range. One output voltage range and three output current ranges are available.
6	CLEAR	DI	Valid V_{IH} will unconditionally force the output to go to the minimum of its programmed range. After CLEAR is removed the DAC output will remain at this value. The data in the input register is unaffected.
7	LATCH	DI	In the three-wire interface mode a rising edge parallel loads the serial input register data into the DAC. To use the asynchronous mode connect LATCH through a current limiting resistor to V_{CC}.
8	CLOCK	DI	Data Clock Input. The clock period is equal to the input data bit rate in the three-wire interface mode and is 16 times the bit rate in asynchronous mode.
9	DATA IN	DI	Serial Data Input.
10	DATA OUT	DO	Serial Data Output. In the three-wire interface mode, this output can be used for daisy chaining multiple AD420s. In the asynchronous mode a positive pulse will indicate a framing error after the stop-bit is received.
11	GND	P	Ground (Common).
14	REF OUT	AO	+5 V Reference Output.
15	REF IN	AI	Reference Input.
16	OFFSET TRIM	AI	Offset Adjust.
17	V_{OUT}	AO	Voltage Output.
18	I_{OUT}	AO	Current Output.
19	BOOST	AO	Connect to an external transistor to reduce the power dissipated in the AD420 output transistor, if desired.
20 21 22	CAP 1 CAP 2 CAP 3	AI	These pins are used for internal filtering. Connect capacitors between each of these pins and V_{CC}. Refer to the description of current output operation.
23	V_{CC}	P	+12 V to +36 V Power.
1, 12, 13, 24	NC		No Connection. No internal connections inside device.

Type: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power

DEFINITIONS OF SPECIFICATIONS

RESOLUTION: For 16-bit resolution, 1 LSB = 0.0015% of the FSR. In the 4–20 mA range 1 LSB = 244 nA.

INTEGRAL NONLINEARITY: Analog Devices defines integral nonlinearity as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to FS−1 LSB) for any bit combination. This is also referred to as relative accuracy.

DIFFERENTIAL NONLINEARITY: Differential nonlinearity is the measure of the change in the analog output, normalized to full scale, associated with an LSB change in the digital input code. Monotonic behavior requires that the differential linearity error be greater than −1 LSB over the temperature range of interest.

MONOTONICITY: A DAC is monotonic if the output either increases or remains constant for increasing digital inputs with the result that the output will always be a single-valued function of the input.

GAIN ERROR: Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out.

OFFSET ERROR: Offset error is the deviation of the output current from its ideal value expressed as a percentage of the full-scale output with all 0s loaded in the DAC.

DRIFT: Drift is the change in a parameter (such as gain and offset) over a specified temperature range. The drift temperature coefficient, specified in ppm/°C, is calculated by measuring the parameter at T_{MIN}, 25°C, and T_{MAX} and dividing the change in the parameter by the corresponding temperature change.

CURRENT LOOP VOLTAGE COMPLIANCE: The voltage compliance is the maximum voltage at the IOUT pin for which the output current will be equal to the programmed value.

THEORY OF OPERATION

The AD420 uses a sigma-delta (ΣΔ) architecture to carry out the digital-to-analog conversion. This architecture is particularly well suited for the relatively low bandwidth requirements of the industrial control environment because of its inherent monotonicity at high resolution.

In the AD420 a second order modulator is used to keep complexity and die size to a minimum. The single bit stream from the modulator controls a switched current source that is then filtered by three, continuous time resistor-capacitor sections. The capacitors are the only external components that have to be added for standard current-out operation. The filtered current is amplified and mirrored to the supply rail so that the application simply sees a 4–20 mA, 0–20 mA, or 0–24 mA current source output with respect to ground. The AD420 is manufactured on a BiCMOS process that is well suited to implementing low voltage digital logic with high performance and high voltage analog circuitry.

The AD420 can also provide a voltage output instead of a current loop output if desired. The addition of a single external amplifier allows the user to obtain 0 V–5 V, 0 V–10 V, ±5 V, or ±10 V.

The AD420 has a loop fault detection circuit that warns if the voltage at IOUT attempts to rise above the compliance range, due to an open loop circuit or insufficient power supply voltage. The FAULT DETECT is an active low open drain signal so that one can connect several AD420s together to one pull-up resistor for global error detection. The pull-up resistor can be tied to the VLL pin, or an external +5 V logic supply.

The IOUT current is controlled by a PMOS transistor and internal amplifier as shown in the functional block diagram. The internal circuitry that develops the fault output avoids using a comparator with "window limits" since this would require an actual output error before the FAULT DETECT output becomes active. Instead, the signal is generated when the internal amplifier in the output stage of the AD420 has less than approximately one volt remaining of drive capability (when the gate of the output PMOS transistor nearly reaches ground). Thus the FAULT DETECT output activates slightly before the compliance limit is reached. Since the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open loop gain, and no output error occurs before the fault detect output becomes active.

The three-wire digital interface, comprising DATA IN, CLOCK, and LATCH, interfaces to all commonly used serial microprocessors without the addition of any external glue logic. Data is loaded into an input register under control of CLOCK and is loaded to the DAC when LATCH is strobed. If a user wants to minimize the number of galvanic isolators in an intrinsically safe application, the AD420 can be configured to run in "asynchronous" mode. This mode is selected by connecting the LATCH pin to V_{CC} through a current limiting resistor. The data must then be combined with a start and stop bit to "frame" the information and trigger the internal LATCH signal.

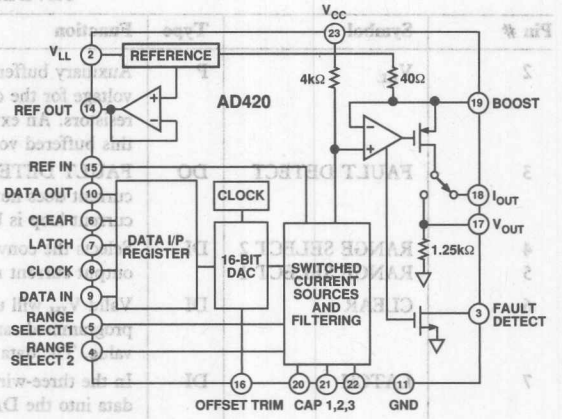


Figure 4. Functional Block Diagram

APPLICATIONS

CURRENT OUTPUT

The AD420 can provide 4–20 mA, 0–20 mA, or 0–24 mA output without any active external components. The three capacitors shown in Figure 5 are all that is required. These can be any type of low cost ceramic capacitors. To meet the specified full-scale settling time of 3 ms, low dielectric absorption capacitors (NPO) are required. Suitable values are C1 = 0.01 μF, C2 = 0.01 μF, and C3 = 0.0033 μF.

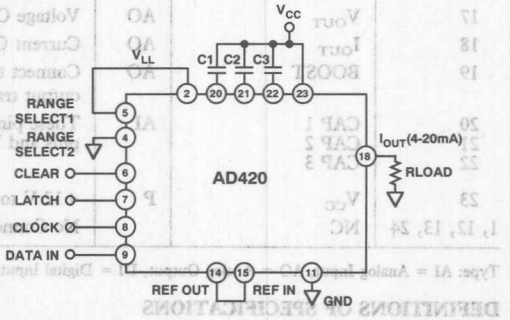


Figure 5. Standard Configuration

DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads connect a 0.01 μF capacitor between IOUT (Pin 18) and GND (Pin 11). This will ensure stability of the AD420 with loads beyond 50 mH. There is no maximum capacitance limit. The capacitive component of the load may cause slower settling, though this may be masked by the settling time of the AD420. A programmed change in the current may cause a back EMF voltage on the output that may exceed the compliance of the AD420. To prevent this voltage from exceeding the supply rails connect protective diodes between IOUT and each of V_{CC} and GND.

VOLTAGE-MODE OUTPUT

Since the AD420 is a single supply device, it is necessary to add an external buffer amplifier to the VOUT pin to obtain a selection of high quality bipolar output voltage ranges as shown in Figure 6.

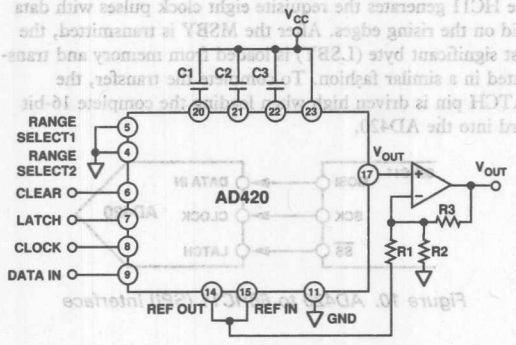


Figure 6.

Table IV. Buffer Amplifier Configuration

R1	R2	R3	VOUT
Open	Open	0	0–5 V
Open	R	R	0–10 V
R	Open	R	±5 V
R	2R	2R	±10 V

Suitable R = 5 kΩ.

OPTIONAL SPAN AND ZERO TRIM

For those users who would like lower than specified values of offset and gain error, Figure 7 shows a simple way to trim these parameters. Care should be taken to select low drift resistors because they will affect the temperature drift performance of the DAC.

The adjustment algorithm is iterative. The procedure for trimming the AD420 in the 4–20 mA mode can be accomplished as follows:

STEP I . . .OFFSET ADJUST
Load all zeros. Adjust RZERO for 4.00000 mA of output current.

STEP II . . .GAIN ADJUST
Load all ones. Adjust RSPAN for 19.99976 mA (FS − 1 LSB) of output current.
Return to STEP I and iterate until convergence is obtained.

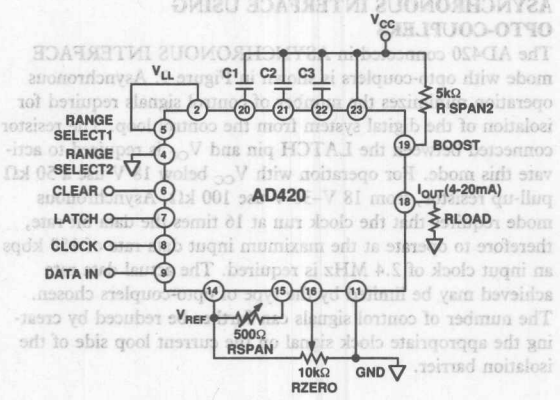


Figure 7. Offset and Gain Adjust

THREE-WIRE INTERFACE

Figure 8 shows the AD420 connected in the three-wire interface mode. The AD420 data input block contains a serial input shift register and a parallel latch. The contents of the shift register are controlled by the DATA IN signal and the rising edges of the CLOCK. Upon request of the LATCH pin the DAC and internal latch are updated from the shift register parallel outputs. The CLOCK should remain inactive while the DAC is updated. Refer to the timing requirements for Three-Wire Interface.

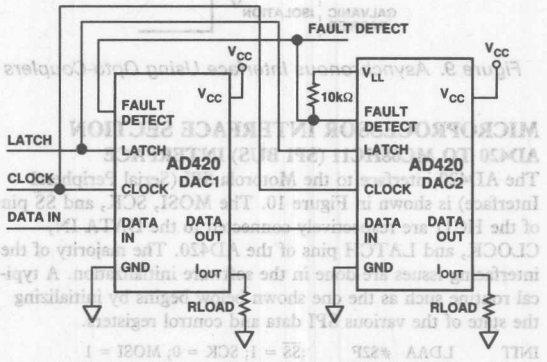


Figure 8. Three-Wire Interface Using Multiple DACs with Joint Fault Detect

USING MULTIPLE DACS WITH FAULT DETECT

The three-wire interface mode can utilize the serial DATA OUT for easy interface to multiple DACs. To program the two AD420s in Figure 8, 32 data bits are required. The first 16 bits are clocked into the input shift register of DAC1. The next 16 bits transmitted pass the first 16 bits from the DATA OUT pin of DAC1 to the input register of DAC2. The input shift registers of the two DACs operate as a single 32-bit shift register, with the leading 16 bits representing information for DAC2 and the trailing 16 bits serving for DAC1. Each DAC is then updated upon request of the LATCH pin. The daisy-chain can be extended to as many DACs as required.

The AD420 connected in ASYNCHRONOUS INTERFACE mode with opto-couplers is shown in Figure 9. Asynchronous operation minimizes the number of control signals required for isolation of the digital system from the control loop. The resistor connected between the LATCH pin and V_{CC} is required to activate this mode. For operation with V_{CC} below 18 V use a 50 kΩ pull-up resistor, from 18 V–36 V use 100 kΩ. Asynchronous mode requires that the clock run at 16 times the data bit rate, therefore to operate at the maximum input data rate of 150 kbps an input clock of 2.4 MHz is required. The actual data rate achieved may be limited by the type of opto-couplers chosen. The number of control signals can further be reduced by creating the appropriate clock signal on the current loop side of the isolation barrier.

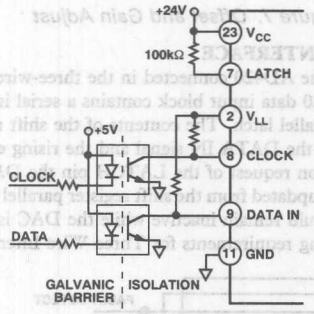


Figure 9. Asynchronous Interface Using Opto-Couplers

MICROPROCESSOR INTERFACE SECTION

AD420 TO MC68HC11 (SPI BUS) INTERFACE

The AD420 interface to the Motorola SPI (Serial Peripheral Interface) is shown in Figure 10. The MOSI, SCK, and $\overline{SS}$ pins of the HC11 are respectively connected to the DATA IN, CLOCK, and LATCH pins of the AD420. The majority of the interfacing issues are done in the software initialization. A typical routine such as the one shown below begins by initializing the state of the various SPI data and control registers.

```
INIT    LDAA  #$2F      ;SS = 1; SCK = 0; MOSI = 1
        STAA  PORTD     ;SEND TO SPI OUTPUTS
        LDAA  #$38      ;SS, SCK,MOSI = OUTPUTS
        STAA  DDRD      ;SEND DATA DIRECTION INFO
        LDAA  #$50      ;DABL INTRPTS,SPI IS MASTER & ON
        STAA  SPCR      ;CPOL = 0, CPHA = 0, 1MHZ BAUDRATE
NEXTPT  LDAA  MSBY      ;LOAD ACCUM W/UPPER 8 BITS
        BSR   SENDAT    ;JUMP TO DAC OUTPUT ROUTINE
        JMP   NEXTPT    ;INFINITE LOOP
SENDAT  LDY   #$1000    ;POINT AT ON-CHIP REGISTERS
        BCLR  $08,Y,$20 ;DRIVE SS (LATCH) LOW
        STAA  SPDR      ;SEND MS-BYTE TO SPI DATA REG
WAIT1   LDAA  SPSR      ;CHECK STATUS OF SPIE
        BPL   WAIT1     ;POLL FOR END OF X-MISSION
        LDAA  LSBY      ;GET LOW 8 BITS FROM MEMORY
        STAA  SPDR      ;SEND LS-BYTE TO SPI DATA REG
WAIT2   LDAA  SPSR      ;CHECK STATUS OF SPIE
        BPL   WAIT2     ;POLL FOR END OF X-MISSION
        BSET  $08,Y,$20 ;DRIVE SS HIGH TO LATCH DATA
        RTS
```

ory and processed by the SENDAT routine. The SS pin is driven low by indexing into the PORTD data register and clear Bit 5. The MSBY is then sent to the SPI data register where it is automatically transferred to the AD420 internal shift resister. The HC11 generates the requisite eight clock pulses with data valid on the rising edges. After the MSBY is transmitted, the least significant byte (LSBY) is loaded from memory and transmitted in a similar fashion. To complete the transfer, the LATCH pin is driven high when loading the complete 16-bit word into the AD420.

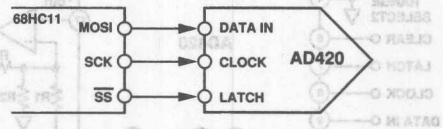


Figure 10. AD420 to 68HC11 (SPI) Interface

AD420 TO MICROWIRE INTERFACE

The flexible serial interface of the AD420 is also compatible with the National Semiconductor MICROWIRE interface. The MICROWIRE interface is used in micro controllers such as the COP400 and COP800 series of processors. A generic interface to use the MICROWIRE interface is shown in Figure 11. The G1, SK, and SO pins of the MICROWIRE interface are respectively connected to the LATCH, CLOCK, and DATA IN pins of the AD420.

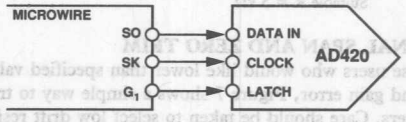


Figure 11. AD420 to MICROWIRE Interface

EXTERNAL BOOST FUNCTION

The external boost transistor reduces the power dissipated in the AD420 by reducing the current flowing in the on-chip output transistor (dividing it by the current gain of the external circuit). A discrete NPN transistor with a breakdown voltage BV_{CEO}, greater than 36 V can be used as shown in Figure 12.

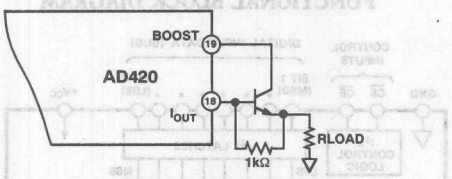


Figure 12. External Boost Configuration

The external boost capability has been developed for those users who may wish to use the AD420, in the SOIC package, at the extremes of the supply voltage, load current, and temperature range. The PDIP package (because of its lower thermal resistance) will operate safely over the entire specified voltage, temperature, and load current ranges without the boost transistor. The plot in Figure 13 shows the safe operating region for both package types. The boost transistor can also be used to reduce the amount of temperature induced drift in the part. This will minimize the temperature induced drift of the on-chip voltage reference, which improves drift and linearity.

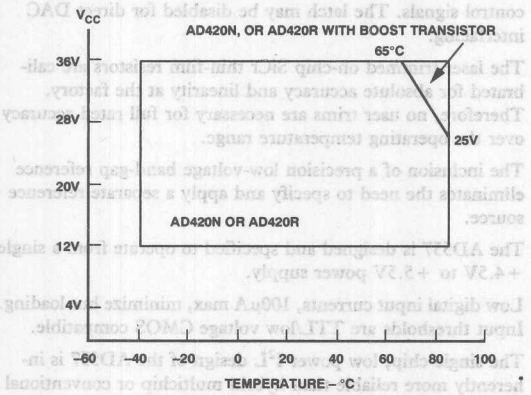


Figure 13. Safe Operating Region

AD420 PROTECTION

TRANSIENT VOLTAGE PROTECTION

The AD420 contains ESD protection diodes which prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. In order to protect the AD420 from excessively high voltage transients such as those specified in IEC 801, external power diodes and a surge current limiting resistor may be required, as shown in Figure 14. The constraint on the resistor is that during normal operation the output voltage level at IOUT must remain within its voltage compliance limit ($IOUT \times (Rp + R_{LOAD}) \leq V_{CC} - 2.5\ V$) and the two protection diodes and resistor must have appropriate power ratings.

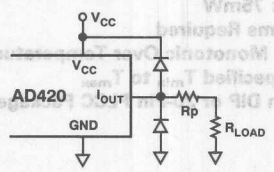


Figure 14. Output Transient Voltage Protection

BOARD LAYOUT AND GROUNDING

The AD420 ground pin, designated GND, is the "high quality" ground reference point for the device. Any external loads on the REF OUT and VOUT pins of the AD420 should be returned to this reference point. Analog and digital ground currents should not share a common path. Each signal should have an appropriate analog or digital signal return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths.

POWER SUPPLIES AND DECOUPLING

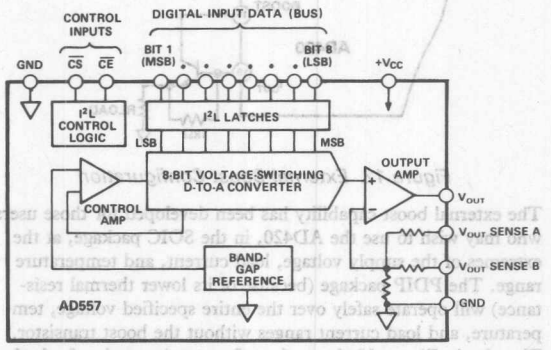
The AD420 supply pins, V_{CC} (Pin 23) and V_{LL} (Pin 2), should be decoupled to GND with 0.1 μF capacitors to eliminate high frequency noise that may otherwise get coupled into the analog system. High frequency ceramic capacitors are recommended. The decoupling capacitors should be located in close proximity to the pins and the ground line to have maximum effect.

DACPORT Low Cost, Complete µP-Compatible 8-Bit DAC

AD557

FEATURES
Complete 8-Bit DAC
Voltage Output – 0 to 2.56V
Internal Precision Band-Gap Reference
Single-Supply Operation: +5V (±10%)
Full Microprocessor Interface
Fast: 1µs Voltage Settling to ±1/2LSB
Low Power: 75mW
No User Trims Required
Guaranteed Monotonic Over Temperature
All Errors Specified T_{min} to T_{max}
Small 16-Pin DIP or 20-Pin PLCC Package
Low Cost

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD557 DACPORT™ is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The low cost and versatility of the AD557 DACPORT are the result of continued development in monolithic bipolar technologies.

The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single +5V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range, while laser-wafer trimming of these thin-film resistors permits absolute calibration at the factory to within ±2.5LSB; thus, no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 800ns.

The AD557 is available in two package configurations. The AD557JN is packaged in a 16-pin plastic, 0.3"-wide DIP. For surface mount applications, the AD557JP is packaged in a 20-pin JEDEC standard PLCC. Both versions are specified over the operating temperature range of 0 to +70°C.

PRODUCT HIGHLIGHTS

1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allow the AD557 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.
2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
4. The AD557 is designed and specified to operate from a single +4.5V to +5.5V power supply.
5. Low digital input currents, 100µA max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible.
6. The single-chip, low power I^2L design of the AD557 is inherently more reliable than hybrid multichip or conventional single-chip bipolar designs.

DACPORT is a trademark of Analog Devices, Inc.
Covered by U.S. Patent Nos. 3,887,863; 3,685,045; 4,323,795; other patents pending.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ T_A = +25C, V_{CC} = +5V unless otherwise specified)

Model	AD557J Min	Typ	Max	Units
RESOLUTION			8	Bits
RELATIVE ACCURACY[1]				
0 to +70°C		±1/2	1	LSB
OUTPUT				
Ranges		0 to +2.56		V
Current Source		+5		mA
Sink		Internal Passive Pull-Down to Ground[2]		
OUTPUT SETTLING TIME[3]		0.8	1.5	µs
FULL SCALE ACCURACY[4]				
@25°C		±1.5	±2.5	LSB
T_{min} to T_{max}		±2.5	±4.0	LSB
ZERO ERROR				
@25°C			±1	LSB
T_{min} to T_{max}			±3	LSB
MONOTONICITY[5]				
T_{min} to T_{max}		Guaranteed		
DIGITAL INPUTS				
T_{min} to T_{max}				
Input Current			±100	µA
Data Inputs, Voltage				
Bit On – Logic "1"	2.0			V
Bit On – Logic "0"	0		0.8	V
Control Inputs, Voltage				
On – Logic "1"	2.0			V
On – Logic "0"	0		0.8	V
Input Capacitance		4		pF
TIMING				
t_W Strobe Pulse Width	225			ns
T_{min} to T_{max}	300			ns
t_{DH} Data Hold Time	10			ns
T_{min} to T_{max}	10			ns
t_{DS} Data Setup Time	225			ns
T_{min} to T_{max}	300			ns
POWER SUPPLY				
Operating Voltage Range (V_{CC})				
2.56 Volt Range	+4.5		+5.5	V
Current (I_{CC})		15	25	mA
Rejection Ratio			0.03	%/%
POWER DISSIPATION, V_{CC} = 5V		75	125	mW
OPERATING TEMPERATURE RANGE	0		+70	°C

NOTES

[1]Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the offset to the full scale of the device. See "Measuring Offset Error" on AD558 data sheet.

[2]Passive pull-down resistance is 2kΩ.

[3]Settling time is specified for a positive-going full-scale step to ± 1/2LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.

[4]The full-scale output voltage is 2.55V and is guaranteed with a +5V supply.

[5]A monotonic converter has a maximum differential linearity error of ± 1LSB.

Specifications shown in **boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

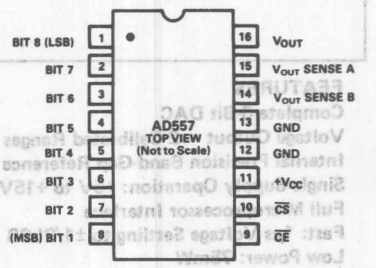
ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Ground . . . . . 0V to +18V
Digital Inputs (Pins 1-10) . . . . . 0 to +7.0V
V_{OUT} . . . . . Indefinite Short to Ground
Momentary Short to V_{CC}
Power Dissipation 450mW
Storage Temperature Range
N/P (Plastic) Packages . . . . . −25°C to +100°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C
Thermal Resistance
Junction to Ambient/Junction to Case
N/P (Plastic) Packages . . . . . 140/55°C/W

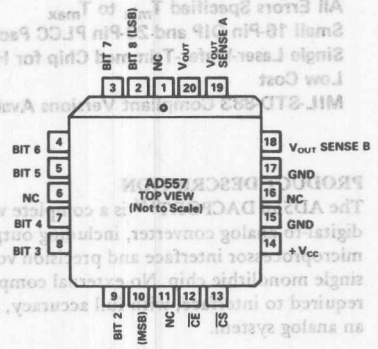
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

DIP



PLCC



ORDERING GUIDE

Model	Package Option*	Temperature
AD557JN	Plastic (N-16)	0 to +70°C
AD557JP	PLCC (P-20A)	0 to +70°C

*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

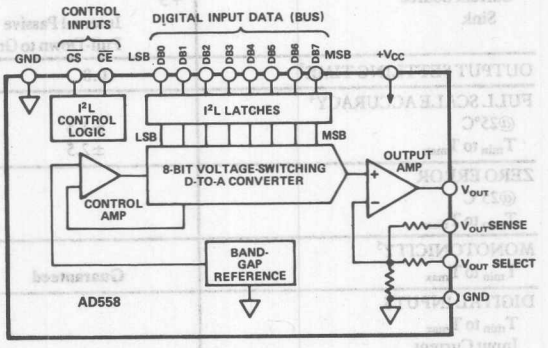
DACPORT Low Cost, Complete µP-Compatible 8-Bit DAC

AD558

FEATURES

- Complete 8-Bit DAC
- Voltage Output — 2 Calibrated Ranges
- Internal Precision Band-Gap Reference
- Single-Supply Operation: +5V to +15V
- Full Microprocessor Interface
- Fast: 1µs Voltage Settling to ±1/2LSB
- Low Power: 75mW
- No User Trims
- Guaranteed Monotonic Over Temperature
- All Errors Specified T_{min} to T_{max}
- Small 16-Pin DIP and 20-Pin PLCC Packages
- Single Laser-Wafer-Trimmed Chip for Hybrids
- Low Cost
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD558 DACPORT™ is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The performance and versatility of the DACPORT is a result of several recently-developed monolithic bipolar technologies. The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single +5V to +15V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range (all grades), while recent advances in laser-wafer-trimming of these thin-film resistors permit absolute calibration at the factory to within ±1LSB; thus no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 800ns.

The AD558 is available in four performance grades. The AD558J and K are specified for use over the 0 to +70°C temperature range, while the AD558S and T grades are specified for −55°C to +125°C operation. The "J" and "K" grades are available either in 16-pin plastic (N) or hermetic ceramic (D) DIPS. They are also available in 20-pin JEDEC standard PLCC packages. The "S" and "T" grades are available in the 16-pin hermetic ceramic DIP package.

***Protected by U.S. Patent Nos. 3,887,863; 3,685,045; 4,323,795; Patents Pending.**

DACPORT is a trademark of Analog Devices, Inc.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allow the AD558 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.
2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
4. The voltage-switching structure of the AD558 DAC section along with a high-speed output amplifier and laser-trimmed resistors give the user a choice of 0V to +2.56V or 0V to +10V output ranges, selectable by pin-strapping. Circuitry is internally compensated for minimum settling time on both ranges; typically settling to ±1/2LSB for a full-scale 2.55 volt step in 800ns.
5. The AD558 is designed and specified to operate from a single +4.5V to +16.5V power supply.
6. Low digital input currents, 100µA max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible over the entire operating V_{CC} range.
7. All AD558 grades are available in chip form with guaranteed specifications from +25°C to T_{max}. MIL-STD-883, Class B visual inspection is standard on Analog Devices bipolar chips. Contact the factory for additional chip information.
8. The AD558 is available in versions compliant with MIL-STD-883. Refer to Analog Devices Military Products Databook or current AD588/883B data sheet for detailed specifications.

SPECIFICATIONS (@ T_A = +25°C, V_{CC} = +5V to +15V unless otherwise specified)

Model	AD558J			AD558K			AD558S[1]			AD558T[1]			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			8			8			8			8	Bits
RELATIVE ACCURACY[2]													
0 to +70°C			±1/2			±1/4			±1/2			±1/4	LSB
−55°C to +125°C									±3/4			±3/8	LSB
OUTPUT													
Ranges[3]		0 to +2.56			0 to +2.56			0 to +2.56			0 to +2.56		V
		0 to +10			0 to +10			0 to +10			0 to +10		V
Current Source	+5			+5			+5			+5			mA
Sink		Internal Passive Pull-Down to Ground[4]			Internal Passive Pull-Down to Ground			Internal Passive Pull-Down to Ground			Internal Passive Pull-Down to Ground		
OUTPUT SETTLING TIME[5]													
0 to 2.56 Volt Range		0.8	1.5		0.8	1.5		0.8	1.5		0.8	1.5	µs
0 to 10 Volt Range[4]		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	µs
FULL SCALE ACCURACY[6]													
@25°C			±1.5			±0.5			±1.5			±0.5	LSB
T_{min} to T_{max}			±2.5			±1			±2.5			±1	LSB
ZERO ERROR													
@25°C			±1			±1/2			±1			±1/2	LSB
T_{min} to T_{max}			±2			±1			±2			±1	LSB
MONOTONICITY[7] T_{min} to T_{max}		Guaranteed			Guaranteed			Guaranteed			Guaranteed		
DIGITAL INPUTS													
T_{min} to T_{max} Input Current			±100			±100			±100			100	µA
Data Inputs, Voltage													
Bit On – Logic "1"	2.0			2.0			2.0			2.0			V
Bit On – Logic "0"	0		0.8	0		0.8	0		0.8	0		0.8	V
Control Inputs, Voltage													
On – Logic "1"	2.0			2.0			2.0			2.0			V
On – Logic "0"	0		0.8	0		0.8	0		0.8	0		0.8	V
Input Capacitance		4			4			4			4		pF
TIMING													
t_W Strobe Pulse Width	200			200			200			200			ns
T_{min} to T_{max}	270			270			270			270			ns
t_{DH} Data Hold Time	10			10			10			10			ns
T_{min} to T_{max}	10			10			10			10			ns
t_{DS} Data Set-Up Time	200			200			200			200			ns
T_{min} to T_{max}	270			270			270			270			ns
POWER SUPPLY													
Operating Voltage Range (V_{CC})													
2.56 Volt Range	+4.5		+16.5	+4.5		+16.5	+4.5		+16.5	+4.5		+16.5	V
10 Volt Range	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	V
Current (I_{CC})		15	25		15	25		15	25		15	25	mA
Rejection Ratio			0.03			0.03			0.03			0.03	%/%
POWER DISSIPATION, V_{CC} = 5V		75	125		75	125		75	125		75	125	mW
V_{CC} = 15V		225	375		225	375		225	375		225	375	mW
OPERATING TEMPERATURE RANGE	0		+70	0		+70	−55		+125	−55		+125	°C

NOTES

[1]The AD558 S & T grades are available processed and screened to MIL-STD-883 Class B. Consult Analog Devices' Military Databook for details.

[2]Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the offset to the full scale of the device. See "Measuring Offset Error".

[3]Operation of the 0 to 10 volt output range requires a minimum supply voltage of +11.4 volts.

[4]Passive pull-down resistance is 2kΩ for 2.56 volt range, 10kΩ for 10 volt range.

[5]Settling time is specified for a positive-going full-scale step to ±1/2LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.

[6]The full range output voltage for the 2.56 range is 2.55V and is guaranteed with a +5V supply, for the 10V range, it is 9.960V guaranteed with a +15V supply.

[7]A monotonic converter has a maximum differential linearity error of ±1LSB.

Specifications shown in **boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

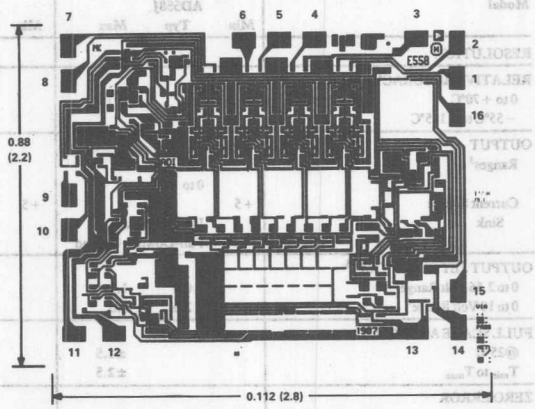
ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Ground . . . . . 0V to +18V
Digital Inputs (Pins 1-10) . . . . . 0V to +7.0V
V_{OUT} . . . . . Indefinite Short to Ground
Momentary Short to V_{CC}
Power Dissipation 450mW
Storage Temperature Range
N/P (Plastic) Packages . . . . . −25°C to +100°C
D (Ceramic) Package . . . . . −55°C to +150°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C
Thermal Resistance
Junction to Ambient/Junction to Case
D (Ceramic) Package . . . . . 100/30°C/W
N/P (Plastic) Packages . . . . . 140/55°C/W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AD558 METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



ORDERING GUIDE

Model[1]	Temperature	Relative Accuracy Error Max T_{min} to T_{max}	Full Scale Error, Max T_{min} to T_{max}	Package Option[2]
AD558JN	0 to +70°C	±1/2LSB	±2.5LSB	Plastic (N-16)
AD558JP	0 to +70°C	±1/2LSB	±2.5LSB	PLCC (P-20A)
AD558JD	0 to +70°C	±1/2LSB	±2.5LSB	TO-116 (D-16)
AD558KN	0 to +70°C	±1/4LSB	±1LSB	Plastic (N-16)
AD558KP	0 to +70°C	±1/4LSB	±1LSB	PLCC (P-20A)
AD558KD	0 to +70°C	±1/4LSB	±1LSB	TO-116 (D-16)
AD558SD	−55°C to +125°C	±3/4LSB	±2.5LSB	TO-116 (D-16)
AD558TD	−55°C to +125°C	±3/8LSB	±1LSB	TO-116 (D-16)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices' Military Products Databook or current AD558/883B data sheet.
[2]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

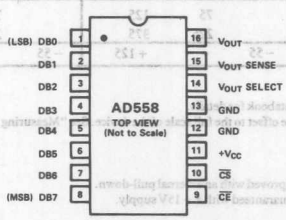


Figure 1a. AD558 Pin Configuration (DIP)

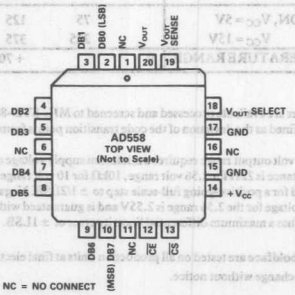


Figure 1b. AD558 Pin Configuration (PLCC)

High Speed 12-Bit Monolithic D/A Converters

AD565A*/AD566A*

FEATURES

- Single Chip Construction
- Very High-Speed Settling to 1/2LSB
  - AD565A: 250ns max
  - AD566A: 350ns max
- Full-Scale Switching Time: 30ns
- Guaranteed for Operation with ±12V Supplies: AD565A with -12V Supply: AD566A
- Linearity Guaranteed Over Temperature: 1/2LSB max (K, T Grades)
- Monotonicity Guaranteed Over Temperature
- Low Power: AD566A = 180mW max; AD565A = 225mW max
- Use with On-Board High-Stability Reference (AD565A) or with External Reference (AD566A)
- Low Cost
- MIL-STD-883-Compliant Versions Available

PRODUCT DESCRIPTION

The AD565A and AD566A are fast 12-bit digital-to-analog converters which incorporate the latest advances in analog circuit design to achieve high speeds at low cost.

The AD565A and AD566A use 12 precision, high-speed bipolar current-steering switches, control amplifier and a laser-trimmed thin-film resistor network to produce a very fast, high accuracy analog output current. The AD565A also includes a buried zener reference that features low-noise, long-term stability and temperature drift characteristics comparable to the best discrete reference diodes.

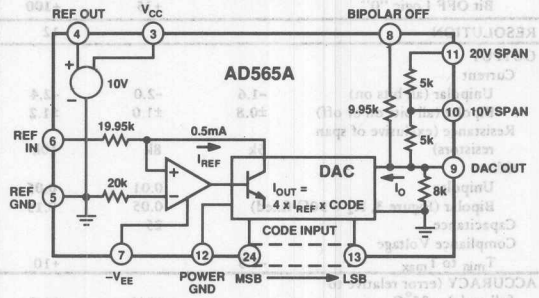
The combination of performance and flexibility in the AD565A and AD566A has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD565A and AD566A have a 10-90% full-scale transition time less than 35ns and settle to within ±1/2LSB in 250ns max (350ns for AD566A). Both are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. High speed and accuracy make the AD565A and AD566A the ideal choice for high-speed display drivers as well as fast analog-to-digital converters.

The laser trimming process which provides the excellent linearity is also used to trim both the absolute value and the temperature coefficient of the reference of the AD565A resulting in a typical full-scale gain TC of 10 ppm/°C. When tighter TC performance is required or when a system reference is available, the AD566A may be used with an external reference.

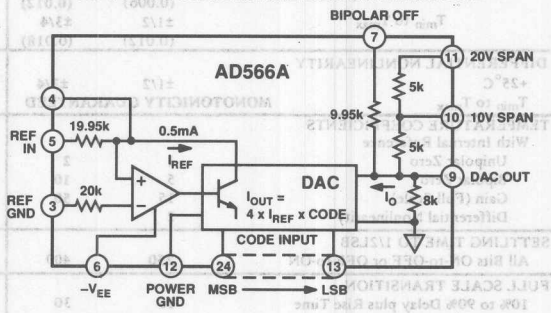
*Covered by Patent Nos.: 3,803,590; RE 28,633; 4,213,806; 4,136,349; 4,020,486; 3,747,088.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD565A FUNCTIONAL BLOCK DIAGRAM



AD566A FUNCTIONAL BLOCK DIAGRAM



AD565A and AD566A are available in four performance grades. The J and K are specified for use over the 0 to +70°C temperature range while the S and T grades are specified for the −55°C to +125°C range. The D grades are all packaged in a 24-pin, hermetically sealed, ceramic, dual-in-line package. The JR grade is packaged in a 28-pin plastic SOIC.

PRODUCT HIGHLIGHTS

1. The wide output compliance range of the AD565A and AD566A are ideally suited for fast, low noise, accurate voltage output configurations without an output amplifier.
2. The devices incorporate a newly developed, fully differential, nonsaturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562/3 with very fast switching times and an optimally-damped settling characteristic.
3. The devices also contain SiCr thin film application resistors which can be used with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full-scale and bipolar offset errors.
4. The AD565A and AD566A are available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current /883B data sheet for detailed specifications.

DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	−1.5		+10	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S. Range
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}		**MONOTONICITY GUARANTEED**			**MONOTONICITY GUARANTEED**		
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	50		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250	400		250	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage	−65		+150	−65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, −11.4 to −16.5V dc		−12	−18		−12	−18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = −11.4 to −16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 2, 3, 4)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)[3]	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

NOTES

[1] The digital inputs are guaranteed but not tested over the operating temperature range.

[2] The power supply gain sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V dc.

[3] For operation at elevated temperatures the reference cannot supply current for external loads. It, therefore, should be buffered if additional loads are to be supplied.

Specifications subject to change without notice.

MODEL	AD565AS MIN	AD565AS TYP	AD565AS MAX	AD565AT MIN	AD565AT TYP	AD565AT MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	−1.5		+10	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of F.S. Range
T_{min} to T_{max}		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}		MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED		
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	30		10	15	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250	400		250	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, −11.4 to −16.5V dc		−12	−18		−12	−18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = −11.4 to −16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGES (see Figures 2, 3, 4)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)[3]	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

AD566A—SPECIFICATIONS (T_A = +25°C, V_{EE} = −15V, unless otherwise specified.)

MODEL	AD566AJ MIN	AD566AJ TYP	AD566AJ MAX	AD566AK MIN	AD566AK TYP	AD566AK MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION		12			12		Bits
OUTPUT							
Current							
Unipolar (all bits on)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.R.
Bipolar (Figure 4 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.R.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	−1.5		+10	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.R.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.R.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		3	5	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, −11.4 to −16.5V dc		−12	−18		−12	−18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{EE} = −11.4 to −16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 3, 4, 5)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.R.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S.R.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.R.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.R.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants		Two (2): Bipolar Operation at Digital Input Only					
Reference Voltage		+1V to +10V, Unipolar					
Accuracy		10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage					
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)		40kHz typ					
Output Slew Rate 10%–90%		5mA/μs					
90%–10%		1mA/μs					
Output Settling Time (all bits on and a 0–10V step change in reference voltage)		1.5μs to 0.01% F.S.					
CONTROL AMPLIFIER							
Full Power Bandwidth		300kHz					
Small-Signal Closed-Loop Bandwidth		1.8MHz					

NOTES
[1] The digital input levels are guaranteed but not tested over the temperature range.
[2] The power supply gain sensitivity is tested in reference to a V_{EE} of −15V dc.
Specifications subject to change without notice.

MODEL	AD566AS MIN	AD566AS TYP	AD566AS MAX	AD566AT MIN	AD566AT TYP	AD566AT MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.R.
Bipolar (Figure 4 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.R
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	−1.5		+10	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.R.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.R.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		3	5	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits On-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, −11.4 to −16.5V dc		−12	−18		−12	−18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{EE} = −11.4 to −16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE (see Figures 3, 4, 5)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.R.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S.R.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.R.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.R.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW

MULTIPLYING MODE PERFORMANCE (All Models)	
Quadrants	Two (2): Bipolar Operation at Digital Input Only
Reference Voltage	+1V to +10V, Unipolar
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)	40kHz typ
Output Slew Rate 10%–90%	5mA/μs
90%–10%	1mA/μs
Output Settling Time (all bits on and a 0–10V step change in reference voltage)	1.5μs to 0.01% F.S.

CONTROL AMPLIFIER	
Full Power Bandwidth	300kHz
Small-Signal Closed-Loop Bandwidth	1.8MHz

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground . . . . . 0V to +18V
V_{EE} to Power Ground (AD565A) . . . . . 0V to −18V
Voltage on DAC Output (Pin 9) . . . . . −3V to +12V
Digital Inputs (Pins 13 to 24) to
Power Ground . . . . . −1.0V to +7.0V
Ref in to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref out (AD565A) . . . . . Indefinite Short to Power Ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

AD565A ORDERING GUIDE

Model[1]	Max Gain T.C. (ppm of F.S./°C)	Temperature Range	Linearity Error Max @ +25°C	Package Option[2]
AD565AJD	50	0 to +70°C	±1/2LSB	Ceramic (D-24)
AD565AJR	50	0 to +70°C	±1/2LSB	SOIC (R-28)
AD565AKD	20	0 to +70°C	±1/4LSB	Ceramic (D-24)
AD565ASD	30	−55°C to +125°C	±1/2LSB	Ceramic (D-24)
AD565ATD	15	−55°C to +125°C	±1/4LSB	Ceramic (D-24)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current /883B data sheet.
[2]D = Ceramic DIP, R = SOIC. For outline information see Package Information section.

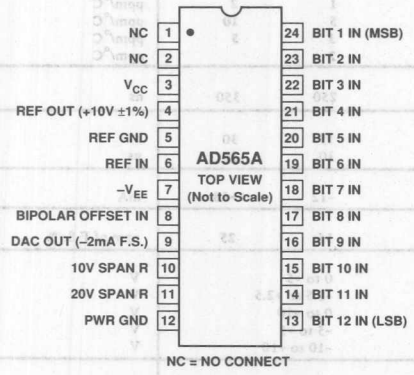
AD566A ORDERING GUIDE

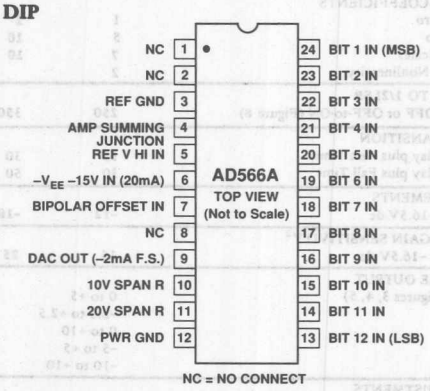
Model[1]	Max Gain T.C. (ppm or F.S./°C)	Temperature Range	Linearity Error Max @ +25°C	Package Option[2]
AD566AJD	10	0 to +70°C	±1/2LSB	Ceramic (D-24)
AD566AKD	3	0 to +70°C	±1/4LSB	Ceramic (D-24)
AD566ASD	10	−55°C to +125°C	±1/2LSB	Ceramic (D-24)
AD566ATD	3	−55°C to +125°C	±1/4LSB	Ceramic (D-24)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current /883B data sheet.
[2]D = Ceramic DIP. For outline information see Package Information section.

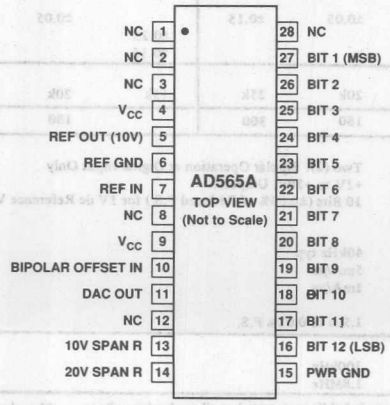
PIN DESIGNATIONS

24-PIN DIP





28-PIN SOIC



ANALOG DEVICES

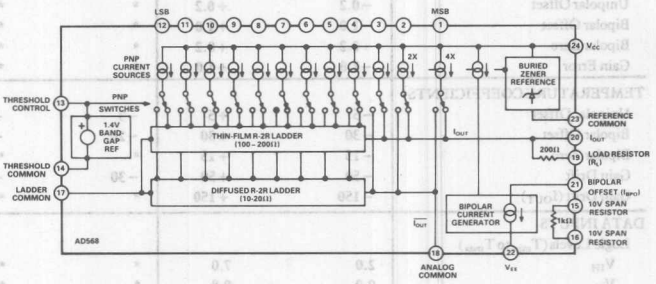
12-Bit Ultrahigh Speed Monolithic D/A Converter

AD568

FEATURES

- Ultrahigh Speed: Current Settling to 1LSB in 35ns
- High Stability Buried Zener Reference on Chip
- Monotonicity Guaranteed Over Temperature
- 10.24mA Full-Scale Output Suitable for Video Applications
- Integral and Differential Linearity Guaranteed Over Temperature
- 0.3" "Skinny DIP" Packaging
- Variable Threshold Allows TTL and CMOS Interface
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD568 is an ultrahigh-speed, 12-bit digital-to-analog converter (DAC) settling to 0.025% in 35ns. The monolithic device is fabricated using Analog Devices' Complementary Bipolar (CB) Process. This is a proprietary process featuring high-speed NPN and PNP devices on the same chip without the use of dielectric isolation or multichip hybrid techniques. The high speed of the AD568 is maintained by keeping impedance levels low enough to minimize the effects of parasitic circuit capacitances.

The DAC consists of 16 current sources configured to deliver a 10.24mA full-scale current. Multiple matched current sources and thin-film ladder techniques are combined to produce bit weighting. The DAC's output is a 10.24mA full scale (FS) for current output applications or a 1.024V FS unbuffered voltage output. Additionally, a 10.24V FS buffered output may be generated using an onboard 1kΩ span resistor with an external op amp. Bipolar ranges are accomplished by pin strapping.

Laser wafer trimming insures full 12-bit linearity. All grades of the AD568 are guaranteed monotonic over their full operating temperature range. Furthermore, the output resistance of the DAC is trimmed to 100Ω ± 1.0%. The gain temperature coefficient of the voltage output is 30ppm/°C max (K).

The AD568 is available in three performance grades. The AD568JQ and KQ are available in 24-pin cerdip (0.3") packages and are specified for operation from 0 to +70°C. The AD568SQ features operation from −55°C to +125°C and is also packaged in the hermetic 0.3" cerdip.

PRODUCT HIGHLIGHTS

1. The ultrafast settling time of the AD568 allows leading edge performance in waveform generation, graphics display and high-speed A/D conversion applications.
2. Pin strapping provides a variety of voltage and current output ranges for application versatility. Tight control of the absolute output current reduces trim requirements in externally-scaled applications.
3. Matched on-chip resistors can be used for precision scaling in high-speed A/D conversion circuits.
4. The digital inputs are compatible with TTL and +5V CMOS logic families.
5. Skinny DIP (0.3") packaging minimizes board space requirements and eases layout considerations.
6. The AD568 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD568/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD568—SPECIFICATIONS (@ = +25°C, V_{CC}, V_{EE} = ±15V unless otherwise noted.)

Model	AD568J			AD568K			AD568S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION	12			12			12			Bits
ACCURACY[1]										
Linearity	−1/2		+1/2	−1/4		+1/4	−1/2		+1/2	LSB
T_{min} to T_{max}	−3/4		+3/4	−1/2		+1/2	−3/4		+3/4	LSB
Differential Nonlinearity	−1		+1	−1/2		+1/2	−1		+1	LSB
T_{min} to T_{max}	−1		+1	−1		+1	−1		−1	LSB
Monotonicity	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE									
Unipolar Offset	−0.2		+0.2	*		*	*		*	% of FSR
Bipolar Offset	−1.0		+1.0	*		*	*		*	% of FSR
Bipolar Zero	−0.2		+0.2	*		*	*		*	% of FSR
Gain Error	−1.0		+1.0	*		*	*		*	% ofFSR
TEMPERATURE COEFFICIENTS[2]										
Unipolar Offset	−5		+5	−3		+3	−5		+5	ppm of FSR/°C
Bipolar Offset	−30		+30	−20		+20	−30		+30	ppm of FSR/°C
Bipolar Zero	−15		+15	*		*	*		*	ppm of FSR/°C
Gain Drift	−50		+50	−30		+30	−50		+50	ppm of FSR/°C
Gain Drift (I_{OUT})	−150		+150	*		*	*		*	ppm of FSR/°C
DATA INPUTS										
Logic Levels (T_{min} to T_{max})										
V_{IH}	2.0		7.0	*		*	*		*	V
V_{IL}	0.0		0.8	*		*	*		*	V
Logic Currents (T_{min} to T_{max})										
I_{IH}	−10	0	+10	*	*	*	*	*	*	µA
I_{IL}	−0.5	−60	−100	*	*	*	*	−100	−200	µA
V_{TH} Pin Voltage		1.4			*			*		V
CODING	BINARY, OFFSET BINARY									
CURRENT OUTPUT RANGES	0 to 10.24, ±5.12									mA
VOLTAGE OUTPUT RANGES	0 to 1.024, ±0.512									V
COMPLIANCE VOLTAGE	−2		+1.2	*		*	*		*	V
OUTPUT RESISTANCE										
Exclusive of R_L	160	200	240		*			*		Ω
Inclusive of R_L	99	100	101		*			*		Ω
SETTLING TIME										
Current to										
±0.025%		35			*			*		ns to 0.025% of FSR
±0.1%		23			*			*		ns to 0.1% of FSR
Voltage										
50Ω Load[3], 0.512V p-p,										
to 0.025%		37			*			*		ns to 0.025% of FSR
to 0.1%		25			*			*		ns to 0.1% of FSR
to 1%		18			*			*		ns to 1% of FSR
75Ω Load[3], 0.768V p-p,										
to 0.025%		40			*			*		ns to 0.025% of FSR
to 0.1%		25			*			*		ns to 0.1% of FSR
to 1%		20			*			*		ns to 1% of FSR
100Ω (Internal R_L)[3], 1.024V p-p,										
to 0.025%		50			*			*		ns to 0.025% of FSR
to 0.1%		38			*			*		ns to 0.1% of FSR
to 1%		24			*			*		ns to 1% of FSR
Glitch Impulse[4]		350			*			*		pV-sec
Peak Amplitude		15			*			*		% of FSR
FULL-SCALE TRANSITION[5]										
10% to 90% Rise Time		11			*			*		ns
90% to 10% Fall Time		11			*			*		ns
POWER REQUIREMENTS										
+13.5V to +16.5V		27	32		*	*		*	*	mA
−13.5V to −16.5V		−7	−8		*	*		*	*	mA
Power Dissipation		525	625		*	*		*	*	mW
PSRR			0.05			*			*	% of FSR/V
TEMPERATURE RANGE										
Rated Specification[2]	0		70	0		70	−55		+125	°C
Storage	−65		+150	*		*	*		*	°C

NOTES

*Same as AD568J.

[1]Measured in I_{OUT} mode.

[2]Measured in V_{OUT} mode, unless otherwise specified. See text for further information.

[3]Total Resistance. Refer to Figure 3.

[4]At the major carry, driven by HCMOS logic. See text for further explanation.

[5]Measured in V_{OUT} mode.

Specifications shown in boldface are tested on all production units at final electrical test.
Specifications subject to change without notice.

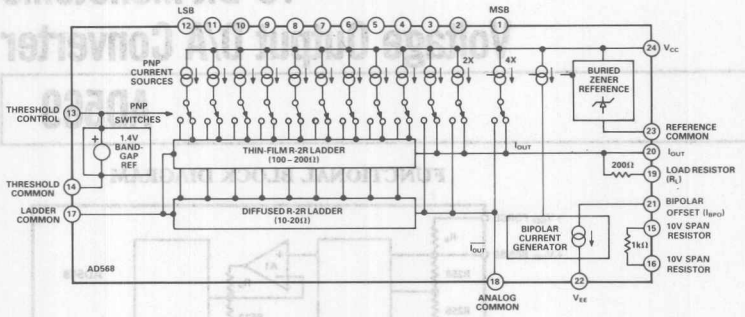
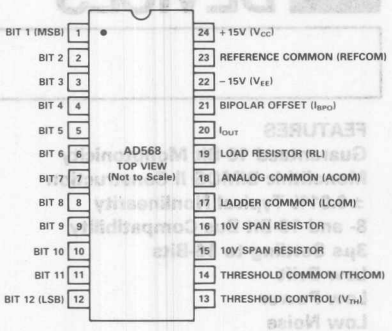


Figure 1. Functional Block Diagram

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

V_{CC} to REFCOM	0V to +18V
V_{EE} to REFCOM	0V to −18V
REFCOM to LCOM	+100mV to −10V
ACOM to LCOM	±100mV
THCOM to LCOM	±500mV
SPANs to LCOM	±12V
I_{BPO} to LCOM	±5V
I_{OUT} to LCOM	−5V to V_{TH}
Digital Inputs to THCOM	−500mV to +7.0V
Voltage Across Span Resistor	12V
V_{TH} to THCOM	−0.7V to +1.4V
Logic Threshold Control Input Current	5mA
Power Dissipation	1000mW
Storage Temperature Range	
Q (Cerdip) Package	−65°C to +150°C
Junction Temperature	175°C
Thermal Resistance	
θ_{ja}	75°C/W
θ_{jc}	25°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Package Option[2]	Temperature Range °C	Linearity Error Max. @ 25°C	Voltage Gain T.C. Max ppm/°C
AD568JQ	24-Lead Cerdip (Q-24)	0 to +70	±1/2	±50
AD568KQ	24-Lead Cerdip (Q-24)	0 to +70	±1/4	±30
AD568SQ	24-Lead Cerdip (Q-24)	−55 to +125	±1/2	±50

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD568/883B data sheet.
[2]Q = Cerdip. For outline information see Package Information section.

Definitions

LINEARITY ERROR (also called INTEGRAL NON-LINEARITY OR INL): Analog Devices defines linearity error as the maximum deviation of the actual analog output from the ideal output (a straight line drawn from 0 to FS) for any bit combination expressed in multiples of 1LSB. The AD568 is laser trimmed to 1/4LSB (0.006% of FS) maximum linearity error at +25°C for the K version and 1/2LSB for the J and S versions.

DIFFERENTIAL LINEARITY ERROR (also called DIFFERENTIAL NONLINEARITY or DNL): DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. Monotonic behavior requires that the differential linearity error not exceed 1LSB in the negative direction.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases.

UNIPOLAR OFFSET ERROR: The deviation of the analog output from the ideal (0V or 0mA) when the inputs are set to all 0s is called unipolar offset error.

BIPOLAR OFFSET ERROR: The deviation of the analog output from the ideal (negative half-scale) when the inputs are set to all 0s is called bipolar offset error.

BIPOLAR ZERO ERROR: The deviation of the analog output from the ideal half-scale output of 0V (or 0mA) for bipolar mode when only the MSB is on (100.....00) is called bipolar zero error.

GAIN ERROR: The difference between the ideal and actual output span of FS −1LSB, expressed in % of FS, or LSB, when all bits are on.

GLITCH IMPULSE: Asymmetrical switching times in a DAC give rise to undesired output transients which are quantified by their glitch impulse. It is specified as the net area of the glitch in nV-sec or pA-sec.

16-Bit Monotonic Voltage Output D/A Converter

AD569

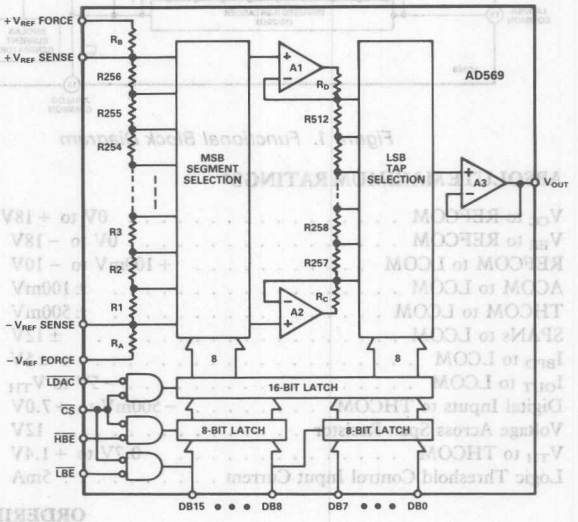
FEATURES

- Guaranteed 16-Bit Monotonicity
- Monolithic BiMOS II Construction
- ±0.01% Typical Nonlinearity
- 8- and 16-Bit Bus Compatibility
- 3μs Settling to 16-Bits
- Low Drift
- Low Power
- Low Noise

APPLICATIONS

- Robotics
- Closed-Loop Positioning
- High-Resolution ADCs
- Microprocessor-Based Process Control
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD569 is a monolithic 16-bit digital-to-analog converter (DAC) manufactured in Analog Devices' BiMOS II process. BiMOS II allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry. The AD569 chip includes two resistor strings, selector switches, decoding logic, buffer amplifiers, and double-buffered input latches.

The AD569's voltage-segmented architecture insures 16-bit monotonicity over time and temperature. Integral nonlinearity is maintained at ±0.01%, while differential nonlinearity is ±0.0004%. The on-chip, high-speed buffer amplifiers provide a voltage output settling time of 3μs to within ±0.001% for a full-scale step.

The reference input voltage which determines the output range can be either unipolar or bipolar. Nominal reference range is ±5V and separate reference force and sense connections are provided for high accuracy applications. The AD569 can operate with an ac reference in multiplying applications.

Data may be loaded into the AD569's input latches from 8- and 16-bit buses. The double-buffered structure simplifies 8-bit bus interfacing and allows multiple DACs to be loaded asynchronously and updated simultaneously. Four TTL/LSTTL/5V CMOS-compatible signals control the latches: $\overline{CS}$, $\overline{LBE}$, $\overline{HBE}$, and $\overline{LDAC}$.

The AD569 is available in five grades: J and K versions are specified from 0 to +70°C and are packaged in a 28-pin plastic DIP and 28-pin PLCC package; AD and BD versions are specified from −25°C to +85°C and are packaged in a 28-pin ceramic DIP. The SD version, also in a 28-pin ceramic DIP, is specified from −55°C to +125°C.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. Monotonicity to 16 bits is insured by the AD569's voltage-segmented architecture.
2. The output range is ratiometric to an external reference or ac signal. Gain error and gain drift of the AD569 are negligible.
3. The AD569's versatile data input structure allows loading from 8- and 16-bit buses.
4. The on-chip output buffer amplifier can supply ±5V into a 1kΩ load, and can drive capacitive loads of up to 1000pF.
5. Kelvin connections to the reference inputs preserve the gain and offset accuracy of the transfer function in the presence of wiring resistances and ground currents.
6. The AD569 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD569/883B data sheet for detailed specifications.

SPECIFICATIONS (T_A = +25°C, $+V_S$ = +12V, $-V_S$ = −12V, $+V_{REF}$ = +5V, $-V_{REF}$ = −5V, unless otherwise noted.)

Model	AD569JN/JP/AD			AD569KN/KP/BD			AD569SD			
Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
RESOLUTION			16			16			16	Bits
LOGIC INPUTS										
V_{IH} (Logic "1")	2.0		5.5	2.0		5.5	2.0		5.5	Volts
V_{IL} (Logic "0")	0		0.8	0		0.8	0		0.8	Volts
I_{IH} (V_{IH} = 5.5V)			10			10			10	μA
I_{IL} (V_{IL} = 0V)			10			10			10	μA
TRANSFER FUNCTION CHARACTERISTICS										
Integral Nonlinearity		±0.02	±0.04		±0.01	±0.024			±0.04	% FSR[1]
T_{min} to T_{max}		±0.02	±0.04		±0.020	±0.024			±0.04	% FSR
Differential Nonlinearity		±1/2	±1		±1/4	±1/2			±1	LSB
T_{min} to T_{max}		±1/2	±1		±1/2	±1			±1	LSB
Unipolar Offset[2]			±500			±350			±500	μV
T_{min} to T_{max}			±750			±450			±750	μV
Bipolar Offset[2]			±500			±350			±500	μV
T_{min} to T_{max}			±750			±450			±750	μV
Full Scale Error[2]			±350			±350			±350	μV
T_{min} to T_{max}			±750			±750			±750	μV
Bipolar Zero[2]			±0.04			±0.024			±0.04	% FSR
T_{min} to T_{max}			±0.04			±0.024			±0.04	% FSR
REFERENCE INPUT										
$+V_{REF}$ Range[3]	−5		+5	−5		+5	−5		+5	Volts
$-V_{REF}$ Range[3]	−5		+5	−5		+5	−5		+5	Volts
Resistance	15	20	25	15	20	25	15	20	25	kΩ[4]
OUTPUT CHARACTERISTICS										
Voltage	−5		+5	−5		+5	−5		+5	Volts
Capacitive Load			1000			1000			1000	pF
Resistive Load	1			1			1			kΩ
Short Circuit Current		10			10			10		mA
POWER SUPPLIES										
Voltage										
$+V_S$	+10.8	+12	+13.2	+10.8	+12	+13.2	+10.8	+12	+13.2	Volts
$-V_S$	−10.8	−12	−13.2	−10.8	−12	−13.2	−10.8	−12	−13.2	Volts
Current										
$+I_S$		+9	+13		+9	+13		+9	+13	mA
$-I_S$		−9	−13		−9	−13		−9	−13	mA
Power Supply Sensitivity[5]										
$+10.8V \le +V_S \le +13.2V$		±0.5	±2		±0.5	±2		±0.5	±2	ppm/%
$-10.8V \ge -V_S \ge -13.2V$		±1	±3		±1	±3		±1	±3	ppm/%
TEMPERATURE RANGE										
Specified										
JN, KN, JP, KP	0		+70	0		+70				°C
AD, BD	−25		+85	−25		+85				°C
SD							−55		+125	°C
Storage										
JN, KN, JP, KP	−65		+150	−65		+150				°C
AD, BD, SD	−65		+150	−65		+150	−65		+150	°C

NOTES
[1]FSR stands for Full-Scale Range, and is 10V for a −5 to +5V span.
[2]Refer to Definitions section.
[3]For operation with supplies other than ±12V, refer to the Power Supply and Reference Voltage Range Section.
[4]Measured between $+V_{REF}$ Force and $-V_{REF}$ Force.
[5]Sensitivity of Full-Scale Error due to changes in $+V_S$ and sensitivity of Offset to changes in $-V_S$.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance Only and are not subject to test.
$+V_S = +12V; -V_S = -12V; +V_{REF} = +5V; -V_{REF} = -5V$ except where stated.

Parameter	Limit	Units	Test Conditions/Comments
Output Voltage Settling	5	µs max	No Load Applied
(Time to ±0.001% FS	3	µs typ	(DAC output measured from falling edge of $\overline{LDAC}$.)
For FS Step)	6	µs max	V_{OUT} Load = 1kΩ, C_{LOAD} = 1000pF.
	4	µs typ	(DAC output measured from falling edge of $\overline{LDAC}$.)
Digital-to-Analog Glitch Impulse	500	nV-sec typ	Measured with V_{REF} = 0V. DAC registers alternatively loaded with input codes of 8000_H and $0FFF_H$ (worst-case transition). Load = 1kΩ.
Multiplying Feedthrough	−100	dB max	$+V_{REF}$ = 1V rms 10kHz sine wave, $-V_{REF}$ = 0V
Output Noise Voltage Density (1kHz-1MHz)	40	nV/√Hz typ	Measured between V_{OUT} and $-V_{REF}$

TIMING CHARACTERISTICS ($+V_S = +12V, -V_S = -12V, V_{IH} = 2.4V, V_{IL} = 0.4V, T_{min}$ to T_{max})

Parameter	Limit	Units	Test Conditions/Comments
Case A			150ns Pulse on $\overline{HBE}$, $\overline{LBE}$, and $\overline{LDAC}$ T_{HS} = 140ns min, T_{HH} = 10ns min
t_{WC}	120	ns min	$\overline{CS}$ Pulse Width
t_{SC}	60	ns min	$\overline{CS}$ Data Setup Time
t_{HC}	20	ns min	$\overline{CS}$ Data Hold Time
Case B			None
t_{WB}	70	ns min	$\overline{HBE}$, $\overline{LBE}$ Pulse Width
t_{SB}	80	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Setup Time
t_{HB}	20	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Hold Time
t_{SCS}	120	ns min	$\overline{CS}$ Setup Time
t_{HCS}	10	ns min	$\overline{CS}$ Hold Time
t_{WD}	120	ns min	$\overline{LDAC}$ Pulse Width
Case C			None
t_{WB}	120	ns min	$\overline{HBE}$, $\overline{LBE}$ Pulse Width
t_{SB}	80	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Setup Time
t_{HB}	20	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Hold Time
t_{SCS}	120	ns min	$\overline{CS}$ Setup Time
t_{HCS}	10	ns min	$\overline{CS}$ Hold Time

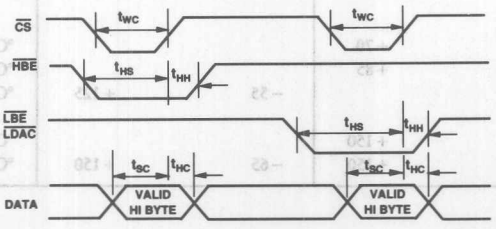


Figure 1. AD569 Timing Diagram – Case A

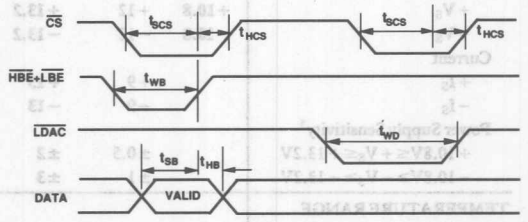


Figure 2a. AD569 Timing Diagram – Case B

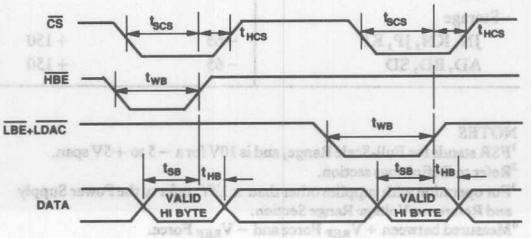


Figure 2b. AD569 Timing Diagram – Case C

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

$+V_S$ (Pin 1) to GND (Pin 18) . . . . . +18V, −0.3V
$-V_S$ (Pin 28) to GND (Pin 18) . . . . . −18V, +0.3V
$+V_S$ (Pin 1) to $-V_S$ (Pin 28) . . . . . +26.4V, −0.3V
Digital Inputs
(Pins 4–14, 19–27) to GND (Pin 18) . . . . . $+V_S$, −0.3V
$+V_{REF}$ Force (Pin 3) to $+V_{REF}$ Sense (Pin 2) . . . . . ±16.5V
$-V_{REF}$ Force (Pin 15) to $-V_{REF}$ Sense (Pin 16) . . . ±16.5V
V_{REF} Force (Pins 3, 15) to GND (Pin 18) . . . . . $\pm V_S$
V_{REF} Sense (Pins 2, 16) to GND (Pin 18) . . . . . $\pm V_S$
V_{OUT} (Pin 17) . . . . . Indefinite Short to GND
Momentary Short to $+V_S$, $-V_S$
Power Dissipation (Any Package) 1000mW
Operating Temperature Range
Commercial Plastic (JN, KN, JP, KP Versions) . 0 to +70°C
Industrial Ceramic (AD, BD Versions) . . −25°C to +85°C
Extended Ceramic (SD Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

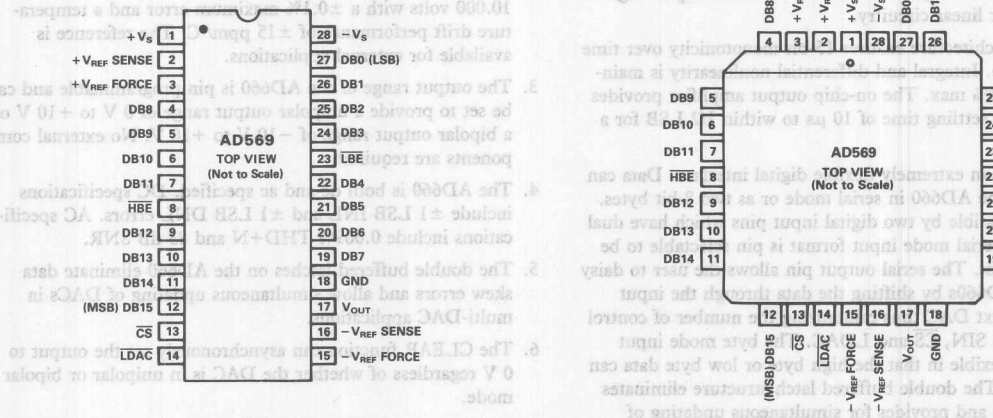
3

ESD SENSITIVITY

The AD569 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high-energy discharges (Human Body Model) and fast, low-energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD569 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.

PIN DESIGNATIONS



ORDERING GUIDE

Model[1]	Integral Nonlinearity +25°C	Integral Nonlinearity T_{min}–T_{max}	Differential Nonlinearity +25°C	Differential Nonlinearity T_{min}–T_{max}	Temperature Range	Package Option[2]
AD569JN	±0.04%	±0.04%	±1LSB	±1LSB	0 to +70°C	N-28
AD569JP	±0.04%	±0.04%	±1LSB	±1LSB	0 to +70°C	P-28A
AD569KN	±0.024%	±0.024%	±1/2LSB	±1LSB	0 to +70°C	N-28
AD569KP	±0.024%	±0.024%	±1/2LSB	±1LSB	0 to +70°C	P-28A
AD569AD	±0.04%	±0.04%	±1LSB	±1LSB	−25°C to +85°C	D-28
AD569BD	±0.024%	±0.024%	±1/2LSB	±1LSB	−25°C to +85°C	D-28
AD569SD	±0.04%	±0.04%	±1LSB	±1LSB	−55°C to +125°C	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD569/883B data sheet.
[2]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

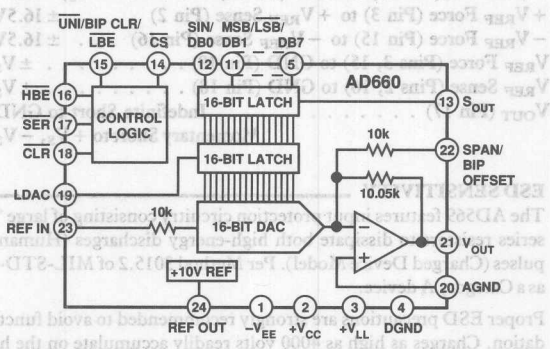
Monolithic 16-Bit Serial/Byte DACPORT

AD660

FEATURES

- Complete 16-Bit D/A Function
  - On-Chip Output Amplifier
  - On-Chip Buried Zener Voltage Reference
- ±1 LSB Integral Linearity
- 15-Bit Monotonic over Temperature
- Microprocessor Compatible
  - Serial or Byte Input
  - Double Buffered Latches
  - Fast (40 ns) Write Pulse
- Asynchronous Clear (to 0 V) Function
- Serial Output Pin Facilitates Daisy Chaining
- Unipolar or Bipolar Output
- Low Glitch: 15 nV-s
- Low THD+N: 0.009%

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD660 DACPORT® is a complete 16-bit monolithic D/A converter with an on-board voltage reference, double buffered latches and output amplifier. It is manufactured on Analog Devices' BiMOS II process. This process allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry.

The AD660's architecture ensures 15-bit monotonicity over time and temperature. Integral and differential nonlinearity is maintained at ±0.003% max. The on-chip output amplifier provides a voltage output settling time of 10 μs to within 1/2 LSB for a full-scale step.

The AD660 has an extremely flexible digital interface. Data can be loaded into the AD660 in serial mode or as two 8-bit bytes. This is made possible by two digital input pins which have dual functions. The serial mode input format is pin selectable to be MSB or LSB first. The serial output pin allows the user to daisy chain several AD660s by shifting the data through the input latch into the next DAC thus minimizing the number of control lines required to SIN, $\overline{CS}$ and LDAC. The byte mode input format is also flexible in that the high byte or low byte data can be loaded first. The double buffered latch structure eliminates data skew errors and provides for simultaneous updating of DACs in a multi-DAC system.

The AD660 is available in five grades. AN and BN versions are specified from −40°C to +85°C and are packaged in a 24-pin 300 mil plastic DIP. AR and BR versions are also specified from −40°C to +85°C and are packaged in a 24-pin SOIC. The SQ version is packaged in a 24-pin 300 mil cerdip package and is also available compliant to MIL-STD-883. Refer to the AD660/883B data sheet for specifications and test conditions.

DACPORT is a registered trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. The AD660 is a complete 16-bit DAC, with a voltage reference, double buffered latches and output amplifier on a single chip.
2. The internal buried Zener reference is laser trimmed to 10.000 volts with a ±0.1% maximum error and a temperature drift performance of ±15 ppm/°C. The reference is available for external applications.
3. The output range of the AD660 is pin programmable and can be set to provide a unipolar output range of 0 V to +10 V or a bipolar output range of −10 V to +10 V. No external components are required.
4. The AD660 is both dc and ac specified. DC specifications include ±1 LSB INL and ±1 LSB DNL errors. AC specifications include 0.009% THD+N and 83 dB SNR.
5. The double buffered latches on the AD660 eliminate data skew errors and allow simultaneous updating of DACs in multi-DAC applications.
6. The CLEAR function can asynchronously set the output to 0 V regardless of whether the DAC is in unipolar or bipolar mode.
7. The output amplifier settles within 10 μs to ±1/2 LSB for a full-scale step and within 2.5 μs for a 1 LSB step over temperature. The output glitch is typically 15 nV-s when a full-scale step is loaded.

SPECIFICATIONS (T_A = +25°C, V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V unless otherwise noted)

Parameter	AD660AN/AR/SQ Min	Typ	Max	AD660BN/BR Min	Typ	Max	Units
RESOLUTION	16			16			Bits
DIGITAL INPUTS (T_{MIN} to T_{MAX})							
V_{IH} (Logic "1")	2.0		5.5	*		*	Volts
V_{IL} (Logic "0")	0		0.8	*		*	Volts
I_{IH} (V_{IH} = 5.5 V)			±10			*	μA
I_{IL} (V_{IL} = 0 V)			±10			*	μA
TRANSFER FUNCTION CHARACTERISTICS[1]							
Integral Nonlinearity			±2			±1	LSB
T_{MIN} to T_{MAX}			±4			±2	LSB
Differential Nonlinearity			±2			±1	LSB
T_{MIN} to T_{MAX}			±4			±2	LSB
Monotonicity Over Temperature	14			15			Bits
Gain Error[2, 3]			±0.10			*	% of FSR
Gain Drift[2] (T_{MIN} to T_{MAX})			25			15	ppm/°C
DAC Gain Error[4]			±0.05			*	% of FSR
DAC Gain Drift[4]			10			*	ppm/°C
Unipolar Offset			±2.5			*	mV
Unipolar Offset Drift (T_{MIN} to T_{MAX})			3			*	ppm/°C
Bipolar Zero Error			±7.5			*	mV
Bipolar Zero Error Drift (T_{MIN} to T_{MAX})			5			*	ppm/°C
REFERENCE INPUT							
Input Resistance	7	10	13	*	*	*	kΩ
Bipolar Offset Input Resistance	7	10	13	*	*	*	kΩ
REFERENCE OUTPUT							
Voltage	9.99	10.00	10.01	*	*	*	Volts
Drift			25			15	ppm/°C
External Current[5]	2	4		*	*		mA
Capacitive Load			1000			*	pF
Short Circuit Current		25			*		mA
OUTPUT CHARACTERISTICS							
Output Voltage Range							
Unipolar Configuration	0		+10	*		*	Volts
Bipolar Configuration	−10		+10	*		*	Volts
Output Current	5			*			mA
Capacitive Load			1000			*	pF
Short Circuit Current		25			*		mA
POWER SUPPLIES							
Voltage							
V_{CC}[6]	+13.5		+16.5	*		*	Volts
V_{EE}[6]	−13.5		−16.5	*		*	Volts
V_{LL}	+4.5		+5.5	*		*	Volts
Current (No Load)							
I_{CC}		+12	+18		*	*	mA
I_{EE}		−12	−18		*	*	mA
I_{LL}							
@ V_{IH}, V_{IL} = 5, 0 V		0.3	2		*	*	mA
@ V_{IH}, V_{IL} = 2.4, 0.4 V		3	7.5		*	*	mA
Power Supply Sensitivity		1	2		*	*	ppm/%
Power Dissipation (Static, No Load)		365	625		*	*	mW
TEMPERATURE RANGE							
Specified Performance (A, B)	−40		+85	*		*	°C
Specified Performance (S)	−55		+125				°C

NOTES

[1]For 16-bit resolution, 1 LSB = 0.0015% of FSR. For 15-bit resolution, 1 LSB = 0.003% of FSR. For 14-bit resolution, 1 LSB = 0.006% of FSR. FSR stands for Full-Scale Range and is 10 V in a Unipolar Mode and 20 V in Bipolar Mode.

[2]Gain error and gain drift are measured using the internal reference. The internal reference is the main contributor to gain drift. If lower gain drift is required, the AD660 can be used with a precision external reference such as the AD587, AD586 or AD688.

[3]Gain Error is measured with fixed 50 Ω resistors as shown in the Application section. Eliminating these resistors increases the gain error by 0.25% of FSR (Unipolar mode) or 0.50% of FSR (Bipolar mode).

[4]DAC Gain Error and Drift are measured with an external voltage reference. They represent the error contributed by the DAC alone, for use with an external reference.

[5]External current is defined as the current available in addition to that supplied to REF IN and SPAN/BIPOLAR OFFSET on the AD660.

[6]Operation on ±12 V supplies is possible using an external reference such as the AD586 and reducing the output range. Refer to the Internal/External Reference section.

*Indicates that the specification is the same as AD660AN/AR/SQ.

Specifications subject to change without notice.

$T_{MIN} \le T_A \le T_{MAX}$, V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V except where noted.)

Parameter	Limit	Units	Test Conditions/Comments
Output Settling Time	13	µs max	20 V Step, T_A = +25°C
(Time to ±0.0008% FS	8	µs typ	20 V Step, T_A = +25°C
with 2 kΩ, 1000 pF Load)	10	µs typ	20 V Step, $T_{MIN} \le T_A \le T_{MAX}$
	6	µs typ	10 V Step, T_A = +25°C
	8	µs typ	10 V Step, $T_{MIN} \le T_A \le T_{MAX}$
	2.5	µs typ	1 LSB Step, $T_{MIN} \le T_A \le T_{MAX}$
Total Harmonic Distortion + Noise			
A, B, S Grade	0.009	% max	0 dB, 990.5 Hz; Sample Rate = 96 kHz; T_A = +25°C
A, B, S Grade	0.056	% max	−20 dB, 990.5 Hz; Sample Rate = 96 kHz; T_A = +25°C
A, B, S Grade	5.6	% max	−60 dB, 990.5 Hz; Sample Rate = 96 kHz; T_A = +25°C
Signal-to-Noise Ratio	83	dB min	T_A = +25°C
Digital-to-Analog Glitch Impulse	15	nV-s typ	DAC Alternately Loaded with 8000_H and $7FFF_H$
Digital Feedthrough	2	nV-s typ	DAC Alternately Loaded with 0000_H and $FFFF_H$; $\overline{CS}$ High
Output Noise Voltage Density (1 kHz–1 MHz)	120	nV/Rt Hz typ	Measured at V_{OUT}, 20 V Span; Excludes Reference
Reference Noise	125	nV/Rt Hz typ	Measured at REF OUT

Specifications subject to change without notice.

CAUTION

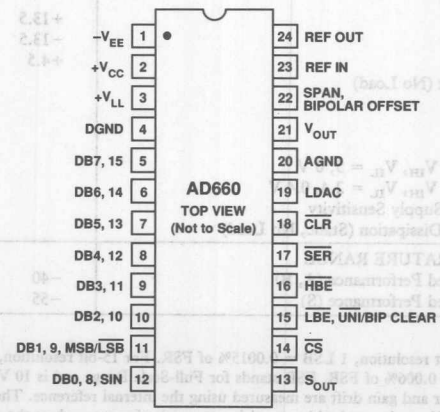
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD660 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to AGND . . . . . −0.3 V to +17.0 V
V_{EE} to AGND . . . . . +0.3 V to −17.0 V
V_{LL} to DGND . . . . . −0.3 V to +7 V
AGND to DGND . . . . . ±1 V
Digital Inputs (Pins 5 through 23) to DGND . . . . . −1.0 V to +7.0 V
REF IN to AGND . . . . . ±10.5 V
Span/Bipolar Offset to AGND . . . . . ±10.5 V
Ref Out, V_{OUT} . . . . . Indefinite Short To AGND, DGND, V_{CC}, V_{EE}, and V_{LL}
Power Dissipation (Any Package)
To +60°C . . . . . 1000 mW
Derates above +60°C . . . . . 8.7 mW/°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Linearity Error Max +25°C	Linearity Error Max $T_{MIN} - T_{MAX}$	Gain TC max ppm/°C	Package Description	Package Option*
AD660AN	−40°C to +85°C	±2 LSB	±4 LSB	25	Plastic DIP	N-28
AD660AR	−40°C to +85°C	±2 LSB	±4 LSB	25	SOIC	R-28
AD660BN	−40°C to +85°C	±1 LSB	±2 LSB	15	Plastic DIP	N-28
AD660BR	−40°C to +85°C	±1 LSB	±2 LSB	15	SOIC	R-28
AD660SQ	−55°C to +125°C	±2 LSB	±4 LSB	25	Cerdip	Q-28
AD660SQ/883B**	−55°C to +125°C	±2 LSB	**	**	**	**

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.
**Refer to AD660/883B military data sheet.

3

TIMING CHARACTERISTICS V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V, V_{HI} = 2.4 V, V_{LO} = 0.4 V

Parameter	Limit +25°C	Limit −55°C to +125°C	Units
(Figure 1a)			
$t_{\overline{CS}}$	40	50	ns min
t_{DS}	40	50	ns min
t_{DH}	0	10	ns min
t_{BES}	40	50	ns min
t_{BEH}	0	10	ns min
t_{LH}	80	100	ns min
t_{LW}	40	50	ns min
(Figure 1b)			
t_{CLK}	80	100	ns min
t_{LO}	30	50	ns min
t_{HI}	30	50	ns min
t_{SS}	0	10	ns min
t_{DS}	40	50	ns min
t_{DH}	0	10	ns min
t_{SH}	0	10	ns min
t_{LH}	80	100	ns min
t_{LW}	40	50	ns min
(Figure 1c)			
$t_{\overline{CLR}}$	80	110	ns min
t_{SET}	80	110	ns min
t_{HOLD}	0	10	ns min
(Figure 1d)			
t_{PROP}	50	100	ns min
t_{DS}	50	80	ns min

Specifications subject to change without notice.

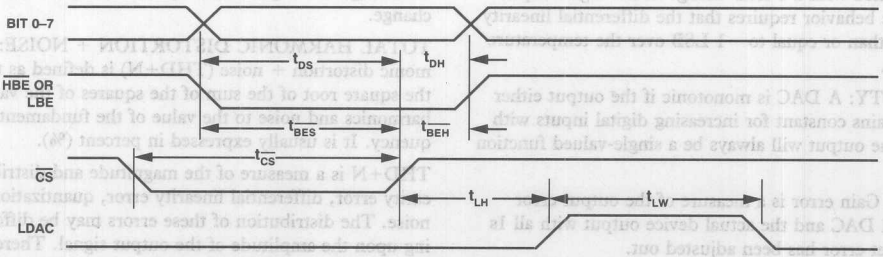


Figure 1a. AD660 Byte Load Timing

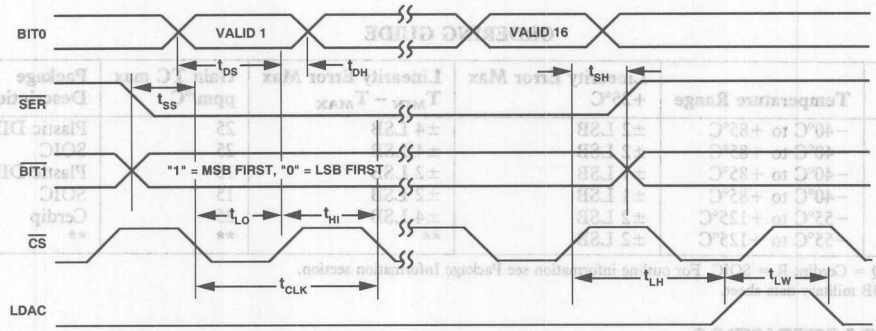


Figure 1b. AD660 Serial Load Timing

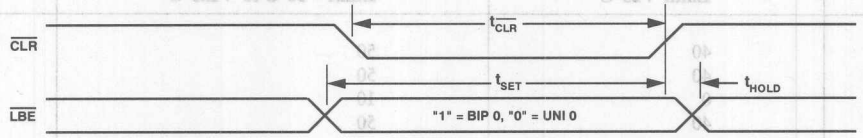


Figure 1c. Asynchronous Clear to Bipolar or Unipolar Zero

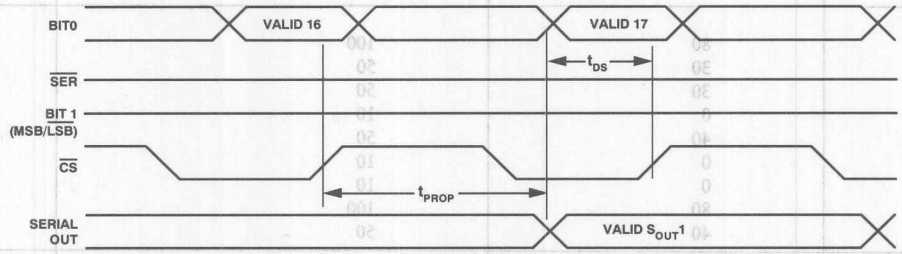


Figure 1d. Serial Out Timing

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY: Analog Devices defines integral nonlinearity as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to FS–1 LSB) for any bit combination. This is also referred to as relative accuracy.

DIFFERENTIAL NONLINEARITY: Differential nonlinearity is the measure of the change in the analog output, normalized to full scale, associated with a 1 LSB change in the digital input code. Monotonic behavior requires that the differential linearity error be greater than or equal to −1 LSB over the temperature range of interest.

MONOTONICITY: A DAC is monotonic if the output either increases or remains constant for increasing digital inputs with the result that the output will always be a single-valued function of the input.

GAIN ERROR: Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out.

OFFSET ERROR: Offset error is a combination of the offset errors of the voltage-mode DAC and the output amplifier and is measured with all 0s loaded in the DAC.

BIPOLAR ZERO ERROR: When the AD660 is connected for bipolar output and 10 . . . 000 is loaded in the DAC, the deviation of the analog output from the ideal midscale value of 0 V is called the bipolar zero error.

DRIFT: Drift is the change in a parameter (such as gain, offset and bipolar zero) over a specified temperature range. The drift temperature coefficient, specified in ppm/°C, is calculated by measuring the parameter at T_{MIN}, 25°C and T_{MAX} and dividing the change in the parameter by the corresponding temperature change.

TOTAL HARMONIC DISTORTION + NOISE: Total harmonic distortion + noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%).

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending upon the amplitude of the output signal. Therefore, to be the most useful, THD+N should be specified for both large and small signal amplitudes.

SIGNAL-TO-NOISE RATIO: The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale signal is present to the output with no signal present. This is measured in dB.

DIGITAL-TO-ANALOG GLITCH IMPULSE: This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is measured at half scale when the DAC switches around the MSB and as many as possible switches change state, i.e., from 011 . . . 111 to 100 . . . 000.

DIGITAL FEEDTHROUGH: When the DAC is not selected (i.e., $\overline{CS}$ is held high), high frequency logic activity on the digital inputs is capacitively coupled through the device to show up as noise on the V_{OUT} pin. This noise is digital feedthrough.

THEORY OF OPERATION

The AD660 uses an array of bipolar current sources with MOS current steering switches to develop a current proportional to the applied digital word, ranging from 0 to 2 mA. A segmented architecture is used, where the most significant four data bits are thermometer decoded to drive 15 equal current sources. The lesser bits are scaled using a R–2R ladder, then applied together with the segmented sources to the summing node of the output amplifier. The internal span/bipolar offset resistor can be connected to the DAC output to provide a 0 V to +10 V span, or it can be connected to the reference input to provide a −10 V to +10 V span.

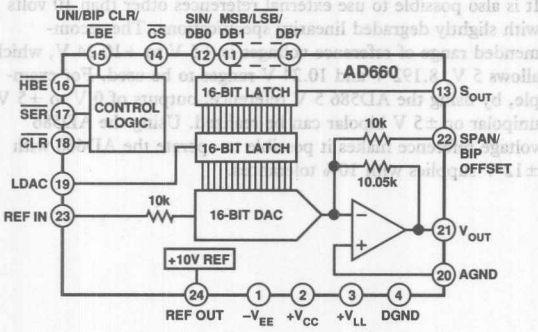


Figure 2. AD660 Functional Block Diagram

ANALOG CIRCUIT CONNECTIONS

Internal scaling resistors provided in the AD660 may be connected to produce a unipolar output range of 0 V to +10 V or a bipolar output range of −10 V to +10 V. Gain and offset drift are minimized in the AD660 because of the thermal tracking of the scaling resistors with other device components.

UNIPOLAR CONFIGURATION

The configuration shown in Figure 3a will provide a unipolar 0 V to +10 V output range. In this mode, 50 Ω resistors are tied between the span/bipolar offset terminal (Pin 22) and V_{OUT} (Pin 21), and between REF OUT (Pin 24) and REF IN (Pin 23). It is possible to use the AD660 without any external components by tying Pin 24 directly to Pin 23 and Pin 22 directly to Pin 21. Eliminating these resistors will increase the gain error by 0.25% of FSR.

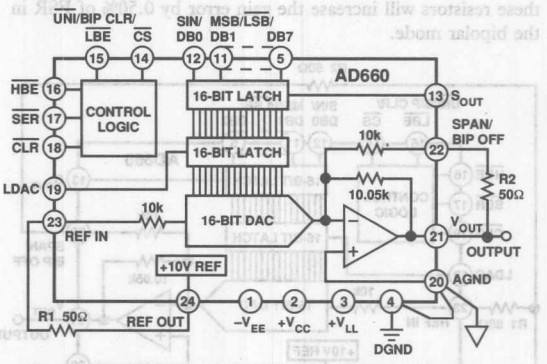


Figure 3a. 0 V to +10 V Unipolar Voltage Output

If it is desired to adjust the gain and offset errors to zero, this can be accomplished using the circuit shown in Figure 3b. The adjustment procedure is as follows:

STEP1 . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R4, until the output reads 0.000000 volts (1 LSB = 153 μV).

STEP 2 . . . GAIN ADJUST

Turn all bits ON and adjust gain trimmer, R1, until the output is 9.999847 volts. (Full scale is adjusted to 1 LSB less than the nominal full scale of 10.000000 volts).

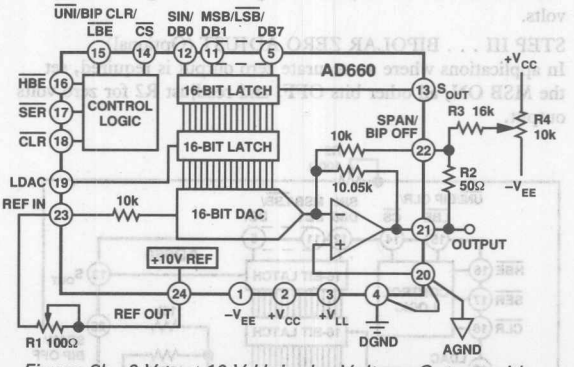


Figure 3b. 0 V to +10 V Unipolar Voltage Output with Gain and Offset Adjustment

BIPOLAR CONFIGURATION

The circuit shown in Figure 4a will provide a bipolar output voltage from −10.000000 V to +9.999694 V with positive full scale occurring with all bits ON. As in the unipolar mode, resistors R1 and R2 may be eliminated altogether to provide AD660 bipolar operation without any external components. Eliminating these resistors will increase the gain error by 0.50% of FSR in the bipolar mode.

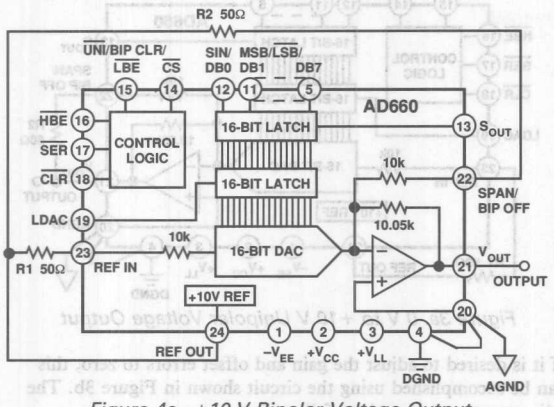


Figure 4a. ±10 V Bipolar Voltage Output

Gain offset and bipolar zero errors can be adjusted to zero using the circuit shown in Figure 4b as follows:

STEP I . . . OFFSET ADJUST
Turn OFF all bits. Adjust trimmer R2 to give −10.000000 volts output.

STEP II . . . GAIN ADJUST
Turn all bits ON and adjust R1 to give a reading of +9.999694 volts.

STEP III . . . BIPOLAR ZERO ADJUST (Optional)
In applications where an accurate zero output is required, set the MSB ON, all other bits OFF, and readjust R2 for zero volts output.

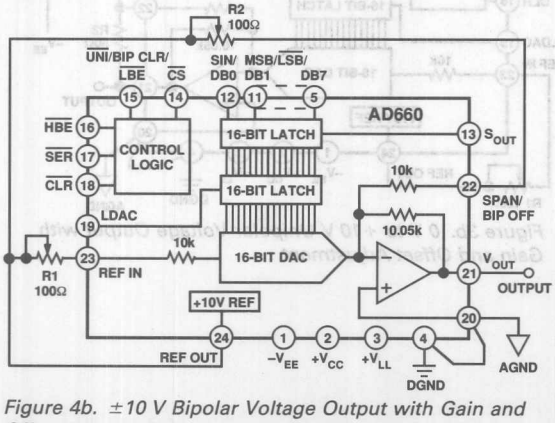


Figure 4b. ±10 V Bipolar Voltage Output with Gain and Offset Adjustment

It should be noted that using external resistors will introduce a small temperature drift component beyond that inherent in the AD660. The internal resistors are trimmed to ratio-match and temperature-track other resistors on chip, even though their absolute tolerances are ±20% and absolute temperature coefficients are approximately −50 ppm/°C. In the case that external resistors are used, the temperature coefficient mismatch between internal and external resistors, multiplied by the sensitivity of the circuit to variations in the external resistor value, will be the resultant additional temperature drift.

INTERNAL/EXTERNAL REFERENCE USE

The AD660 has an internal low noise buried Zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete Zener diode references. The performance of the AD660 is specified with the internal reference driving the DAC and with the DAC alone (for use with a precision external reference).

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 1 mA to REF IN and 1 mA to BIPOLAR OFFSET). A minimum of 2 mA is available for driving external loads. The AD660 reference output should be buffered with an external op amp if it is required to supply more than 4 mA total current. The reference is tested and guaranteed to ±0.2% max error.

It is also possible to use external references other than 10 volts with slightly degraded linearity specifications. The recommended range of reference voltages is +5 V to +10.24 V, which allows 5 V, 8.192 V and 10.24 V ranges to be used. For example, by using the AD586 5 V reference, outputs of 0 V to +5 V unipolar or ±5 V bipolar can be realized. Using the AD586 voltage reference makes it possible to operate the AD660 with ±12 V supplies with 10% tolerances.

Figure 5 shows the AD660 using the AD586 precision 5 V reference in the bipolar configuration. The highest grade AD586MN is specified with a drift of 2 ppm/°C which is a 7.5× improvement over the AD660's internal reference. This circuit includes two optional potentiometers and one optional resistor that can be used to adjust the gain, offset and bipolar zero errors in a manner similar to that described in the BIPOLAR CONFIGURATION section. Use −5.000000 V and +4.999847 as the output values.

The AD660 can also be used with the AD587 10 V reference, using the same configuration shown in Figure 5 to produce a ±10 V output. The highest grade AD587LR, N is specified at 5 ppm/°C, which is a 3× improvement over the AD660's internal reference.

Figure 6 shows the AD660 using the AD680 precision ±10 V reference, in the unipolar configuration. The highest grade AD688BQ is specified with a temperature coefficient of 1.5 ppm/°C. The ±10 V output is also ideal for providing precise biasing for the offset trim resistor R4.

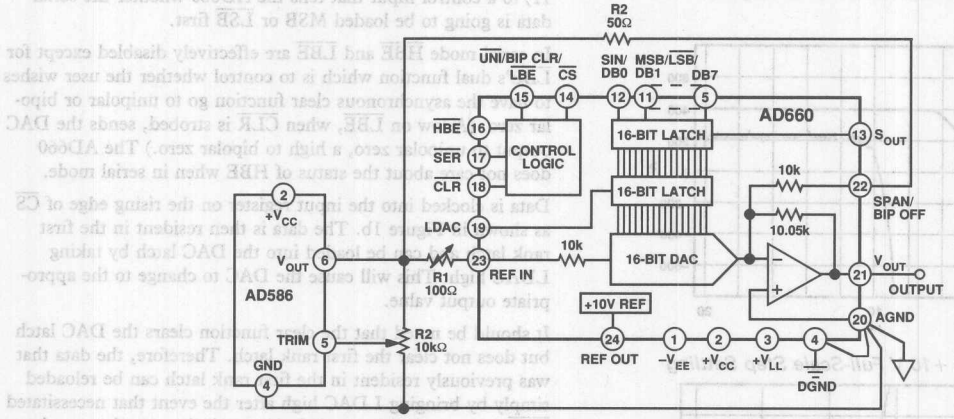


Figure 5. Using the AD660 with the AD586 5 V Reference

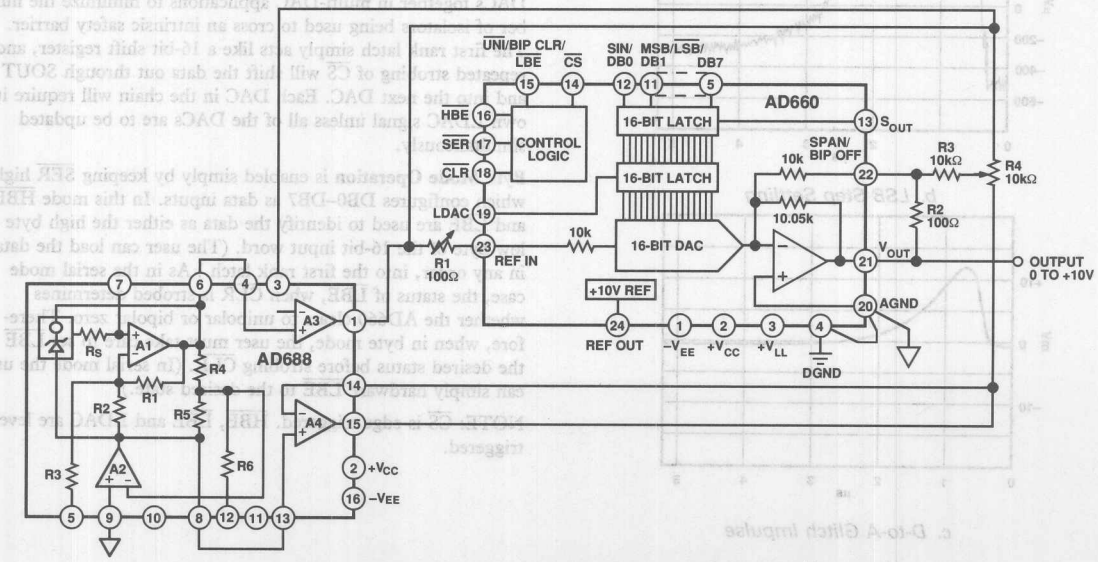
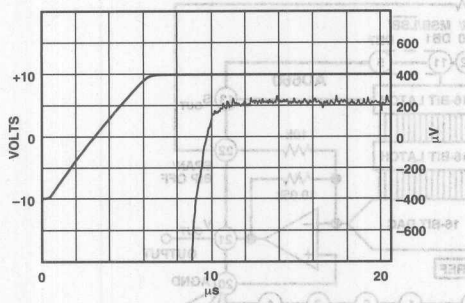


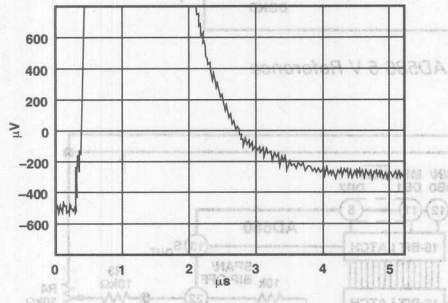
Figure 6. Using the AD660 with the AD688 High Precision ±10 V Reference

step. Figures 7a and 7b show settling for a full-scale and an LSB step, respectively, with a 2 kΩ, 1000 pF load applied. The guaranteed maximum settling time at +25°C for a full-scale step is 13 μs with this load. The typical settling time for a 1 LSB step is 2.5 μs.

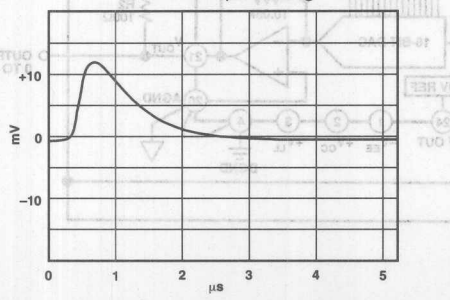
The digital-to-analog glitch impulse is specified as 15 nV-s typical. Figure 7c shows the typical glitch impulse characteristic at the code 011 . . . 111 to 100 . . . 000 transition when loading the second rank register from the first rank register.



a. −10 V to +10 V Full-Scale Step Settling



b. LSB Step Settling



c. D-to-A Glitch Impulse

Figure 7. Output Characteristics

consequently the smallest package size. The user should, therefore, pay careful attention to the following information when applying the AD660.

Data can be loaded into the AD660 in serial or byte mode as described below.

Serial Mode Operation is enabled by bringing $\overline{\text{SER}}$ (Pin 17) low. This changes the function of DB0 (Pin 12) to that of the serial input pin, SIN. It also changes the function of DB1 (Pin 11) to a control input that tells the AD660 whether the serial data is going to be loaded MSB or $\overline{\text{LSB}}$ first.

In serial mode $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ are effectively disabled except for $\overline{\text{LBE}}$'s dual function which is to control whether the user wishes to have the asynchronous clear function go to unipolar or bipolar zero. (A low on $\overline{\text{LBE}}$, when $\overline{\text{CLR}}$ is strobed, sends the DAC output to unipolar zero, a high to bipolar zero.) The AD660 does not care about the status of HBE when in serial mode.

Data is clocked into the input register on the rising edge of $\overline{\text{CS}}$ as shown in Figure 1b. The data is then resident in the first rank latch and can be loaded into the DAC latch by taking LDAC high. This will cause the DAC to change to the appropriate output value.

It should be noted that the clear function clears the DAC latch but does not clear the first rank latch. Therefore, the data that was previously resident in the first rank latch can be reloaded simply by bringing LDAC high after the event that necessitated $\overline{\text{CLR}}$ to be strobed has ended. Alternatively, new data can be loaded into the first rank latch if desired.

The serial out pin (SOUT) can be used to daisy chain several DACs together in multi-DAC applications to minimize the number of isolators being used to cross an intrinsic safety barrier. The first rank latch simply acts like a 16-bit shift register, and repeated strobing of $\overline{\text{CS}}$ will shift the data out through SOUT and into the next DAC. Each DAC in the chain will require its own LDAC signal unless all of the DACs are to be updated simultaneously.

Byte Mode Operation is enabled simply by keeping $\overline{\text{SER}}$ high, which configures DB0–DB7 as data inputs. In this mode $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ are used to identify the data as either the high byte or low byte of the 16-bit input word. (The user can load the data, in any order, into the first rank latch.) As in the serial mode case, the status of $\overline{\text{LBE}}$, when $\overline{\text{CLR}}$ is strobed determines whether the AD660 clears to unipolar or bipolar zero. Therefore, when in byte mode, the user must take care to set $\overline{\text{LBE}}$ to the desired status before strobing $\overline{\text{CLR}}$. (In serial mode the user can simply hardware $\overline{\text{LBE}}$ to the desired state.)

NOTE: $\overline{\text{CS}}$ is edge triggered. $\overline{\text{HBE}}$, $\overline{\text{LBE}}$ and LDAC are level triggered.

AD660 TO MC68HC11 (SPI BUS) INTERFACE

The AD660 interface to the Motorola SPI (serial peripheral interface) is shown in Figure 8. The MOSI, SCK, and $\overline{SS}$ pins of the HC11 are respectively connected to the BIT0, $\overline{CS}$ and LDAC pins of the AD660. The $\overline{SER}$ pin of the AD660 is tied low causing the first rank latch to be transparent. The majority of the interfacing issues are taken care of in the software initialization. A typical routine such as the one shown below begins by initializing the state of the various SPI data and control registers.

The most significant data byte (MSBY) is then retrieved from memory and processed by the SENDAT subroutine. The $\overline{SS}$ pin is driven low by indexing into the PORTD data register and clear Bit 5. This causes the 2nd rank latch of the AD660 to become transparent. The MSBY is then set to the SPI data register where it is automatically transferred to the AD660.

The HC11 generates the requisite 8 clock pulses with data valid on the rising edges. After the most significant byte is transmitted, the least significant byte (LSBY) is loaded from memory and transmitted in a similar fashion. To complete the transfer, the LDAC pin is driven high latching the complete 16-bit word into the AD660.

```
INIT    LDAA #$2F     ;SS = 1; SCK = 0; MOSI = 1
        STAA PORTD    ;SEND TO SPI OUTPUTS
        LDAA #$38     ;SS, SCK,MOSI = OUTPUTS
        STAA DDRD     ;SEND DATA DIRECTION INFO
        LDAA #$50     ;DABL INTRPTS,SPI IS MASTER & ON
        STAA SPCR     ;CPOL=0, CPHA = 0,1MHZ BAUD RATE
NEXTPT  LDAA MSBY     ;LOAD ACCUM W/UPPER 8 BITS
        BSR  SENDAT   ;JUMP TO DAC OUTPUT ROUTINE
        JMP  NEXTPT   ;INFINITE LOOP
SENDAT  LDY  #$1000   ;POINT AT ON-CHIP REGISTERS
        BCLR $08,Y,$20 ;DRIVE SS (LDAC) LOW
        STAA SPDR     ;SEND MS-BYTE TO SPI DATA REG
WAIT1   LDAA SPSR     ;CHECK STATUS OF SPIE
        BPL  WAIT1    ;POLL FOR END OF X-MISSION
        LDAA LSBY     ;GET LOW 8 BITS FROM MEMORY
        STAA SPDR     ;SEND LS-BYTE TO SPI DATA REG
WAIT2   LDAA SPSR     ;CHECK STATUS OF SPIE
        BPL  WAIT2    ;POLL FOR END OF X-MISSION
        BSET $08,Y,$20 ;DRIV SS HIGH TO LATCH DATA
        RTS
```

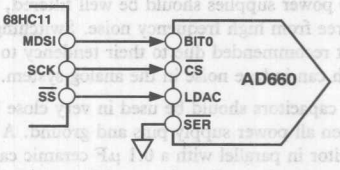


Figure 8. AD660 to 68HC11 (SPI) Interface

AD660 TO MICROWIRE INTERFACE

The flexible serial interface of the AD660 is also compatible with the National Semiconductor MICROWIRE™ interface. The MICROWIRE interface is used on microcontrollers such as the COP400 and COP800 series of processors. A generic interface to the MICROWIRE interface is shown in Figure 9. The G1, SK, And SO pins of the MICROWIRE interface are respectively connected to the LDAC, $\overline{CS}$ and BIT0 pins of the AD660.

MICROWIRE is a registered trademark of National Semiconductor.

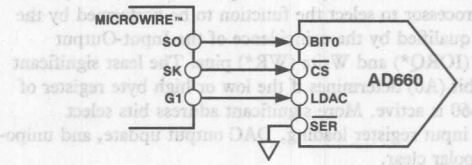


Figure 9. AD660 to MICROWIRE Interface

3

AD660 TO ADSP-210x FAMILY INTERFACE

The serial mode of the AD660 minimizes the number of control and data lines required to interface to digital signal processors (DSPs) such as the ADSP-210x family. The application in Figure 10 shows the interface between an ADSP-2101 and the AD660. Both the TFS pin and the DT pins of the ADSP-2101 should be connected to the $\overline{SER}$ and BIT0 pins of the AD660, respectively. An inverter is required between the SCLK output and the $\overline{CS}$ input of the AD660 in order to assure that data transmitted to the BIT0 pin is valid on the rising edge of $\overline{CS}$.

The serial port (SPORT) of the DSP should be configured for alternate framing mode so that TFS complies with the word-length framing requirement of $\overline{SER}$. Note that the INVTFS bit in the SPORT control register should be set to invert the TFS signal so that $\overline{SER}$ is the correct polarity. The LDAC signal, which must meet the minimum hold specification of t_{IH}, is easily generated by delaying the rising edge of $\overline{SER}$ with a 74HC74 flip-flop. The $\overline{CS}$ signal clocks the flip-flop resulting in a delay of approximately one $\overline{CS}$ clock cycle.

In applications such as waveform generation, accurate timing of the output samples is important to avoid noise that would be induced by jitter on the LDAC signal. In this example, the ADSP-2101 is set up to use the internal timer to interrupt the processor at the precise and desired sample rate. When the timer interrupt occurs, the processors's 16-bit data word is written to the transmit register (TXn). This causes the DSP to automatically generate the TFS signal and begin transmission of the data.

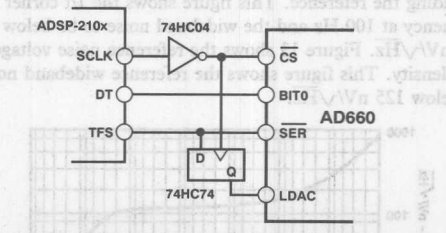


Figure 10. AD660 to ADSP-210x Interface

AD660 TO Z80 INTERFACE

Figure 11 shows a Zilog Z-80 8-bit microprocessor connected to the AD660 using the byte mode interface. The double-buffered capability of the AD660 allows the microprocessor to independently write to the low and high byte registers, and update the DAC output. Processor speeds up to 6 MHz on Z-80B require no extra wait states to interface with the AD660 using a 74ALS138 as the address decoder.

The address decoder analyzes the input-output address produced by the processor to select the function to be performed by the AD660, qualified by the coincidence of the Input-Output Request (IORQ*) and Write (WR*) pins. The least significant address bit (A0) determines if the low or high byte register of the AD660 is active. More significant address bits select between input register loading, DAC output update, and unipolar or bipolar clear.

A typical Z-80 software routine begins by writing the low byte of the desired 16-bit DAC data to address 0, followed by the high byte to address 1. The DAC output is then updated by activating LDAC with a write to address 2 (or 3). A clear to unipolar zero occurs on a write to address 4, and a clear to bipolar zero is performed by a write to address 5. The actual data written to addresses 2 through 5 is irrelevant. The decoder can easily be expanded to control as many AD660s as required.

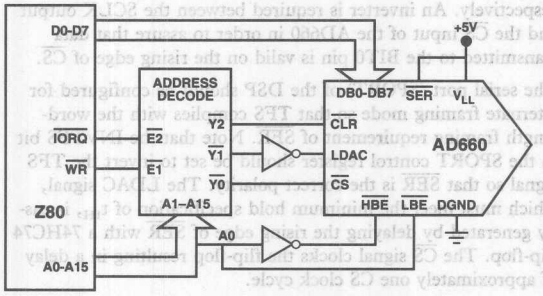


Figure 11. Connections for 8-Bit Bus Interface

NOISE

In high resolution systems, noise is often the limiting factor. A 16-bit DAC with a 10 volt span has an LSB size of 153 μV (−96 dB). Therefore, the noise floor must remain below this level in the frequency range of interest. The AD660's noise spectral density is shown in Figures 12 and 13. Figure 12 shows the DAC output noise voltage spectral density for a 20 V span excluding the reference. This figure shows the 1/f corner frequency at 100 Hz and the wideband noise to be below 120 nV/$\sqrt{\text{Hz}}$. Figure 13 shows the reference noise voltage spectral density. This figure shows the reference wideband noise to be below 125 nV/$\sqrt{\text{Hz}}$.

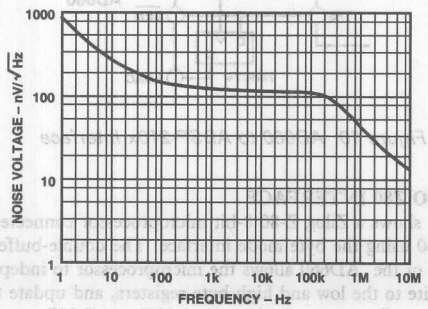


Figure 12. DAC Output Noise Voltage Spectral Density

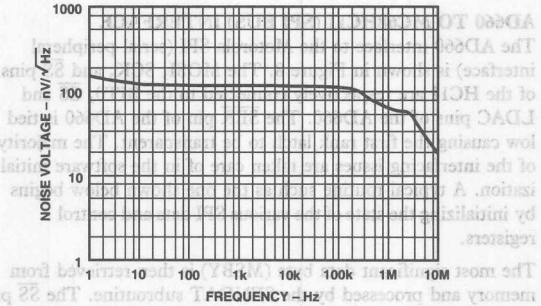


Figure 13. Reference Noise Voltage Spectral Density

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is the first issue. A 306 μA current through a 0.5 Ω trace will develop a voltage drop of 153 μV, which is 1 LSB at the 16-bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes should also be used, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

One feature that the AD660 incorporates to help the user layout is that the analog pins (V_{CC}, V_{EE}, REF OUT, REF IN, SPAN/BIP OFFSET, V_{OUT} and AGND) are adjacent to help isolate analog signals from digital signals.

SUPPLY DECOUPLING

The AD660 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

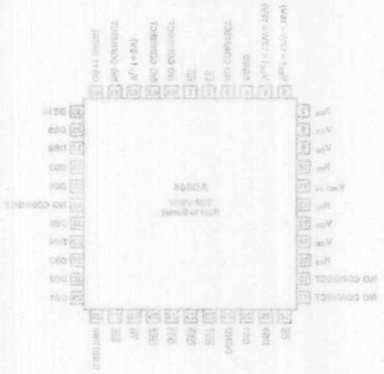
Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor provides adequate decoupling. V_{CC} and V_{EE} should be bypassed to analog ground, while V_{LL} should be decoupled to digital ground.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD660, associated analog circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD660 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

The AD660 has two pins, designated analog ground (AGND) and digital ground (DGND.) The analog ground pin is the "high quality" ground reference point for the device. Any external loads on the output of the AD660 should be returned to analog ground. If an external reference is used, this should also be returned to the analog ground.

If a single AD660 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD660. If multiple AD660s are used or the AD660 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This single interconnection of grounds prevents large ground loops and consequently prevents digital currents from flowing through the analog ground.



FEATURES

Four Complete Voltage Output DACs
Data Register Readback Feature
"Reset to Zero" Override
Multiplying Operation
Double-Buffered Latches
Surface Mount and DIP Packages
MIL-STD-883 Compliant Versions Available

APPLICATIONS

Automatic Test Equipment
Robotics
Process Control
Disk Drives
Instrumentation
Avionics

PRODUCT DESCRIPTION

The AD664 is four complete 12-bit, voltage-output DACs on one monolithic IC chip. Each DAC has a double-buffered input latch structure and a data readback function. All DAC read and write operations occur through a single microprocessor-compatible I/O port.

The I/O port accommodates 4-, 8- or 12-bit parallel words allowing simple interfacing with a wide variety of microprocessors. A reset to zero control pin is provided to allow a user to simultaneously reset all DAC outputs to zero, regardless of the contents of the input latch. Any one or all of the DACs may be placed in a transparent mode allowing immediate response by the outputs to the input data.

The analog portion of the AD664 consists of four DAC cells, four output amplifiers, a control amplifier and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-board application resistors and output amplifier. The output range of each DAC cell is programmed through the digital I/O port and may be set to unipolar or bipolar range, with a gain of one or two times the reference voltage. All DACs are operated from a single external reference.

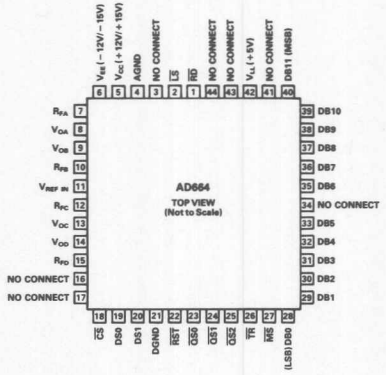
The functional completeness of the AD664 results from the combination of Analog Devices' BiMOS II process, laser-trimmed thin-film resistors and double-level metal interconnects.

PRODUCT HIGHLIGHTS

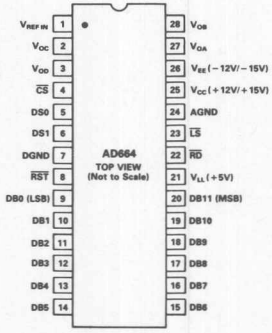
1. The AD664 provides four voltage-output DACs on one chip offering the highest density 12-bit D/A function available.
2. The output range of each DAC is fully and independently programmable.
3. Readback capability allows verification of contents of the internal data registers.

PIN CONFIGURATIONS

44-Pin Package



28-Pin DIP Package



4. The asynchronous RESET control returns all D/A outputs to zero volts.
5. DAC-to-DAC matching performance is specified and tested.
6. Linearity error is specified to be 1/2LSB at room temperature and 3/4LSB maximum for the K, B and T grades.
7. DAC performance is guaranteed to be monotonic over the full operating temperature range.
8. Readback buffers have tristate outputs.
9. Multiplying-mode operation allows use with fixed or variable, positive or negative external references.
10. The AD664 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD664/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (V_{LL} = +5V, V_{CC} = +15V, V_{EE} = −15V, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

Model	JN/JP/AD/AJ/SD			KN/KP/BD/BJ/BE/TD/TE			
	Min	Typ	Max	Min	Typ	Max	Units
RESOLUTION		12	12		*	*	Bits
ANALOG OUTPUT							
Voltage Range[1]							
UNI Versions	0		V_{CC} − 2.0[2]	*		*	Volts
BIP Versions	V_{EE} + 2.0[2]		V_{CC} − 2.0[2]	*		*	Volts
Output Current	5			*			mA
Load Resistance		2			*		kΩ
Load Capacitance			500			*	pF
Short-Circuit Current		25	40		*	*	mA
ACCURACY							
Gain Error	−7	±3	7	−5	±2	5	LSB
Unipolar Offset	−2	±1/2	2	−1	±1/4	1	LSB
Bipolar Zero[3]	−3	±3/4	3	−2	±1/2	2	LSB
Linearity Error[4]	−3/4	±1/2	3/4	−1/2	±1/4	1/2	LSB
Linearity T_{min} to T_{max}	−1	±3/4	1	−3/4	±1/2	3/4	LSB
Differential Linearity	−3/4		3/4	−1/2		1/2	LSB
Differential Linearity T_{min} to T_{max}	Monotonic @ All Temperatures			Monotonic @ All Temperatures			
Gain Error Drift							
Unipolar 0 to +10V Mode	−12	±7	12	−10	±5	10	ppm of FSR[5]/°C
Bipolar −5V to +5V Mode	−12	±7	12	−10	±5	10	ppm of FSR/°C
Bipolar −10V to +10V Mode	−12	±7	12	−10	±5	10	ppm of FSR/°C
Unipolar Offset Drift							
Unipolar 0 to +10V Mode	−3	±1.5	3	−2	±1	2	ppm of FSR/°C
Bipolar Zero Drift							
Bipolar −5V to +5V Mode	−12	±7	12	−10	±5	10	ppm of FSR/°C
Bipolar −10V to +10V Mode	−12	±7	12	−10	±5	10	ppm of FSR/°C
REFERENCE INPUT							
Input Resistance	1.3		2.6	*		*	kΩ
Voltage Range[6]	V_{EE} + 2.0[2]		V_{CC} − 2.0[2]	*		*	Volts
POWER REQUIREMENTS							
V_{LL}	4.5	5.0	5.5	*	*	*	Volts
I_{LL}							
@ V_{IH}, V_{IL} = 5, 0V		0.1	1		*	*	mA
@ V_{IH}, V_{IL} = 2.4, 0.4V		3	6		*	*	mA
V_{CC}/V_{EE}	±11.4		±16.5	*		*	Volts
I_{CC}		12	15		*	*	mA
I_{EE}		15	19		*	*	mA
Total Power		400	525		*	*	mW
ANALOG GROUND CURRENT[7]	−600	±400	+600	*	*	*	µA
MATCHING PERFORMANCE							
Gain[8]	−6	±3	6	−4	±2	4	LSB
Offset[9]	−2	±1/2	2	−1	±1/4	1	LSB
Bipolar Zero[10]	−3	±1	3	−2	±1	2	LSB
Linearity[11]	−1.5	±1/2	1.5	−1	±1/2	1	LSB
CROSSTALK							
Analog			−90			*	dB
Digital			−60			*	dB
DYNAMIC PERFORMANCE (R_L = 2kΩ, C_L = 500pF)							
Settling Time to ±1/2LSB							
Off←Bits→On, GAIN = 1, V_{REF} = 10		8	10		*	*	µs
Settling Time to ±1/2LSB							
−10←V_{REF}→10V, GAIN = 1, Bits On		10			*		µs
Glitch Impulse			500			*	nV-sec
MULTIPLYING MODE PERFORMANCE							
Reference Feedthrough @ 1kHz		−75			*		dB
Reference −3dB Bandwidth		70			*		kHz
POWER SUPPLY GAIN SENSITIVITY							
11.4V←V_{CC}→16.5V		±2	±5		*	*	ppm/%
−16.5V←V_{EE}→−11.4V		±2	±5		*	*	ppm/%
4.5V←V_{LL}→5.5V		±2	±5		*	*	ppm/%

Model	JN/JP/AD/AJ/SD Min	JN/JP/AD/AJ/SD Typ	JN/JP/AD/AJ/SD Max	KN/KP/BD/BJ/BE/TD/TE Min	KN/KP/BD/BJ/BE/TD/TE Typ	KN/KP/BD/BJ/BE/TD/TE Max	Units
DIGITAL INPUTS							
V_{IH}	2.0			*			Volts
V_{IL}	0		0.8	*		*	Volts
Data Inputs							
I_{IH} @ $V_{IN} = V_{LL}$	−10	±1	10	*	*	*	µA
I_{IL} @ V_{IN} = DGND	−10	±1	10	*	*	*	µA
$\overline{CS}$/DS0/DS1/$\overline{RST}$/$\overline{RD}$/$\overline{LS}$							
I_{IH} @ $V_{IN} = V_{LL}$	−10	±1	10	*	*	*	µA
I_{IH} @ $V_{IN} = V_{LL}$	−10	±1	10	*	*	*	µA
$\overline{MS}$/$\overline{TR}$[12]							
I_{IH} @ $V_{IN} = V_{LL}$	−10	5	10	*	*	*	µA
I_{IL} @ V_{IN} = DGND	−10	−5	0	*	*	*	µA
$\overline{QS0}$/$\overline{QS1}$/$\overline{QS2}$[12]							
I_{IH} @ $V_{IN} = V_{LL}$	−10	5	10	*	*	*	µA
I_{IL} @ V_{IN} = DGND	−10	±1	10	*	*	*	µA
DIGITAL OUTPUTS							
V_{OL} @ 1.6mA Sink			0.4			*	Volts
V_{OH} @ 0.5mA Source	2.4			*			Volts
TEMPERATURE RANGE							
JN/JP/KN/KP	0		+70	*		*	°C
AD/AJ/BD/BJ/BE	−40		+85	*		*	°C
SD/TD/TE	−55		+125	*		*	°C

NOTES

[1]A minimum power supply of ±12.0V is required for 0 to +10V and ±10V operation. A minimum power supply of ±11.4V is required for −5V to +5V operation.

[2]For V_{CC}<12V and V_{EE}>−12V. Voltage not to exceed 10V maximum.

[3]Bipolar zero error is the difference from the ideal output (0 volts) and the actual output voltage with code 100 000 000 000 applied to the inputs.

[4]Linearity error is defined as the maximum deviation of the actual DAC output from the ideal output (a straight line drawn from 0 to F.S. −1LSB).

[5]FSR means Full-Scale Range and is 20V for ±10V range and 10V for ±5V range.

[6]A minimum power supply of ±12.0V is required for a 10V reference voltage.

[7]Analog Ground Current is input code dependent.

[8]Gain error matching is the largest difference in gain error between any two DACs in one package.

[9]Offset error matching is the largest difference in offset error between any two DACs in one package.

[10]Bipolar zero error matching is the largest difference in bipolar zero error between any two DACs in one package.

[11]Linearity error matching is the difference in the worst case linearity error between any two DACs in one package.

[12]44-pin versions only.

*Specifications same as JN/JP/AD/AJ/SD.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those test are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

(Specifications apply to all grades except where noted.)

V_{LL} to DGND . . . . . 0 to +7V
V_{CC} to DGND . . . . . 0 to +18V
V_{EE} to DGND . . . . . −18V to 0V
Soldering . . . . . +300°C, 10 sec
Power Dissipation 1000mW
AGND to DGND . . . . . −1V to +1V
Reference Input . . . . . $V_{REF} \leq \pm 10V$ and $V_{REF} \leq (V_{CC} - 2V, V_{EE} + 2V)$
V_{CC} to V_{EE} . . . . . 0 to +36V
Digital Inputs . . . . . −0.3V to +7V
Analog Outputs . . . . . Indefinite Shorts to V_{CC}, V_{LL}, V_{EE} and GND

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

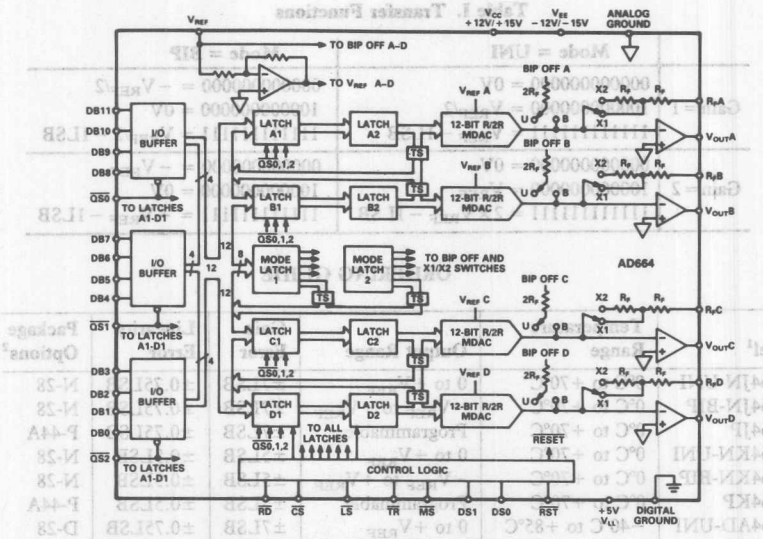


Figure 1a. 44-Pin Block Diagram

FUNCTIONAL DESCRIPTION

The AD664 combines four complete 12-bit voltage output D/A converters with a fast, flexible digital input/output port on one monolithic chip. It is available in two forms, a 44-pin version shown in Figure 1a and a 28-pin version shown in Figure 1b.

44-Pin Versions

Each DAC offers flexibility, accuracy and good dynamic performance. The R-2R structure is fabricated from thin-film resistors which are laser-trimmed to achieve 1/2LSB linearity and guaranteed monotonicity. The output amplifier combines the best features of the bipolar and MOS devices to achieve good dynamic performance and low offset. Settling time is under 10μs and each output can drive a 5mA, 500pF load. Short-circuit protection allows indefinite shorts to V_{LL}, V_{CC}, V_{EE} and GND. The output and span resistor pins are available separately. This feature allows a user to insert current-boosting elements to increase the drive capability of the system, as well as to overcome parasitics.

Digital circuitry is implemented in CMOS logic. The fast, low power, digital interface allows the AD664 to be interfaced with most microprocessors. Through this interface, the wide variety of features on each chip may be accessed. For example, the input data for each DAC is programmed by way of 4-, 8-, 12- or 16-bit words. The double-buffered input structure of this latch allows all four DACs to be updated simultaneously. A readback feature allows the internal registers to be read back through the same digital port, as either 4-, 8- or 12-bit words. When disabled, the readback drivers are placed in a high impedance (tristate) mode. A TRANSPARENT mode allows the input data to pass straight through both ranks of input registers and appear at the DAC with a minimum of delay. One D/A may be placed in the transparent mode at a time, or all four may be made transparent at once. The MODE SELECT feature allows the output range and mode of the DACs to be selected via the data bus inputs. An internal mode select register stores the selections. This register may also be read back to check its contents. A RESET-TO-ZERO feature allows all DACs to be reset to 0 volts out by strobing a single pin.

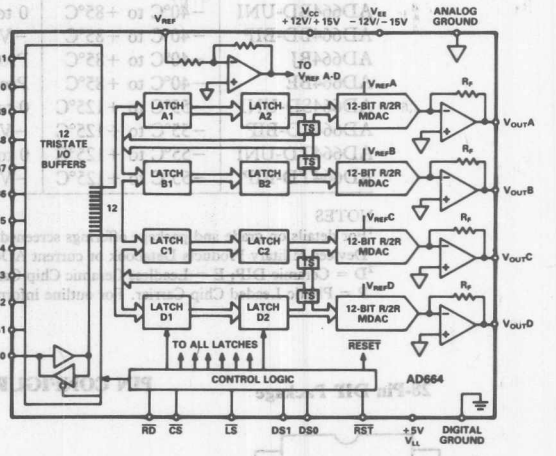


Figure 1b. 28-Pin Block Diagram

28-Pin Versions

The 28-pin versions are dedicated versions of the 44-pin AD664. Each offers a reduced set of features from those offered in the 44-pin version. This accommodates the reduced number of package pins available. Data is written and read with 12-bit words only. Output range and mode select functions are also not available in 28-pin versions. As an alternative, users specify either the UNI (unipolar, 0 to V_{REF}) models or the BIP (bipolar, $-V_{REF}$ to V_{REF}) models depending on the application requirements. Finally, the transparent mode is not available on the 28-pin versions.

Table I. Transfer Functions

	Mode = UNI	Mode = BIP
Gain = 1	000000000000 = 0V 100000000000 = $V_{REF}/2$ 111111111111 = V_{REF} − 1LSB	000000000000 = $-V_{REF}/2$ 100000000000 = 0V 111111111111 = $V_{REF}/2$ − 1LSB
Gain = 2	000000000000 = 0V 100000000000 = V_{REF} 111111111111 = 2 × V_{REF} − 1LSB	000000000000 = $-V_{REF}$ 100000000000 = 0V 111111111111 = $+V_{REF}$ − 1LSB

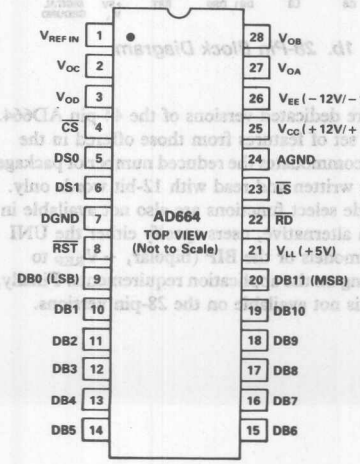
ORDERING GUIDE

Model[1]	Temperature Range	Output Range	Gain Error	Linearity Error	Package Options[2]
AD664JN-UNI	0°C to +70°C	0 to $+V_{REF}$	±7LSB	±0.75LSB	N-28
AD664JN-BIP	0°C to +70°C	$-V_{REF}$ to $+V_{REF}$	±7LSB	±0.75LSB	N-28
AD664JP	0°C to +70°C	Programmable	±7LSB	±0.75LSB	P-44A
AD664KN-UNI	0°C to +70°C	0 to $+V_{REF}$	±5LSB	±0.5LSB	N-28
AD664KN-BIP	0°C to +70°C	$-V_{REF}$ to $+V_{REF}$	±5LSB	±0.5LSB	N-28
AD664KP	0°C to +70°C	Programmable	±5LSB	±0.5LSB	P-44A
AD664AD-UNI	−40°C to +85°C	0 to $+V_{REF}$	±7LSB	±0.75LSB	D-28
AD664AD-BIP	−40°C to +85°C	$-V_{REF}$ to $+V_{REF}$	±7LSB	±0.75LSB	D-28
AD664AJ	−40°C to +85°C	Programmable	±7LSB	±0.75LSB	J-44
AD664BD-UNI	−40°C to +85°C	0 to $+V_{REF}$	±5LSB	±0.5LSB	D-28
AD664BD-BIP	−40°C to +85°C	$-V_{REF}$ to $+V_{REF}$	±5LSB	±0.5LSB	D-28
AD664BJ	−40°C to +85°C	Programmable	±5LSB	±0.5LSB	J-44
AD664BE	−40°C to +85°C	Programmable	±5LSB	±0.5LSB	E-44A
AD664SD-UNI	−55°C to +125°C	0 to $+V_{REF}$	±7LSB	±0.75LSB	D-28
AD664SD-BIP	−55°C to +125°C	$-V_{REF}$ to $+V_{REF}$	±7LSB	±0.75LSB	D-28
AD664TD-UNI	−55°C to +125°C	0 to $+V_{REF}$	±5LSB	±0.5LSB	D-28
AD664TD-BIP	−55°C to +125°C	$-V_{REF}$ to $+V_{REF}$	±5LSB	±0.5LSB	D-28

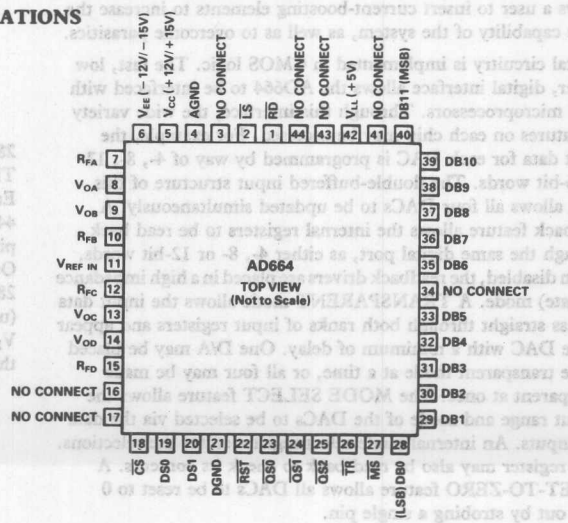
NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD664/883B data sheet.
[2]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; J = Leaded Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN CONFIGURATIONS

28-Pin DIP Package



44-Pin Package



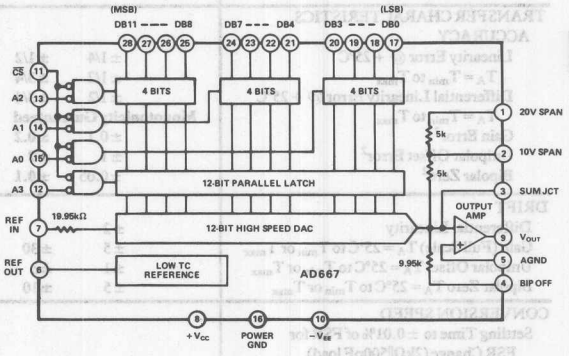
Microprocessor-Compatible 12-Bit D/A Converter

AD667*

FEATURES

- Complete 12-Bit D/A Function
  - Double-Buffered Latch
  - On Chip Output Amplifier
  - High Stability Buried Zener Reference
- Single Chip Construction
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature: 1/2LSB max
- Settling Time: 3μs max to 0.01%
- Guaranteed for Operation with ±12V or ±15V Supplies
- Low Power: 300mW Including Reference
- TTL/5V CMOS Compatible Logic Inputs
- Low Logic Input Currents
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD667 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried Zener voltage reference and double-buffered input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser trimmed thin film resistor network to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latch. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 100ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance in the AD667 results from a combination of advanced switch design, high speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology. The AD667 is trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (K, B grades) at 25°C and ±1/2LSB over the full operating temperature range.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity, is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD667 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 5ppm/°C.

***Protected by Patent Numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and others pending.**

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

The AD667 is available in five performance grades. The AD667J and K are specified for use over the 0 to +70°C temperature range and are available in a 28-pin molded plastic DIP (N) or PLCC (P) package. The AD667S grade is specified for the −55°C to +125°C range and is available in the ceramic DIP (D) or LCC (E) package. The AD667A and B are specified for use over the −25°C to +85°C temperature range and are available in a 28-pin hermetically sealed ceramic DIP (D) package.

PRODUCT HIGHLIGHTS

1. The AD667 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The double-buffered latch structure permits direct interface to 4-, 8-, 12-, or 16-bit data buses. All logic inputs are TTL or 5 volt CMOS compatible.
3. The internal buried Zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The gain setting and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The precision high speed current steering switch and on-board high speed output amplifier settle within 1/2LSB for a 10V full scale transition in 2.0μs when properly compensated.
6. The AD667 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD667/883B data sheet for detailed specifications.

DIGITAL INPUTS							
Resolution			12			12	Bits
Logic Levels (TTL Compatible, T_{min}–T_{max})[1]							
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)		3	10		3	10	µA
I_{IL} (V_{IL} = 0.8V)		1	5		1	5	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error @ +25°C		±1/4	±1/2		±1/8	±1/4	LSB
$T_A = T_{min}$ to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error @ +25°C		±1/2	±3/4		±1/4	±1/2	LSB
$T_A = T_{min}$ to T_{max}		Monotonicity Guaranteed			Monotonicity Guaranteed		LSB
Gain Error[2]		±0.1	±0.2		±0.1	±0.2	%FSR[3]
Unipolar Offset Error[2]		±1	±2		±1	±2	LSB
Bipolar Zero[2]		±0.05	±0.1		±0.05	±0.1	% of FSR
DRIFT							
Differential Linearity		±2			±2		ppm of FSR/°C
Gain (Full Scale) T_A = 25°C to T_{min} or T_{max}		±5	±30		±5	±15	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} or T_{max}		±1	±3			±3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{min} or T_{max}		±5	±10			±10	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR Change (2kΩ‖500pF load)							
with 10kΩ Feedback		3	4		3	4	µs
with 5kΩ Feedback		2	3		2	3	µs
For LSB Change		1			1		µs
Slew Rate	10			10			V/µs
ANALOG OUTPUT							
Ranges[4]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			mA
Output Impedance (dc)		0.05			0.05		Ω
Short Circuit Current			40			40	mA
REFERENCE OUTPUT	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 to +16.5V dc		5	10		5	10	ppm of FS/%
V_{EE} = −11.4 to −16.5V dc		5	10		5	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			±12, ±15		V
Range[4]	±11.4		±16.5	±11.4		±16.5	V
Supply Current							
+11.4 to +16.5V dc		8	12		8	12	mA
−11.4 to −16.5V dc		20	25		20	25	mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Storage	−65		+125	−65		+125	°C

NOTES

[1]The digital input specifications are 100% tested at +25°C, and guaranteed but not tested over the full temperature range.

[2]Adjustable to zero.

[3]FSR means "Full Scale Range" and is 20V for ±10V range and 10V for the ±5V range.

[4]A minimum power supply of ±12.5V is required for a ±10V full scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

TIMING SPECIFICATIONS

(All Models, T_A = 25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V)

Symbol	Parameter	Min	Typ	Max	
t_{DC}	Data Valid to End of $\overline{CS}$	50	–	–	ns
t_{AC}	Address Valid to End of $\overline{CS}$	100	–	–	ns
t_{CP}	$\overline{CS}$ Pulse Width	100	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{SETT}	Output Voltage Settling Time	–	2	4	µs

ABSOLUTE MAXIMUM RATINGS

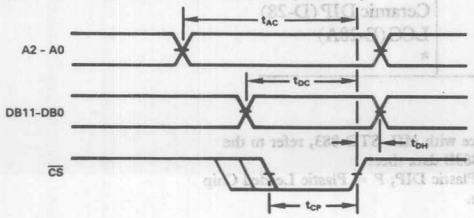
V_{CC} to Power Ground . . . . . 0V to +18V
V_{EE} to Power Ground . . . . . 0V to −18V
Digital Inputs (Pins 11–15, 17–28)
to Power Ground . . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out, V_{OUT} (Pins 6, 9) . . Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

Model	AD667A Min	AD667A Typ	AD667A Max	AD667B Min	AD667B Typ	AD667B Max	AD667S Min	AD667S Typ	AD667S Max	Units
DIGITAL INPUTS										
Resolution			12			12			12	Bits
Logic Levels (TTL Compatible, T_{min}–T_{max})[1]										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.7	V
I_{IH} (V_{IH} = 5.5V)		3	10		3	10		3	10	μA
I_{IL} (V_{IL} = 0.8V)		1	5		1	5		1	5	μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ + 25°C		± 1/4	± 1/2		± 1/8	± 1/4		± 1/8	± 1/2	LSB
$T_A = T_{min}$ to T_{max}		± 1/2	± 3/4		± 1/4	± 1/2		± 1/2	± 3/4	LSB
Differential Linearity Error @ + 25°C		± 1/2	± 3/4		± 1/4	± 1/2		± 1/4	± 3/4	LSB
$T_A = T_{min}$ to T_{max}		Monotonicity Guaranteed			Monotonicity Guaranteed			Monotonicity Guaranteed		LSB
Gain Error[2]		± 0.1	± 0.2		± 0.1	± 0.2		± 0.1	± 0.2	% of FSR[3]
Unipolar Offset Error[2]		± 1	± 2		± 1	± 2		± 1	± 2	LSB
Bipolar Zero[2]		± 0.05	± 0.1		± 0.05	± 0.1		± 0.05	± 0.1	% of FSR
DRIFT										
Differential Linearity		± 2			± 2			± 2		ppm of FSR/°C
Gain (Full Scale) T_A = 25°C to T_{min} or T_{max}		± 5	± 30		± 5	± 15		± 15	± 30	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} or T_{max}		± 1	± 3			± 3			± 3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{min} or T_{max}		± 5	± 10			± 10			± 10	ppm of FSR/°C
CONVERSION SPEED										
Settling Time to ± 0.01% of FSR for										
FSR change (2kΩ‖500pF load)										
with 10kΩ Feedback		3	4		3	4		3	4	μs
with 5kΩ Feedback		2	3		2	3		2	3	μs
For LSB Change		1			1			1		μs
Slew Rate	10			10			10			V/μs
ANALOG OUTPUT										
Ranges[4]		± 2.5, ± 5, ± 10, + 5, + 10			± 2.5, ± 5, ± 10, + 5, + 10			± 2.5, ± 5, ± 10, + 5, + 10		V
Output Current	± 5			± 5			± 5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Current			40			40			40	mA
REFERENCE OUTPUT	9.90	10.00	10.10	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY										
V_{CC} = + 11.4 to + 16.5V dc		5	10		5	10		5	10	ppm of FS/%
V_{EE} = − 11.4 to − 16.5V dc		5	10		5	10		5	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS										
Rated Voltages		± 12, ± 15			± 12, ± 15			± 12, ± 15		V
Range[4]	± 11.4		± 16.5	± 11.4		± 16.5	± 11.4		± 16.5	V
Supply Current										
+ 11.4 to + 16.5V dc		8	12		8	12		8	12	mA
− 11.4 to − 16.5V dc		20	25		20	25		20	25	mA
TEMPERATURE RANGE										
Specification	− 25		+ 85	− 25		+ 85	− 55		+ 125	°C
Storage	− 65		+ 150	− 65		+ 150	− 65		+ 150	°C

TIMING DIAGRAMS

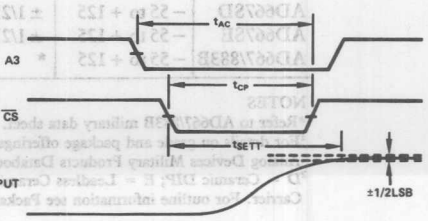
WRITE CYCLE #1

(Load First Rank from Data Bus; A3 = 1)

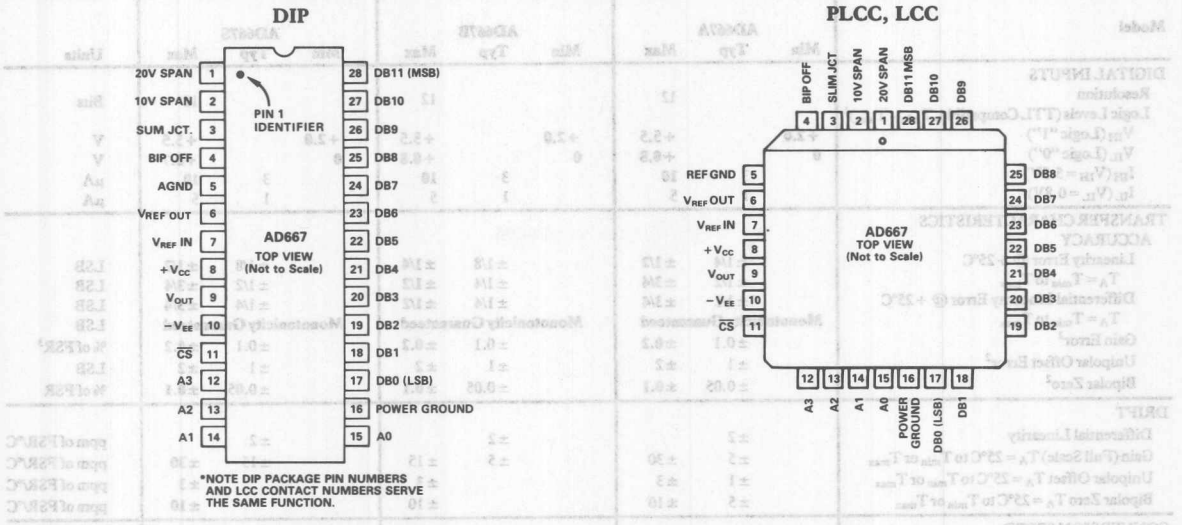


WRITE CYCLE #2

(Load Second Rank from First Rank; A2, A1, A0 = 1)



PIN CONNECTIONS



THE AD667 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

LINEARITY ERROR: Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. The AD667 is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K and B versions and 1/2LSB for the J, A and S versions.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. All versions of the AD667 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V × 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be −1.83mV, or −3/4LSB. The AD667K and B grades have a max differential linearity error of 1/2LSB, which specifies that every step will be at least 1/2LSB and at most 1 1/2 LSB.

ORDERING GUIDE

Model[1]	Temperature Range – °C	Linearity Error Max @ 25°C	Gain T.C. Max ppm/°C	Package Option[2]
AD667JN	0 to +70	±1/2LSB	30	Plastic DIP (N-28)
AD667JP	0 to +70	±1/2LSB	30	PLCC (P-28A)
AD667KN	0 to +70	±1/4LSB	15	Plastic DIP (N-28)
AD667KP	0 to +70	±1/4LSB	15	PLCC (P-28A)
AD667AD	−25 to +85	±1/2LSB	30	Ceramic DIP (D-28)
AD667BD	−25 to +85	±1/4LSB	15	Ceramic DIP (D-28)
AD667SD	−55 to +125	±1/2LSB	30	Ceramic DIP (D-28)
AD667SE	−55 to +125	±1/2LSB	30	LCC (E-28A)
AD667/883B	−55 to +125	*	*	*

NOTES
*Refer to AD667/883B military data sheet.
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD667/883B data sheet.
[2]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

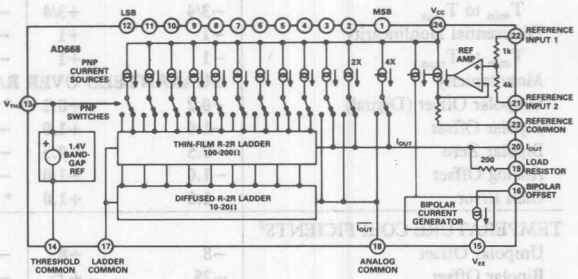
12-Bit Ultrahigh Speed Multiplying D/A Converter

AD668

FEATURES

- **Ultrahigh Speed: Current Settling to 1 LSB in 90 ns for a Full-Scale Change in Digital Input. Voltage Settling to 1 LSB in 120 ns for a Full-Scale Change in Analog Input**
- **15 MHz Reference Bandwidth**
- **Monotonicity Guaranteed over Temperature**
- **10.24 mA Current Output or 1.024 V Voltage Output**
- **Integral and Differential Linearity Guaranteed over Temperature**
- **0.3" "Skinny DIP" Packaging**
- **MIL-STD-883 Compliant Versions Available**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD668 is an ultrahigh speed, 12-bit, multiplying digital-to-analog converter, providing outstanding accuracy and speed performance in responding to both analog and digital inputs. The AD668 provides a level of performance and functionality in a monolithic device that exceeds that of many contemporary hybrid devices. The part is fabricated using Analog Devices' Complementary Bipolar (CB) Process, which features vertical NPN and PNP devices on the same chip without the use of dielectric isolation. The AD668's design capitalizes on this proprietary process in combination with standard low impedance circuit techniques to provide its unique combination of speed and accuracy in a monolithic part.

The wideband reference input is buffered by a high gain, closed loop reference amplifier. The reference input is essentially a 1 V, high impedance input, but trimmed resistive dividers are provided to readily accommodate 5 V and 1.25 V references. The reference amplifier features an effective small signal bandwidth of 15 MHz and an effective slew rate of 3% of full scale/ns.

Multiple matched current sources and thin film ladder techniques are combined to produce bit weighting. The output range can nominally be taken as a 10.24 mA current output or a 1.024 V voltage output. Varying the analog input can provide modulation of the DAC full scale from 10% to 120% of its nominal value. Bipolar outputs can be realized through pin-strapping to provide two-quadrant operation without additional external circuitry.

Laser wafer trimming insures full 12-bit linearity and excellent gain accuracy. All grades of the AD668 are guaranteed monotonic over their full operating temperature range. Furthermore, the output resistance of the DAC is trimmed to 100 Ω ± 1.0%.

The AD668 is available in four performance grades. The AD668JQ and KQ are specified for operation from 0°C to +70°C, the AD668AQ is specified for operation from −40°C to +85°C, and the AD668SQ specified for operation from −55°C to +125°C. All grades are available in a 24-pin cerdip (0.3" package.

PRODUCT HIGHLIGHTS

1. The fast settling time of the AD668 provides suitable performance for waveform generation, graphics display, and high-speed A/D conversion applications.
2. The high bandwidth reference channel allows high frequency modulation between analog and digital inputs.
3. The AD668's design is configured to allow wide variation of the analog input, from 10% to 120% of its nominal value.
4. The AD668's combination of high performance and tremendous flexibility makes it an ideal building block for a variety of high speed, high accuracy instrumentation applications.
5. The digital inputs are readily compatible with both TTL and 5V CMOS logic families.
6. Skinny DIP (0.3") packaging minimizes board space requirements and eases layout considerations.
7. The AD668 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD668/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD668—SPECIFICATIONS (@ T_A = +25°C, V_{CC} = +15 V, V_{EE} = −15 V, unless otherwise noted)

Parameter	AD668J/A Min	AD668J/A Typ	AD668J/A Max	AD668K Min	AD668K Typ	AD668K Max	AD668S Min	AD668S Typ	AD668S Max	Units
RESOLUTION	12			12			12			Bits
LSB WEIGHT (At Nominal FSR)										
Current		2.5			*			*		μA
Voltage (Current into R_L)		250			*			*		μV
ACCURACY[1]										
Linearity	−1/2		+1/2	−1/4		+1/4	*		*	LSB
T_{min} to T_{max}	−3/4		+3/4	−1/2		+1/2	*		*	LSB
Differential Nonlinearity	−1		+1	−1/2		+1/2	*		*	LSB
T_{min} to T_{max}	−1		+1	−1/2		+1/2	*		*	LSB
Monotonicity	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE									
Unipolar Offset (Digital)	−0.2		+0.2	*		*	*		*	% of FSR
Bipolar Offset	−1.0		+1.0	−0.6		+0.6	*		*	% of FSR
Bipolar Zero	−0.5		+0.5	−0.2		+0.2	*		*	% of FSR
Analog Offset	−1.0		+1.0	−0.7		+0.7	*		*	% of V_{NOM}
Gain Error	−1.0		+1.0	*		*	*		*	% of FSR
TEMPERATURE COEFFICIENTS[2]										
Unipolar Offset	−8		+8	−5		+5	*		*	ppm of FSR/°C
Bipolar Offset	−25		+25	−15		+15	*		*	ppm of FSR/°C
Bipolar Zero	−20		+20	−15		+15	*		*	ppm of FSR/°C
Analog Offset	−20		+20	−10		+10	−20		+20	ppm of V_{NOM}/°C
Gain Drift	−30		+30	−15		+15	−40		+40	ppm of FSR/°C
Gain Drift (I_{OUT})		±150			±150			±150		ppm of FSR/°C
REFERENCE INPUT										
Input Resistance										
5.0 V Range		5			*			*		kΩ
1.25 V Range		5			*			*		kΩ
1.0 V Range		1			*			*		MΩ
Reference Range (T_{min} to T_{max})	10	100	120	*	*	*	*	*	*	% of V_{NOM}
DATA INPUTS										
Logic Levels (T_{min} to T_{max})										
V_{IH}	2.0		7.0	*	*	*	*	*	*	V
V_{IL}	0.0		0.8	*	*	*	*	*	*	V
Logic Currents (T_{min} to T_{max})										
I_{IH}	−10		+10	*		*	*		*	μA
I_{IL}	0	60	100	*	*	*	0	100	200	−μA
V_{TH} Pin Voltage		1.4			*			*		V
CODING	BINARY, OFFSET BINARY									
CURRENT OUTPUT RANGES	0 to 10.24, ± 5.12									mA
VOLTAGE OUTPUT RANGES	0 to 1.024, ± 0.512									V
OUTPUT COMPLIANCE	−2		+1.2	*		*	*		*	V
OUTPUT RESISTANCE										
Exclusive of R_L	160	200	240	*	*	*	*	*	*	Ω
Inclusive of R_L	99	100	101	*	*	*	*	*	*	Ω
REFERENCE AMPLIFIER										
Input Bias Current		1.5			*			*		μA
Slew Rate		3			*			*		% of FS/ns
Large Signal Bandwidth		10			*			*		MHz
Small Signal Bandwidth		15			*			*		MHz
Undervoltage Recovery Time										
V_{REF}/V_{NOM} to 0%		35			*			*		ns

Parameter	AD668J/A Min	AD668J/A Typ	AD668J/A Max	AD668K Min	AD668K Typ	AD668K Max	AD668S Min	AD668S Typ	AD668S Max	Units
AC CHARACTERISTICS										
Analog Settling Time										
(10% to 120% Step)										
to ±1%		60			*			*		ns to 1% of FSR
to ±0.1%		90			*			*		ns to 0.1% of FSR
to ±0.025%		120			*			*		ns to 0.025% of FSR
Digital Settling Time										
Current										
to ±1%		30			*			*		ns to 1% of FSR
to ±0.025%		90			*			*		ns to 0.025% of FSR
Voltage (100 Ω, Internal R_L)[3]										
to 1%		50			*			*		ns to 1% of FSR
to 0.1%		75			*			*		ns to 0.1% of FSR
to 0.025%		110			*			*		ns to 0.025% of FSR
Glitch Impulse[4]		350			*			*		pV-sec
Peak Amplitude		20			*			*		% of FSR
Total Harmonic Distortion[5]		−75			*			*		dB
Multiplying Feedthrough Error[6]		−62			*			*		dB
FULL-SCALE TRANSITION[2]										
10% to 90% Rise Time		11			*			*		ns
90% to 10% Fall Time		11			*			*		ns
POWER REQUIREMENTS										
+10.8 V to +16.5 V		27	32		*			*		mA
−10.8 V to −16.5 V		7	9		*			*		−mA
Power Dissipation		510	615		*			*		mW
PSRR[7]			0.05		*			*		% of FSR/V
TEMPERATURE RANGE										
Rated Specification[2] (J, K, S)	0		+70	*		*	−55		+125	°C
Rated Specification (A)	−40		+85							°C
Storage	−65		+150	*		*	*		*	°C

NOTES
*Same as AD668J/A.
[1]Measured in I_{OUT} mode. Specified at nominal 5 V full-scale reference.
[2]Measured in V_{OUT} mode, unless otherwise specified. Specified at nominal 5 V full-scale reference.
[3]Total resistance.
[4]At the major carry, driven by HCMOS logic.
[5]V_{OUT} = 1 V p-p, V_{IN} = 10% to 110%, 100 kHz. Digital Input All 1s.
[6]V_{IN} = 200 mV p-p, 1 MHz Sine Wave. Digital Input all 0s.
[7]Measured at 15 V ± 10% and 12 V ± 10%.

Specifications shown in **boldface** are tested on all production units at final electrical test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to REFCOM . . . . . 0 V to +18 V
V_{EE} to REFCOM . . . . . 0 V to −18 V
REFCOM to LCOM . . . . . +100 mV to −10 V
ACOM to LCOM . . . . . ±100 mV
THCOM to LCOM . . . . . ±500 mV
REFCOM to REFIN (1, 2) . . . . . 18 V
I_{BPO} to LCOM . . . . . ±5 V
I_{OUT} to LCOM . . . . . −5 V to V_{TH}
Digital Inputs to THCOM . . . . . −500 mV to +7.0 V
REFIN1 to REFIN2 . . . . . 36 V
V_{TH} to THCOM . . . . . −0.7 V to +1.4 V
Logic Threshold Control Input Current . . . . . 5 mA
Power Dissipation . . . . . 670 mW
Storage Temperature Range
Q (Cerdip) Package . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Thermal Resistance
θ_{JA} . . . . . +75°C/W
θ_{JC} . . . . . +25°C/W

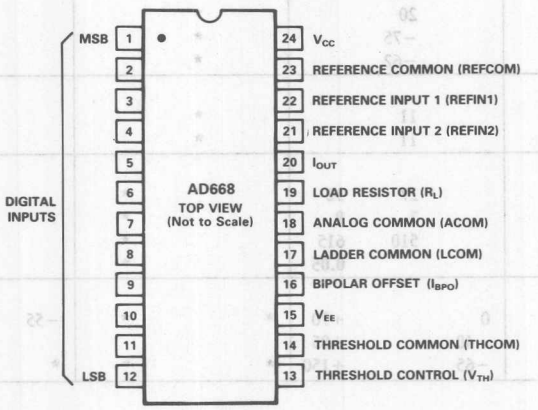
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error Max @ 25°C	Voltage Gain T.C. Max ppm/°C	Package Option[2]
AD668JQ	0°C to +70°C	±1/2	±30	Q-24
AD668KQ	0°C to +70°C	±1/4	±15	Q-24
AD668AQ	−40°C to +85°C	±1/2	±30	Q-24
AD668SQ	−55°C to +125°C	±1/2	±40	Q-24

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD668/883B data sheet.
[2]Q = Cerdip. For outline information see Package Information section.

PIN CONFIGURATION



DEFINITIONS

LINEARITY ERROR (also called INTEGRAL NONLINEARITY OR INL): Analog Devices defines linearity error as the maximum deviation of the actual analog output from the ideal output (a straight line drawn from 0 to FS) for any bit combination expressed in multiples of 1 LSB. The AD668 is laser trimmed to 1/4 LSB (0.006% of FS) maximum linearity error at +25°C for the K version and 1/2 LSB for the J and S versions.

DIFFERENTIAL LINEARITY ERROR (also called DIFFERENTIAL NONLINEARITY or DNL): DNL is the measure of the variation in the analog output, normalized to full scale, associated with a 1 LSB change in digital input code.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases. Monotonic behavior requires that the differential linearity error not exceed 1 LSB in the negative direction.

UNIPOLAR OFFSET ERROR (DAC OFFSET): The DAC offset is the portion of the DAC output that is independent of the digital input. The unipolar DAC offset error is measured as the deviation of the analog output from the ideal (0 V or 0 mA) when the analog input is set to 100% and the digital inputs are set to all 0s.

BIPOLAR OFFSET ERROR: The deviation of the analog output from the ideal (negative half-scale) when the DAC is connected in the bipolar mode (Pin 16 connected to Pin 20), the analog input is set to 100%, and the digital inputs are set to all 0s is called the bipolar offset error.

BIPOLAR ZERO ERROR: The deviation of the analog output from the ideal (0 V or 0 mA) for bipolar mode when only the MSB is on (100 . . . 00) is called bipolar zero error.

COMPLIANCE VOLTAGE: The allowable voltage excursion at the output node of a DAC which will not degrade the accuracy of the DAC output.

SETTLING TIME (DIGITAL CHANNEL): The time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition.

SETTLING TIME (ANALOG CHANNEL): The time required for the output to reach and remain within a specified error band about its final value, measured from the analog input's crossing of it's 50% value.

GAIN ERROR: The difference between the ideal and actual output span of FS−1 LSB, expressed either in % of FS or LSB, when all bits are on is called the gain error.

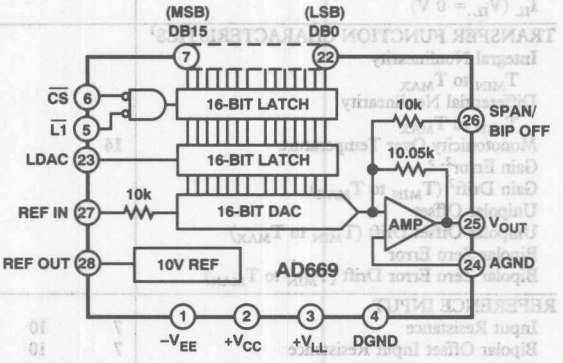
Monolithic 16-Bit DACPORT

AD669

FEATURES

- Complete 16-Bit D/A Function
  - On-Chip Output Amplifier
  - High Stability Buried Zener Reference
- Monolithic BiMOS II Construction
- ±1 LSB Integral Linearity Error
- 15-Bit Monotonic over Temperature
- Microprocessor Compatible
  - 16-Bit Parallel Input
  - Double-Buffered Latches
  - Fast 40 ns Write Pulse
- Unipolar or Bipolar Output
- Low Glitch: 15 nV-s
- Low THD+N: 0.009%
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD669 DACPORT® is a complete 16-bit monolithic D/A converter with an on-board reference and output amplifier. It is manufactured on Analog Devices' BiMOS II process. This process allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry. The AD669 chip includes current switches, decoding logic, an output amplifier, a buried Zener reference and double-buffered latches.

The AD669's architecture insures 15-bit monotonicity over temperature. Integral nonlinearity is maintained at ±0.003%, while differential nonlinearity is ±0.003% max. The on-chip output amplifier provides a voltage output settling time of 10 μs to within 1/2 LSB for a full-scale step.

Data is loaded into the AD669 in a parallel 16-bit format. The double-buffered latch structure eliminates data skew errors and provides for simultaneous updating of DACs in a multi-DAC system. Three TTL/LSTTL/5 V CMOS compatible signals control the latches: $\overline{CS}$, $\overline{LI}$ and LDAC.

The output range of the AD669 is pin programmable and can be set to provide a unipolar output range of 0 V to +10 V or a bipolar output range of −10 V to +10 V.

The AD669 is available in seven grades: AN and BN versions are specified from −40°C to +85°C and are packaged in a 28-pin plastic DIP. The AR and BR versions are specified for −40°C to +85°C operation and are packaged in a 28-pin SOIC. The SQ version is specified from −55°C to +125°C and is packaged in a hermetic 28-pin cerdip package. The AD669 is also available compliant to MIL-STD-883. Refer to the AD669/883B data sheet for specifications and test conditions.

DACPORT is a registered trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. The AD669 is a complete voltage output 16-bit DAC with voltage reference and digital latches on a single IC chip.
2. The internal buried Zener reference is laser trimmed to 10.000 volts with a ±0.2% maximum error. The reference voltage is also available for external applications.
3. The AD669 is both dc and ac specified. DC specs include ±1 LSB INL error and ±1 LSB DNL error. AC specs include 0.009% THD+N and 83 dB SNR. The ac specifications make the AD669 suitable for signal generation applications.
4. The double-buffered latches on the AD669 eliminate data skew errors while allowing simultaneous updating of DACs in multi-DAC systems.
5. The output range is a pin-programmable unipolar 0 V to +10 V or bipolar −10 V to +10 V output. No external components are necessary to set the desired output range.
6. The AD669 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD669/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD669—SPECIFICATIONS (T_A = +25°C, V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V unless otherwise stated)

Model	AD669AN/AR Min	AD669AN/AR Typ	AD669AN/AR Max	AD669AQ/SQ Min	AD669AQ/SQ Typ	AD669AQ/SQ Max	AD669BN/BQ/BR Min	AD669BN/BQ/BR Typ	AD669BN/BQ/BR Max	Units
RESOLUTION	16			16			16			Bits
DIGITAL INPUTS (T_{MIN} to T_{MAX})										
V_{IH} (Logic "1")	2.0		5.5	*		*	*		*	Volts
V_{IL} (Logic "0")	0		0.8	*		*	*		*	Volts
I_{IH} (V_{IH} = 5.5 V)			±10			*			*	μA
I_{IL} (V_{IL} = 0 V)			±10			*			*	μA
TRANSFER FUNCTION CHARACTERISTICS[1]										
Integral Nonlinearity			±2			*			±1	LSB
T_{MIN} to T_{MAX}			±4			*			±2	LSB
Differential Nonlinearity			±2			*			±1	LSB
T_{MIN} to T_{MAX}			±4			*			±2	LSB
Monotonicity Over Temperature	14			14			15			Bits
Gain Error[2, 5]			±0.15			±0.10			±0.10	% of FSR
Gain Drift[2] (T_{MIN} to T_{MAX})			25			15			15	ppm/°C
Unipolar Offset			±5			±5			±2.5	mV
Unipolar Offset Drift (T_{MIN} to T_{MAX})			5			3			3	ppm/°C
Bipolar Zero Error			±15			±15			±10	mV
Bipolar Zero Error Drift (T_{MIN} to T_{MAX})			12			10			5	ppm/°C
REFERENCE INPUT										
Input Resistance	7	10	13	*	*	*	*	*	*	kΩ
Bipolar Offset Input Resistance	7	10	13	*	*	*	*	*	*	kΩ
REFERENCE OUTPUT										
Voltage	9.98	10.00	10.02	*	*	*	*	*	*	Volts
Drift			25			15			15	ppm/°C
External Current[3]	2	4		*	*		*	*		mA
Capacitive Load			1000			*			*	pF
Short Circuit Current		25			*			*		mA
OUTPUT CHARACTERISTICS										
Output Voltage Range										
Unipolar Configuration	0		+10	*		*	*		*	Volts
Bipolar Configuration	−10		+10	*		*	*		*	Volts
Output Current	5			*			*			mA
Capacitive Load			1000			*			*	pF
Short Circuit Current		25			*			*		mA
POWER SUPPLIES										
Voltage										
V_{CC}[4]	+13.5		+16.5	*		*	*		*	Volts
V_{EE}[4]	−13.5		−16.5	*		*	*		*	Volts
V_{LL}	+4.5		+5.5	*		*	*		*	Volts
Current (No Load)										
I_{CC}		+12	+18		*	*		*	*	mA
I_{EE}		−12	−18		*	*		*	*	mA
I_{LL}										
@ V_{IH}, V_{IL} = 5, 0 V		0.3	2		*	*		*	*	mA
@ V_{IH}, V_{IL} = 2.4, 0.4 V		3	7.5		*	*		*	*	mA
Power Supply Sensitivity		1	3		*	*		*	*	ppm/%
Power Dissipation (Static, No Load)		365	625		*			*		mW
TEMPERATURE RANGE										
Specified Performance (A, B)	−40		+85	−40		+85	−40		+85	°C
Specified Performance (S)				−55		+125				°C

NOTES

[1]For 16-bit resolution, 1 LSB = 0.0015% of FSR = 15 ppm of FSR. For 15-bit resolution, 1 LSB = 0.003% of FSR = 30 ppm of FSR. For 14-bit resolution 1 LSB = 0.006% of FSR = 60 ppm of FSR. FSR stands for Full-Scale Range and is 10 V for a 0 to +10 V span and 20 V for a −10 V to +10 V span.

[2]Gain error and gain drift measured using the internal reference. Gain drift is primarily reference related. See the Using the AD669 with the AD688 Reference section for further information.

[3]External current is defined as the current available in addition to that supplied to REF IN and SPAN/BIPOLAR OFFSET on the AD669.

[4]Operation on ±12 V supplies is possible using an external reference like the AD586 and reducing the output range. Refer to the Internal/External Reference Use section.

[5]Measured with fixed 50 Ω resistors. Eliminating these resistors increases the gain error by 0.25% of FSR (Unipolar mode) or 0.50% of FSR (Bipolar mode). Refer to the Analog Circuit Connections section.

*Same as AD669AN/AR specification.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed. Those shown in boldface are tested on all production units.

AC PERFORMANCE CHARACTERISTICS

(With the exception of Total Harmonic Distortion + Noise and Signal-to-Noise Ratio, these characteristics are included for design guidance only and are not subject to test. THD+N and SNR are 100% tested. $T_{MIN} \le T_A \le T_{MAX}$, V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V except where stated.)

Parameter	Limit	Units	Test Conditions/Comments
Output Settling Time	13	µs max	20 V Step, T_A = +25°C
(Time to ±0.0008% FS	8	µs typ	20 V Step, T_A = +25°C
with 2 kΩ, 1000 pF Load)	10	µs typ	20 V Step, $T_{MIN} \le T_A \le T_{MAX}$
	6	µs typ	10 V Step, T_A = +25°C
	8	µs typ	10 V Step $T_{MIN} \le T_A \le T_{MAX}$
	2.5	µs typ	1 LSB Step, $T_{MIN} \le T_A \le T_{MAX}$
Total Harmonic Distortion + Noise			
A, B, S Grade	**0.009**	% max	0 dB, 1001 Hz; Sample Rate = 100 kHz; T_A = +25°C
A, B, S Grade	**0.07**	% max	−20 dB, 1001 Hz; Sample Rate = 100 kHz; T_A = +25°C
A, B, S Grade	**7.0**	% max	−60 dB, 1001 Hz; Sample Rate = 100 kHz; T_A = +25°C
Signal-to-Noise Ratio	**83**	dB min	T_A = +25°C
Digital-to-Analog Glitch Impulse	15	nV-s typ	DAC Alternately Loaded with 8000H and 7FFFH
Digital Feedthrough	2	nV-s typ	DAC Alternately Loaded with 0000H and FFFFH; $\overline{CS}$ High
Output Noise Voltage Density (1 kHz – 1 MHz)	120	nV/$\sqrt{Hz}$ typ	Measured at V_{OUT}, 20 V Span; Excludes Reference
Reference Noise	125	nV/$\sqrt{Hz}$ typ	Measured at REF OUT

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed. Those shown in boldface are tested on all production units.

TIMING CHARACTERISTICS

V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V, V_{HI} = 2.4 V, V_{LO} = 0.4 V

Parameter	Limit +25°C	Limit −40°C to +85°C	Limit −55°C to +125°C	Units
(Figure 1a)				
$t_{\overline{CS}}$	**40**	**50**	**55**	ns min
$t_{\overline{L1}}$	**40**	**50**	**55**	ns min
t_{DS}	**30**	**35**	**40**	ns min
t_{DH}	**10**	**10**	**15**	ns min
t_{LH}	**90**	**110**	**120**	ns min
t_{LW}	**40**	**45**	**45**	ns min
(Figure 1b)				
t_{LOW}	**130**	**150**	**165**	ns min
t_{HIGH}	**40**	**45**	**45**	ns min
t_{DS}	**120**	**140**	**150**	ns min
t_{DH}	**10**	**10**	**15**	ns min

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed. Those shown in boldface are tested on all production units.

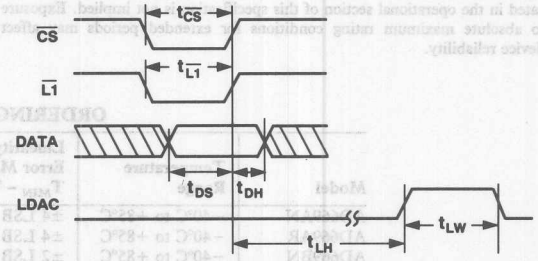
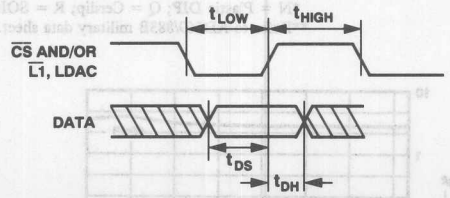


Figure 1a. AD669 Level Triggered Timing Diagram



TIE $\overline{CS}$ AND/OR $\overline{L1}$ TO GROUND OR TOGETHER WITH LDAC

Figure 1b. AD669 Edge Triggered Timing Diagram

ESD SENSITIVITY

The AD669 features input protection circuitry consisting of large transistors and polysilicon series resistors to dissipate both high-energy discharges (Human Body Model) and fast, low-energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD669 has been classified as a Class 2 device.

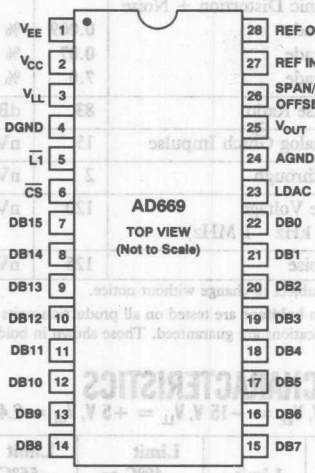
Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to AGND . . . . . −0.3 V to +17.0 V
V_{EE} to AGND . . . . . +0.3 V to −17.0 V
V_{LL} to DGND . . . . . −0.3 V to +7 V
AGND to DGND . . . . . ±1 V
Digital Inputs (Pins 5 through 23) to DGND . . . . . −1.0 V to +7.0 V
REF IN to AGND . . . . . ±10.5 V
Span/Bipolar Offset to AGND . . . . . ±10.5 V
Ref Out, V_{OUT} . . . . . Indefinite Short To AGND, DGND, V_{CC}, V_{EE}, and V_{LL}
Power Dissipation (Any Package)
To +60°C . . . . . 1000 mW
Derates above +60°C . . . . . 8.7 mW/°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

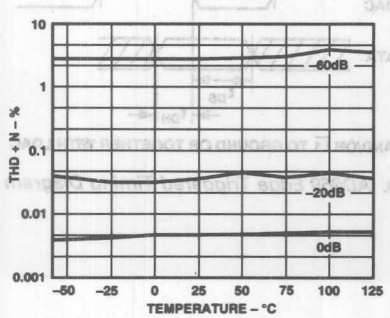
PIN CONFIGURATION



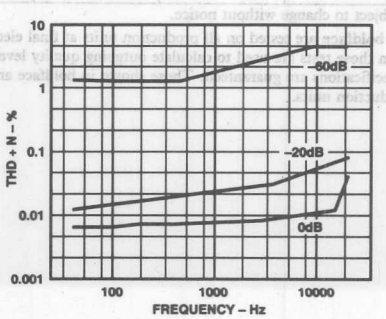
ORDERING GUIDE

Model	Temperature Range	Linearity Error Max T_{MIN} – T_{MAX}	Gain TC max ppm/°C	Package Description	Package Option*
AD669AN	−40°C to +85°C	±4 LSB	25	Plastic DIP	N-28
AD669AR	−40°C to +85°C	±4 LSB	25	SOIC	R-28
AD669BN	−40°C to +85°C	±2 LSB	15	Plastic DIP	N-28
AD669BR	−40°C to +85°C	±2 LSB	15	SOIC	R-28
AD669SQ	−55°C to +125°C	±4 LSB	15	Cerdip	Q-28
AD669/883B**	−55°C to +125°C	**	**	**	**

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.
**Refer to AD669/883B military data sheet.



THD+N vs. Temperature



THD+N vs. Frequency

16-Bit Self-Calibrating Serial/Byte DACPORT

AD760

3

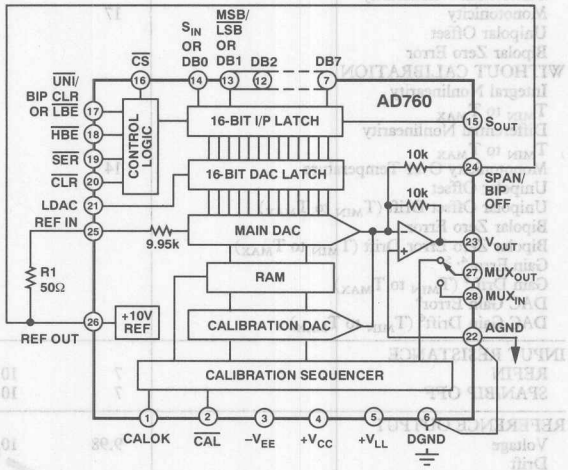
FEATURES

±0.00076% Integral and Differential Linearity
±0.00038% Unipolar Offset, Bipolar Zero
17-Bit Monotonic
Complete 16-Bit D/A Function
- **On-Chip Output Amplifier**
- **On-Chip Buried Zener Voltage Reference**

Microprocessor Compatible
- **Serial or Byte Input**
- **Double Buffered Latches**
- **Fast (40 ns) Write Pulse**
- **Asynchronous Clear (to 0 V) Function**

Serial Output Pin Facilitates Daisy Chaining
Pin Strappable Unipolar or Bipolar Output
Low Glitch: 15 nV-sec
Low THD+N: 0.009%
Output Control on Power-Up & Power-Down

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD760 is a complete 16-bit self-calibrating monolithic DAC (DACPORT®) with onboard voltage reference, double buffered latches and output amplifier. It is manufactured on Analog Devices' BiMOS II process. This process allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry.

Self-calibration is initiated by simply bringing the $\overline{CAL}$ pin low. The CALOK pin indicates when calibration has been successfully completed. The output multiplexer (MUX_{OUT}) can be used to isolate the load from the movement of the DAC output during calibration. The INL and DNL errors are less than ±0.5 LSB or ±0.00076% after calibration. Unipolar offset or bipolar zero is less than ±0.25 LSB or ±0.00038%. This level of performance is unmatched by any other monolithic DAC.

Data can be loaded into the AD760 in serial mode or as two 8-bit bytes. This is made possible by two digital input pins which have dual functions (Pins 13 and 14). The serial mode input format is pin selectable, to be MSB or $\overline{LSB}$ first. In byte mode the user can similarly define whether the high byte or low byte is loaded first. The serial output (S_{OUT}) pin allows the user to daisy chain several AD760s by shifting the data through the input latch into the next DAC thus minimizing the number of control lines required in a multiple DAC application. The double buffered latch structure eliminates data skew errors and provides for simultaneous updating of DACs in a multi-DAC system.

The asynchronous $\overline{CLR}$ function can be configured to clear the output to unipolar or bipolar zero depending on the state of LBE (another dual-use pin) when $\overline{CLR}$ is strobed. The AD760 also powers up or down with the output in a predetermined state by means of a digital and analog power supply detection circuit which is built in to the output multiplexer. This is particularly useful for robotic and industrial control applications.

The AD760 is available in three grades. AN and AP versions are specified from −40°C to +85°C and are packaged in a 28-pin 600 mil plastic DIP and a 28-pin PLCC. The SD version is packaged in a 28-pin 600 mil cerdip package and is also available compliant to MIL-STD-883. Refer to the AD760/883B data sheet for specifications and test conditions.

DACPORT is a registered trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. Complete, true 16-bit, self-calibrating DAC, with a voltage reference, double-buffered latches and output amplifier on a single chip.
2. Pin programmable output can provide a unipolar output range of 0 V to +10 V or a bipolar output range of −10 V to +10 V. No external components required.
3. Asynchronous $\overline{CLR}$ function can send the output to unipolar or bipolar zero.
4. MUX_{OUT} is switched to a user defined input when powering up or down.
5. The AD760 is both dc and ac specified. DC specifications include ±0.5 LSB INL and DNL errors. AC specifications include 0.009% THD+N and 83 dB SNR.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD760 SPECIFICATIONS

TRANSFER FUNCTION CHARACTERISTICS[2]						
WITH CALIBRATION @ T_{CAL} ± 20°C[3]						
Integral Nonlinearity			±0.5		*	LSB
Differential Nonlinearity			±0.5		*	LSB
Monotonicity	17			*		Bits
Unipolar Offset			±0.25		*	LSB
Bipolar Zero Error			±0.25		*	LSB
WITHOUT CALIBRATION						
Integral Nonlinearity			±2		*	LSB
T_{MIN} to T_{MAX}			±4		*	LSB
Differential Nonlinearity			±2		*	LSB
T_{MIN} to T_{MAX}			±4		*	LSB
Monotonicity Over Temperature	14			*		Bits
Unipolar Offset			±5		*	mV
Unipolar Offset Drift (T_{MIN} to T_{MAX})			5		*	ppm/°C
Bipolar Zero Error			±15		*	mV
Bipolar Zero Error Drift (T_{MIN} to T_{MAX})			12		*	ppm/°C
Gain Error[4, 5]			±0.10		±0.15	% of FSR
Gain Drift[5] (T_{MIN} to T_{MAX})			15		25	ppm/°C
DAC Gain Error[6]			TBD		*	% of FSR
DAC Gain Drift[6] (T_{MIN} to T_{MAX})			TBD		*	ppm/°C
INPUT RESISTANCE						
REFIN	7	10	13	*	*	kΩ
SPAN/BIP OFF	7	10	13	*	*	kΩ
REFERENCE OUTPUT						
Voltage	9.98	10.00	10.02	*	*	V
Drift			15		25	ppm/°C
External Current[7]	2	4		*	*	mA
Capacitive Load			1000		*	pF
Short Circuit Current		25		*		mA
Long Term Stability		TBD		*		ppm/1000 Hrs.
OUTPUT CHARACTERISTICS[2]						
Output Voltage Range						
Unipolar Configuration	0		+10	*	*	V
Bipolar Configuration	−10		+10	*	*	V
Output Current	5			*		mA
Capacitive Load			1000		*	pF
Short Circuit Current		25		*		mA
MUX_{OUT} Resistance	TBD		TBD	*	*	kΩ
DIGITAL INPUTS (T_{MIN} to T_{MAX})						
V_{IH} (Logic "1")	2.0		5.5	*	*	V
V_{IL} (Logic "0")	0		0.8	*	*	V
I_{IH} (V_{IH} = 5.5 V)			±10		*	µA
I_{IL} (V_{IL} = 0 V)			±10		*	µA
DIGITAL OUTPUTS (T_{MIN} to T_{MAX})						
V_{OH} (I_{OH} = −0.6 mA)	2.4			*		V
V_{OL} (I_{OL} = 1.6 mA)			0.4		*	V
POWER SUPPLIES						
Voltage						
V_{CC}[8]	+13.5		+16.5	*	*	V
V_{EE}	−16.5		−13.5	*	*	V
V_{LL}	+4.5		+5.5	*	*	V
Current (No Load)						
I_{CC}		+16	+21	*	*	mA
I_{EE}	−21	−16		*	*	mA
I_{LL}						
@ V_{IH}, V_{IL} = 5 V, 0 V		0.3	2	*	*	mA
@ V_{IH}, V_{IL} = 2.4 V, 0.4 V		3	7.5	*	*	mA
Power Supply Sensitivity with V_{OUT} = 10 V		1	3	*	*	ppm/%
Power Dissipation (Static, No Load)		495	725	*	*	mW
TEMPERATURE RANGE						
Specified Performance (A)	−40		+85			°C
Specified Performance (S)				−55	+125	°C

PRELIMINARY TECHNICAL DATA

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NOTES
[1]For 16-bit resolution, 1 LSB = 0.0015% of FSR. For 15-bit resolution, 1 LSB = 0.003% of FSR. For 14-bit resolution, 1 LSB = 0.006% of FSR. FSR stands for full-scale range and is 10 V in unipolar mode and 20 V in bipolar mode.
[2]Characteristics are guaranteed at V_{OUT} Pin (23).
[3]T_{CAL} is the calibration temperature.
[4]Gain Error is measured with a fixed 50 Ω resistor as shown in Figure 4a and Figure 5a.
[5]Gain Error and gain drift are measured with the internal reference. The internal reference is the main contributor to the gain drift. If lower drift is required the AD760 can be used with a precision external reference such as the AD587, AD586 or AD688.
[6]DAC Gain Error is measured without the on-chip voltage reference. It represents the performance that can be obtained with an external precision reference.
[7]External current is defined as the current available in addition to that supplied to REF IN and SPAN/BIPOLAR OFFSET on the AD760.
[8]Operation on ±12 V supplies is possible using an external reference such as the AD586 and reducing the output range. Refer to the Internal/External Reference section.
*Indicates that the specification is the same as the AD760AN.
Specifications subject to change without notice.

3

AC PERFORMANCE CHARACTERISTICS

With the exception of Total Harmonic Distortion + Noise and Signal-to-Noise Ratio, these characteristics are included for design guidance only and are not subject to test. THD+N and SNR are 100% tested. ($T_{MIN} < T_A < T_{MAX}$, $V_{CC} = +15$ V, $V_{EE} = -15$ V, $V_{LL} = +5$ V, tested at V_{OUT} except where stated.)

Parameter	Limit	Units	Test Conditions/Comments
Output Settling Time	13	µs max	20 V Step, $T_A = +25°C$
(Time to +0.0008% FS, with	8	µs typ	20 V Step, $T_A = +25°C$
2 kΩ, 1000 pF Load)	10	µs typ	20 V Step
	6	µs typ	10 V Step, $T_A = +25°C$
	8	µs typ	10 V Step
	2.5	µs typ	1 LSB Step
MUX_{OUT} Settling Time			Settling Time is referenced to the rising edge of CALOK,
(Time to +0.0008% FS, with			when the multiplexer switches from MUX_{IN} to V_{OUT}.
100 pF Load)	TBD	µs max	20 V Step, $T_A = +25°C$
	TBD	µs typ	20 V Step, $T_A = +25°C$
	TBD	µs typ	20 V Step
	TBD	µs typ	10 V Step, $T_A = +25°C$
	TBD	µs typ	10 V Step
Total Harmonic Distortion + Noise			
A, S Grade	0.009	% max	0 dB, 1001 Hz. Sample Rate = 100 kHz. $T_A = +25°C$
A, S Grade	0.07	% max	−20 dB, 1001 Hz. Sample Rate = 100 kHz. $T_A = +25°C$
A, S Grade	7.0	% max	−60 dB, 1001 Hz. Sample Rate = 100 kHz. $T_A = +25°C$
Signal-to-Noise Ratio	83	dB min	$T_A = +25°C$
Digital-to-Analog Glitch Impulse	15	nV sec typ	DAC Alternatively Loaded with 8000_H and $7FFF_H$
MUX_{OUT} Glitch Impulse	TBD	nV sec typ	100 pF Load
Digital Feedthrough	2	nV sec typ	DAC Alternatively Loaded with 0000_H and $FFFF_H$. $\overline{CS}$ High
Output Noise Voltage Density (1 kHz–1 MHz)	60	nV/√Hz typ	Measured at V_{OUT}, 20 V Span, Excludes Reference
Reference Noise (1 kHz–1 MHz)	125	nV/√Hz typ	Measured at REF OUT

Specifications are subject to change without notice.

PRELIMINARY TECHNICAL DATA

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TIMING CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V, V_{HI} = 2.4 V, V_{LO} = 0.4 V)

Parameter	Limit +25°C	Limit −40°C to +85°C	Limit −55°C to +125°C	Units
(Figure 1a)				
t_{CS}	50	50	50	ns min
t_{DS}	50	60	70	ns min
t_{DH}	10	10	10	ns min
t_{BES}	40	50	50	ns min
t_{BEH}	0	10	10	ns min
t_{LH}	140	200	200	ns min
t_{LW}	50	60	60	ns min
(Figure 1b)				
t_{CLK}	80	100	100	ns min
t_{LO}	30	50	50	ns min
t_{HI}	30	50	50	ns min
t_{DS}	50	60	70	ns min
t_{DH}	10	10	10	ns min
t_{LH}	140	200	200	ns min
t_{LW}	40	50	50	ns min
(Figure 1c)				
t_{CLR}	90	100	100	ns min
t_{SET}	80	100	100	ns min
t_{HOLD}	0	0	0	ns min
(Figure 1d)				
t_{PROP}	60	100	100	ns max
(Figure 1e)				
t_{CAL}	30	30	30	ns min
t_{BUSY}	200	200	200	ms max
t_{CD}	150	180	180	ns max
t_{CS}	140	180	180	ns max
t_{CV}	120	150	150	ns max

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

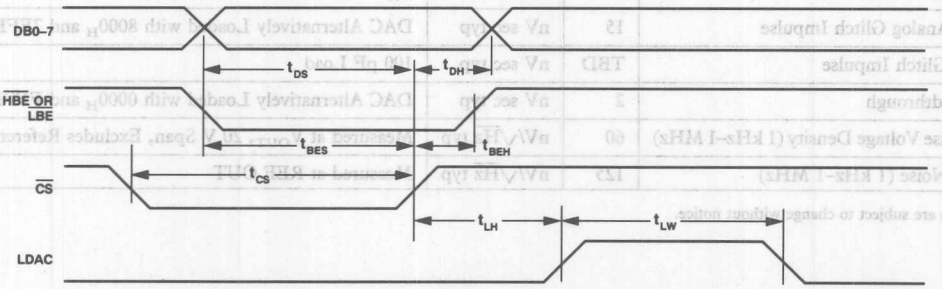

Figure 1a. AD760 Byte Load Timing

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

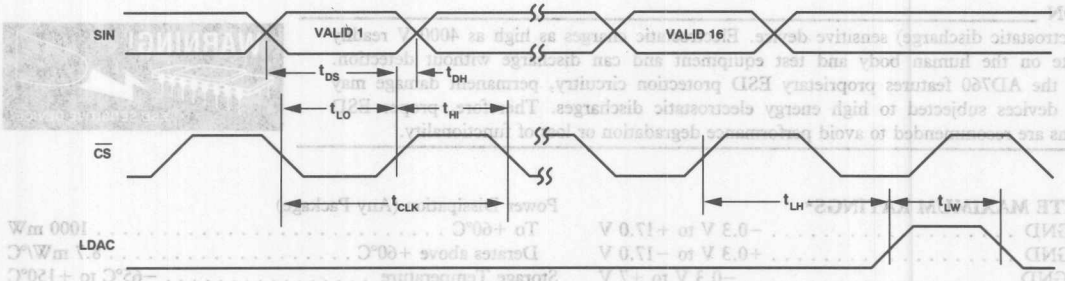

Figure 1b. AD760 Serial Load Timing

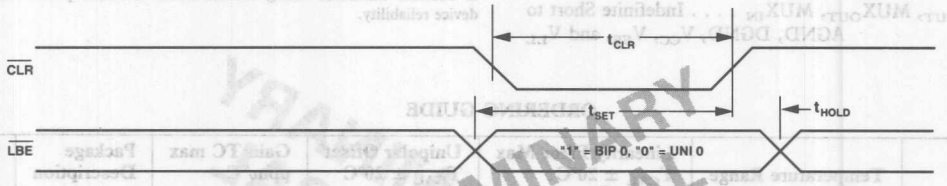

Figure 1c. Asynchronous Clear to Bipolar or Unipolar Zero

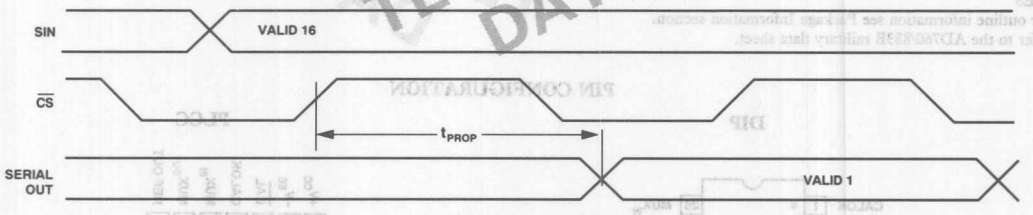

Figure 1d. Serial Out Timing

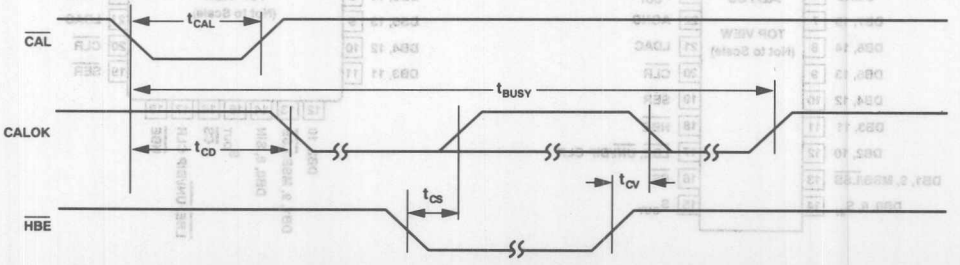

Figure 1e. Calibration Timing

PRELIMINARY TECHNICAL DATA

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accumulate on the human body and test equipment and can discharge without detection. Although the AD760 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to AGND . . . . . −0.3 V to +17.0 V
V_{EE} to AGND . . . . . +0.3 V to −17.0 V
V_{LL} to DGND . . . . . −0.3 V to +7 V
AGND to DGND . . . . . ±1 V
Digital Inputs (Pins 2, 7–14, and 16–21)
to DGND . . . . . −1.0 V to +7.0 V
REF IN to AGND . . . . . ±10.5 V
Span/Bipolar Offset to AGND . . . . . ±10.5 V
REF OUT, V_{OUT}, MUX_{OUT}, MUX_{IN} . . . . Indefinite Short to AGND, DGND, V_{CC}, V_{EE}, and V_{LL}
Power Dissipation (Any Package)
To +60°C . . . . . 1000 mW
Derates above +60°C . . . . . 8.7 mW/°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

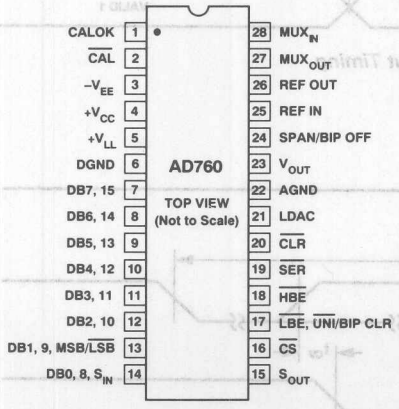
Model	Temperature Range	Linearity Error Max T_{CAL} ± 20°C	Unipolar Offset T_{CAL} ± 20°C	Gain TC max ppm/°C	Package Description	Package Option*
AD760AN	−40°C to +85°C	±0.5 LSB	±0.25 LSB	15	Plastic DIP	N-28
AD760AP	−40°C to +85°C	±0.5 LSB	±0.25 LSB	15	PLCC	P-28A
AD760SQ	−55°C to +125°C	±0.5 LSB	±0.25 LSB	25	Cerdip	Q-28
AD760SQ/883B**	−55°C to +125°C	±0.5 LSB	**	**	**	**

NOTES
*For outline information see Package Information section.
**Refer to the AD760/883B military data sheet.

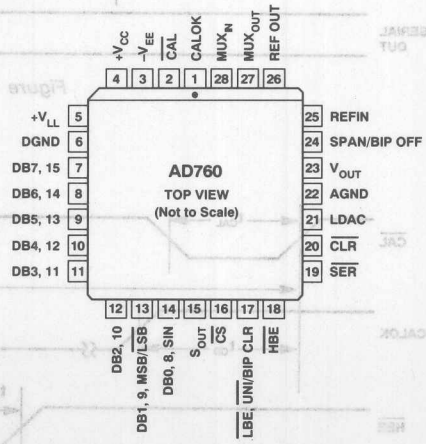
PRELIMINARY TECHNICAL DATA

PIN CONFIGURATION

DIP



PLCC



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DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY: Analog Devices defines integral nonlinearity as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to FS–1 LSB) for any bit combination. This is also referred to as relative accuracy.

DIFFERENTIAL NONLINEARITY: Differential nonlinearity is the measure of the change in the analog output, normalized to full scale, associated with a 1 LSB change in the digital input code. Monotonic behavior requires that the differential linearity error be greater than or equal to −1 LSB over the temperature range of interest.

MONOTONICITY: A DAC is monotonic if the output either increases or remains constant for increasing digital inputs with the result that the output will always be a single-valued function of the input.

GAIN ERROR: Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out.

OFFSET ERROR: Offset error is a combination of the offset errors of the voltage-mode DAC and the output amplifier and is measured with all 0s loaded in the DAC.

BIPOLAR ZERO ERROR: When the AD760 is connected for bipolar output and 10 . . . 000 is loaded in the DAC, the deviation of the analog output from the ideal midscale value of 0 V is called the bipolar zero error.

DRIFT: Drift is the change in a parameter (such as gain, offset and bipolar zero) over a specified temperature range. The drift temperature coefficient, specified in ppm/°C, is calculated by measuring the parameter at T_{MIN}, 25°C and T_{MAX} and dividing the change in the parameter by the corresponding temperature change.

TOTAL HARMONIC DISTORTION + NOISE: Total harmonic distortion + noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%).

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending upon the amplitude of the output signal. Therefore, to be the most useful, THD+N should be specified for both large and small signal amplitudes.

SIGNAL-TO-NOISE RATIO: The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale signal is present to the output with no signal present. This is measured in dB.

DIGITAL-TO-ANALOG GLITCH IMPULSE: This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is measured at half scale when the DAC switches around the MSB and as many as possible switches change state, i.e., from 011 . . . 111 to 100 . . . 000.

DIGITAL FEEDTHROUGH: When the DAC is not selected (i.e., $\overline{CS}$ is held high), high frequency logic activity on the digital inputs is capacitively coupled through the device to show up as noise on the V_{OUT} pin. This noise is digital feedthrough.

THEORY OF OPERATION

The AD760 uses autocalibration circuitry to produce a true 16-bit DAC with less than 0.5 LSB Integral and Differential Linearity Error and 0.25 LSB Offset Error. The block diagram in Figure 2 shows the circuit components needed for calibration.

The MAIN DAC uses an array of bipolar current sources with MOS current steering switches to develop a current proportional to the applied digital word, ranging from 0 to 2 mA. A segmented architecture is used, where the most significant four data bits are thermometer decoded to drive 15 equal current sources. The lesser bits are scaled using a R-2R ladder, then applied together with the segmented sources at the summing node of the output amplifier. An extra LSB is added to the MAIN DAC, for use during calibration.

The self calibration architecture of the AD760 attempts to reduce the linearity errors of its transfer function. The algorithm measures and removes the carry errors (DNL errors) associated with the upper 64 codes, including the zero offset.

In normal operation the top six bits of a code entering the MAIN DAC simultaneously address the RAM, calling up a correction code which is then applied to the CALDAC. The output currents of both the MAIN DAC and CALDAC are combined in the summing amplifier to produce the corrected output voltage.

In the first step of calibration the output of the MAIN DAC is set to the code just below the code to be calibrated. The extra LSB in the MAIN DAC is turned on to find the extrapolated value for the next code. The comparator is then nulled using the TRANSFER STD DAC. The voltage at V_{OUT} has in effect been sampled at the code to be calibrated.

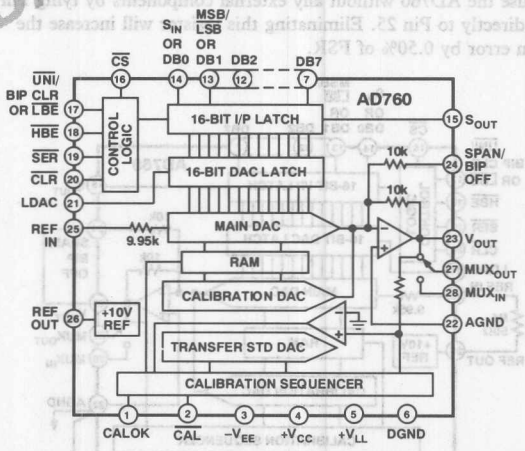

Figure 2. Functional Block Diagram

Next, the extra LSB is turned off and the MAIN DAC code is incremented by one LSB. The comparator is once again nulled, this time with the CALDAC, until the V_{OUT} is adjusted to equal the previously sampled output. The CALDAC code is stored in RAM and the process is repeated for the next code.

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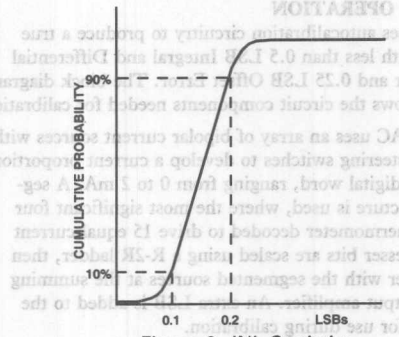

Figure 3. INL Statistics

Calibration repeatability is limited by thermal noise and the finite resolution of the two adjusting DACs. Over many recalibrations the AD760 will produce less than 0.2 LSB of peak INL for 90% of calibrations (0.5 LSB at a 30 ppm reject rate). A cumulative probability plot of the peak INL is shown in Figure 3.

ANALOG CIRCUIT CONNECTIONS

Internal scaling resistors provided in the AD760 may be connected to produce a unipolar output range of 0 V to +10 V or a bipolar output range of −10 V to +10 V. Gain and offset drift are minimized in the AD760 because of the thermal tracking of the scaling resistors with other device components.

UNIPOLAR CONFIGURATION

The configuration shown in Figure 4a will provide a unipolar 0 V to +10 V output range. In this mode a 50 Ω resistor is tied between REF OUT (Pin 26) and REF IN (Pin 25). It is possible to use the AD760 without any external components by tying Pin 26 directly to Pin 25. Eliminating this resistor will increase the gain error by 0.50% of FSR.

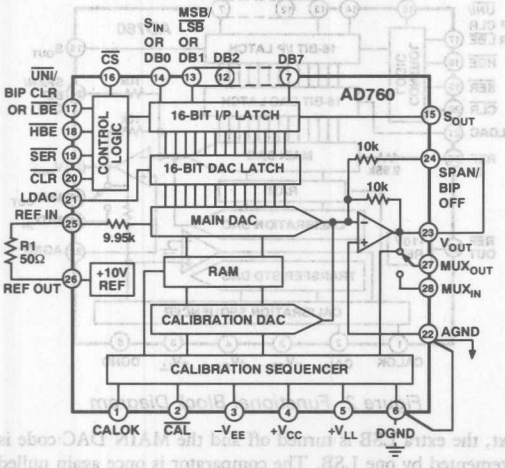

Figure 4a. 0 V to +10 V Unipolar Voltage Output

If it is desired to adjust the gain error to zero, this can be accomplished using the circuit shown in Figure 4b. The adjustment procedure is as follows:

STEP1 . . . ZERO ADJUST

Initiate calibration sequence. CALOK (Pin 1) must remain high throughout Gain Adjust.

STEP 2 . . . GAIN ADJUST

Turn all bits ON and adjust gain trimmer, R1, until the output is 9.999847 volts. (Full scale is adjusted to 1 LSB less than the nominal full scale of 10.000000 volts).

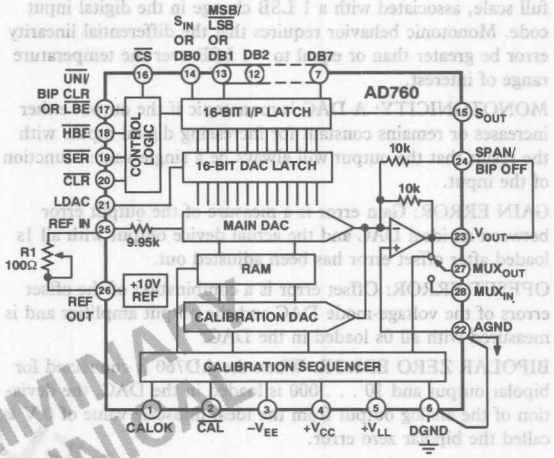

Figure 4b. 0 V to +10 V Unipolar Voltage Output with Gain Adjust

BIPOLAR CONFIGURATION

The circuit shown in Figure 5a will provide a bipolar output voltage from −10.000000 V to +9.999694 V with positive full scale occurring with all bits ON. As in the unipolar mode, resistor R1 may be eliminated altogether to provide AD760 bipolar operation without any external components. Eliminating this resistor will increase the gain error by 0.50% of FSR in the bipolar mode.

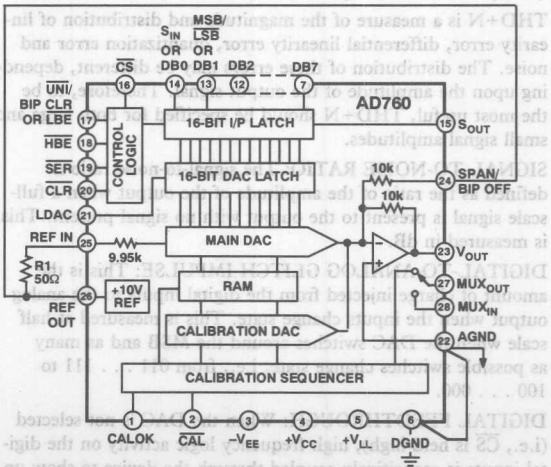

Figure 5a. ±10 V Bipolar Voltage Output

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Gain Error can be adjusted to zero using the circuit shown in Figure 5b.

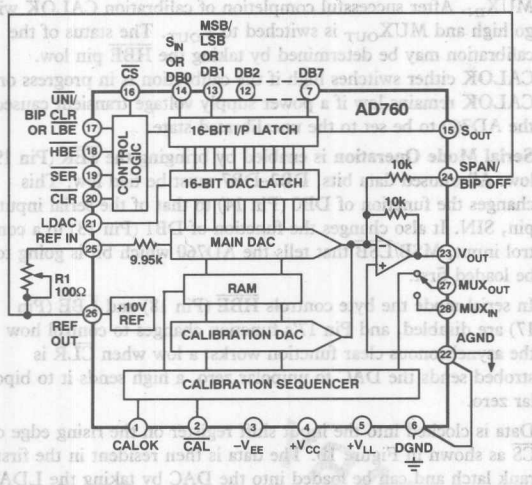

Figure 5b. ±10 V Bipolar Voltage Output Gain Adjustment

It should be noted that using external resistors will introduce a small temperature drift component beyond that inherent in the AD760. The internal resistors are trimmed to ratio-match and temperature-track other resistors on chip, even though their absolute tolerances are ±20% and absolute temperature coefficients are approximately −50 ppm/°C. In the case that external resistors are used, the temperature coefficient mismatch between internal and external resistors, multiplied by the sensitivity of the circuit to variations in the external resistor value, will be the resultant additional temperature drift.

INTERNAL/EXTERNAL REFERENCE USE

The AD760 has an internal low noise buried Zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete Zener diode references. The performance of the AD760 is specified with the internal reference driving the DAC and with the DAC alone (for use with a precision external reference).

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 1 mA to REF IN and 1 mA to BIPOLAR OFFSET). A minimum of 2 mA is available for driving external loads. The AD760 reference output should be buffered with an external op amp if it is required to supply more than 4 mA total current. The reference is tested and guaranteed to ±0.2% max error.

It is also possible to use external references other than 10 volts with slightly degraded linearity specifications. The recommended range of reference voltages is +5 V to +10.24 V, which allows 5 V, 8.192 V and 10.24 V ranges to be used. For example, by using the AD586 5 V reference, outputs of 0 V to +5 V unipolar or ±5 V bipolar can be realized. Using the AD586 voltage reference makes it possible to operate the AD760 with ±12 V supplies with 10% tolerances.

Figure 6 shows the AD760 using the AD586 precision 5 V reference in the bipolar configuration. The highest grade AD586MN is specified with a drift of 2 ppm/°C which is a 7.5× improvement over the AD760's internal reference. This circuit includes an optional potentiometer that can be used to adjust the gain error in a manner similar to that described in the BIPOLAR CONFIGURATION section. Use −5.000000 V and +4.999847 as the output values.

The AD760 can also be used with the AD587 10 V reference, using the same configuration shown in Figure 6 to produce a ±10 V output. The highest grade AD587LR, N is specified at 5 ppm/°C, which is a 3× improvement over the AD760's internal reference.

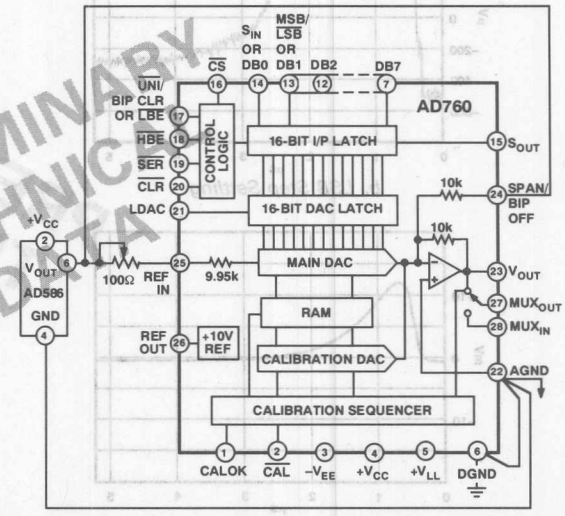

Figure 6. Using the AD760 with the AD586 5 V Reference

OUTPUT SETTLING AND GLITCH

The AD760's output buffer amplifier typically settles to within 0.0008% FS (1/2 LSB) of its final value in 8 μs for a full-scale step. Figures 7a and 7b show settling for a full-scale and an LSB step, respectively, with a 2 kΩ, 1000 pF load applied. The guaranteed maximum settling time at +25°C for a full-scale step is 13 μs with this load. The typical settling time for a 1 LSB step is 2.5 μs.

The digital-to-analog glitch impulse is specified as 15 nV-s typical. Figure 7c shows the typical glitch impulse characteristic at the code 011 . . . 111 to 100 . . . 000 transition when loading the second rank register from the first rank register.

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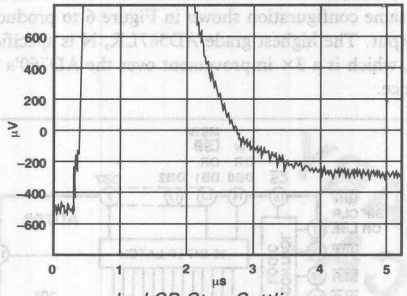
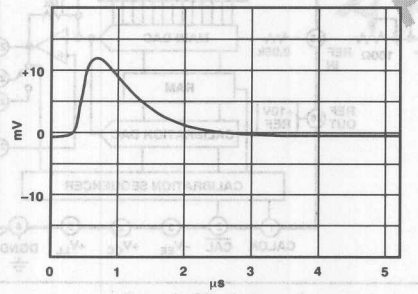
a. −10 V to +10 V Full-Scale Step Settling



b. LSB Step Settling



c. D-to-A Glitch Impulse

Figure 7. Output Characteristics

DIGITAL CIRCUIT DETAILS

The AD760 has several "dual-use" pins which allow flexible operation while maintaining the lowest possible pin count and consequently the smallest package size. The following information is useful when applying the AD760.

The AD760 uses an internal **Output Multiplexer** to disconnect the DAC output from MUX_{OUT} (Pin 27) when the device is uncalibrated or when a calibration sequence is in progress. At those times MUX_{OUT} is switched to MUX_{IN} (Pin 28) so the user can force a predetermined output voltage.

A **Power On-Reset** feature senses whenever any power supply is low enough to jeopardize the integrity of the calibration data in the RAM. At power-up or in the event of a power supply transient, CALOK (Pin 1) is low and the MUX_{OUT} pin is switched to MUX_{IN}. After successful completion of calibration CALOK will go high and MUX_{OUT} is switched to V_{OUT}. The status of the calibration may be determined by taking the $\overline{HBE}$ pin low. CALOK either switches high if the calibration is in progress or CALOK remains low if a power supply voltage transient caused the AD760 to be set to the uncalibrated state.

Serial Mode Operation is enabled by bringing the $\overline{SER}$ (Pin 19) low. All unused data bits, DB2–DB7 must be tied low. This changes the function of DB0 (Pin 14) to that of the serial input pin, SIN. It also changes the function of DB1 (Pin 13) to a control input, MSB/$\overline{LSB}$ that tells the AD760 which bit is going to be loaded first.

In serial mode the byte controls $\overline{HBE}$ (Pin 18) and $\overline{LBE}$ (Pin 17) are disabled, and Pin 17's function changes to control how the asynchronous clear function works: a low when $\overline{CLR}$ is strobed sends the DAC to unipolar zero, a high sends it to bipolar zero.

Data is clocked into the input shift register on the rising edge of $\overline{CS}$ as shown in Figure 1b. The data is then resident in the first rank latch and can be loaded into the DAC by taking the LDAC pin high. This will cause the DAC to change to the appropriate output value. The second rank latch controlled by LDAC is a Transparent latch. Changes in the first rank latch will be reflected in the DAC output immediately, as long as LDAC remains high.

It should be noted that the clear function clears the DAC latch but does not clear the first rank latch. Therefore, the data that was previously resident in the first rank latch can be reloaded by simply bringing LDAC high again. Alternatively, new data can be loaded into the first rank latch if desired.

The serial out pin (S_{OUT}) can be used to daisy chain several DACs together in multi-DAC applications to minimize the number of data lines required. The first rank latch simply acts like a 16-bit shift register, and repeated strobing of $\overline{CS}$ will shift the data out through S_{OUT} and into the next DAC. Each DAC in the chain will require its own LDAC signal unless all of the DACs are to be updated simultaneously.

Byte Mode Operation is enabled by setting $\overline{SER}$ high, which configures DB0–DB7 as data inputs. In this mode $\overline{HBE}$ and $\overline{LBE}$ are used to identify the data as either the high byte or the low byte of the 16-bit word. The user can load the data in either order into the first rank latch using the rising edge of the $\overline{CS}$ signal as shown in Figure 1a. The status of Pin 17, when $\overline{CLR}$ is strobed determines whether the AD760 clears to unipolar or bipolar zero. (But it can not be hardwired to the desired state, as in the serial mode.)

NOTE: $\overline{CS}$ and $\overline{CAL}$ are edge triggered. $\overline{HBE}$, $\overline{LBE}$, $\overline{CLR}$, $\overline{SER}$, and LDAC are level triggered.

AD760 TO MC68HC11 (SPI BUS) INTERFACE

The AD760 interface to the Motorola SPI (serial peripheral interface) is shown in Figure 8. The MOSI, SCK, and $\overline{SS}$ pins of the HC11 are respectively connected to the BIT0, $\overline{CS}$ and LDAC pins of the AD760. The $\overline{SER}$ pin of the AD760 is tied low causing the first rank latch to be transparent. The majority of the interfacing issues are taken care of in the software initialization. A typical routine such as the one shown below begins

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by initializing the state of the various SPI data and control registers.

The most significant data byte (MSBY) is then retrieved from memory and processed by the SENDAT subroutine. The $\overline{SS}$ pin is driven low by indexing into the PORTD data register and clear Bit 5. This causes the 2nd rank latch of the AD760 to become transparent. The MSBY is then set to the SPI data register where it is automatically transferred to the AD760.

The HC11 generates the requisite 8 clock pulses with data valid on the rising edges. After the most significant byte is transmitted, the least significant byte (LSBY) is loaded from memory and transmitted in a similar fashion. To complete the transfer, the LDAC pin is driven high latching the complete 16-bit word into the AD760.

```
INIT    LDAA #$2F     ;SS = 1; SCK = 0; MOSI = 1
        STAA PORTD    ;SEND TO SPI OUTPUTS
        LDAA #$38     ;SS, SCK,MOSI = OUTPUTS
        STAA DDRD     ;SEND DATA DIRECTION INFO
        LDAA #$50     ;DABL INTRPTS,SPI IS MASTER & ON
        STAA SPCR     ;CPOL=0, CPHA = 0,1MHZ BAUD RATE

NEXTPT  LDAA MSBY     ;LOAD ACCUM W/UPPER 8 BITS
        BSR  SENDAT   ;JUMP TO DAC OUTPUT ROUTINE
        JMP  NEXTPT   ;INFINITE LOOP

SENDAT  LDY  #$1000   ;POINT AT ON-CHIP REGISTERS
        BCLR $08,Y,$20 ;DRIVE SS (LDAC) LOW
        STAA SPDR     ;SEND MS-BYTE TO SPI DATA REG
WAIT1   LDAA SPSR     ;CHECK STATUS OF SPIE
        BPL  WAIT1    ;POLL FOR END OF X-MISSION
        LDAA LSBY     ;GET LOW 8 BITS FROM MEMORY
        STAA SPDR     ;SEND LS-BYTE TO SPI DATA REG
WAIT2   LDAA SPSR     ;CHECK STATUS OF SPIE
        BPL  WAIT2    ;POLL FOR END OF X-MISSION
        BSET $08,Y,$20 ;DRIV SS HIGH TO LATCH DATA
        RTS
```

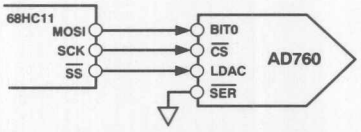

Figure 8. AD760 to 68HC11 (SPI) Interface

AD760 TO MICROWIRE INTERFACE

The flexible serial interface of the AD760 is also compatible with the National Semiconductor MICROWIRE* interface. The MICROWIRE interface is used on microcontrollers such as the COP400 and COP800 series of processors. A generic interface to the MICROWIRE interface is shown in Figure 9. The G1, SK, and SO pins of the MICROWIRE interface are respectively connected to the LDAC, $\overline{CS}$ and BIT0 pins of the AD760.

*MICROWIRE is a registered trademark of National Semiconductor.

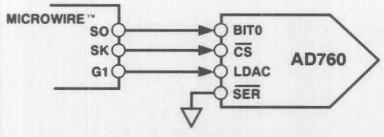

Figure 9. AD760 to MICROWIRE Interface

NOISE

In high resolution systems, noise is often the limiting factor. A 16-bit DAC with a 10 volt span has an LSB size of 153 μV (−96 dB). Therefore, the noise floor must remain below this level in the frequency range of interest. The AD760's noise spectral density is shown in Figures 10 and 11. Figure 12 shows the DAC output noise voltage spectral density for a 20 V span excluding the reference. This figure shows the 1/f corner frequency at 100 Hz and the wideband noise to be below 120 nV/$\sqrt{Hz}$. Figure 13 shows the reference noise voltage spectral density. This figure shows the reference wideband noise to be below 125 nV/$\sqrt{Hz}$.

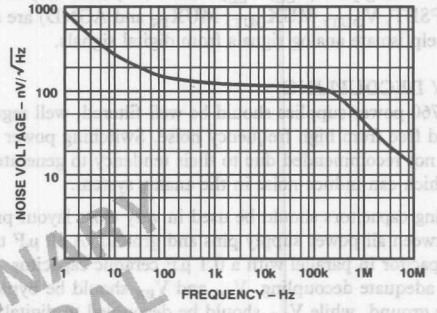

Figure 10. DAC Output Noise Voltage Spectral Density

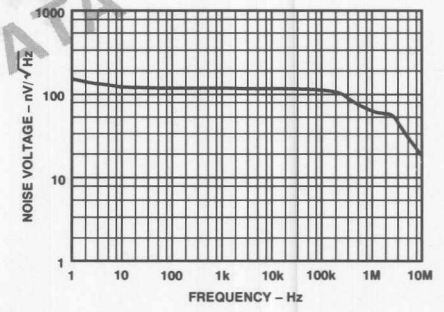

Figure 11. Reference Noise Voltage Spectral Density

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is the first issue. A 306 μA current through a 0.5 Ω trace will develop a voltage drop of 153 μV, which is 1 LSB at the 16-bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

PRELIMINARY TECHNICAL DATA

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Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes should also be used, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

One feature that the AD760 incorporates to help the user layout is that the analog pins (V_{CC}, V_{EE}, REF OUT, REF IN, SPAN/BIP OFFSET, V_{OUT}, MUX_{OUT}, MUX_{IN} and AGND) are adjacent to help isolate analog signals from digital signals.

SUPPLY DECOUPLING

The AD760 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor provides adequate decoupling. V_{CC} and V_{EE} should be bypassed to analog ground, while V_{LL} should be decoupled to digital ground.

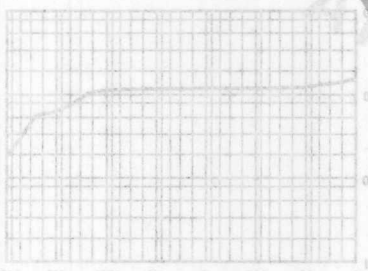
An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD760, associated analog circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD760 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

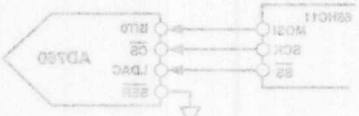
GROUNDING

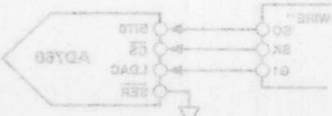
The AD760 has two pins, designated analog ground (AGND) and digital ground (DGND.) The analog ground pin is the "high quality" ground reference point for the device. Any external loads on the output of the AD760 should be returned to analog ground. If an external reference is used, this should also be returned to the analog ground.

If a single AD760 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD760. If multiple AD760s are used or the AD760 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This single interconnection of grounds prevents large ground loops and consequently prevents digital currents from flowing through the analog ground.

PRELIMINARY TECHNICAL DATA







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ANALOG DEVICES

16-Bit DSP DACPORT

AD766

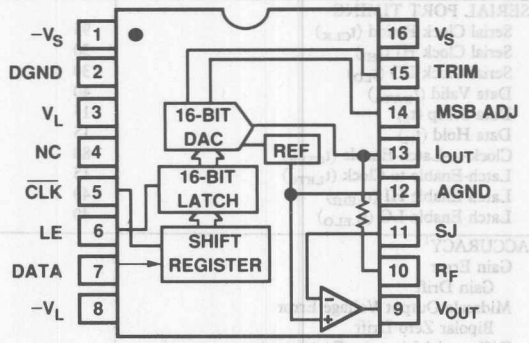
FEATURES

- Zero-Chip Interface to Digital Signal Processors
- Complete DACPORT®
  - On-Chip Voltage Reference
  - Voltage and Current Outputs
- Serial, Twos-Complement Input
- ±3 V Output
- Sample Rates to 390 kSPS
- 94 dB Minimum Signal-to-Noise Ratio
- –81 dB Maximum Total Harmonic Distortion
- 15-Bit Monotonicity
- ±5 V to ±12 V Operation
- 16-Pin Plastic and Ceramic Packages
- Available in Commercial, Industrial, and Military Temperature Ranges

APPLICATIONS

- Digital Signal Processing
- Noise Cancellation
- Radar Jamming
- Automatic Test Equipment
- Precision Industrial Equipment
- Waveform Generation

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD766 16-bit DSP DACPORT provides a direct, three-wire interface to the serial ports of popular DSP processors, including the ADSP-2101, TMS320CXX, and DSP56001. No additional "glue logic" is required. The AD766 is also complete, offering on-chip serial-to-parallel input format conversion, a 16-bit current-steering DAC, voltage reference, and a voltage output op amp. The AD766 is fabricated in Analog Devices' BiMOS II mixed-signal process which provides bipolar transistors, MOS transistors, and thin-film resistors for precision analog circuits in addition to CMOS devices for logic.

The design and layout of the AD766 have been optimized for ac performance and are responsible for its guaranteed and tested 94 dB signal-to-noise ratio to 20 kHz and 79 dB SNR to 250 kHz. Laser-trimming the AD766's silicon chromium thin-film resistors reduces total harmonic distortion below −81 dB (at 1 kHz), a specification also production tested. An optional linearity trim pin allows elimination of midscale differential linearity error for even lower THD with small signals.

The AD766's output amplifier provides a ±3 V signal with a high slew rate, small glitch, and fast settling. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial interface consists of bit clock, data, and latch enable inputs. The twos-complement data word is clocked MSB first on falling clock edges into the serial-to-parallel converter, consistent with the serial protocols of popular DSP processors. The input clock can support data transfers up to 12.5 MHz. The falling edge of latch enable updates the internal DAC input register at the sample rate with the sixteen bits most recently clocked into the serial input register.

The AD766 operates over a ±5 V to ±12 V power supply range. The digital supplies, $+V_L$ and $-V_L$, can be separated from the analog signal supplies, $+V_S$ and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided. An internal bandgap reference provides a precision voltage source to the output amp that is stable over temperature and time.

Power dissipation is typically 120 mW with ±5 V supplies and 300 mW with ±12 V. The AD766 is available in commercial (0°C to 70°C), industrial (−40°C to 85°C), and military (−55°C to 125°C) grades. Commercial and industrial grade parts are available in a 16-pin plastic DIP; military parts processed to MIL-STD-883B are packaged in a 16-pin ceramic DIP. See Analog Devices' *Military Products Databook* or current military data sheet for specifications for the military version.

DACPORT is a registered trademark of Analog Devices, Inc.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD766—SPECIFICATIONS (T_{min} to T_{max}, ±5 V supplies, F_S = 500 kSPS unless otherwise noted. No deglitchers or MSB trimming is used.)

Parameter	AD766J Min	AD766J Typ	AD766J Max	AD766A Min	AD766A Typ	AD766A Max	Units
RESOLUTION			16			16	Bits
DIGITAL INPUTS							
V_{IH}	2.0		$+V_L$	2.0		$+V_L$	V
V_{IL}			0.8			0.8	V
I_{IH}, $V_{IH} = V_L$			1.0			1.0	μA
I_{IL}, $V_{IL} = 0.4$			−10			−10	μA
SERIAL PORT TIMING							
Serial Clock Period (t_{CLK})	95			115			ns
Serial Clock HI (t_{HI})	30			30			ns
Serial Clock LO (t_{LO})	30			70			ns
Data Valid (t_{DATA})	40			40			ns
Data Setup (t_S)	15			20			ns
Data Hold (t_H)	15			20			ns
Clock-to-Latch-Enable (t_{CTLE})	80			100			ns
Latch-Enable-to-Clock (t_{LETC})	15			15			ns
Latch Enable HI (t_{LEHI})	40			40			ns
Latch Enable LO (t_{LELO})	40			80			ns
ACCURACY[1]							
Gain Error		±2.0			±2.0		% of FSR
Gain Drift		±25			±25		ppm of FSR/°C
Midscale Output Voltage Error		±30			±30		mV
Bipolar Zero Drift		±4			±4		ppm of FSR/°C
Differential Linearity Error		±0.001			±0.001		% of FSR
Monotonicity		15			15		Bits
TOTAL HARMONIC DISTORTION							
F_{OUT} = 1037 Hz[1]							
0 dB		−88	−81		−88	−81	dB
−20 dB		−75	−65		−75	−65	dB
−60 dB		−37	−27		−37	−27	dB
F_{OUT} = 49.07 kHz[2]							
0 dB		−77	−72		−77	−72	dB
−20 dB		−69	−66		−69	−66	dB
−60 dB		−25	−21		−25	−21	dB
SIGNAL-TO-NOISE RATIO[3]							
20 Hz to 20 kHz (F_{OUT} = 1037 Hz)[1]	94	102		94	102		dB
20 kHz to 250 kHz (F_{OUT} = 49.07 kHz)[2]	79	83		79	83		dB
SETTLING TIME (to ±0.0015% of FSR)							
Voltage Output[1]							
6 V Step		1.5			1.5		μs
1 LSB Step		1.0			1.0		μs
Slew Rate		9			9		V/μs
Current Output							
1 mA Step 10 Ω to 100 Ω Load		350			350		ns
1 kΩ Load		350			350		ns
OUTPUT							
Voltage Output Configuration[1]							
Bipolar Range	±2.88	±3.0	±3.12	±2.88	±3.0	±3.12	V
Output Current		±8.0			±8.0		mA
Output Impedance		0.1			0.1		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
Current Output Configuration							
Bipolar Range	±0.7	±1.0	±1.3	±0.7	±1.0	±1.3	mA
Output Impedance (±30%)		1.7			1.7		kΩ
POWER SUPPLY							
Voltage: $+V_L$ and $+V_S$	4.75		13.2	4.75		13.2	V
$-V_L$ and $-V_S$	−13.2		−4.75	−13.2		−4.75	V
Current Case 1[1]: V_S and V_L = +5 V +I		12.0	15.0		12.0	15.0	mA
$-V_S$ and $-V_L$ = −5 V −I		−12.0	−15.0		−12.0	−15.0	mA
Case 2: V_S and V_L = +12 V +I		10.5			10.5		mA
$-V_S$ and $-V_L$ = −12 V −I		−14			−14		mA
Case 3[4]: V_S and V_L = +5 V +I		12			12		mA
$-V_S$ and $-V_L$ = −12 V −I		−14			−14		mA
Power Dissipation: V_S and V_L = ±5 V[1]		120	150		120	150	mW
V_S and V_L = ±12 V		300			300		mW
V_S and V_L = +5 V, $-V_S$ and $-V_L$ = −12 V[4]		225			225		mW

Parameter	AD766J Min	AD766J Typ	AD766J Max	AD766A Min	AD766A Typ	AD766A Max	Units
TEMPERATURE RANGE							
Specified	0		+70	−40		+85	°C
Storage	−60		+100	−60		+100	°C

NOTES
[1]For A grade only, voltage outputs are guaranteed only if $+V_S \geq 7$ V and $-V_S \leq -7$ V.
[2]Specified using external op amp, see Figure 3 for more details.
[3]Tested at full-scale input.
[4]For A grade only, power supplies must be symmetric, i.e., $V_S = |-V_S|$ and $+V_L = |-V_L|$. Each supply must independently meet this equality within ±5%.
All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 13.2 V
V_S to AGND . . . . . 0 to 13.2 V
$-V_L$ to DGND . . . . . −13.2 V to 0 V
$-V_S$ to AGND . . . . . −13.2 V to 0 V
Digital Inputs to DGND . . . . . −0.3 V to V_L
AGND to DGND . . . . . ±0.3 V
Short Circuit Protection . . . . . Indefinite Short to Ground
Soldering . . . . . +300°C, 10 sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

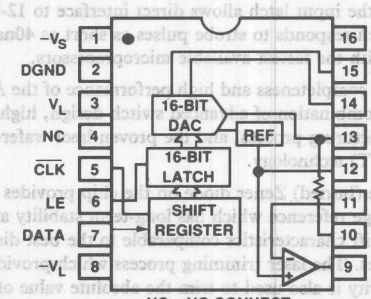
Model	Temperature Range	Package Option*
AD766JN	0°C to +70°C	N-16
AD766AN	−40°C to +85°C	N-16
AD766SD/883B	−55°C to +125°C	D-16

*N = Plastic DIP; D = Ceramic DIP. For outline information see Package Information section.

PIN DESIGNATIONS

Pin	Function	Description
1	$-V_S$	Analog Negative Power Supply
2	DGND	Digital Ground
3	V_L	Logic Positive Power Supply
4	NC	No Connection
5	$\overline{CLK}$	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Power Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	AGND	Analog Ground
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trimming Potentiometer Terminal
16	V_S	Analog Positive Power Supply

CONNECTION DIAGRAM



NC = NO CONNECT

ESD SENSITIVITY

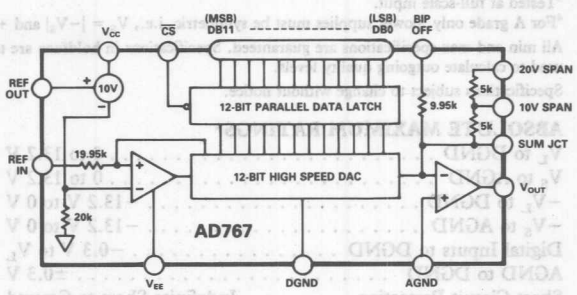
The AD766 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD766 has been classified as a Category 1 Device.
Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment, and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam discharged to the destination socket before devices are removed. For further information on ESD precaution, refer to Analog Devices' *ESD Prevention Manual*.

AD767*

FEATURES

- Complete 12-Bit D/A Function
  - On-Chip Output Amplifier
  - High Stability Buried Zener Reference
- Fast 40ns Write Pulse
- 0.3" Skinny DIP and PLCC Packages
- Single Chip Construction
- Monotonicity Guaranteed Over Temperature
- Settling Time: 3μs max to 1/2LSB
- Guaranteed for Operation with ±12V or ±15V Supplies
- TTL/5V CMOS Compatible Logic Inputs
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD767 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried Zener reference and input latch on a single chip. The converter uses 12 precision high-speed bipolar current steering switches and a laser-trimmed thin-film resistor network to provide high accuracy.

Microprocessor compatibility is achieved by the on-chip latch. The design of the input latch allows direct interface to 12-bit buses. The latch responds to strobe pulses as short as 40ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance of the AD767 result from a combination of advanced switch design, high-speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD767 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full-scale gain T.C. is 5ppm/°C.

***Protected by Patent Numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and others pending.**

PRODUCT HIGHLIGHTS

1. The AD767 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The input latch responds to write pulse widths as short as 40ns assuring direct interface with the industry's fastest microprocessors.
3. The internal buried Zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The gain setting and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser trimmed for minimum full-scale and bipolar offset errors.
5. The precision high-speed current steering switches and on-board high-speed output amplifier settle within 1/2LSB for a 10V full-scale transition in 3.0μs when properly compensated.
6. The AD767 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD767/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (T_A = +25°C, ±15 volt power supplies, Unipolar Mode, unless otherwise noted.)

Model	AD767J/A/S[1]			AD767K/B			AD767A[2] Chips			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DIGITAL INPUTS										
Resolution			12			12			12	Bits
Logic Levels (TTL Compatible, T_{min}–T_{max})[3]										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0") J, K, A, B	0		+0.8	0		+0.8	0		+0.8	V
V_{IL} (Logic "0") S	0		+0.7							V
I_{IH} (V_{IH} = 5.5V)		3	10		3	10		3	10	μA
I_{IL} (V_{IL} = 0.8V)		1	5		1	5		1	5	μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ + 25°C		±1/2	±1		±1/8	±1/2		±1/2	±1	LSB
$T_A = T_{min}$ to T_{max}		±1/2	±1		±1/4	±1/2		±1/2	±1	LSB
Differential Linearity Error @ + 25°C		±1/2	±1		±1/4	±1		±1/2	±1	LSB
$T_A = T_{min}$ to T_{max}	Monotonicity Guaranteed			Monotonicity Guaranteed			Monotonicity Guaranteed			LSB
Gain Error[4]		±0.1	±0.2		±0.1	±0.2		±0.1	±0.2	% of FSR[5]
Unipolar Offset Error[4]		±1	±2		±1	±2		±1	±2	LSB
Bipolar Zero Error[4]		±0.05	±0.1		±0.05	±0.1		±0.05	±0.1	% of FSR
DRIFT										
Gain T_A = 25°C to T_{min} or T_{max}		±5	±30		±5	±15		±5	±30	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} or T_{max}		±1	±3		±1	±3		±1	±3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{min} or T_{max}		±5	±10			±10		±5	±10	ppm of FSR/°C
CONVERSION SPEED										
Settling Time to ±0.01% of FSR for FSR change (2kΩ‖500pF load)										
with 10kΩ Feedback		3	4		3	4		3	4	μs
with 5kΩ Feedback		2	3		2	3		2	3	μs
For LSB Change		1			1			1		μs
Slew Rate	10			10			10			V/μs
ANALOG OUTPUT										
Ranges[6]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short-Circuit Current			40			40			40	mA
REFERENCE OUTPUT	9.90	10.00	10.10	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY										
V_{CC} = + 11.4 to + 16.5V dc		5	10		5	10		5	10	ppm of FS/%
V_{EE} = − 11.4 to − 16.5V dc		5	10		5	10		5	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±12, ±15			±12, ±15			±12, ±15		V
Range[6]	±11.4		±16.5	±11.4		±16.5	±11.4		±16.5	V
Supply Current										
+ 11.4 to + 16.5V dc		9	13		9	13		9	13	mA
− 11.4 to − 16.5V dc		18	23		18	23		18	23	mA
Total Power Consumption		400	600		400	600		400	600	mW
TEMPERATURE RANGE										
J/K	0		+70	0		+70				°C
A/B	−25		+85	−25		+85	−25		+85	°C
S	−55		+125	−55		+125				°C
Operating	−55		+125	−55		+125				°C
Storage (All Grades)	−65		+125	−65		+125	−65		+125	°C

NOTES

[1]AD767 "S" specifications shown for information only. Consult Analog Devices Military Databook or contact factory for a controlled specification sheet.

[2]AD767A Chips specifications are tested at +25°C and, when in boldface, at +85°C. They are typical at −25°C.

[3]The digital input specifications are 100% tested at +25°C, and guaranteed but not tested over the full temperature range.

[4]Adjustable to zero.

[5]FSR means "Full-Scale Range" and is 20V for ±10V range and 10V for the ±5V range.

[6]A minimum power supply of ±12.5V is required for a ±10V full-scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test (except per Notes 1 and 2). Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

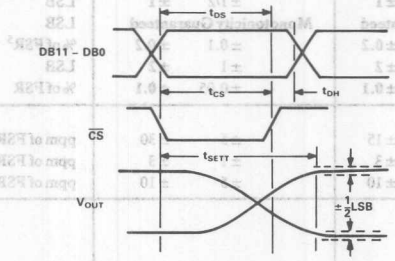
ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Power Ground . . . . . 0V to +18V
V_{EE} to Power Ground . . . . . 0V to −18V
Digital Inputs (Pins 11, 13–24)
to Power Ground . . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out, V_{OUT} (Pins 6, 9) . . Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TIMING SPECIFICATIONS

(All Models, T_A = 25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V)

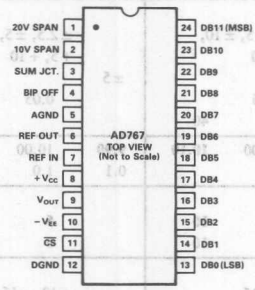


Symbol	Parameter	Min	Typ	Max	
t_{DS}	Data Valid to End of $\overline{CS}$	40	–	–	ns
	(−25°C to +85°C)	60	–	–	ns
	(−55°C to +125°C)	90	–	–	ns
t_{DH}	Data Hold Time	10	–	–	ns
	(−25°C to +85°C)	10	–	–	ns
	(−55°C to +125°C)	20	–	–	ns
t_{CS}	$\overline{CS}$ Pulse Width	40	–	–	ns
	(−25°C to +85°C)	60	–	–	ns
	(−55°C to +125°C)	90	–	–	ns
t_{SETT}	Output Voltage Settling Time*	–	2	4	µs

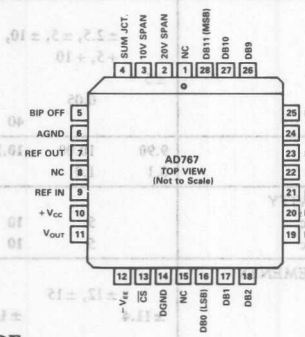
*t_{SETT} is measured referenced to the leading edge of t_{CS}. If $t_{CS} > t_{DS}$, then t_{SETT} is measured referenced to the beginning of Data Valid.

PIN CONFIGURATION

DIP



PLCC



ORDERING GUIDE

Model[1]	Package Option[2]	Temperature Range °C	Linearity Error Max T_{min}–T_{max}	Gain T.C. Max ppm/°C
AD767JN	Plastic DIP (N-24)	0 to +70	±1LSB	30
AD767JP	PLCC (P-28A)	0 to +70	±1LSB	30
AD767KN	Plastic DIP (N-24)	0 to +70	±1/2LSB	15
AD767KP	PLCC (P-28A)	0 to +70	±1/2LSB	15
AD767AD	Ceramic DIP (D-24A)	−25 to +85	±1LSB	30
AD767BD	Ceramic DIP (D-24A)	−25 to +85	±1/2LSB	15
AD767SD/883B	Ceramic DIP (D-24A)	−55 to +125	Note 2	Note 2
AD767A Chips	N/A	−25 to +85	±1LSB	30

NOTES
[1]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.
[2]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD767/883B data sheet.

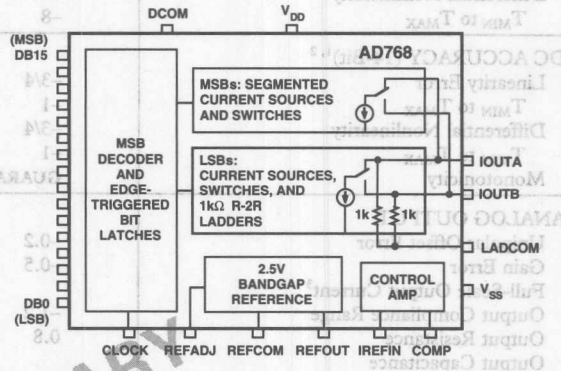
ANALOG DEVICES

16-Bit, 32 MSPS Low Glitch D/A Converter

AD768

FEATURES
32 MSPS Update Rate
16-Bit Resolution
Linearity: 1 LSB DNL @ 14 Bits
1 LSB INL @ 14 Bits
Fast Settling: 25 ns Full-Scale Settling to 0.025%
SFDR @ 1 MHz Output: 80 dBc
Low Glitch Impulse: 60 pV-s
Power Dissipation: 500 mW
On-Chip 2.5 V Reference
Edge-Triggered Latches
CMOS Compatibility

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD768 is a 16-bit, high speed digital-to-analog converter (DAC) that offers exceptional ac and dc linearity. The AD768 is manufactured on Analog Devices' Advanced Bipolar CMOS (ABCMOS) process, combining the speed of bipolar transistors, the accuracy of laser trimmable thin-film resistors, and the efficiency of CMOS logic. A segmented current source architecture is combined with a proprietary switching technique to reduce glitch energy and maximize dynamic accuracy. Edge triggered input latches and a temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution.

The AD768 is a current-output DAC with a nominal full-scale output current of 20 mA and a 1 kΩ output impedance. Differential current outputs are provided to support single-ended or differential applications. The current outputs may be tied directly to an output resistor to provide a voltage output, or fed to the summing junction of a high speed amplifier to provide a buffered voltage output.

The on-chip reference and control amplifer are configured for maximum accuracy and flexibility. The AD768 can be driven by the on-chip reference or by a variety of external reference voltages based on the selection of an external resistor. An external capacitor allows the user to optimally tradeoff reference bandwidth and noise performance.

The AD768 operates on ±5 V supplies, typically consuming 500 mW of power. The AD768 is available in a 28-pin SOIC package and is specified for operation over the industrial temperature range.

PRODUCT HIGHLIGHTS

1. The low glitch and fast settling time provide outstanding dynamic performance for waveform reconstruction or digital synthesis requirements, including communications.
2. The excellent dc accuracy of the AD768 makes it suitable for high speed A/D conversion applications.
3. On-chip, edge-triggered input CMOS latches interface readily to CMOS logic families. The AD768 can support update rates up to 32 Msps.
4. A temperature compensated, 2.5 V bandgap reference is included on-chip allowing for generation of the reference input current with the use of a single external resistor. An external reference may also be used.
5. The current output(s) of the AD768 may be used singly or differentially, either into a load resistor or external op amp summing junction.
6. Proper selection of an external resistor and compensation capacitor allow the performance-conscious user to optimize the AD768 reference level and bandwidth for the target application.

PRELIMINARY TECHNICAL DATA

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD768–SPECIFICATIONS (T_A = +25°C, V_{DD} = +5.0 V, V_{SS} = –5 V, LADCOM, REFCOM, DCOM = 0 V, IREFIN = 5 mA, CLOCK =10 MHz, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	16			Bits
DC ACCURACY (16-Bit)[1]				
Linearity Error	–6	±4	+6	LSB
T_{MIN} to T_{MAX}	–8		+8	LSB
Differential Nonlinearity	–6	±4	+6	LSB
T_{MIN} to T_{MAX}	–8		+8	LSB
DC ACCURACY (14-Bit)[1, 2]				
Linearity Error	–3/4	±1/2	+3/4	LSB
T_{MIN} to T_{MAX}	–1		+1	LSB
Differential Nonlinearity	–3/4	±1/2	+3/4	LSB
T_{MIN} to T_{MAX}	–1		+1	LSB
Monotonicity	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE			
ANALOG OUTPUT				
Unipolar Offset Error	–0.2		+0.2	% of FSR
Gain Error	–0.5		+0.5	% of FSR
Full-Scale Output Current[3]		20		mA
Output Compliance Range	–1.2		+2.5	V
Output Resistance	0.8	1.0	1.2	kΩ
Output Capacitance		15		pF
REFERENCE OUTPUT				
Reference Voltage	2.475	2.5	2.525	V
Reference Output Current[4]			+10	mA
REFERENCE INPUT				
Reference Input Current	4.5	5	5.5	mA
Reference Bandwidth[5]		20		MHz
TEMPERATURE COEFFICIENTS				
Unipolar Offset Drift	–5		+5	ppm of FSR/°C
Gain Drift[6]	–20		+20	ppm of FSR/°C
Gain Drift[7]	–40		+40	ppm of FSR/°C
Reference Voltage Drift	–20		+20	ppm/°C
DYNAMIC PERFORMANCE				
Output Update Rate	32	40		Msps
Output Settling Time (t_{ST})(to 0.025%)[8]		25	35	ns
Output Propagation Delay (t_{PD})		5		ns
Glitch Impulse		60		pV-s
Output Rise Time		5		ns
Output Fall Time		5		ns
DIGITAL INPUTS				
Logic "1" Voltage	3.5			V
Logic "0" Voltage			1.5	V
Logic "1" Current	–10		+10	µA
Logic "0" Current	–10		+10	µA
Input Capacitance		10		pF
Input Setup Time (t_S)	5			ns
Input Hold Time (t_H)	5			ns
Latch Pulse Width (t_{LPW})	15			ns
OPERATING RANGE	–40		+85	°C

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	Min	Typ	Max	Units
AC LINEARITY				
Spurious-Free Dynamic Range (SFDR)				
f_{OUT} = 500 kHz; CLOCK = 10 MHz		–80		dB
f_{OUT} = 1.0 MHz; CLOCK = 10 MHz		–80	TBD	dB
f_{OUT} = 5 MHz; CLOCK = 30 MHz		TBD		dB
Total Harmonic Distortion (THD)				
f_{OUT} = 500 kHz; CLOCK = 10 MHz		TBD		dB
f_{OUT} = 1.0 MHz; CLOCK = 10 MHz		TBD	TBD	dB
f_{OUT} = 5 MHz; CLOCK = 30 MHz		TBD		dB
POWER SUPPLY				
Positive Voltage Range	4.75		5.25	V
Negative Voltage Range	–5.25		–4.75	V
Positive Supply Current		33	TBD	mA
Negative Supply Current		67	TBD	mA
Nominal Power Dissipation		500	TBD	mW
Power Supply Rejection Ratio (PSRR)			TBD	% of FSR/V

NOTES
[1]Measured at $I_{OUT}A$, driving a virtual ground.
[2]Three LSBs are grounded, DB0, DB1, and DB2.
[3]Nominal FS output current is 4× the current at IREFIN. Therefore, nominal FS current is 20 mA when IREFIN = 5 mA.
[4]Output current is defined as total current available for IREFIN and any external load.
[5]Reference bandwidth is a function of external cap at COMP pin.
[6]Excludes internal reference drift.
[7]Includes internal reference drift.
[8]Measured as unbuffered voltage output (1 V step) with FS current into 50 Ω load.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

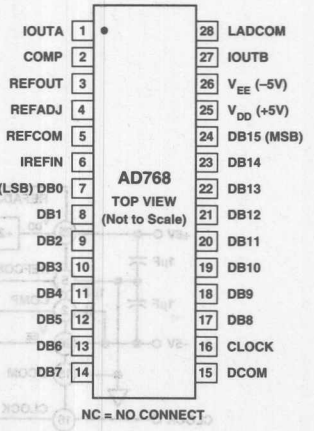
ABSOLUTE MAXIMUM RATINGS[1]

Parameter	With Respect to	Min	Max	Units
Positive Supply Voltage (V_{DD})	DCOM, REFCOM, LADCOM	–0.5	+6.0	V
Negative Supply Voltage (V_{EE})	DCOM, REFCOM, LADCOM	–6.0	+0.5	V
Analog-to-Other Grounds (REFCOM)	DCOM, LADCOM	–0.5	+0.5	V
Digital-to-Other Grounds (DCOM)	LADCOM, REFCOM	–0.5	+0.5	V
Reference Output (REFOUT)	REFCOM		V_{DD} + 0.5	V
Reference Adjust (REFADJ)	REFCOM	–0.5	V_{DD} + 0.5	V
Reference Input Current (IREFIN)			+6.0	mA
Digital Inputs (DB0–DB15, Clock)	DCOM	–0.5	V_{DD} + 0.5	V
Analog Outputs ($I_{OUT}A$, $I_{OUT}B$)	LADCOM	–2.0	+5.0	V
Maximum Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature			+300	°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating for extended periods may affect device reliability.

PIN CONFIGURATION

28-PIN SOIC



NC = NO CONNECT

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD768 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PIN DESCRIPTION

Pin No.	Symbol	Type	Name and Function
1	IOUTA	AO	DAC Current Output. Full-scale current when all data bits are 1s.
2	COMP	AI	Compensation Node. Add capacitor for noise reduction.
3	REFOUT	AO	Reference Output Voltage. Nominal value is 2.5 V.
4	REFADJ	AI	Reference Adjust. Apply voltage from 0 to 2.5 V to adjust DAC gain.
5	REFCOM	P	Reference Ground.
6	IREFIN	AI	Reference Input Current. Nominal is 5 mA. DAC full-scale is 4× this current.
7	DB0	DI	Data Bit 0 (LSB).
8–14	DB1–7	DI	Data Bits 1–7.
15	DCOM	P	Digital Ground.
16	CLOCK	DI	Clock Input. Data latched on positive edge of clock.
17–23	DB8–DB14	DI	Data Bits 8–14.
24	DB15	DI	Data Bit 15 (MSB).
25	V_{DD}	P	Positive Supply Voltage. Nominal is +5 V.
26	V_{EE}	P	Negative Supply Voltage. Nominal is –5 V.
27	IOUTB	AO	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
28	LADCOM	P	DAC Ladder Common.

Type: AI = Analog Input; DI = Digital Input; AO = Analog Output; P = Power

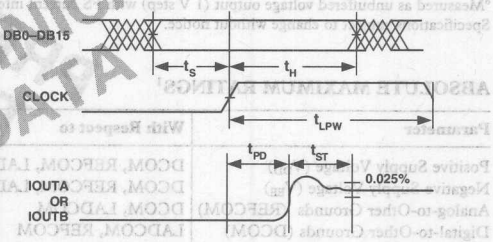
ORDERING GUIDE

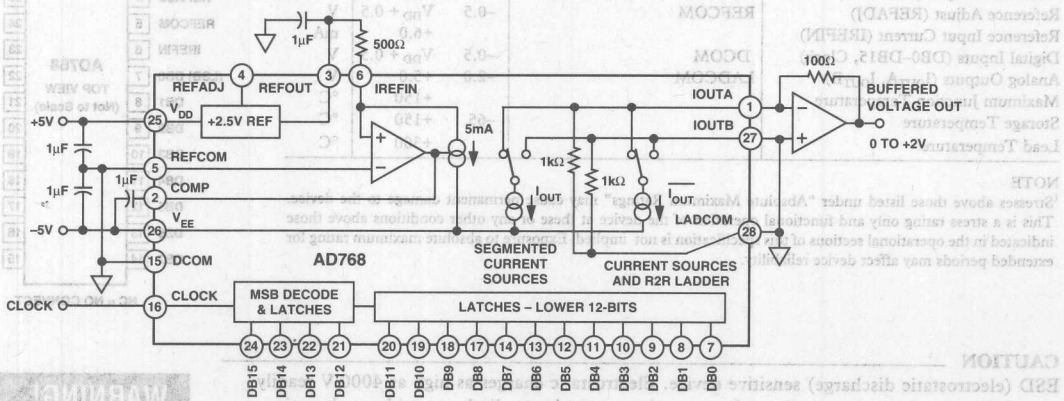
Model	Package*
AD768AR	28-Pin 300 mil SOIC

*For outline information see Package Information section.

PRELIMINARY TECHNICAL DATA

TIMING DIAGRAM





Typical Configuration: Buffered Unipolar Voltage Output

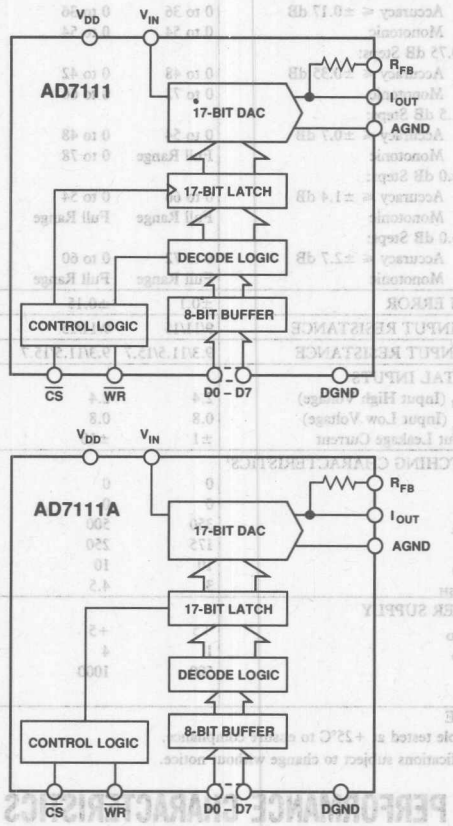
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

LC²MOS LOGDAC
Logarithmic D/A Converter
AD7111/AD7111A

FEATURES
- Dynamic Range: 88.5 dB
- Resolution: 0.375 dB
- On-Chip Data Latches
- +5 V Operation
- AD7111A Pin Compatible with AD7524
- Low Power

APPLICATIONS
- Audio Attenuators
- Sonar Systems
- Function Generators
- Digitally Controlled AGC System

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The LOGDAC® AD7111/AD7111A are monolithic multiplying D/A converters featuring wide dynamic range in a small package. Both DACs can attenuate an analog input signal over the range 0 dB to 88.5 dB in 0.375 dB steps. They are available in 16-pin DIPs and SOIC packages. The AD7111 is also available in a 20-terminal LCCC package.

The degree of attenuation across the DAC is determined by an 8-bit word applied to the on-board decode logic. This 8-bit word is decoded into a 17-bit word which is then applied to a 17-bit R-2R ladder. The very fine step resolution, which is available over the entire dynamic range, is due to the use of this 17-bit DAC.

The AD7111/AD7111A are easily interfaced to a standard 8-bit MPU bus via an 8-bit data port and standard microprocessor control lines. The AD7111 $\overline{WR}$ input is edge triggered and requires a rising edge to load new data to the DAC. The AD7111A $\overline{WR}$ is level triggered to allow transparent operation of the latches, if required. It should also be noted that the AD7111A is exactly pin and function-compatible with the AD7524, an industry standard 8-bit multiplying DAC. This allows an easy upgrading of existing AD7524 designs which would benefit both from the wider dynamic range and the finer step resolution offered by the AD7111A.

The AD7111/AD7111A are fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic.

LOGDAC is a registered trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. Wide Dynamic Range: 0 dB to 88.5 dB attenuation range in 0.375 dB steps.
2. Small Package: The AD7111/AD7111A are available in 16-pin DIPs and SOIC packages.
3. Transparent Latch Operation: By tying the $\overline{CS}$ and $\overline{WR}$ inputs low, the DAC latches in the AD7111A can be made transparent.
4. Fast Microprocessor Interface: Data setup times of 25 ns and write pulse width of 57 ns make the AD7111A compatible with modern microprocessors.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7111—ELECTRICAL CHARACTERISTICS (Output amplifier AD711 except where noted)

Parameter	AD7111L/C/U Grades T_A = +25°C	AD7111L/C/U Grades T_A = T_{MIN}, T_{MAX}	AD7111K/B/T Grades T_A = +25°C	AD7111K/B/T Grades T_A = T_{MIN}, T_{MAX}	Units	Conditions/Comments
NOMINAL RESOLUTION	0.375	0.375	0.375	0.375	dB	
ACCURACY RELATIVE TO						
0 dB ATTENUATION						
0.375 dB Steps:						
Accuracy ≤ ±0.17 dB	0 to 36	0 to 36	0 to 30	0 to 30	dB min	Guaranteed Attenuation Ranges
Monotonic	0 to 54	0 to 54	0 to 48	0 to 48	dB min	for Specified Step Sizes
0.75 dB Steps:						
Accuracy ≤ ±0.35 dB	0 to 48	0 to 42	0 to 42	0 to 36	dB min	
Monotonic	0 to 72	0 to 66	0 to 72	0 to 60	dB min	
1.5 dB Steps:						
Accuracy ≤ ±0.7 dB	0 to 54	0 to 48	0 to 48	0 to 42	dB min	Full Range Is from 0 dB
Monotonic	Full Range	0 to 78	0 to 85.5	0 to 72	dB min	to 88.5 dB
3.0 dB Steps:						
Accuracy ≤ ±1.4 dB	0 to 66	0 to 54	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range	dB min	
6.0 dB Steps:						
Accuracy ≤ ±2.7 dB	0 to 72	0 to 60	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range	dB min	
GAIN ERROR	±0.1	±0.15	±0.15	±0.20	dB max	
V_{IN}, INPUT RESISTANCE	9/11/15	9/11/15	7/11/18	7/11/18	kΩ min/typ/max	
R_{FB} INPUT RESISTANCE	9.3/11.5/15.7	9.3/11.5/15.7	7.3/11.5/18.8	7.3/11.5/18.8	kΩ min/typ/max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±10	±1	±10	μA max	Digital Inputs = V_{DD}
SWITCHING CHARACTERISTICS[1]						
t_{CS}	0	0	0	0	ns min	Chip Select to Write Setup Time
t_{CH}	0	0	0	0	ns min	Chip Select to Write Hold Time
t_{WR}	350	500	350	500	ns min	Write Pulse Width
t_{DS}	175	250	175	250	ns min	Data Valid to Write Setup Time
t_{DH}	10	10	10	10	ns min	Data Valid to Write Hold Time
t_{RFSH}	3	4.5	3	4.5	μs min	Refresh Time
POWER SUPPLY						
V_{DD}	+5	+5	+5	+5	V	
I_{DD}	1	4	1	4	mA max	Digital Inputs = V_{IL} or V_{IH}
	500	1000	500	1000	μA max	Digital Inputs = 0 V or V_{DD}; See Figure 6

NOTE
[1]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test. V_{DD} = +5 V, V_{IN} = −10 V dc except where noted, I_{OUT} = AGND = DGND = 0 V, output amplifier AD711 except where noted.

Parameter	AD7111L/C/U Grades T_A = +25°C	AD7111L/C/U Grades T_A = T_{MIN}, T_{MAX}	AD7111K/B/T Grades T_A = +25°C	AD7111K/B/T Grades T_A = T_{MIN}, T_{MAX}	Units	Conditions/Comments
DC Supply Rejection, $\Delta Gain/\Delta V_{DD}$	0.001	0.005	0.001	0.005	dB per % max	ΔV_{DD} = ± 10%, Input Code = 00000000
Propagation Delay	3.0	4.5	3.0	4.5	μs max	Full Scale Change Measured from $\overline{WR}$ Going High, $\overline{CS}$ = 0 V
Digital-to-Analog Glitch Impulse	100	–	100	–	nV secs typ	Measured with AD843 as Output Amplifier for Code Transition 10000000 to 00000000 C1 of Figure 1 is 0 pF
Output Capacitance, Pin 1	185	185	185	185	pF max	
Input Capacitance, Pin 15 and Pin 16	7	7	7	7	pF max	
Feedthrough at 1 kHz	−94	−72	−92	−68	dB max	
Total Harmonic Distortion	−91	−91	−91	−91	dB typ	V_{IN} = 6 V rms at 1 kHz
Output Noise Voltage Density	70	70	70	70	nV/√Hz max	Includes AD711 Amplifier Noise
Digital Input Capacitance	7	7	7	7	pF max	

Specifications subject to change without notice.

AD7111A—ELECTRICAL CHARACTERISTICS (V_{DD} = +5 V, V_{IN} = −10 V dc, I_{OUT} = AGND = DGND = 0 V output amplifier AD711 except where noted)

Parameter	AD7111AC Grade T_A = +25°C	AD7111AC Grade T_A = T_{MIN}, T_{MAX}	AD7111AB Grade T_A = +25°C	AD7111AB Grade T_A = T_{MIN}, T_{MAX}	Units	Conditions/Comments
NOMINAL RESOLUTION	0.375	0.375	0.375	0.375	dB	
ACCURACY RELATIVE TO 0 dB ATTENUATION						
0.375 dB Steps:						
Accuracy ≤ ±0.17 dB	0 to 36	0 to 36	0 to 30	0 to 30	dB min	Guaranteed Attenuation Ranges
Monotonic	0 to 54	0 to 54	0 to 48	0 to 48	dB min	for Specified Step Sizes
0.75 dB Steps:						
Accuracy ≤ ±0.35 dB	0 to 48	0 to 42	0 to 42	0 to 36	dB min	
Monotonic	0 to 72	0 to 66	0 to 72	0 to 60	dB min	
1.5 dB Steps:						
Accuracy ≤ ±0.7 dB	0 to 54	0 to 48	0 to 48	0 to 42	dB min	Full Range Is from 0 dB
Monotonic	Full Range	0 to 78	0 to 85.5	0 to 72	dB min	to 88.5 dB
3.0 dB Steps:						
Accuracy ≤ ±1.4 dB	0 to 66	0 to 54	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range	dB min	
6.0 dB Steps:						
Accuracy ≤ ±2.7 dB	0 to 72	0 to 60	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range	dB min	
GAIN ERROR	±0.1	±0.15	±0.15	±0.20	dB max	
V_{IN} INPUT RESISTANCE	9/11/15	9/11/15	7/11/18	7/11/18	kΩ min/typ/max	
R_{FS} INPUT RESISTANCE	9.3/11.5/15.7	9.3/11.5/15.7	7.3/11.5/18.8	7.3/11.5/18.8	kΩ min/typ/max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±10	±1	±10	μA max	Digital Inputs = V_{DD}
SWITCHING CHARACTERISTICS[1]						
t_{CS}	0	0	0	0	ns min	Chip Select to Write Setup Time
t_{CH}	0	0	0	0	ns min	Chip Select to Write Hold Time
t_{WR}	57	57	57	57	ns min	Write Pulse Width
t_{DS}	25	25	25	25	ns min	Data Valid to Write Setup Time
t_{DH}	10	10	10	10	ns min	Data Valid to Write Hold Time
POWER SUPPLY						
V_{DD}	+5	+5	+5	+5	V	Data Inputs = V_{IL} or V_{IH}
I_{DD}	1	2	1	2	mA max	$\overline{CS}$ = $\overline{WR}$ = 0 V
	1	1	1	1	mA max	Digital Inputs = 0 V or V_{DD}; See Figure 6

NOTE
[1]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS These characteristics are included for design guidance only and are not subject to test. V_{DD} = +5 V, V_{IN} = −10 V dc except where noted, I_{OUT} = AGND = DGND = 0 V, output amplifier AD711 except where noted.

Parameter	AD7111AC Grade T_A = +25°C	AD7111AC Grade T_A = T_{MIN}, T_{MAX}	AD7111AB Grade T_A = +25°C	AD7111AB Grade T_A = T_{MIN}, T_{MAX}	Units	Conditions/Comments
DC Supply Rejection, $\Delta Gain/\Delta V_{DD}$	0.001	0.005	0.001	0.005	dB per % max	ΔV_{DD} = ± 10%, Input Code = 00000000
Propagation Delay	1	1.5	1	1.5	μs max	Full Scale Change Measured from $\overline{WR}$ Going High, $\overline{CS}$ = 0 V
Digital-to-Analog Glitch Impulse	10	20	10	20	nV secs typ	Measured with AD843 as Output Amplifier for Code Transition 10000000 to 00000000 C1 of Figure 1 is 0 pF
Output Capacitance, Pin 1	50	50	50	50	pF max	
Input Capacitance, Pin 15 and Pin 16	7	7	7	7	pF max	
Feedthrough at 1 kHz	−94	−90	−92	−90	dB max	
Total Harmonic Distortion	−91	−91	−91	−91	dB typ	V_{IN} = 6 V rms at 1 kHz
Output Noise Voltage Density	70	70	70	70	nV/√Hz max	Includes AD711 Amplifier Noise
Digital Input Capacitance	7	7	7	7	pF max	

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (to DGND)	+7 V
V_{IN} (to AGND)	±35 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
I_{OUT} to AGND	−0.3 V to V_{DD}
V_{RFB} to AGND	±35 V
AGND to DGND	0 to V_{DD}
DGND to AGND	0 to V_{DD}
Power Dissipation, DIP	1 W
θ_{JA}, Thermal Impedance	117°C/W
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation, SOIC	1 W
θ_{JA}, Thermal Impedance	75°C/W
Lead Temperature (Soldering)	
Vapor Phase (60 secs)	215°C
Infrared (15 secs)	220°C
Power Dissipation, LCCC	1 W
θ_{JA}, Thermal Impedance	76°C/W
Lead Temperature (Soldering, 10secs)	+300°C
Operating Temperature Range	
Commercial (K, L Versions)	0°C to +70°C
Industrial (B, C Versions)	−40°C to +85°C
Extended (T, U Versions)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper precautions are recommended to avoid any performance degradation or loss of functionality.

ORDERING GUIDES

AD7111A ORDERING GUIDE

Model	Temperature Range	Specified Accuracy Range	Package Option[1]
AD7111ABN	−40°C to +85°C	0 dB to 60 dB	N-16
AD7111ACN	−40°C to +85°C	0 dB to 72 dB	N-16
AD7111ABR	−40°C to +85°C	0 dB to 60 dB	R-16
AD7111ACR	−40°C to +85°C	0 dB to 72 dB	R-16

NOTE
[1]N = Plastic DIP; R = SOIC. For outline information see Package Information section.

AD7111 ORDERING GUIDE

Model[1]	Temperature Range	Specified Accuracy Range	Package Option[2]
AD7111KN	0°C to +70°C	0 dB to 60 dB	N-16
AD7111BQ	−40°C to +85°C	0 dB to 60 dB	Q-16
AD7111LN	0°C to +70°C	0 dB to 72 dB	N-16
AD7111CQ	−40°C to +85°C	0 dB to 72 dB	Q-16
AD7111UQ/883B	−55°C to +125°C	0 dB to 72 dB	Q-16
AD7111TE/883B	−55°C to +125°C	0 dB to 60 dB	E-20A

NOTES
[1]To order MIL-STD-883B, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet and availability.
[2]N = Plastic DIP; Q = Cerdip; E = LCCC; R = SOIC. For outline information see Package Information section.

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent codes.

MONOTONICITY: The device is monotonic if the analog output decreases (or remains constant) as the digital code increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when all digital inputs are high. See section on Applications.

OUTPUT LEAKAGE CURRENT: Current which appears on the I_{OUT} terminal with all digital inputs high.

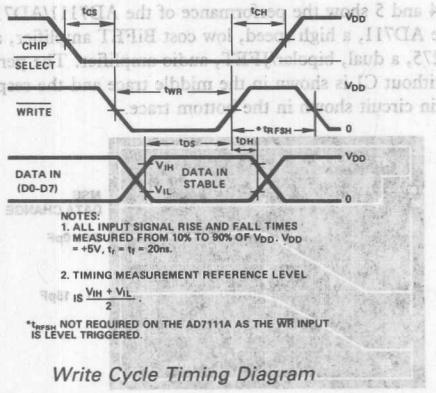
TOTAL HARMONIC DISTORTION: A measure of the harmonics introduced by the circuit when a pure sinusoid is applied to the input. It is expressed as the harmonic energy divided by the fundamental energy at the output.

ACCURACY: The difference (measured in dB) between the ideal transfer function as listed in Table I and the actual transfer function as measured with the device.

OUTPUT CAPACITANCE: Capacitance from I_{OUT} to ground.

DIGITAL-TO-ANALOG GLITCH IMPULSE: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{IN} = AGND.

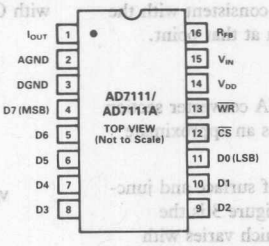
PROPAGATION DELAY: This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.



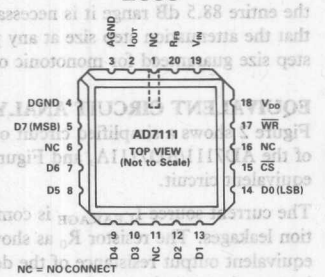
Write Cycle Timing Diagram

PIN CONFIGURATIONS

DIP/SOIC



LCCC



3

CIRCUIT DESCRIPTION

GENERAL CIRCUIT DESCRIPTION

The AD7111/AD7111A consists of a 17-bit R-2R CMOS multiplying D/A converter with extensive digital logic. The logic translates the 8-bit binary input into a 17-bit word which is used to drive the D/A converter. Input data on the D7–D0 bus is loaded into the input data latches using $\overline{CS}$ and $\overline{WR}$ control signals. When using the AD7111, the rising edge of $\overline{WR}$ latches the input data and initiates the internal data transfer to the decoder. A minimum time t_{RFSH}, the refresh time, is required for the data to propagate through the decoder before a new data write is attempted.

In contrast, the AD7111A $\overline{WR}$ input is level triggered to allow transparent operation of the latches if required.

The transfer function for the circuit of Figure 1 is given by:

$$V_O = -V_{IN}\, 10\, exp\, -\frac{0.375\, N}{20}$$

$$or \left|\frac{V_O}{V_{IN}}\right| dB = -0.375\, N$$

where 0.375 is the step size (resolution) in dB and N is the input code in decimal for values 0 to 239. For $240 \leq N \leq 255$ the output is zero. Table I gives the output attenuation relative to 0 dB for all possible input codes.

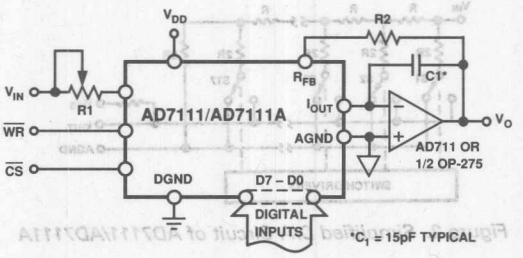


Figure 1. Typical Circuit Configuration

The graphs on the last page give a pictorial representation of the specified accuracy and monotonic ranges for all grades of the AD7111/AD7111A. High attenuation levels are specified with less accuracy than low attenuation levels. The range of monotonic behavior depends upon the attenuation step size used. For

Table I. Ideal Attenuation in dB vs. Input Code

D7–D4 \ D3–D0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0.0	0.375	0.75	1.125	1.5	1.875	2.25	2.625	3.0	3.375	3.75	4.125	4.5	4.875	5.25	5.625
0001	6.0	6.375	6.75	7.125	7.5	7.875	8.25	8.625	9.0	9.375	9.75	10.125	10.5	10.875	11.25	11.625
0010	12.0	12.375	12.75	13.125	13.5	13.875	14.25	14.625	15.0	15.375	15.75	16.125	16.5	16.875	17.25	17.625
0011	18.0	18.375	18.75	19.125	19.5	19.875	20.25	20.625	21.0	21.375	21.75	22.125	22.5	22.875	23.25	23.625
0100	24.0	24.375	24.75	25.125	25.5	25.875	26.25	26.625	27.0	27.375	27.75	28.125	28.5	28.875	29.25	29.625
0101	30.0	30.375	30.75	31.125	31.5	31.875	32.25	32.625	33.0	33.375	33.75	34.125	34.5	34.875	35.25	35.625
0110	36.0	36.375	36.75	37.125	37.5	37.875	38.25	38.625	39.0	39.375	39.75	40.125	40.5	40.875	41.25	41.625
0111	42.0	42.375	42.75	43.125	43.5	43.875	44.25	44.625	45.0	45.375	45.75	46.125	46.5	46.875	47.25	47.625
1000	48.0	48.375	48.75	49.125	49.5	49.875	50.25	50.625	51.0	51.375	51.75	52.125	52.5	52.875	53.25	53.625
1001	54.0	54.375	54.75	55.125	55.5	55.875	56.25	56.625	57.0	57.375	57.75	58.125	58.5	58.875	59.25	59.625
1010	60.0	60.375	60.75	61.125	61.5	61.875	62.25	62.625	63.0	63.375	63.75	64.125	64.5	64.875	65.25	65.625
1011	66.0	66.375	66.75	67.125	67.5	67.875	68.25	68.625	69.0	69.375	69.75	70.125	70.5	70.875	71.25	71.625
1100	72.0	72.375	72.75	73.125	73.5	73.875	74.25	74.625	75.0	75.375	75.75	76.125	76.5	76.875	77.25	77.625
1101	78.0	78.375	78.75	79.125	79.5	79.875	80.25	80.625	81.0	81.375	81.75	82.125	82.5	82.875	83.25	83.625
1110	84.0	84.375	84.75	85.125	85.5	85.875	86.25	86.625	87.0	87.375	87.75	88.125	88.5	88.875	89.25	89.625
1111	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE

0 dB to −72 dB inclusive. To achieve monotonic operation over the entire 88.5 dB range it is necessary to select input codes so that the attenuation step size at any point is consistent with the step size guaranteed for monotonic operation at that point.

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows a simplified circuit of the D/A converter section of the AD7111/AD7111A, and Figure 3 gives an approximate equivalent circuit.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R_0 as shown in Figure 3 is the equivalent output resistance of the device which varies with input code (excluding all 0s code) from 0.8R to 2R. R is typically 12 kΩ. C_{OUT} is the capacitance due to the N channel switches and varies from about 20 pF to 50 pF depending upon the digital input. For further information on CMOS multiplying D/A converters, refer to "CMOS DAC Application Guide" which is available from Analog Devices, Publication Number G872b–8–1/89.

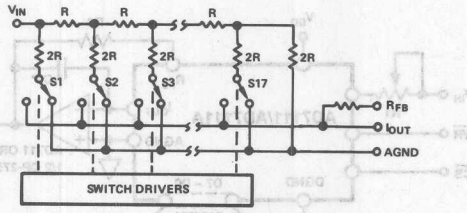


Figure 2. Simplified D/A Circuit of AD7111/AD7111A

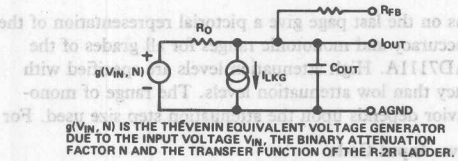


Figure 3. Equivalent Analog Output Circuit of AD7111/AD7111A

DYNAMIC PERFORMANCE

The dynamic performance of the AD7111/AD7111A will depend upon the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Circuit layout is most important if the optimum performance of the AD7111/AD7111A is to be achieved. Most application problems stem from either poor layout, grounding errors, or inappropriate choice of amplifier.

It is recommended that when using the AD7111/AD7111A with a high speed amplifier, a capacitor (C1) be connected in the feedback path as shown in Figure 1. This capacitor, which should be between 10 pF and 30 pF, compensates for the phase lag introduced by the output capacitance of the D/A converter.

the OP-279, a dual, bipolar/JFET, audio amplifier. The performance without C1 is shown in the middle trace and the response with C1 in circuit shown in the bottom trace.

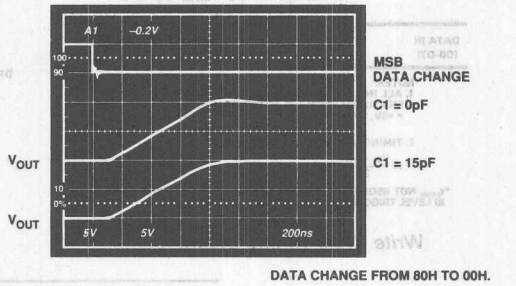


Figure 4. Response of AD7111/AD7111A with AD711

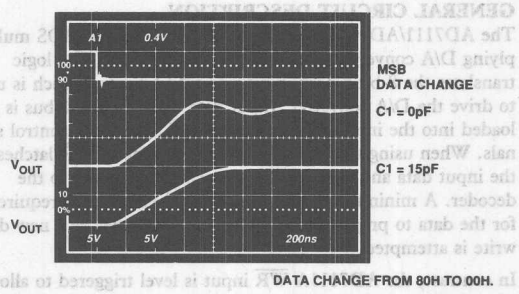


Figure 5. Response of AD7111/AD7111A with 1/2 OP-275

In conventional CMOS D/A converter design, parasitic capacitance in N-channel D/A converter switches can give rise to glitches on the D/A converter output. These glitches result from digital feedthrough. The AD7111/AD7111A has been designed to minimize these glitches as much as possible.

For operation beyond 250 kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figure 5. In circuits where C1 is not included, the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7111/AD7111A.

Feedthrough and absolute accuracy are sensitive to output leakage current effects. For this reason it is recommended that the operating temperature of the AD7111/AD7111A be kept as close to 25°C as is practically possible, particularly where the device's performance at high attenuation levels is important.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7111/AD7111A does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

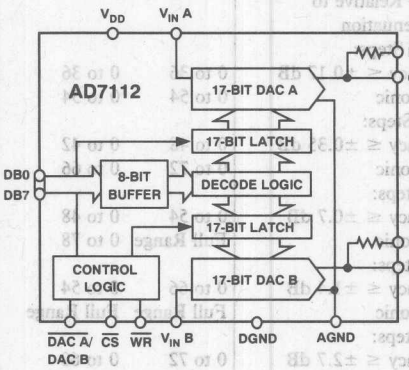
LC²MOS LOGDAC
Dual Logarithmic D/A Converter

AD7112*

FEATURES
Dynamic Range: 88.5 dB
Resolution: 0.375 dB
On-Chip Data Latches for Both DACs
Four-Quadrant Multiplication
+5 V Operation
Pin Compatible with AD7528
Low Power

APPLICATIONS
Audio Attenuators
Sonar Systems
Function Generators

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The LOGDAC® AD7112 is a monolithic dual multiplying D/A converter featuring wide dynamic range and excellent DAC-to-DAC matching. Both DACs can attenuate an analog input signal over the range 0 to 88.5 dB in 0.375 dB steps. It is available in skinny 0.3″ wide 20-pin DIPs and in 20-terminal surface mount packages.

The degree of attenuation in either channel is determined by the 8-bit word applied to the on-board decode logic. This 8-bit word is decoded into a 17-bit word which is then loaded into one of the 17-bit data latches, determined by $\overline{\text{DACA}}$/DACB. The fine step resolution over the entire dynamic range is due to the use of these 17-bit DACs.

The AD7112 is easily interfaced to a standard 8-bit MPU bus via an 8-bit data port and standard microprocessor control lines. It should be noted that the AD7112 is exactly pin-compatible with the AD7528, an industry standard dual 8-bit multiplying DAC. This allows an easy upgrading of existing AD7528 designs which would benefit both from the wider dynamic range and the finer step resolution offered by the AD7112.

The AD7112 is fabricated in Linear Compatible CMOS (LC^2MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic.

PRODUCT HIGHLIGHTS

1. DAC-to-DAC Matching: Since both of the AD7112 DACs are fabricated at the same time on the same chip, precise matching and tracking between the two DACs is inherent.
2. Small Package: The AD7112 is available in a 20-pin DIP and a 20-terminal SOIC package.
3. Fast Microprocessor Interface: The AD7112 has bus interface timing compatible with all modern microprocessors.

***Protected by U.S. Patent No. 4521764**
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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7112—SPECIFICATIONS (V_{DD} = +5 V ± 5%; OUT A = OUT B = AGND = DGND = 0 V; V_{IN} A = V_{IN} B = 10 V. Output amplifier AD712 except where stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	C Version[1] T_A = 25°C	C Version[1] T_A = T_{MIN}, T_{MAX}	B Version T_A = 25°C	B Version T_A = T_{MIN}, T_{MAX}	Units	Conditions/Comments
ACCURACY						
Resolution	0.375	0.375	0.375	0.375	dB	
Accuracy Relative to 0 dB Attenuation						Guaranteed Attenuation Ranges for Specified Step Sizes.
0.375 dB Steps:						
Accuracy ≤ ±0.17 dB	0 to 36	0 to 36	0 to 30	0 to 30	dB min	
Monotonic	0 to 54	0 to 54	0 to 48	0 to 48	dB min	
0.75 dB Steps:						
Accuracy ≤ ±0.35 dB	0 to 48	0 to 42	0 to 42	0 to 36	dB min	
Monotonic	0 to 72	0 to 66	0 to 72	0 to 60	dB min	
1.5 dB Steps:						
Accuracy ≤ ±0.7 dB	0 to 54	0 to 48	0 to 48	0 to 42	dB min	
Monotonic	Full Range	0 to 78	0 to 85.5	0 to 72	dB min	Full Range Is 0 to 88.5 dB.
3.0 dB Steps:						
Accuracy ≤ ±1.4 dB	0 to 66	0 to 54	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range	dB min	
6.0 dB Steps:						
Accuracy ≤ ±2.7 dB	0 to 72	0 to 60	0 to 60	0 to 60	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range	dB min	
Gain Error	±0.1	±0.15	±0.15	±0.2	dB max	Measured Using R_{FB} A, R_{FB} B. Both DAC Registers Loaded With All 0s.
Output Leakage Current OUT A, OUT B	±50	±400	±50	±400	nA max	
Input Resistance, V_{IN} A, V_{IN} B	9/15	9/15	9/15	9/15	kΩ min/max	Typically 12 kΩ.
Input Resistance Match	±1	±1	±2	±2	% max	
Feedback Resistance, R_{FB} A, R_{FB} B	9.3/15.7	9.3/15.7	9.3/15.7	9.3/15.7	kΩ min/max	
LOGIC INPUTS $\overline{CS}$, $\overline{WR}$, $\overline{DAC}$ A/DAC B, DB0–DB7						
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Leakage Current	±1	±10	±1	±10	μA max	
Input Capacitance[2]	10	10	10	10	pF max	
POWER REQUIREMENTS						
V_{DD} Range[3]	4.75/5.25	4.75/5.25	4.75/5.25	4.75/5.25	V min/max	For Specified Performance.
	2	2	2	2	mA max	Logic Inputs = V_{IL} or V_{IH}
	2	2	2	2	mA max	Logic Inputs = 0 V or V_{DD}

NOTES
[1]Temperature Range as follows: B, C Versions: −40°C to +85°C.
[2]Guaranteed by design, not production tested.
[3]The part will function with V_{DD} = 5 V ± 10% with degraded performance.
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +5 V ± 5%; OUT A = OUT B = AGND = DGND = 0 V; V_{IN} A = V_{IN} B = 10 V)

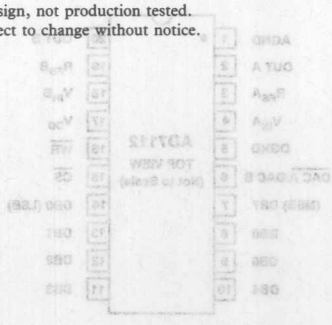
Parameter		T_A = +25°C	T_A = −40°C to +85°C	Units	Conditions/Comments
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CS}	0	0	ns min	See Figure 3.
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CH}	0	0	ns min	
DAC Select to $\overline{WR}$ Setup Time	t_{AS}	4	4	ns min	
DAC Select to $\overline{WR}$ Hold Time	t_{AH}	0	0	ns min	
Data Valid to $\overline{WR}$ Setup Time	t_{DS}	55	55	ns min	
Data Valid to $\overline{WR}$ Hold Time	t_{DH}	10	10	ns min	
$\overline{WR}$ Pulse Width	t_{WR}	53	53	ns min	

NOTES
[1]Timing specifications guaranteed by design not production tested. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%; OUT A = OUT B = AGND = DGND = 0 V; V_{IN} A = V_{IN} B = 10 V. Output amplifier AD712 except where noted.)

Parameter	T_A = +25°C	T_A = −40°C to +85°C	Units	Conditions/Comments
DC Supply Rejection Δ Gain/Δ V_{DD}	0.001	0.005	dB/% max	Δ V_{DD} = ± 5%. Input Code = 00000000
Digital-to-Analog Glitch Impulse	10	10	nV s typ	Measured with AD843 as output amplifier for input code transition 10000000 to 00000000
Output Capacitance, $C_{OUT\,A}$, $C_{OUT\,B}$	50	50	pF max	
AC Feedthrough				
V_{IN} A to OUT A	−94	−90	dB max	V_{IN} A, V_{IN} B = 6 V rms at 1 kHz. DAC Registers loaded with all 1s.
V_{IN} B to OUT B	−94	−90	dB max	
Channel-to-Channel Isolation				
V_{IN} A to OUT B	−87	−87	dB typ	V_{IN} A = 6 V rms at 10 kHz sine wave, V_{IN} B = 0 V. DAC Registers loaded with all 0s.
V_{IN} B to OUT A	−87	−87	dB typ	V_{IN} B = 6 V rms at 10 kHz sine wave, V_{IN} A = 0 V. DAC Registers loaded with all 0s.
Digital Feedthrough	1	1	nV s typ	Measured with input code transitions of all 0s to all 1s.
Output Noise Voltage Density (30 Hz to 50 kHz)	15	15	nV/$\sqrt{Hz}$ typ	Measured between R_{FB} A and OUT A or between R_{FB} B and OUT B.
Total Harmonic Distortion	−91	−91	dB typ	V_{IN} A = V_{IN} B = 6 V rms at 1 kHz. DAC Registers loaded with all 0s.

NOTES
[1]Guaranteed by design, not production tested.
Specifications subject to change without notice.



ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND or DGND . . . . . −0.3 V, +7 V
AGND to DGND . . . . . −0.3 V, V_{DD} + 0.3 V
Digital Inputs to DGND . . . . . −0.3 V, V_{DD} + 0.3 V
OUT A, OUT B to AGND . . . . . −0.3 V, V_{DD} + 0.3 V
V_{IN} A, V_{IN} B to AGND . . . . . ±25 V
V_{RFB} A, V_{RFB} B to AGND . . . . . ±25 V
Operating Temperature Range
All Versions . . . . . −40°C to +85°C
Junction Temperature . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Power Dissipation, DIP . . . . . 1 W
θ_{JA}, Thermal Impedance . . . . . 102°C/W
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation, SOIC . . . . . 1 W
θ_{JA}, Thermal Impedance . . . . . 75°C/W
Lead Temperature (Soldering)
Vapor Phase (60 secs) . . . . . 215°C
Infrared (15 secs) . . . . . 220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although devices feature proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper precautions are recommended to avoid any performance degradation or loss of functionality.

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent codes.

MONOTONICITY: The device is monotonic if the analog output decreases or remains constant as the digital code increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when all digital inputs are high.

OUTPUT CAPACITANCE: Capacitance from OUT A or OUT B to ground.

GAIN ERROR: Gain error results from a mismatch between R_{FB} (the feedback resistance) and the R–2R ladder resistance. Its effect in a LOGDAC is to produce a constant additive attenuation error in dB over the whole range of the DAC.

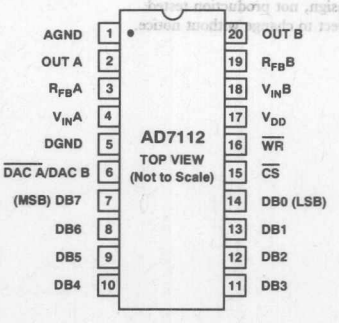
ACCURACY: The difference (measured in dB) between the ideal transfer function as listed in Table I and the actual transfer function as measured with the device.

DIGITAL-TO-ANALOG GLITCH IMPULSE: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-s or nV-s depending on whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{IN} = AGND.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	AGND	Analog Ground.
2	OUT A	Current Output Terminal of DAC A.
3	R_{FB} A	Feedback Resistor for DAC A.
4	V_{IN} A	Reference Input to DAC A
5	DGND	Digital Ground.
6	$\overline{\text{DAC A}}$ / DAC B	Selects Which DAC Can Accept Data from Input Port.
7–14	DB7–DB0	8 Data Inputs.
15	$\overline{\text{CS}}$	Chip Select Input, Active Low.
16	$\overline{\text{WR}}$	Write Input, Active Low.
17	V_{DD}	Power Supply Input 5 V ± 5%.
18	V_{IN} B	Reference Input to DAC B.
19	R_{FB} B	Feedback Resistor for DAC B.
20	OUT B	Current Output Terminal of DAC B.

PIN CONFIGURATION DIP/SOIC



ORDERING GUIDE

Model	Temperature Range	Specified Accuracy Range	Package Option*
AD7112BN	−40°C to +85°C	0 dB to 60 dB	N-20
AD7112CN	−40°C to +85°C	0 dB to 72 dB	N-20
AD7112BR	−40°C to +85°C	0 dB to 60 dB	R-20
AD7112CR	−40°C to +85°C	0 dB to 72 dB	R-20

*N = Plastic DIP; R = SOIC. For outline information see Package Information section.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7112 consists of a dual 17-bit R–2R CMOS multiplying D/A converter with extensive digital logic. Figure 1 shows a simplified circuit of the D/A converter section of the AD7112. The logic translates the 8-bit binary input into a 17-bit word which is used to drive the D/A converter. Figure 2 shows a typical circuit configuration for the AD7112.

The transfer function for the circuit of Figure 2 is given by:

$$V_O = -V_{IN} \times 10\ exp - \frac{0.375\ N}{20}$$

or

$$\left| \frac{V_O}{V_{IN}} \right| dB = -0.375\ N$$

where 0.375 is the step size (resolution) in dB and N is the input code in decimal for values 0 to 239. For $240 \leq N \leq 255$ the output is zero. Table I gives the output attenuation relative to 0 dB for all possible input codes.

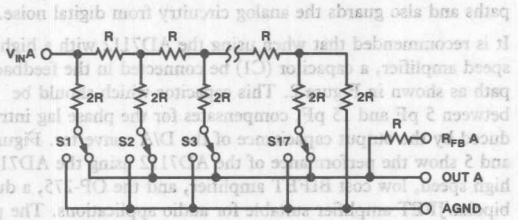
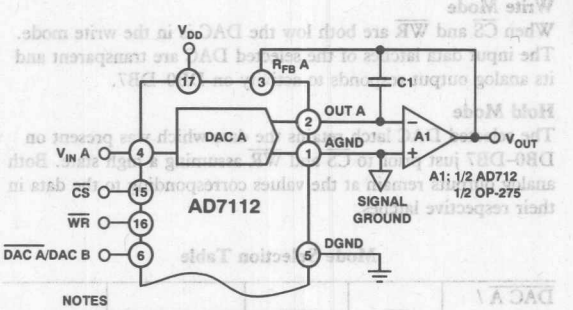


Figure 1. Simplified D/A Circuit of 1/2 AD7112

Figures 16 and 17 give a pictorial representation of the specified accuracy and monotonic ranges for all grades of the AD7112. High attenuation levels are specified with less accuracy than low attenuation levels. The range of monotonic behavior depends upon the attenuation step size used. To achieve monotonic operation over the entire 88.5 dB range, it is necessary to select input codes so that the attenuation step size at any point is consistent with the step size guaranteed for monotonic operation at that point.



NOTES
1. ONLY ONE DAC IS SHOWN FOR CLARITY.
2. DATA INPUT CONNECTIONS ARE OMITTED.
3. C1 PHASE COMPENSATION (5–15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

Figure 2. Typical Circuit Configuration

Table I. Ideal Attenuation in dB vs. Input Code

D3–D0 / D7–D4	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0.000	0.375	0.750	1.125	1.500	1.875	2.250	2.625	3.000	3.375	3.750	4.125	4.500	4.875	5.250	5.625
0001	6.000	6.375	6.750	7.125	7.500	7.875	8.250	8.625	9.000	9.375	9.750	10.125	10.500	10.875	11.250	11.625
0010	12.000	12.375	12.750	13.125	13.500	13.875	14.250	14.625	15.000	15.375	15.750	16.125	16.500	16.875	17.250	17.625
0011	18.000	18.375	18.750	19.125	19.500	19.875	20.250	20.625	21.000	21.375	21.750	22.125	22.500	22.875	23.250	23.625
0100	24.000	24.375	24.750	25.125	25.500	25.875	26.250	26.625	27.000	27.375	27.750	28.125	28.500	28.875	29.250	29.625
0101	30.000	30.375	30.750	31.125	31.500	31.875	32.250	32.625	33.000	33.375	33.750	34.125	34.500	34.875	35.250	35.625
0110	36.000	36.375	36.750	37.125	37.500	37.875	38.250	38.625	39.000	39.375	39.750	40.125	40.500	40.875	41.250	41.625
0111	42.000	42.375	42.750	43.125	43.500	43.875	44.250	44.625	45.000	45.375	45.750	46.125	46.500	46.875	47.250	47.625
1000	48.000	48.375	48.750	49.125	49.500	49.875	50.250	50.625	51.000	51.375	51.750	52.125	52.500	52.875	53.250	53.625
1001	54.000	54.375	54.750	55.125	55.500	55.875	56.250	56.625	57.000	57.375	57.750	58.125	58.500	58.875	59.250	59.625
1010	60.000	60.375	60.750	61.125	61.500	61.875	62.250	62.625	63.000	63.375	63.750	64.125	64.500	64.875	65.250	65.625
1011	66.000	66.375	66.750	67.125	67.500	67.875	68.250	68.625	69.000	69.375	69.750	70.125	70.500	70.875	71.250	71.625
1100	72.000	72.375	72.750	73.125	73.500	73.875	74.250	74.625	75.000	75.375	75.750	76.125	76.500	76.875	77.250	77.625
1101	78.000	78.375	78.750	79.125	79.500	79.875	80.250	80.625	81.000	81.375	81.750	82.125	82.500	82.875	83.250	83.625
1110	84.000	84.375	84.750	85.125	85.500	85.875	86.250	86.625	87.000	87.375	87.750	88.125	88.500	88.875	89.250	89.625
1111	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE

Both DAC latches share a common 8-bit port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

Mode Selection

Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See the Mode Selection Table below.

Write Mode

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low the DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

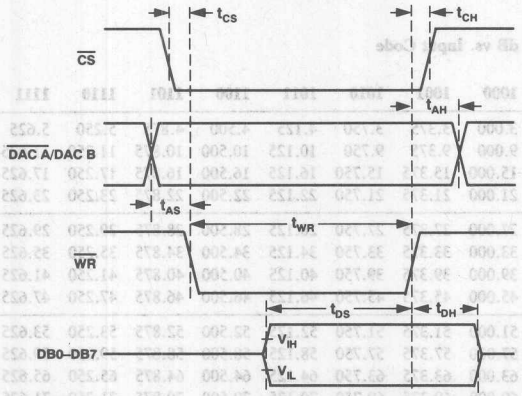
Hold Mode

The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{\text{CS}}$ and $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Mode Selection Table

$\overline{\text{DAC A}}$ / DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State, V_{IL}; H = High State, V_{IH}; X = Don't Care.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}. $t_R = t_F = 20ns$.
2. CONTROL TIMING MEASUREMENT REFERENCE LEVEL = $(V_{IH} + V_{IL}) / 2$

Figure 3. Write Cycle Timing Diagram

gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Circuit layout is most important if the optimum performance of the AD7112 is to be achieved. Most application problems stem from either poor layout, grounding errors, or inappropriate choice of amplifier. Ensure that the layout of the printed circuit board has the digital and analog lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Establish a single point analog ground (star ground) separate from the logic system ground. Place this ground as close as possible to the AD7112. Connect all analog grounds to this star ground, and also connect the AD7112 DGND to this ground. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential for low noise and high performance of these converters, therefore the foil width of these tracks should be as wide as possible. The use of ground planes is recommended as this minimizes impedance paths and also guards the analog circuitry from digital noise.

It is recommended that when using the AD7112 with a high speed amplifier, a capacitor (C1) be connected in the feedback path as shown in Figure 2. This capacitor which should be between 5 pF and 15 pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 4 and 5 show the performance of the AD7112 using the AD712, a high speed, low cost BIFET amplifier, and the OP-275, a dual bipolar/JFET amplifier suitable for audio applications. The performance with and without the compensation capacitor is shown in both cases. For operation beyond 250 kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figure 7. In circuits where C1 is not included, the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7112.

Feedthrough and accuracy are sensitive to output leakage currents effects. For this reason it is recommended that the operating temperature of the AD7112 be kept as close to 25°C as is practically possible, particularly where the devices performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 11.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7112 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

STATIC ACCURACY PERFORMANCE

The D/A converter section of the AD7112 consists of a 17-bit R–2R type converter. To obtain optimum static performance at this level of resolution it is necessary to pay great attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to current flowing in the feedback resistor R_{FB}. It is recommended that amplifiers with input bias currents of less than 10 nA be used (e.g., AD712) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7112 output impedance) varies as a function of the attenuation level. This has the effect of varying the noise gain of the amplifier thus creating a varying error due to amplifier offset voltage. It is recommended that an amplifier with less than 50 μV of input offset be used (such as the AD712 or ADOP-07) in dc applications. Amplifiers with a large input offset voltage may cause audible thumps in audio applications due to dc output changes. The AD7112 accuracy is specified and tested using only the internal feedback resistor. Any Gain error (i.e., mismatch of R_{FB} to the R–2R ladder) that may exist in the AD7112 D/A converter circuit results in a constant attenuation error over the whole range. The AD7112 accuracy is specified relative to 0 dB attenuation, hence gain trim resistors can be used to adjust $V_{OUT} = V_{IN}$ precisely (i.e., 0 dB attenuation) with input code 00000000. For further information on gain error refer to the "CMOS DAC Application Guide" which is available from Analog Devices, Publication Number G872b–8–1/89.

3

TYPICAL PERFORMANCE CHARACTERISTICS

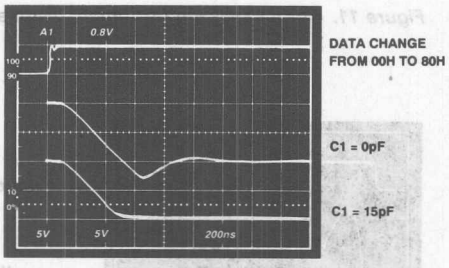


Figure 4. Response of AD7112 with AD712

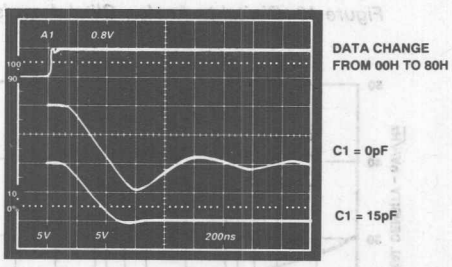


Figure 5. Response of AD7112 with OP-275

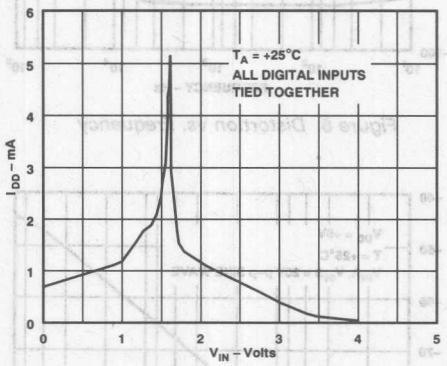


Figure 6. Supply Current vs. Logic Input Level

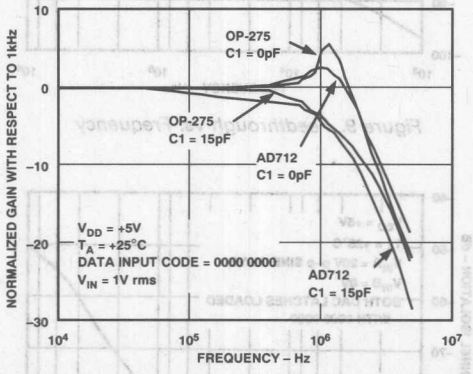


Figure 7. Frequency Response with AD712 and OP-275

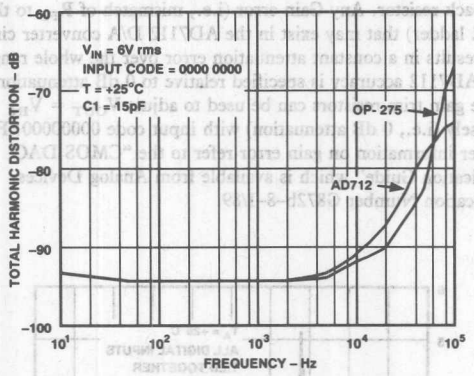


Figure 8. Distortion vs. Frequency

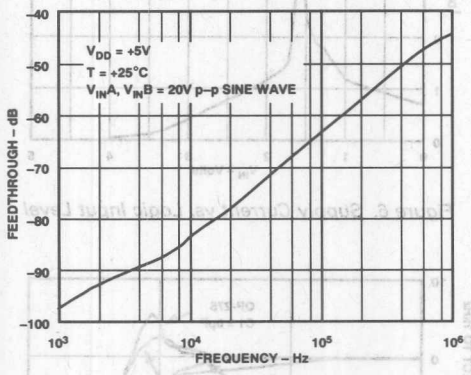


Figure 9. Feedthrough vs. Frequency

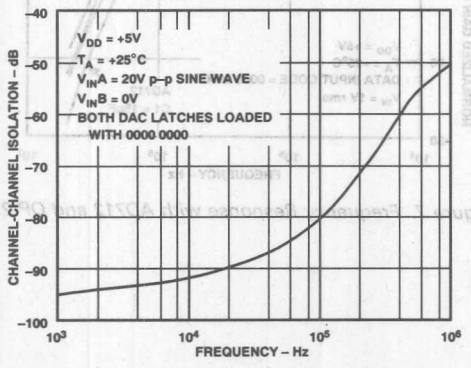


Figure 10. Channel-to-Channel Isolation vs. Frequency

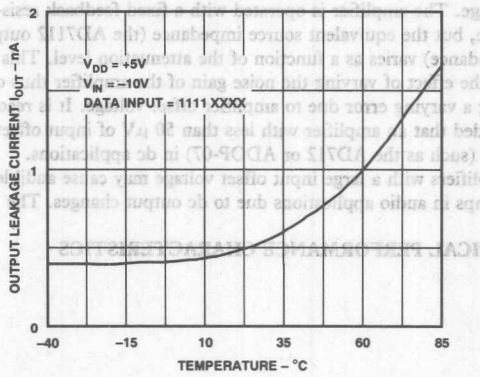


Figure 11. Output Leakage Current vs. Temperature

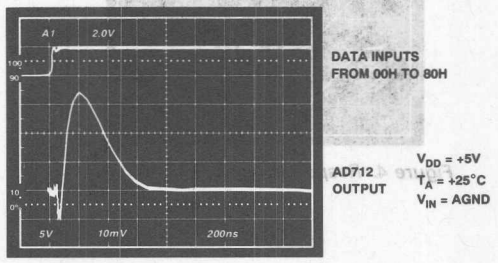


Figure 12. Digital-to-Analog Glitch Impulse

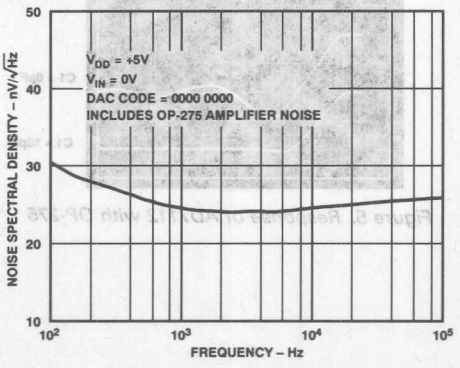


Figure 13. Noise Spectral Density vs. Frequency

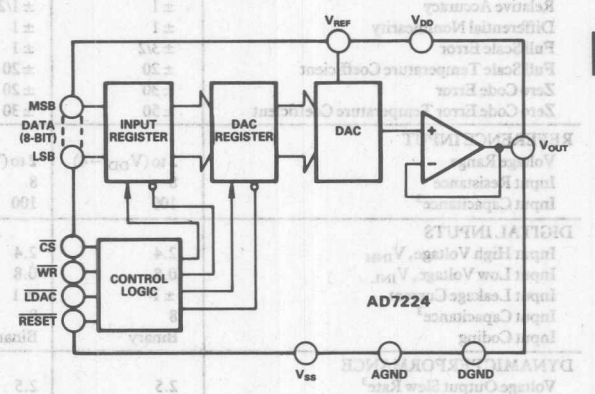
LC²MOS 8-Bit DAC with Output Amplifier

AD7224

FEATURES

- 8-Bit CMOS DAC with Output Amplifier
- Operates with Single or Dual Supplies
- Low Total Unadjusted Error:
  - Less than 1 LSB Over Temperature
- Extended Temperature Range Operation
- µP-Compatible with Double Buffered Input
- Standard 18-Pin DIPs and 20-Terminal Surface Mount Package and SOIC Package

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7224 is a precision 8-bit, voltage-output, digital-to-analog converter with output amplifier and double buffered interface logic on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The double buffered interface logic consists of two 8-bit registers– an input register and a DAC register. Only the data held in the DAC register determines the analog output of the converter. The double buffering allows simultaneous update in a system containing multiple AD7224's. Both registers may be made transparent under control of three external lines, $\overline{CS}$, $\overline{WR}$ and $\overline{LDAC}$. With both registers transparent, the $\overline{RESET}$ line functions like a zero override; a useful function for system calibration cycles. All logic inputs are TTL and CMOS (5V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V when using dual supplies. The part is also specified for single supply operation using a reference of +10V. The output amplifier is capable of developing +10V across a 2kΩ load.

The AD7224 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. DAC and Amplifier on CMOS Chip
   The single-chip design of the 8-bit DAC and output amplifier is inherently more reliable than multi-chip designs. CMOS fabrication means low power consumption (35mW typical with single supply).
2. Low Total Unadjusted Error
   The fabrication of the AD7224 on Analog Devices Linear Compatible CMOS (LC²MOS) process, coupled with a novel DAC switch-pair arrangement, enables an excellent total unadjusted error of less than 1LSB over the full operating temperature range.
3. Single or Dual Supply Operation
   The voltage-mode configuration of the AD7224 allows operation from a single power supply rail. The part can also be operated with dual supplies giving enhanced performance for some parameters.
4. Versatile Interface Logic
   The high speed logic allows direct interfacing to most microprocessors. Additionally, the double buffered interface enables simultaneous update of the AD7224 in multiple DAC systems. The part also features a zero override function.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter	K, B, T Versions[2]	L, C, U Versions	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±1	LSB max	V_{DD} = +15V ± 5%, V_{REF} = +10V
Relative Accuracy	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Full Scale Error	±3/2	±1	LSB max	
Full Scale Temperature Coefficient	±20	±20	ppm/°C max	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error	±30	±20	mV max	
Zero Code Error Temperature Coefficient	±50	±30	µV/°C typ	
REFERENCE INPUT				
Voltage Range	2 to (V_{DD} −4)	2 to (V_{DD} −4)	V_{min} to V_{max}	
Input Resistance	8	8	kΩ min	
Input Capacitance[3]	100	100	pF max	Occurs when DAC is loaded with all 1's.
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[3]	2.5	2.5	V/µs min	
Voltage Output Settling Time[3]				
Positive Full Scale Change	5	5	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Negative Full Scale Change	7	7	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Digital Feedthrough	50	50	nV secs typ	V_{REF} = 0V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES				
V_{DD} Range	11.4/16.5	11.4/16.5	V_{min}/V_{max}	For Specified Performance
V_{SS} Range	4.5/5.5	4.5/5.5	V_{min}/V_{max}	For Specified Performance
I_{DD}				
@25°C	4	4	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{min} to T_{max}	6	6	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}				
@25°C	3	3	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{min} to T_{max}	5	5	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3,4]				
t_1				
@25°C	90	90	ns min	Chip Select/Load DAC Pulse Width
T_{min} to T_{max}	90	90	ns min	
t_2				
@25°C	90	90	ns min	Write/Reset Pulse Width
T_{min} to T_{max}	90	90	ns min	
t_3				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Setup Time
T_{min} to T_{max}	0	0	ns min	
t_4				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Hold Time
T_{min} to T_{max}	0	0	ns min	
t_5				
@25°C	90	90	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	90	90	ns min	
t_6				
@25°C	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions: −40°C to +85°C
B, C Versions: −40°C to +85°C
T, U Versions: −55°C to +125°C
[3]Sample Tested at 25°C by Product Assurance to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.
Specifications subject to change without notice.

SINGLE SUPPLY (V_{DD} = +15V ± 5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V[1] unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B, T Versions[2]	L, C, U Versions	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT				
Input Resistance	8	8	kΩ min	
Input Capacitance[3]	100	100	pF max	Occurs when DAC is loaded with all 1's.
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[4]	2	2	V/μs min	
Voltage Output Settling Time[4]				
Positive Full Scale Change	5	5	μs max	Settling Time to ± 1/2LSB
Negative Full Scale Change	20	20	μs max	Settling Time to ± 1/2LSB
Digital Feedthrough[3]	50	50	nV secs typ	V_{REF} = 0V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES				
V_{DD} Range	14.25/15.75	14.25/15.75	V_{min}/V_{max}	For Specified Performance
I_{DD}				
@25°C	4	4	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{min} to T_{max}	6	6	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3,4]				
t_1				
@25°C	90	90	ns min	Chip Select/Load DAC Pulse Width
T_{min} to T_{max}	90	90	ns min	
t_2				
@25°C	90	90	ns min	Write/Reset Pulse Width
T_{min} to T_{max}	90	90	ns min	
t_3				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Setup Time
T_{min} to T_{max}	0	0	ns min	
t_4				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Hold Time
T_{min} to T_{max}	0	0	ns min	
t_5				
@25°C	90	90	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	90	90	ns min	
t_6				
@25°C	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions: −40°C to +85°C
B, C Versions: −40°C to +85°C
T, U Versions: −55°C to +125°C
[3]Sample Tested at 25°C by Product Assurance to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND	−0.3V, +17V
V_{DD} to DGND	−0.3V, +17V
V_{DD} to V_{SS}	−0.3V, +24V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD} +0.3V
V_{OUT} to AGND[1]	V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C	450mW
Derates above 75°C by	6mW/°C
Operating Temperature	
Commercial (K, L Versions)	−40°C to +85°C
Industrial (B, C Versions)	−40°C to +85°C
Extended (T, U Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

NOTES

[1]The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7224KN	−40°C to +85°C	±2 max	N-18
AD7224LN	−40°C to +85°C	±1 max	N-18
AD7224KP	−40°C to +85°C	±2 max	P-20A
AD7224LP	−40°C to +85°C	±1 max	P-20A
AD7224KR-1	−40°C to +85°C	±2 max	R-20
AD7224LR-1	−40°C to +85°C	±1 max	R-20
AD7224KR-18	−40°C to +85°C	±2 max	R-18
AD7224LR-18	−40°C to +85°C	±1 max	R-18
AD7224BQ	−40°C to +85°C	±2 max	Q-18
AD7224CQ	−40°C to +85°C	±1 max	Q-18
AD7224TQ	−55°C to +125°C	±2 max	Q-18
AD7224UQ	−55°C to +125°C	±1 max	Q-18
AD7224TE	−55°C to +125°C	±2 max	E-20A
AD7224UE	−55°C to +125°C	±1 max	E-20A

NOTES

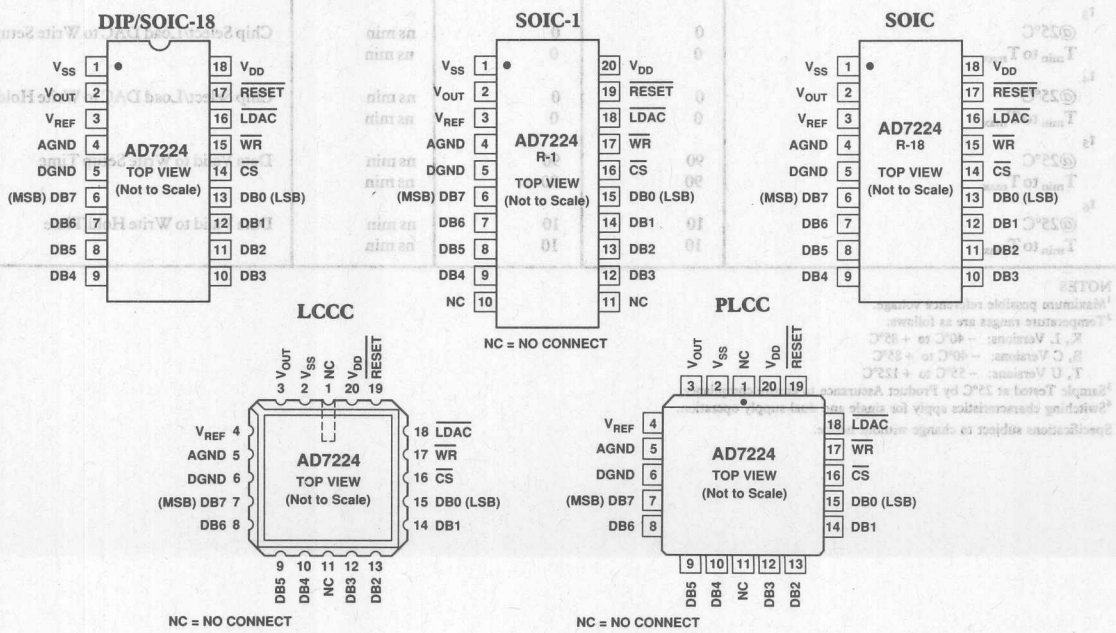
[1]To order MIL-STD-883 processed parts, add /883B to part number. Contact your local sales office for military data sheet.

[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded; Q = Cerdip; R = SOIC. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS



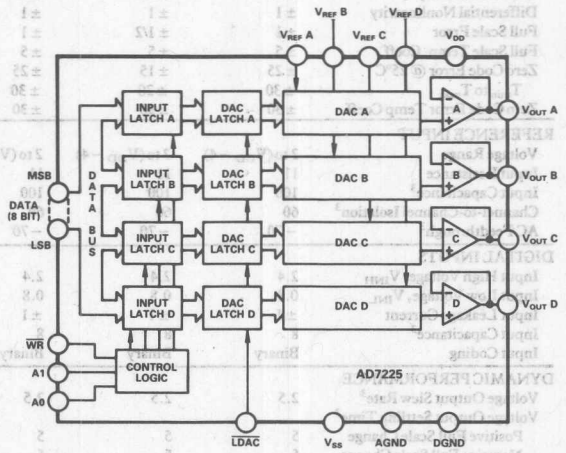
LC²MOS Quad 8-Bit DAC with Separate Reference Inputs

AD7225

FEATURES

- Four 8-Bit DACs with Output Amplifiers
- Separate Reference Input for Each DAC
- µP Compatible with Double-Buffered Inputs
- Simultaneous Update of All Four Outputs
- Operates with Single or Dual Supplies
- Extended Temperature Range Operation
- No User Trims Required
- Skinny 24-Pin DIP, SOIC and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7225 contains four 8-bit voltage output digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. Each D/A converter has a separate reference input terminal. No external trims are required to achieve full specified performance for the part.

The double-buffered interface logic consists of two 8-bit registers per channel–an input register and a DAC register. Control inputs A0 and A1 determine which input register is loaded when $\overline{WR}$ goes low. Only the data held in the DAC registers determines the analog outputs of the converters. The double-buffering allows simultaneous update of all four outputs under control of $\overline{LDAC}$. All logic inputs are TTL and CMOS (5V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V when using dual supplies. The part is also specified for single supply operation using a reference of +10V. Each output buffer amplifier is capable of developing +10V across a 2kΩ load.

The AD7225 is fabricated on an all ion-implanted high-speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to integrate high-speed digital logic circuits and precision analog circuitry on the same chip.

PRODUCT HIGHLIGHTS

1. DACs and Amplifiers on CMOS Chip
   The single-chip design of four 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one end of the package and all digital inputs at the other.
2. Single or Dual Supply Operation
   The voltage-mode configuration of the AD7225 allows single supply operation. The part can also be operated with dual supplies giving enhanced performance for some parameters.
3. Versatile Interface Logic
   The AD7225 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. The double-buffered interface allows simultaneous update of the four outputs.
4. Separate Reference Input for Each DAC
   The AD7225 offers great flexibility in dealing with input signals with a separate reference input provided for each DAC and each reference having variable input voltage capability.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter	K, B Versions[2]	L, C Versions[2]	T Version	U Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	V_{DD} = +15V ± 5%, V_{REF} = +10V
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full Scale Error	±1	±1/2	±1	±1/2	LSB max	
Full Scale Temp. Coeff.	±5	±5	±5	±5	ppm/°C typ	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error @ 25°C	±25	±15	±25	±15	mV max	
T_{min} to T_{max}	±30	±20	±30	±20	mV max	
Zero Code Error Temp Coeff.	±30	±30	±30	±30	µV/°C typ	
REFERENCE INPUT						
Voltage Range	2 to (V_{DD} − 4)	2 to (V_{DD} − 4)	2 to (V_{DD} − 4)	2 to (V_{DD} − 4)	V_{min} to V_{max}	
Input Resistance	11	11	11	11	kΩ min	
Input Capacitance[3]	100	100	100	100	pF max	Occurs when each DAC is loaded with all 1's.
Channel-to-Channel Isolation[3]	60	60	60	60	dB min	V_{REF} = 10V p-p Sine Wave @ 10kHz
AC Feedthrough[3]	−70	−70	−70	−70	dB max	V_{REF} = 10V p-p Sine Wave @ 10kHz
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate[3]	2.5	2.5	2.5	2.5	V/µs min	
Voltage Output Settling Time[3]						
Positive Full Scale Change	5	5	5	5	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Negative Full Scale Change	5	5	5	5	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Digital Feedthrough[3]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Digital Crosstalk[3]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES						
V_{DD} Range	11.4/16.5	11.4/16.5	11.4/16.5	11.4/16.5	V_{min}/V_{max}	For Specified Performance
I_{DD}	10	10	12	12	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}	9	9	10	10	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3,4]						
t_1						
@ 25°C	95	95	95	95	ns min	Write Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	
t_2						
@ 25°C	0	0	0	0	ns min	Address to Write Setup Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_3						
@ 25°C	0	0	0	0	ns min	Address to Write Hold Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_4						
@ 25°C	70	70	70	70	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	90	90	90	90	ns min	
t_5						
@ 25°C	10	10	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	10	10	ns min	
t_6						
@ 25°C	95	95	95	95	ns min	Load DAC Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions: −40°C to +85°C
B, C Versions: −40°C to +85°C
T, U Versions: −55°C to +125°C
[3]Sample Tested at 25°C to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.
Specifications subject to change without notice.

SINGLE SUPPLY (V_{DD} = +15V ± 5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V[1] unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	K, B Versions[2]	L, C Versions[2]	T Version	U Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	
Differential Nonlinearity[3]	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT						
Input Resistance	11	11	11	11	kΩ min	
Input Capacitance[4]	100	100	100	100	pF max	Occurs when each DAC is loaded with all 1's.
Channel-to-Channel Isolation[3,4]	60	60	60	60	dB min	V_{REF} = 10V p-p Sine Wave @ 10kHz
AC Feedthrough[3,4]	−70	−70	−70	−70	dB max	V_{REF} = 10V p-p Sine Wave @ 10kHz
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[4]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate[4]	2	2	2	2	V/μs min	
Voltage Output Settling Time[4]						
Positive Full Scale Change	5	5	5	5	μs max	Settling Time to ± 1/2LSB
Negative Full Scale Change	7	7	7	7	μs max	Settling Time to ± 1/2LSB
Digital Feedthrough[3,4]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Digital Crosstalk[3,4]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES						
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	V_{min}/V_{max}	For Specified Performance
I_{DD}	10	10	12	12	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[4]						
t_1						
@ 25°C	95	95	95	95	ns min	Write Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	
t_2						
@ 25°C	0	0	0	0	ns min	Address to Write Setup Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_3						
@ 25°C	0	0	0	0	ns min	Address to Write Hold Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_4						
@ 25°C	70	70	70	70	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	90	90	90	90	ns min	
t_5						
@ 25°C	10	10	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	10	10	ns min	
t_6						
@ 25°C	95	95	95	95	ns min	Load DAC Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions: −40°C to +85°C
B, C Versions: −40°C to +85°C
T, U Versions: −55°C to +125°C
[3]Sample Tested at 25°C to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.
Specifications subject to change without notice.

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error	Package Option[2]
AD7225KN	−40°C to +85°C	±2 LSB	N-24
AD7225LN	−40°C to +85°C	±1 LSB	N-24
AD7225KP	−40°C to +85°C	±2 LSB	P-28A
AD7225LP	−40°C to +85°C	±1 LSB	P-28A
AD7225KR	−40°C to +85°C	±2 LSB	R-24
AD7225LR	−40°C to +85°C	±1 LSB	R-24
AD7225BQ	−40°C to +85°C	±2 LSB	Q-24
AD7225CQ	−40°C to +85°C	±1 LSB	Q-24
AD7225TQ	−55°C to +125°C	±2 LSB	Q-24
AD7225UQ	−55°C to +125°C	±1 LSB	Q-24
AD7225TE	−55°C to +125°C	±2 LSB	E-28A
AD7225UE	−55°C to +125°C	±1 LSB	E-28A

NOTES
[1]To order MIL-STD-883 processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND	−0.3V, +17V
V_{DD} to DGND	−0.3V, +17V
V_{DD} to V_{SS}	−0.3V, +24V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD} +0.3V
V_{OUT} to AGND[1]	V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C	500mW
Derates above 75°C by	2.0mW/°C
Operating Temperature	
Commercial (K, L Versions)	−40°C to +85°C
Industrial (B, C Versions)	−40°C to +85°C
Extended (T, U Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

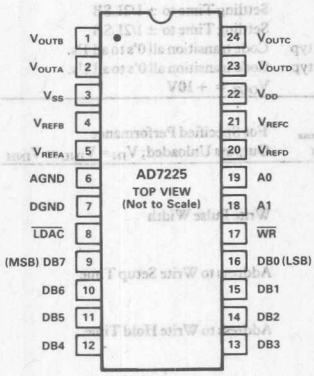
[1]Outputs may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit current for a short to AGND or V_{SS} is 50mA.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

DIP and SOIC



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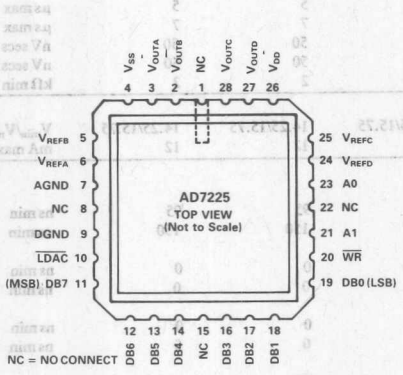
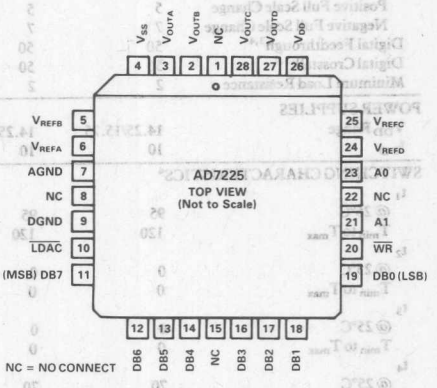


PLCC



TERMINOLOGY

TOTAL UNADJUSTED ERROR

Total Unadjusted Error is a comprehensive specification which includes full scale error, relative accuracy, and zero code error. Maximum output voltage is V_{REF} − 1LSB (ideal), where 1 LSB (ideal) is $V_{REF}/256$. The LSB size will vary over the V_{REF} range. Hence the zero code error will, relative to the LSB size, increase as V_{REF} decreases. Accordingly, the total unadjusted error, which includes the zero code error, will also vary in terms of LSB's over the V_{REF} range. As a result, total unadjusted error is specified for a fixed reference voltage of +10V.

RELATIVE ACCURACY

Relative Accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after allowing for zero code error and full scale error and is normally expressed in LSB's or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

DIGITAL FEEDTHROUGH

Digital Feedthrough is the glitch impulse transferred to the output of the DAC due to a change in its digital input code. It is specified in nV secs and is measured at V_{REF} = 0V.

DIGITAL CROSSTALK

Digital Crosstalk is the glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter. It is specified in nV secs and is measured at V_{REF} = 0V.

AC FEEDTHROUGH

AC Feedthrough is the proportion of reference input signal which appears at the output of a converter when that DAC is loaded with all 0's.

CHANNEL-TO-CHANNEL ISOLATION

Channel-to-channel isolation is the proportion of input signal from the reference of one DAC (loaded with all 1's) which appears at the output of one of the other three DACs (loaded with all 0's). The figure given is the worst case for the three other outputs and is expressed as a ratio in dBs.

FULL SCALE ERROR

Full Scale Error is defined as:

Measured Value – Zero Code Error – Ideal Value

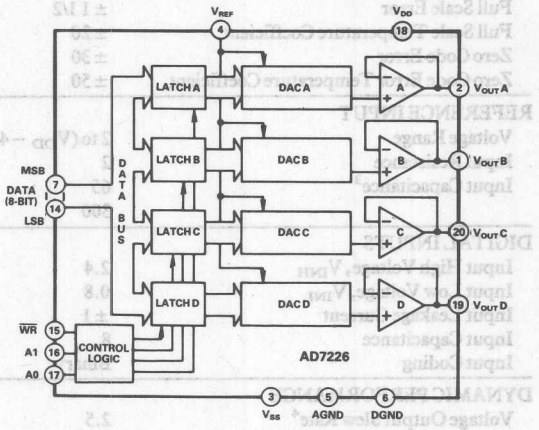
LC²MOS Quad 8-Bit D/A Converter

AD7226

FEATURES
- Four 8-Bit DACs with Output Amplifiers
- Skinny 20-Pin DIP, SOIC and 20-Terminal Surface Mount Packages
- Microprocessor Compatible
- TTL/CMOS Compatible
- No User Trims
- Extended Temperature Range Operation
- Single Supply Operation Possible

APPLICATIONS
- Process Control
- Automatic Test Equipment
- Automatic Calibration of Large System Parameters, e.g., Gain/Offset

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7226 contains four 8-bit voltage-output digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the four D/A converters. Data is transferred into one of these data latches through a common 8-bit TTL/CMOS (5V) compatible input port. Control inputs A0 and A1 determine which DAC is loaded when $\overline{WR}$ goes low. The control logic is speed-compatible with most 8-bit microprocessors.

Each D/A converter includes an output buffer amplifier capable of driving up to 5mA of output current. The amplifiers' offsets are laser-trimmed during manufacture, thereby eliminating any requirement for offset nulling.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V with dual supplies. The part is also specified for single supply operation at a reference of +10V.

The AD7226 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. DAC-to-DAC Matching
   Since all four DACs are fabricated on the same chip at the same time, precise matching and tracking between the DACs is inherent.
2. Single Supply Operation
   The voltage mode configuration of the DACs allows the AD7226 to be operated from a single power supply rail.
3. Microprocessor Compatibility
   The AD7226 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered.
4. Small Size
   Combining four DACs and four op-amps plus interface logic into 20-pin DIP or SOIC or a 20-terminal surface mount package allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all the analog inputs and outputs at one end of the package and all the digital inputs at the other.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7226—SPECIFICATIONS

Dual Supply

(V_{DD} = 11.4V to 16.5V; V_{SS} = −5V ±10%; AGND = DGND = 0V; V_{REF} = 2V to (V_{DD} −4V)[1] unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B, T Versions[2]	Units	Conditions/Comments
STATIC PERFORMANCE			
Resolution	8	Bits	
Total Unadjusted Error	±2	LSB max	V_{DD} = +15V ± 5%, V_{REF} = +10V
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Full Scale Error	±1 1/2	LSB max	
Full Scale Temperature Coefficient	±20	ppm/°C typ	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error	±30	mV max	
Zero Code Error Temperature Coefficient	±50	µV/°C typ	
REFERENCE INPUT			
Voltage Range	2 to (V_{DD} −4)	V_{MIN} to V_{MAX}	
Input Resistance	2	kΩ min	
Input Capacitance[3]	65	pF min	Occurs when each DAC loaded with all 0's.
	300	pF max	Occurs when each DAC loaded with all 1's.
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Leakage Current	±1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance	8	pF max	
Input Coding	Binary		
DYNAMIC PERFORMANCE			
Voltage Output Slew Rate[4]	2.5	V/µs min	
Voltage Output Settling Time[4]			
Positive Full Scale Change	5	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Negative Full Scale Change	7	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Digital Crosstalk	50	nV secs typ	
Minimum Load Resistance	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES			
V_{DD} Range	11.4/16.5	V_{MIN}/V_{MAX}	For Specified Performance
I_{DD}	13	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}.
I_{SS}	11	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}.
SWITCHING CHARACTERISTICS[4,5]			
Address to Write Setup Time, t_{AS}			
@25°C	0	ns min	
T_{MIN} to T_{MAX}	0	ns min	
Address to Write Hold Time, t_{AH}			
@25°C	10	ns min	
T_{MIN} to T_{MAX}	10	ns min	
Data Valid to Write Setup Time, t_{DS}			
@25°C	90	ns min	
T_{MIN} to T_{MAX}	100	ns min	
Data Valid to Write Hold Time, t_{DH}			
@25°C	10	ns min	
T_{MIN} to T_{MAX}	10	ns min	
Write Pulse Width, t_{WR}			
@25°C	150	ns min	
T_{MIN} to T_{MAX}	200	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K Version: −40°C to +85°C
B Version: −40°C to +85°C
T Version: −55°C to +125°C
[3]Guaranteed by design. Not production tested.
[4]Sample Tested at 25°C to ensure compliance.
[5]Switching Characteristics apply for both single and dual supply operation.

Specifications subject to change without notice.

Single Supply

(V_{DD} = +15V ± 5%; V_{SS} = AGND = DGND = 0V; V_{REF} +10V[1] unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B, T Versions[2]	Units	Conditions/Comments
STATIC PERFORMANCE			
Resolution	8	Bits	
Total Unadjusted Error	±2	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT			
Input Resistance	2	kΩ min	
Input Capacitance[3]	65	pF min	Occurs when each DAC loaded with all 0's.
	300	pF max	Occurs when each DAC loaded with all 1's.
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Leakage Current	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance	8	pF max	
Input Coding	Binary		
DYNAMIC PERFORMANCE			
Voltage Output Slew Rate[4]	2	V/μs min	
Voltage Output Settling Time[4]			
Positive Full Scale Change	5	μs max	Settling Time to ± 1/2LSB
Negative Full Scale Change	20	μs max	Settling Time to ± 1/2LSB
Digital Crosstalk	50	nV secs typ	
Minimum Load Resistance	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES			
V_{DD} Range	14.25 to 15.75	V_{MIN}/V_{MAX}	For Specified Performance
I_{DD}	13	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K Version: −40°C to +85°C
B Version: −40°C to +85°C
T Version: −55°C to +125°C
[3]Guaranteed by design. Not production tested.
[4]Sample Tested at 25°C to ensure compliance.
[5]Switching Characteristics apply for both single and dual supply operation.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND	−0.3V, +17V
V_{DD} to DGND	−0.3V, +17V
V_{SS} to AGND	−7V, V_{DD}
V_{SS} to DGND	−7V, V_{DD}
V_{DD} to V_{SS}	−0.3V, +24V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD}
V_{OUT} to AGND[1]	V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C	500mW
Derates above 75°C by	2.0mW/°C
Operating Temperature	
Commerical (K Version)	−40°C to +85°C
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

NOTES
[1]Outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error	Package Option[2]
AD7226KN	−40°C to +85°C	±2LSB	N-20
AD7226KP	−40°C to +85°C	±2LSB	P-20A
AD7226KR	−40°C to +85°C	±2LSB	R-20
AD7226BQ	−40°C to +85°C	±2LSB	Q-20
AD7226TQ	−55°C to +125°C	±2LSB	Q-20
AD7226TE	−55°C to +125°C	±2LSB	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962–87802.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

TERMINOLOGY

TOTAL UNADJUSTED ERROR
This is a comprehensive specification which includes full-scale error, relative accuracy and zero code error. Maximum output voltage is V_{REF} −1 LSB (ideal), where 1 LSB (ideal) is $V_{REF}/256$. The LSB size will vary over the V_{REF} range. Hence the zero code error will, relative to the LSB size, increase as V_{REF} decreases. Accordingly, the total unadjusted error, which includes the zero code error, will also vary in terms of LSB's over the V_{REF} range. As a result, total unadjusted error is specified for a fixed reference voltage of +10V.

RELATIVE ACCURACY
Relative Accuracy or end-point nonlinearity, is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after allowing for zero and full-scale error and is normally expressed in LSB's or as a percentage of full-scale reading.

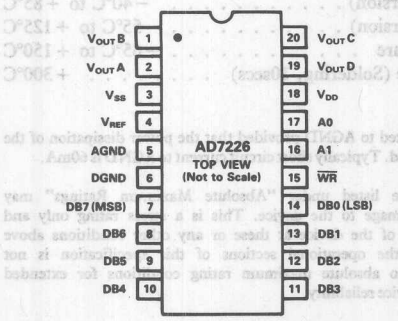
DIFFERENTIAL NONLINEARITY
Differential Nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

DIGITAL CROSSTALK
The glitch impulse transferred to the output of one converter due to a change in the digital input code to another of the converters. It is specified in nV secs and is measured at V_{REF}=0V.

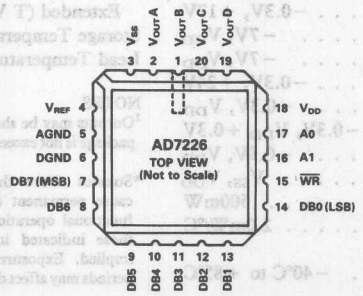
FULL-SCALE ERROR
Full-Scale Error is defined as:
Measured Value – Zero Code Error – Ideal Value.

PIN CONFIGURATIONS

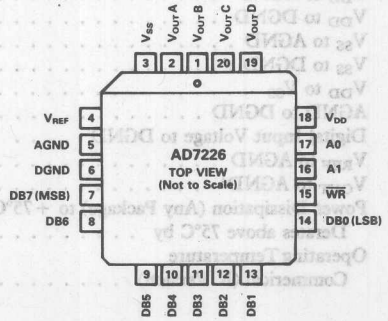
DIP, SOIC



LCCC



PLCC



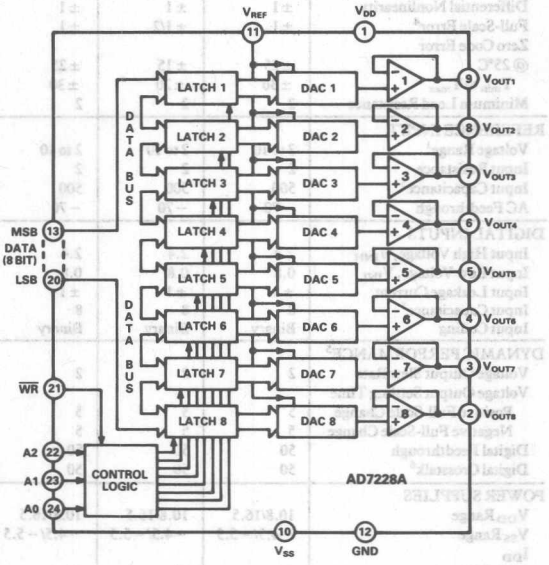
LC²MOS Octal 8-Bit DAC

AD7228A

FEATURES

Eight 8-Bit DACs with Output Amplifiers
Operates with Single or Dual Supplies
µP Compatible (95ns $\overline{WR}$ Pulse)
No User Trims Required
Skinny 24-Pin DIPs, SOIC, and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7228A contains eight 8-bit voltage-mode digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the eight D/A converters. Data is transferred into the data latches through a common 8-bit TTL/CMOS (5V) compatible input port. Address inputs A0, A1 and A2 determine which latch is loaded when $\overline{WR}$ goes low. The control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2 to +10V when using dual supplies. The part is also specified for single supply +15V operation using a reference of +10V and single supply +5V operation using a reference of +1.23V. Each output buffer amplifier is capable of developing +10V across a 2kΩ load.

The AD7228A is fabricated on an all ion-implanted, high-speed, Linear Compatible CMOS (LC²MOS) process which has been specifically developed to integrate high-speed digital logic circuits and precision analog circuits on the same chip.

PRODUCT HIGHLIGHTS

1. Eight DACs and Amplifiers in Small Package
   The single-chip design of eight 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one side of the package and all digital inputs at the other.
2. Single or Dual Supply Operation
   The voltage-mode configuration of the DACs allows single supply operation of the AD7228A. The part can also be operated with dual supplies giving enhanced performance for some parameters.
3. Microprocessor Compatibility
   The AD7228A has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered and speed compatible with most high-performance 8-bit microprocessors.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7228A—SPECIFICATIONS

DUAL SUPPLY (V_{DD} = 10.8V to 16.5V; V_{SS} = −5V ±10%; GND = 0V; V_{REF} = +2V to +10V[1]; R_L = 2kΩ, C_L = 100pF unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	AB Version[2]	AC Version	AT Version	AU Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	V_{DD} = +15V ± 10%, V_{REF} = +10V
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error[4]	±1	±1/2	±1	±1/2	LSB max	Typical tempco is 5ppm/°C with V_{REF} = +10V
Zero Code Error						
@ 25°C	±25	±15	±25	±15	mV max	Typical tempco is 30μV/°C
T_{min} to T_{max}	±30	±20	±30	±20	mV max	
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
REFERENCE INPUT						
Voltage Range[1]	2 to 10	2 to 10	2 to 10	2 to 10	V_{min} to V_{max}	
Input Resistance	2	2	2	2	kΩ min	
Input Capacitance[5]	500	500	500	500	pF max	Occurs when each DAC is loaded with all 1s.
AC Feedthrough	−70	−70	−70	−70	dB typ	V_{REF} = 8V p-p Sine Wave @ 10kHz/
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[5]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE[5]						
Voltage Output Slew Rate	2	2	2	2	V/μs min	
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	μs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Negative Full-Scale Change	5	5	5	5	μs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Digital Feedthrough	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. V_{REF} = 0V; $\overline{WR}$ = V_{DD}
Digital Crosstalk[6]	50	50	50	50	nVsecs typ	Code transition all 0s to all 1s. V_{REF} = +10V; $\overline{WR}$ = 0V
POWER SUPPLIES						
V_{DD} Range	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V_{min}/V_{max}	For Specified Performance
V_{SS} Range	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	V_{min}/V_{max}	For Specified Performance
I_{DD}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@25°C	16	16	16	16	mA max	
T_{min} to T_{max}	20	20	22	22	mA max	
I_{SS}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@25°C	14	14	14	14	mA max	
T_{min} to T_{max}	18	18	20	20	mA max	

SINGLE SUPPLY[7] (V_{DD} = +15V ± 10%, V_{SS} = GND = 0V; V_{REF} = +10V; R_L = 2kΩ, C_L = 100pF unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
REFERENCE INPUT						
Input Resistance	2	2	2	2	kΩ min	
Input Capacitance[5]	500	500	500	500	pF max	Occurs when each DAC is loaded with all 1s.
DIGITAL INPUTS	As per Dual Supply Specifications					
DYNAMIC PERFORMANCE[5]						
Voltage Output Slew Rate	2	2	2	2	V/μs min	
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	μs max	Settling Time to ± 1/2LSB
Negative Full-Scale Change	7	7	7	7	μs max	Settling Time to ± 1/2LSB
Digital Feedthrough	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. V_{REF} = 0V; $\overline{WR}$ = V_{DD}
Digital Crosstalk[6]	50	50	50	50	nVsecs typ	Code transition all 0s to all 1s. V_{REF} = +10V; $\overline{WR}$ = 0V.
POWER SUPPLIES						
V_{DD} Range	13.5/16.5	13.5/16.5	13.5/16.5	13.5/16.5	V_{min}/V_{max}	For Specified Performance
I_{DD}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@25°C	16	16	16	16	mA max	
T_{min} to T_{max}	20	20	22	22	mA max	

NOTES
[1]V_{OUT} must be less than V_{DD} by 3.5V to ensure correct operation.
[2]Temperature ranges are as follows:
AB, C Versions; −40°C to +85°C
AT, U Versions; −55°C to +125°C
[3]Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.
[4]Calculated after zero code error has been adjusted out.
[5]Sample tested at 25°C to ensure compliance.
[6]The glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter.
[7]Single +5V operation is also possible with degraded performance (see Figure 14).
Specifications subject to change without notice.

+5V SUPPLY OPERATION (V_{DD} = +5V ± 5%, V_{SS} = 0 to −5V ± 10%, GND = 0V, V_{REF} = +1.25V, R_L = 2kΩ, C_L = 100pF unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	AD7228AB	AD7228AC	AD7228AT	AD7228AU	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Relative Accuracy	±2	±2	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±4	±2	±4	±2	LSB max	
Zero Code Error						
@ 25°C	±30	±20	±30	±20	mV max	
T_{min} to T_{max}	±40	±30	±40	±30	mV max	
REFERENCE INPUT						
Reference Input Range	1.2	1.2	1.2	1.2	V min	
	1.3	1.3	1.3	1.3	V max	
Reference Input Resistance	2	2	2	2	kΩ min	
Reference Input Capacitance	500	500	500	500	pF max	
POWER REQUIREMENTS						
Positive Supply Range	4.75/5.25	4.75/5.25	4.75/5.25	4.75/5.25	V min/V max	For Specified Performance
Positive Supply Current						
@ 25°C	16	16	16	16	μA max	
T_{min} to T_{max}	20	20	22	22	μA max	
Negative Supply Current						
@ 25°C	14	14	14	14	μA max	
T_{min} to T_{max}	18	18	20	20	μA max	

NOTES
All other specifications as per Dual Supply Specifications except for negative full-scale settling-time when V_{SS} = 0V.
Specifications subject to change without notice.

SWITCHING CHARACTERISTICS[1, 2] (See Figures 1, 2; V_{DD} = +5V ± 5% or +10.8V to +16.5V; V_{SS} = 0V or −5V ± 10%)

Parameters	Limit at 25°C All Grades	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Limit at T_{min}, T_{max} (T, U Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	Address to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	Address to $\overline{WR}$ Hold Time
t_3	70	90	100	ns min	Data Valid to $\overline{WR}$ Setup Time
t_4	10	10	10	ns min	Data Valid to $\overline{WR}$ Hold Time
t_5	95	120	150	ns min	Write Pulse Width

NOTES
[1]Sample tested at 25°C to ensure compliance. All input rise and fall times measured from 10% to 90% of +5V, $t_R = t_F = 5$ns.
[2]Timing measurement reference level is $\frac{V_{INH} + V_{INL}}{2}$

INTERFACE LOGIC INFORMATION

Address lines A0, A1 and A2 select which DAC accepts data from the input port. Table I shows the selection table for the eight DACs with Figure 1 showing the input control logic. When the $\overline{WR}$ signal is low, the input latch of the selected DAC is transparent, and its output responds to activity on the data bus. The data is latched into the addressed DAC latch on the rising edge of $\overline{WR}$. While $\overline{WR}$ is high, the analog outputs remain at the value corresponding to the data held in their respective latches.

AD7228A Control Inputs				AD7228A
$\overline{WR}$	A2	A1	A0	Operation
H	X	X	X	No Operation Device Not Selected
L	L	L	L	DAC 1 Transparent
↑	L	L	L	DAC 1 Latched
L	L	L	H	DAC 2 Transparent
L	L	H	L	DAC 3 Transparent
L	L	H	H	DAC 4 Transparent
L	H	L	L	DAC 5 Transparent
L	H	L	H	DAC 6 Transparent
L	H	H	L	DAC 7 Transparent
L	H	H	H	DAC 8 Transparent

H = High State L = Low State X = Don't Care

Table I. AD7228A Truth Table

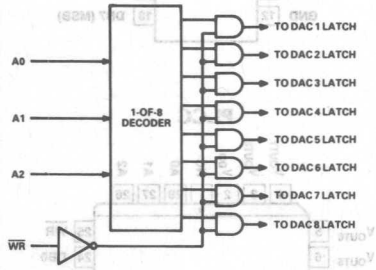
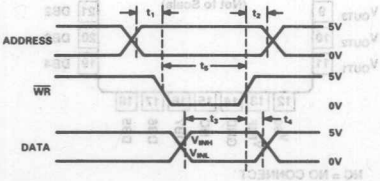


Figure 1. Input Control Logic



NOTE:
THE SELECTED INPUT LATCH IS TRANSPARENT WHILE $\overline{WR}$ IS LOW, THUS INVALID DATA DURING THIS TIME CAN CAUSE SPURIOUS OUTPUTS

Figure 2. Write Cycle Timing Diagram

V_{REF} to GND	−0.3V, V_{DD}
V_{OUT} to GND[1]	V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C	1000mW
Derates above 75°C by	2.0mW/°C
Operating Temperature	
Commercial	−40°C to +85°C
Industrial	−40°C to +85°C
Extended	−55°C to +125°C

that the power dissipation of the package is not exceeded. Typical short circuit current for a short to GND or V_{SS} is 50mA.

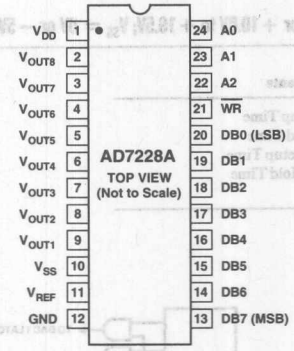
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

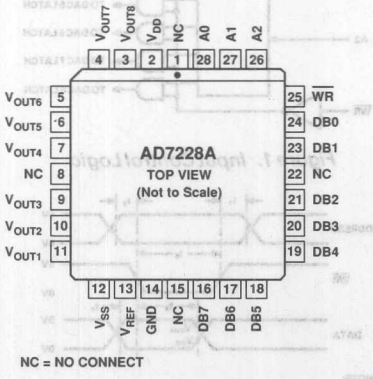
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

PIN CONFIGURATIONS

DIP, SOIC



PLCC



NC = NO CONNECT

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7228ABN	−40°C to +85°C	±2 max	N-24
AD7228ACN	−40°C to +85°C	±1 max	N-24
AD7228ABP	−40°C to +85°C	±2 max	P-28A
AD7228ACP	−40°C to +85°C	±1 max	P-28A
AD7228ABR	−40°C to +85°C	±2 max	R-24
AD7228ACR	−40°C to +85°C	±1 max	R-24
AD7228ABQ	−40°C to +85°C	±2 max	Q-24
AD7228ACQ	−40°C to +85°C	±1 max	Q-24
AD7228ATQ[3]	−55°C to +125°C	±2 max	Q-24
AD7228AUQ[3]	−55°C to +125°C	±1 max	Q-24

NOTES

[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet and availability.

[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

[3]These grades will be available to /883B processing only.

LC²MOS
12-Bit Serial Mini-DIP DACPORT
AD7233

FEATURES

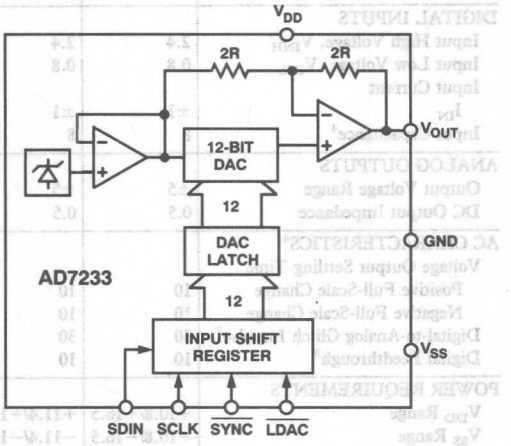
12-Bit CMOS DAC with
- **On-Chip Voltage Reference**
- **Output Amplifier**
- **−5 V to +5 V Output Range**

Serial Interface
300 kHz DAC Update Rate
Small Size : 8-Pin Mini-DIP
Nonlinearity : ±1/2 LSB T_{min} to T_{max}
Low Power Dissipation: 100 mW typical

APPLICATIONS

Process Control
Industrial Automation
Digital Signal Processing Systems
Input/Output Ports

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7233 is a complete 12-bit, voltage-output, digital-to-analog converter with output amplifier and Zener voltage reference all in an 8-pin package. No external trims are required to achieve full specified performance. The data format is 2s complement, and the output range is −5 V to +5 V.

The AD7233 features a fast, versatile serial interface which allows easy connection to both microcomputers and 16-bit digital signal processors with serial ports. When the $\overline{SYNC}$ input is taken low, data on the SDIN pin is clocked into the input shift register on each falling edge of SCLK. On completion of the 16-bit data transfer, bringing $\overline{LDAC}$ low updates the DAC latch with the lower 12 bits of data and updates the output. Alternatively, $\overline{LDAC}$ can be tied permanently low, and in this case the DAC register is automatically updated with the contents of the shift register when all sixteen data bits have been clocked in. The serial data may be applied at rates up to 5 MHz allowing a DAC update rate of 300 kHz.

For applications which require greater flexibility and unipolar output ranges with single supply operation, please refer to the AD7243 data sheet.

The AD7233 is fabricated on Linear Compatible CMOS (LC²MOS), an advanced, mixed-technology process. It is packaged in an 8-pin DIP package.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit DACPORT®
2. The AD7233 is a complete, voltage output, 12-bit DAC on a single chip. This single-chip design is inherently more reliable than multichip designs.
3. Simple 3-Wire Interface to Most Microcontrollers and DSP Processors.
4. DAC Update Rate—300 kHz.
5. Space Saving 8-Pin Package.

DACPORT is a registered trademark of Analog Devices, Inc.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7233—SPECIFICATIONS[1] (V_{DD} = +12 V to +15 V,[2] V_{SS} = −12 V to −15 V,[2] GND= 0 V, R_L = 2 kΩ, C_L = 100 pF to GND. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	A	B	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error[3]	±6	±6	LSB max	DAC Latch Contents 0000 0000 0000
Full-Scale Error[3]	±8	±8	LSB max	
Full-Scale Temperature Coefficient	±30	±30	ppm of FSR/°C typ	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current				
I_{IN}	±1	±1	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[4]	8	8	pF max	
ANALOG OUTPUTS				
Output Voltage Range	±5	±5	V	
DC Output Impedance	0.5	0.5	Ω typ	
AC CHARACTERISTICS[4]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	10	10	μs max	Typically 3 μs; DAC Latch 100. . .000 to 011. . .111
Negative Full-Scale Change	10	10	μs max	Typically 5 μs; DAC Latch 011. . .111 to 100. . .000
Digital-to-Analog Glitch Impulse[3]	30	30	nV secs typ	DAC Latch Contents Toggled Between All 0s and all 1s
Digital Feedthrough[3]	10	10	nV secs typ	$\overline{LDAC}$ = High
POWER REQUIREMENTS				
V_{DD} Range	+10.8/+16.5	+11.4/+15.75	V min/V max	For Specified Performance Unless Otherwise Stated
V_{SS} Range	−10.8/−16.5	−11.4/−15.75	V min/V max	For Specified Performance Unless Otherwise Stated
I_{DD}	10	10	mA max	Output Unloaded; Typically 7 mA
I_{SS}	4	4	mA max	Output Unloaded; Typically 2 mA

NOTES
[1]Temperature Ranges are as follows: A, B Versions: −40°C to +85°C.
[2]Power Supply Tolerance: A Version: ±10%; B Version: ±5%.
[3]See Terminology.
[4]Sample tested @ 25°C to ensure compliance.
Specifications subject to change without notice.

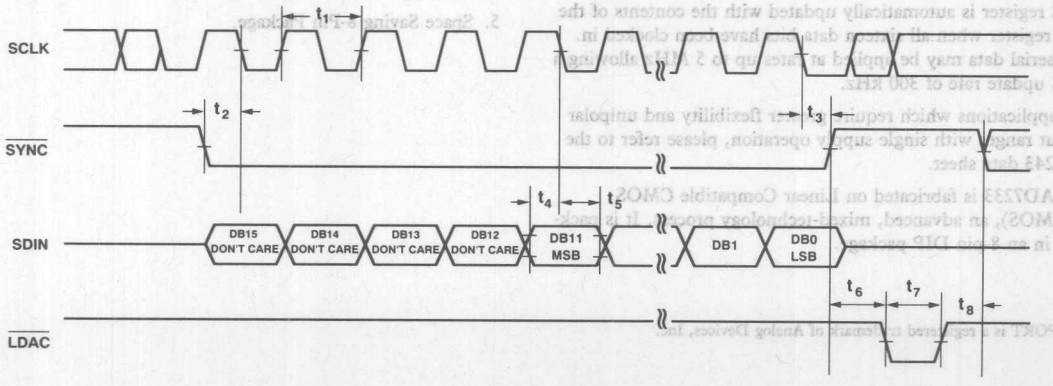


Figure 3. AD7233 Timing Diagram

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +10.8 V to +16.5 V, V_{SS} = −10.8 V to −16.5 V, GND = 0 V, R_L = 2 kΩ, C_L = 100 pF. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	Limit at 25°C (All Versions)	Limit at T_{min}, T_{max} (All Versions)	Units	Conditions/Comments
t_1[3]	200	200	ns min	SCLK Cycle Time
t_2	50	50	ns min	$\overline{SYNC}$ to SCLK Falling Edge Setup Time
t_3	120	190	ns min	$\overline{SYNC}$ to SCLK Hold Time
t_4	10	10	ns min	Data Setup Time
t_5	100	100	ns min	Data Hold Time
t_6	0	0	ns min	$\overline{SYNC}$ High to $\overline{LDAC}$ Low
t_7	50	50	ns min	$\overline{LDAC}$ Pulse Width
t_8	0	0	ns min	$\overline{LDAC}$ High to $\overline{SYNC}$ Low

NOTES
[1]Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figure 3.
[3]SCLK Mark/Space Ratio range is 40/60 to 60/40.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . −0.3 V to +17 V
V_{SS} to GND . . . . . +0.3 V to −17 V
V_{OUT}[1] to GND . . . . . −6 V to V_{DD} +0.3 V
Digital Inputs to GND . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Industrial (A, B Versions) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTE
[1]The output may be shorted to voltages in this range provided the power dissipation of the package is not exceeded. Short circuit current is typically 80 mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

TERMINOLOGY

RELATIVE ACCURACY (LINEARITY)

Relative accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints of the transfer function. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

BIPOLAR ZERO ERROR

Bipolar zero error is the voltage measured at V_{OUT} when the DAC is loaded with all 0s. It is due to a combination of offset errors in the DAC, amplifier and mismatch between the internal gain resistors around the amplifier.

FULL-SCALE ERROR

Full-scale error is a measure of the output error when the amplifier output is at full scale (full scale is either positive or negative full scale).

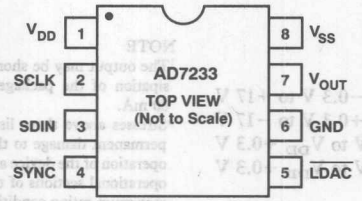
DIGITAL-TO-ANALOG GLITCH IMPULSE

This is the voltage spike that appears at the output of the DAC when the digital code in the DAC latch changes before the output settles to its final value. The energy in the glitch is specified in nV secs, and is measured for an all codes change (0000 0000 0000 to 1111 1111 1111).

DIGITAL FEEDTHROUGH

This is a measure of the voltage spike that appears on V_{OUT} as a result of feedthrough from the digital inputs on the AD7233. It is measured with $\overline{LDAC}$ held high.

1	V_{DD}	Positive Supply (+12 V to +15 V).
2	SCLK	Serial Clock, Logic Input. Data is clocked into the input register on each falling SCLK edge.
3	SDIN	Serial Data In, Logic Input. The 16-bit serial data word is applied to this input.
4	$\overline{SYNC}$	Data Synchronization Pulse, Logic Input. Taking this input low initializes the internal logic in readiness for a new data word.
5	$\overline{LDAC}$	Load DAC, Logic Input. Updates the DAC output. The DAC output is updated on the falling edge of this signal, or alternatively if this line in permanently low, an automatic update mode is selected whereby the DAC is updated on the 16th falling SCLK pulse.
6	GND	Ground pin = 0 V.
7	V_{OUT}	Analog Output Voltage. This is the buffered DAC output voltage (−5 V to +5 V).
8	V_{SS}	Negative Supply (−12 V to −15 V).



ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option*
AD7233AN	−40°C to +85°C	±1 LSB	N-8
AD7233BN	−40°C to +85°C	±1/2 LSB	N-8

*N = Plastic DIP. For outline information see Package Information section.

AD7237A/AD7247A

FEATURES

Complete Dual 12-Bit DAC Comprising
- **Two 12-Bit CMOS DACs**
- **On-Chip Voltage Reference**
- **Output Amplifiers**
- **Reference Buffer Amplifiers**

Improved AD7237/AD7247:
- **12 V to 15 V Operation**
- **Faster Interface –30 ns typ Data Setup Time**

Parallel Loading Structure: AD7247A
(8+4) Loading Structure: AD7237A
Single or Dual Supply Operation
Low Power – 165 mW typ in Single Supply

GENERAL DESCRIPTION

The AD7237A/AD7247A is an enhanced version of the industry standard AD7237/AD7247. Improvements include operation from 12 V to 15 V supplies, faster interface times and better reference variations with V_{DD}. Additional features include faster settling times.

The AD7237A/AD7247A is a complete, dual, 12-bit, voltage output digital-to-analog converter with output amplifiers and Zener voltage reference on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

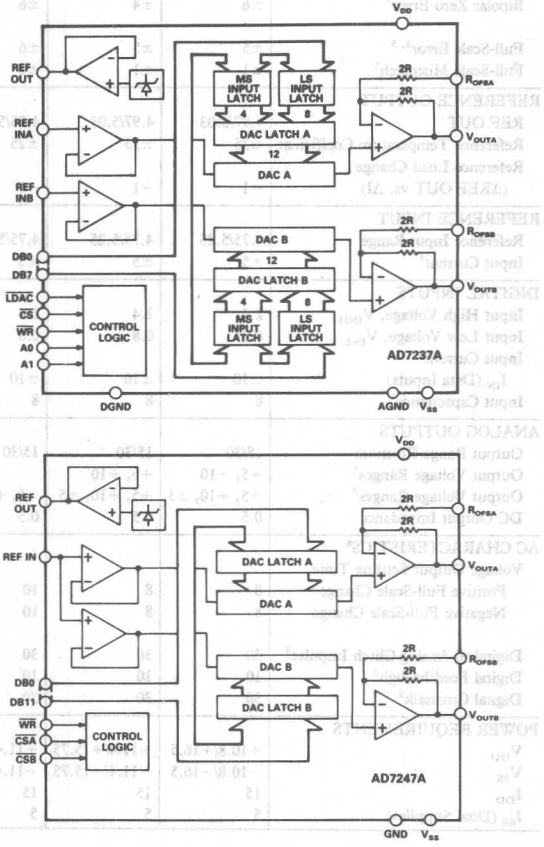
Both parts are microprocessor compatible, with high speed data latches and interface logic. The AD7247A accepts 12-bit parallel data which is loaded into the respective DAC latch using the $\overline{WR}$ input and a separate Chip Select input for each DAC. The AD7237A has a double buffered interface structure and an 8-bit wide data bus with data loaded to the respective input latch in two write operations. An asynchronous $\overline{LDAC}$ signal on the AD7237A updates the DAC latches and analog outputs.

A REF OUT/REF IN function is provided which allows either the on-chip 5 V reference or an external reference to be used as a reference voltage for the part. For single supply operation, two output ranges of 0 to +5 V and 0 to +10 V are available, while these two ranges plus an additional ±5 V range are available with dual supplies. The output amplifiers are capable of developing +10 V across a 2 kΩ load to GND.

The AD7237A/AD7247A is fabricated in Linear Compatible CMOS (LC^2MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. Both parts are available in a 24-pin, 0.3″ wide plastic and hermetic dual-in-line package (DIP) and are also packaged in a 24-lead small outline (SOIC) package.

DACPORT is a registered trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT HIGHLIGHTS

1. The AD7237A/AD7247A is a dual 12-bit DACPORT® on a single chip. This single chip design and small package size offer considerable space saving and increased reliability over multichip designs.
2. The improved interface times of the parts allow easy, direct interfacing to most modern microprocessors, whether they have 8-bit or 16-bit data bus structures.
3. The AD7237A/AD7247A features a wide power supply range allowing operation from 12 V supplies.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7237A/AD7247A—SPECIFICATIONS (V_{DD} = +12 V to +15 V,[1] V_{SS} = 0 V or −12 V to −15 V,[1] AGND = DGND = 0 V [AD7237A], GND = 0 V [AD7247A], REF IN = +5 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	A[2]	B[2]	T[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]	±3	±3	±4	LSB max	V_{SS} = 0 V or −12 V to −15 V[4]. DAC Latch Contents All 0s
Bipolar Zero Error[3]	±6	±4	±6	LSB max	V_{SS} = −12 V to −15 V[4]. DAC Latch Contents 1000 0000 0000
Full-Scale Error[3, 5]	±5	±5	±6	LSB max	
Full-Scale Mismatch[5]	±1	±1	±1	LSB typ	
REFERENCE OUTPUT					
REF OUT	4.97/5.03	4.97/5.03	4.95/5.05	V min/max	
Reference Temperature Coefficient	±25	±25	±25	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	−1	mV max	Reference Load Current Change (0–100 μA)
REFERENCE INPUT					
Reference Input Range	4.75/5.25	4.75/5.25	4.75/5.25	V min/max	5 V ± 5%
Input Current[6]	±5	±5	±5	μA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current I_{IN} (Data Inputs)	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[6]	8	8	8	pF max	
ANALOG OUTPUTS					
Output Range Resistors	15/30	15/30	15/30	kΩ min/max	
Output Voltage Ranges[7]	+5, +10	+5, +10		V	Single Supply; (V_{SS} = 0 V)
Output Voltage Ranges[7]	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5		Dual Supply; (V_{SS} = −12 V to −15 V[4])
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[6]					
Voltage Output Settling Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	8	8	10	μs max	DAC Latch all 0s to all 1s. Typically 5 μs
Negative Full-Scale Change	8	8	10	μs max	DAC Latch all 1s to all 0s. Typically 5 μs V_{SS} = −12 V to −15 V[4].
Digital-to-Analog Glitch Impulse[3]	30	30	30	nV secs typ	DAC Latch Contents Toggled Between all 0's and all 1's.
Digital Feedthrough[3]	10	10	10	nV secs typ	
Digital Crosstalk[3]	30	30	30	nV secs typ	
POWER REQUIREMENTS					
V_{DD}	+10.8/+16.5	+11.4/+15.75	+11.4/+15.75	V min/max	For Specified Performance Unless Otherwise Stated
V_{SS}	−10.8/−16.5	−11.4/−15.75	−11.4/−15.75	V min/max	For Specified Performance Unless Otherwise Stated
I_{DD}	15	15	15	mA max	Output Unloaded. Typically 10 mA
I_{SS} (Dual Supplies)	5	5	5	mA max	Output Unloaded. Typically 3 mA

NOTES
[1]Power Supply tolerance is ±10% for A version and ±5% for B and T versions.
[2]Temperature ranges are as follows: A, B Versions, −40°C to +85°C; T Version, −55°C to +125°C.
[3]See Terminology.
[4]With appropriate power supply tolerances.
[5]Measured with respect to REF IN and includes unipolar/bipolar offset error.
[6]Sample tested @ +25°C to ensure compliance.
[7]0 to +10 V range is only available with V_{DD} ≥ 14.25 V.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +12 V to +15 V,[3] V_{SS} = 0 V or −12 V to −15 V,[3] AGND = DGND = 0 V [AD7237A], GND = 0 V [AD7247A])

Parameter	Limit at T_{min}, T_{max} (A, B Versions)	Limit at T_{min}, T_{max} (T Version)	Units	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	80	100	ns min	$\overline{WR}$ Pulse Width
t_4	80	80	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5[4]	10	10	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6[5]	0	0	ns min	Address to $\overline{WR}$ Setup Time
t_7[5]	0	0	ns min	Address to $\overline{WR}$ Hold Time
t_8[5]	80	100	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 5 and 7.
[3]Power Supply tolerance is ±10% for A version and ±5% for B and T versions.
[4]If 0 ns<t_2<10 ns, add t_2 to t_5. If $t_2 \geq$ 10 ns, add 10 ns to t_5.
[5]AD7237A only.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND (AD7247A) . . . . . −0.3 V to +17 V
V_{DD} to AGND, DGND (AD7237A) . . . . . −0.3 V to +17 V
V_{DD} to V_{SS} . . . . . −0.3 V to +34 V
AGND to DGND (AD7237A) . . . . . −0.3 V, V_{DD} +0.3 V
V_{OUTA}[1], V_{OUTB}[1] to AGND (GND)
. . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
REF OUT to AGND (GND) . . . . . 0 V to V_{DD}
REF IN to AGND (GND) . . . . . −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND (GND) . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTE
[1]Short-circuit current is typically 80mA. The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy (LSB)	Package Option[2]
AD7237AAN	−40°C to +85°C	±1 max	N-24
AD7237ABN	−40°C to +85°C	±1/2 max	N-24
AD7237AAR	−40°C to +85°C	±1 max	R-24
AD7237ABR	−40°C to +85°C	±1/2 max	R-24
AD7237ATQ	−55°C to +125°C	±1/2 max	Q-24
AD7247AAN	−40°C to +85°C	±1 max	N-24
AD7247ABN	−40°C to +85°C	±1/2 max	N-24
AD7247AAR	−40°C to +85°C	±1 max	R-24
AD7247ABR	−40°C to +85°C	±1/2 max	R-24
AD7247ATQ	−55°C to +125°C	±1/2 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet and availability.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline (SOIC). For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7237A/AD7247A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD7237A PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

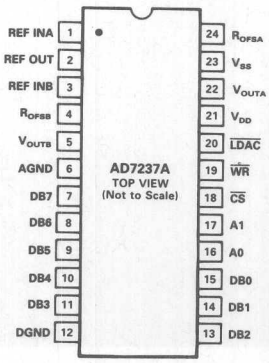
Pin	Mnemonic	Description
1	REF INA	Voltage Reference Input for DAC A. The reference voltage for DAC A is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7237A is 5 V.
2	REF OUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part with internal reference, REF OUT should be connected to REF INA, REF INB.
3	REF INB	Voltage Reference Input for DAC B. The reference voltage for DAC B is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7237A is 5 V.
4	R_{OFSB}	Output Offset Resistor for DAC B. This input configures the output ranges for DAC B. It is connected to V_{OUTB} for the +5 V range, to AGND for the +10 V range and to REF INB for the ±5 V range.
5	V_{OUTB}	Analog Output Voltage from DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
6	AGND	Analog Ground. Ground reference for DACs, reference and output buffer amplifiers.
7	DB7	Data Bit 7.
8–10	DB6–DB4	Data Bit 6 to Data Bit 4.
11	DB3	Data Bit 3/Data Bit 11 (MSB).
12	DGND	Digital Ground. Ground reference for digital circuitry.
13	DB2	Data Bit 2/Data Bit 10.
14	DB1	Data Bit 1/Data Bit 9.
15	DB0	Data Bit 0 (LSB)/Data Bit 8.
16	A0	Address Input. Least significant address input for input latches. A0 and A1 select which of the four input latches data is written to (see Table II).
17	A1	Address Input. Most significant address input for input latches.
18	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
19	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CS}$, A0 and A1 to write data to the input latches.
20	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded into the DAC latches from the respective input latches on the falling edge of this signal.
21	V_{DD}	Positive Supply (+12 V to +15 V).
22	V_{OUTA}	Analog Output Voltage from DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
23	V_{SS}	Negative Supply (0 V or −12 V to −15 V).
24	R_{OFSA}	Output Offset Resistor for DAC A. This input configures the output ranges for DAC A. It is connected to V_{OUTA} for the +5 V range, to AGND for the +10 V range and to REF INA for the ±5 V range.

AD7247A PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

Pin	Mnemonic	Description
1	REF OUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part with internal reference, REF OUT should be connected to REF IN.
2	R_{OFSB}	Output Offset Resistor for DAC B. This input configures the output ranges for DAC B. It is connected to V_{OUTB} for the +5 V range, to GND for the +10 V range and to REF IN for the ±5 V range.
3	V_{OUTB}	Analog Output Voltage from DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
4	DB11	Data Bit 11 (MSB).
5	DB10	Data Bit 10.
6	GND	Ground. Ground reference for all on-chip circuitry.
7–15	DB9–DB1	Data Bit 9 to Data Bit 1.
16	DB0	Data Bit 0 (LSB).
17	$\overline{CSB}$	Chip Select Input for DAC B. Active low logic input. DAC B is selected when this input is active.
18	$\overline{CSA}$	Chip Select Input for DAC A. Active low logic input. DAC A is selected when this input is active.
19	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CSA}$ and $\overline{CSB}$ to write data to the DAC latches.
20	V_{DD}	Positive Supply (+12 V to +15 V).
21	V_{OUTA}	Analog Output Voltage from DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
22	V_{SS}	Negative Supply (0 V or −12 V to −15 V).
23	R_{OFSA}	Output Offset Resistor for DAC A. This input configures the output ranges for DAC A. It is connected to V_{OUTA} for the +5 V range, to GND for the +10 V range and to REF IN for the ±5 V range.
24	REF IN	Voltage Reference Input. The common reference voltage for both DACs is applied to this pin. It is internally buffered before being applied to both DACs. The nominal reference voltage for correct operation of the AD7247A is 5 V.

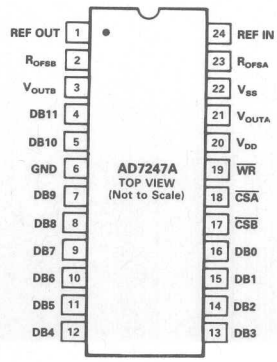
AD7237A PIN CONFIGURATIONS

DIP and SOIC



AD7247A PIN CONFIGURATIONS

DIP and SOIC



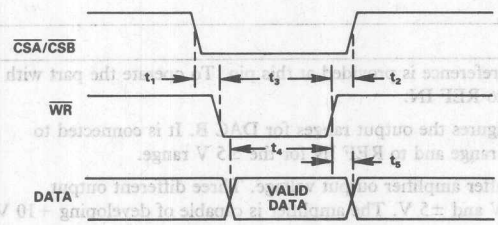


Figure 1. AD7247A Write Cycle Timing Diagram

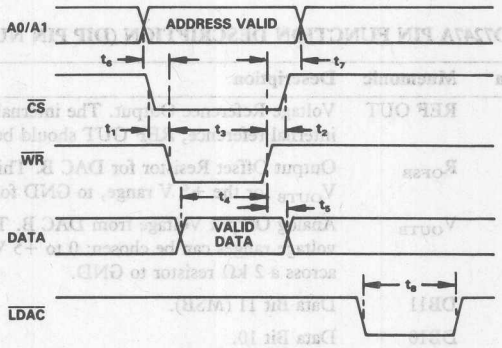


Figure 2. AD7237A Write Cycle Timing Diagram

LC²MOS Dual, Complete, 12-Bit/14-Bit Serial DACs

AD7242/AD7244

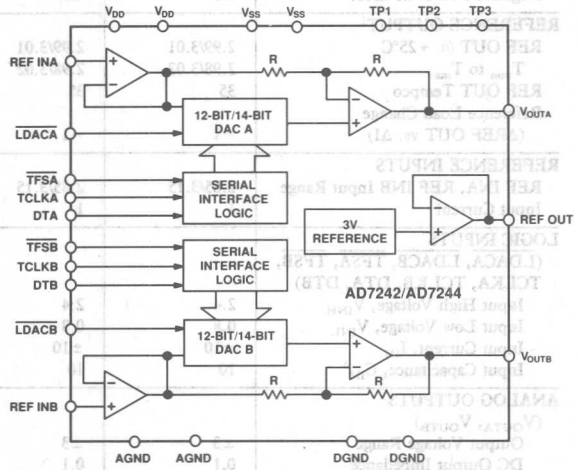
FEATURES

Two 12-Bit/14-Bit DACs with Output Amplifiers
- **AD7242: 12-Bit Resolution**
- **AD7244: 14-Bit Resolution**

On-Chip Voltage Reference
Fast Settling Time
- **AD7242: 3 µs to ±1/2 LSB**
- **AD7244: 4 µs to ±1/2 LSB**

High Speed Serial Interface
Operates from ±5 V Supplies
Specified Over −40°C to +85°C in Plastic Packages
Low Power – 130 mW typ

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7242/AD7244 is a fast, complete, dual 12-bit/14-bit voltage output D/A converter. It consists of a 12-bit/14-bit DAC, 3 V buried Zener reference, DAC output amplifiers and high speed serial interface logic.

Interfacing to both DACs is serial, minimizing pin count and allowing a small package size. Standard control signals allow interfacing to most DSP processors and microcontrollers. Asynchronous control of DAC updating for both DACs is made possible with a separate $\overline{\text{LDAC}}$ input for each DAC.

The AD7242/AD7244 operates from ±5 V power supplies, providing an analog output range of ±3 V. A REF OUT/REF IN function allows the DACs to be driven from the on-chip 3 V reference or from an external reference source.

The AD7242/AD7244 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced mixed technology process that combines precision bipolar circuits with low power CMOS logic. Both parts are available in a 24-pin, 0.3 inch wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin, plastic small outline (SOIC) package. The AD7242 and AD7244 are available in the same pinout to allow easy upgrade from 12-bit to 14-bit performance.

PRODUCT HIGHLIGHTS

1. Complete, Dual 12-Bit/14-Bit DACs
   The AD7242/AD7244 provides the complete function for generating voltages to 12-bit/14-bit resolution. The part features an on-chip reference, output buffer amplifiers and two 12-bit/14-bit D/A converters.
2. High Speed Serial Interface
   The AD7242/AD7244 provides a high speed, easy-to-use, serial interface allowing direct interfacing to DSP processors and microcontrollers. A separate serial port is provided for each DAC.
3. Small Package Size
   The AD7242/AD7244 is available in a 24-pin DIP and a 28-pin SOIC package offering considerable space saving over comparable solutions.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7242/AD7244—SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, REF INA = REF INB = +3 V. V_{OUTA}, V_{OUTB} load to AGND: R_L = 2 kΩ, C_L = 100 pF. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	AD7242 J, A Versions[1]	AD7242 K, B Versions[1]	Units	Test Conditions/Comments
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±5	±5	LSB max	
Positive Full-Scale Error[2]	±5	±5	LSB max	
Negative Full-Scale Error[2]	±5	±5	LSB max	
REFERENCE OUTPUT[3]				
REF OUT @ +25°C	2.99/3.01	2.99/3.01	V min/V max	
T_{min} to T_{max}	2.98/3.02	2.98/3.02	V min/V max	
REF OUT Tempco	35	35	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUTS				
REF INA, REF INB Input Range	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	1	1	μA max	
LOGIC INPUTS (LDACA, $\overline{\text{LDACB}}$, $\overline{\text{TFSA}}$, $\overline{\text{TFSB}}$, TCLKA, TCLKB, DTA, DTB)				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
ANALOG OUTPUTS (V_{OUTA}, V_{OUTB})				
Output Voltage Range	±3	±3	V nom	
DC Output Impedance	0.1	0.1	Ω typ	
Short Circuit Current	20	20	mA typ	
AC CHARACTERISTICS[4]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	3	3	μs max	Typically 2 μs
Negative Full-Scale Change	3	3	μs max	Typically 2 μs
Digital-to-Analog Glitch Impulse	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough	2	2	nV secs typ	
Channel-to-Channel Isolation	110	110	dB typ	V_{OUT} = 10 kHz Sine Wave
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	27	27	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	15	15	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	195	195	mW max	Typically 130 mW

NOTES
[1]Temperature ranges are as follows: J, K Versions: −40°C to +85°C; A, B Versions: −40°C to +85°C.
[2]Measured with respect to REF IN and includes bipolar offset error.
[3]For capacitive loads greater than 50 pF a series resistor is required (see Internal Reference section).
[4]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

AD7242 ORDERING GUIDE

Model	Temperature Range	Integral Nonlinearity	Package Option*
AD7242JN	−40°C to +85°C	±1 LSB max	N-24
AD7242KN	−40°C to +85°C	±1/2 LSB max	N-24
AD7242JR	−40°C to +85°C	±1 LSB max	R-28
AD7242KR	−40°C to +85°C	±1/2 LSB max	R-28
AD7242AQ	−40°C to +85°C	±1 LSB max	Q-24
AD7242BQ	−40°C to +85°C	±1/2 LSB max	Q-24

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

Parameter	AD7244 J/A Versions[1]	AD7244 S Version[1]	Units	Test Conditions/Comments
DC ACCURACY				
Resolution	14	14	Bits	
Integral Nonlinearity	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±10	±15	LSB max	
Positive Full-Scale Error[2]	±10	±15	LSB max	
Negative Full-Scale Error[2]	±10	±15	LSB max	
REFERENCE OUTPUT[3]				
REF OUT @ +25°C	2.99/3.01	2.99/3.01	V min/V max	
T_{min} to T_{max}	2.98/3.02	2.93/3.05	V min/V max	
REF OUT Tempco	35	35	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUTS				
REF INA, REF INB Input Range	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	1	1	μA max	
LOGIC INPUTS ($\overline{LDACA}$, $\overline{LDACB}$, $\overline{TFSA}$, $\overline{TFSB}$, TCLKA, TCLKB, DTA, DTB)				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
ANALOG OUTPUTS (V_{OUTA}, V_{OUTB})				
Output Voltage Range	±3	±3	V nom	
DC Output Impedance	0.1	0.1	Ω typ	
Short Circuit Current	20	20	mA typ	
AC CHARACTERISTICS[4]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	4	4	μs max	Typically 2.5 μs
Negative Full-Scale Change	4	4	μs max	Typically 2.5 μs
Digital-to-Analog Glitch Impulse	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough	2	2	nV secs typ	
Channel-to-Channel Isolation	110	110	dB typ	V_{OUT} = 10 kHz Sine Wave
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	27	28	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	15	15	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	195	205	mW max	Typically 130 mW

NOTES
[1]Temperature ranges are as follows: J Version: 0°C to +70°C; A Version: −40°C to +85°C; S Version: −55°C to +125°C.
[2]Measured with respect to REF IN and includes bipolar offset error.
[3]For capacitive loads greater than 50 pF a series resistor is required (see Internal Reference section).
[4]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

AD7244 ORDERING GUIDE

Model[1]	Temperature Range	Integral Nonlinearity	Package Option[2]
AD7244JN	−40°C to +85°C	±2 LSB max	N-24
AD7244JR	−40°C to +85°C	±2 LSB max	R-28
AD7244AQ	−40°C to +85°C	±2 LSB max	Q-24
AD7244SQ[3]	−55°C to +125°C	±2 LSB max	Q-24

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet and availability.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[3]This grade will be available to /883B processing only.

Parameter	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (S Version)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{TFS}$ to TCLK Falling Edge
t_2	75	100	ns min	TCLK Falling Edge to $\overline{TFS}$
t_3[3]	150	200	ns min	TCLK Cycle Time
t_4	30	40	ns min	Data Valid to TCLK Setup Time
t_5	75	100	ns min	Data Valid to TCLK Hold Time
t_6	40	40	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Timing specifications are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figure 6.
[3]TCLK Mark/Space ratio is 40/60 to 60/40.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
V_{OUT} to AGND . . . . . V_{SS} to V_{DD}
REF OUT to AGND . . . . . −0.3 V to V_{DD} + 0.3 V
REF INA, REF INB to AGND . . . . −0.3 V to V_{DD} + 0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
J, K Versions
AD7244 . . . . . 0°C to +70°C
AD7242 . . . . . −40°C to +85°C
A, B Versions . . . . . −40°C to +85°C
S Version . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 550 mW
Derates above +75°C by . . . . . 6 mW/°C

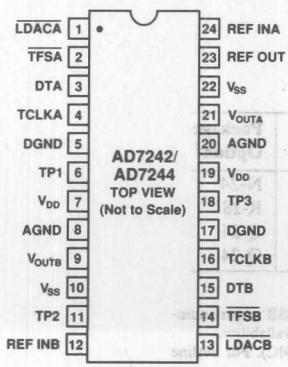
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

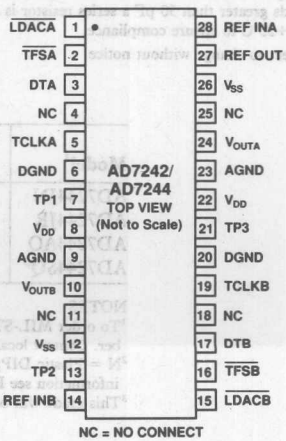
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

PIN CONFIGURATIONS

DIP



SOIC



NC = NO CONNECT

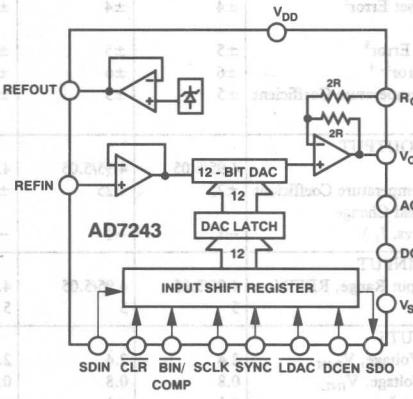
LC²MOS 12-Bit Serial DACPORT

AD7243

FEATURES
- 12-Bit CMOS DAC with
  - On-Chip Voltage Reference
  - Output Amplifier
- 3 Selectable Output Ranges
  - −5 V to +5 V, 0 to +5 V, 0 to +10 V
- Serial Interface
- 300 kHz DAC Update Rate
- Small Size: 16-Pin DIP or SOIC
- Nonlinearity: ±1/2 LSB T_{min} to T_{max}
- Low Power Dissipation: 100 mW typical

APPLICATIONS
- Process Control
- Industrial Automation
- Digital Signal Processing Systems
- Input/Output Ports

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7243 is a complete 12-bit, voltage output, digital-to-analog converter with output amplifier and Zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance.

The output amplifier is capable of developing +10 V across a 2 kΩ load. The output voltage ranges with single supply operation are 0 to +5 V or 0 to +10 V, while an additional bipolar ±5 V output range is available with dual supplies. The ranges are selected using the internal gain resistor.

The data format is natural binary in both unipolar ranges, while either offset binary or 2s complement format may be selected in the bipolar range. A $\overline{CLR}$ function is provided which sets the output to 0 V in both unipolar ranges and in the 2s complement bipolar range, while with offset binary data format, the output is set to −REFIN. This function is useful as a power-on reset as it allows the output to be set to a known voltage level.

The AD7243 features a fast versatile serial interface which allows easy connection to both microcomputers and 16-bit digital signal processors with serial ports. The serial data may be applied at rates up to 5 MHz allowing a DAC update rate of 300 kHz. A serial data output capability is also provided which allows daisy chaining in multi-DAC systems. This feature allows any number of DACs to be used in a system with a simple 4-wire interface. All DACs may be updated simultaneously using $\overline{LDAC}$.

DACPORT is a registered trademark of Analog Devices, Inc.

The AD7243 is fabricated on Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process. It is packaged in 16-pin DIP and 16-pin SOIC packages.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit DACPORT®
   The AD7243 is a complete, voltage output, 12-bit DAC on a single chip. The single chip design is inherently more reliable than multichip designs.
2. Single or Dual Supply Operation.
3. Minimum 3-wire interface to most DSP processors.
4. DAC Update Rate–300 kHz.
5. Serial Data Output allows easy daisy-chaining in multiple DAC systems.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7243—SPECIFICATIONS

(V_{DD} = +12 V to +15 V,[1] V_{SS} = 0 V or −12 V to −15 V,[1] AGND = DGND = 0 V, REFIN = +5 V, R_L = 2 kΩ, C_L = 100 pF to AGND. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	A[2]	B[2]	S[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]	±4	±4	±5	LSB max	V_{SS} = 0 V or −12 V to −15 V;[1] DAC Latch Contents All 0s
Bipolar Zero Error[3]	±5	±5	±6	LSB max	V_{SS} = −12 V to −15 V[1]; DAC Latch Contents All 0s
Full-Scale Error[3, 4]	±6	±6	±7	LSB max	
Full-Scale Temperature Coefficient	±5	±5	±5	ppm of FSR/°C typ	
REFERENCE OUTPUT					
REFOUT	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	
Reference Temperature Coefficient	±25	±25	±30	ppm/°C typ	
Reference Load Change (ΔREFOUT vs. I_L)	−1	−1	−1	mV max	Reference Load Current (I_L) Change (0–100 μA)
REFERENCE INPUT					
Reference Input Range, REFIN	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	5 V ±1% for Specified Performance
Input Current	5	5	5	μA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current, I_{IN}	±1	±1	±1	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[5]	8	8	8	pF max	
DIGITAL OUTPUT					
Serial Data Out (SDO)					
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.0 mA
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 400 μA
ANALOG OUTPUT					
Output Range Resistor, R_{OFS}	15/30	15/30	15/30	kΩ min/ max	
Output Voltage Ranges[6]	+5, +10	+5, +10	+5, +10	V	Single Supply; V_{SS} = 0 V
Output Voltage Ranges[6]	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5	V	Dual Supply; V_{SS} = −12 V to −15 V
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[5]					
Voltage Output Settling-Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	10	10	12	μs max	Typically 3 μs
Negative Full-Scale Change	10	10	10	μs max	Typically 5 μs; V_{SS} = −12 V to −15 V[1]
Negative Full-Scale Change	10	10	10	μs typ	V_{SS} = 0 V
Digital-to-Analog Glitch Impulse[3]	30	30	30	nV secs typ	DAC Latch Contents Toggled Between All 0s and All 1s
Digital Feedthrough[3]	10	10	10	nV secs typ	LDAC = High
POWER REQUIREMENTS					
V_{DD} Range	+10.8/+16.5	+11.4/+15.75	+11.4/+15.75	V min/V max	For Specified Performance Unless Otherwise Stated
V_{SS} Range (Dual Supplies)	−10.8/−16.5	−11.4/−15.75	−11.4/−15.75	V min/V max	For Specified Performance Unless Otherwise Stated
I_{DD}	10	10	12	mA max	Output Unloaded; Typically 7 mA
I_{SS} (Dual Supplies)	4	4	4	mA max	Output Unloaded; Typically 2 mA

NOTES

[1]Power Supply Tolerance A Version: ±10%; B, S Versions: ±5%.

[2]Temperature Ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.

[3]See terminology.

[4]Measured with respect to REFIN and includes unipolar/bipolar offset error.

[5]Sample tested @ +25°C to ensure compliance.

[6]0 to +10 V output range is available only with $V_{DD} \geq$ +14.25 V.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +10.8 V to +16.5 V, V_{SS} = 0 V or −10.8 V to −16.5 V, AGND = DGND = 0 V, R_L = 2kΩ, C_L = 100 pF. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	Limit at +25°C (All Versions)	Limit at T_{min}, T_{max} (All Versions)	Units	Conditions/Comments
t_1[3]	200	200	ns min	SCLK Cycle Time
t_2	50	50	ns min	$\overline{SYNC}$ to SCLK Falling Edge Setup Time
t_3	120	190	ns min	$\overline{SYNC}$ to SCLK Hold Time
t_4	10	10	ns min	Data Setup Time
t_5	100	100	ns min	Data Hold Time
t_6	0	0	ns min	$\overline{SYNC}$ High to $\overline{LDAC}$ Low
t_7	50	50	ns min	$\overline{LDAC}$ Pulse Width
t_8	0	0	ns min	$\overline{LDAC}$ High to $\overline{SYNC}$ Low
t_9	75	75	ns min	$\overline{CLR}$ Pulse Width
t_{10}[4]	120	180	ns max	SCLK Falling Edge to SDO Valid

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 7 & 8.
[3]SCLK mark/space ratio range is 40/60 to 60/40.
[4]SDO load capacitance is no greater than 50 pF.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND, DGND . . . . . −0.3 V to +17 V
V_{SS} to AGND, DGND . . . . . +0.3 V to −17 V
AGND to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
V_{OUT}[2] to AGND . . . . . −6 V to V_{DD} + 0.3 V
REFOUT to AGND . . . . . 0 V to V_{DD}
REFIN to AGND . . . . . −0.3 V to V_{DD} + 0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
SDO to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 6 mW/°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any time.
[2]The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded. Short circuit current is typically 80 mA.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

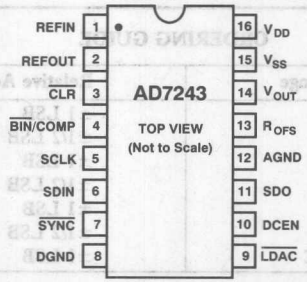
ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option[1]
AD7243AN	−40°C to +85°C	±1 LSB	N-16
AD7243BN	−40°C to +85°C	±1/2 LSB	N-16
AD7243AR	−40°C to +85°C	±1 LSB	R-16
AD7243BR	−40°C to +85°C	±1/2 LSB	R-16
AD7243AQ	−40°C to +85°C	±1 LSB	Q-16
AD7243BQ	−40°C to +85°C	±1/2 LSB	Q-16
AD7243SQ[2]	−55°C to +125°C	±1 LSB	Q-16

NOTES
[1]N = Plastic DIP; R = SOIC; Q = Cerdip. For outline information see Package Information section.
[2]Available to /883B processing only. Contact your local sales office for military data sheet.

Pin	Mnemonic	Description
1	REFIN	Voltage Reference Input. It is internally buffered before being applied to the DAC. The nominal reference voltage for specified operation of the AD7243 is 5 V.
2	REFOUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part using its internal reference, REFOUT should be connected to REFIN.
3	$\overline{\text{CLR}}$	Clear, Logic Input. Taking this input low sets V_{OUT} to 0 V in both unipolar ranges and the 2s complement bipolar range and to −REFIN in the offset binary bipolar range.
4	$\overline{\text{BIN}}$/COMP	Logic Input . This input selects the data format to be either binary or 2s complement. In both unipolar ranges, natural binary format is selected by connecting this input to a logic "0." In the bipolar configuration, offset binary format is selected with a logic "0" while a logic "1" selects 2s complement format.
5	SCLK	Serial Clock, Logic Input. Data is clocked into the input register on each falling SCLK edge.
6	SDIN	Serial Data In, Logic Input. The 16-bit serial data word is applied to this input.
7	$\overline{\text{SYNC}}$	Data Synchronization Pulse, Logic Input. Taking this input low initializes the internal logic in readiness for a new data word.
8	DGND	Digital Ground. Ground reference for all digital circuitry.
9	$\overline{\text{LDAC}}$	Load DAC, Logic Input. Updates the DAC output. The DAC output is updated on the falling edge of this signal or alternatively if this line is permanently low, an automatic update mode is selected whereby the DAC is updated on the 16th falling SCLK pulse.
10	DCEN	Daisy-Chain Enable, Logic Input. Connect this pin high if a daisy-chain interface is being used, otherwise this pin must be connected low.
11	SDO	Serial Data Out, Logic Output. With DCEN at Logic "1" this output is enabled, and the serial data in the input shift register is clocked out on each falling SCLK edge.
12	AGND	Analog Ground. Ground reference for all analog circuitry.
13	R_{OFS}	Output Offset Resistor for the amplifier. It is connected to V_{OUT} for the +5 V range, to AGND for the +10 V range and to REFIN for the −5 V to +5 V range.
14	V_{OUT}	Analog Output Voltage. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and −5 V to +5 V.
15	V_{SS}	Negative Power Supply (used for the output amplifier only, may be connected to 0 V for single supply operation or to −12 V to −15 V for dual supplies).
16	V_{DD}	Positive Power Supply (+12 V to +15 V).

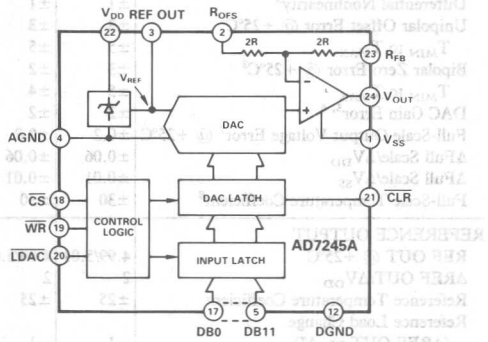
PIN CONFIGURATION
DIP and SOIC



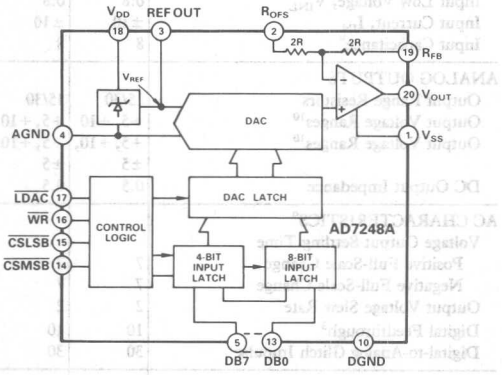
FEATURES

12-Bit CMOS DAC with Output Amplifier and Reference
Improved AD7245/AD7248:
12 V to 15 V Operation
±1/2 LSB Linearity Grade
Faster Interface–30 ns typ Data Setup Time
Extended Plastic Temperature Range (–40°C to +85°C)
Single or Dual Supply Operation
Low Power–65 mW typ in Single Supply
Parallel Loading Structure: AD7245A
(8+4) Loading Structure: AD7248A

AD7245A FUNCTIONAL BLOCK DIAGRAM



AD7248A FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7245A/AD7248A is an enhanced version of the industry standard AD7245/AD7248. Improvements include operation from 12 V to 15 V supplies, a ±1/2 LSB linearity grade, faster interface times and better full scale and reference variations with V_{DD}. Additional features include extended temperature range operation for commercial and industrial grades.

The AD7245A/AD7248A is a complete, 12-bit, voltage output, digital-to-analog converter with output amplifier and Zener voltage reference on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and double-buffered interface logic. The AD7245A accepts 12-bit parallel data which is loaded into the input latch on the rising edge of $\overline{CS}$ or $\overline{WR}$. The AD7248A has an 8-bit wide data bus with data loaded to the input latch in two write operations. For both parts, an asynchronous $\overline{LDAC}$ signal transfers data from the input latch to the DAC latch and updates the analog output. The AD7245A also has a $\overline{CLR}$ signal on the DAC latch which allows features such as power-on reset to be implemented.

The on-chip 5 V buried Zener diode provides a low noise, temperature compensated reference for the DAC. For single supply operation, two output ranges of 0 to +5 V and 0 to +10 V are available, while these two ranges plus an additional ±5 V range are available with dual supplies. The output amplifiers are capable of developing +10 V across a 2 kΩ load to GND.

The AD7245A/AD7248A is fabricated in linear compatible CMOS (LC^2MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The AD7245A is available in a small, 0.3″ wide, 24-pin DIP and SOIC and in 28-terminal surface mount packages. The AD7248A is packaged in a small, 0.3″ wide, 20-pin DIP and SOIC and in 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. The AD7245A/AD7248A is a 12-bit DACPORT® on a single chip. This single chip design and small package size offer considerable space saving and increased reliability over multichip designs.
2. The improved interface times on the part allows easy, direct interfacing to most modern microprocessors.
3. The AD7245A/AD7248A features a wide power supply range allowing operation from 12 V supplies.

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7245A/AD7248A—SPECIFICATIONS (V_{DD} = +12 V to +15 V,[1] V_{SS} = 0 V or −12 V to −15 V,[1] AGND = DGND = 0 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A[2] Version	B[2] Version	T[2] Version	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy @ +25°C[3]	±3/4	±1/2	±1/2	LSB max	
T_{MIN} to T_{MAX}	±1	±3/4	±3/4	LSB max	
T_{MIN} to T_{MAX}		±1/2		LSB max	V_{DD} = 15 V ± 5%
Differential Nonlinearity[3]	±1	±1	±1	LSB max	Guaranteed Monotonic
Unipolar Offset Error @ +25°C[3]	±3	±3	±3	LSB max	V_{SS} = 0 V or −12 V to −15 V[4]
T_{MIN} to T_{MAX}	±5	±5	±5	LSB max	Typical Tempco is ±3 ppm of FSR[5]/°C.
Bipolar Zero Error @ +25°C[3]	±3	±2	±2	LSB max	R_{OFS} connected to REF OUT; V_{SS} = −12 V to −15 V[4]
T_{MIN} to T_{MAX}	±5	±4	±4	LSB max	Typical Tempco is ±3 ppm of FSR[5]/°C.
DAC Gain Error[3, 6]	±2	±2	±2	LSB max	
Full-Scale Output Voltage Error[7] @ +25°C	±0.2	±0.2	±0.2	% of FSR max	V_{DD} = +15 V
ΔFull Scale/ΔV_{DD}	±0.06	±0.06	±0.06	% of FSR/V max	V_{DD} = +12 V to +15 V[4]
ΔFull Scale/ΔV_{SS}	±0.01	±0.01	±0.01	% of FSR/V max	V_{SS} = −12 V to −15 V[4]
Full-Scale Temperature Coefficient[8]	±30	±30	±40	ppm of FSR/°C max	V_{DD} = +15 V
REFERENCE OUTPUT					
REF OUT @ +25°C	4.99/5.01	4.99/5.01	4.99/5.01	V min/V max	V_{DD} = +15 V
ΔREF OUT/ΔV_{DD}	2	2	2	mV/V max	V_{DD} = +12 V to +15 V[4]
Reference Temperature Coefficient	±25	±25	±35	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	−1	mV max	Reference Load Current Change (0–100 μA)
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[9]	8	8	8	pF max	
ANALOG OUTPUTS					
Output Range Resistors	15/30	15/30	15/30	kΩ min/kΩ max	
Output Voltage Ranges[10]	+5, +10	+5, +10	+5, +10	V	V_{SS} = 0 V; Pin Strappable
Output Voltage Ranges[10]	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5	V	V_{SS} = −12 V to −15 V;[4] Pin Strappable
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[9]					
Voltage Output Settling Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	7	7	10	μs max	DAC Latch All 0s to All 1s
Negative Full-Scale Change	7	7	10	μs max	DAC Latch All 1s to All 0s; V_{SS} = −12 V to −15 V[4]
Output Voltage Slew Rate	2	2	1.5	V/μs min	
Digital Feedthrough[3]	10	10	10	nV-s typ	
Digital-to-Analog Glitch Impulse	30	30	30	nV-s typ	
POWER REQUIREMENTS					
V_{DD}	+10.8/ +16.5	+11.4/ +15.75	+11.4/ +15.75	V min/ V max	For Specified Performance Unless Otherwise Stated
V_{SS}	−10.8/ −16.5	−11.4/ −15.75	−11.4/ −15.75	V min/ V max	For Specified Performance Unless Otherwise Stated
I_{DD} @ +25°C	9	9	9	mA max	Output Unloaded; Typically 5 mA
T_{MIN} to T_{MAX}	10	10	12	mA max	Output Unloaded
I_{SS} (Dual Supplies)	3	3	5	mA max	Output Unloaded; Typically 2 mA

NOTES
[1]Power supply tolerance is ±10% for A Version and ±5% for B and T Versions.
[2]Temperature ranges are as follows: A/B Versions; −40°C to +85°C; T Version; −55°C to +125°C.
[3]See Terminology.
[4]With appropriate power supply tolerances.
[5]FSR means Full-Scale Range and is 5 V for the 0 to +5 V output range and 10 V for both the 0 to +10 V and ±5 V output ranges.
[6]This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.
[7]This error is calculated with respect to an ideal 4.9988 V on the 0 to +5 V and ±5 V ranges; it is calculated with respect to an ideal 9.9976 V on the 0 to +10 V range. It includes the effects of internal voltage reference, gain and offset errors.
[8]Full-Scale TC = ΔFS/ΔT, where ΔFS is the full-scale change from T_A = +25°C to T_{MIN} or T_{MAX}.
[9]Sample tested at +25°C to ensure compliance.
[10]0 to +10 V output range is available only when $V_{DD} \geq$ +14.25 V.
Specifications subject to change without notice.

SWITCHING CHARACTERISTICS[1] (V_{DD} = +12 V to +15 V;[2] V_{SS} = 0 V or −12 V to −15 V;[2] See Figures 5 and 7.)

Parameter	A, B Versions	S Version	Units	Conditions
t_1				
@ +25°C	55	55	ns typ	Chip Select Pulse Width
T_{min} to T_{max}	80	100	ns min	
t_2				
@ +25°C	40	40	ns typ	Write Pulse Width
T_{min} to T_{max}	80	100	ns min	
t_3				
@ +25°C	0	0	ns min	Chip Select to Write Setup Time
T_{min} to T_{max}	0	0	ns min	
t_4				
@ +25°C	0	0	ns min	Chip Select to Write Hold Time
T_{min} to T_{max}	0	0	ns min	
t_5				
@ +25°C	40	40	ns typ	Data Valid to Write Setup Time
T_{min} to T_{max}	80	80	ns min	
t_6				
@ +25°C	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	ns min	
t_7				
@ +25°C	40	40	ns typ	Load DAC Pulse Width
T_{min} to T_{max}	80	100	ns min	
t_8				
@ +25°C	40	40	ns typ	Clear Pulse Width
T_{min} to T_{max}	80	100	ns min	

NOTE
[1]Sample tested at +25°C to ensure compliance.
[2]Power supply tolerance is ±10% for A Version and ±5% for B and S Versions.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3 V to +17 V
V_{DD} to DGND . . . . . −0.3 V to +17 V
V_{DD} to V_{SS} . . . . . −0.3 V to +34 V
AGND to DGND . . . . . −0.3 V, V_{DD}
Digital Input Voltage to DGND . . . . −0.3 V, V_{DD} +0.3 V
V_{OUT} to AGND[1] . . . . . V_{SS}, V_{DD}
V_{OUT} to V_{SS}[1] . . . . . 0 V, +24 V
V_{OUT} to V_{DD}[1] . . . . . −32 V, 0 V
REF OUT[1] to AGND . . . . . 0 V, V_{DD}
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 6 mW/°C

Operating Temperature
Commercial (A, B Versions) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

NOTE
[1]The output may be shorted to voltages in this range provided the power dissipation of the package is not exceeded. V_{OUT} short circuit current is typically 80 mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

Model[1]	Temperature Range	Relative Accuracy	Package Option[2]
AD7245AAN	−40°C to +85°C	±3/4 LSB	N-24
AD7245ABN	−40°C to +85°C	±1/2 LSB	N-24
AD7245AAQ	−40°C to +85°C	±3/4 LSB	Q-24
AD7245ATQ[3]	−55°C to +125°C	±3/4 LSB	Q-24
AD7245AAP	−40°C to +85°C	±3/4 LSB	P-28A
AD7245AAR	−40°C to +85°C	±3/4 LSB	R-24
AD7245ABR	−40°C to +85°C	±1/2 LSB	R-24
AD7245ATE[3]	−55°C to +125°C	±3/4 LSB	E-28A

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[3]This grade will be available to /883B processing only.

AD7248A ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Option[2]
AD7248AAN	−40°C to +85°C	±3/4 LSB	N-20
AD7248ABN	−40°C to +85°C	±1/2 LSB	N-20
AD7248AAQ	−40°C to +85°C	±3/4 LSB	Q-20
AD7248ATQ[3]	−55°C to +125°C	±3/4 LSB	Q-20
AD7248AAP	−40°C to +85°C	±3/4 LSB	P-20A
AD7248AAR	−40°C to +85°C	±3/4 LSB	R-20
AD7248ABR	−40°C to +85°C	±1/2 LSB	R-20

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[3]This grade will be available to /883B processing only.

TERMINOLOGY

RELATIVE ACCURACY
Relative Accuracy, or end-point nonlinearity, is a measure of the actual deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after allowing for zero and full scale and is normally expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY
Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

DIGITAL FEEDTHROUGH
Digital Feedthrough is the glitch impulse injected from the digital inputs to the analog output when the inputs change state. It is measured with $\overline{LDAC}$ high and is specified in nV-s.

ideal DAC and the actual device output with all 1s loaded after offset error has been allowed for. It is, therefore defined as:

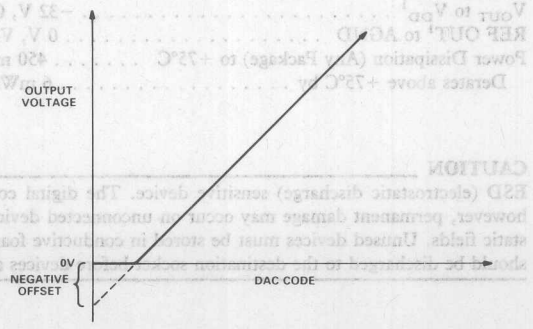
Measured Value—Offset—Ideal Value

where the ideal value is calculated relative to the actual reference value.

UNIPOLAR OFFSET ERROR
Unipolar Offset Error is a combination of the offset errors of the voltage mode DAC and the output amplifier and is measured when the part is configured for unipolar outputs. It is present or all codes and is measured with all 0s in the DAC register.

BIPOLAR ZERO OFFSET ERROR
Bipolar Zero Offset Error is measured when the part is configured for bipolar output and is a combination of errors from the DAC and output amplifier. It is present for all codes and is measured with a code of 2048 (decimal) in the DAC register.

SINGLE SUPPLY LINEARITY AND GAIN ERROR
The output amplifier of the AD7245A/AD7248A can have a true negative offset even when the part is operated from a single positive power supply. However, because the lower supply rail to the part is 0 V, the output voltage cannot actually go negative. Instead the output voltage sits on the lower rail and this results in the transfer function shown across. This is an offset effect and the transfer function would have followed the dotted line if the output voltage could have gone negative. Normally, linearity is measured after offset and full scale have been adjusted or allowed for. On the AD7245A/AD7248A the negative offset is allowed for by calculating the linearity from the code which the amplifier comes off the lower rail. This code is given by the negative offset specification. For example, the single supply linearity specification applies between Code 3 and Code 4095 for the 25°C specification and between Code 5 and Code 4095 over the T_{min} to T_{max} temperature range. Since gain error is also measured after offset has been allowed for, it is calculated between the same codes as the linearity error. Bipolar linearity and gain error are measured between Code 0 and Code 4095.

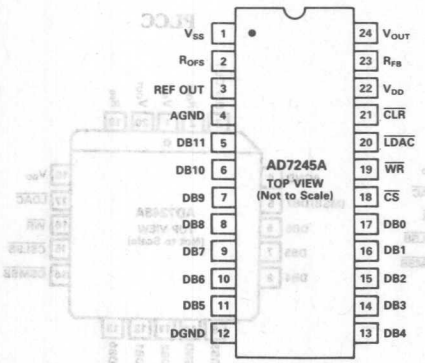


AD7245A PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

Pin	Mnemonic	Description
1	V_{SS}	Negative Supply Voltage (0 V for single supply operation).
2	R_{OFS}	Bipolar Offset Resistor. This provides access to the on-chip application resistors and allows different output voltage ranges.
3	REF OUT	Reference Output. The on-chip reference is provided at this pin and is used when configuring the part for bipolar outputs.
4	AGND	Analog Ground.
5	DB11	Data Bit 11. Most Significant Bit (MSB).
6–11	DB10–DB5	Data Bit 10 to Data Bit 5.
12	DGND	Digital Ground.
13–16	DB4–DB1	Data Bit 4 to Data Bit 1.
17	DB0	Data Bit 0. Least Significant Bit (LSB).
18	$\overline{CS}$	Chip Select Input (Active LOW). The device is selected when this input is active.
19	$\overline{WR}$	Write Input (Active LOW). This is used in conjunction with $\overline{CS}$ to write data into the input latch of the AD7245A.
20	$\overline{LDAC}$	Load DAC Input (Active LOW). This is an asynchronous input which when active transfers data from the input latch to the DAC latch.
21	$\overline{CLR}$	Clear Input (Active LOW). When this input is active the contents of the DAC latch are reset to all 0s.
22	V_{DD}	Positive Supply Voltage.
23	R_{FB}	Feedback Resistor. This allows access to the amplifier's feedback loop.
24	V_{OUT}	Output Voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V or −5 V to +5 V.

AD7245A PIN CONFIGURATIONS

DIP and SOIC



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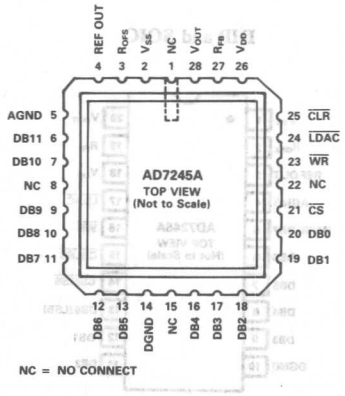

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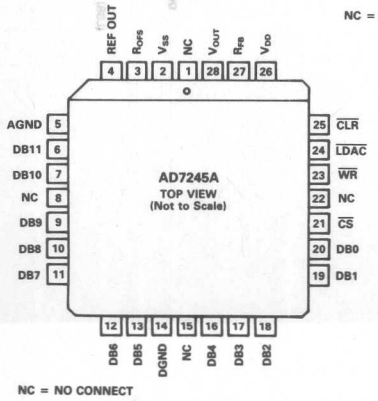
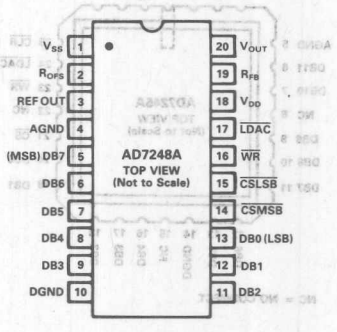


AD7248A PIN FUNCTION DESCRIPTION
(ANY PACKAGE)

Pin	Mnemonic	Description
1	V_{SS}	Negative Supply Voltage (0 V for single supply operation).
2	R_{OFS}	Bipolar Offset Resistor. This provides access to the on-chip application resistors and allows different output voltage ranges.
3	REF OUT	Reference Output. The on-chip reference is provided at this pin and is used when configuring the part for bipolar outputs.
4	AGND	Analog Ground.
5	DB7	Data Bit 7.
6	DB6	Data Bit 6.
7	DB5	Data Bit 5.
8	DB4	Data Bit 4.
9	DB3	Data Bit 3/Data Bit 11 (MSB).
10	DGND	Digital Ground.
11	DB2	Data Bit 2/Data Bit 10.
12	DB1	Data Bit 1/Data Bit 9.
13	DB0	Data Bit 0 (LSB)/Data Bit 8.
14	$\overline{CSMSB}$	Chip Select Input for MS Nibble. (Active LOW). This selects the upper 4 bits of the input latch. Input data is right justified.
15	$\overline{CSLSB}$	Chip Select Input for LS byte. (Active LOW). This selects the lower 8 bits of the input latch.
16	$\overline{WR}$	Write Input This is used in conjunction with $\overline{CSMSB}$ and $\overline{CSLSB}$ to load data into the input latch of the AD7248A.
17	$\overline{LDAC}$	Load DAC Input (Active LOW). This is an asynchronous input which when active transfers data from the input latch to the DAC latch.
18	V_{DD}	Positive Supply Voltage.
19	R_{FB}	Feedback Resistor. This allows access to the amplifier's feedback loop.
20	V_{OUT}	Output Voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V or −5 V to +5 V.

AD7248A PIN CONFIGURATIONS

DIP and SOIC



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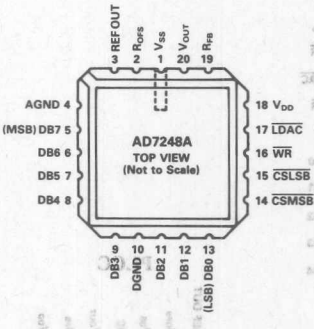

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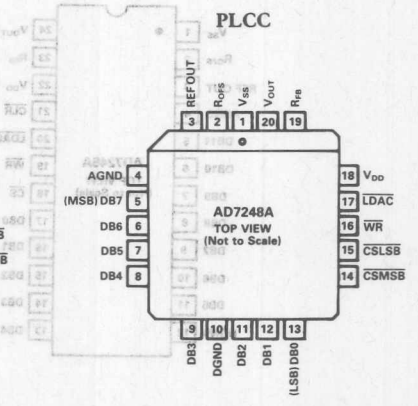


LC²MOS Dual 12-Bit Serial DACPORT

AD7249

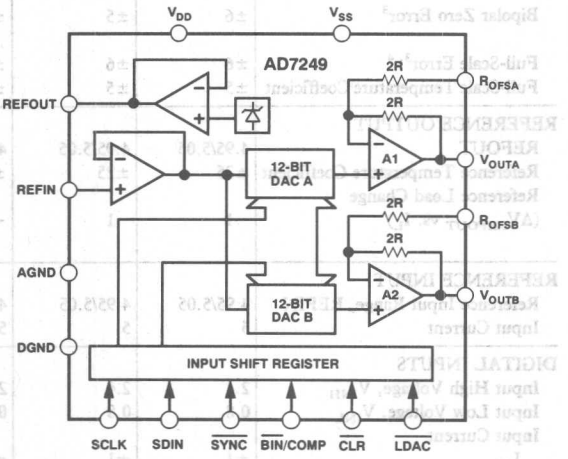
FEATURES

- Two 12-Bit CMOS DAC Channels with
  - On-Chip Voltage Reference
  - Output Amplifiers
- Three Selectable Output Ranges per Channel
  - −5 V to +5 V, 0 to +5 V, 0 to +10 V
- Serial Interface
- 125 kHz DAC Update Rate
- Small Size : 16-Pin DIP or SOIC
- Low Power Dissipation

APPLICATIONS

- Process Control
- Industrial Automation
- Digital Signal Processing Systems
- Input/Output Ports

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7249 contains a pair of 12-bit, voltage-output, digital-to-analog converters with output amplifiers and Zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance.

The output amplifiers are capable of developing +10 V across a 2 kΩ load. The output voltage ranges with single supply operation are 0 V to +5 V or 0 V to +10 V, while an additional bipolar ±5 V output range is available with dual supplies. The ranges are selected using the internal gain resistor.

Interfacing to the AD7249 is serial, minimizing pin count and allowing a small package size. Standard control signals allow interfacing to most DSP processors and microcontrollers. The data stream consists of 16 bits, DB15 to DB13 are don't care bits, the 13th bit (DB12) is used as the channel select bit and the remaining 12 bits (DB11 to DB0) contain the data to update the DAC. The 16-bit data word is clocked into the input register on each falling SCLK edge.

The data format is natural binary in both unipolar ranges, while either offset binary or twos complement format may be selected in the bipolar range. A $\overline{\text{CLR}}$ function is provided which sets the output to 0 V in both unipolar ranges and in the twos complement bipolar range, while with offset binary data format, the output is set to −REFIN. This function is useful as a power-on reset as it allows the outputs to be set to a known voltage level.

DACPORT is a registered trademark of Analog Devices, Inc.

The AD7249 features a serial interface which allows easy connection to both microcomputers and 16-bit digital signal processors with serial ports. The serial data may be applied at rates up to 2 MHz allowing a DAC update rate of 125 kHz.

The AD7249 is fabricated on linear compatible CMOS (LC²MOS), an advanced, mixed technology process. It is packaged in 16-pin DIP and 16-pin SOIC packages.

PRODUCT HIGHLIGHTS

1. Two complete 12-bit DACPORTs®
   The AD7249 contains two complete voltage output, 12-bit DACs in both 16-lead DIP and SOIC packages.
2. Single or dual supply operation
3. Minimum 3-wire interface to most DSP processors
4. DAC update rate—125 kHz

AD7249—SPECIFICATIONS (V_{DD} = +12 V to +15 V,[1] V_{SS} = 0 V or −12 V to −15 V,[1] AGND = DGND = 0 V, REFIN = +5 V, R_L = 2 kΩ, C_L = 100 pF to AGND All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version[2]	B Version[2]	S Version[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]	±5	±5	±6	LSB max	V_{SS} = 0 V or −12 V to −15 V[1]; DAC Latch Contents All 0s
Bipolar Zero Error[3]	±6	±5	±7	LSB max	V_{SS} = −12 V to −15 V[1] DAC Latch Contents All 0s
Full-Scale Error[3,4]	±6	±6	±7	LSB max	
Full-Scale Temperature Coefficient	±5	±5	±5	ppm of FSR/°C typ	
REFERENCE OUTPUT					
REFOUT	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	
Reference Temperature Coefficient	±25	±25	±30	ppm/°C typ	
Reference Load Change (ΔV_{REFOUT} vs. I_L)	−1	−1	−1	mV max	Reference Load Current (I_L) Change (0 μA–100 μA)
REFERENCE INPUT					
Reference Input Range, REFIN	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	5 V ± 1%
Input Current	5	5	5	μA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current					
I_{IN}	±1	±1	±1	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[5]	8	8	8	pF max	
ANALOG OUTPUTS					
Output Range Resistor, R_{OFSA} & R_{OFSB}	15/30	15/30	15/30	kΩ min/ max	
Output Voltage Ranges[6]	+5, +10	+5, +10	+5, +10	V	Single Supply; V_{SS} = 0 V
Output Voltage Ranges[6]	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5	V	Dual Supply; V_{SS} = −12 V or −15 V
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[5]					
Voltage Output Settling-Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	10	10	10	μs max	Typically 3 μs
Negative Full-Scale Change	10	10	10	μs max	Typically 5 μs. V_{SS} = −12 V to −15 V
	10	10	10	μs typ	V_{SS} = 0 V
Digital-to-Analog Glitch Impulse[3]	30	30	30	nV secs typ	DAC Latch Contents Toggled Between All 0s and All 1s
Digital Feedthrough[3]	10	10	10	nV secs typ	
Digital Crosstalk[3]	10	10	10	nV secs typ	
POWER REQUIREMENTS					
V_{DD} Range	+10.8/+16.5	+11.4/+15.75	+11.4/+15.75	V min/V max	For Specified Performance Unless Otherwise Stated
V_{SS} Range (Dual Supplies)	−10.8/−16.5	−11.4/−15.75	−11.4/−15.75	V min/V max	For Specified Performance Unless Otherwise Stated
I_{DD}	15	15	15	mA max	Output Unloaded; Typically 11 mA
I_{SS} (Dual Supplies)	5	5	5	mA max	Output Unloaded; Typically 3 mA

NOTES
[1]Power supply tolerance, A Version: ±10%; B, S Versions: ±5%.
[2]Temperature ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.
[3]See Terminology.
[4]Measured with respect to REFIN and includes unipolar/bipolar offset error.
[5]Guaranteed by design not production tested.
[6]0 V to 10 V output range available only with $V_{DD} \geq 14.25$ V.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2]

(V_{DD} = +12 V to +15 V,[3] V_{SS} = 0 V or −12 V to −15 V,[3] AGND = DGND = 0 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (All Versions)	Units	Conditions/Comments
t_1[4]	400	500	ns min	SCLK Cycle Time
t_2	50	50	ns min	$\overline{SYNC}$ to SCLK Falling Edge Setup Time
t_3	120	150	ns min	$\overline{SYNC}$ to SCLK Hold Time
t_4	10	10	ns min	Data Setup Time
t_5	170	225	ns min	Data Hold Time
t_6	0	0	ns min	$\overline{SYNC}$ High to $\overline{LDAC}$ Low
t_7	50	50	ns min	$\overline{LDAC}$ Pulse Width
t_8	0	0	ns min	$\overline{LDAC}$ High to $\overline{SYNC}$ Low
t_9	75	75	ns min	$\overline{CLR}$ Pulse Width
t_{10}	75	100	ns min	$\overline{SYNC}$ High Time

NOTES
[1]Timing specifications guaranteed by design not production tested. All input signals are specified with tr= tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figure 8.
[3]Power supply tolerance, A Version: ±10%; B, S Versions: ±5%.
[4]SCLK Mark/Space Ratio range is 45/55 to 55/45.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND, DGND . . . . . −0.3 V to +17 V
V_{SS} to AGND, DGND . . . . . +0.3 V to −17 V
AGND to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
$V_{OUTA, B}$[2] to AGND . . . . . V_{SS} − 0.3 V to V_{DD} + 0.3 V
REFOUT to AGND . . . . . 0 V to V_{DD}
REFIN to AGND . . . . . −0.3 V to V_{DD} + 0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Industrial (A, B Versions) . . . . . −40°C to +85°C
  Extended (S Version) . . . . . −55°C to +125°C
Junction Temperature . . . . . +150°C
Storage Temperature Range . . . . . −65°C to +150°C
Power Dissipation Plastic DIP . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . +117°C/W
  Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation, Cerdip . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 76°C/W
  Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation, SOIC . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 75°C/W
  Lead Temperature (Soldering)
    Vapor Phase (60 secs) . . . . . +215°C
    Infrared (15 secs) . . . . . +220°C

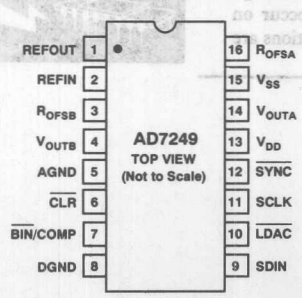
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability Only one Absolute Maximum Rating may be applied at any time.
[2]The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7249 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Pin	Mnemonic	Description
1	REFOUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part using its internal reference, REFOUT should be connected to REFIN.
2	REFIN	Voltage Reference Input. It is internally buffered before being applied to both DACs. The nominal reference voltage for specified operation of the AD7249 is 5 V.
3	R_{OFSB}	Output Offset Resistor for the amplifier of DAC B. It is connected to V_{OUTB} for the +5 V range, to AGND for the +10 V range and to REFIN for the −5 V to +5 V range.
4	V_{OUTB}	Analog Output Voltage of DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and −5 V to +5 V.
5	AGND	Analog Ground. Ground reference for all analog circuitry.
6	$\overline{CLR}$	Clear, Logic Input. Taking this input low clears both DACs. It sets V_{OUTA} and V_{OUTB} to 0 V in both unipolar ranges and the twos complement bipolar range and to −REFIN in the offset binary bipolar range.
7	$\overline{BIN}$/COMP	Logic Input. This input selects the data format to be either binary or twos complement. In both unipolar ranges natural binary format is selected by connecting this input to a Logic "0". In the bipolar configuration offset binary format is selected with a logic "0" while a Logic "1" selects twos complement.
8	DGND	Digital Ground. Ground reference for all digital circuitry.
9	SDIN	Serial Data In, Logic Input. The 16-bit serial data word is applied to this input.
10	$\overline{LDAC}$	Load DAC, Logic Input. Updates both DAC outputs. The DAC outputs are updated on the falling edge of this signal or alternatively if this line is permanently low, an automatic update mode is selected whereby both DACs are updated on the 16th falling SCLK pulse.
11	SCLK	Serial Clock, Logic Input. Data is clocked into the input register on each falling SCLK edge.
12	$\overline{SYNC}$	Data Synchronization Pulse, Logic Input. Taking this input low initializes the internal logic in readiness for a new data word.
13	V_{DD}	Positive Power Supply.
14	V_{OUTA}	Analog Output Voltage of DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and −5 V to +5 V.
15	V_{SS}	Negative Power Supply (used for the output amplifier only) may be connected to 0 V for single supply operation or −12 V to −15 V for dual supplies.
16	R_{OFSA}	Output Offset Resistor for the amplifier of DAC A. It is connected to V_{OUTA} for the +5 V range, to AGND for the +10 V range and to REFIN for the −5 V to +5 V range.

PIN CONFIGURATIONS (DIP and SOIC)



ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option[1]
AD7249AN	−40°C to +85°C	±1 LSB	N-16
AD7249BN	−40°C to +85°C	±1/2 LSB	N-16
AD7249AR	−40°C to +85°C	±1 LSB	R-16
AD7249BR	−40°C to +85°C	±1/2 LSB	R-16
AD7249SQ[2]	−55°C to +125°C	±1 LSB	Q-16

NOTES
[1]For outline information see Package Information section.
[2]Available to /883B processing only. Contact your local sales office for military data sheet.

TERMINOLOGY

Bipolar Zero Error
Bipolar Zero Error is the voltage measured at V_{OUT} when the DAC is configured for bipolar output and loaded with all 0s (Twos Complement Coding) or with 1000 0000 0000 (Offset Binary Coding). It is due to a combination of offset errors in the DAC, amplifier and mismatch between the internal gain resistors around the amplifier.

Full-Scale Error
Full-Scale Error is a measure of the output error when the amplifier output is at full scale (for the bipolar output range full scale is either positive or negative full scale). It is measured with respect to the reference input voltage and includes the offset errors.

Digital-to-Analog Glitch Impulse
This is the voltage spike that appears at V_{OUT} when the digital code in the DAC Latch changes, before the output settles to its final value. The energy in the glitch is specified in nV secs, and is measured for an all codes change from 0000 0000 0000 to 1111 1111 1111.

Digital Feedthrough
This is a measure of the voltage spike that appears on V_{OUT} as a result of feedthrough from the digital inputs on the AD7249. It is measured with $\overline{LDAC}$ held high.

Relative Accuracy (Linearity)
Relative Accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints of the transfer function. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

Single Supply Linearity and Gain Error
The output amplifier on the AD7249 can have true negative offsets even when the part is operated from a single +15 V supply. However, because the negative supply rail (V_{SS}) is 0 V, the output cannot actually go negative. Instead, when the output offset voltage is negative, the output voltage sits at 0 V, resulting in the transfer function shown in Figure 1.

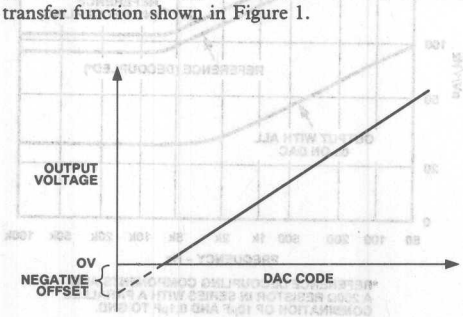


Figure 1. Effect of Negative Offset (Single Supply)

This "knee" is an offset effect, not a linearity error, and the transfer function would have followed the dotted line if the output voltage could have gone negative.

Normally, linearity is measured between zero (all 0s input code) and full scale (all 1s input code) after offset and full scale have been adjusted out or allowed for, but this is not possible in single supply operation if the offset is negative, due to the knee in the transfer function. Instead, linearity of the AD7249 in the unipolar mode is measured between full scale and the lowest code which is guaranteed to produce a positive output voltage. This code is calculated from the maximum specification for negative offset. For the A and B versions, the linearity is measured between Codes 3 and 4095. For the S grade, linearity is measured between Code 5 and Code 4095.

Differential Nonlinearity
Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

Unipolar Offset Error
Unipolar Offset Error is the measured output voltage from V_{OUT} with all zeros loaded into the DAC latch, when the DAC is configured for unipolar output. It is due to a combination of the offset errors in the DAC and output amplifier.

CIRCUIT INFORMATION

D/A Section
The AD7249 contains two 12-bit voltage-mode D/A converters consisting of highly stable thin film resistors and high-speed NMOS single-pole, double-throw switches. The simplified circuit diagram for the DAC section is shown in Figure 2. The output voltage from the converter has the same polarity as the reference voltage, REFIN, allowing single supply operation.

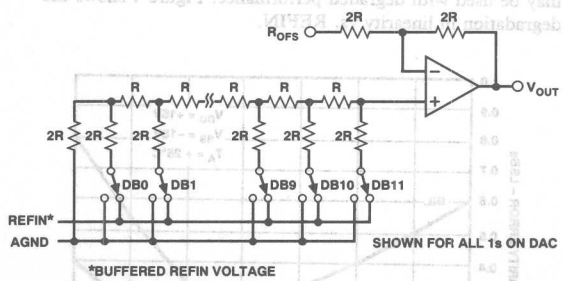


Figure 2. D/A Simplified Circuit Diagram

Internal Reference

The AD7249 has an on-chip temperature compensated buried Zener reference which is factory trimmed to 5 V ± 50 mV. The reference voltage is provided at the REFOUT pin. This reference can be used to provide the reference voltage for the D/A converter by connecting the REFOUT pin to the REFIN pin.

The reference voltage can also be used as a reference for other components and is capable of providing up to 500 μA to an external load. The maximum recommended capacitance on REFOUT for normal operation is 50 pF. If the reference output is required to drive a capacitive load greater than 50 pF, then a 200 Ω resistor should be placed in series with the capacitive load. Figure 3 shows the suggested REF OUT decoupling scheme, a 200 Ω resistor and the parallel combination of a 10 μF tantalum and a 0.1 μF ceramic capacitor. This decoupling scheme reduces the noise spectral density of the reference.

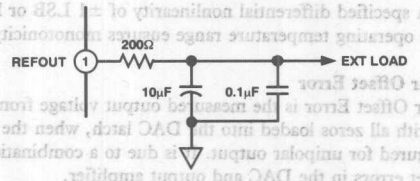


Figure 3. Reference Decoupling Scheme

External Reference

In some applications, the user may require a system reference or some other external reference to drive the AD7249. References such as the AD586 provide an ideal external reference source (See Figure 10). The REFIN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converter. The D/A converter is scaled for a 5 V reference and the device is tested with 5 V applied to REFIN. Other reference voltages may be used with degraded performance. Figure 4 shows the degradation in linearity vs. REFIN.

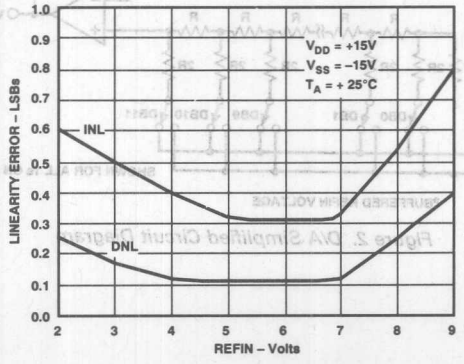


Figure 4. Linearity vs. REFIN Voltage

Op Amp Section

The output of the voltage-mode D/A converter is buffered by a noninverting CMOS amplifier. The R_{OFS} input allows three output voltage ranges to be selected. The buffer amplifier is capable of developing +10 V across a 2 kΩ load to AGND.

The output amplifier can be operated from a single +15 V supply by tying V_{SS} = 0 V.

The amplifier can also be operated from dual supplies to allow an additional bipolar output range of −5 V to +5 V. Dual supplies are necessary for the bipolar output range but can also be used for the unipolar ranges to give faster settling time to voltages near 0 V, to allow full sink capability of 2.5 mA over the entire output range and to eliminate the effects of negative offsets on the transfer characteristic (outlined previously). A plot of the output sink capability of the amplifier is shown in Figure 5.

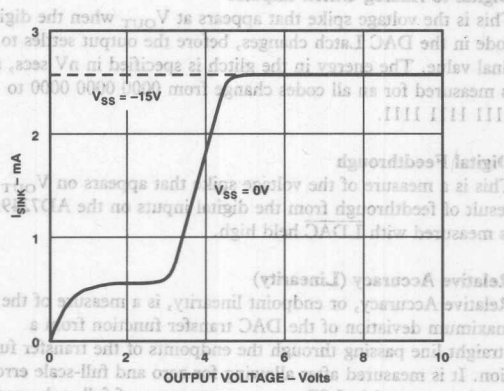


Figure 5. Amplifier Sink Current

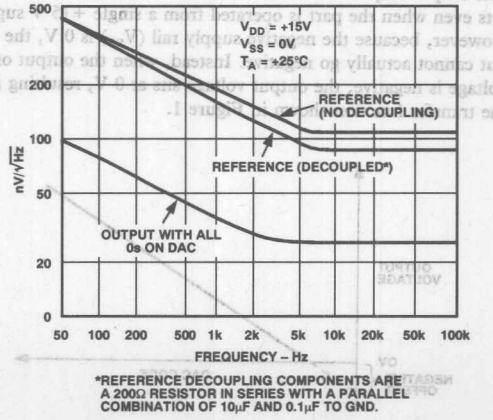


Figure 6. Noise Spectral Density vs. Frequency

DIGITAL INTERFACE

The AD7249 contains an input serial to parallel shift register and a DAC latch for both DAC A and DAC B. A simplified diagram of the input loading circuitry is shown in Figure 7. Serial data on the SDIN input is loaded to the input register under control of $\overline{SYNC}$ and SCLK. The $\overline{SYNC}$ input provides the frame synchronization signal which tells the AD7249 that valid serial data on the SDIN input will be available for the next 16 falling edges of SCLK. An internal counter/decoder circuit provides a low gating signal so that only 16 data bits are clocked into the input shift register. After 16 SCLK pulses the internal gating signal goes inactive (high) thus locking out any further clock pulses. Therefore either a continuous clock or a burst clock source may be used to clock in the data. The $\overline{SYNC}$ input is taken high after the complete 16-bit word is loaded in.

DAC selection is accomplished using the thirteenth bit (DB12) of the serial data input stream. A zero in DB12 will select DAC A while a one in this position selects DAC B. Although 16 bits of data are clocked into the input register, only 12 bits get transferred into the DAC latch. The relevant DAC latch is determined by the value of the thirteenth bit and the first three bits in the 16-bit stream are don't cares. Therefore, the data format is three don't cares followed by the DAC selection bit and the 12-bit data word with the LSB as the last bit in the serial stream.

There are two ways in which a DAC latches and hence the analog outputs may be updated. The status of the $\overline{LDAC}$ input is examined after $\overline{SYNC}$ is taken low. Depending on its status, one of two update modes are selected.

If $\overline{LDAC}$ = 0, then the automatic update mode is selected. In this mode the DAC latch and analog output are updated automatically when the last bit in the serial data stream is clocked in. The update thus takes place on the sixteenth falling SCLK edge.

If $\overline{LDAC}$ = 1, then the automatic update is disabled and both DAC latches are updated by taking $\overline{LDAC}$ low any time after the 16-bit data transfer is complete. The update now occurs on the falling edge of $\overline{LDAC}$. Note that the $\overline{LDAC}$ input must be taken back high again before the next data transfer is initiated. When a complete word is held in the shift register it may then be loaded into the DAC latch under control of $\overline{LDAC}$.

Clear Function ($\overline{CLR}$)

The clear function clears the contents of the input shift register and loads both DAC Latches with all 0s. It is activated by taking $\overline{CLR}$ low. In all ranges except the Offset Binary bipolar range (−5 V to +5 V) the output voltage is reset to 0 V. In the offset binary bipolar range the output is set to −REFIN. The clear function is especially useful at power-up as it enables the output to be reset to a known state.

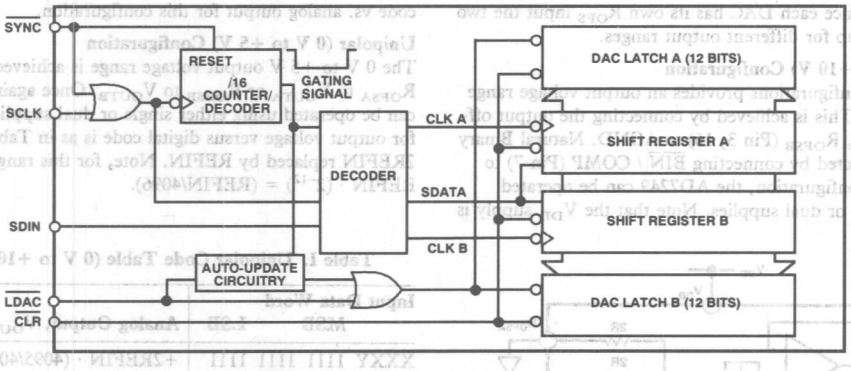


Figure 7. Simplified Loading Structure

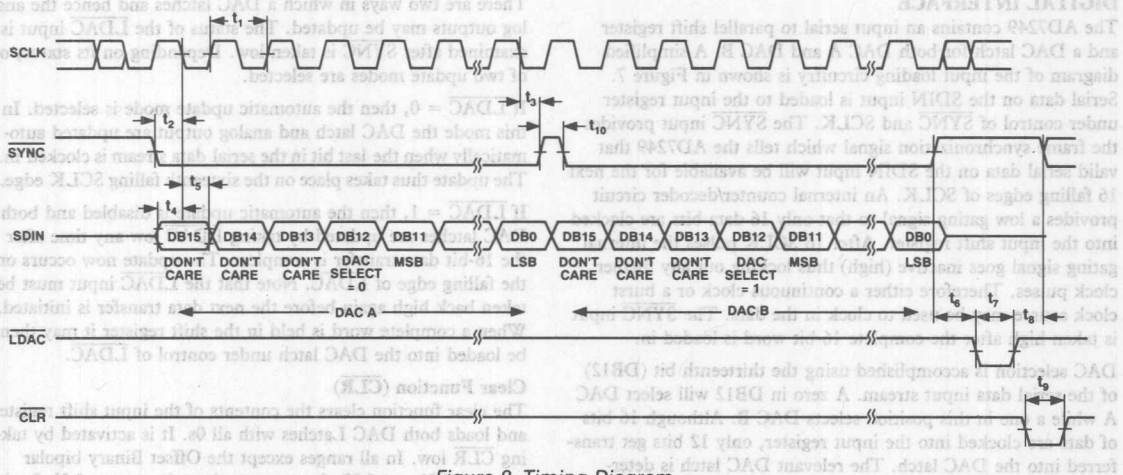


Figure 8. Timing Diagram

TRANSFER FUNCTION

The internal scaling resistors provided on the AD7249 allow several output voltage ranges. The part can produce unipolar output ranges of 0 V to +5 V or 0 V to +10 V and a bipolar output range of ±5 V. Connections for the various ranges are outlined below. Since each DAC has its own R_{OFS} input the two DACs can be set up for different output ranges.

Unipolar (0 V to +10 V) Configuration

The first of the configurations provides an output voltage range of 0 V to +10 V. This is achieved by connecting the output offset resistor R_{OFSA}, R_{OFSB} (Pin 3, 16) to AGND. Natural Binary data format is selected by connecting $\overline{BIN}$ / COMP (Pin 7) to DGND. In this configuration, the AD7249 can be operated using either single or dual supplies. Note that the V_{DD} supply is restricted to +15 V ± 10% for this range in order to maintain sufficient amplifier headroom. Dual supplies may be used to improve settling time and give increased current sink capability for the amplifier. Figure 9 shows the connection diagram for unipolar operation of the AD7249. Table I shows the digital code vs. analog output for this configuration.

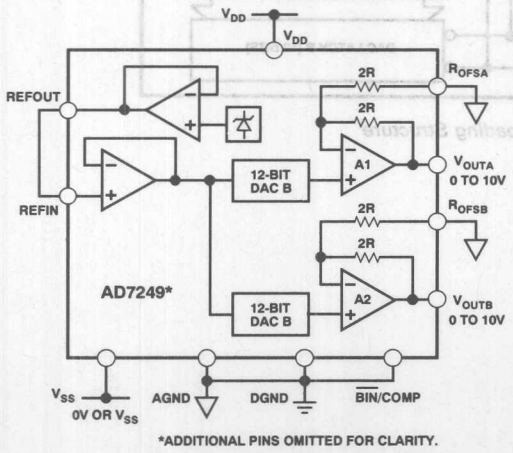


Figure 9. Unipolar (0 V to +10 V) Configuration

Unipolar (0 V to +5 V) Configuration

The 0 V to +5 V output voltage range is achieved by tying R_{OFSA} to V_{OUTA} or R_{OFSB} to V_{OUTB}. Once again, the AD7249 can be operated using either single or dual supplies. The table for output voltage versus digital code is as in Table I, with 2REFIN replaced by REFIN. Note, for this range, 1 LSB = REFIN · (2^{-12}) = (REFIN/4096).

Table I. Unipolar Code Table (0 V to +10 V Range)

Input Data Word MSB LSB	Analog Output, V_{OUT}
XXXY 1111 1111 1111	+2REFIN · (4095/4096)
XXXY 1000 0000 0001	+2REFIN · (2049/4096)
XXXY 1000 0000 0000	+2REFIN · (2048/4096) = +REFIN
XXXY 0111 1111 1111	+2REFIN · (2047/4096)
XXXY 0000 0000 0001	+2REFIN · (1/4096)
XXXY 0000 0000 0000	0 V

X = Don't Care.
Y = DAC Select Bit, 0 = DACA, 1= DACB.
Note: 1 LSB = 2REFIN/4096.

Bipolar (±5 V) Configuration

The bipolar configuration for the AD7249, which gives an output range of −5 V to +5 V, is achieved by connecting R_{OFSA}, R_{OFSB} to V_{REFIN}. The AD7249 must be operated from dual supplies to achieve this output voltage range. Either offset binary or twos complement coding may be selected. Figure 10 shows the connection diagram for bipolar operation. An AD586 provides the reference voltage for the DAC but this could be provided by the on-chip reference by connecting REFOUT to REFIN.

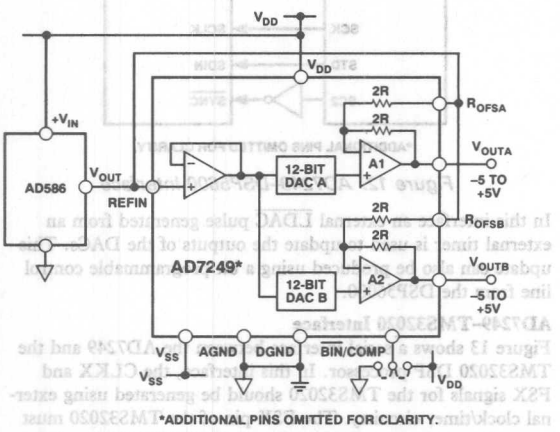


Figure 10. Bipolar Configuration with External Reference

Bipolar Operation (Twos Complement Data Format)

The AD7249 is configured for twos complement data format by connecting $\overline{BIN}$/COMP (Pin 7) high. The analog output vs. digital code is shown in Table II.

Table II. Twos Complement Bipolar Code Table

Input Data Word MSB LSB	Analog Output, V_{OUT}
XXXY 0111 1111 1111	+REFIN · (2047/2048)
XXXY 0000 0000 0001	+REFIN · (1/2048)
XXXY 0000 0000 0000	0 V
XXXY 1111 1111 1111	−REFIN · (1/2048)
XXXY 1000 0000 0001	−REFIN · (2047/2048)
XXXY 1000 0000 0000	−REFIN · (2048/2048)=−REFIN

X = Don't Care.
Y = DAC Select Bit, 0 = DACA, 1 = DACB.
Note: 1 LSB = REFIN/2048.

Bipolar Operation (Offset Binary Data Format)

The AD7249 is configured for Offset Binary data format by connecting $\overline{BIN}$/COMP (Pin 7) low. The analog output vs. digital code may be obtained by inverting the MSB in Table II.

APPLYING THE AD7249

Good printed circuit board layout is as important as the overall circuit design itself in achieving high speed converter performance. The AD7249 works on an LSB size of 2.44 mV for the unipolar 0 V to 10 V range and the bipolar ±5 V range, when using the unipolar 0 V to 5 V range the LSB size is 1.22 mV. Therefore the designer must be conscious of minimizing noise in both the converter itself and in the surrounding circuitry. Switching mode power supplies are not recommended as switching spikes can feedthrough to the on-chip amplifier. Other causes of concern are ground loops and feedthrough from microprocessors. These are factors which influence any high performance converter, and proper printed circuit board layout which minimizes these effects is essential to obtain high performance.

LAYOUT HINTS

Ensure that the layout has the digital and analog tracks separated as much as possible. Take care not to run any digital track alongside an analog signal track. Establish a single point analog ground separate from the logic system ground. Place this star ground as close as possible to the AD7249. Connect all analog grounds to this star point and also connect the AD7249 DGND pin to this point. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential for low noise operation of high performance converters. To accomplish this track widths should be kept a wide as possible and also the use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise.

NOISE

Keep the signal leads on the V_{OUTA} and V_{OUTB} signals and the signal return leads to AGND as short as possible to minimize noise coupling. In applications where this is not possible use a shielded cable between the DAC outputs and their destination. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the DAC and its destination device appears as an error voltage in series with the DAC output.

Power Supply Decoupling

To achieve optimum performance when using the AD7249, the V_{DD} and V_{SS} lines should be decoupled to AGND using 0.1 μF capacitors. In noisy environments it is recommended that 10 μF capacitors be connected in parallel with the 0.1 μF capacitors.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD7249 is via a serial bus which uses standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a three-wire interface consisting of a clock signal, a data signal and a synchronization signal. The AD7249 requires a 16-bit data word with data valid on the falling edge of SCLK. For all the interfaces, the DAC update may be done automatically when all the data is clocked in or it may be done under control of $\overline{\text{LDAC}}$.

Figures 11 to 15 show the AD7249 configured for interfacing to a number of popular DSP processors and microcontrollers.

AD7249–ADSP-2101/ADSP-2102 Interface

Figure 11 shows a serial interface between the AD7249 and the ADSP-2101/ ADSP-2102 DSP processor. The ADSP-2101/ ADSP-2102 contains two serial ports and either port may be used in the interface. The data transfer is initiated by $\overline{\text{TFS}}$ going low. Data from the ADSP-2101/ADSP-2102 is clocked into the AD7249 on the falling edge of SCLK. DB12 of the 16-bit serial data stream selects the DAC to be updated. Both DACs can be updated by holding $\overline{\text{LDAC}}$ high while performing two write cycles to the DAC. $\overline{\text{TFS}}$ must be taken high after each 16 bit write cycle. $\overline{\text{LDAC}}$ is brought low at the end of the second cycle and both DAC outputs are updated together. In the interface shown the DAC is updated using an external timer

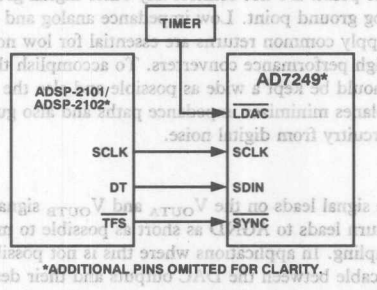


Figure 11. AD7249–ADSP-2101/ADSP-2102 Interface

which generates an $\overline{\text{LDAC}}$ pulse. This could also be done using a control or decoded address line from the processor. Alternatively, if the $\overline{\text{LDAC}}$ input is hardwired low the output update takes place automatically on the 16th falling edge of SCLK.

AD7249–DSP56000 Interface

A serial interface between the AD7249 and the DSP56000 is shown in Figure 12. The DSP56000 is configured for Normal Mode Asynchronous operation with Gated Clock. It is also set up for a 16-bit word with SCK and SC2 as outputs and the FSL control bit set to a "0." SCK is internally generated on the DSP56000 and applied to the AD7249 SCLK input. Data from the DSP56000 is valid on the falling edge of SCK. The SC2 output provides the framing pulse for valid data. This line must be inverted before being applied to the $\overline{\text{SYNC}}$ input of the AD7249.

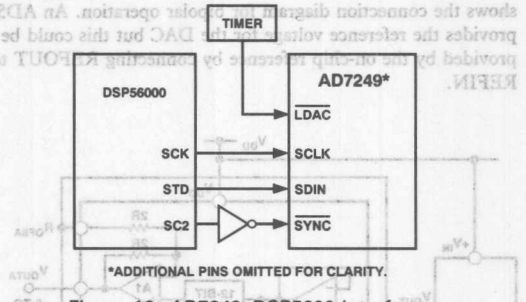


Figure 12. AD7249–DSP5600 Interface

In this interface an external $\overline{\text{LDAC}}$ pulse generated from an external timer is used to update the outputs of the DACs. This update can also be produced using a bit programmable control line from the DSP56000.

AD7249–TMS32020 Interface

Figure 13 shows a serial interface between the AD7249 and the TMS32020 DSP processor. In this interface, the CLKX and FSX signals for the TMS32020 should be generated using external clock/timer circuitry. The FSX pin of the TMS32020 must be configured as an input. Data from the TMS32020 is valid on the falling edge of CLKX.

The clock/timer circuitry generates the $\overline{\text{LDAC}}$ signal for the AD7249 to synchronize the update of the output with the serial transmission. Alternatively, the automatic update mode may be selected by connecting $\overline{\text{LDAC}}$ to DGND.

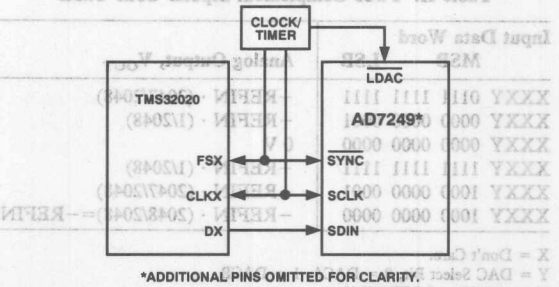


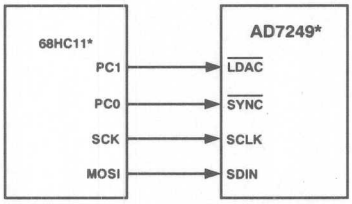
Figure 13. AD7249–TMS32020 Interface

AD7249–68HC11 Interface

Figure 14 shows a serial interface between the AD7249 and the 68HC11 microcontroller. SCK of the 68HC11 drives SCLK of the AD7249 while the MOSI output drives the serial data line of the AD7249. The $\overline{SYNC}$ signal is derived from a port line (PC0 shown).

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 0 and its CPHA bit is a 1. When data is to be transmitted to the part, PC0 is taken low. When the 68HC11 is configured like this, data on MOSI is valid on the falling edge of SCK. The 68HC11 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7249, PC0 is left low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7249. When the second serial transfer is complete, the PC0 line is taken high.

Figure 14 shows the $\overline{LDAC}$ input of the AD7249 being driven from another bit programmable port line (PC1). As a result, both DACs can be updated simultaneously by taking $\overline{LDAC}$ low after both DACs latches have updated.



*ADDITIONAL PINS OMITTED FOR CLARITY.

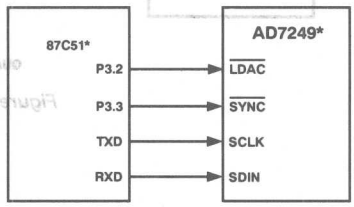
Figure 14. AD7249–68HC11 Interface

AD7249–87C51 Interface

A serial interface between the AD7249 and the 87C51 microcontroller is shown in Figure 15. TXD of the 87C51 drives SCLK of the AD7249 while RXD drives the serial data line of the part. The $\overline{SYNC}$ signal is derived from the port line P3.3 and the $\overline{LDAC}$ line is driven port line P3.2.

The 87C51 provides the LSB of its SBUF register as the first bit in the serial data stream. Therefore, the user will have to ensure that the data in the SBUF register is arranged correctly so that the don't care bits are the first to be transmitted to the AD7249 and the last bit to be sent is the LSB of the word to be loaded to the AD7249. When data is to be transmitted to the part, P3.3 is taken low. Data on RXD is valid on the falling edge of TXD. The 87C51 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7249, P3.3 is left low after the first eight bits are transferred, and a second byte of data is then transferred serially to the AD7249 with DB12 used to select the appropriate DAC register. When the second serial transfer is complete, the P3.3 line is taken high and then taken low again to start the loading sequence to the second DAC (see timing diagram Figure 8).

Figure 15 shows the $\overline{LDAC}$ input of the AD7249 driven from the bit programmable port line P3.2. As a result, both DAC outputs can be updated simultaneously by taking the $\overline{LDAC}$ line low following the completion of the write cycle to the second DAC. Alternatively $\overline{LDAC}$ could be hardwired low and the analog output will be updated on the sixteenth falling edge of TXD after the $\overline{SYNC}$ signal for the DAC has gone low.



*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 15. AD7249–87C51 Interface

APPLICATIONS

OPTO-ISOLATED INTERFACE

In many process control type applications it is necessary to provide an isolation barrier between the controller and the unit being controlled. Opto-isolators can provide voltage isolation in excess of 3 kΩ. The serial loading structure of the AD7249 makes it ideal for opto-isolated interfaces as the number of interface lines is kept to a minimum.

Figure 16 shows a 2-channel isolated interface using the AD7249.

The sequence of events to program the output channels is as follows.

1. Take the $\overline{SYNC}$ line low.
2. Transmit the 16-bit word for DAC A (DB 12 of the 16 bit data word selects the DAC, DB12 = 0 to select DAC A) and bring the $\overline{SYNC}$ line high after the 16 bits have been transmitted.
3. Bring $\overline{SYNC}$ line low again and transmit 16 bits for DAC B, bring $\overline{SYNC}$ back high at end of transmission.
4. Pulse the $\overline{LDAC}$ line low. This updates both output channels simultaneously on the falling edge of $\overline{LDAC}$.

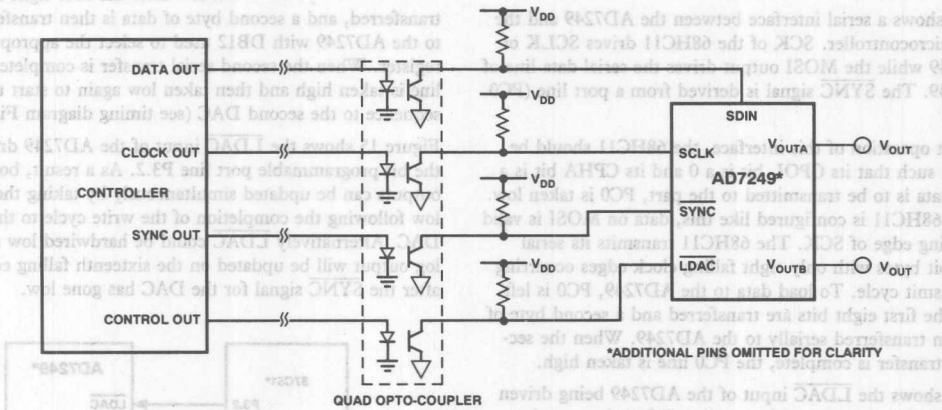


Figure 16. Opto-Isolated Interface

CMOS 8-Bit Buffered Multiplying DAC

AD7524

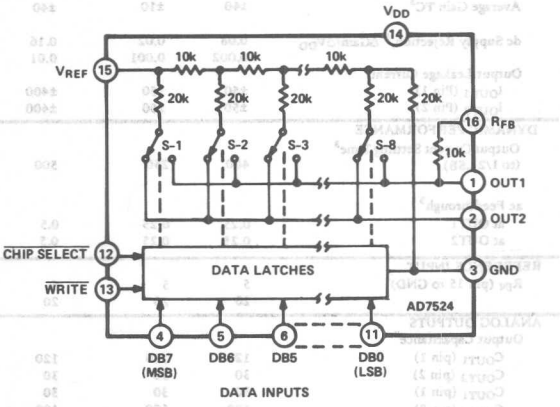
FEATURES

- Microprocessor Compatible (6800, 8085, Z80, etc.)
- TTL/CMOS Compatible Inputs
- On-Chip Data Latches
- End Point Linearity
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)
- Latch Free (No Protection Schottky Required)

APPLICATIONS

- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits
- Bus Structured Instruments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7524 is a low cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

Basically an 8-bit DAC with input latches, the AD7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the AD7524 provides accuracy to 1/8LSB with a typical power dissipation of less than 10 milliwatts.

A newly improved design eliminates the protection Schottky previously required and guarantees TTL compatibility when using a +5V supply. Loading speed has been increased for compatibility with most microprocessors.

Featuring operation from +5V to +15V, the AD7524 interfaces directly to most microprocessor buses or output ports.

Excellent multiplying characteristics (2- or 4-quadrant) make the AD7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

ORDERING GUIDE

Model[1]	Temperature Range	Nonlinearity (V_{DD} = +15V)	Package Option[2]
AD7524JN	−40°C to +85°C	±1/2LSB	N-16
AD7524KN	−40°C to +85°C	±1/4LSB	N-16
AD7524LN	−40°C to +85°C	±1/8LSB	N-16
AD7524JP	−40°C to +85°C	±1/2LSB	P-20A
AD7524KP	−40°C to +85°C	±1/4LSB	P-20A
AD7524LP	−40°C to +85°C	±1/8LSB	P-20A
AD7524JR	−40°C to +85°C	±1/2LSB	R-16A
AD7524AQ	−40°C to +85°C	±1/2LSB	Q-16
AD7524BQ	−40°C to +85°C	±1/4LSB	Q-16
AD7524CQ	−40°C to +85°C	±1/8LSB	Q-16
AD7524SQ	−55°C to +125°C	±1/2LSB	Q-16
AD7524TQ	−55°C to +125°C	±1/4LSB	Q-16
AD7524UQ	−55°C to +125°C	±1/8LSB	Q-16
AD7524SE	−55°C to +125°C	±1/2LSB	E-20A
AD7524TE	−55°C to +125°C	±1/4LSB	E-20A
AD7524UE	−55°C to +125°C	±1/8LSB	E-20A

NOTES

[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC drawing #5962-87700.

[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7524—SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, unless otherwise noted)

PARAMETER	LIMIT, T_A = +25°C V_{DD} = +5V	LIMIT, T_A = +25°C V_{DD} = +15V	LIMIT, T_{MIN}, T_{MAX}[1] V_{DD} = 5V	LIMIT, T_{MIN}, T_{MAX}[1] V_{DD} = +15V	UNITS	TEST CONDITIONS/COMMENTS
STATIC PERFORMANCE						
Resolution		8	8	8	Bits	
Relative Accuracy						
J, A, S Versions	±1/2	±1/2	±1/2	±1/2	LSB max	
K, B, T Versions	±1/2	±1/4	±1/2	±1/4	LSB max	
L, C, U Versions	±1/2	±1/8	±1/2	±1/8	LSB max	
Monotonicity	guaranteed	guaranteed	guaranteed	guaranteed		
Gain Error[2]	±2 1/2	±1 1/4	±3 1/2	±1 1/2	LSB max	
Average Gain TC[3]	±40	±10	±40	±10	ppm/°C	Gain TC measured from +25°C to T_{min} or from +25°C to T_{max}
dc Supply Rejection,[3] $\Delta Gain/\Delta V_{DD}$	0.08	0.02	0.16	0.04	% FSR/% max	ΔV_{DD} = ±10%
	0.002	0.001	0.01	0.005	% FSR/% typ	
Output Leakage Current						
I_{OUT1} (Pin 1)	±50	±50	±400	±200	nA max	DB0–DB7 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V; V_{REF} = ±10V
I_{OUT2} (Pin 2)	±50	±50	±400	±200	nA max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V; V_{REF} = ±10V
DYNAMIC PERFORMANCE						
Output Current Settling Time[3] (to 1/2 LSB)	400	250	500	350	ns max	OUT1 Load = 100Ω, C_{EXT} = 13pF; $\overline{WR}$, $\overline{CS}$ = 0V; DB0–DB7 = 0V to V_{DD} to 0V.
ac Feedthrough[3]						
at OUT1	0.25	0.25	0.5	0.5	% FSR max	V_{REF} = ±10V, 100kHz sine wave; DB0–DB7 =
at OUT2	0.25	0.25	0.5	0.5	% FSR max	0V; $\overline{WR}$, $\overline{CS}$ = 0V
REFERENCE INPUT						
R_{IN} (pin 15 to GND)[4]	5	5	5	5	kΩ min	
	20	20	20	20	kΩ max	
ANALOG OUTPUTS						
Output Capacitance[3]						
C_{OUT1} (pin 1)	120	120	120	120	pF max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT2} (pin 2)	30	30	30	30	pF max	
C_{OUT1} (pin 1)	30	30	30	30	pF max	DB0–DB7 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT2} (pin 2)	120	120	120	120	pF max	
DIGITAL INPUTS						
Input HIGH Voltage Requirement						
V_{IH}	+2.4	+13.5	+2.4	+13.5	V min	
Input LOW Voltage Requirement						
V_{IL}	+0.8	+1.5	+0.8	+1.5	V max	
Input Current						
I_{IN}	±1	±1	±10	±10	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]						
DB0–DB7	5	5	5	5	pF max	V_{IN} = 0V
$\overline{WR}$, $\overline{CS}$	20	20	20	20	pF max	V_{IN} = 0V
SWITCHING CHARACTERISTICS						
Chip Select to Write Setup Time[5]						See timing diagram.
t_{CS}						t_{WR} = t_{CS}
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Chip Select to Write Hold Time						
t_{CH}						
All Grades	0	0	0	0	ns min	
Write Pulse Width						
t_{WR}						$t_{CS} \geq t_{WR}, t_{CH} \geq 0$
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Data Setup Time						
t_{DS}						
AD7524J, K, L, A, B, C	135	60	170	80	ns min	
AD7524S, T, U	135	60	170	100	ns min	
Data Hold Time						
t_{DH}						
All Grades	10	10	10	10	ns min	
POWER SUPPLY						
I_{DD}	1	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	100	100	500	500	μA max	All Digital Inputs 0V or V_{DD}

NOTES
[1]Temperate ranges as follows: J, K, L versions: −40°C to +85°C
A, B, C versions: −40°C to +85°C
S, T, U versions: −55°C to +125°C
[2]Gain error is measured using internal feedback resistor. Full Scale Range (FRS) = V_{REF}.
[3]Guaranteed, not tested.
[4]DAC thin-film resistor temperature coefficient is approximately −300ppm/°C.
[5]AC parameter, sample tested @ 25°C to ensure conformance to specifications.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C, unless otherwise noted)

V_{DD} to GND	−0.3V, +17V
V_{RFB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage to GND	−0.3V to V_{DD} +0.3V
OUT1, OUT2 to GND	−0.3V to V_{DD} +0.3V
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above 75°C by	6mW/°C
Operating Temperature	
Commerical (J, K, L)	−40°C to +85°C
Industrial (A, B, C)	−40°C to +85°C
Extended (S, T, U)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY: A measure of the deviation from a straight line through the end points of the DAC transfer function. Normally expressed as a percentage of full scale range. For the AD7524 DAC, this holds true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

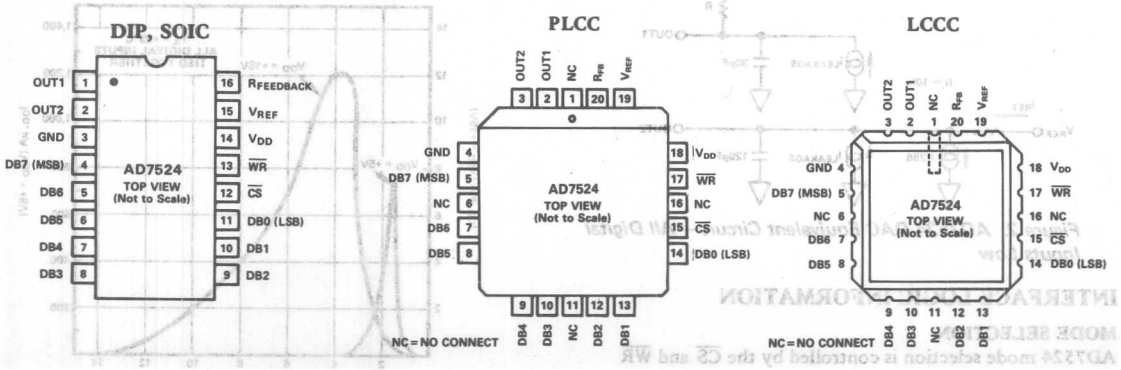
GAIN ERROR: Gain Error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in LSBs. Gain Error is adjustable to zero with an external potentiometer.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from OUT1 and OUT2 terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on OUT1 terminal with all digital inputs LOW or on OUT2 terminal when all inputs are HIGH. This is an error current which contributes an offset voltage at the amplifier output.

PIN CONFIGURATIONS



CIRCUIT DESCRIPTION

CIRCUIT INFORMATION

The AD7524, an 8-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and eight N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

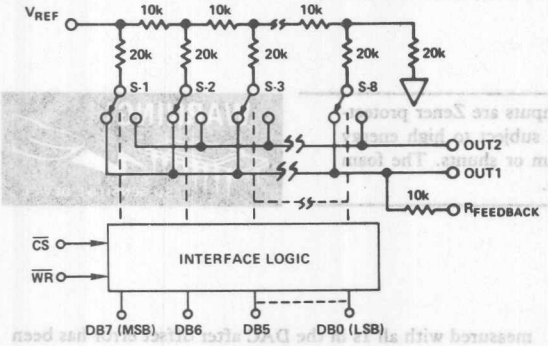


Figure 1. AD7524 Functional Diagram

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuit for all digital inputs LOW is shown in Figures 2. In Figure 2 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{1}{256}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switches is 120pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 30pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs high is similar to Figure 2 however, the "ON" switches are now on terminal OUT1, hence the 120pF appears at that terminal.

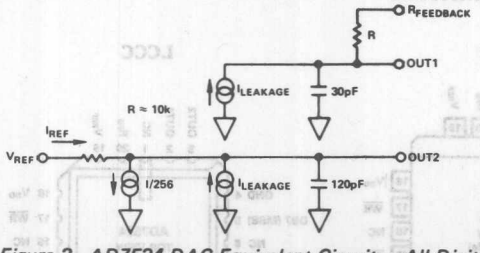


Figure 2. AD7524 DAC Equivalent Circuit – All Digital Inputs Low

INTERFACE LOGIC INFORMATION

MODE SELECTION

AD7524 mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

WRITE MODE

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the AD7524 is in the WRITE mode, and the AD7524 analog output responds to data activity at the DB0–DB7 data bus inputs. In this mode, the AD7524 acts like a nonlatched input D/A converter.

HOLD MODE

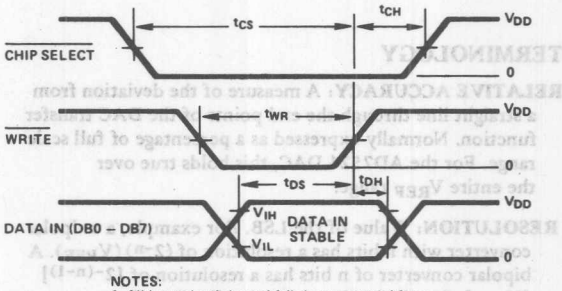
When either $\overline{CS}$ or $\overline{WR}$ is HIGH, the AD7524 is in the HOLD mode. The AD7524 analog output holds the value corresponding to the last digital input present at DB0–DB7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the HIGH state.

MODE SELECTION TABLE

$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	Write	DAC responds to data bus (DB0 – DB7) inputs
H	X	Hold	Data bus (DB0 – DB7) is locked out;
X	H	Hold	DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed HIGH state.

L = Low State, H = High State, X = Don't Care.

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. All input signal rise and fall times measured from 10% to 90% of V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. Timing Measurement Reference level is $\frac{V_{IH} + V_{IL}}{2}$
3. $t_{DS} + t_{DH}$ is approximately constant at 145ns min at +25°C, V_{DD} = +5V and t_{WR} = 170ns min. The AD7524 is specified for a minimum t_{DH} of 10ns, however, in applications where $t_{DH} > 10$ns, t_{DS} may be reduced accordingly up to the limit t_{DS} = 65ns, t_{DH} = 80ns.

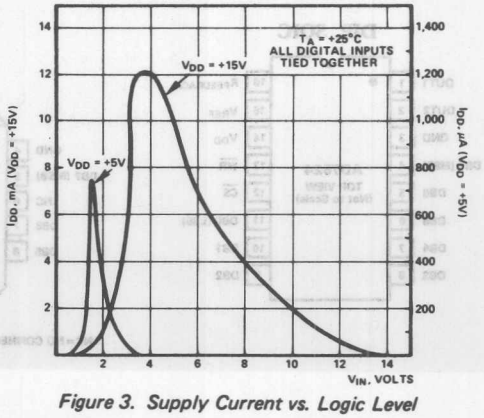


Figure 3. Supply Current vs. Logic Level

Typical plots of supply current, I_{DD}, versus logic input voltage, V_{IN}, for V_{DD} = +5V and V_{DD} = +15V are shown above.

CMOS Dual 8-Bit Buffered Multiplying DAC

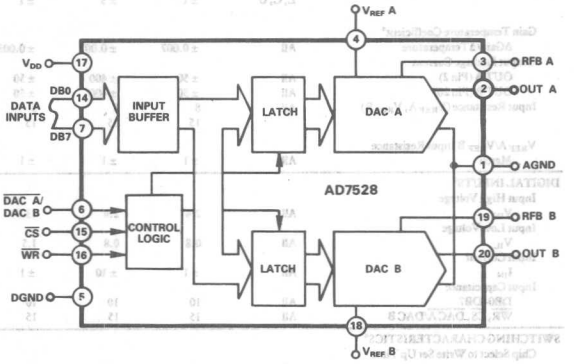
AD7528

FEATURES
- On-Chip Latches for Both DACs
- +5V to +15V Operation
- DACs Matched to 1%
- Four Quadrant Multiplication
- TTL/CMOS Compatible
- Latch Free (Protection Schottkys not Required)

APPLICATIONS

Digital Control of:
- Gain/Attenuation
- Filter Parameters
- Stereo Audio Circuits
- X–Y Graphics

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7528 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in skinny 0.3" wide 20-pin DIPs and in 20-terminal surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The AD7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5V to +15V power supply, dissipating only 20mW of power.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

1. DAC to DAC matching: since both of the AD7528 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7528's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A}}$/DAC B select line has allowed the AD7528 to be packaged in either a small 20-pin DIP, SOIC, PLCC or LCCC.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

STATIC PERFORMANCE[2]							
Resolution	All	8	8	8	8	Bits	
Relative Accuracy	J, A, S	±1	±1	±1	±1	LSB max	This is an Endpoint Linearity Specification
	K, B, T	±½	±½	±½	±½	LSB max	
	L, C, U	±½	±½	±½	±½	LSB max	
Differential Nonlinearity	All	±1	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	J, A, S	±4	±6	±4	±5	LSB max	Measured Using Internal RFB A and RFB B.
	K, B, T	±2	±4	±2	±3	LSB max	Both DAC Latches Loaded with 11111111.
	L, C, U	±1	±3	±1	±1	LSB max	Gain Error is Adjustable Using Circuits of Figures 4 and 5.
Gain Temperature Coefficient[4]							
ΔGain/ΔTemperature	All	±0.007	±0.007	±0.0035	±0.0035	%/°C max	
Output Leakage Current							
OUT A (Pin 2)	All	±50	±400	±50	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	All	±50	±400	±50	±200	nA max	
Input Resistance (V_{REF} A, V_{REF} B)	All	8	8	8	8	kΩ min	Input Resistance TC = −300ppm/°C, Typical
		15	15	15	15	kΩ max	Input Resistance is 11kΩ
V_{REF} A/V_{REF} B Input Resistance Match	All	±1	±1	±1	±1	% max	
DIGITAL INPUTS[3]							
Input High Voltage							
V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage							
V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current							
I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance							
DB0–DB7	All	10	10	10	10	pF max	
$\overline{WR}$, $\overline{CS}$, DAC A/DAC B	All	15	15	15	15	pF max	
SWITCHING CHARACTERISTICS[4]							See Timing Diagram
Chip Select to Write Set Up Time							
t_{CS}	All	200	230	60	80	ns min	
Chip Select to Write Hold Time							
t_{CH}	All	20	30	10	15	ns min	
DAC Select to Write Set Up Time							
t_{AS}	All	200	230	60	80	ns min	
DAC Select to Write Hold Time							
t_{AH}	All	20	30	10	15	ns min	
Data Valid to Write Set Up Time							
t_{DS}	All	110	130	30	40	ns min	
Data Valid to Write Hold Time							
t_{DH}	All	0	0	0	0	ns min	
Write Pulse Width							
t_{WR}	All	180	200	60	80	ns min	
POWER SUPPLY							See Figure 3
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	All	100	500	100	500	μA max	All Digital Inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS[5] (Measured Using Recommended P.C. Board Layout (Figure 7) and AD644 as Output Amplifiers)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{min}, T_{max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{min}, T_{max}	Units	Test Conditions/Comments
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	All	0.02	0.04	0.01	0.02	% per % max	ΔV_{DD} = ±5%
CURRENT SETTLING TIME[2]	All	350	400	180	200	ns max	To 1/2LSB. Out A/Out B load = 100Ω. $\overline{WR}$ = $\overline{CS}$ = 0V. DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
PROPAGATION DELAY (From Digital Input to 90% of Final Analog Output Current)	All	220	270	80	100	ns max	V_{REF} A = V_{REF} B = +10V OUT A, OUT B Load = 100Ω C_{EXT} = 13pF $\overline{WR}$, $\overline{CS}$ = 0V DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
DIGITAL TO ANALOG GLITCH IMPULSE	All	160	–	440	–	nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE							
C_{OUT} A	All	50	50	50	50	pF max	DAC Latches Loaded with 00000000
C_{OUT} B		50	50	50	50	pF max	
C_{OUT} A		120	120	120	120	pF max	DAC Latches Loaded with 11111111
C_{OUT} B		120	120	120	120	pF max	
AC FEEDTHROUGH[6]							
V_{REF} A to OUT A	All	−70	−65	−70	−65	dB max	V_{REF} A, V_{REF} B = 20V p-p Sine Wave
V_{REF} B to OUT B		−70	−65	−70	−65	dB max	@ 100kHz
CHANNEL TO CHANNEL ISOLATION							Both DAC Latches Loaded with 11111111.
V_{REF} A to OUT B	All	−77	–	−77	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 100kHz V_{REF} B = 0V see Figure 6.
V_{REF} B to OUT A		−77	–	−77	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 100kHz V_{REF} A = 0V see Figure 6.
DIGITAL CROSSTALK	All	30	–	60	–	nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	All	−85	–	−85	–	dB typ	V_{IN} = 6V rms @ 1kHz

NOTES
[1]Temperature Ranges are J, K, L Versions: −40°C to +85°C
A, B, C Versions: −40°C to +85°C
S, T, U Versions: −55°C to +125°C
[2]Specification applies to both DACs in AD7528.
[3]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1nA.
[4]Guaranteed by design but not production tested.
[5]These characteristics are for design guidance only and are not subject to test.
[6]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	V_{DD} +0.3V
DGND to AGND	V_{DD} +0.3V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{PIN2}, V_{PIN20} to AGND	−0.3V, V_{DD} +0.3V
V_{REF} A, V_{REF} B to AGND	±25V
V_{RFB} A, V_{RFB} B to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (J, K, L) Grades	−40°C to +85°C
Industrial (A, B, C) Grades	−40°C to +85°C
Extended (S, T, U) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs.)	+300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

TERMINOLOGY

Relative Accuracy:
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full scale reading.

Differential Nonlinearity:
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

Gain Error:
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the AD7528, ideal maximum output is V_{REF} − 1LSB. Gain error of both DACs is adjustable to zero with external resistance.

Output Capacitance:
Capacitance from OUT A or OUT B to AGND.

Digital to Analog Glitch Impulse:
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{REF} A, V_{REF} B = AGND.

Propagation Delay:
This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

Channel-to-Channel Isolation:
The proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

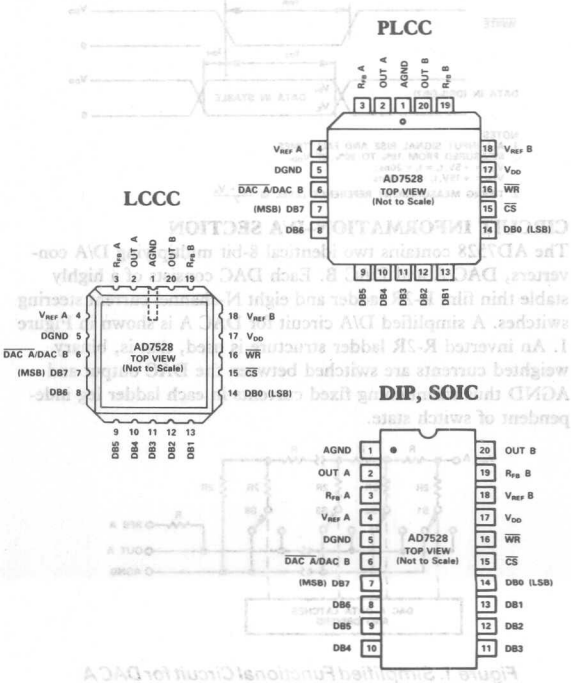
Digital Crosstalk:
The glitch energy transferred to the output of one converter due to a change in digital input code to the other converter. Specified in nV secs.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7528JN	−40°C to +85°C	±1LSB	±4LSB	N-20
AD7528KN	−40°C to +85°C	±1/2LSB	±2LSB	N-20
AD7528LN	−40°C to +85°C	±1/2LSB	±1LSB	N-20
AD7528JP	−40°C to +85°C	±1LSB	±4LSB	P-20A
AD7528KP	−40°C to +85°C	±1/2LSB	±2LSB	P-20A
AD7528LP	−40°C to +85°C	±1/2LSB	±1LSB	P-20A
AD7528JR	−40°C to +85°C	±1LSB	±4LSB	R-20
AD7528KR	−40°C to +85°C	±1/2LSB	±2LSB	R-20
AD7528LR	−40°C to +85°C	±1/2LSB	±1LSB	R-20
AD7528AQ	−40°C to +85°C	±1LSB	±4LSB	Q-20
AD7528BQ	−40°C to +85°C	±1/2LSB	±2LSB	Q-20
AD7528CQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-20
AD7528SQ	−55°C to +125°C	±1LSB	±4LSB	Q-20
AD7528TQ	−55°C to +125°C	±1/2LSB	±2LSB	Q-20
AD7528UQ	−55°C to +125°C	±1/2LSB	±1LSB	Q-20
AD7528SE	−55°C to +125°C	±1LSB	±4LSB	E-20A
AD7528TE	−55°C to +125°C	±1/2LSB	±2LSB	E-20A
AD7528UE	−55°C to +125°C	±1/2LSB	±1LSB	E-20A

NOTES
[1]Analog Devices reserves the right to ship side-brazed ceramic in lieu of cerdip. Parts will be marked with cerdip designator "Q."
[2]Processing to MIL-STD-883C, Class B is available. To order, add suffix "/883B" to part number. For further information, see Analog Devices' 1990 Military Products Databook.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

PIN CONFIGURATIONS



INTERFACE LOGIC INFORMATION

DAC Selection:

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

Mode Selection:

Inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode:

When $\overline{CS}$ and $\overline{WR}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

Hold Mode:

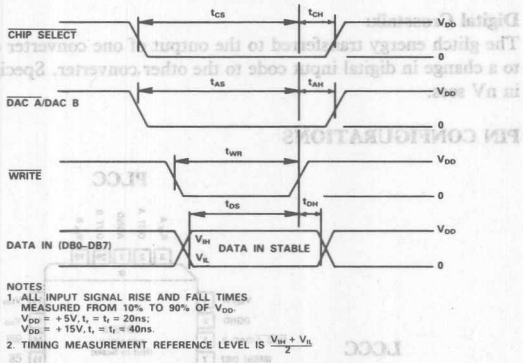
The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{\text{DAC A}}$/DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Mode Selection Table

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

CIRCUIT INFORMATION–D/A SECTION

The AD7528 contains two identical 8-bit multiplying D/A converters, DAC A and DAC B. Each DAC consists of a highly stable thin film R-2R ladder and eight N-channel current steering switches. A simplified D/A circuit for DAC A is shown in Figure 1. An inverted R-2R ladder structure is used, that is, binary weighted currents are switched between the DAC output and AGND thus maintaining fixed currents in each ladder leg independent of switch state.

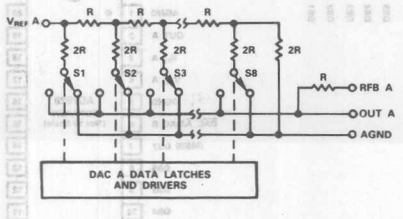


Figure 1. Simplified Functional Circuit for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an approximate equivalent circuit for one of the AD7528's D/A converters, in this case DAC A. A similar equivalent circuit can be drawn for DAC B. Note that AGND (Pin 1) is common for both DAC A and DAC B.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and, as with most semiconductor devices, approximately doubles every 10°C. The resistor R_O as shown in Figure 2 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50pF to 120pF depending upon the digital input. g(V_{REF} A, N) is the Thevenin equivalent voltage generator due to the reference input voltage V_{REF} A and the transfer function of the R-2R ladder.

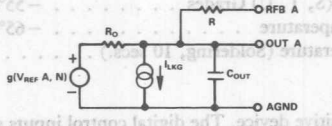


Figure 2. Equivalent Analog Output Circuit of DAC A

For further information on CMOS multiplying D/A converters refer to "Appplication Guide to CMOS Multiplying D/A Converters" available from Analog Devices, Publication Number G479–15–8/78.

CIRCUIT INFORMATION–DIGITAL SECTION

The input buffers are simple CMOS inverters designed such that when the AD7528 is operated with V_{DD} = 5V, the buffer converts TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and pass a quiescent current, see Figure 3. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7528 may be operated with any supply voltage in the range $5 \le V_{DD} \le 15$ volts. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

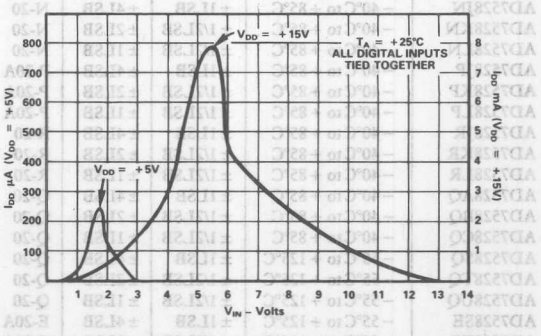


Figure 3. Typical Plots of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5V and +15V

LC²MOS Dual 12-Bit DACs

AD7537/AD7547

FEATURES

- Two 12-Bit DACs in One Package
- DAC Ladder Resistance Matching: 0.5%
- Space Saving Skinny DIP and Surface Mount Packages
- 4-Quadrant Multiplication
- Low Gain Error (1LSB max Over Temperature)
- Byte Loading Structure
- Fast Interface Timing

APPLICATIONS

- Automatic Test Equipment
- Programmable Filters
- Audio Applications
- Synchro Applications
- Process Control

GENERAL DESCRIPTION

The AD7537/AD7547 contains two 12-bit current output DACs on one monolithic chip. Also on-chip are the level shifters, data registers and control logic for easy microprocessor interfacing. There are 12 data inputs. The AD7537 has a 2-byte loading structure making it compatible with 8-bit processor systems. The AD7547 has a 12-bit parallel loading structure for use in 16-bit systems.

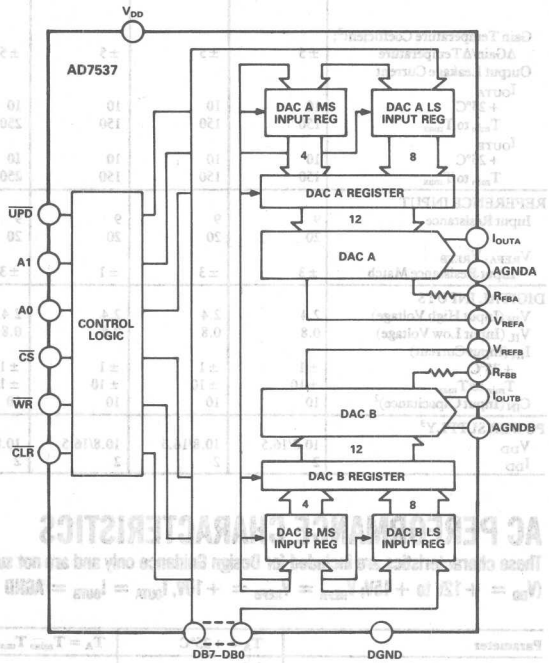
The D/A converters provide 4-quadrant multiplication capabilities with separate reference inputs and feedback resistors. Monolithic construction ensures that thermal and gain error tracking is excellent. Twelve-bit monotonicity is guaranteed for both DACs over the full temperature range.

The DACs are manufactured using the Linear Compatible CMOS (LC²MOS) process. This allows fast digital logic and precision linear circuitry to be fabricated on the same die.

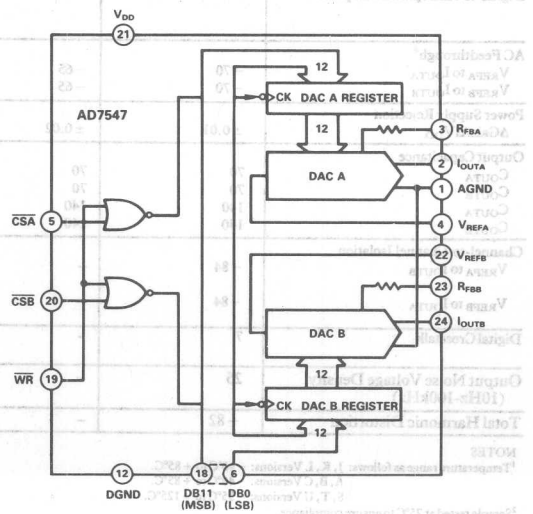
PRODUCT HIGHLIGHTS

1. DAC to DAC Matching
   Since both DACs are fabricated on the same chip, precise matching and tracking is inherent. Many applications which are not practical using two discrete DACs are now possible. Typical matching: 0.5%.
2. Wide Power Supply Tolerance
   The device operates on a +12V to +15V V_{DD}, with ±10% tolerance on this nominal figure. All specifications are guaranteed over this range.

AD7537 FUNCTIONAL BLOCK DIAGRAM



AD7547 FUNCTIONAL BLOCK DIAGRAM



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AD7537/AD7547—SPECIFICATIONS[1]

(V_{DD} = +12V to +15V, ±10%, V_{REFA} = V_{REFB} = 10V; I_{OUTA} = I_{OUTB} = AGND = 0V. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A Versions	K, B Versions	L, C Versions	S Version	T Version	U Version	Units	Test Conditions/Comments
ACCURACY								
Resolution	12	12	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1/2	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Gain Error	±6	±3	±1	±6	±3	±2	LSB max	Measured using R_{FBA}, R_{FBB}. Both DAC registers loaded with all 1's.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	±5	±5	ppm/°C max	Typical value is 1ppm/°C
Output Leakage Current								
I_{OUTA}								
+25°C	10	10	10	10	10	10	nA max	DAC A Register loaded
T_{min} to T_{max}	150	150	150	250	250	250	nA max	with all 0's.
I_{OUTB}								
+25°C	10	10	10	10	10	10	nA max	DAC B Register loaded
T_{min} to T_{max}	150	150	150	250	250	250	nA max	with all 0's.
REFERENCE INPUT								
Input Resistance	9	9	9	9	9	9	kΩ min	Typical Input Resistance = 14kΩ
	20	20	20	20	20	20	kΩmax	
V_{REFA}, V_{REFB} Input Resistance Match	±3	±3	±1	±3	±3	±1	% max	Typically ±0.5%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)								
+25°C	±1	±1	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	10	10	10	10	10	10	pF max	
POWER SUPPLY[3]								
V_{DD}	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	
I_{DD}	2	2	2	2	2	2	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +12V to +15V; V_{REFA} = V_{REFB} = +10V, I_{OUTA} = I_{OUTB} = AGND = 0V. Output Amplifiers are AD644 except where stated.)

Parameter	T_A = +25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.01% of full-scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC output measured from rising edge of $\overline{WR}$. Typical Value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	7	–	nV-s typ	Measured with V_{REFA} = V_{REFB} = 0V. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF. DAC registers alternately loaded with all 0's and all 1's.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	–70	–65	dB max	V_{REFA}, V_{REFB} = 20Vp-p 10kHz sinewave. DAC
V_{REFB} to I_{OUTB}	–70	–65	dB max	registers loaded with all 0's.
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = V_{DD} max – V_{DD} min
Output Capacitance				
C_{OUTA}	70	70	pF max	DAC A, DAC B loaded with all 0's.
C_{OUTB}	70	70	pF max	
C_{OUTA}	140	140	pF max	DAC A, DAC B loaded with all 1's.
C_{OUTB}	140	140	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	–84	–	dB typ	V_{REFA} = 20V p-p 10kHz sinewave, V_{REFB} = 0V. Both DACs loaded with all 1's.
V_{REFB} to I_{OUTA}	–84	–	dB typ	V_{REFB} = 20V p-p 10kHz sinewave, V_{REFA} = 0V. Both DACs loaded with all 1's.
Digital Crosstalk	7	–	nV-s typ	Measured for a Code Transition of all 0's to all 1's. I_{OUTA}, I_{OUTB} Load = 100Ω, C_{EXT} = 13pF
Output Noise Voltage Density (10Hz-100kHz)	25	–	nV/√Hz typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}. Frequency of measurement is 10Hz–100kHz.
Total Harmonic Distortion	–82	–	dB typ	V_{IN} = 6V rms, 1kHz. Both DACs loaded with all 1's.

NOTES

[1]Temperature range as follows: J, K, L Versions: –40°C to +85°C.
A, B, C Versions: –40°C to +85°C.
S, T, U Versions: –55°C to +125°C.

[2]Sample tested at 25°C to ensure compliance.

[3]Functional at V_{DD} = 5V with degraded specifications.

[4]Pin 12 (DGND) on ceramic DIPs is connected to lid.

Specifications subject to change without notice.

AD7537 TIMING CHARACTERISTICS (V_{DD} = 10.8V to 16.5V, $V_{REFA} = V_{REFB}$ = +10V, I_{OUTA} = AGNDA = 0V, I_{OUTB} = AGNDB = 0V).

Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Limit at T_A = +55°C to +125°C	Units	Test Conditions/Comments
t_1	15	15	30	ns min	Address Valid to Write Setup Time
t_2	15	15	25	ns min	Address Valid to Write Hold Time
t_3	60	80	80	ns min	Data Setup Time
t_4	25	25	25	ns min	Data Hold Time
t_5	0	0	0	ns min	Chip Select or Update to Write Setup Time
t_6	0	0	0	ns min	Chip Select or Update to Write Hold Time
t_7	80	80	100	ns min	Write Pulse Width
t_8	80	80	100	ns min	Clear Pulse Width

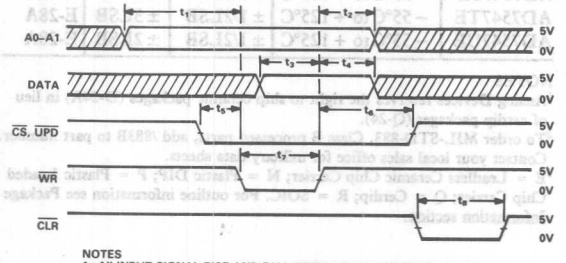
Specifications subject to change without notice.

3

Table I. AD7537 Truth Table

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
↓	↓	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Loads Data to the Respective DAC from the Data Bus
0	1	↓	DAC A Register Loaded from Data Bus
1	0	↓	DAC B Register Loaded from Data Bus
0	0	↓	DAC A and DAC B Registers Loaded from Data Bus

NOTES
1. X = Don't care
2. ↓ means rising edge triggered



NOTES
1. All INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_H + V_L}{2}$

Figure 1. Timing Diagram for AD7537

AD7537 ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7537JN	−40°C to +85°C	±1LSB	±6LSB	N-24
AD7537KN	−40°C to +85°C	±1/2LSB	±3LSB	N-24
AD7537LN	−40°C to +85°C	±1/2LSB	±1LSB	N-24
AD7537JP	−40°C to +85°C	±1LSB	±6LSB	P-28A
AD7537KP	−40°C to +85°C	±1/2LSB	±3LSB	P-28A
AD7537LP	−40°C to +85°C	±1/2LSB	±1LSB	P-28A
AD7537AQ	−40°C to +85°C	±1LSB	±6LSB	Q-24
AD7537BQ	−40°C to +85°C	±1/2LSB	±3LSB	Q-24
AD7537CQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-24
AD7537SQ	−55°C to +125°C	±1LSB	±6LSB	Q-24
AD7537TQ	−55°C to +125°C	±1/2LSB	±3LSB	Q-24
AD7537UQ	−55°C to +125°C	±1/2LSB	±2LSB	Q-24
AD7537SE	−55°C to +125°C	±1LSB	±6LSB	E-28A
AD7537TE	−55°C to +125°C	±1/2LSB	±3LSB	E-28A
AD7537UE	−55°C to +125°C	±1/2LSB	±2LSB	E-28A

NOTES
[1]Analog Devices reserves the right to ship ceramic packages (D-24A) in lieu of cerdip packages (Q-24).
[2]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

AD7547 TIMING CHARACTERISTICS (V_{DD} = 10.8V to 16.5V, V_{REFA} = V_{REFB} = +10V, I_{OUTA} = AGNDA = 0V).

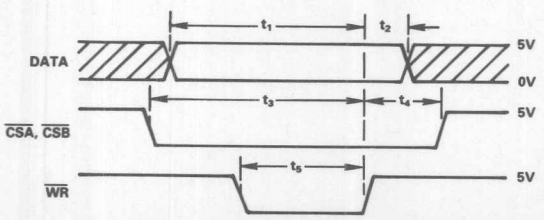
Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	60	80	80	ns min	Data Setup Time
t_2	25	25	25	ns min	Data Hold Time
t_3	80	80	100	ns min	Chip Select to Write Setup Time
t_4	0	0	0	ns min	Chip Select to Write Hold Time
t_5	80	80	100	ns min	Write Pulse Width

Specifications subject to change without notice.

Table II. AD7547 Truth Table

$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A1	A0	FUNCTION
1	1	1	X	X	X	No Data Transfer
1	1	X	1	X	X	No Data Transfer
0	X	X	X	X	X	All Registers Cleared
1	1	0	0	0	0	DAC A LS Input Register Loaded with DB7-DB0(LSB)
1	1	0	0	0	1	DAC A MS Input Register Loaded with DB3(MSB)-DB0
1	1	0	0	1	0	DAC B LS Input Register Loaded with DB7-DB0(LSB)
1	1	0	0	1	1	DAC B MS Input Register Loaded with DB3(MSB)-DB0
1	0	1	0	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
1	0	0	0	X	X	DAC A, DAC B Registers are Transparent

NOTE: X = Don't care



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH}+V_{IL}}{2}$

Figure 2. Timing Diagram for AD7547

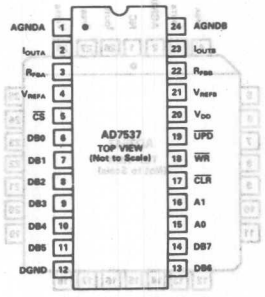
AD7547 ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7547JN	−40°C to +85°C	±1LSB	±6LSB	N-24
AD7547KN	−40°C to +85°C	±1/2LSB	±3LSB	N-24
AD7547LN	−40°C to +85°C	±1/2LSB	±1LSB	N-24
AD7547JP	−40°C to +85°C	±1LSB	±6LSB	P-28A
AD7547KP	−40°C to +85°C	±1/2LSB	±3LSB	P-28A
AD7547LP	−40°C to +85°C	±1/2LSB	±1LSB	P-28A
AD7547JR	−40°C to +85°C	±1LSB	±6LSB	R-24
AD7547KR	−40°C to +85°C	±1/2LSB	±3LSB	R-24
AD7547LR	−40°C to +85°C	±1/2LSB	±1LSB	R-24
AD7547AQ	−40°C to +85°C	±1LSB	±6LSB	Q-24
AD7547BQ	−40°C to +85°C	±1/2LSB	±3LSB	Q-24
AD7547CQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-24
AD7547SQ	−55°C to +125°C	±1LSB	±6LSB	Q-24
AD7547TQ	−55°C to +125°C	±1/2LSB	±3LSB	Q-24
AD7547UQ	−55°C to +125°C	±1/2LSB	±2LSB	Q-24
AD7547SE	−55°C to +125°C	±1LSB	±6LSB	E-28A
AD7547TE	−55°C to +125°C	±1/2LSB	±3LSB	E-28A
AD7547UE	−55°C to +125°C	±1/2LSB	±2LSB	E-28A

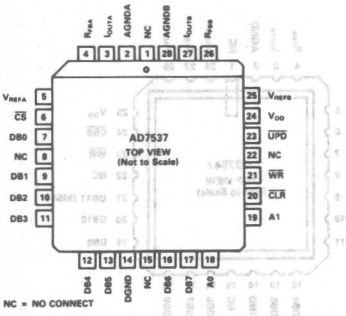
NOTES
[1]Analog Devices reserves the right to ship ceramic packages (D-24A) in lieu of cerdip packages (Q-24).
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheets.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

AD7537 PIN CONFIGURATIONS

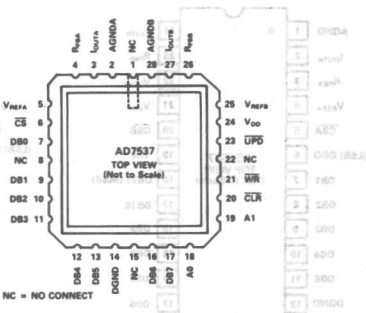
DIP



PLCC



LCCC



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PIN FUNCTION DESCRIPTION (DIP)

PIN	MNEMONIC	DESCRIPTION
1	AGNDA	Analog Ground for DAC A.
2	I_{OUTA}	Current output terminal of DAC A.
3	R_{FBA}	Feedback resistor for DAC A.
4	V_{REFA}	Reference input to DAC A.
5	$\overline{CS}$	Chip Select Input. Active low.
6–14	DB0–DB7	Eight data inputs, DB0–DB7.
12	DGND	Digital Ground.
15	A0	Address Line 0.
16	A1	Address Line 1.
17	$\overline{CLR}$	Clear Input. Active low. Clears all registers.
18	$\overline{WR}$	Write Input. Active low.
19	$\overline{UPD}$	Updates DAC Registers from inputs registers.
20	V_{DD}	Power supply input. Nominally +12V to +15V, with ±10% tolerance.
21	V_{REFB}	Reference input to DAC B.
22	R_{FBB}	Feedback resistor for DAC B.
23	I_{OUTB}	Current output terminal of DAC B.
24	AGNDB	Analog Ground for DAC B.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise stated)

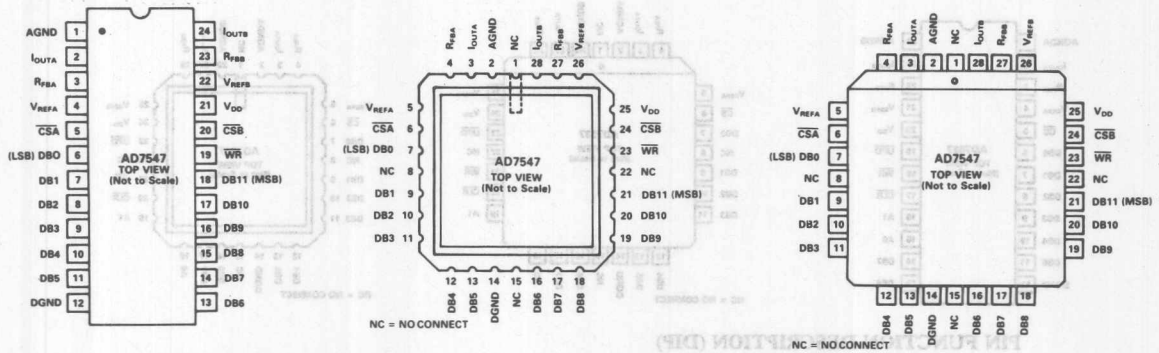
V_{DD} to DGND . . . . . −0.3V, +17V
V_{REFA}, V_{REFB} to AGND, ... ±25V
V_{RFBA}, V_{RFBB} to AGND, ... ±25V
Digital Input Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
I_{OUTA}, I_{OUTB} to DGND . . . . . −0.3V, V_{DD} +0.3V
AGND to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C

Operating Temperature Range
Commercial (J, K, L Versions) . . . . . −40°C to +85°C
Industrial (A, B, C Versions) . . . . . −40°C to +85°C
Extended (S, T, U Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



PIN FUNCTION DESCRIPTION (DIP)

PIN	MNEMONIC	DESCRIPTION
1	AGND	Analog Ground.
2	I_{OUTA}	Current output terminal of DACA.
3	R_{FBA}	Feedback resistor for DACA.
4	V_{REFA}	Reference input to DACA.
5	$\overline{CSA}$	Chip Select Input for DAC A. Active low.
6-18	DB0-DB11	12 data inputs, DB0 (LSB) – DB11 (MSB).
12	DGND	Digital Ground.
19	$\overline{WR}$	Write Input. Data transfer occurs on rising edge of $\overline{WR}$. See Table I.
20	$\overline{CSB}$	Chip Select Input for DACB. Active low.
21	V_{DD}	Power supply input. Nominally + 12V to + 15V with ± 10% tolerance.
22	V_{REFB}	Reference input to DACB.
23	R_{FBB}	Feedback resistor of DACB.
24	I_{OUTB}	Current output terminal of DACB.

CIRCUIT INFORMATION

D/A SECTION

The AD7537/AD7547 contains two identical 12-bit multiplying D/A converters. Each DAC consists of a highly stable R-2R ladder and 12 N-channel current steering switches. Figure 3 shows a simplified D/A circuit for DAC A. In the R-2R ladder, binary weighted currents are steered between I_{OUTA} and AGND. The current flowing in each ladder leg is constant, irrespective of switch state. The feedback resistor R_{FBA} is used with an op-amp to convert the current flowing in I_{OUTA} to a voltage output.

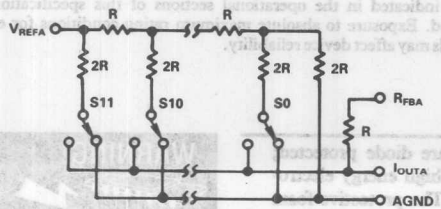


Figure 3. Simplified Circuit Diagram for DACA

EQUIVALENT CIRCUIT ANALYSIS

Figure 4 shows the equivalent circuit for one of the D/A converters (DAC A) in the AD7537/AD7547. A similar equivalent circuit can be drawn for DACB. Note that AGND is common to both DAC A and DAC B.

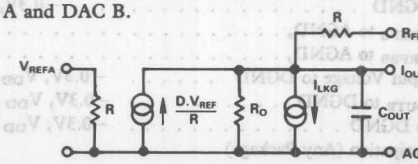


Figure 4. Equivalent Analog Circuit for DACA

C_{OUT} is the output capacitance due to the N-channel switches and varies from about 50pF to 150pF with digital input code. The current source I_{LKG} is composed of surface and junction leakages and approximately doubles every 10°C. R_O is the equivalent output resistance of the device which varies with input code.

DIGITAL CIRCUIT INFORMATION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static-protected MOS gates with typical input currents of less than 1nA.

LC²MOS
µP-Compatible 14-Bit DAC

AD7538

3

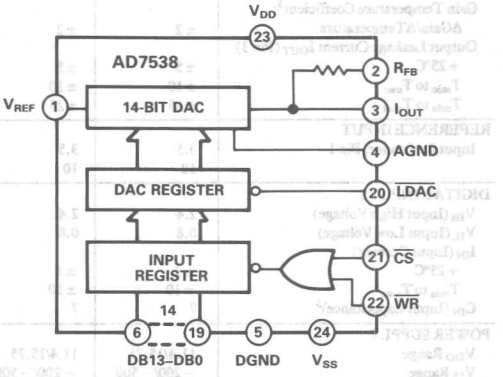
FEATURES

- All Grades 14-Bit Monotonic over the Full Temperature Range
- Low Cost 14-Bit Upgrade for 12-Bit Systems
- 14-Bit Parallel Load with Double Buffered Inputs
- Small 24-Pin, 0.3" DIP and SOIC
- Low Output Leakage (<20nA) over the Full Temperature Range

APPLICATIONS

- Microprocessor Based Control Systems
- Digital Audio
- Precision Servo Control
- Control and Measurement in High Temperature Environments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7538 is a 14-bit monolithic CMOS D/A converter which uses laser trimmed thin-film resistors to achieve excellent linearity.

The DAC is loaded by a single 14-bit wide word using standard Chip Select and Memory Write Logic. Double buffering, which is optional using $\overline{LDAC}$, allows simultaneous update in a system containing multiple AD7538s.

A novel low leakage configuration (U.S. Patent No. 4,590,456) enables the AD7538 to exhibit excellent output leakage current characteristics over the specified temperature range.

The AD7538 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Guaranteed Monotonicity
   The AD7538 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Cost
   The AD7538, with its 14-bit dynamic range, affords a low cost solution for 12-bit system upgrades.
3. Small Package Size
   The AD7538 is packaged in a small 24-pin, 0.3" DIP and a 24-pin SOIC.
4. Low Output Leakage
   By tying V_{SS} (Pin 24) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
5. Wide Power Supply Tolerance
   The device operates on a +12 to +15V V_{DD}, with a ±5% tolerance on this nominal figure. All specifications are guaranteed over this range.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7538—SPECIFICATIONS (V_{DD} = +11.4V to +15.75V[2], V_{REF} = +10V; V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	J, K Versions	A, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	over temperature.
Full-Scale Error						Measured using internal R_{FB}
+25°C	±4	±4	±4	±4	LSB max	DAC registers loaded with
T_{min}–T_{max}	±8	±5	±10	±6	LSB max	all 1s.
Gain Temperature Coefficient[3];						
ΔGain/ΔTemperature	±2	±2	±2	±2	ppm/°C typ	
Output Leakage Current I_{OUT} (Pin 3)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs 0V
T_{min} to T_{max}	±10	±10	±20	±20	nA max	V_{SS} = −300mV
T_{min} to T_{max}	±25	±25	±150	±150	nA max	V_{SS} = 0V
REFERENCE INPUT						
Input Resistance, Pin 1	3.5	3.5	3.5	3.5	kΩ min	Typical Input Resistance = 6kΩ
	10	10	10	10	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V_{min}/V_{max}	Specification guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range
I_{DD}	4	4	4	4	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test. (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = 0V OR −300mV, Output Amplifier is AD711 except where stated.)

Parameter	T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.003% of full-scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s. Typical value of Settling Time is 0.8μs.
Digital to Analog Glitch Impulse	20	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s.
Multiplying Feedthrough Error	3	5	mV p-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0s.
Power Supply Rejection				
ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 3)	260	260	pF max	DAC register loaded with all 1s
C_{OUT} (Pin 3)	130	130	pF max	DAC register loaded with all 0s
Output Noise Voltage Density (10Hz–100kHz)	15	–	nV$\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3]Sample tested to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = 0V or −300mV
All specifications T_{min} to T_{max} unless otherwise stated. See Figure 1 for Timing Diagram.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	170	200	240	ns min	$\overline{LDAC}$ Pulse Width
t_4	170	200	240	ns min	Write Pulse Width
t_5	140	160	180	ns min	Data Setup Time
t_6	20	20	30	ns min	Data Hold Time

NOTES
[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

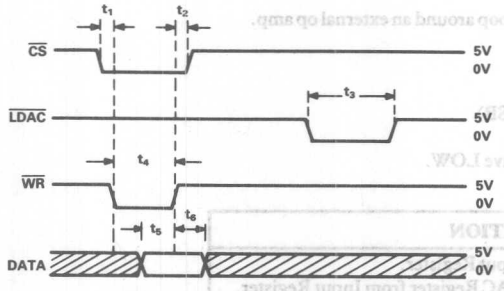
V_{DD} (Pin 23) to DGND . . . . . −0.3V, +17V
V_{SS} (Pin 24) to AGND . . . . . −15V, +0.3V
V_{REF} (Pin 1) to AGND . . . . . ±25V
V_{RFB} (Pin 2) to AGND . . . . . ±25V
Digital Input Voltage (Pins 6–22)
to DGND . . . . . −0.3V, V_{DD} +0.3V
V_{PIN3} to DGND . . . . . −0.3V, V_{DD} +0.3V
AGND to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 1000mW
Derates above +75°C . . . . . 10mW/°C

Operating Temperature Range
Commercial (J, K versions) . . . . . 0 to +70°C
Industrial (A, B versions) . . . . . −25°C to +85°C
Extended (S, T versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

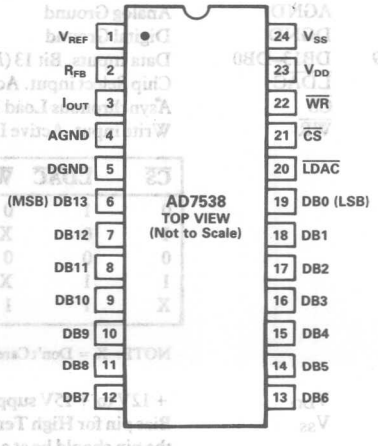


NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURES FROM 10% TO 90% OF +5V. $t_r = t_f = 20$ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. If $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 or LONGER AFTER WR GOES HIGH.

Figure 1. AD7538 Timing Diagram

PIN CONFIGURATION

DIP, SOIC



end-points of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustable to zero with an external potentiometer.

log Glitch Impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. It is measured with V_{REF} = AGND.

OUTPUT CAPACITANCE

This is the capacitance from I_{OUT} to AGND.

OUTPUT LEAKAGE CURRENT

Output Leakage Current is current which appears at I_{OUT} with the DAC register loaded to all 0s.

MULTIPLYING FEEDTHROUGH ERROR

This is the ac error due to capacitive feedthrough from V_{REF} terminal to I_{OUT} with DAC register loaded to all zeros.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Full-Scale Error	Package Option*
AD7538JN	0°C to +70°C	±2LSB	±8LSB	N-24
AD7538KN	0°C to +70°C	±1LSB	±4LSB	N-24
AD7538JR	0°C to +70°C	±2LSB	±8LSB	R-24
AD7538KR	0°C to +70°C	±1LSB	±4LSB	R-24
AD7538AQ	−25°C to +85°C	±2LSB	±8LSB	Q-24
AD7538BQ	−25°C to +85°C	±1LSB	±4LSB	Q-24
AD7538SQ	−55°C to +125°C	±2LSB	±8LSB	Q-24
AD7538TQ	−55°C to +125°C	±1LSB	±4LSB	Q-24

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	V_{REF}	Voltage Reference.
2	R_{FB}	Feedback resistor. Used to close the loop around an external op amp.
3	I_{OUT}	Current Output Terminal.
4	AGND	Analog Ground
5	DGND	Digital Ground
6–19	DB13–DB0	Data Inputs. Bit 13 (MSB) to Bit 0 (LSB).
20	$\overline{LDAC}$	Chip Select input. Active LOW.
21	$\overline{CS}$	Asynchronous Load DAC input. Active LOW.
22	$\overline{WR}$	Write input. Active LOW.

$\overline{CS}$	$\overline{LDAC}$	$\overline{WR}$	OPERATION
0	1	0	Load Input Register.
1	0	X	Load DAC Register from Input Register.
0	0	0	Input and DAC Registers are transparent
1	1	X	No operation.
X	1	1	No operation.

NOTE: X = Don't Care.

23	V_{DD}	+12V to +15V supply input.
24	V_{SS}	Bias pin for High Temperature Low Leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figures 4 and 5 for recommended circuitry.

ANALOG DEVICES

LC²MOS +3.3 V/+5 V Quad 12-Bit DAC

AD7564

3

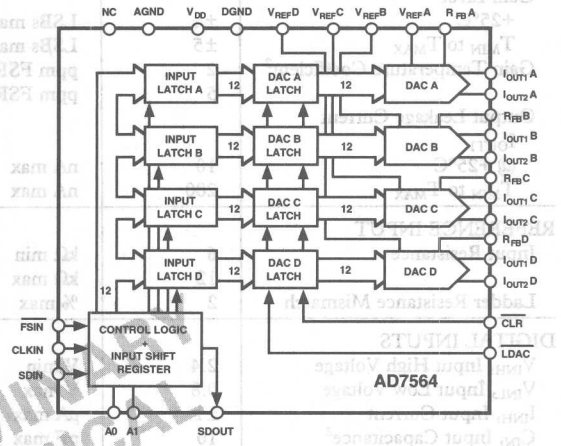
FEATURES

Four 12-Bit DACs in One Package
4-Quadrant Multiplication
Separate References
Single Supply Operation
Guaranteed Specifications with +3.3 V/+5 V Supply
Low Power
Versatile Serial Interface
Simultaneous Update Capability
Reset Function
28-Pin SOIC, SSOP and DIP Packages

APPLICATIONS

Process Control
Portable Instrumentation
General Purpose Test Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7564 contains four 12-bit DACs in one monolithic device. The DACs are standard current output with separate V_{REF}, I_{OUT1}, I_{OUT2} and R_{FB} terminals. These DACs operate from a single +5 V supply (Normal Mode) and a single +3.3 V to +5 V supply (Biased Mode).

The AD7564 is a serial input device. Data is loaded using $\overline{FSIN}$, CLKIN and SDIN. Two address pins A0 and A1 set up a device address, and this feature may be used to simplify device loading in a multi-DAC environment. Alternatively, A0 and A1 can be ignored and the serial out capability used to configure a daisy-chained system.

All DACs can be simultaneously updated using the asynchronous $\overline{LDAC}$ input, and they can be cleared by asserting the asynchronous $\overline{CLR}$ input.

The device is packaged in 28-pin SOIC, SSOP and DIP packages.

PRODUCT HIGHLIGHTS

1. The AD7564 contains four 12-bit current output DACs with separate V_{REF} inputs.
2. The AD7564 can be operated from a single +5 V supply (Normal Mode) or a single +3.3 V to +5 V supply (Biased Mode).
3. Simultaneous update capability and reset function are available.
4. The AD7564 features a fast, versatile serial interface compatible with all modern microprocessors and microcomputers.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSBs)	Nominal Supply Voltage	Package Option*
AD7564BN	–40°C to +85°C	±0.5	+5 V	N-28
AD7564BR	–40°C to +85°C	±0.5	+5 V	R-28
AD7564BRS	–40°C to +85°C	±0.5	+5 V	RS-28
AD7564AR-B	–40°C to +85°C	±1	+3.3 V to +5 V	R-28
AD7564ARS-B	–40°C to +85°C	±1	+3.3 V to +5 V	RS-28

*N = DIP; R = SOIC; RS = SSOP. For outline information see Package Information section.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7564–SPECIFICATIONS

Normal Mode

(V_{DD} = +4.75 V to +5.25 V; $I_{OUT1}A$ to $I_{OUT1}D$ = $I_{OUT2}A$ = $I_{OUT2}B$ = AGND = 0 V; V_{REF} = +10 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	B Grade	Units	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	1 LSB = $V_{REF}/2^{12}$ = 2.44 mV when V_{REF} = 10 V
Relative Accuracy	±0.5	LSB max	
Differential Nonlinearity	±0.9	LSB max	All Grades Guaranteed Monotonic Over Temperature
Gain Error			
+25°C	±4	LSBs max	
T_{MIN} to T_{MAX}	±5	LSBs max	
Gain Temperature Coefficient[2]	2	ppm FSR/°C typ	
	5	ppm FSR/°C max	
Output Leakage Current			
I_{OUT1}			
@ +25°C	10	nA max	
T_{MIN} to T_{MAX}	200	nA max	
REFERENCE INPUT			
Input Resistance	6	kΩ min	Typical Input Resistance = 9 kΩ
	12	kΩ max	
Ladder Resistance Mismatch	2	% max	Typically 0.6%
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±1	μA max	
C_{IN}, Input Capacitance[2]	10	pF max	
DIGITAL OUTPUT (SDOUT)			
Output Low Voltage (V_{OL})	0.4	V max	
Output High Voltage (V_{OH})	4.0	V min	
POWER REQUIREMENTS			
V_{DD} Range	4.75/5.25	V min/V max	
Power Supply Rejection			
$\Delta Gain/\Delta V_{DD}$	–75	dB min	
I_{DD}	300	μA max	V_{INH} = 4.0 V min, V_{INL} = 0.4 V max
	2	mA max	V_{INH} = 2.4 V min, V_{INL} = 0.8 V max

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Not production tested. Guaranteed by characterization at initial product release.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ACCURACY			
Resolution	12	Bits	1 LSB = $(V_{IOUT2} - V_{REF})/2^{12}$ = 300 μV when V_{IOUT2} = 1.23 V and V_{REF} = 0 V
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±0.9	LSB max	All Grades Guaranteed Monotonic Over Temperature
Gain Error			
+25°C	±4	LSBs max	
T_{MIN} to T_{MAX}	±5	LSBs max	
Gain Temperature Coefficient[3]	2	ppm FSR/°C typ	
	5	ppm FSR/°C max	
Output Leakage Current			See Terminology Section
I_{OUT1}			
@ +25°C	10	nA max	
T_{MIN} to T_{MAX}	200	nA max	
Input Resistance			
@ I_{OUT2} Pins	6	kΩ min	This Varies with DAC Input Code
DIGITAL INPUTS			
V_{INH}, Input High Voltage @ V_{DD} = +5 V	2.4	V min	
V_{INH}, Input High Voltage @ V_{DD} = +3.3 V	2.1	V min	
V_{INL}, Input Low Voltage @ V_{DD} = +5 V	0.8	V max	
V_{INL}, Input Low Voltage @ V_{DD} = +3.3 V	0.6	V max	
I_{INH}, Input Current	±1	μA max	
C_{IN}, Input Capacitance[2]	10	pF max	
DIGITAL OUTPUT (SDOUT)			
Output Low Voltage (V_{OL})	0.4	V max	V_{DD} = +5 V
Output Low Voltage (V_{OL})	0.2	V max	V_{DD} = +3.3 V
Output High Voltage (V_{OH})	4.0	V min	V_{DD} = +5 V
Output High Voltage (V_{OH})	V_{DD} – 0.2	V min	V_{DD} = +3.3 V
POWER REQUIREMENTS			
V_{DD} Range	4.75/5.25	V min/V max	
Power Supply Sensitivity[2]			
$\Delta Gain/\Delta V_{DD}$	–75	dB typ	
I_{DD}	300	μA max	$V_{INH} = V_{DD}$ – 0.1 V min, V_{INL} = 0.1 V max; SDOUT Open Circuit
	2	mA max	V_{DD} = +5 V, V_{INH} = 2.4 V min, V_{INL} = 0.8 V max; SDOUT Open Circuit

NOTES

[1]These specifications apply with the devices biased up at 1.23 V for single supply applications. The model numbering reflects this by means of a "-B" suffix (for example: AD7564AN-B). Figure 16 is an example of Biased Mode Operation.

[2]Temperature ranges is as follows: A Version: –40°C to +85°C.

[3]Not production tested. Guaranteed by characterization at initial product release.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AC Performance Characteristics

Normal Mode

(V_{DD} = +4.75 V to +5.25 V; V_{IOUT1} = V_{IOUT2} = AGND = 0 V. V_{REF} = 6 V rms, 1 kHz sine wave; DAC output op amp is AD843; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. These characteristics are included for Design Guidance and are not subject to test.)

Parameter	B Grade	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	500	ns typ	To 0.01% of Full-Scale Range. DAC Latch Alternately Loaded with All 0s and All 1s
Digital-to-Analog Glitch Impulse	40	nV-s typ	Measured with V_{REF} = 0 V. DAC Register Alternately Loaded with All 0s and All 1s
Multiplying Feedthrough Error	–70	dB max	V_{REF} = 20 V p-p, 10 kHz Sine Wave. DAC Latch Loaded with All 0s
Channel-to-Channel Isolation	–76	dB typ	Feedthrough from Any One Reference to the Others with 20 V p-p, 10 kHz Sine Wave Applied
Digital Crosstalk	10	nV-s typ	Effect of All 0s to All 1s Code Transition on Nonselected DACs
Digital Feedthrough	10	nV-s typ	Feedthrough to Any DAC Output with $\overline{FSIN}$ High and Square Wave Applied to SDIN and SCLK
Total Harmonic Distortion	–83	dB typ	V_{REF} = 6 V rms, 1 kHz Sine Wave
Output Noise Spectral Density @ 1 kHz	20	nV/$\sqrt{Hz}$	All 1s Loaded to the DAC. V_{REF} = 0 V. Output Op Amp Is ADOP07

PRELIMINARY TECHNICAL DATA

AC Performance Characteristics

Biased Mode

(V_{DD} = +3 V to +5.5 V; V_{IOUT1} = V_{IOUT2} = AGND = 1.23 V. V_{REF} = 1 kHz, 2.45 V p-p, sine wave biased at 1.23 V; DAC output op amp is AD820; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. These characteristics are included for Design Guidance and are not subject to test.)

Parameter	A Grade	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	5	µs typ	To 0.01% of Full Scale Range. V_{REF} = 0 V. DAC Latch Alternately Loaded with all 0s and all 1s.
Digital to Analog Glitch Impulse	40	nV-s typ	Measured with V_{IOUT2} = 0 V and V_{REF} = 0 V. DAC Register Alternately Loaded with all 0s and all 1s.
Multiplying Feedthrough Error	–70	dB max	DAC Latch Loaded with all 0s.
Output Capacitance	60	pF max	All 1s Loaded to DAC
	30	pF max	All 0s Loaded to DAC
Digital Feedthrough	10	nV-s typ	Feedthrough to Any DAC Output with FSIN HIGH and a Square Wave Applied to SDIN and CLKIN
Total Harmonic Distortion	–83	dB typ	
Output Noise Spectral Density @ 1 kHz	20	nV/$\sqrt{Hz}$ typ	All 1s Loaded to DAC. V_{IOUT2} = 0 V; V_{REF} = 0 V

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Timing Specifications[1] ($T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	Limit at V_{DD} = +3 V to +3.6 V	Limit at V_{DD} = +4.75 V to +5.25 V	Units	Description
t_1	140	100	ns min	CLKIN Cycle Time
t_2	60	40	ns min	CLKIN High Time
t_3	60	40	ns min	CLKIN Low Time
t_4	50	30	ns min	$\overline{FSIN}$ Setup Time
t_5	50	30	ns min	Data Setup Time
t_6	10	5	ns min	Data Hold Time
t_7	125	90	ns min	$\overline{FSIN}$ Hold Time
t_8[2]	100	70	ns max	SDOUT Valid After CLKIN Falling Edge
t_9	60	40	ns min	$\overline{LDAC}$, $\overline{CLR}$ Pulse Width

NOTES

[1]Not production tested. Guaranteed by characterization at initial product release. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V for a V_{DD} of 5 V and from a voltage level 1.35 V for a V_{DD} of 3.3 V.

[2]t_8 is measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V with a V_{DD} of 5 V and 0.6 V or 2.1 V for a V_{DD} of 3.3 V.

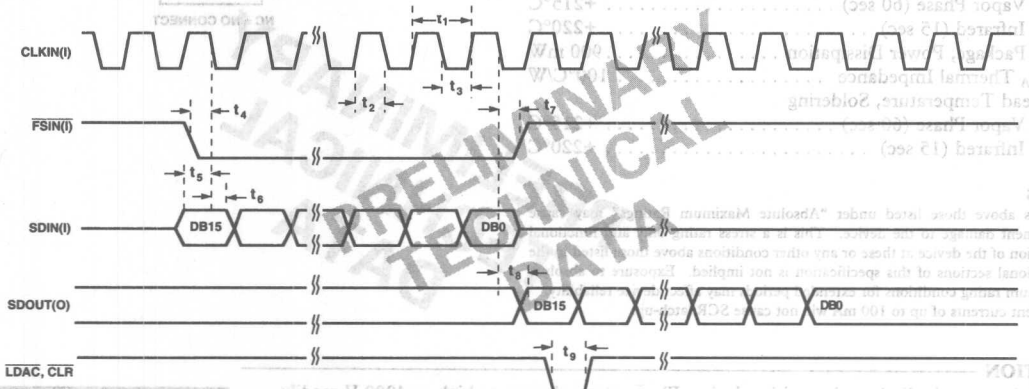


Figure 1. Timing Diagram

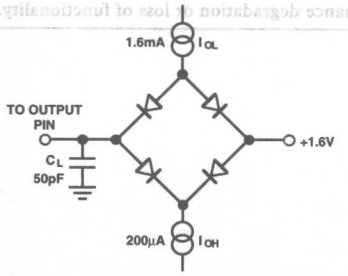
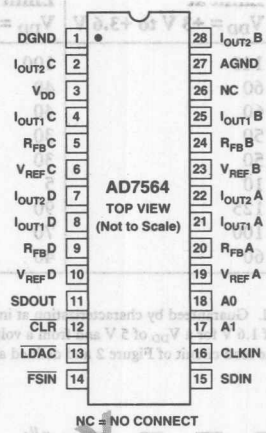


Figure 2. Load Circuit for Digital Output Timing Specifications

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

V_{DD} to DGND ..... –0.3 V to +6 V
I_{OUT1} to DGND ..... –0.3 V to V_{DD} + 0.3 V
I_{OUT2} to DGND ..... –0.3 V to V_{DD} + 0.3 V
AGND to DGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
V_{RFB}, V_{REF} to DGND ..... ±15 V
Input Current to Any Pin Except Supplies[2] ..... ±10 mA
Operating Temperature Range
Commercial Plastic (A, B Versions) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
DIP Package, Power Dissipation ..... 875 mW
θ_{JA} Thermal Impedance ..... 75°C/W
Lead Temperature, Soldering (10 sec) ..... 260°C
SOIC Package, Power Dissipation ..... 875 mW
θ_{JA} Thermal Impedance ..... 75°C/W
Lead Temperature, Soldering (10 sec) ..... 260°C
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
SSOP Package, Power Dissipation ..... 900 mW
θ_{JA} Thermal Impedance ..... 100°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

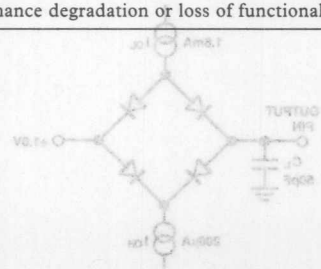


NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

PRELIMINARY TECHNICAL DATA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7564 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



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PIN DESCRIPTIONS

Pin Number	Mnemonic	Description
1	DGND	Digital Ground.
2	$I_{OUT2}C$	I_{OUT2} terminal for DAC C. This should normally connect to the signal ground of the system.
3	V_{DD}	Positive power supply. This is +5 V ± 5%.
4	$I_{OUT1}C$	I_{OUT1} terminal for DAC C.
5	$R_{FB}C$	Feedback resistor for DAC C.
6	$V_{REF}C$	DAC C reference input.
7	$I_{OUT2}D$	I_{OUT2} terminal for DAC D. This should normally connect to the signal ground of the system.
8	$I_{OUT1}D$	I_{OUT1} terminal for DAC D.
9	$R_{FB}D$	Feedback resistor for DAC D.
10	$V_{REF}D$	DAC D reference input.
11	SDOUT	This shift register output allows multiple devices to be connected in a daisy chain configuration.
12	$\overline{CLR}$	Asynchronous $\overline{CLR}$ input. When this input is taken low, all DAC latches are loaded with all 0s.
13	$\overline{LDAC}$	Asynchronous LDAC input. When this input is taken low, all DAC latches are simultaneously updated with the contents of the input latches.
14	$\overline{FSIN}$	Level-triggered control input (active low). This is the frame synchronization signal for the input data. When $\overline{FSIN}$ goes low, it enables the input shift register, and data is transferred on the falling edges of CLKIN. If the address bits are valid, the 12-bit DAC data is transferred to the appropriate input latch on the sixteenth falling edge after $\overline{FSIN}$ goes low.
15	SDIN	Serial data input. The device accepts a 16-bit word. DB0 and DB1 are DAC select bits. DB2 and DB3 are device address bits. DB4 to DB15 contain the 12-bit data to be loaded to the selected DAC.
16	CLKIN	Clock Input. Data is clocked into the input shift register on the falling edges of CLKIN.
17	A1	Device address pin. This input in association with A0 gives the device an address. If DB2 and DB3 of the serial input stream do not correspond to this address, the data which follows is ignored and not loaded to any input latch. However, it will appear at SDOUT irrespective of this.
18	A0	Device address pin. This input in association with A1 gives the device an address.
19	$V_{REF}A$	DAC A reference input.
20	$R_{FB}A$	Feedback resistor for DAC A.
21	$I_{OUT1}A$	I_{OUT1} terminal for DAC A.
22	$I_{OUT2}A$	I_{OUT2} terminal for DAC A. This should normally connect to the signal ground of the system.
23	$V_{REF}B$	DAC B reference input.
24	$R_{FB}B$	Feedback resistor for DAC B.
25	$I_{OUT1}B$	I_{OUT1} terminal for DAC B.
26	N/C	No Connect pin.
27	AGND	This pin connects to the back gates of the current steering switches. It should be connected to the signal ground of the system.
28	$I_{OUT2}B$	I_{OUT2} terminal for DAC B. This should normally connect to the signal ground of the system.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Gain Error
Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustable to zero with an external potentiometer.

Output Leakage Current
Output leakage current is current which flows in the DAC ladder switches when these are turned off. For the I_{OUT1} terminal, it can be measured by loading all 0s to the DAC and be measured by loading all 0s to the DAC and measuring the I_{OUT1} current. Minimum current will flow in the I_{OUT2} line when the DAC is loaded with all 1s. This is a combination of the switch leakage current and the ladder termination resistor current. The I_{OUT2} leakage current is typically equal to that in I_{OUT1}.

Output Capacitance
This is the capacitance from the I_{OUT1} pin to AGND.

Output Voltage Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For the AD7564, it is specified with the AD843 as the output op amp.

Digital to Analog Glitch Impulse
This is the amount of charge injected into the analog output when the inputs change state. It is normally specified as the area of the glitch in either pA-secs or nV-secs, depending upon whether the glitch is measured as a current or voltage signal. It is measured with the reference input connected to AGND and the digital inputs toggled between all 1s and all 0s.

AC Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC I_{OUT} terminal, when all 0s are loaded in the DAC.

Channel-to-Channel Isolation
Channel-to-channel isolation refers to the proportion of input signal from one DAC's reference input which appears at the output of any other DAC in the device and is expressed in dBs.

Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as the Digital Crosstalk and is specified in nV-secs.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up at on the I_{OUT} pin and subsequently on the op amp output. This noise is digital feedthrough.

PRELIMINARY TECHNICAL DATA

Table I. AD7564 Loading Sequence

DB15											DB0				
DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	A1	A0	DS1	DS0

Table II. DAC Selection

DS1	DS0	Function
0	0	DAC A Selected
0	1	DAC B Selected
1	0	DAC C Selected
1	1	DAC D Selected

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

LC²MOS Octal 12-Bit DAC

AD7568

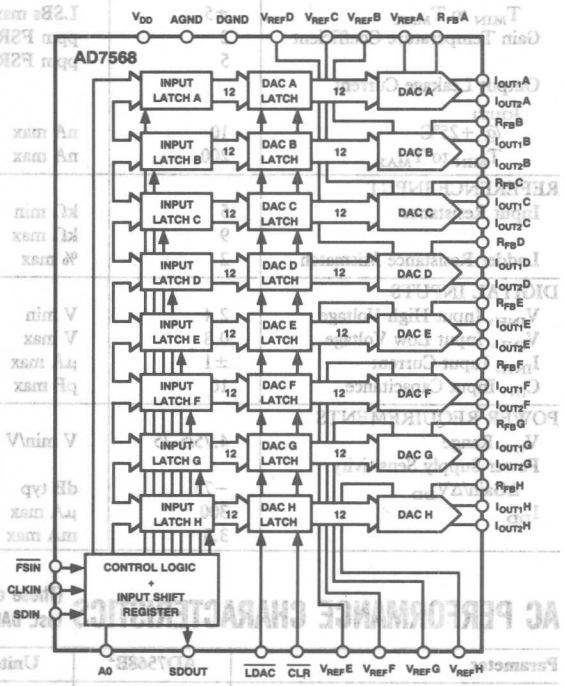
FEATURES

- Eight 12-Bit DACs in One Package
- 4-Quadrant Multiplication
- Separate References
- Single +5 V Supply
- Low Power: 1 mW
- Versatile Serial Interface
- Simultaneous Update Capability
- Reset Function
- 44-Pin PQFP and PLCC

APPLICATIONS

- Process Control
- Automatic Test Equipment
- General Purpose Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7568 contains eight 12-bit DACs in one monolithic device. The DACs are standard current output with separate V_{REF}, I_{OUT1}, I_{OUT2} and R_{FB} terminals.

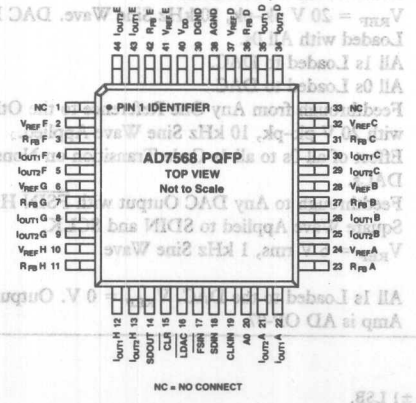
The AD7568 is a serial input device. Data is loaded using $\overline{FSIN}$, CLKIN and SDIN. One address pin, A0, sets up a device address, and this feature may be used to simplify device loading in a multi-DAC environment.

All DACs can be simultaneously updated using the asynchronous $\overline{LDAC}$ input and they can be cleared by asserting the asynchronous $\overline{CLR}$ input.

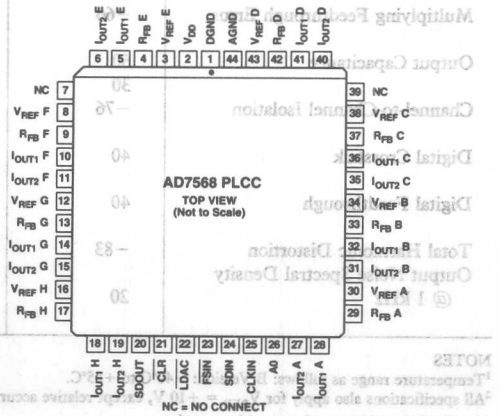
The AD7568 is housed in a space-saving 44-pin plastic quad flatpack and 44-lead PLCC.

PIN CONFIGURATIONS

Plastic Quad Flatpack



Plastic Leaded Chip Carrier



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7568—SPECIFICATIONS[1] (V_{DD} = +4.75 V to +5.25 V; I_{OUT1} = I_{OUT2} = 0 V; V_{REF} = +5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise stated)

Parameter	AD7568B[2]	Units	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	1 LSB = $V_{REF}/2^{12}$ = 1.22 mV when V_{REF} = 5 V
Relative Accuracy	±0.5	LSB max	
Differential Nonlinearity	±0.9	LSB max	All Grades Guaranteed Monotonic over Temperature
Gain Error			
+25°C	±4	LSBs max	
T_{MIN} to T_{MAX}	±5	LSBs max	
Gain Temperature Coefficient	2	ppm FSR/°C typ	
	5	ppm FSR/°C max	
Output Leakage Current			
I_{OUT1}			
@ +25°C	10	nA max	See Terminology Section
T_{MIN} to T_{MAX}	200	nA max	
REFERENCE INPUT			
Input Resistance	5	kΩ min	Typical Input Resistance = 7 kΩ
	9	kΩ max	
Ladder Resistance Mismatch	2	% max	Typically 0.6%
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±1	μA max	
C_{IN}, Input Capacitance	10	pF max	
POWER REQUIREMENTS			
V_{DD} Range	4.75/5.25	V min/V max	
Power Supply Sensitivity			
$\Delta Gain/\Delta V_{DD}$	−75	dB typ	
I_{DD}	300	μA max	V_{INH} = 4.0 V min, V_{INL} = 0.4 V max
	3.5	mA max	V_{INH} = 2.4 V min, V_{INL} = 0.8 V max

AC PERFORMANCE CHARACTERISTICS (These characteristics are included for Design Guidance and are not subject to test. DAC output op amp is AD843.)

Parameter	AD7568B[2]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	500	ns typ	To 0.01% of Full-Scale Range. DAC Latch Alternately Loaded with All 0s and All 1s.
Digital to Analog Glitch Impulse	40	nV–s typ	Measured with V_{REF} = 0 V. DAC Register Alternately Loaded with All 0s and All 1s.
Multiplying Feedthrough Error	−66	dB max	V_{REF} = 20 V pk–pk, 10 kHz Sine Wave. DAC Latch Loaded with All 0s.
Output Capacitance	60	pF max	All 1s Loaded to DAC.
	30	pF max	All 0s Loaded to DAC.
Channel-to-Channel Isolation	−76	dB typ	Feedthrough from Any One Reference to the Others with 20 V pk–pk, 10 kHz Sine Wave Applied.
Digital Crosstalk	40	nV–s typ	Effect of all 0s to all 1s Code Transition on Nonselected DACs.
Digital Feedthrough	40	nV–s typ	Feedthrough to Any DAC Output with $\overline{FSIN}$ High and Square Wave Applied to SDIN and SCLK.
Total Harmonic Distortion	−83	dB typ	V_{REF} = 6 V rms, 1 kHz Sine Wave.
Output Noise Spectral Density			
@ 1 kHz	20	nV/$\sqrt{Hz}$	All 1s Loaded to the DAC. V_{REF} = 0 V. Output Op Amp is AD OP-07.

NOTES
[1]Temperature range as follows: B Version: −40°C to +85°C.
[2]All specifications also apply for V_{REF} = +10 V, except relative accuracy which degrades to ±1 LSB.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{DD} = +5 V ± 5%; I_{OUT1} = I_{OUT2} = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Units	Description
t_1	100	100	ns min	CLKIN Cycle Time
t_2	40	40	ns min	CLKIN High Time
t_3	40	40	ns min	CLKIN Low Time
t_4	30	30	ns min	$\overline{FSIN}$ Setup Time
t_5	30	30	ns min	Data Setup Time
t_6	5	5	ns min	Data Hold Time
t_7	90	90	ns min	$\overline{FSIN}$ Hold Time
t_8[2]	70	70	ns max	SDOUT Valid After CLKIN Falling Edge
t_9	40	40	ns min	$\overline{LDAC}$, $\overline{CLR}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]t_8 is measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V.

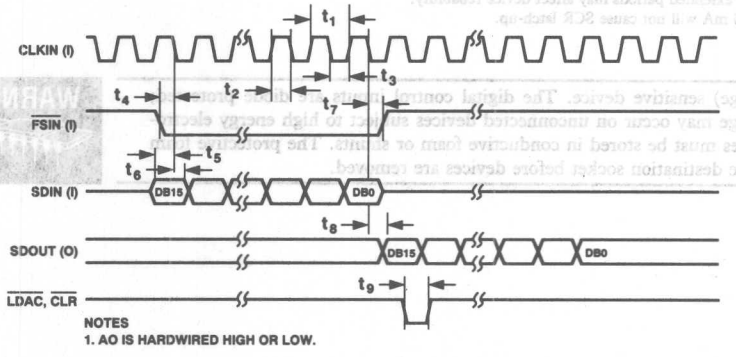


Figure 1. Timing Diagram

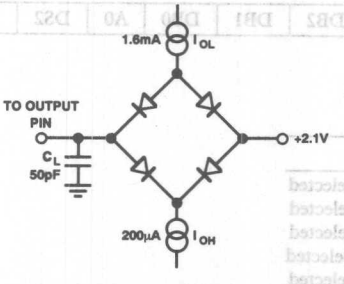


Figure 2. Load Circuit for Digital Output Timing Specifications

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSBs)	Package Option*
AD7568BS	−40°C to +85°C	±0.5	S-44
AD7568BP	−40°C to +85°C	±0.5	P-44A

*S = Plastic Quad Flatpack (PQFP), P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	−0.3 V to +6 V
I_{OUT1} to DGND	−0.3 V to V_{DD} + 0.3 V
I_{OUT2} to DGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
V_{RFB}, V_{REF} to DGND	±15 V
Input Current to Any Pin Except Supplies[2]	±10 mA
Operating Temperature Range	
Commercial Plastic (B Versions)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Any Package) to +75°C	250 mW
Derates above +75°C by	10 mW/°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Table I. AD7568 Loading Sequence

DB15															DB0
DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	A0	DS2	DS1	DS0

Table II. DAC Selection

DS2	DS1	DS0	Function
0	0	0	DAC A Selected
0	0	1	DAC B Selected
0	1	0	DAC C Selected
0	1	1	DAC D Selected
1	0	0	DAC E Selected
1	0	1	DAC F Selected
1	1	0	DAC G Selected
1	1	1	DAC H Selected

TERMINOLOGY

Relative Accuracy
Relative Accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage or full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Gain Error
Gain Error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustable to zero with an external potentiometer.

Output Leakage Current
Output leakage current is current which flows in the DAC ladder switches when these are turned off. For the I_{OUT1} terminal, it can be measured by loading all 0s to the DAC and measuring the I_{OUT1} current. Minimum current will flow in the I_{OUT2} line when the DAC is loaded with all 1s. This is a combination of the switch leakage current and the ladder termination resistor current. The I_{OUT2} leakage current is typically equal to that in I_{OUT1}.

Output Capacitance
This is the capacitance from the I_{OUT1} pin to AGND.

Output Voltage Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For the AD7568, it is specified with the AD843 as the output op amp.

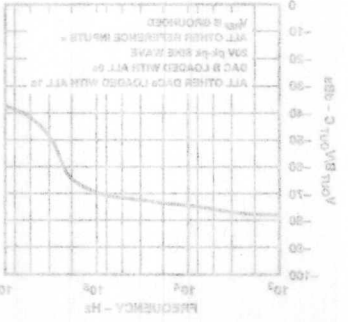
Digital to Analog Glitch Impulse
This is the amount of charge injected into the analog output when the inputs change state. It is normally specified as the area of the glitch in either pA-secs or nV-secs, depending upon whether the glitch is measured as a current or voltage signal. It is measured with the reference input connected to AGND and the digital inputs toggled between all 1s and all 0s.

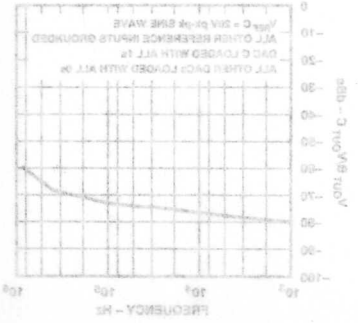
AC Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC I_{OUT} terminal, when all 0s are loaded in the DAC.

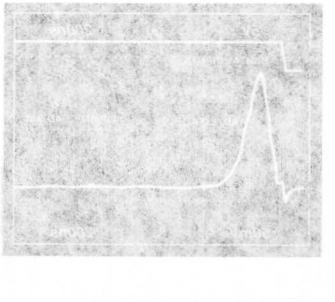
Channel-to-Channel Isolation
Channel-to-channel isolation refers to the proportion of input signal from one DAC's reference input which appears at the output of any other DAC in the device and is expressed in dBs.

Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as the Digital Crosstalk and is specified in nV-secs.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up as noise on the I_{OUT} pin and subsequently on the op amp output. This noise is digital feedthrough.







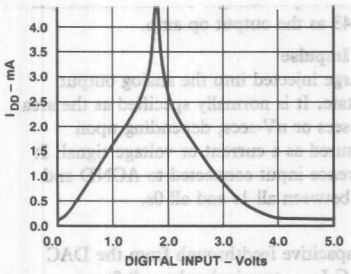


Figure 3. Supply Current vs. Logic Input Voltage

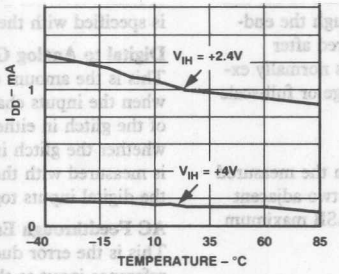


Figure 4. Supply Current vs. Temperature

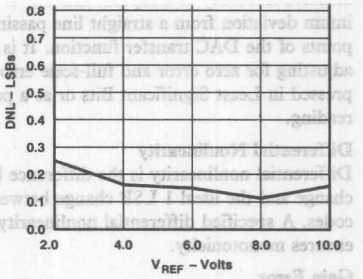


Figure 5. Differential Nonlinearity Error vs. V_{REF}

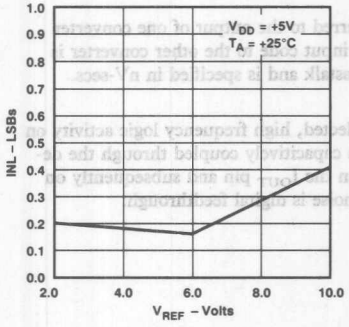


Figure 6. Integral Nonlinearity Error vs. V_{REF}

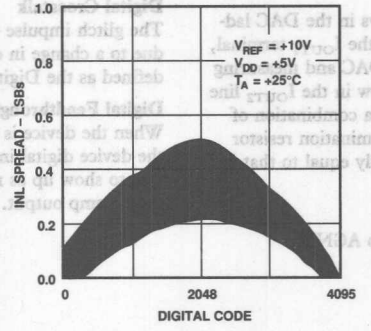


Figure 7. Typical DAC to DAC Linearity Matching

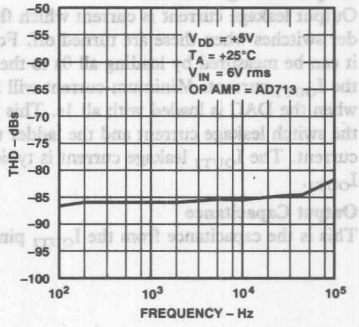


Figure 8. Total Harmonic Distortion vs. Frequency

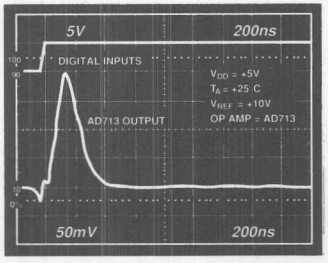


Figure 9. Digital-to-Analog Glitch Impulse

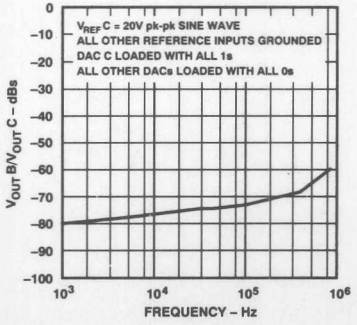


Figure 10. Channel-to-Channel Isolation (1 DAC to 1 DAC)

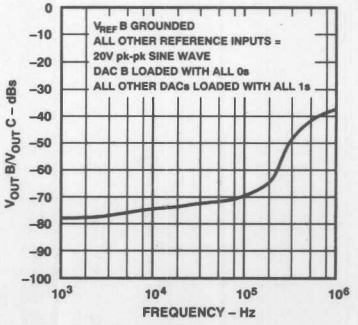


Figure 11. Channel-to-Channel Isolation (1 DAC to All Other DACs)

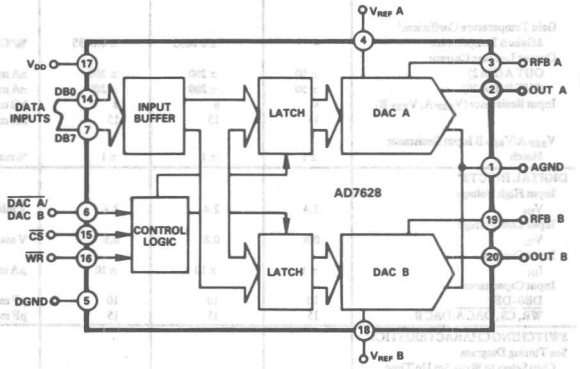
CMOS Dual 8-Bit Buffered Multiplying DAC

AD7628

FEATURES
- On-Chip Latches for Both DACs
- +12V to +15V Operation
- DACs Matched to 1%
- Four Quadrant Multiplication
- TTL/CMOS Compatible from +12V to +15V
- Latch Free (Protection Schottkys not Required)

APPLICATIONS
- Disk Drives
- Programmable Filters
- X-Y Graphics
- Gain/Attenuation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7628 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in small 0.3"-wide 20-pin DIPs and in 20-terminal surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The AD7628's load cycle is similar to the write cycle of a random access memory, and the device is bus compatible with most 8-bit microprocessors, including 6502, 6809, 8085, Z80.

The device operates from a +12V to +15V power supply and is TTL-compatible over this range. Power dissipation is a low 20mW.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

1. DAC to DAC matching: since both of the AD7628 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7628's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A}}$/DAC B select line has allowed the AD7628 to be packaged in a small 20-pin 0.3" wide DIP, 20-pin SOIC, 20-terminal PLCC and 20-terminal LCC.
3. TTL-Compatibility: All digital inputs are TTL-compatible over a +12V to +15V power supply range.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7628–SPECIFICATIONS

V_{DD} = +10.8V to +15.75V, (V_{REF} A = V_{REF} B = +10V; OUT A = OUT B = 0V unless otherwise specified)

Parameter	T_A = +25°C[1]	T_A = −40°C to +85°C	T_A = −55°C to +125°C[1]	Units	Test Conditions/Comments
STATIC PERFORMANCE[2]					
Resolution	8	8	8	Bits	
Relative Accuracy	±1/2	±1/2	±1/2	LSB max	This is an Endpoint Linearity Specification
Differential Nonlinearity	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	±2	±3	±3	LSB max	Measured Using Internal RFB A and RFB B. Both DAC Latches Loaded with 11111111. Gain Error is Adjustable Using Circuits of Figures 4 and 5.
Gain Temperature Coefficient[3]					
ΔGain/ΔTemperature	–	±0.0035	±0.0035	%/°C max	
Output Leakage Current					
OUT A (Pin 2)	±50	±200	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	±50	±200	±200	nA max	
Input Resistance (V_{REF} A, V_{REF} B)	8	8	8	kΩ min	Input Resistance TC = −300ppm/°C, Typical
	15	15	15	kΩ max	Input Resistance is 11kΩ
V_{REF} A/V_{REF} B Input Resistance Match	±1	±1	±1	% max	
DIGITAL INPUTS[4]					
Input High Voltage					
V_{IH}	2.4	2.4	2.4	V min	
Input Low Voltage					
V_{IL}	0.8	0.8	0.8	V max	
Input Current					
I_{IN}	±1	±10	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance					
DB0–DB7	10	10	10	pF max	
WR, CS, DAC A/DAC B	15	15	15	pF max	
SWITCHING CHARACTERISTICS[3] See Timing Diagram					
Chip Select to Write Set Up Time					
t_{CS}	160	160	210	ns min	
Chip Select to Write Hold Time					
t_{CH}	10	10	10	ns min	
DAC Select to Write Set Up Time					
t_{AS}	160	160	210	ns min	
DAC Select to Write Hold Time					
t_{AH}	10	10	10	ns min	
Data Valid to Write Set Up Time					
t_{DS}	160	160	210	ns min	
Data Valid to Write Hold Time					
t_{DH}	10	10	10	ns min	
Write Pulse Width					
t_{WR}	150	170	210	ns min	
POWER SUPPLY					See Figure 3
I_{DD}, K Grade	2	2	–	mA	All Digital Inputs V_{IL} or V_{IH}
B, T Grades	2	2.5	2.5	mA	All Digital Inputs V_{IL} or V_{IH}
All Grades	100	500	500	μA	All Digital Inputs 0V or V_{DD}

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

V_{DD} = +10.8V to +15.75V. (Measured Using Recommended P.C. Board Layout (Figure 7) and AD644 as Output Amplifiers)

Parameter	T_A = +25°C[1]	T_A = −40°C to +85°C[1]	T_A = −55°C to +125°C[1]	Units	Test Conditions/Comments
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	0.01	0.02	0.02	% per % max	ΔV_{DD} = ±5%
CURRENT SETTLING TIME	350	400	400	ns max	To 1/2LSB. Out A/Out B load = 100Ω. WR = CS = 0V. DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
DIGITAL-TO-ANALOG GLITCH IMPULSE	330	–	–	nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE					
C_{OUT} A	25	25	25	pF max	DAC Latches Loaded with 00000000
C_{OUT} B	25	25	25	pF max	
C_{OUT} A	60	60	60	pF max	DAC Latches Loaded with 11111111
C_{OUT} B	60	60	60	pF max	
AC FEEDTHROUGH					
V_{REF} A to OUT A	−70	−65	−65	dB max	V_{REF} A, V_{REF} B = 20V p-p Sine Wave
V_{REF} B to OUT B	−70	−65	−65	dB max	@ 10kHz
CHANNEL-TO-CHANNEL ISOLATION					Both DAC Latches Loaded with 11111111.
V_{REF} A to OUT B	−80	–	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 10kHz V_{REF} B = 0V see Figure 6.
V_{REF} B to OUT A	−80	–	–	dB typ	V_{REF} B = 20V p-p Sine Wave @ 10kHz V_{REF} A = 0V see Figure 6.
DIGITAL CROSSTALK	60	–	–	nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	−85	–	–	dB typ	V_{IN} = 6V rms @ 1kHz

NOTES
[1]Temperature Ranges are K Version; −40°C to +85°C
B Version; −40°C to +85°C
T Version; −55°C to +125°C
[2]Specification applies to both DACs in AD7628.
[3]Guaranteed by design but not production tested.
[4]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1nA.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	V_{DD} +0.3V
DGND to AGND	V_{DD} +0.3V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{PIN2}, V_{PIN20} to AGND	−0.3V, V_{DD} +0.3V
V_{REF} A, V_{REF} B to AGND	±25V
V_{RFB} A, V_{RFB} B to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (K) Grades	−40°C to +85°C
Industrial (B) Grades	−40°C to +85°C
Extended (T) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Gain Error	Package Option[2]
AD7628KN	−40°C to +85°C	±1/2LSB	±2LSB	N-20
AD7628KP	−40°C to +85°C	±1/2LSB	±2LSB	P-20A
AD7628KR	−40°C to +85°C	±1/2LSB	±2LSB	R-20
AD7628BQ	−40°C to +85°C	±1/2LSB	±2LSB	Q-20
AD7628TQ	−55°C to +125°C	±1/2LSB	±2LSB	Q-20
AD7628TE	−55°C to +125°C	±1/2LSB	±2LSB	E-20A

NOTES

[1]To order MIL-STD-883, Class B process parts, add /883B to part number. Contact your local sales office for military data sheet.

[2]For outline information see Package Information section.

TERMINOLOGY

Relative Accuracy:
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full-scale and is normally expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity:
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

Gain Error:
Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC latches after offset error has been adjusted out. Gain error of both DACs is adjustable to zero with external resistance.

Output Capacitance:
Capacitance from OUT A or OUT B to AGND.

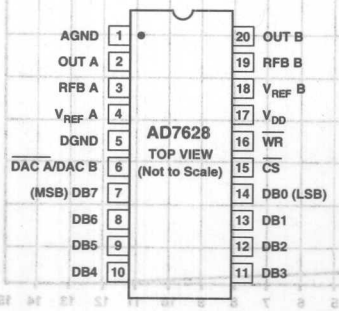
Digital-to-Analog Glitch Impulse:
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{REF} A, V_{REF} B = AGND.

Channel-to-Channel Isolation:
The proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

Digital Crosstalk:
The glitch energy transferred to the output of one converter due to a change in digital input code to the other converter. Specified in nV secs.

PIN CONFIGURATIONS

DIP, SOIC



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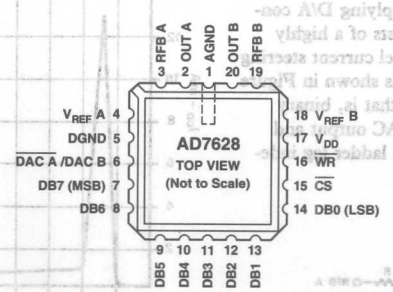
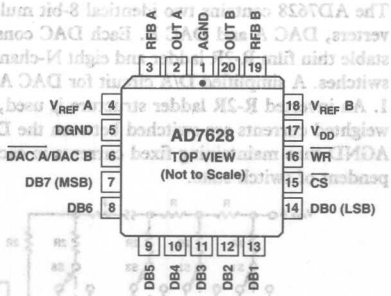


PLCC



INTERFACE LOGIC INFORMATION

DAC Selection:

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

Mode Selection:

Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode:

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

Hold Mode:

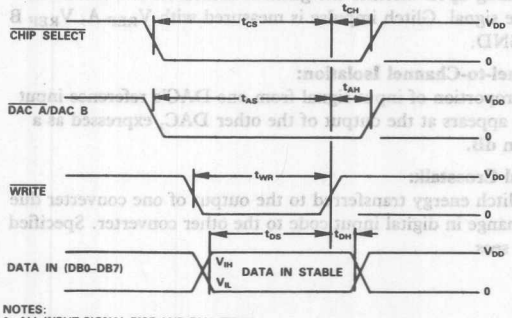
The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{\text{DAC A}}$/DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Mode Selection Table

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. V_{DD} = +10.8V TO +15.75V, $t_R = t_F$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

CIRCUIT INFORMATION – D/A SECTION

The AD7628 contains two identical 8-bit multiplying D/A converters, DAC A and DAC B. Each DAC consists of a highly stable thin film R-2R ladder and eight N-channel current steering switches. A simplified D/A circuit for DAC A is shown in Figure 1. An inverted R-2R ladder structure is used, that is, binary weighted currents are switched between the DAC output and AGND thus maintaining fixed currents in each ladder leg independent of switch state.

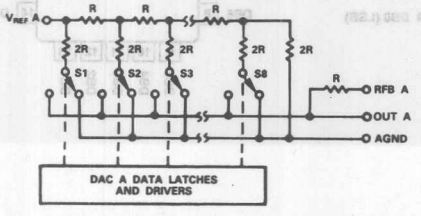


Figure 1. Simplified Functional Circuit for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an approximate equivalent circuit for one of the AD7628's D/A converters, in this case DAC A. A similar equivalent circuit can be drawn for DAC B. Note that AGND (Pin 1) is common for both DAC A and DAC B.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and, as with most semiconductor devices, approximately doubles every 10°C. The resistor R_O as shown in Figure 2 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50pF to 120pF depending upon the digital input. g(V_{REF} A, N) is the Thevenin equivalent voltage generator due to the reference input voltage V_{REF} A and the transfer function of the R-2R ladder.

For further information on CMOS multiplying D/A converters refer to "CMOS DAC Application Guide, 2ND Edition" available from Analog Devices, Publication Number G872a–15–4/86.

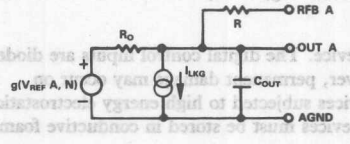


Figure 2. Equivalent Analog Output Circuit of DAC A

CIRCUIT INFORMATION – DIGITAL SECTION

The input buffers are simple CMOS level-shifters designed such that when the AD7628 is operated with V_{DD} from 10.8V to 15.75V, the buffer converts TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 1.0 volt to 2.0 volts the input buffers operate in their linear region and pass a quiescent current, see Figure 3. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7628 may be operated with any supply voltage in the range $10.8 \le V_{DD} \le 15.75$ volts.

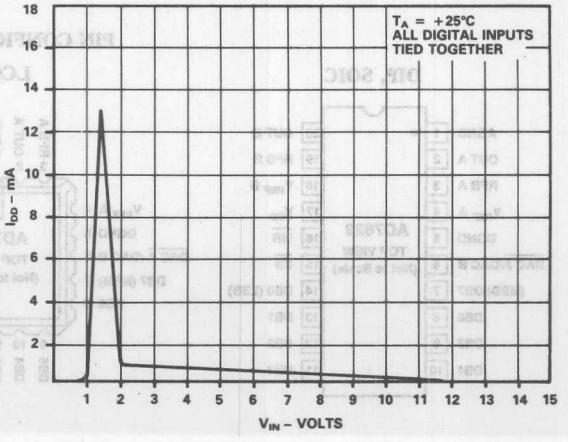


Figure 3. Typical Plot of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN} for V_{DD} = +15V.

5 V/3.3 V Quad and Octal 10-Bit DACs

AD7804/AD7808

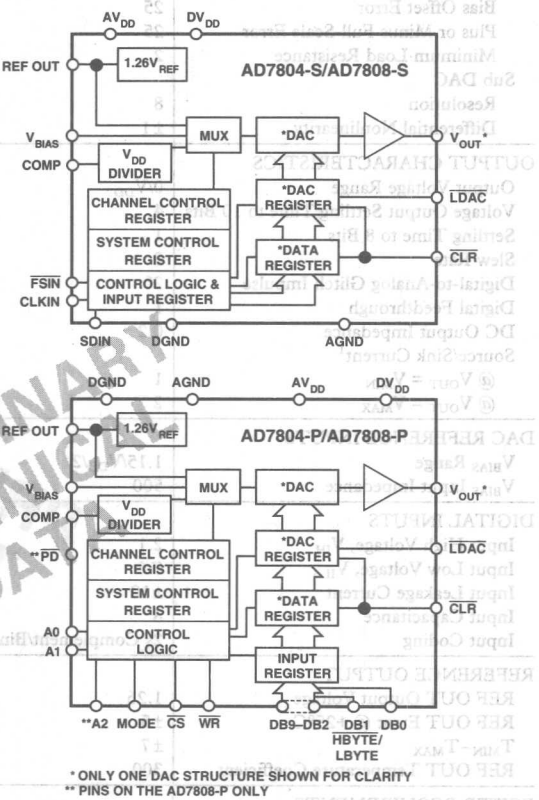
FEATURES

- Four/Eight 10-Bit DACs in One Package
- Serial and Parallel Loading Facilities Available
  - AD7808-S Octal 10-Bit Serial Loading
  - AD7808-P Octal 10-Bit Parallel Loading
  - AD7804-S Quad 10-Bit Serial Loading
  - AD7804-P Quad 10-Bit Parallel Loading
- 3.3 V and 5 V Operation
- Low Power All CMOS Construction
- 10-Bit Resolution, ±1 LSB DNL, ±1 LSB INL
- Four/Eight Output Amplifiers
- Double Buffered DAC Registers
- Power-Down Mode
- Low Cost

APPLICATIONS

- Optical Disk Drives
- Automatic Test Equipment
- Instrumentation Systems
- Communication Systems
- Process Control
- Voltage Set Point Control
- Trim Potentiometer Replacement
- Automatic Calibration

FUNCTIONAL BLOCK DIAGRAMS



* ONLY ONE DAC STRUCTURE SHOWN FOR CLARITY
** PINS ON THE AD7808-P ONLY

GENERAL DESCRIPTION

The AD7804/AD7808 are quad and octal 10-bit digital-to-analog converters, with serial or parallel data load facilities depending on the version used. These parts operate from a +5 V or +3.3 V (±10%) power supply and incorporate an on-board reference. These DACs provide output signals in the form of $V_{BIAS} \pm V_{SWING}$ that swing rail to rail.

On-chip control registers include a system control register and a channel control register. The system control register has control over all DACs in the package. Its controls include power down, input coding select, clearing of all DACs and the facility to put all DACs into standby. The channel control register, allows individual control over all DACs and its contents allow individual DACs to be cleared, put into standby and reference selection for the relevant DAC. The complete transfer function of each individual DAC can be shifted around the V_{BIAS} point using an on-chip 8-bit Sub DAC. All DACs contain double buffered data inputs, which allow all analog outputs to be simultaneously updated using the asynchronous $\overline{LDAC}$ input.

PRODUCT HIGHLIGHTS

1. The AD7804/AD7808 are complete voltage output 10-bit quad and octal DACs capable of operating from 5 V and 3.3 V supplies with on-board reference.
2. CMOS construction ensures very low power dissipation, the part dissipating 5 mW/DAC typically in normal operation.
3. The AD7804-S and AD7808-S have a fast versatile serial interface while the AD7804-P and AD7808-P offer a fast parallel interface. Both interfaces are compatible with all modern microprocessors and microcomputers, and the output voltage settles to ±1/2 LSB within 4 µs.

PRELIMINARY TECHNICAL DATA

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

STATIC PERFORMANCE				
Main DAC				
Resolution	10	10	Bits	
Relative Accuracy	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Bias Offset Error	25	25	mV max	DAC Code = 0.5 Full
Plus or Minus Full-Scale Error	25	25	mV max	Scale
Minimum Load Resistance	2	2	kΩ min	
Sub DAC				
Resolution	8	8	Bits	
Differential Nonlinearity	±1	±1	LSB	Guaranteed Monotonic
OUTPUT CHARACTERISTICS				
Output Voltage Range	$0/V_{DD}$	$0/V_{DD}$	V min/max	
Voltage Output Settling Time to 10 Bits	4	4	µs max	Typically 2 µs
Settling Time to 8 Bits	1	1	µs max	
Slew Rate	2	2	V/µs min	
Digital-to-Analog Glitch Impulse	20	20	nV-s typ	
Digital Feedthrough	1	1	nV-s typ	
DC Output Impedance	0.2	0.2	Ω typ	
Source/Sink Current[1]				
@ $V_{OUT} = V_{MIN}$	1	1	mA max	
@ $V_{OUT} = V_{MAX}$	2	2	mA max	
DAC REFERENCE INPUTS				
V_{BIAS} Range	$1.15/V_{DD}/2$	$1.15/V_{DD}/2$	V min/max	
V_{BIAS} Input Impedance	500	500	kΩ typ	
DIGITAL INPUTS				
Input High Voltage, V_{IH}	2.1	2.4	V min	
Input Low Voltage, V_{IL}	0.6	0.8	V max	
Input Leakage Current	±10	±10	µA max	
Input Capacitance	8	8	pF max	
Input Coding	2s Complement/Binary	2s Complement/Binary		
REFERENCE OUTPUT				
REF OUT Output Voltage	1.26	1.26	V nom	
REF OUT Error @ +25°C	±5	±5	% max	
$T_{MIN}-T_{MAX}$	±7	±7	% max	
REF OUT Temperature Coefficient	300	300	ppm/°C	
POWER REQUIREMENTS				
V_{DD}	3.3 ± 10%	5 ± 10%	V	
I_{DD}				
@ +25°C	2	2.5	mA/DAC max	Excluding Load Currents
$T_{MIN}-T_{MAX}$	2.5	3	mA/DAC max	
Power Dissipation				
Normal Mode @ +25°C	$7.2 + V_O^2/R_L$	$13.75 + V_O^2/R_L$	mW/DAC max	
$T_{MIN}-T_{MAX}$	$9 + V_O^2/R_L$	$16.5 + V_O^2/R_L$	mW/DAC max	
Power Save Mode @ +25°C	1.5	2	µW/DAC max	
$T_{MIN}-T_{MAX}$	2	3	µW/DAC max	

NOTES
[1] $V_{MIN} = V_{BIAS}/16$, $V_{MAX} = 2\ V_{BIAS} - V_{BIAS}/16$.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

TIMING CHARACTERISTICS unless otherwise noted.)

AD7804-S AND AD7808-S

Parameter	Limit at T_A = +25°C	Limit at T_A = –40°C to +85°C	Units	Description
t_1	100	100	ns min	CLKIN Cycle Time
t_2	40	40	ns min	CLKIN High Time
t_3	40	40	ns min	CLKIN Low Time
t_4	30	30	ns min	$\overline{FSIN}$ Setup Time
t_5	30	30	ns min	Data Setup Time
t_6	5	5	ns min	Data Hold Time
t_7	90	90	ns min	$\overline{FSIN}$ Hold Time
t_8	40	40	ns min	$\overline{LDAC}$, $\overline{CLR}$ Pulse Width

NOTE
[1]Guaranteed by design not production tested. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage of 1.6 V.

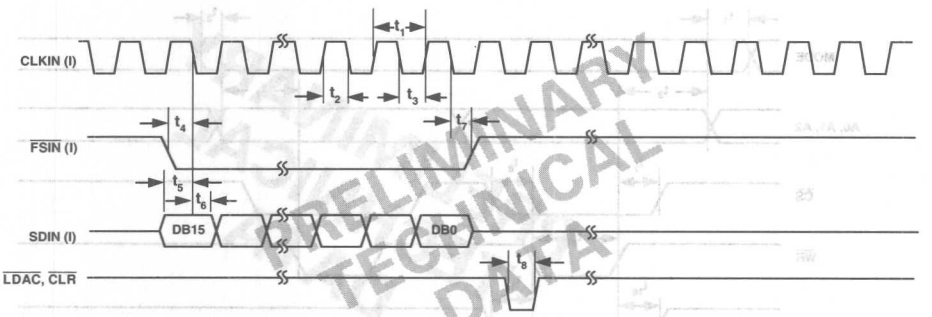


Figure 1. Timing Diagram for AD7804-S and AD7808-S

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7804-P AND AD7808-P

Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Units	Description
t_1	4	4	ns min	Mode Valid to Address Setup Time
t_2	0	0	ns min	Mode Valid to Address Hold Time
t_3	4	4	ns min	Address Valid to Write Setup Time
t_4	0	0	ns min	Address Valid to Write Hold Time
t_5	25	25	ns min	Data Setup Time
t_6	10	10	ns min	Data Hold Time
t_7	0	0	ns min	Chip Select to Write Setup Time
t_8	0	0	ns min	Chip Select to Write Hold Time
t_9	40	40	ns min	Write Pulse Width
t_{10}	0	0	ns min	$\overline{HBEN}$ to Write Setup Time
t_{11}	0	0	ns min	$\overline{HBEN}$ to Write Hold Time
t_{12}	40	40	ns min	$\overline{LDAC}$, $\overline{CLR}$ Pulse Width

NOTE
[1]Guaranteed by design not production tested. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage of 1.6 V.

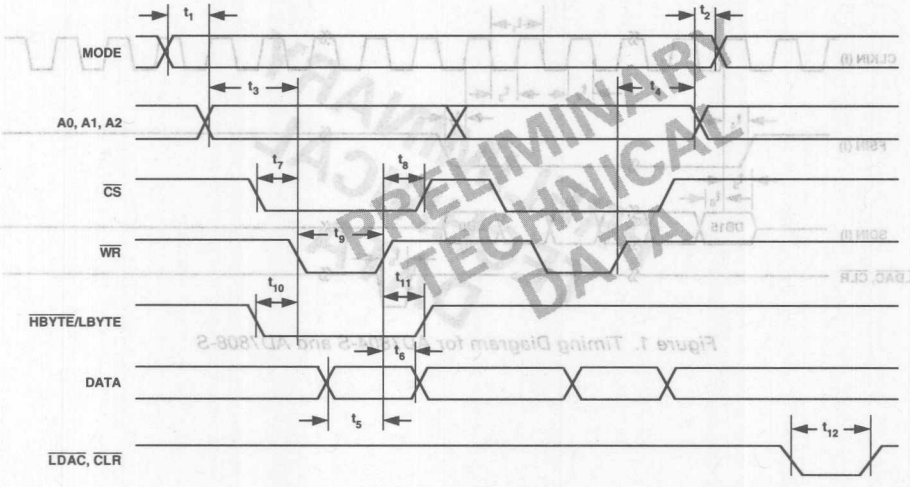


Figure 2. Timing Diagram for AD7804-P and AD7808-P Parallel Write

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PIN DESCRIPTION (AD7804-S and AD7808-S)

Mnemonic	Description
AV_{DD}	Analog Power Supply. +5 V or +3 V.
DV_{DD}	Digital Power Supply.
AGND	Ground reference point for analog circuitry.
DGND	Ground reference point for digital circuitry.
V_{BIAS}	This is an external reference input for the DAC. When this reference is selected for the DAC in the control register, the analog output from the selected DAC swings around this point.
REFOUT	Reference Output; this is a bandgap reference and is typically 1.26 V.
CLKIN	Clock Input. Data is clocked into the input shift register on the falling edges of CLKIN.
$\overline{FSIN}$	Level-triggered control input (active low). This is the frame synchronization signal for the input data. When $\overline{FSIN}$ goes low, it enables the input shift register and data is transferred on the falling edges of CLKIN.
SDIN	Serial Data Input. These devices accept a 16-bit word. The first 2 bits (DB15 and DB14) are used to select either writing to the DACs data registers or to the control registers. If the DAC data register is selected, DB13 is used to select either the Main DAC or the Sub DAC, DB12 to DB10 provide the DAC address and DB9 to DB0 contain the 10-bit data. If control registers are selected by the 2 MSBs, then remaining bits are defined in the section Serial Interface.
$\overline{LDAC}$	Asynchronous $\overline{LDAC}$ Input. When this digital input is taken low, all DAC registers are simultaneously updated with the contents of the DAC data registers.
$\overline{CLR}$	Asynchronous $\overline{CLR}$ Input. When this input is taken low, all DAC register outputs are cleared.
$\overline{COMP}$	Compensation Pin. This is a compensation pin for the internal $V_{DD}/2$ reference and should be decoupled with a 0.1 µF capacitor to analog ground.
V_{OUTA}–V_{OUTD}	Analog output voltages from the DACs.
V_{OUTE}–V_{OUTH}	Analog output voltages from the DACs.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

DV_{DD} to DGND ..... –0.3 V to +7 V
AV_{DD} to AGND ..... –0.3 V to +7 V
AGND to DGND ..... –0.3 V + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Analog Input Voltage to AGND .....–0.3 V to AV_{DD} + 0.3 V
REF OUT to AGND ..... –0.3 V to $+V_{DD}$
V_{BIAS} to AGND ..... –0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] .....±10 mA
Operating Temperature Range
  Commercial Plastic (A, B Versions) .....–40°C to +85°C
Storage Temperature Range .....–65°C to +150°C
Junction Temperature ..... +150°C
SOIC Package, Power Dissipation ..... 875 mW
θ_{JA} Thermal Impedance .....75°C/W
Lead Temperature, Soldering
  Vapor Phase (60 sec) ..... +215°C
  Infrared (15 sec) ..... +220°C
PQFP Package, Power Dissipation ..... 500 mW
θ_{JA} Thermal Impedance .....95°C/W
Lead Temperature, Soldering
  Vapor Phase (60 sec) ..... +215°C
  Infrared (15 sec) ..... +220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latchup.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7804/AD7808 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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AV_{DD}	Analog Power Supply. +5 V or +3.3 V.
DV_{DD}	Digital Power Supply.
AGND	Ground reference point for analog circuitry.
DGND	Ground reference point for digital circuitry.
V_{BIAS}	This is the midpoint for the DAC outputs. The analog output from the DACs swings around this point.
REFOUT	Reference Output; this is a bandgap reference and is typically 1.23 V.
DB9–DB2	Data Inputs. DB9 to DB2 are the 8 MSBs of the data word. DB9 and DB8 function also as the 2 LSBs of the 10-bit word when BYTE loading structure is used.
DB0	Data Input. Functions as the LSB when in the 10-bit parallel mode.
DB1/($\overline{\text{HBYTE}}$/LBYTE)	Data Input in 10-bit parallel mode. Functions as a high byte and low byte enable when BYTE loading structure is selected.
A0, A1, A2	DAC Address Inputs. These digital inputs are used in conjunction with $\overline{\text{CS}}$ and $\overline{\text{WR}}$ to determine which DAC channel control register or DAC data register is loaded from the input register.
$\overline{\text{CS}}$	Chip Select. Active low logic input.
$\overline{\text{WR}}$	Write Input $\overline{\text{WR}}$ is an active low logic input which is used in conjunction with $\overline{\text{CS}}$ and the address pins to write data to the relevant registers.
$\overline{\text{LDAC}}$	Asynchronous $\overline{\text{LDAC}}$ Input. When this digital input is taken low, all DAC registers are simultaneously updated with the contents of the DAC data registers.
$\overline{\text{CLR}}$	Asynchronous $\overline{\text{CLR}}$ Input. When this input is taken low, all Main DAC outputs are cleared either to V_{BIAS} or to $V_{BIAS}/16$ volts. This input does not affect the operation of the Sub DAC.
$\overline{\text{COMP}}$	Compensation Pin. This is a compensation pin for the internal $V_{DD}/2$ reference and should be decoupled with a 0.1 μF capacitor to analog ground.
Mode	Logic Input. Logic enables writing to the DAC input register, a logic 1 enables writing to the selected DACs control register.
V_{OUTA}–V_{OUTD}	Analog output voltages from the DACs.
V_{OUTE}–V_{OUTH}	Analog output voltages from the DACs.

PRELIMINARY TECHNICAL DATA

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The AD7804-S and AD7808-S are serial input devices. Three lines control the serial interface, $\overline{FSIN}$, CLKIN and SDIN. The timing diagram is shown in Figure 1.

When the $\overline{FSIN}$ input goes low, data appearing on the SDIN line is clocked into the input register on each falling edge of CLKIN. When sixteen bits have been received, input register loading is automatically disabled until the next falling edge of $\overline{FSIN}$ is detected. Table I shows the loading sequence for both the AD7804-S and the AD7808-S system control register, Table II shows the sequence for the channel control register and Table III the sequence for loading data to the DAC data registers. Figure 3 shows the internal registers associated with the AD7804-S and AD7808-S serial interface DACs. Only one DAC structure is shown for clarity.

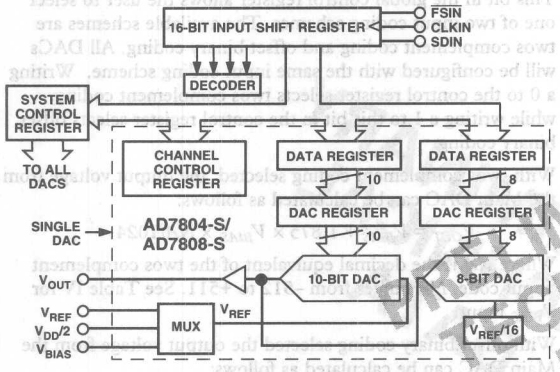

Figure 3. AD7804-S and AD7808-S Internal Registers

cycle accesses the control registers or the DAC data registers. When the system control register is selected by writing zeros to the modes bits MD1 and MD0, the address bits are ignored as the system control register controls all DACs in the package. When MD1 = 0 and MD0 = 1, writing is to the channel control register. Only the DAC selected by the address bits will be affected by writing to this register. Each individual DAC has a channel control register.

The DACs data registers are addressed by writing a one to both MD1 and MD0 (DB15 and DB14 of the input word). DB13 determines whether writing is to the Main DAC data register or to the Sub DAC data register. The Main DAC is 10 bits wide and the Sub DAC is 8 bits wide. Thus when writing to the Sub DAC, DB9 and DB8 become don't cares. The Sub DAC is used the shift the complete transfer function of the Main DAC around its V_{BIAS} point. The Sub DAC has 1/4 LSB resolution and will enable the transfer function to be shifted by $\pm V_{BIAS}/16$.

When the $\overline{LDAC}$ line goes low, all DAC registers in the device are simultaneously loaded with the contents of their respective DAC data registers, and the outputs change accordingly.

Bringing the $\overline{CLR}$ line low resets the DAC data and DAC registers. This hardware clear only effects the Main DAC, the Sub DAC is not effected by issuing a hardware clear to the part. This operation sets the analog output of the Main DAC to $V_{BIAS}/16$ volts when offset binary coding is selected and the output is set to V_{BIAS} when twos complement coding is used.

PRELIMINARY TECHNICAL DATA

Table I. AD7804-S/AD7808-S System Control Register Loading Sequence

MSB															LSB
MD1 = 0	MD0 = 0	X	X	X	X	X	X	0	BIN/$\overline{COMP}$	PD	$\overline{SSTBY}$	$\overline{SCLRM}$	$\overline{SCLRS}$	X	0

Table II. AD7804-S/AD7808-S Channel Control Register Loading Sequence

DB15 (MSB)															DB0 (LSB)
MD1 = 1	MD0 = 0	X	A2	A1	A0	X	X	X	X	X	$\overline{STBY}$	$\overline{CLR}$	MX0	MX1	0

Table III. AD7804-S/AD7808-S DAC Data Register Loading Sequence

DB15 (MSB)															DB0 (LSB)
MD1 = 1	MD0 = 1	$\overline{MAIN}$/SUB	A2	A1	A0	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

X = Don't Care.

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INPUT/CONTROL REGISTERS

Two mode bits (MD1 and MD0), which are the two MSBs of the serial word written to the AD7804-S or the AD7808-S, are used to determine whether writing is to the DAC registers or the control registers for these parts. These parts contain a system control register for controlling the operation of all DACs in the package as well as a channel control register for controlling the operation of each individual DAC. All registers are write-only registers. The following table shows how to access these registers.

Table IV. Register Selection

MD1	MD0	Function
0	0	Write Enable to System Control Register
0	1	Write Enable to Channel Control Register
1	1	Write Enable to DAC Data Registers

Figures 1–3 show the contents of the above registers.

DAC SELECTION (A2, A1, A0)

Bits A2, A1 and A0 in the input register are used to address a specific DAC. The following tables show how the DACs are selected.

Table V. AD7808-S DAC Selection

A2	A1	A0	Function
0	0	0	DAC A Selected
0	0	1	DAC B Selected
0	1	0	DAC C Selected
0	1	1	DAC D Selected
1	0	0	DAC E Selected
1	0	1	DAC F Selected
1	1	0	DAC G Selected
1	1	1	DAC H Selected

Table VI. AD7804-S DAC Selection

A2	A1	A0	Function
X	0	0	DAC A Selected
X	0	1	DAC B Selected
X	1	0	DAC C Selected
X	1	1	DAC D Selected

X = Don't Care.

SYSTEM CONTROL REGISTER (MD1 = 0, MD0 = 0)

This register has control over all DACs in the package. The control bits include power down (PD), DAC input coding select (BIN/$\overline{\text{COMP}}$), global standby ($\overline{\text{SSTBY}}$) and a global clear of all Main DACs ($\overline{\text{SCLRM}}$) and a global clear of all Sub DACs ($\overline{\text{SCLRS}}$). The function of these bits is as follows.

POWER DOWN (PD)

This bit in the control register is used to shut down the complete device. With a 1 in this position, the reference and all DACs are put into low power mode. Writing a 0 to this bit puts the part in the normal operating mode. When in power-down mode the contents of all registers are retained and are valid when the device is taken out of standby.

CODING (BIN/$\overline{\text{COMP}}$)

This bit in the global control register allows the user to select one of two input coding schemes. The available schemes are twos complement coding and offset binary coding. All DACs will be configured with the same input coding scheme. Writing a 0 to the control register selects twos complement coding, while writing a 1 to this bit in the control register selects offset binary coding.

With twos complement coding selected, the output voltage from the Main DAC can be calculated as follows:

$$V_{OUT} = V_{BIAS} + 1.875 \times V_{BIAS} \times NA/1024$$

Where *NA* is the decimal equivalent of the twos complement input code. *NA* ranges from –512 to +511. See Table IV for V_{BIAS} input.

With offset binary coding selected the output voltage from the Main DAC can be calculated as follows:

$$V_{OUT} = V_{BIAS} + 1.875 \times V_{BIAS} \times ((NA - 512)/1024)$$

Where *NA* is the decimal equivalent of the offset binary input code. *NA* ranges from 0 to 1023. See Table IV for V_{BIAS} input.

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SYSTEM STANDBY ($\overline{SSTBY}$)
This bit allows all the DACs in the package to be put into low power mode simultaneously. Writing a 0 to the $\overline{SSTBY}$ bit in the system control register puts all DACs into standby mode. The following changes take place on writing a 0 to this bit. All linear circuitry is switched off . The V_{OUT} from all DACs is connected through a high impedance to ground. The DACs come out of power-down mode when a 1 is written to the $\overline{SSTBY}$ bit. The contents of other locations in the control register are retained when the device is placed in power-down mode and are valid when normal operation is restored.

SYSTEM SOFTWARE CLEAR FUNCTIONS ($\overline{SCLRM}$, $\overline{SCLRS}$)
This function allows the user to clear the contents of all the DAC registers in software. There are two bits available, one to clear all Main DACs and the second to clear all Sub DACs. The output of the Main DAC can be cleared to one of two places depending on the input coding used. Input coding is also programmable through the system control register. If twos complement coding is selected then issuing a software clear will reset the output of the Main DAC to mid-scale (V_{BIAS}). If offset binary coding is selected the output will be reset to $V_{BIAS}/16$ following the execution of a software clear. The Sub DAC will be cleared to midscale regardless of the input coding selected. Writing a zero to the $\overline{SCLRM}$ or $\overline{SCLRS}$ bit in the control register clears the DACs outputs. A 1 in these bit positions puts the DAC in normal operating mode.

CHANNEL CONTROL REGISTER (MD1 = 1, MD0 = 1)
This register allows the user to have control over individual DACs in the package. The control bits in this register include standby ($\overline{STBY}$), individual DAC clear ($\overline{CLR}$) and multiplexer output selection (MX1 and MX0). The function of these bits is as follows.

STANDBY ($\overline{STBY}$)
This bit allows the selected DAC in the package to be put into low power mode. Writing a 0 to the $\overline{STBY}$ bit in the individual control register puts the selected DAC into standby mode. The following changes take place on writing a zero to this bit. All linear circuitry is switched off. The V_{OUT} from the DAC is connected through a high impedance to ground. The DAC is returned to normal operation by writing a 1 to the $\overline{STBY}$ bit. The contents of other locations in the control register are retained when the device is placed in power-down mode and are valid when normal operation is restored.

SOFTWARE CLEAR FUNCTION ($\overline{CLR}$)
This function allows the user to clear the contents of the selected DAC latch in software. This software clear, clears only the Main DAC contents of the Sub DAC. DAC register is unaffected by a $\overline{CLR}$ operation. The output of the Main DAC can be cleared to one of two places depending on the input coding used. Input coding is also programmable through the global control register. If twos complement coding is selected, then issuing a software clear will reset the output of the Main DAC to midscale (V_{BIAS}). If offset binary coding is selected, the output will be reset to $V_{BIAS}/16$ following the execution of a software clear. Writing a 0 to the $\overline{CLR}$ bit in the control register clears the DACs output. A 1 in the $\overline{CLR}$ bit position puts the DAC in normal operating mode.

MULTIPLEXER SELECTION (MX1, MX0)
These two bits are used to select the reference input for the selected DAC. The following table shows the options available.

Table VII. Multiplexer Output Selection

MX1	MX0	V_{BIAS}
0	1	INTERNAL V_{REF}
1	1	$V_{DD}/2$
1	0	EXT V_{BIAS}

SUB DAC DATA REGISTER
Figure 3 shows the loading sequence for writing to the data registers of the DACs. DB13 determines whether writing is to the Main or Sub DACs data register. A one in this position selects the addressed Sub DACs data register. The Sub DAC is eight-bits wide and thus DB9 and DB8 are don't cares when writing to the Sub DAC. This Sub DAC allows the complete transfer function of each individual DAC to be shifted around the V_{BIAS} point. This is achieved by using a Sub DAC whose output is either added or subtracted to the output of the Main DAC. This Sub DAC has a span of $\pm V_{DAC}/16$ with 1/4-bit resolution. An 8-bit DAC is used to implement this function. The output of this Sub DAC is guaranteed monotonic. The coding scheme for the Sub DAC is programmed through the control register. With offset binary coding the transfer function for the Sub DAC is

$$V_{BIAS}/16 \times (2 \times NA/256-1)$$

where NA is the digital code written to the Sub DAC and varies from 0 to 255. See Table IV for V_{BIAS} input.

With twos complement coding the transfer function for the Sub DAC is:

$$V_{BIAS}/8 \times (NB/256)$$

where NB is the digital code written to the Sub DAC and varies from –128 to 127. See Table IV for V_{BIAS} input.

The DAC register for the relevant Sub DAC is selected by writing 0, 1 to the mode bits MD1 and MD0.

PRELIMINARY TECHNICAL DATA

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CONTROL REGISTER (PARALLEL VERSION)

Access to the control register of the AD7804-P and the AD7808-P is achieved by taking the mode pin to a logic high. The control register of these DACs is eight bits wide and is configured as in Tables V and VI. There are two control registers associated with the part. System control register which looks after the input coding, data format, power down, global clear, and global standby. The channel control register contains bits that effect the operation of the selected DAC. The external address bits are used to select the DACs. When mode is high, the two mode bits select which of the control registers is being addressed.

Table VIII. AD7804-P and AD7808-P System Control Register Configuration

DB9									DB0
0	X	SCLRS	SCLRM	SSTBY	PD	BIN/COMP	10/8	X	MD0 = 0

Table IX. AD7804-P and AD7808-P Channel Control Register Configuration

DB9									DB0
X	MX1	MX0	CLR	STBY	X	X	MAIN/SUB	X	MD0 = 1

Each DAC has a separate channel control register. The following is a brief discussion on each bit in these registers.

SYSTEM OR CHANNEL CONTROL REGISTER SELECTION

MD0

0 This enables writing to the system control register. The contents of this are shown in Table VIII. Mode must be low to access this control register.

1 This enables writing to the channel control register. The contents of this are shown in Table IX. Mode must also be low to access this control register.

DATA FORMAT

10/8

0 10-Bit Parallel Loading Structure (Default on Power-Up).

1 Byte Loading Structure (8 + 2 Loading Left Justified Data).

INPUT CODING

BIN/COMP

0 Twos Complement Coding.

1 Offset Binary Coding (Default on Power-Up).

POWER DOWN

PD

0 Normal Operation.

1 Complete Power Down of Device (Default on Power-Up).

SYSTEM STANDBY

SSTBY

0 All DACs in the Package Put in Standby Mode.

1 Normal Operation (Default on Power-Up).

SYSTEM CLEAR

SCLRM & SCLRS

0 All DACs in the package are cleared to a known state depending on the coding scheme selected. The SCLRM bit clears the Main DACs while the SCLRS bit clears the Sub DACs. The Sub DAC is always cleared to mid-scale regardless of the coding. The Main DAC is cleared to different levels depending on the coding scheme. With offset binary coding the output is cleared to $V_{BIAS}/16$. With twos complement coding the output is cleared to V_{BIAS}.

1 Normal Operation (Default on Power-Up).

MAIN DAC OR SUB DAC SELECTION

MAIN/SUB

0 When Mode is taken low, writing to the AD7804/AD7808 loads data to the input register of the selected Sub DAC.

1 Writing to the DAC with MODE low loads data to the input register of the selected Main DAC (Default Condition on Power-Up).

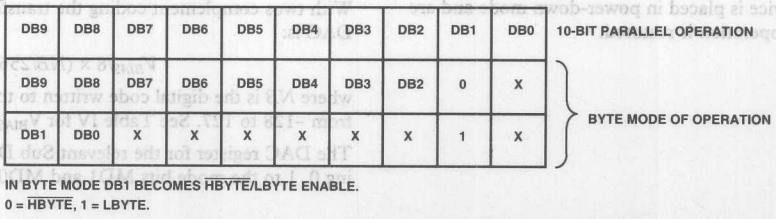

Figure 4. AD7804-P and AD7808-P Parallel & Byte Loading Structure

PRELIMINARY TECHNICAL DATA

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LC²MOS
Complete, Dual 12-Bit MDACs

AD7837/AD7847

FEATURES
- Two 12-Bit MDACS with Output Amplifiers
- 4-Quadrant Multiplication
- Space-Saving 0.3", 24-Pin DIP and 24-Terminal SOIC Package
- Parallel Loading Structure: AD7847
- (8 + 4) Loading Structure: AD7837

APPLICATIONS
- Automatic Test Equipment
- Function Generation
- Waveform Reconstruction
- Programmable Power Supplies
- Synchro Applications

GENERAL DESCRIPTION

The AD7837/AD7847 is a complete, dual, 12-bit multiplying digital-to-analog converter with output amplifiers on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and interface logic. The AD7847 accepts 12-bit parallel data which is loaded into the respective DAC latch using the $\overline{WR}$ input and a separate Chip Select input for each DAC. The AD7837 has a double-buffered 8-bit bus interface structure with data loaded to the respective input latch in two write operations. An asynchronous $\overline{LDAC}$ signal on the AD7837 updates the DAC latches and analog outputs.

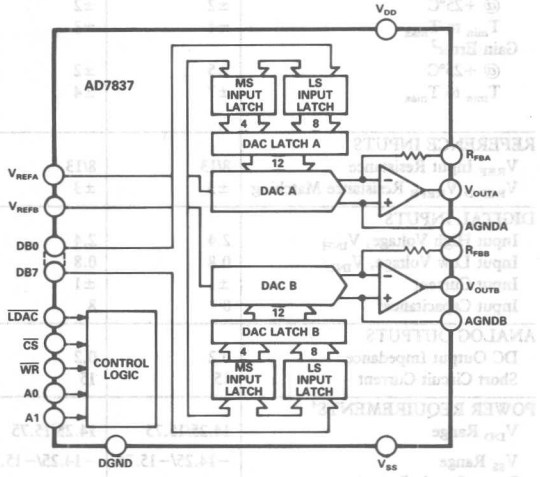
The output amplifiers are capable of developing ±10 V across a 2 kΩ load. They are internally compensated with low input offset voltage due to laser trimming at wafer level.

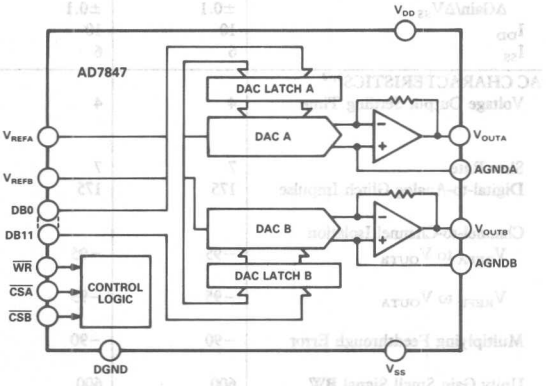
The amplifier feedback resistors are internally connected to V_{OUT} on the AD7847.

The AD7837/AD7847 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic.

A novel low leakage configuration (U.S. Patent No. 4,590,456) ensures low offset errors over the specified temperature range.

FUNCTIONAL BLOCK DIAGRAMS





PRODUCT HIGHLIGHTS

1. The AD7837/AD7847 is a dual, 12-bit, voltage-out MDAC on a single chip. This single chip design offers considerable space saving and increased reliability over multichip designs.
2. The AD7837 and the AD7847 provide a fast versatile interface to 8-bit or 16-bit data bus structures.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter	A Version	B Version	S Version	Units	Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[2]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[2]	±1	±1	±1	LSB max	Guaranteed Monotonic
Zero Code Offset Error[2]					
@ +25°C	±2	±2	±2	mV max	DAC Latch Loaded with All 0s
T_{min} to T_{max}	±4	±3	±5	mV max	Temperature Coefficient = ±5 μV/°C typ
Gain Error[2]					
@ +25°C	±5	±2	±5	LSB max	DAC Latch Loaded with All 1s
T_{min} to T_{max}	±7	±4	±7	LSB max	Temperature Coefficient = ±2 ppm of FSR/°C typ
REFERENCE INPUTS					
V_{REF} Input Resistance	8/13	8/13	8/13	kΩ min/max	Typical Input Resistance = 10 kΩ
V_{REFA}, V_{REFB} Resistance Matching	±3	±3	±3	% max	Typically ±0.5%
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current	±1	±1	±1	μA max	Digital Inputs at 0 V and V_{DD}
Input Capacitance[3]	8	8	8	pF max	
ANALOG OUTPUTS					
DC Output Impedance	0.2	0.2	0.2	Ω typ	
Short Circuit Current	15	15	15	mA typ	V_{OUT} Connected to AGND
POWER REQUIREMENTS[4]					
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	V min/max	
V_{SS} Range	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	V min/max	
Power Supply Rejection					
$\Delta Gain/\Delta V_{DD}$	±0.1	±0.1	±0.1	%per %max	V_{DD} = 15 V ± 5%, V_{REF} = −10 V
$\Delta Gain/\Delta V_{SS}$	±0.1	±0.1	±0.1	%per %max	V_{SS} = −15 V ± 5%, V_{REF} = +10 V
I_{DD}	10	10	10	mA max	Output Unloaded. Typically 5 mA
I_{SS}	6	6	6	mA max	Output Unloaded. Typically 4 mA
AC CHARACTERISTICS[2, 3]					
Voltage Output Settling Time	4	4	4	μs typ	Settling Time to Within ±1/2 LSB of Final Value. DAC Latch Alternately Loaded with All 0s and All 1s
Slew Rate	7	7	7	V/μs typ	
Digital-to-Analog Glitch Impulse	175	175	175	nV secs typ	DAC Latch Alternately Loaded with 01 . . . 11 and 10 . . . 00
Channel-to-Channel Isolation					
V_{REFA} to V_{OUTB}	−95	−95	−95	dB typ	V_{REFA} = 20 V p–p, 10 kHz Sine Wave. DAC Latches Loaded with All 0s
V_{REFB} to V_{OUTA}	−95	−95	−95	dB typ	V_{REFB} = 20 V p–p, 10 kHz Sine Wave. DAC Latches Loaded with All 0s
Multiplying Feedthrough Error	−90	−90	−90	dB typ	V_{REF} = 20 V p–p, 10 kHz Sine Wave. DAC Latch Loaded with All 0s
Unity Gain Small Signal BW	600	600	600	kHz typ	V_{REF} = 100 mV p–p Sine Wave. DAC Latch Loaded with All 1s
Full Power BW	110	110	90	kHz typ	V_{REF} = 20 V p–p Sine Wave. DAC Latch Loaded with All 1s
Total Harmonic Distortion	−88	−88	−88	dB typ	V_{REF} = 6 V rms, 1 kHz. DAC Latch Loaded with All 1s
Digital Crosstalk	10	10	10	nV secs typ	Code Transition from All 0s to All 1s
Output Noise Voltage @ +25°C					See Typical Performance Graphs
(0.1 Hz to 10 Hz)	2	2	2	μV rms typ	Amplifier Noise and Johnson Noise of R_{FB}

NOTES

[1]Temperature Ranges are as follows: A, B Versions, −40°C to +85°C; S Version, −55°C to +125°C.

[2]See Terminology.

[3]Sample tested @+25°C to ensure compliance.

[4]The Devices are functional with V_{DD}/V_{SS} = ±12 V (See typical performance graphs.)

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +15 V ± 5%, V_{SS} = −15 V ± 5%, AGNDA = AGNDB = DGND = 0 V)

Parameter	Limit at T_{min}, T_{max} (A, B Versions)	Limit at T_{min}, T_{max} (S Version)	Units	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	80	100	ns min	$\overline{WR}$ Pulse Width
t_4	80	80	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5	10	10	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6[3]	15	15	ns min	Address to $\overline{WR}$ Setup Time
t_7[3]	15	15	ns min	Address to $\overline{WR}$ Hold Time
t_8[3]	80	100	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Sample tested @ +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 3 and 5.
[3]AD7837 only.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to DGND, AGNDA, AGNDB . . . . . −0.3 V to +17 V
V_{SS}[1] to DGND, AGNDA, AGNDB . . . . . +0.3 V to −17 V
V_{REFA}, V_{REFB} to AGNDA, AGNDB
. . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
AGNDA, AGNDB to DGND . . . . . −0.3 V to V_{DD} +0.3 V
V_{OUTA}[2], V_{OUTB}[2] to AGNDA, AGNDB
. . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
R_{FBA}[3], R_{FBB}[3] to AGNDA, AGNDB
. . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial/Industrial (A, B Versions) . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTES
[1]If V_{SS} is open circuited with V_{DD} and either AGND applied, the V_{SS} pin will float positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode connected between V_{SS} and AGND (cathode to AGND) ensures the Maximum Ratings will be observed.
[2]The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.
[3]AD7837 only.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Option[2]
AD7837AN	−40°C to +85°C	±1 LSB	N-24
AD7837BN	−40°C to +85°C	±1/2 LSB	N-24
AD7837AR	−40°C to +85°C	±1 LSB	R-24
AD7837BR	−40°C to +85°C	±1/2 LSB	R-24
AD7837AQ	−40°C to +85°C	±1 LSB	Q-24
AD7837BQ	−40°C to +85°C	±1/2 LSB	Q-24
AD7837SQ	−55°C to +125°C	±1 LSB	Q-24
AD7847AN	−40°C to +85°C	±1 LSB	N-24
AD7847BN	−40°C to +85°C	±1/2 LSB	N-24
AD7847AR	−40°C to +85°C	±1 LSB	R-24
AD7847BR	−40°C to +85°C	±1/2 LSB	R-24
AD7847AQ	−40°C to +85°C	±1 LSB	Q-24
AD7847BQ	−40°C to +85°C	±1/2 LSB	Q-24
AD7847SQ	−55°C to +125°C	±1 LSB	Q-24

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number.
[2]N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

TERMINOLOGY

Relative Accuray (Linearity)
Relative accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

Zero Code Offset Error
Zero code offset error is the error in output voltage from V_{OUTA} or V_{OUTB} with all 0s loaded into the DAC latches. It is due to a combination of the DAC leakage current and offset errors in the output amplifier.

Gain Error
Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded. It does not include offset error.

Total Harmonic Distortion
This is the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental, expressed in dBs.

Multiplying Feedthrough Error
This is an ac error due to capacitive feedthrough from the V_{REF} input to V_{OUT} of the same DAC when the DAC latch is loaded with all 0s.

Channel-to-Channel Isolation
This is an ac error due to capacitive feedthrough from the V_{REF} input on one DAC to V_{OUT} on the other DAC. It is measured with the DAC latches loaded with all 0s.

Digital Feedthrough
Digital feedthrough is the glitch impulse injected from the digital inputs to the analog output when the data inputs change state, but the data in the DAC latches is not changed.

For the AD7837, it is measured with $\overline{LDAC}$ held high. For the AD7847, it is measured with $\overline{CSA}$ and $\overline{CSB}$ held high.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one converter due to a change in digital code on the DAC latch of the other converter. It is specified in nV secs.

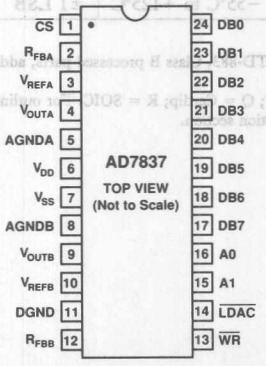
Digital-to-Analog Glitch Impulse
This is the voltage spike that appears at the output of the DAC when the digital code changes, before the output settles to its final value. The energy in the glitch is specified in nV secs and is measured for a 1 LSB change around the major carry transition (0111 1111 1111 to 1000 0000 0000).

Unity Gain Small Signal Bandwidth
This is the frequency at which the small signal voltage output from the output amplifier is 3 dB below its dc level. It is measured with the DAC latch loaded with all 1s.

Full Power Bandwidth
This is the maximum frequency for which a sinusoidal input signal will produce full output at rated load with a distortion less than 3%. It is measured with the DAC latch loaded with all 1s.

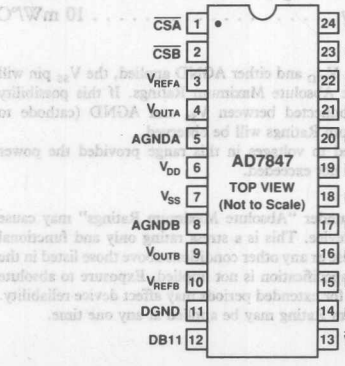
AD7837 PIN CONFIGURATION

DIP & SOIC



AD7847 PIN CONFIGURATION

DIP & SOIC



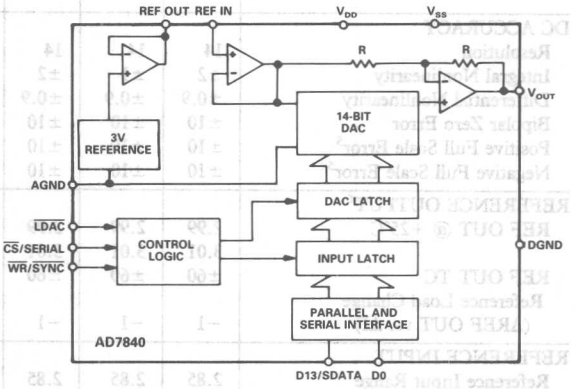
LC²MOS Complete 14-Bit DAC

AD7840

FEATURES

Complete 14-Bit Voltage Output DAC
Parallel and Serial Interface Capability
80dB Signal-to-Noise Ratio
Interfaces to High Speed DSP Processors
e.g., ADSP-2100, TMS32010, TMS32020
45ns min $\overline{WR}$ Pulse Width
Low Power – 70mW typ.
Operates from ±5V Supplies

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7840 is a fast, complete 14-bit voltage output D/A converter. It consists of a 14-bit DAC, 3V buried Zener reference, DAC output amplifier and high speed control logic.

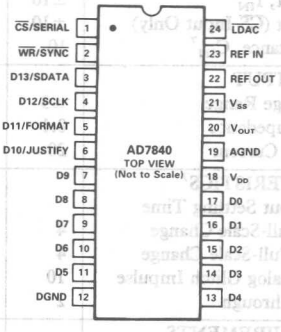
The part features double-buffered interface logic with a 14-bit input latch and 14-bit DAC latch. Data is loaded to the input latch in either of two modes, parallel or serial. This data is then transferred to the DAC latch under control of an asynchronous $\overline{LDAC}$ signal. A fast data setup time of 21ns allows direct parallel interfacing to digital signal processors and high speed 16-bit microprocessors. In the serial mode, the maximum serial data clock rate can be as high as 6MHz.

The analog output from the AD7840 provides a bipolar output range of ±3V. The AD7840 is fully specified for dynamic performance parameters such as signal-to-noise ratio and harmonic distortion as well as for traditional dc specifications. Full power output signals up to 20kHz can be created.

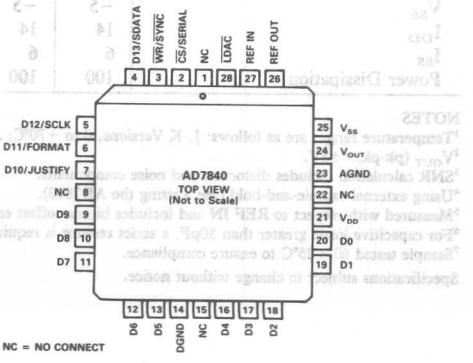
The AD7840 is fabricated in linear compatible CMOS (LC^2MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin plastic and hermetic dual-in-line package (DIP) and is also packaged in a 28-terminal plastic leaded chip carrier (PLCC).

PIN CONFIGURATIONS

DIP



PLCC



NC = NO CONNECT

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

DYNAMIC PERFORMANCE					
Signal to Noise Ratio[3] (SNR)	76	78	76	dB min	V_{OUT}=1kHz Sine Wave, f_{SAMPLE} =100kHz Typically 82dB at +25°C for 0 <V_{OUT}<20kHz[4]
Total Harmonic Distortion (THD)	−78	−80	−78	dB max	V_{OUT}=1kHz Sine Wave, f_{SAMPLE}= 100kHz Typically −84dB at +25°C for 0 <V_{OUT}<20kHz[4]
Peak Harmonic or Spurious Noise	−78	−80	−78	dB max	V_{OUT}=1kHz Sine Wave, f_{SAMPLE}=100kHz Typically −84dB at +25°C for 0 <V_{OUT}<20kHz[4]
DC ACCURACY					
Resolution	14	14	14	Bits	
Integral Nonlinearity	±2	±1	±2	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±10	±10	±10	LSB max	
Positive Full Scale Error[5]	±10	±10	±10	LSB max	
Negative Full Scale Error[5]	±10	±10	±10	LSB max	
REFERENCE OUTPUT[6]					
REF OUT @ +25°C	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	V max	
REF OUT TC	±60	±60	±60	ppm/°C max	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	−1	mV max	Reference Load Current Change (0-500μA)
REFERENCE INPUT					
Reference Input Range	2.85	2.85	2.85	V min	3V ±5%
	3.15	3.15	3.15	V max	
Input Current	50	50	50	μA max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD}=5V ±5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD}=5V ±5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0V to V_{DD}
Input Current (CS Input Only)	±10	±10	±10	μA max	V_{IN} =V_{SS} to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	10	pF max	
ANALOG OUTPUT					
Output Voltage Range	±3	±3	±3	V Nom	
dc Output Impedance	0.1	0.1	0.1	Ω typ	
Short-Circuit Current	20	20	20	mA typ	
AC CHARACTERISTICS[7]					
Voltage Output Settling Time					Settling Time to within ±1/2LSB of Final Value
Positive Full-Scale Change	4	4	4	μs max	Typically 2μs
Negative Full-Scale Change	4	4	4	μs max	Typically 2.5μs
Digital-to-Analog Glitch Impulse	10	10	10	nV secs typ	
Digital Feedthrough	2	2	2	nV secs typ	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	14	14	15	mA max	Output Unloaded, SCLK=+5V. Typically 10mA
I_{SS}	6	6	7	mA max	Output Unloaded, SCLK=+5V. Typically 4mA
Power Dissipation	100	100	110	mW max	Typically 70mW

NOTES

[1]Temperature ranges are as follows: J, K Versions, 0 to +70°C; A, B Versions, −25°C to +85°C; S Version, −55°C to +125°C.

[2]V_{OUT} (pk-pk)=±3V.

[3]SNR calculation includes distortion and noise components.

[4]Using external sample-and-hold (see Testing the AD7840).

[5]Measured with respect to REF IN and includes bipolar offset error.

[6]For capacitive loads greater than 50pF, a series resistor is required (see Internal Reference section).

[7]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5V ±5%, V_{SS} = −5V ±5%, AGND = DGND = 0V.)

Parameter	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (S Version)	Units	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	45	50	ns min	$\overline{WR}$ Pulse Width
t_4	21	28	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5	10	15	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6	40	40	ns min	$\overline{LDAC}$ Pulse Width
t_7	50	50	ns min	$\overline{SYNC}$ to SCLK Falling Edge
t_8[3]	150	200	ns min	SCLK Cycle Time
t_9	30	40	ns min	Data Valid to SCLK Setup Time
t_{10}	75	100	ns min	Data Valid to SCLK Hold Time
t_{11}	75	100	ns min	$\overline{SYNC}$ to SCLK Hold Time

NOTE
[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr= tf= 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
[2]See Figures 6 and 8.
[3]SCLK mark/space ratio is 40/60 to 60/40.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3V to +7V
V_{SS} to AGND . . . . . +0.3V to −7V
AGND to DGND . . . . . −0.3V to V_{DD} +0.3V
V_{OUT} to AGND . . . . . V_{SS} to V_{DD}
REF OUT to AGND . . . . . 0V to V_{DD}
REF IN to AGND . . . . . −0.3V to V_{DD} +0.3V
Digital Inputs to DGND . . . . . −0.3V to V_{DD} +0.3V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above +75°C by . . . . . 10mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

Model[1]	Temperature Range	SNR (dB)	Integral Nonlinearity (LSB)	Package Option[2]
AD7840JN	0 to +70°C	78 min	±2 max	N-24
AD7840KN	0 to +70°C	80 min	±1 max	N-24
AD7840JP	0 to +70°C	78 min	±2 max	P-28A
AD7840KP	0 to +70°C	80 min	±1 max	P-28A
AD7840AQ	−25°C to +85°C	78 min	±2 max	Q-24
AD7840BQ	−25°C to +85°C	80 min	±1 max	Q-24
AD7840SQ[3]	−55°C to +125°C	78 min	±2 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet and availability.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.
[3]This grade will be available to /883B processing only.

PIN FUNCTION DESCRIPTION

DIP Pin No.	Pin Mnemonic	Function
1	$\overline{CS}$/SERIAL	Chip Select/Serial Input. When driven with normal logic levels, it is an active low logic input which is used in conjunction with $\overline{WR}$ to load parallel data to the input latch. For applications where $\overline{CS}$ is permanently low, an R, C is required for correct power-up (see $\overline{LDAC}$ input). If this input is tied to V_{SS}, it defines the AD7840 for serial mode operation.
2	$\overline{WR}$/$\overline{SYNC}$	Write/Frame Synchronization Input. In the parallel data mode, it is used in conjunction with $\overline{CS}$ to load parallel data. In the serial mode of operation, this pin functions as a Frame Synchronization pulse with serial data expected after the falling edge of this signal.
3	D13/SDATA	Data Bit 13(MSB)/Serial Data. When parallel data is selected, this pin is the D13 input. In serial mode, SDATA is the serial data input which is used in conjunction with $\overline{SYNC}$ and SCLK to transfer serial data to the AD7840 input latch.
4	D12/SCLK	Data Bit 12/Serial Clock. When parallel data is selected, this pin is the D12 input. In the serial mode, it is the serial clock input. Serial data bits are latched on the falling edge of SCLK when $\overline{SYNC}$ is low.
5	D11/FORMAT	Data Bit 11/Data Format. When parallel data is selected, this pin is the D11 input. In serial mode, a logic 1 on this input indicates that the MSB is the first valid bit in the serial data stream. A logic 0 indicates that the LSB is the first valid bit (see Table I).
6	D10/JUSTIFY	Data Bit 10/Data Justification. When parallel data is selected, this pin is the D10 input. In serial mode, this input controls the serial data justification (see Table I).
7–11	D9–D5	Data Bit 9 to Data Bit 5. Parallel data inputs.
12	DGND	Digital Ground. Ground reference for digital circuitry.
13–16	D4–D1	Data Bit 4 to Data Bit 1. Parallel data inputs.
17	D0	Data Bit 0 (LSB). Parallel data input.
18	V_{DD}	Positive Supply, +5V± 5%.
19	AGND	Analog Ground. Ground reference for DAC, reference and output buffer amplifier.
20	V_{OUT}	Analog Output Voltage. This is the buffer amplifier output voltage. Bipolar output range (±3V with REF IN = +3V).
21	V_{SS}	Negative Supply Voltage, −5V ±5%.
22	REF OUT	Voltage Reference Output. The internal 3V analog reference is provided at this pin. To operate the AD7840 with internal reference, REF OUT should be connected to REF IN. The external load capability of the reference is 500μA.
23	REF IN	Voltage Reference Input. The reference voltage for the DAC is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7840 is 3V.
24	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded into the DAC latch from the input latch on the falling edge of this signal (see Interface Logic Information section). The AD7840 should be powered-up with $\overline{LDAC}$ high. For applications where $\overline{LDAC}$ is permanently low, an R, C is required for correct power-up (see Figure 19).

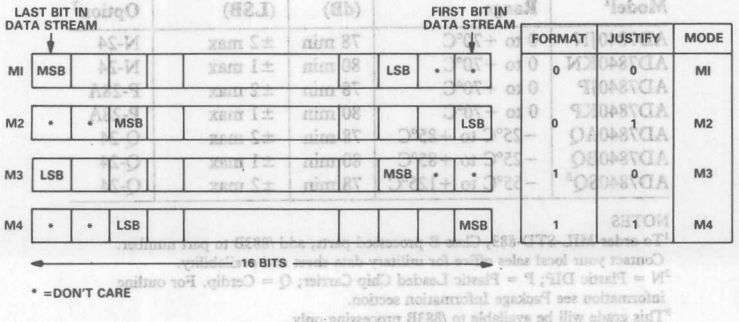


Table I. Serial Data Modes

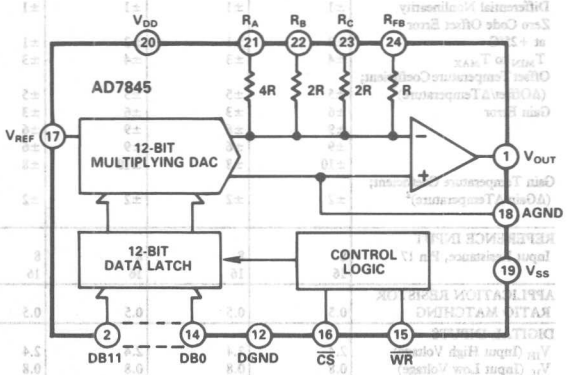
LC²MOS Complete 12-Bit Multiplying DAC

AD7845

FEATURES
- 12-Bit CMOS MDAC with Output Amplifier
- 4-Quadrant Multiplication
- Guaranteed Monotonic (T_{MIN} to T_{MAX})
- Space-Saving 0.3" DIPs and 24- or 28-Terminal Surface Mount Packages
- Application Resistors On Chip for Gain Ranging, etc.
- Low Power LC²MOS

APPLICATIONS
- Automatic Test Equipment
- Digital Attenuators
- Programmable Power Supplies
- Programmable Gain Amplifiers
- Digital-to-4–20 mA Converters

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7845 is the industry's first 4-quadrant multiplying D/A converter with an on-chip amplifier. It is fabricated on the LC²MOS process, which allows precision linear components and digital circuitry to be implemented on the same chip.

The 12 data inputs drive latches which are controlled by standard $\overline{CS}$ and $\overline{WR}$ signals, making microprocessor interfacing simple. For stand-alone operation, the $\overline{CS}$ and $\overline{WR}$ inputs can be tied to ground, making all latches transparent. All digital inputs are TTL and 5 V CMOS compatible.

The output amplifier can supply ±10 V into a 2 kΩ load. It is internally compensated, and its input offset voltage is low due to laser trimming at wafer level. For normal operation, R_{FB} is tied to V_{OUT}, but the user may alternatively choose R_A, R_B or R_C to scale the output voltage range.

PRODUCT HIGHLIGHTS

1. Voltage Output Multiplying DAC
   The AD7845 is the first DAC which has a full 4-quadrant multiplying capability and an output amplifier on chip. All specifications include amplifier performance.
2. Matched Application Resistors
   Three application resistors provide an easy facility for gain ranging, voltage offsetting, etc.
3. Space Saving
   The AD7845 saves space in two ways. The integration of the output amplifier on chip means that chip count is reduced. The part is housed in skinny 24-pin, 0.3" DIP, 28-terminal LCC and PLCC and 24-terminal SOIC packages.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ACCURACY								
Resolution	12	12	12	12	12	12	Bits	1 LSB = $\frac{V_{REF}}{2^{12}}$ = 2.4 mV
Relative Accuracy								
at +25°C	±1	±1/2	±1	±1/2	±1	±1/2	LSB max	All Grades Are Guaranteed
T_{MIN} to T_{MAX}	±1	±3/4	±3/2	±1	±2	±1	LSB max	Monotonic over Temperature
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	DAC Register Loaded with All 0s.
Zero Code Offset Error								
at +25°C	±2	±1	±2	±1	±2	±1	mV max	
T_{MIN} to T_{MAX}	±4	±3	±4	±3	±5	±4	mV max	
Offset Temperature Coefficient; (ΔOffset/ΔTemperature)[2]	±5	±5	±5	±5	±5	±5	µV/°C typ	
Gain Error	±6	±3	±6	±3	±6	±3	LSB max	R_{FB}, V_{OUT} Connected
	±9	±6	±9	±6	±9	±6	LSB max	R_C, V_{OUT} Connected, V_{REF} = +5 V
	±9	±6	±9	±6	±9	±6	LSB max	R_B, V_{OUT} Connected, V_{REF} = +5 V
	±10	±8	±10	±8	±10	±8	LSB max	R_A, V_{OUT} Connected, V_{REF} = +2.5 V
Gain Temperature Coefficient; (ΔGain/ΔTemperature)[2]	±2	±2	±2	±2	±2	±2	ppm of FSR/°C typ	R_{FB}, V_{OUT} Connected
REFERENCE INPUT								
Input Resistance, Pin 17	8	8	8	8	8	8	kΩ min	Typical Input Resistance = 12 kΩ
	16	16	16	16	16	16	kΩ max	
APPLICATION RESISTOR RATIO MATCHING	0.5	0.5	0.5	0.5	0.5	0.5	% max	Matching Between R_A, R_B, R_C
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)	±1	±1	±1	±1	±1	±1	µA max	Digital Inputs at 0 V and V_{DD}
C_{IN} (Input Capacitance)[2]	7	7	7	7	7	7	pF max	
POWER SUPPLY[4]								
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	V min/V max	
V_{SS} Range	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	V min/V max	
Power Supply Rejection								
ΔGain/ΔV_{DD}	±0.2	±0.2	±0.2	±0.2	±0.2	±0.2	% per % max	V_{DD} = +15 V ± 5%, V_{REF} = −10 V
ΔGain/ΔV_{SS}	±0.2	±0.2	±0.2	±0.2	±0.2	±0.2	% per % max	V_{SS} = −15 V ± 5%.
I_{DD}	10	10	10	10	10	10	mA max	V_{OUT} Unloaded
I_{SS}	4	4	4	4	4	4	mA max	V_{OUT} Unloaded

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance and are not subject to test.

DYNAMIC PERFORMANCE								
Output Voltage Settling Time	5	5	5	5	5	5	µs max	To 0.01% of Full-Scale Range. V_{OUT} Load = 2 kΩ, 100 pF. DAC Register Alternately Loaded with All 0s and All 1s. Typically 2.5 µs at 25°C.
Slew Rate	7	7	7	7	7	7	V/µs typ	V_{OUT} Load = 2 kΩ, 100 pF.
Digital-to-Analog Glitch Impulse	450	450	450	450	450	450	nV-s typ	Measured with V_{REF} = 0 V. DAC Register Alternately Loaded with All 0s and All 1s.
Multiplying Feedthrough Error[3]	5	5	5	5	5	5	mV p-p typ	V_{REF} = ±10 V, 10 kHz Sine Wave DAC Register Loaded with All 0s.
Unity Gain Small Signal Bandwidth	600	600	600	600	600	600	kHz typ	V_{OUT}, R_{FB} Connected. DAC Loaded with All 1s. V_{REF} = 100 mV p-p Sine Wave.
Full Power Bandwidth	250	250	250	250	250	250	kHz typ	V_{OUT}, R_{FB} Connected. DAC Loaded with All 1s. V_{REF} = 20 V p-p Sine Wave. R_L = 2 kΩ.
Total Harmonic Distortion	−90	−90	−90	−90	−90	−90	dB typ	V_{REF} = 6 V rms, 1 kHz Sine Wave.
OUTPUT CHARACTERISTICS[5]								
Open Loop Gain	85	85	85	85	85	85	dB min	V_{OUT}, R_{FB} Not Connected
Output Voltage Swing	±10	±10	±10	±10	±10	±10	V min	V_{OUT} = ±10 V, R_L = 2 kΩ
Output Resistance	0.2	0.2	0.2	0.2	0.2	0.2	Ω typ	R_L = 2 kΩ, C_L = 100 pF
Short Circuit Current @ +25°C	15	15	15	15	15	15	mA typ	R_{FB}, V_{OUT} Connected, V_{OUT} Shorted to AGND
Output Noise Voltage (0.1Hz to 10Hz) @ +25°C	2	2	2	2	2	2	µV rms typ	Includes Noise Due to Output Amplifier and Johnson Noise of R_{FB}
f = 10 Hz	250	250	250	250	250	250	nV/√Hz typ	
f = 100 Hz	100	100	100	100	100	100	nV/√Hz typ	
f = 1 kHz	50	50	50	50	50	50	nV/√Hz typ	
f = 10 kHz	50	50	50	50	50	50	nV/√Hz typ	
f = 100 kHz	50	50	50	50	50	50	nV/√Hz typ	

NOTES

[1]Temperature Ranges are as follows: J, K Versions: 0 to +70°C; A, B Versions: −25°C to +85°C; S, T Versions: −55°C to +125°C.

[2]Sample tested to ensure compliance.

[3]The metal lid on the ceramic D-24A package is connected to Pin 12 (DGND).

[4]The device is functional with a power supply of ±12 V.

[5]Minimum specified load resistance is 2 kΩ.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = +15 V, ± 5%. V_{SS} = −15 V, ± 5%. V_{REF} = +10 V. AGND = DGND = 0 V.)

Parameter	Limit at T_A = +25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_{CS}	100	135	140	ns min	Chip Select to Write Setup Time
t_{CH}	0	0	0	ns min	Chip Select to Write Hold Time
t_{WR}	100	135	140	ns min	Write Pulse Width
t_{DS}	100	100	120	ns min	Data Setup Time
t_{DH}	20	20	20	ns min	Data Hold Time

Specifications subject to change without notice.

3

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND . . . . . −0.3 V to +17 V
V_{SS} to DGND . . . . . +0.3 V to −17 V
V_{REF} to AGND . . . . . ±25 V
V_{RFB} to AGND . . . . . ±25 V
V_{RA} to AGND . . . . . ±25 V
V_{RB} to AGND . . . . . ±25 V
V_{RC} to AGND . . . . . ±25 V
V_{OUT} to AGND[1] . . . . . V_{DD} +0.3 V, V_{SS} −0.3 V
AGND to DGND . . . . . −0.3 V, V_{DD}
Digital Input Voltage to DGND . . . . −0.3 V to V_{DD} + 0.3 V
Power Dissipation (Any Package)
To +75°C . . . . . 650 mW
Derates above +75°C . . . . . .10 mW/°C

Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

NOTE
[1]V_{OUT} may be shorted to AGND provided that the power dissipation of the package is not exceeded.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

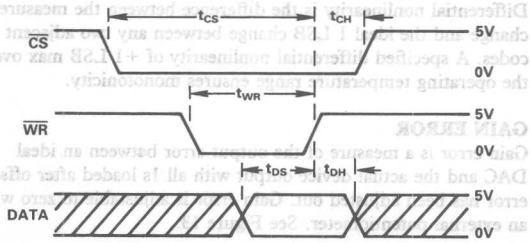
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Package Option[3]
AD7845JN	0°C to +70°C	±1 LSB	N-24
AD7845KN	0°C to +70°C	±1/2 LSB	N-24
AD7845JP	0°C to +70°C	±1 LSB	P-28A
AD7845KP	0°C to +70°C	±1/2 LSB	P-28A
AD7845JR	0°C to +70°C	±1 LSB	R-24
AD7845KR	0°C to +70°C	±1/2 LSB	R-24
AD7845AQ	−25°C to +85°C	±1 LSB	Q-24
AD7845BQ	−25°C to +85°C	±1/2 LSB	Q-24
AD7845SQ/883B	−55°C to +125°C	±1 LSB	Q-24
AD7845TQ/883B	−55°C to +125°C	±1/2 LSB	Q-24
AD7845SE/883B	−55°C to +125°C	±1 LSB	E-28A

NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-24A) or cerdip (Q-24) hermetic packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

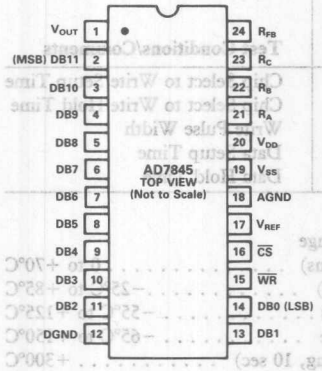


NOTES
1. All input signal rise and fall times measured from 10% to 90% of +5V. $t_R = t_F = 20$ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

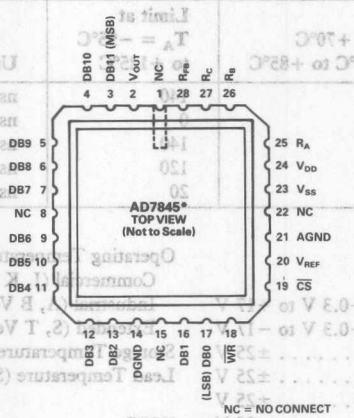
Figure 1. AD7845 Timing Diagram

PIN CONFIGURATIONS

DIP, SOIC

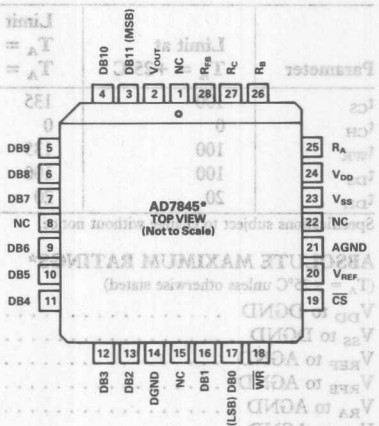


LCC



NC = NO CONNECT

PLCC



NC = NO CONNECT

TERMINOLOGY

LEAST SIGNIFICANT BIT

This is the analog weighting of 1 bit of the digital word in a DAC. For the AD7845, 1LSB = $\frac{V_{REF}}{2^{12}}$.

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for both endpoints (i.e., offset and gain error are adjusted out) and is normally expressed in least significant bits or as a percentage of full-scale range.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of +1 LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out. Gain error is adjustable to zero with an external potentiometer. See Figure 13.

ZERO CODE OFFSET ERROR

This is the error present at the device output with all 0s loaded in the DAC. It is due to the op amp input offset voltage and bias current and the DAC leakage current.

TOTAL HARMONIC DISTORTION

This is the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental, expressed in dBs.

OUTPUT NOISE

This is the noise due to the white noise of the DAC and the input noise of the amplifier.

DIGITAL-TO-ANALOG GLITCH IMPULSE

This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. The measurement takes place with V_{REF} = AGND.

DIGITAL FEEDTHROUGH

When the DAC is not selected (i.e., $\overline{CS}$ is high) high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up as noise on the V_{OUT} pin. This noise is digital feedthrough.

MULTIPLYING FEEDTHROUGH ERROR

This is ac error due to capacitive feedthrough from the V_{REF} terminal to V_{OUT} when the DAC is loaded with all 0s.

OPEN-LOOP GAIN

Open-loop gain is defined as the ratio of a change of output voltage to the voltage applied at the V_{REF} pin with all 1s loaded in the DAC. It is specified at dc.

UNITY GAIN SMALL SIGNAL BANDWIDTH

This is the frequency at which the magnitude of the small signal voltage gain of the output amplifier is 3 dB below unity. The device is operated as a closed-loop unity gain inverter (i.e., DAC is loaded with all 1s).

OUTPUT RESISTANCE

This is the effective output source resistance.

FULL POWER BANDWIDTH

Full power bandwidth is specified as the maximum frequency, at unity closed-loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding a distortion level of 3%.

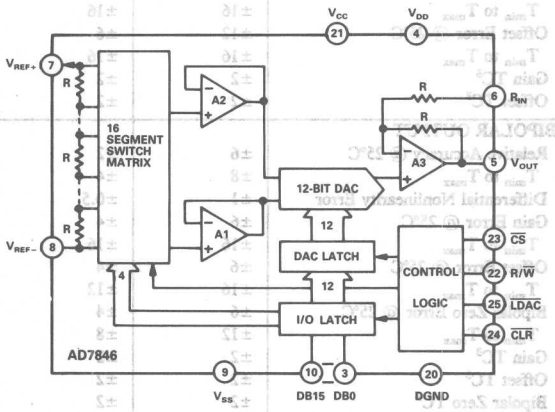
LC²MOS 16-Bit Voltage Output DAC

AD7846

FEATURES

16-Bit Monotonicity over Temperature
±2LSBs Integral Linearity Error
Microprocessor Compatible with Readback Capability
Unipolar or Bipolar Output
Multiplying Capability
Low Power (100mW typical)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7846 is a 16-bit DAC constructed with Analog Devices' LC²MOS process. It has V_{REF+} and V_{REF-} reference inputs and an on-chip output amplifier. These can be configured to give a unipolar output range (0 to +5V, 0 to +10V) or bipolar output ranges (±5V, ±10V).

The DAC uses a segmented architecture. The 4MSBs in the DAC latch select one of the segments in a 16-resistor string. Both taps of the segment are buffered by amplifiers and fed to a 12-bit DAC, which provides a further 12 bits of resolution. This architecture ensures 16-bit monotonicity. Excellent integral linearity results from tight matching between the input offset voltages of the two buffer amplifiers.

In addition to the excellent accuracy specifications, the AD7846 also offers a comprehensive microprocessor interface. There are 16 data I/O pins, plus control lines ($\overline{CS}$, R/$\overline{W}$, $\overline{LDAC}$ and $\overline{CLR}$). R/$\overline{W}$ and $\overline{CS}$ allow writing to and reading from the I/O latch. This is the readback function which is useful in ATE applications. $\overline{LDAC}$ allows simultaneous updating of DACs in a multi-DAC system and the $\overline{CLR}$ line will reset the contents the DAC latch to 00 . . . 000 or 10 . . . 000 depending on the state of R/$\overline{W}$. This means that the DAC output can be reset to 0V in both the unipolar and bipolar configurations.

The AD7846 is available in 28-pin plastic, ceramic, LCCC and PLCC packages.

PRODUCT HIGHLIGHTS

1. 16-Bit Monotonicity
   The guaranteed 16-bit monotonicity over temperature makes the AD7846 ideal for closed-loop applications.
2. Readback
   The ability to read back the DAC register contents minimizes software routines when the AD7846 is used in ATE systems.
3. Power Dissipation
   Power dissipation of 100mW makes the AD7846 the lowest power, high accuracy DAC on the market.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7846—SPECIFICATIONS[1]

(V_{DD} = +14.25V to +15.75V, V_{SS} = −14.25V to −15.75V, V_{CC} = +4.75V to +5.25V. V_{OUT} loaded with 2kΩ, 1000pF to 0V. V_{REF+} = +5V, R_{IN} connected to 0V. All specifications T_{MIN} to T_{MAX} unless otherwise stated.)

Parameter	J, A Versions	K, B Versions	S Version[2]	Units	Test Conditions/Comments
Resolution	16	16	16	Bits	
UNIPOLAR OUTPUT					V_{REF-}=0V, V_{OUT}=0V to +10V
Relative Accuracy @ 25°C	±12	±4	±12	LSB typ	1LSB=153μV
T_{min} to T_{max}	±16	±8	±16	LSB max	
Differential Nonlinearity Error	±1	±0.5	±1	LSB max	All Grades Guaranteed Monotonic
Gain Error @ 25°C	±12	±6	±12	LSB typ	V_{OUT} Load=10MΩ
T_{min} to T_{max}	±16	±16	±24	LSB max	
Offset Error @ 25°C	±12	±6	±12	LSB typ	
T_{min} to T_{max}	±16	±16	±24	LSB max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
BIPOLAR OUTPUT					V_{REF-}=−5V, V_{OUT}=−10V to +10V
Relative Accuracy @ 25°C	±6	±2	±6	LSB typ	1LSB=305μV
T_{min} to T_{max}	±8	±4	±8	LSB max	
Differential Nonlinearity Error	±1	±0.5	±1	LSB max	All Grades Guaranteed Monotonic
Gain Error @ 25°C	±6	±4	±6	LSB typ	V_{OUT} Load=10MΩ
T_{min} to T_{max}	±16	±16	±16	LSB max	
Offset Error @ 25°C	±6	±4	±6	LSB typ	V_{OUT} Load=10MΩ
T_{min} to T_{max}	±16	±12	±16	LSB max	
Bipolar Zero Error @ 25°C	±6	±4	±6	LSB typ	
T_{min} to T_{max}	±12	±8	±16	LSB max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
Bipolar Zero TC[3]	±2	±2	±2	ppm FSR/°C typ	
REFERENCE INPUT					
Input Resistance	20	20	20	kΩ min	Resistance from V_{REF-} to V_{REF+}
	40	40	40	kΩ max	Typically 30kΩ
V_{REF+} Range	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	Volts	
V_{REF-} Range	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	Volts	
OUTPUT CHARACTERISTICS					
Output Voltage Swing	V_{SS}+4 to V_{DD}−3	V_{SS}+4 to V_{DD}−3	V_{SS}+4 to V_{DD}−3	V max	
Resistive Load	2	2	3	kΩ min	To 0V
Capacitive Load	1000	1000	1000	pF max	To 0V
Output Resistance	0.3	0.3	0.3	Ω typ	
Short Circuit Current	±25	±25	±25	mA typ	To 0V or Any Power Supply
DIGITAL INPUTS					
V_{IH} (Input High Voltage)	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	V max	
I_{IN} (Input Current)	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	10	10	10	pF max	
DIGITAL OUTPUTS					
V_{OL} (Output Low Voltage)	0.4	0.4	0.4	Volts max	I_{SINK}=1.6mA
V_{OH} (Output High Voltage)	4.0	4.0	4.0	Volts min	I_{SOURCE}=400μA
Floating State Leakage Current	±10	±10	±10	μA max	DB0-DB15=0 to V_{CC}
Floating State Output Capacitance[3]	10	10	10	pF max	
POWER REQUIREMENTS[4]					
V_{DD}	+11.4/+15.75	+11.4/+15.75	+11.4/+15.75	Vmin/Vmax	
V_{SS}	−11.4/−15.75	−11.4/−15.75	−11.4/−15.75	Vmin/Vmax	
V_{CC}	+4.75/+5.25	+4.75/+5.25	+4.75/+5.25	Vmin/Vmax	
I_{DD}	5	5	5	mA max	V_{OUT} Unloaded
I_{SS}	5	5	5	mA max	V_{OUT} Unloaded
I_{CC}	1	1	1	mA max	
Power Supply Sensitivity[5]	1.5	1.5	2	LSB/V max	
Power Dissipation	100	100	100	mW typ	V_{OUT} Unloaded

NOTES

[1]Temperature Ranges as follows: J, K Versions: 0 to +70°C; A, B Versions: −25°C to +85°C; S Version: −55°C to +125°C.

[2]Minimum load for S version is 3kΩ.

[3]Sample tested to ensure compliance.

[4]AD7846 is functional with power supplies of ±12V. See Typical Performance Curves.

[5]Sensitivity of Gain Error, Offset Error and Bipolar Zero Error to V_{DD}, V_{SS} variations.

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test. (V_{REF+} = +5V, V_{DD} = +14.25V to +15.75V, V_{SS} = −14.25V to −15.75V, V_{CC} = +4.75V to +5.25V, R_{IN} connected to 0V.)

Parameter	T_A = 25°C	T_A = T_{min} to T_{max}	Units	Test Conditions/Comments
Output Settling Time	7	7	µs max	To 0.006% FSR. V_{OUT} loaded. V_{REF-} = 0V.
	9	9	µs max	To 0.003% FSR. V_{OUT} loaded. V_{REF-} = −5V.
Digital-to-Analog Glitch Impulse	400	400	nV-secs typ	DAC alternately loaded with 10 . . . 0000 and 01 . . . 1111. V_{OUT} unloaded.
AC Feedthrough	0.5	0.5	mV pk-pk typ	V_{REF-} = 0V, V_{REF+} = 1V rms, 10kHz sine wave. DAC loaded with all 0s.
Digital Feedthrough	10	10	nV-secs typ	DAC alternately loaded with all 1s and all 0s. $\overline{CS}$ High.
Output Noise Voltage Density (1kHz–100kHz)	50	50	nV/√Hz typ	Measured at V_{OUT}. DAC loaded with 0111011 . . . 11. V_{REF+} = V_{REF-} = 0V.

TIMING CHARACTERISTICS (V_{DD} = +14.25V to +15.75V, V_{SS} = −14.25V to −15.75V, V_{CC} = +4.75V to +5.25V.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	40	40	50	ns min	R/$\overline{W}$ to $\overline{CS}$ Setup Time
t_2	150	160	190	ns min	$\overline{CS}$ Pulse Width (Write Cycle)
t_3	40	40	50	ns min	R/$\overline{W}$ to $\overline{CS}$ Hold Time
t_4	110	110	120	ns min	Data Setup Time
t_5	0	0	0	ns min	Data Hold Time
t_6	230	270	320	ns max	Data Access Time
t_7	10	10	10	ns min	Bus Relinquish Time
	80	90	90	ns max	
t_8	20	20	20	ns min	$\overline{CLR}$ Setup Time
t_9	150	150	150	ns min	$\overline{CLR}$ Pulse Width
t_{10}	0	0	0	ns min	$\overline{CLR}$ Hold Time
t_{11}	80	100	100	ns min	$\overline{LDAC}$ Pulse Width
t_{12}	240	280	330	ns min	$\overline{CS}$ Pulse Width (Read Cycle)

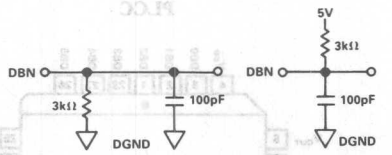
NOTES

[1]Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

[2]t_6 is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

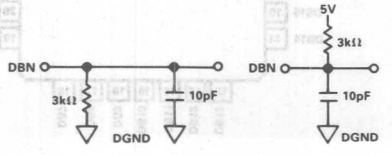
[3]t_7 is defined as the time required for an output to change 0.5V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.



a. High Z to V_{OH} b. High Z to V_{OL}

Figure 1. Load Circuits for Access Time (t_6)



a. V_{OH} to High Z b. V_{OL} to High Z

Figure 2. Load Circuits for Bus Relinquish Time (t_7)

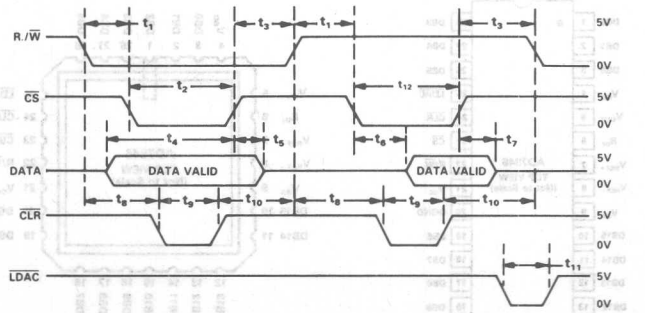


Figure 3. AD7846 Timing Diagram

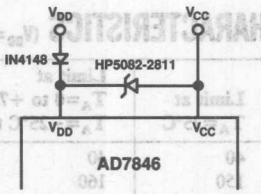
ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to DGND[2] . . . . . −0.3V or +17V
V_{CC} to DGND[2] . . . . . −0.3V, V_{DD} +0.3V or +7V (Whichever Is Lower)
V_{SS} to DGND . . . . . +0.3V to −17V
V_{REF+} to DGND . . . . . ±25V
V_{REF-} to DGND . . . . . ±25V
V_{OUT} to DGND[3] . . . . . ±25V
R_{IN} to DGND . . . . . ±25V
Digital Input Voltage to DGND . . . . . −0.3V to V_{CC} +0.3V
Digital Output Voltage to DGND . . . . . −0.3V to V_{CC} +0.3V
Power Dissipation (Any Package)
To +75°C 1000mW
Derates above +75°C . . . . . 10mW/°C
Operating Temperature Range
J, K Versions . . . . . 0 to +70°C
A, B Versions . . . . . −25°C to +85°C
S Version . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

[2]V_{CC} must not exceed V_{DD} by more than 0.3V. If it is possible for this to happen during power supply sequencing, the following diode protection scheme will ensure protection.



[3]V_{OUT} may be shorted to DGND, V_{DD}, V_{SS}, V_{CC} provided that the power dissipation of the package is not exceeded.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option*
AD7846JN	0°C to +70°C	±16 LSB	N-28
AD7846KN	0°C to +70°C	±8 LSB	N-28
AD7846JP	0°C to +70°C	±16 LSB	P-28A
AD7846KP	0°C to +70°C	±8 LSB	P-28A
AD7846AQ	−25°C to +85°C	±16 LSB	Q-28
AD7846BQ	−25°C to +85°C	±8 LSB	Q-28
AD7846SQ/883B	−55°C to +125°C	±16 LSB	Q-28
AD7846SE/883B	−55°C to +125°C	±16 LSB	E-28A

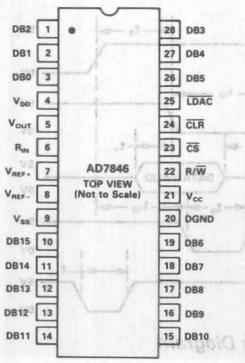
*Q = Ceramic DIP; E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

CAUTION

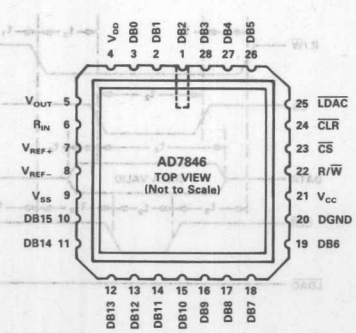
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

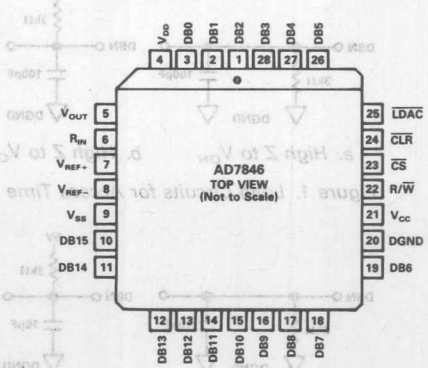
DIP



LCCC



PLCC



Serial Input, 14-Bit/16-Bit DAC

AD7849

FEATURES
14-Bit/16-Bit Multiplying DAC
Guaranteed Monotonicity
Output Control on Power-Up and Power-Down
Internal or External Control
Versatile Serial Interface
DAC Clears to 0 V in Both Unipolar and Bipolar Output Ranges

APPLICATIONS
Industrial Process Control
PC Analog I/O Boards
Instrumentation

GENERAL DESCRIPTION

The AD7849 is a 14-bit/16-bit serial input multiplying DAC. The DAC architecture ensures excellent differential linearity performance, and monotonicity is guaranteed to 14 bits for the A grade and to 16 bits for all other grades over the specified temperature ranges.

During power-up and power-down sequences (when the supply voltages are changing), the V_{OUT} pin is clamped to 0 V via a low impedance path. To prevent the output of A3 being shorted to 0 V during this time, transmission gate G1 is also opened. These conditions are maintained until the power supplies stabilize and a valid word is written to the DAC register. At this time, G2 opens and G1 closes. Both transmission gates are also externally controllable via the Reset In ($\overline{RST\ IN}$) control input. For instance, if the $\overline{RST\ IN}$ input is driven from a battery supervisor chip, then on power-off or during a brown out, the $\overline{RST\ IN}$ input will be driven low to open G1 and close G2. The DAC must be reloaded, with $\overline{RST\ IN}$ high, to re-enable the output. Conversely, the on-chip voltage detector output ($\overline{RST\ OUT}$) is also available to the user to control other parts of the system.

The AD7849 has a versatile serial interface structure and can be controlled over three lines to facilitate opto-isolator applications.

SDOUT is the output of the on-chip shift register and can be used in a daisy-chain fashion to program devices in the multi-channel system. The DCEN (Daisy Chain Enable) input controls this function.

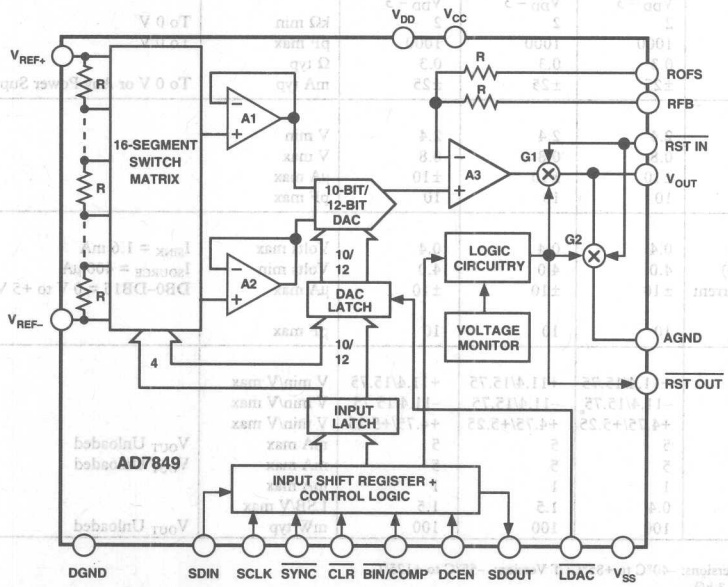
The $\overline{BIN}$/COMP pin sets the DAC coding; with $\overline{BIN}$/COMP set to 0, the coding is straight binary; and with it set to 1, the coding is 2s complement. This allows the user to reset the DAC to 0 V in both the unipolar and bipolar output ranges.

In addition, the output loop is closed externally allowing the user to accurately drive remote loads using force and sense techniques.

The part is available in a 20-pin DIP and 20-pin SOIC package.

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	A Versions	B, T Versions	C Versions	Units	Test Conditions/Comments
Resolution	14	16	16	Bits	A Versions: 1 LSB = 2 (V_{REF+}–V_{REF-})/2^{14} B, C, T Versions: 1 LSB = 2 (V_{REF+}–V_{REF-})/2^{16}
UNIPOLAR OUTPUT					V_{REF-} = 0 V, V_{OUT} = 0 V to +10 V
Relative Accuracy	±4	±16	±4	LSBs max	
Differential Nonlinearity	±0.25	±0.9	±0.5	LSBs max	All Grades Guaranteed Monotonic Over Temperature
Gain Error @ +25°C	±3	±12	±6	LSBs max	V_{OUT} Load = 10 MΩ
T_{MIN} to T_{MAX}	±4	±16	±16	LSBs max	
Offset Error @ +25°C	±3	±12	±6	LSBs max	
T_{MIN} to T_{MAX}	±4	±16	±16	LSBs max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
BIPOLAR OUTPUT					V_{REF-} = –5 V, V_{OUT} = –10 V to +10 V
Relative Accuracy	±2	±8	±2	LSBs max	
Differential Nonlinearity	±0.25	±0.9	±0.5	LSBs max	All Grades Guaranteed Monotonic Over Temperature
Gain Error @ +25°C	±1.5	±6	±4	LSBs max	V_{OUT} Load = 10 MΩ
T_{MIN} to T_{MAX}	±3	±12	±8	LSBs max	
Offset Error @ +25°C	±1.5	±6	±4	LSBs max	
T_{MIN} to T_{MAX}	±3	±12	±8	LSBs max	
Bipolar Zero Error @ +25°C	±1.5	±6	±4	LSBs max	
T_{MIN} to T_{MAX}	±3	±12	±8	LSBs max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
Bipolar Zero TC[3]	±2	±2	±2	ppm FSR/°C typ	
REFERENCE INPUT					
Input Resistance	20 40	20 40	20 40	kΩ min kΩ max	Resistance from V_{REF+} to V_{REF-} Typically 30 kΩ
V_{REF+} Range	V_{SS} + 6 to V_{DD} – 6	V_{SS} + 6 to V_{DD} – 6	V_{SS} + 6 to V_{DD} – 6	Volts	
V_{REF-} Range	V_{SS} + 6 to V_{DD} – 6	V_{SS} + 6 to V_{DD} – 6	V_{SS} + 6 to V_{DD} – 6	Volts	
OUTPUT CHARACTERISTICS					
Output Voltage Swing	V_{SS} + 4 to V_{DD} – 3	V_{SS} + 4 to V_{DD} – 3	V_{SS} + 4 to V_{DD} – 3	V max	
Resistive Load	2	2	2	kΩ min	To 0 V
Capacitive Load	1000	1000	1000	pF max	To 0 V
Output Resistance	0.3	0.3	0.3	Ω typ	
Short Circuit Current	±25	±25	±25	mA typ	To 0 V or Any Power Supply
DIGITAL INPUTS					
V_{INH}, Input High Voltage	2.4	2.4	2.4	V min	
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
I_{INH}, Input Current	±10	±10	±10	µA max	
C_{IN}, Input Capacitance	10	10	10	pF max	
DIGITAL OUTPUTS					
V_{OL} (Output Low Voltage)	0.4	0.4	0.4	Volts max	I_{SINK} = 1.6 mA
V_{OH} (Output High Voltage)	4.0	4.0	4.0	Volts min	I_{SOURCE} = 400 µA
Floating State Leakage Current	±10	±10	±10	µA max	DB0–DB15 = 0 V to +5 V
Floating State Output Capacitance	10	10	10	pF max	
POWER REQUIREMENTS					
V_{DD}	+11.4/15.75	+11.4/15.75	+11.4/15.75	V min/V max	
V_{SS}	–11.4/15.75	–11.4/15.75	–11.4/15.75	V min/V max	
V_{CC}	+4.75/+5.25	+4.75/+5.25	+4.75/+5.25	V min/V max	
I_{DD}	5	5	5	mA max	V_{OUT} Unloaded
I_{SS}	5	5	5	mA max	V_{OUT} Unloaded
I_{CC}	1	1	1	mA max	
Power Supply Sensitivity[4]	0.4	1.5	1.5	LSB/V max	
Power Dissipation	100	100	100	mW typ	V_{OUT} Unloaded

NOTES
[1]Temperature ranges: A, B, C Versions: –40°C to +85°C; T Version: –55°C to +125°C.
[2]Minimum load for T Version is 3 kΩ.
[3]Sample tested to ensure compliance.
[4]Sensitivity of gain error, offset error and bipolar zero error to V_{DD}, V_{SS} variations.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	All Versions	Units	Test Conditions/Comments
V_A, Low Threshold Voltage for V_{DD}, V_{SS}	1	Volt max	This is the lower V_{DD}/V_{SS} threshold voltage for the reset function. Above this, the reset is activated.
	0	Volts typ	
V_B, High Threshold Voltage for V_{DD}, V_{SS}	8.5	Volts max	This is the higher V_{DD}/V_{SS} threshold voltage for the reset function. Below this, the reset is activated. Typically 8 volts.
	7.5	Volts min	
V_C, Low Threshold Voltage for V_{CC}	1	Volt max	This is the lower threshold voltage for the reset function. Above this, the reset is activated.
	0	Volts typ	
V_D, High Threshold Voltage for V_{CC}	3.5	Volts max	This is the higher V_{CC} threshold voltage for the reset function. Below this, the reset is activated. Typically 3 volts.
	2.5	Volts min	
G2 R_{ON}	1	kΩ max	On Resistance of G2; V_{DD} = 2 V; V_{SS} = –2 V; I_{G2} = 1 mA.

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS (These characteristics are included for Design Guidance and are not subject to test. (V_{REF+} = +5 V; V_{DD} = +11.4 V to +15.75 V; V_{SS} = –11.4 V to –15.75 V; V_{CC} = 4.75 V to 5.25 V; R_{IN} connected to 0 V.)

Parameter	T Version[1]	A, B, C Versions	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Output Settling Time	7	7	µs max	To 0.006% FSR. V_{OUT} Loaded. V_{REF-} = 0 V.
	7	7	µs max	To 0.003% FSR. V_{OUT} Loaded. V_{REF-} = –5 V.
Digital to Analog Glitch Impulse	400	400	nV-s typ	DAC Alternately Loaded with 10 . . . 00 and 011 . . . 11. V_{OUT} Unloaded. $\overline{LDAC}$ Permanently Low.
	100	100	nV-s typ	$\overline{LDAC}$ Frequency = 100 kHz
AC Feedthrough	0.5	0.5	mV pk-pk typ	V_{REF-} = 0 V, V_{REF+} = 1 V rms, 10 kHz Sine Wave. DAC Loaded with All 0s.
Digital Feedthrough	10	10	nV-s typ	DAC Alternately Loaded with All 1s and All 0s. $\overline{SYNC}$ High.
Output Noise Voltage Density 1 kHz–100 kHz	50	50	nV/√Hz	Measured at V_{OUT}. DAC Loaded with 0111011 . . . 111. V_{REF+} = V_{REF-} = 0 V.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +11.4 V to +15.75 V; V_{SS} = –11.4 V to –15.75 V; V_{CC} = 4.75 V to 5.25 V; R_L = 2 kΩ, C_L = 200 pF. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (All Versions)	Units	Conditions/Comments
t_1	200	200	ns min	SCLK Cycle Time
t_2	50	50	ns min	$\overline{SYNC}$ to SCLK Setup Time
t_3	30	30	ns min	$\overline{SYNC}$ to SCLK Hold Time
t_4	60	60	ns min	$\overline{BIN}$/COMP to SCLK Setup Time
t_5	10	10	ns min	Data Setup Time
t_6	100	100	ns min	Data Hold Time
t_7[4]	80	80	ns max	SCLK Rising Edge to SDO Valid
t_8	80	80	ns min	$\overline{LDAC}$, $\overline{CLR}$ Pulse Width
t_r	100	100	µs max	Digital Input Rise Time
t_f	100	100	µs max	Digital Input Fall Time

NOTES
[1]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Guaranteed by characterization.
[3]SCLK mark/space ratio range is 40/60 to 60/40.
[4]SDO load capacitance is 50 pF.

PRELIMINARY TECHNICAL DATA

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ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	–0.3 V to +17 V
V_{CC} to DGND	–0.3 V, V_{DD} + 0.3 V or +7 V (Whichever Is Lower)
V_{SS} to DGND	–0.3 V to –17 V
V_{REF+} to DGND	±25 V
V_{REF-} to DGND	±25 V
V_{OUT} to DGND[2]	±25 V
R_{IN} to DGND	±25 V
Digital Input Voltage to DGND	–0.3 V to V_{CC} + 0.3 V
Input Current to any Pin Except Supplies[3]	±10 mA
Operating Temperature Range	
Commercial/Industrial (B Versions)	–40°C to +85°C
Extended (S Versions)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
DIP Package, Power Dissipation	875 mW
θ_{JA} Thermal Impedance	75°C/W
Lead Temperature (Soldering, 10 secs)	+260°C
SOIC Package, Power Dissipation	875 mW
θ_{JA} Thermal Impedance	75°C/W
Lead Temperature, Soldering	
Vapor Phase (60 secs)	+215°C
Infrared (15 secs)	+220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]V_{OUT} may be shorted to DGND, V_{DD}, V_{SS}, provided that the power dissipation of the package is not exceeded.

[3]Transient currents of up to 100 mA will not cause SCR latch-up.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7849 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PRELIMINARY TECHNICAL DATA

ORDERING GUIDE

Model	Temperature Range	Resolution (Bits)	Bipolar INL (LSBs)	Package Option*
AD7849AN	–40°C to +85°C	14	±2	N-20
AD7849BN	–40°C to +85°C	16	±8	N-20
AD7849CN	–40°C to +85°C	16	±2	N-20
AD7849AR	–40°C to +85°C	14	±2	R-20
AD7849BR	–40°C to +85°C	16	±8	R-20
AD7849CR	–40°C to +85°C	16	±2	R-20
AD7849TQ	–55°C to +125°C	16	±8	Q-20

*N = Plastic DIP; R = SOP (Small Outline Package); Q = Cerdip. For outline information see Package Information section.

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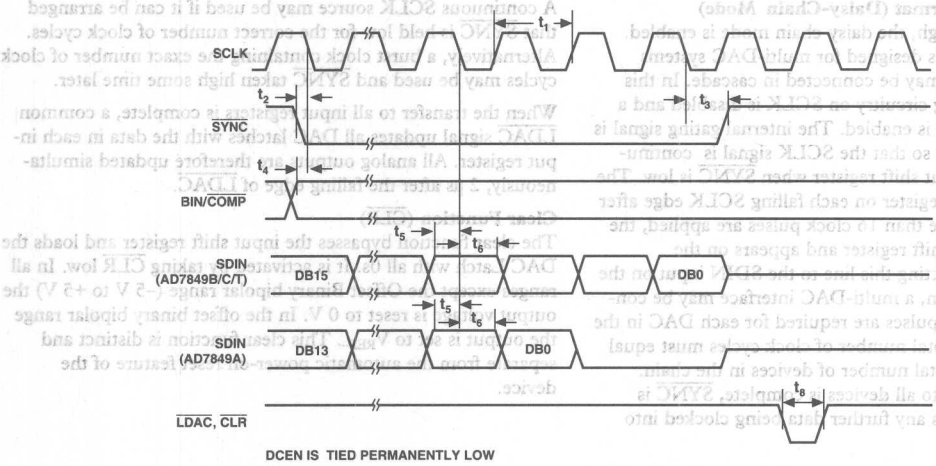


Figure1. Timing Diagram (Stand-Alone Mode)

DIGITAL INTERFACE

The AD7849 contains an input serial to parallel shift register and a DAC latch. A simplified diagram of the input loading circuitry is shown in Figure 2. Serial data on the SDIN input is loaded to the input register under control of DCEN, $\overline{\text{SYNC}}$ and, SCLK. When a complete word is held in the shift register, it may then be loaded into the DAC latch under control of $\overline{\text{LDAC}}$. Only the data in the DAC latch determines the analog output on the AD7849.

The DCEN (daisy-chain enable) input is used to select either a stand-alone mode or a daisy-chain mode. The loading format is slightly different depending on which mode is selected .

Serial Data Loading Format (Stand-Alone Mode)

With DCEN at logic 0 the stand-alone mode is selected. In this mode a low $\overline{\text{SYNC}}$ input provides the frame synchronization signal which tells the AD7849 that valid serial data on the SDIN input will be available for the next 16 falling edges of SCLK. An internal counter/decoder circuit provides a low gating signal so that only 16 data bits are clocked into the input shift register. After 16 SCLK pulses the internal gating signal goes inactive (high) thus locking out any further clock pulses. Therefore either a continuous clock or a burst clock source may be used to clock in the data.

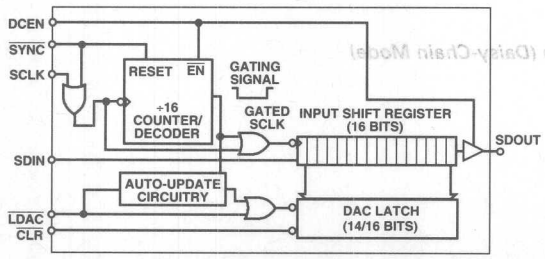


Figure 2. Simplified Loading Structure

The $\overline{\text{SYNC}}$ input is taken high after the complete 16-bit word is loaded in.

The AD7849B, AD7849C and AD7849T versions are 16-bit resolution DACs and have a straight 16-bit load format, with the MSB (DB15) being loaded first. The AD7849A is a 14-bit DAC, but the loading structure is still 16-bit. The MSB (DB13) is loaded first and the final two bits of the 16-bit stream must be 0s.

There are two ways in which the DAC latch and hence the analog output may be updated. The status of the $\overline{\text{LDAC}}$ input is examined after $\overline{\text{SYNC}}$ is taken low. Depending on its status, one of two update modes is selected.

If $\overline{\text{LDAC}}$ = 0, then the automatic update mode is selected. In this mode the DAC latch and analog output are updated automatically when the last bit in the serial data stream is clocked in. The update thus takes place on the sixteenth falling SCLK edge.

If $\overline{\text{LDAC}}$ = 1, then the automatic update is disabled. The DAC latch update and output update are now separate. The DAC latch is updated on the falling edge of $\overline{\text{LDAC}}$. However, the output update is delayed for a further 2 µs by means of an internal track-and-hold amplifier in the output stage. This function results in lower digital-to-analog glitch impulse at the DAC output. Note that the $\overline{\text{LDAC}}$ input must be taken back high again before the next data transfer is initiated.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Serial Data Loading Format (Daisy-Chain Mode)
By connecting DCEN high, the daisy-chain mode is enabled. This mode of operation is designed for multi-DAC systems where several AD7849s may be connected in cascade. In this mode, the internal gating circuitry on SCLK is disabled and a serial data output facility is enabled. The internal gating signal is permanently active (low) so that the SCLK signal is continuously applied to the input shift register when $\overline{SYNC}$ is low. The data is clocked into the register on each falling SCLK edge after $\overline{SYNC}$ going low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDOUT line. By connecting this line to the SDIN input on the next AD7849 in the chain, a multi-DAC interface may be constructed. Sixteen SCLK pulses are required for each DAC in the system. Therefore, the total number of clock cycles must equal $16 \times N$ where N is the total number of devices in the chain. When the serial transfer to all devices is complete, $\overline{SYNC}$ is taken high. This prevents any further data being clocked into the input register.

A continuous SCLK source may be used if it can be arranged that $\overline{SYNC}$ is held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles may be used and $\overline{SYNC}$ taken high some time later.

When the transfer to all input registers is complete, a common $\overline{LDAC}$ signal updates all DAC latches with the data in each input register. All analog outputs are therefore updated simultaneously, 2 µs after the falling edge of $\overline{LDAC}$.

Clear Function ($\overline{CLR}$)
The clear function bypasses the input shift register and loads the DAC Latch with all 0s. It is activated by taking $\overline{CLR}$ low. In all ranges except the Offset Binary bipolar range (–5 V to +5 V) the output voltage is reset to 0 V. In the offset binary bipolar range the output is set to V_{REF-}. This clear function is distinct and separate from the automatic power-on reset feature of the device.

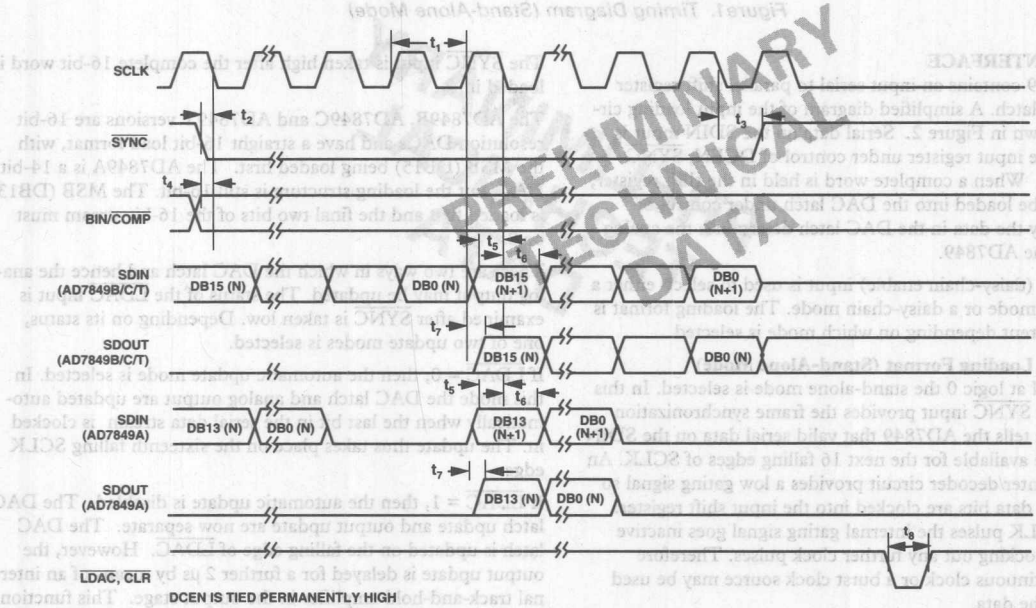
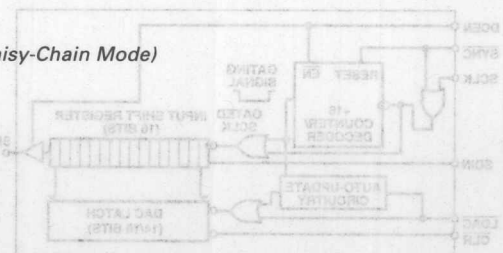


Figure 3. Timing Diagram (Daisy-Chain Mode)

PRELIMINARY TECHNICAL DATA



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

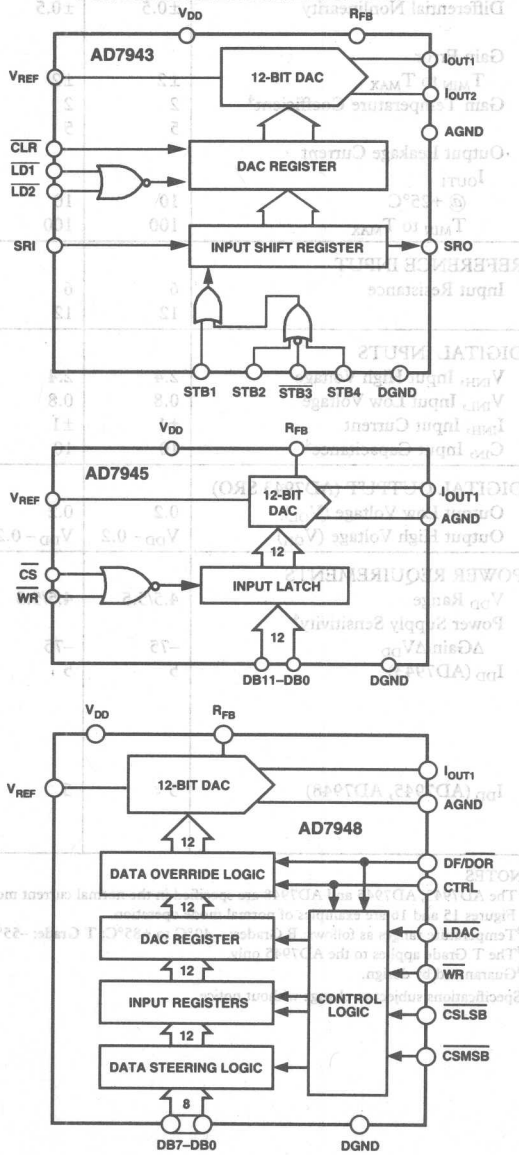
+3.3 V/+5 V Multiplying 12-Bit DACs

AD7943/AD7945/AD7948

FEATURES
12-Bit Multiplying DACs
Guaranteed Specifications with +3.3 V/+5 V Supply
0.5 LSBs INL and DNL
Low Power: 5 μW typ
Fast Interface
40 ns Strobe Pulse Width (AD7943)
40 ns Write Pulse Width (AD7945, AD7948)
Low Glitch: 60 nV-s with Amplifier Connected
Fast Settling: 600 ns to 0.01% with AD843

APPLICATIONS
Battery-Powered Instrumentation
Laptop Computers
Upgrades for All 754x Series DACs (5 V Designs)

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The AD7943, AD7945 and AD7948 are fast 12-bit multiplying DACs that operate from a single +5 V supply (Normal Mode) and a single +3.3 V to +5 V supply (Biased Mode). The AD7943 has a serial interface, the AD7945 has a 12-bit parallel interface, and the AD7948 has an 8-bit byte interface. They will replace the industry-standard AD7543, AD7545 and AD7548 in many applications, and they offer superior speed and power consumption performance.

The AD7943 is available in 16-pin DIP, 16-pin SOP (Small Outline Package) and 20-pin SSOP (Shrink Small Outline Package).

The AD7945 is available in 20-pin DIP, 20-pin SOP and 20-pin SSOP.

The AD7948 is available in 20-pin DIP, 20-pin SOP and 20-pin SSOP.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7943/AD7945/AD7948 SPECIFICATIONS[1]

ACCURACY				
Resolution	12	12	Bits	1 LSB = $V_{REF}/2^{12}$ = 2.44 mV when V_{REF} = 10 V
Relative Accuracy	±0.5	±0.5	LSB max	
Differential Nonlinearity	±0.5	±0.5	LSB max	All Grades Guaranteed Monotonic over Temperature
Gain Error				
T_{MIN} to T_{MAX}	±2	±2	LSB max	
Gain Temperature Coefficient[4]	2	2	ppm FSR/°C typ	
	5	5	ppm FSR/°C max	
Output Leakage Current				
I_{OUT1}				
@ +25°C	10	10	nA max	See Terminology Section
T_{MIN} to T_{MAX}	100	100	nA max	Typically 20 nA over Temperature
REFERENCE INPUT				
Input Resistance	6	6	kΩ min	Typical Input Resistance = 9 kΩ
	12	12	kΩ max	
DIGITAL INPUTS				
V_{INH}, Input High Voltage	2.4	2.4	V min	
V_{INL}, Input Low Voltage	0.8	0.8	V max	
I_{INH}, Input Current	±1	±1	μA max	
C_{IN}, Input Capacitance[4]	10	10	pF max	
DIGITAL OUTPUT (AD7943 SRO)				For 1 CMOS Load
Output Low Voltage (V_{OL})	0.2	0.2	V max	
Output High Voltage (V_{OH})	V_{DD} – 0.2	V_{DD} – 0.2	V min	
POWER REQUIREMENTS				
V_{DD} Range	4.5/5.5	4.5/5.5	V min/V max	
Power Supply Sensitivity[4]				
$\Delta Gain/\Delta V_{DD}$	–75	–75	dB typ	
I_{DD} (AD7943)	5	5	μA max	$V_{INH} = V_{DD} - 0.1$ V min, V_{INL} = 0.1 V max. SRO Open Circuit. No STB Signal. Typically 1 μA. Typically 100 μA with a 1 MHz STB Frequency. At Input Levels of 0.8 V and 2.4 V, I_{DD} Is Typically 2.5 mA.
I_{DD} (AD7945, AD7948)	5	5	μA max	$V_{INH} = V_{DD} - 0.1$ V min, V_{INL} = 0.1 V max. Typically 1 μA. At Input Levels of 0.8 V and 2.4 V, I_{DD} Is Typically 2.5 mA.

NOTES

[1]The AD7943, AD7945 and AD7948 are specified in the normal current mode configuration and in the biased current mode for single-supply applications. Figures 15 and 16 are examples of normal mode operation.

[2]Temperature ranges as follows: B Grades: –40°C to +85°C; T Grade: –55°C to +125°C.

[3]The T Grade applies to the AD7945 only.

[4]Guaranteed by design.

Specifications subject to change without notice.

SPECIFICATIONS[1]

BIASED MODE

(AD7943: V_{DD} = +3 V to +5.5 V; V_{IOUT1} = V_{IOUT2} = AGND = 1.23 V; V_{REF} = +0 V to 2.45 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. AD7945, AD7948: V_{DD} = +3 V to +5.5 V; V_{IOUT1} = AGND = 1.23 V; V_{REF} = +0 V to 2.45 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Grades[2]	Units	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	1 LSB = $(V_{IOUT1} - V_{REF})/2^{12}$ = 300 µV When V_{IOUT1} = 1.23 V and V_{REF} = 0 V
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±0.9	LSB max	All Grades Guaranteed Monotonic over Temperature
Gain Error @ +25°C	±3	LSB max	
T_{MIN} to T_{MAX}	±4	LSB max	
Gain Temperature Coefficient[3]	2	ppm FSR/°C typ	
	5	ppm FSR/°C max	
Output Leakage Current			See Terminology Section
I_{OUT1}			
@ +25°C	10	nA max	
T_{MIN} to T_{MAX}	100	nA max	Typically 20 nA over Temperature
Input Resistance			This Varies with DAC Input Code
@ I_{OUT2} Pin (AD7943)	6	kΩ min	
@ AGND Pin (AD7945, AD7948)	6	kΩ min	
DIGITAL INPUTS			
V_{INH}, Input High Voltage @ V_{DD} = +5 V	2.4	V min	
V_{INH}, Input High Voltage @ V_{DD} = +3.3 V	2.1	V min	
V_{INL}, Input Low Voltage @ V_{DD} = +5 V	0.8	V max	
V_{INL}, Input Low Voltage @ V_{DD} = +3.3 V	0.6	V max	
I_{INH}, Input Current	±1	µA max	
C_{IN}, Input Capacitance[3]	10	pF max	
DIGITAL OUTPUT (SRO)			For 1 CMOS Load
Output Low Voltage (V_{OL})	0.2	V max	
Output High Voltage (V_{OH})	V_{DD} – 0.2	V min	
POWER REQUIREMENTS			
V_{DD} Range	3.0/5.5	V min/V max	
Power Supply Sensitivity[3]			
$\Delta Gain/\Delta V_{DD}$	–75	dB typ	
I_{DD} (AD7943)	5	µA max	V_{INH} = V_{DD} – 0.1 V min, V_{INL} = 0.1 V max. SRO Open Circuit; No STB Signal; Typically 1 µA. Typically 100 µA with 1 MHz STB Frequency.
I_{DD} (AD7945, AD7948)	5	µA max	V_{INH} = V_{DD} – 0.1 V min, V_{INL} = 0.1 V max. Typically 1 µA.

NOTES

[1]These specifications apply with the devices biased up at 1.23 V for single supply applications. The model numbering reflects this by means of a "–B" suffix (for example: AD7943AN-B). Figure 17 is an example of Biased Mode Operation.

[2]Temperature ranges as follows: A Versions: –40°C to +85°C.

[3]Guaranteed by design.

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

Normal Mode (AD7943: V_{DD} = +4.5 V to +5.5 V; V_{IOUT1} = V_{IOUT2} = AGND = 0 V. AD7945, AD7948: V_{DD} = +4.5 V to +5.5 V; V_{IOUT1} = AGND = 0 V. V_{REF} = 6 V rms, 1 kHz sine wave; T_A = T_{MIN} to T_{MAX}; DAC output op amp is AD843; unless otherwise noted.) These characteristics are included for Design Guidance and are not subject to test.

Parameter	B Grades	T Grade	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Output Voltage Settling Time	600	700	ns typ	To 0.01% of Full-Scale Range. V_{REF} = +10 V; DAC Latch Alternately Loaded with All 0s and All 1s
Digital to Analog Glitch Impulse	60	60	nV-s typ	Measured with V_{REF} = 0 V. DAC Latch Alternately Loaded with All 0s and All 1s
Multiplying Feedthrough Error	–75	–75	dB max	DAC Latch Loaded with All 0s
Output Capacitance	60	60	pF max	All 1s Loaded to DAC
	30	30	pF max	All 0s Loaded to DAC
Digital Feedthrough (AD7943)	5	5	nV-s typ	Feedthrough to the DAC Output with $\overline{LD1}$, $\overline{LD2}$ High and Alternate Loading of All 0s and All 1s into the Input Shift Register
Digital Feedthrough (AD7945, AD7948)	5	5	nV-s typ	Feedthrough to the DAC Output with $\overline{CS}$ High and Alternate Loading of All 0s and All 1s to the DAC Bus
Total Harmonic Distortion	–83	–83	dB typ	
Output Noise Spectral Density @ 1 kHz	35	35	nV/$\sqrt{Hz}$ typ	All 1s Loaded to DAC. V_{REF} = 0 V. Output Op Amp Is OP07

AC PERFORMANCE CHARACTERISTICS

Biased Mode (AD7943: V_{DD} = +3 V to +5.5 V; V_{IOUT1} = V_{IOUT2} = AGND = 1.23 V. AD7945, AD7948: V_{DD} = +3 V to +5.5 V; V_{IOUT1} = AGND = 1.23 V. V_{REF} = 1 kHz, 2.45 V p-p, sine wave biased at 1.23 V; DAC output op amp is AD820; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.) These characteristics are included for Design Guidance and are not subject to test.

Parameter	A Grades	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	5	µs typ	To 0.01% of Full-Scale Range. V_{REF} = 0 V DAC Latch Alternately Loaded with All 0s and All 1s
Digital to Analog Glitch Impulse	60	nV-s typ	V_{REF} = 1.23 V. DAC Register Alternately Loaded with All 0s and All 1s
Multiplying Feedthrough Error	–75	dB max	DAC Latch Loaded with All 0s
Output Capacitance	60	pF max	All 1s Loaded to DAC
	30	pF max	All 0s Loaded to DAC
Digital Feedthrough	5	nV-s typ	Feedthrough to the DAC Output with $\overline{LD1}$, $\overline{LD2}$ High and Alternate Loading of All 0s and All 1s into the Input Shift Register
Digital Feedthrough (AD7945, AD7948)	5	nV-s typ	Feedthrough to the DAC Output with $\overline{CS}$ High and Alternate Loading of All 0s and All 1s to the DAC Bus
Total Harmonic Distortion	–83	dB typ	
Output Noise Spectral Density @ 1 kHz	25	nV/$\sqrt{Hz}$ typ	All 1s Loaded to DAC. V_{REF} = 1.23 V

AD7943 TIMING SPECIFICATIONS[1] ($T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Limit @ V_{DD} = +3 V to +3.6 V	Limit @ V_{DD} = +4.5 V to +5.5 V	Units	Description
t_{STB}[2]	60	40	ns min	STB Pulse Width
t_{DS}	15	10	ns min	Data Setup Time
t_{DH}	35	25	ns min	Data Hold Time
t_{SRI}	55	35	ns min	SRI Data Pulse Width
t_{LD}	55	35	ns min	Load Pulse Width
t_{CLR}	55	35	ns min	CLR Pulse Width
t_{ASB}	0	0	ns min	Min Time Between Strobing Input Shift Register and Loading DAC Register
t_{SV}[3]	60	35	ns max	STB Clocking Edge to SRO Data Valid Delay

NOTES
[1]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V. tr and tf should not exceed 1 µs on any digital input.
[2]STB mark/space ratio range is 60/40 to 40/60.
[3]t_{SV} is measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V.

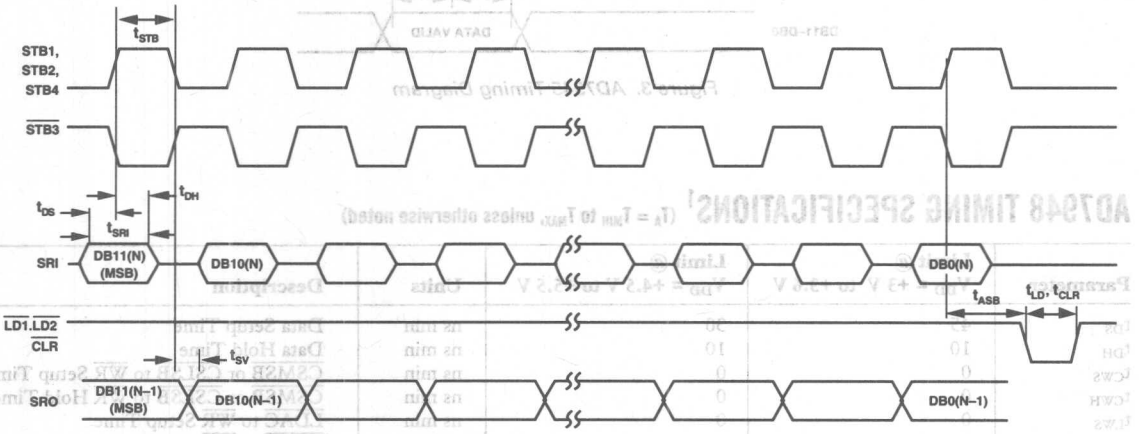


Figure 1. AD7943 Timing Diagram

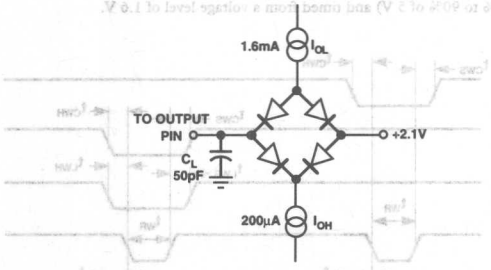


Figure 2. Load Circuit for Digital Output Timing Specifications

Parameter	Limit @ V_{DD} = +3 V to +3.6 V	Limit @ V_{DD} = +4.5 V to +5.5 V	Units	Description
t_{DS}	35	20	ns min	Data Setup Time
t_{DH}	10	10	ns min	Data Hold Time
t_{CS}	60	40	ns min	Chip Select Setup Time
t_{CH}	0	0	ns min	Chip Select Hold Time
t_{WR}	60	40	ns min	Write Pulse Width

NOTE
[1]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

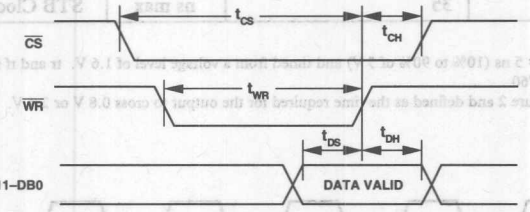


Figure 3. AD7945 Timing Diagram

AD7948 TIMING SPECIFICATIONS[1] ($T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Limit @ V_{DD} = +3 V to +3.6 V	Limit @ V_{DD} = +4.5 V to +5.5 V	Units	Description
t_{DS}	45	30	ns min	Data Setup Time
t_{DH}	10	10	ns min	Data Hold Time
t_{CWS}	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_{CWH}	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_{LWS}	0	0	ns min	$\overline{LDAC}$ to $\overline{WR}$ Setup Time
t_{LWH}	0	0	ns min	$\overline{LDAC}$ to $\overline{WR}$ Hold Time
t_{WR}	60	40	ns min	Write Pulse Width

NOTE
[1]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

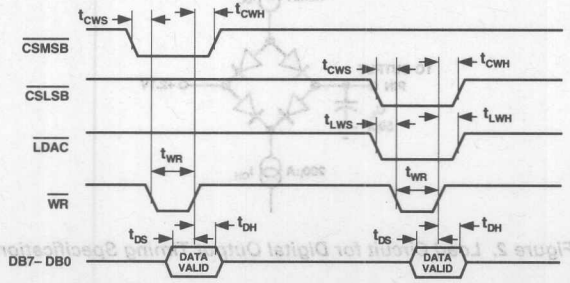


Figure 4. AD7948 Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND ..... –0.3 V to +6 V
I_{OUT1} to DGND ..... –0.3 V to V_{DD} + 0.3 V
I_{OUT2} to DGND ..... –0.3 V to V_{DD} + 0.3 V
AGND to DGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
V_{RFB}, V_{REF} to DGND ..... ±15 V
Input Current to Any Pin Except Supplies[2] ..... ±10 mA
Operating Temperature Range
  Industrial (A, B Versions) ..... –40°C to +85°C
  Extended (T Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
DIP Package, Power Dissipation ..... 670 mW
  θ_{JA} Thermal Impedance ..... 116°C/W
  Lead Temperature, Soldering, (10 sec) ..... +260°C
SOP Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C
SSOP Package, Power Dissipation ..... 875 mW
  θ_{JA} Thermal Impedance ..... 132°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSBs)	Nominal Supply Voltage	Package Option*
AD7943BN	–40°C to +85°C	±0.5	+5 V	N-16
AD7943BR	–40°C to +85°C	±0.5	+5 V	R-16
AD7943BRS	–40°C to +85°C	±0.5	+5 V	RS-20
AD7943AN-B	–40°C to +85°C	±1	+3.3 V to +5 V	N-16
AD7943ARS-B	–40°C to +85°C	±1	+3.3 V to +5 V	RS-20
AD7945BN	–40°C to +85°C	±0.5	+5 V	N-20
AD7945BR	–40°C to +85°C	±0.5	+5 V	R-20
AD7945BRS	–40°C to +85°C	±0.5	+5 V	RS-20
AD7945AN-B	–40°C to +85°C	±1	+3.3 V to +5 V	N-20
AD7945ARS-B	–40°C to +85°C	±1	+3.3 V to +5 V	RS-20
AD7945TQ	–55°C to +125°C	±1	+5 V	Q-20
AD7948BN	–40°C to +85°C	±0.5	+5 V	N-20
AD7948BR	–40°C to +85°C	±0.5	+5 V	R-20
AD7948BRS	–40°C to +85°C	±0.5	+5 V	RS-20
AD7948AN-B	–40°C to +85°C	±1	+3.3 V to +5 V	N-20
AD7948ARS-B	–40°C to +85°C	±1	+3.3 V to +5 V	RS-20

*N = Plastic DIP; R = SOP (Small Outline Package); RS = SSOP (Shrink Small Outline Package); Q = Cerdip. For outline information see Package Information section.

TERMINOLOGY

Relative Accuracy
Relative Accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Gain Error
Gain Error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustable to zero with an external potentiometer.

Output Leakage Current
Output leakage current is current which flows in the DAC ladder switches when these are turned off. For the I_{OUT1} terminal, it can be measured by loading all 0s to the DAC and measuring the I_{OUT1} current. Minimum current will flow in the I_{OUT2} line when the DAC is loaded with all 1s.

Output Capacitance
This is the capacitance from the I_{OUT1} pin to AGND.

Output Voltage Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For these devices, it is specified both with the AD843 as the output op amp in the normal current mode and with the AD820 in the biased current mode.

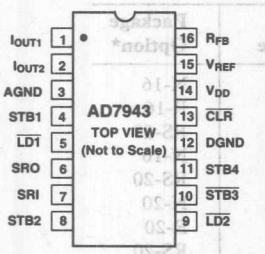
Digital to Analog Glitch Impulse
This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV-s. It is measured with the reference input connected to AGND and the digital inputs toggled between all 1s and all 0s. As with Settling Time, it is specified with both the AD817 and the AD820.

AC Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC I_{OUT1} terminal, when all 0s are loaded in the DAC.

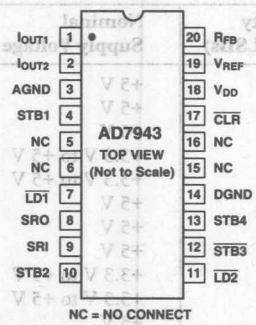
Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up as noise on the I_{OUT1} pin and subsequently on the op amp output. This noise is digital feedthrough.

PIN CONFIGURATIONS

DIP/SOP

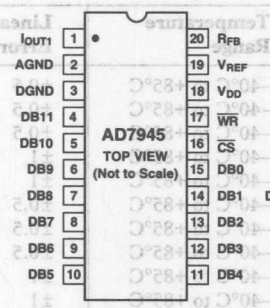


SSOP

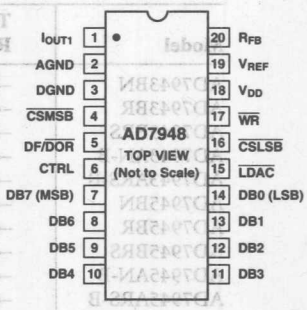


NC = NO CONNECT

DIP/SOP/SSOP



DIP/SOP/SSOP



AD7943 PIN DESCRIPTION

Pin Mnemonic	Description
I_{OUT1}	DAC current output terminal 1.
I_{OUT2}	DAC current output terminal 2. This should be connected to the AGND pin.
AGND	This pin connects to the back gates of the current steering switches. In normal operation, it should be connected to the signal ground of the system. In biased single-supply operation it may be biased to some voltage between 0 V and the 1.23 V. See Figure 11 for more details.
STB 1	This is the Strobe 1 input. Data is clocked into the input shift register on the rising edge of this signal. $\overline{\text{STB 3}}$ must be high. STB 2, STB 4 must be low.
$\overline{\text{LD1}}$, $\overline{\text{LD2}}$	Active low inputs. When both of these are low, the DAC register is updated and the output will change to reflect this.
SRI	Serial Data Input. Data on this line will be clocked into the input shift register on one of the Strobe inputs, when they are enabled.
STB 2	This is the Strobe 2 input. Data is clocked into the input shift register on the rising edge of this signal. $\overline{\text{STB 3}}$ must be high. STB 1, STB 4 must be low.
$\overline{\text{STB 3}}$	This is the Strobe 3 input. Data is clocked into the input shift register on the falling edge of this signal. STB 1, STB 2, STB 4, must be low.
STB 4	This is the Strobe 4 input. Data is clocked into the input shift register on the rising edge of this signal. $\overline{\text{STB 3}}$ must be high. STB 1, STB 2 must be low.
DGND	Digital Ground.
$\overline{\text{CLR}}$	Asynchronous CLR input. When this input is taken low, all 0s are loaded to the DAC latch.
V_{DD}	Power supply input. This is nominally +5 V for Normal Mode Operation and +3.3 V to +5 V for Biased Mode Operation.
V_{REF}	DAC reference input.
R_{FB}	DAC feedback resistor pin.

AD7945 PIN DESCRIPTION

Pin Mnemonic	Description
I_{OUT1}	DAC current output terminal 1.
AGND	This pin connects to the back gates of the current steering switches. The DAC I_{OUT2} terminal is also connected internally to this point.
DGND	Digital Ground.
DB11–DB0	Digital Data Inputs.
$\overline{\text{CS}}$	Active Low, Chip Select Input.
$\overline{\text{WR}}$	Active Low, Write Input.
V_{DD}	Power supply input. This is nominally +5 V for Normal Mode Operation and +3.3 V to +5 V for Biased Mode Operation.
V_{REF}	DAC reference input.
R_{FB}	DAC feedback resistor pin.

I_{OUT1}	DAC current output terminal 1. Normally terminated at the virtual ground of output amplifier.
AGND	Analog Ground Pin. This pin connects to the back gates of the current steering switches. The DAC I_{OUT2} terminal is also connected internally to this point.
DGND	Digital Ground Pin.
$\overline{CSMSB}$	Chip Select Most Significant Byte. Active Low Input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{LDAC}$ and $\overline{WR}$ to load external data into both input and DAC registers.
DF/$\overline{DOR}$	Data Format/Data Override. When this input is low, data in the DAC register is forced to one of two override codes selected by CTRL. When the override signal is removed, the DAC output returns to reflect the value in the DAC register. With DF/$\overline{DOR}$ high, CTRL selects either a left or right justified input data format. For normal operation, DF/$\overline{DOR}$ is held high. See Table I.

Table I. Truth Table for DF/$\overline{DOR}$ CTRL

DF/$\overline{DOR}$	CTRL	Function
0	0	DAC Register Contents Overridden by All 0s
0	1	DAC Register Contents Overridden by All 1s
1	0	Left-Justified Input Data Selected
1	1	Right-Justified Input Data Selected

CTRL	Control Input. See DF/$\overline{DOR}$ description.
DB7–DB0	Digital Data Inputs.
$\overline{LDAC}$	Load DAC input, active low. This signal, in combination with others, is used to load the DAC register from either the input register or the external data bus.
$\overline{CSLSB}$	Chip Select Least Significant (LS) Byte. Active Low Input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers.

Table II. Truth Table for AD7948 Write Operation

$\overline{WR}$	$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	Function
0	1	0	1	Load LS Byte to Input Register
0	1	0	0	Load LS Byte to Input Register and DAC Register
0	0	1	1	Load MS Byte to Input Register
0	0	1	0	Load MS Byte to Input Register and DAC Register
0	1	1	0	Load Input Register to DAC Register
1	X	X	X	No Data Transfer

$\overline{WR}$	Write input, active low. This active low signal, in combination with others is used in loading external data into the AD7948 input register and in transferring data from the input register to the DAC register.
V_{DD}	Power supply input. This is nominally +5 V for Normal Mode Operation and +3.3 V to +5 V for Biased Mode Operation.
V_{REF}	DAC reference input.
R_{FB}	DAC feedback resistor pin.

Typical Performance Curves

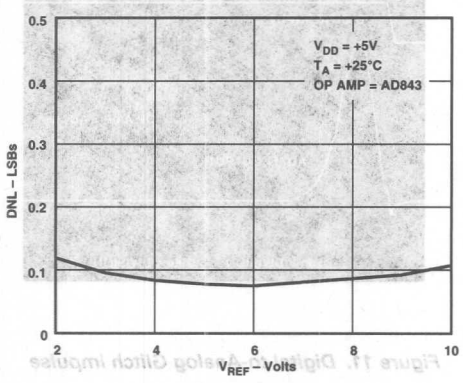


Figure 5. Differential Nonlinearity Error vs. V_{REF} (Normal Mode)

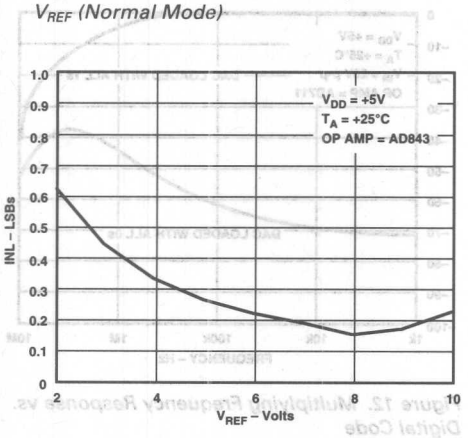


Figure 6. Integral Nonlinearity Error vs. V_{REF} (Normal Mode)

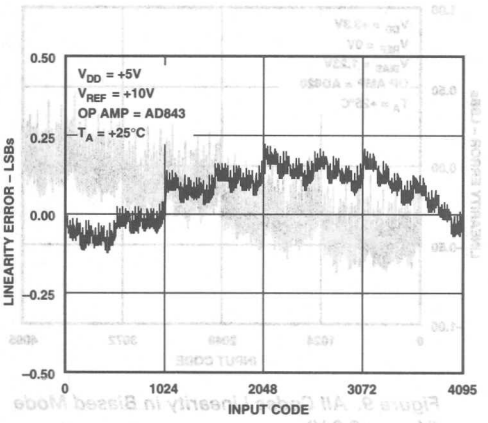


Figure 7. All Codes Linearity In Normal Mode (V_{DD} = +5 V)

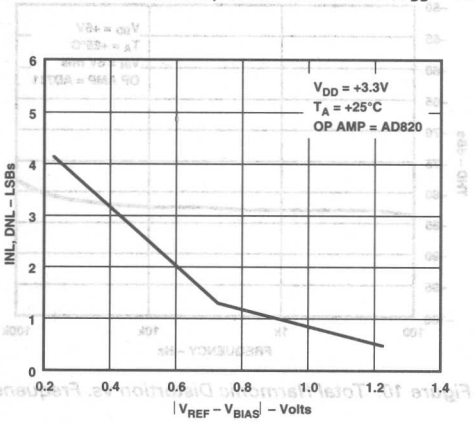


Figure 8. Linearity Error vs. V_{REF} (Biased Mode)

3

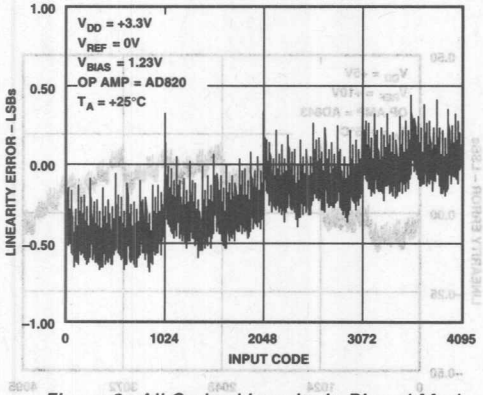


Figure 9. All Codes Linearity in Biased Mode (V_{DD} = +3.3 V)

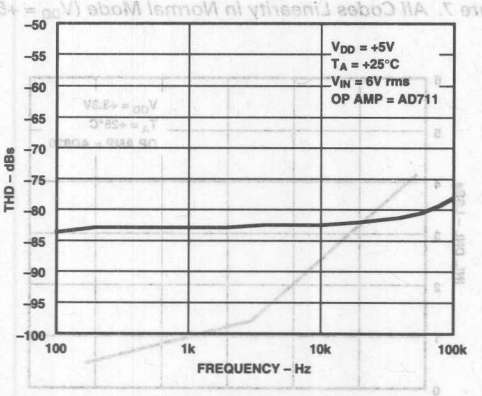


Figure 10. Total Harmonic Distortion vs. Frequency

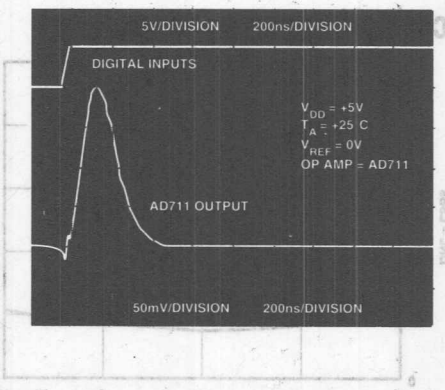


Figure 11. Digital-to-Analog Glitch Impulse

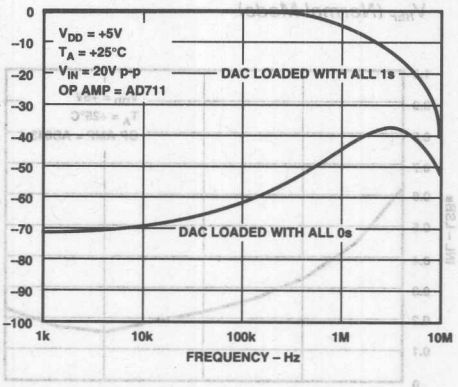


Figure 12. Multiplying Frequency Response vs. Digital Code

GENERAL DESCRIPTION

D/A Section

The AD7943, AD7945 and AD7948 are 12-bit current-output D/A converters. A simplified circuit diagram is shown in Figure 13. The DAC architecture is segmented. This means that the 2 MSBs of the 12-bit data word are decoded to drive the three switches A, B and C. The remaining 10 bits of the data word drive the switches S0 to S9 in a standard inverting R-2R ladder configuration.

Each of the switches A to C steers 1/4 of the total reference current into either I_{OUT1} or I_{OUT2} with the remaining 1/4 of the total current passing through the R-2R section. Switches S9 to S0 steer binarily weighted currents into either I_{OUT1} or I_{OUT2}. If I_{OUT1} and I_{OUT2} are kept at the same potential, a constant current flows in each ladder leg, regardless of digital input code. Thus, the input resistance seen at V_{REF} is always constant. It is equal to R/2. The V_{REF} input may be driven by any reference voltage or current, ac or dc that is within the Absolute Maximum Ratings.

The device provides access to the V_{REF}, R_{FB}, and I_{OUT1} terminals of the DAC. This makes the device extremely versatile and allows it to be configured in several different operating modes. Examples of these are shown in the following sections. The AD7943 also has a separate I_{OUT2} pin. In the AD7945 and AD7948 this is internally tied to AGND.

When an output amplifier is connected in the standard configuration of Figure 14, the output voltage is given by:

$$V_{OUT} = -D \times V_{REF}$$

where D is the fractional representation of the digital word loaded to the DAC. D can be set from 0 to 4095/4096, since it has 12-bit resolution.

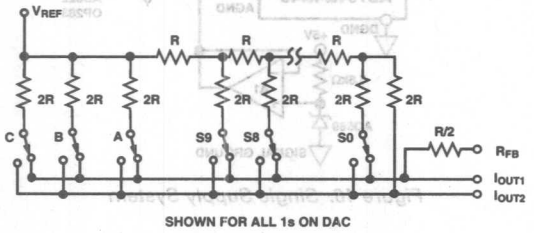
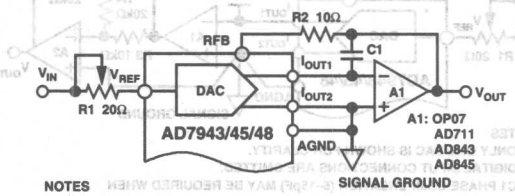


Figure 13. Simplified D/A Circuit Diagram

UNIPOLAR BINARY OPERATION (Two-Quadrant Multiplication)

Figure 14 shows the standard unipolar binary connection diagram for the AD7943, AD7945 and AD7948. When V_{IN} is an ac signal, the circuit performs two-quadrant multiplication. Resistors R1 and R2 allow the user to adjust the DAC gain error. With a specified gain error of 2 LSBs over temperature, these are not necessary in many applications. Circuit offset is due completely to the output amplifier offset. It can be removed by adjusting the amplifier offset voltage. Alternatively, choosing a low offset amplifier makes this unnecessary.

A1 should be chosen to suit the application. For example, the OP07 is ideal for very low bandwidth applications (10 kHz or



NOTES
1. ONLY ONE DAC IS SHOWN FOR CLARITY.
2. DIGITAL INPUT CONNECTIONS ARE OMITTED.
3. C1 PHASE COMPENSATION (5–15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

Figure 14. Unipolar Binary Operation

lower) while the AD711 is suitable for medium bandwidth applications (200 kHz or lower). For high bandwidth applications of greater than 200 kHz, the AD843 and AD847 offer very fast settling times.

The code table for Figure 14 is shown in Table III.

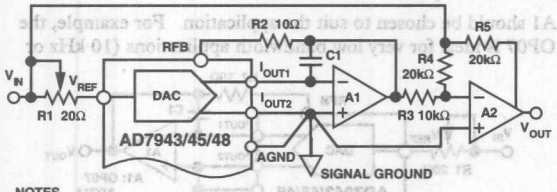
Table III. Unipolar Binary Code

Digital Input MSB LSB	Analog Output (V_{OUT} as Shown in Figure 15)
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0001	$-V_{REF}$ (2049/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096)
0111 1111 1111	$-V_{REF}$ (2047/4096)
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	$-V_{REF}$ (0/4096) = 0

NOTE
Nominal LSB size for the circuit of Figure 14 is given by: V_{REF} (1/4096).

BIPOLAR OPERATION (Four-Quadrant Multiplication)

Figure 15 shows the standard connection diagram for bipolar operation of the AD7943, AD7945 and AD7948. The coding is offset binary as shown in Table IV. When V_{IN} is an ac signal, the circuit performs four-quadrant multiplication. Resistors R1 and R2 are for gain error adjustment and are not needed in many applications where the device gain error specifications are adequate. To maintain the gain error specifications, resistors R3, R4 and R5 should be ratio matched to 0.01%.



NOTES
1. ONLY ONE DAC IS SHOWN FOR CLARITY.
2. DIGITAL INPUT CONNECTIONS ARE OMITTED.
3. C1 PHASE COMPENSATION (5–15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER, A1.

Figure 15. Bipolar Operation (Four-Quadrant Multiplication)

Suitable dual amplifiers for use with Figure 15 are the OP270 (low noise, low bandwidth, 15 kHz), the AD712 (medium bandwidth, 200 kHz) or the AD827 (wide bandwidth, 1 MHz).

Table IV. Bipolar (Offset Binary) Code

Table Digital Input MSB LSB	Analog Output (V_{OUT} as Shown in Figure 16)
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
1000 0000 0000	$+V_{REF}$ (0/2048) = 0
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0001	$-V_{REF}$ (2047/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048) = $-V_{REF}$

NOTE
Nominal LSB size for the circuit of Figure 15 is given by: V_{REF} (1/2048).

SINGLE SUPPLY APPLICATIONS

The "-B" versions of the devices are specified and tested for single supply applications. Figure 16 shows the recommended circuit for operation with a single +5 V to +3.3 V supply. The I_{OUT2} and AGND terminals are biased to 1.23 V. Thus, with 0 V applied to the V_{REF} terminal, the output will go from 1.23 V (all 0s loaded to the DAC) to 2.46 V (all 1s loaded). With 2.45 V applied to the V_{REF} terminal, the output will go from 1.23 V (all 0s loaded) to 0.01 V (all 1s loaded). It is important when considering INL in a single-supply system to realize that most single-supply amplifiers cannot sink current and maintain zero volts at the output. In Figure 16, with V_{REF} = 2.45 V the required sink current is 200 μA. The minimum output voltage level is 10 mV. Op amps like the OP295 are capable of maintaining this level while sinking 200 μA.

Figure 16 shows the I_{OUT2} and AGND terminals being driven by an amplifier. This is to maintain the bias voltage at 1.23 V as the impedance seen looking into the I_{OUT2} terminal changes. This impedance is code dependent and varies from infinity (all 0s loaded in the DAC) to about 6 kΩ minimum. The AD589 has a typical output resistance of 0.6 Ω and it can be used to drive the terminals directly. However, this will cause a typical linearity degradation of 0.2 LSBs. If this is unacceptable then the buffer amplifier is necessary. Figure 9 shows the typical linearity performance of the AD7943/AD7945/AD7948 when used as in Figure 16 with V_{DD} set at +3.3 V and V_{REF} = 0 V.

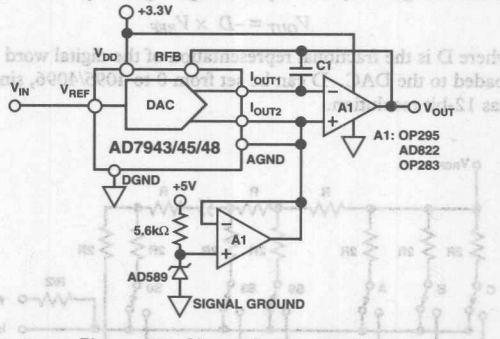


Figure 16. Single Supply System

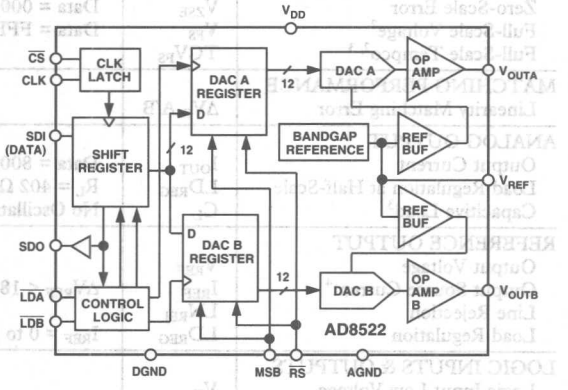
+5 Volt, Serial Input, Dual 12-Bit DAC

AD8522

FEATURES
Complete Dual 12-Bit DAC
No External Components
+5 V Single-Supply Operation ±10%
4.095 V Full Scale (1 mV/LSB)
Buffered Voltage Outputs
Low Power: 5 mW/DAC
Space Saving 1.5 mm Height SO-14 Package

APPLICATIONS
Digitally Controlled Calibration
Servo Controls
Process Control Equipment
Computer Peripherals
Portable Instrumentation
Cellular Base Stations Voltage Adjustment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8522 is a complete dual 12-bit, single-supply, voltage output DAC in a 14-pin DIP, or SO-14 surface mount package. Fabricated in a CBCMOS process, features include a serial digital interface, onboard reference, and buffered voltage output. Ideal for +5 V-only systems, this monolithic device offers low cost and ease of use, and requires no external components to realize the full performance of the device.

The serial digital interface allows interfacing directly to numerous microcontroller ports, with a simple high speed, three-wire data, clock, and load strobe format. The 16-bit serial word contains the 12-bit data word and DAC select address, which is decoded internally or can be decoded externally using $\overline{LDA}$, $\overline{LDB}$ inputs. A serial data output allows the user to easily daisy-chain multiple devices in conjunction with a chip select input. A reset $\overline{RS}$ input sets the outputs to zero scale or midscale, as determined by the input MSB.

The output 4.095 V full scale is laser trimmed to maintain accuracy over the operating temperature range of the device, and gives the user an easy-to-use one-millivolt-per-bit resolution. A 2.5 V reference output is also available externally for other data acquisition circuitry, and for ratiometric applications. The output buffers are capable of driving ±5 mA.

The AD8522 is available in the 14-pin plastic DIP and low profile 1.5 mm SOIC-14 packages.

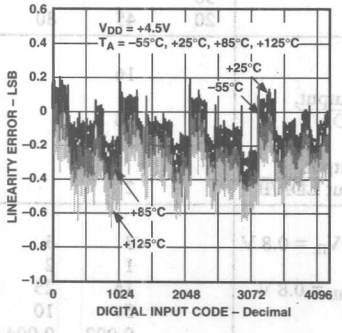
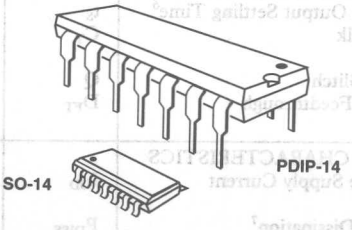


Figure 1. Linearity Error vs. Digital Code & Temperature

PACKAGE TYPES AVAILABLE



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

STATIC PERFORMANCE						
Resolution[1]	N		12			Bits
Relative Accuracy	INL		-1.5	±0.5	+1.5	LSB
Differential Nonlinearity	DNL	Monotonic	-1	±0.5	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+0.5	+3	mV
Full-Scale Voltage[2]	V_{FS}	Data = FFF_H	4.079	4.095	4.111	Volts
Full-Scale Tempco[2, 3]	TCV_{FS}			±15		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching Error	$\Delta V_{FS}A/B$			±1		LSB
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = 800_H, $\Delta V_{OUT} \leq 3$ LSB			±5	mA
Load Regulation at Half-Scale	LD_{REG}	R_L = 402 Ω to ∞, Data = 800_H		1	3	LSB
Capacitive Load[3]	C_L	No Oscillation		500		pF
REFERENCE OUTPUT						
Output Voltage	V_{REF}		2.484	2.500	2.516	V
Output Source Current[4]	I_{REF}	$\Delta V_{REF} < 18$ mV			5	mA
Line Rejection	LN_{REJ}			0.025	0.08	%/V
Load Regulation	LD_{REG}	I_{REF} = 0 to 5 mA, Data = 800_H		0.025	0.1	%/mA
LOGIC INPUTS & OUTPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance[3]	C_{IL}				10	pF
Logic Output Voltage Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Logic Output Voltage High	V_{OH}	I_{OH} = 400 µA	3.5			V
TIMING SPECIFICATIONS[3, 5]						
Clock Width High	t_{CH}		35			ns
Clock Width Low	t_{CL}		35			ns
Load Pulse Width	t_{LDW}		25			ns
Data Setup	t_{DS}		10			ns
Data Hold	t_{DH}		20			ns
Clear Pulse Width	t_{CLRW}		20			ns
Load Setup	t_{LD1}		10			ns
Load Hold	t_{LD2}		10			ns
Select	t_{CSS}		30			ns
Deselect	t_{CSH}		30			ns
Clock to SDO Propagation Delay	t_{PD}		20	45	80	ns
AC CHARACTERISTICS[3, 5]						
Voltage Output Settling Time[6]	t_S	To ±1 LSB of Final Value		16		µs
Crosstalk	C_T	Signal Measured at DAC Output, While Changing Opposite $\overline{LDA}/B$		38		dB
DAC Glitch	Q	Half-Scale Transition		13		nV s
Digital Feedthrough	D_{FT}	Signal Measured at DAC Output, While Changing Data Without $\overline{LDA}/B$		2		nV s
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{DD} = 5.5 V, V_{IH} = 2.4 V or V_{IL} = 0.8 V		3	5	mA
		V_{DD} = 5 V, V_{IL} = 0 V		1	2	mA
Power Dissipation[7]	P_{DISS}	V_{DD} = 5 V, V_{IH} = 2.4 V or V_{IL} = 0.8 V		15	25	mW
		V_{DD} = 5 V, V_{IL} = 0 V		5	10	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTES
[1]1 LSB = 1 mV for 0 V to +4.095 V output range.
[2]Includes internal voltage reference error.
[3]These parameters are guaranteed by design and not subject to production testing.
[4]Very little sink current is available at the V_{REF} pin. Use external buffer if setting up a virtual ground.
[5]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[6]The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.
[7]Power Dissipation is calculated $I_{DD} \times 5$ V.
Specifications subject to change without notice.

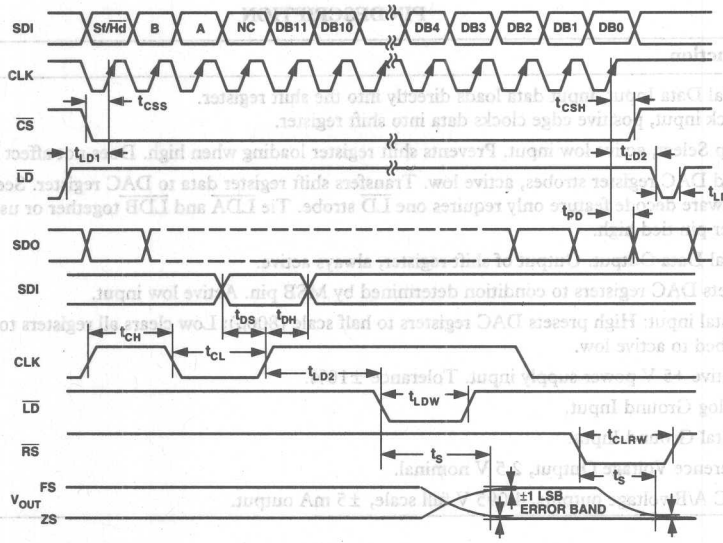


Figure 2. Timing Diagram

SERIAL INPUT REGISTER DATA FORMAT

Last															First
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	NC	A	B	Sf/Hd

Table I. Truth Table

Data Word			Ext Pins		
Sf/$\overline{Hd}$	B	A	$\overline{LDA}$	$\overline{LDB}$	DAC Register
Hardware Load:					
L	X	X	↓	↓	Loads DACA + DACB with Data from SR
L	X	X	↓	H	Loads DACA with Data from SR
L	X	X	H	↓	Loads DACB with Data from SR
L	X	X	H	H	No Load
Software Decode Load:					
H	L	L	X	X	No Load
H	H	L	↓	↓	Loads DACB with Data from SR, See Note 1 Below
H	H	L	H	H	No Load
H	L	H	↓	↓	Loads DACA with Data from SR, See Note 1 Below
H	L	H	H	H	No Load
H	H	H	↓	↓	Loads DACA + DACB with Data from SR, See 1 Note Below
H	H	H	H	H	No Load

NOTES
[1]In software mode $\overline{LDA}$ and $\overline{LDB}$ perform the same function. They can be tied together or the unused pin should be tied high.
[2]External Pins $\overline{LDA}$ and $\overline{LDB}$ should always be high when shifting Data into the shift register.
[3]↓ symbol denotes negative transition.

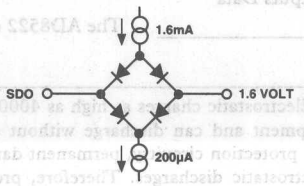


Figure 3. AC Timing SDO Pin Load Circuit

PIN DESCRIPTION

Pin	Function
SDI	Serial Data Input, input data loads directly into the shift register.
CLK	Clock input, positive edge clocks data into shift register.
$\overline{CS}$	Chip Select, active low input. Prevents shift register loading when high. Does not affect $\overline{LDA}$ and $\overline{LDB}$ operation.
$\overline{LDA}/\overline{B}$	Load DAC register strobes, active low. Transfers shift register data to DAC register. See truth table for operation. Software decode feature only requires one $\overline{LD}$ strobe. Tie $\overline{LDA}$ and $\overline{LDB}$ together or use one of them with the other pin tied high.
SDO	Serial Data Output. Output of shift register, always active.
$\overline{RS}$	Resets DAC registers to condition determined by MSB pin. Active low input.
MSB	Digital input: High presets DAC registers to half scale (800_H); Low clears all registers to zero (000_H), when $\overline{RS}$ is strobed to active low.
V_{DD}	Positive +5 V power supply input. Tolerance ±10%.
AGND	Analog Ground Input.
DGND	Digital Ground Input.
V_{REF}	Reference Voltage Output, 2.5 V nominal.
$V_{OUT\ A/B}$	DAC A/B voltage outputs, 4.095 V full scale, ±5 mA output.

PIN CONFIGURATION

14-Pin Plastic DIP **14-Lead SO-14**

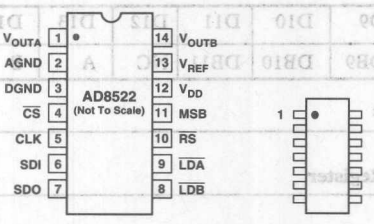


Table II. Truth Tables

DAC Register Preset		
$\overline{RS}$	MSB	Register Activity
0	0	Asynchronously Resets DAC Registers to Zero Scale
0	1	Asynchronously Presets DAC Registers to Half Scale (800_H)
1	X	None

Shift Register		
$\overline{CS}$	CLK	Shift Register
1	X	No Effect
0	↑	Shifts Register One Bit, SDO Outputs Data from 16 Clocks Earlier

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to DGND & AGND ..... –0.3 V, +7 V
Logic Inputs and Output to DGND ..... –0.3 V, V_{DD} + 0.3 V
V_{OUT} to AGND ..... –0.3 V, V_{DD} + 0.3 V
V_{REF} to AGND ..... –0.3 V, V_{DD} + 0.3 V
AGND to DGND ..... –0.3 V, V_{DD}
I_{OUT} Short Circuit to GND or V_{DD} ..... 50 mA
Package Power Dissipation ..... $(T_J\ max–T_A)/\theta_{JA}$
Thermal Resistance, θ_{JA}
14-Pin Plastic DIP Package (N-14) ..... 83°C/W
14-Lead SOIC Package (SO-14) ..... 120°C/W
Maximum Junction Temperature (T_J max) ..... 150°C
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD8522AN	–40°C to +85°C	14-Pin P-DIP	N-14
AD8522AR	–40°C to +85°C	14-Lead SOIC	SO-14
AD8522Chips	+25°C	Die	

*For outline information see Package Information section.

The AD8522 contains 1482 transistors.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8522 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

+5 Volt, Parallel Input Complete Dual 12-Bit DAC

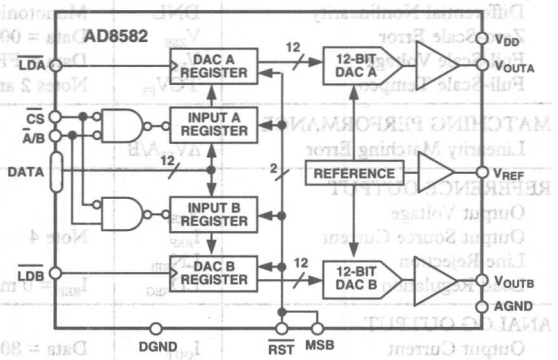
AD8582

3

FEATURES
- Complete Dual 12-Bit DAC
- No External Components
- Single +5 Volt Operation
- 1 mV/Bit with 4.095 V Full Scale
- True Voltage Output, ±5 mA Drive
- Very Low Power: 5 mW

APPLICATIONS
- Digitally Controlled Calibration
- Portable Equipment
- Servo Controls
- Process Control Equipment
- PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8582 is a complete, parallel input, dual 12-bit, voltage output DAC designed to operate from a single +5 volt supply. Built using a CBCMOS process, this monolithic DAC offers the user low cost, and ease-of-use in +5 volt only systems.

Included on the chip, in addition to the DACs, are a rail-to-rail amplifier, latch and reference. The reference (V_{REF}) is trimmed to 2.5 volts output, and the on-chip amplifier gains up the DAC output to 4.095 volts full scale. The user needs only supply a +5 volt supply.

The AD8582 is coded natural binary. The op amp output swings from 0 volt to +4.095 volts for a one-millivolt-per-bit resolution, and is capable of driving ±5 mA. Operation down to 4.3 V is possible with output load currents less than 1 mA.

The high speed parallel data interface connects to the fastest processors without wait states. The double-buffered input structure allows the user to load the input registers one at a time, then a single load strobe tied to both LDA + LDB inputs will update both DAC outputs simultaneously. LDA and LDB can also be activated independently to immediately update their respective DAC registers. An address input decodes DAC A or DAC B when the chip select $\overline{CS}$ input is strobed. An asynchronous reset input sets the output to zero scale. The MSB bit can be used to establish a preset to midscale when the reset input is strobed.

The AD8582 is available in the 24-pin plastic DIP and the surface mount SOIC-24. Each part is fully specified for operation over –40°C to +85°C, and the full +5 V ± 5% power supply range.

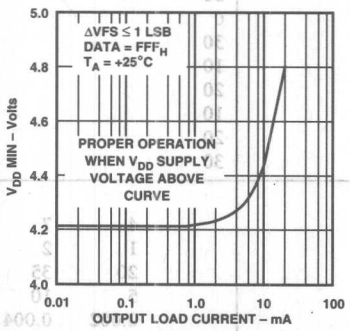


Figure 1. Minimum Supply Voltage vs. Load

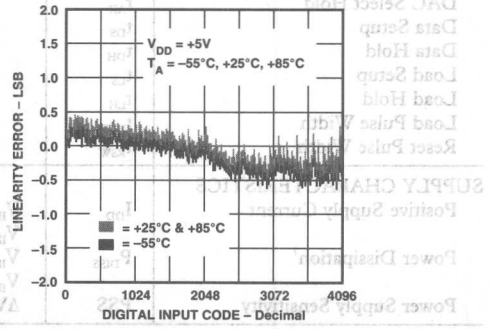


Figure 2. Linearity Error vs. Digital Code and Temperature

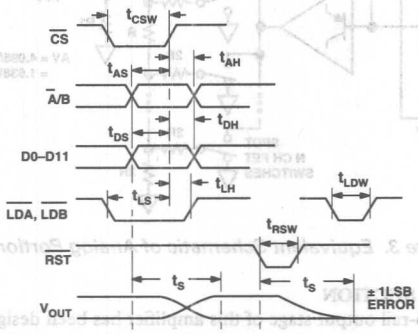
Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N	Note 1	12			Bits
Relative Accuracy	INL		–2	±3/4	+2	LSB
Differential Nonlinearity	DNL	Monotonic	–1	±3/4	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+0.2	+3	mV
Full-Scale Voltage	V_{FS}	Data = FFF_H,[2]	4.079	4.095	4.111	V
Full-Scale Tempco	TCV_{FS}	Notes 2 and 3		±16		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching Error	$\Delta V_{FS}A/B$			±1		LSB
REFERENCE OUTPUT						
Output Voltage	V_{REF}		2.484	2.500	2.516	V
Output Source Current	I_{REF}	Note 4			–5	mA
Line Rejection	LN_{REJ}				0.08	%/V
Load Regulation	LD_{REG}	I_{REF} = 0 mA to 5 mA			0.1	%/mA
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = 800_H			±5	mA
Load Regulation at Half Scale	LD_{REG}	R_L = 402 Ω to ∞, Data = 800_H		1	3	LSB
Capacitive Load	C_L	No Oscillation[3]		500		pF
DYNAMIC CHARACTERISTICS[3]						
Crosstalk	C_T			>64		dB
Voltage Output Settling Time[5]	t_S	To ±1 LSB of Final Value		16		µs
Digital Feedthrough	F_T	Signal Measured at DAC Output, While Changing Data ($\overline{LDA}$ = $\overline{LDB}$ = "1")		35		nV s
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance	C_{IL}	Note 3			10	pF
TIMING SPECIFICATIONS[3, 6]						
Chip Select Pulse Width	t_{CSW}		30			ns
DAC Select Setup	t_{AS}		30			ns
DAC Select Hold	t_{AH}		0			ns
Data Setup	t_{DS}		30			ns
Data Hold	t_{DH}		10			ns
Load Setup	t_{LS}		20			ns
Load Hold	t_{LH}		10			ns
Load Pulse Width	t_{LDW}		20			ns
Reset Pulse Width	t_{RSW}		30			ns
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		4	7	mA
		V_{IL} = 0 V, V_{DD} = +5 V		1	2	mA
Power Dissipation[7]	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		20	35	mW
		V_{IL} = 0 V, V_{DD} = +5 V		5	10	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTES
[1]1 LSB = 1 mV for 0 V to +4.095 V output range.
[2]Includes internal voltage reference error.
[3]These parameters are guaranteed by design and not subject to production testing.
[4]Very little sink current is available at the V_{REF} pin. Use external buffer if setting up a virtual ground.
[5]Settling time is not guaranteed for the first six codes 0 through 5.
[6]All input control signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[7]Power dissipation is a calculated value $I_{DD} \times 5$ V.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to DGND & AGND ..... –0.3 V, +7 V
Logic Inputs to DGND ..... –0.3 V, V_{DD} + 0.3 V
V_{OUT} to AGND ..... –0.3 V, V_{DD} + 0.3 V
V_{REF} to AGND ..... –0.3 V, V_{DD} + 0.3 V
AGND to DGND ..... –0.3 V, V_{DD}
I_{OUT} Short Circuit to GND ..... 50 mA
Package Power Dissipation ..... $(T_J \text{ max} - T_A)/\theta_{JA}$
Thermal Resistance, θ_{JA}
24-Pin Plastic DIP Package (N-24) ..... 62°C/W
24-Lead SOIC Package (SOL-24) ..... 73°C/W
Maximum Junction Temperature (T_J max) ..... 150°C
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



Timing Diagram

ORDERING INFORMATION[1]

Model	Temperature Range	Package Description	Package Option[2]
AD8582AN	–40°C to +85°C	24-Pin Plastic DIP	N-24
AD8582AR	–40°C to +85°C	24-Lead SOIC	SOL-24
AD8582Chips	+25°C	Die	

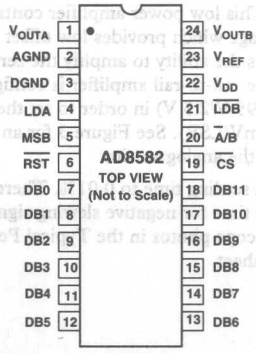
NOTES
[1]For die specifications contact your local Analog Devices sales office. The AD8582 contains 1270 transistors.
[2]For outline information see Package Information section.

PIN DESCRIPTION

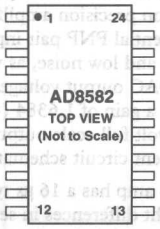
Pin No.	Name	Description
1, 24	V_{OUTA} V_{OUTB}	Voltage outputs from the DACs. Fixed output voltage range of 0 V to 4.095 V with 1 mV/LSB. An internal temperature stabilized reference maintains a fixed full-scale voltage independent of time, temperature and power supply variations.
2	AGND	Analog Ground. Ground reference for the internal bandgap reference voltage, the DAC, and the output buffer.
3	DGND	Digital ground for input logic.
4, 21	$\overline{LDA}$, $\overline{LDB}$	Load DAC register strobes. Transfers input register data to the DAC registers. Active low inputs, Level sensitive latch. May be connected together to double-buffer load DAC registers.
5	MSB	Digital Input: High presets DAC registers to half scale (800_H), Low clears DAC registers to zero (000_H) upon $\overline{RST}$ assertion.
6	$\overline{RST}$	Active low digital input that clears the DAC register to zero, setting the DAC to minimum scale when MSB pin = 0, or half-scale when MSB pin = 1.
7–18	DB_{0-11}	Twelve Binary Data Bit Inputs. DB11 is the MSB and DB0 is the LSB.
19	$\overline{CS}$	Chip Select. Active low input.
20	$\overline{A/B}$	Select DAC A = 0 or DAC B = 1.
22	V_{DD}	Positive Supply. Nominal value +5 V, ±5%.
23	V_{REF}	Nominal 2.5 V reference output voltage. This node must be buffered if required to drive external loads.

PIN CONFIGURATIONS

N-24
24-Pin Plastic DIP



SOL-24
24-Pin SOIC



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8582 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table I. Control Logic Truth Table

$\overline{CS}$	A/B	$\overline{LDA}$	$\overline{LDB}$	$\overline{RST}$	MSB	Input Register	DAC Register
L	L	H	H	H	X	Write to A	Latched
L	H	H	H	H	X	Write to B	Latched
L	L	L	H	H	X	Write to A	A Transparent
L	H	H	L	H	X	Write to B	B Transparent
H	X	L	L	H	X	Latched	A & B Transparent
H	X	^	^	H	X	Latched	Latched
X	X	X	X	L	L	Reset to Zero Scale	Reset to Zero Scale
X	X	X	X	L	H	Reset to Midscale	Reset to Midscale
H	X	X	X	^	X	Latch Reset Value	Latch Reset Value

^Denotes positive edge triggered.

OPERATION

The AD8582 is a complete, ready-to-use dual 12-bit digital-to-analog converter. Only one +5 V power supply is necessary for operation. It contains two voltage-switched, 12-bit, laser-trimmed digital-to-analog converters, a curvature-corrected bandgap reference, rail-to-rail output op amps, input registers, and DAC registers. The parallel data interface consists of twelve data bits, DB0–DB11, an address select pin A/B, two load strobe pins ($\overline{LDA}$, $\overline{LDB}$) and an active low $\overline{CS}$ strobe. In addition an asynchronous $\overline{RST}$ pin will set all DAC register bits to zero causing the V_{OUT} to become zero volts, or to midscale for trimming applications when the MSB pin is programmed to Logic 1. This function is useful for power on reset or system failure recovery to a known state.

D/A CONVERTER SECTION

The internal DAC is a 12-bit voltage-mode device with an output that swings from AGND potential to the 2.5 volt internal bandgap voltage. It uses a laser trimmed R-2R ladder which is switched by N channel MOSFETs. The output voltage of the DAC has a constant resistance independent of digital input code. The DAC output (not available to the user) is internally connected to the rail-to-rail output op amp.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. This low power amplifier contains a differential PNP pair input stage which provides low offset voltage and low noise, as well as the ability to amplify the zero-scale DAC output voltages. The rail-to-rail amplifier is configured in a gain of 1.6384 (= 4.095 V/2.5 V) in order to set the 4.095 volt full-scale output (1 mV/LSB). See Figure 3 for an equivalent circuit schematic of the analog section.

The op amp has a 16 µs typical settling time to 0.01%. There are slight differences in settling time for negative slewing signals versus positive. See the oscilloscope photos in the Typical Performances section of this data sheet.

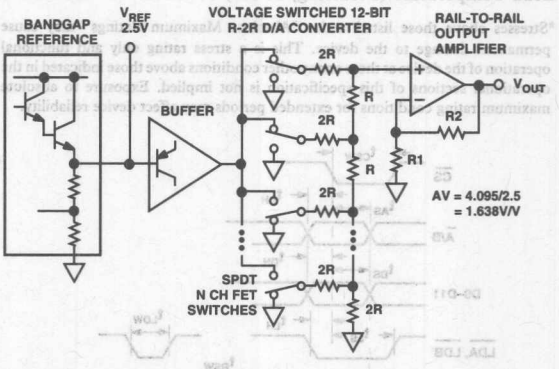


Figure 3. Equivalent Schematic of Analog Portion

OUTPUT SECTION

The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 4 shows an equivalent output schematic of the rail-to-rail amplifier with its N channel pull-down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P channel pull-up device that can supply GND terminated loads, especially important at the –5% supply tolerance value of 4.75 volts.

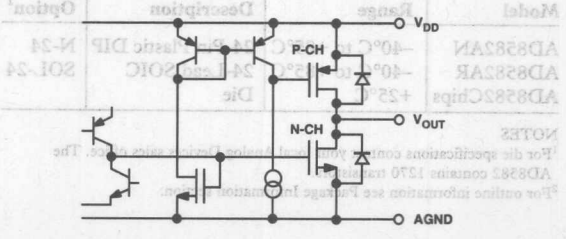


Figure 4. Equivalent Analog Output Circuit

Figures 5 and 6 in the typical performance characteristics section provide information on output swing performance near ground and full-scale as a function of load. In addition to resistive load driving capability, the amplifier has also been carefully designed and characterized for up to 500 pF capacitive load driving capability.

REFERENCE SECTION

The internal 2.5 V curvature-corrected bandgap voltage reference is laser trimmed for both initial accuracy and low temperature coefficient. The voltage generated by the reference is available at the V_{REF} pin. Since V_{REF} is not intended to drive external loads, it must be buffered. The equivalent emitter follower output circuit of the V_{REF} pin is shown in Figure 3.

Bypassing the V_{REF} pin will improve noise performance; however, bypassing is not required for proper operation. Figure 8 shows broadband noise performance.

POWER SUPPLY

The very low power consumption of the AD8582 is a direct result of a circuit design optimizing use of the CBCMOS process. By using the low power characteristics of the CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors good analog accuracy is achieved.

For power-consumption sensitive applications it is important to note that the internal power consumption of the AD8582 is strongly dependent on the actual logic-input voltage levels present on the DB0–DB11, $\overline{CS}$, $\overline{A}$/B, MSB, $\overline{LDA}$, $\overline{LDB}$ and $\overline{RST}$ pins. Since these inputs are standard CMOS logic structures they contribute static power dissipation dependent on the actual driving logic V_{OH} and V_{OL} voltage levels. The graph in Figure 9 shows the effect on total AD8582 supply current as a function of the actual value of input logic voltage. Consequently, for optimum dissipation use of CMOS logic versus TTL provides minimal dissipation in the static state. A V_{INL} = 0 V on the DB0–11 pins provides the lowest standby dissipation of 1 mA typical with a +5 V power supply.

As with any analog system, it is recommended that the AD8582 power supply be bypassed on the same PC card that contains the chip. Figure 10 shows the power supply rejection versus frequency performance. This should be taken into account when using higher frequency switched-mode power supplies with ripple frequencies of 100 kHz and higher.

One advantage of the rail-to-rail output amplifiers used in the AD8582 is the wide range of usable supply voltage. The part is fully specified and tested over temperature for operation from +4.75 V to +5.25 V. If reduced linearity and source current capability near full scale can be tolerated, operation of the AD8582 is possible down to +4.3 volts. The minimum operating supply voltage versus load current plot, in Figure 1, provides information for operation below V_{DD} = +4.75 V.

TIMING AND CONTROL

The input registers are level triggered and acquire data from the data bus during the time period when $\overline{CS}$ is low. The input register selected is determined by the $\overline{A}$/B select pin, see Table I. for a complete description. When $\overline{CS}$ goes high, the data is latched into the register and held until $\overline{CS}$ returns low. The minimum time required for the data to be present on the bus before $\overline{CS}$ returns high is called the data setup time (t_{DS}) as seen in Timing Diagram. The data hold time (t_{DH}) is the amount of time that the data has to remain on the bus after $\overline{CS}$ goes high. The high speed timing offered by the AD8582 provides for direct interface with no wait states in all but the fastest microprocessors.

The data from the input registers is transferred to the DAC registers by the active low $\overline{LDA}$ and $\overline{LDB}$ pins. If these inputs are tied together, a single logic input can perform a double buffer update of the DAC registers, which in turn simultaneously changes the analog output voltages to a new value. If the $\overline{LDA}$ and $\overline{LDB}$ pins are wired low, they become transparent. In this mode the input register data will directly control the output voltages. Refer to the Control Logic Truth Table for a complete description.

Unipolar Output Operation

This is the basic mode of operation for the AD8582. The AD8582 has been designed to drive loads as low as 820Ω in parallel with 500 pF. The code table for this operation is shown in Table II.

Table II. Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	+ 4.095
801	2049	+ 2.049
800	2048	+ 2.048
7FF	2047	+ 2.047
000	0	0

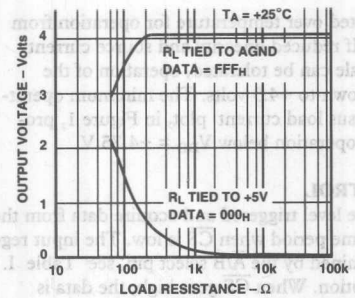


Figure 5. Output Swing vs. Load

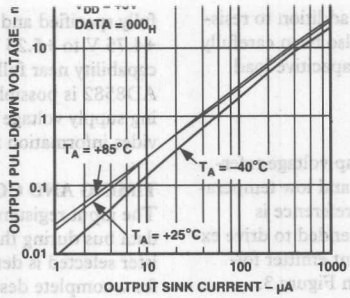


Figure 6. Pull-Down Voltage vs. Output Sink Current Capability

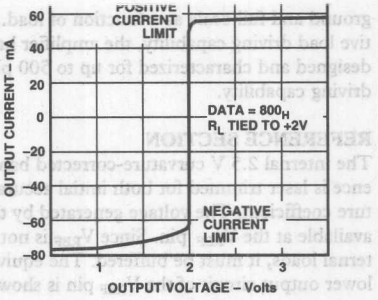


Figure 7. I_{OUT} vs. V_{OUT}

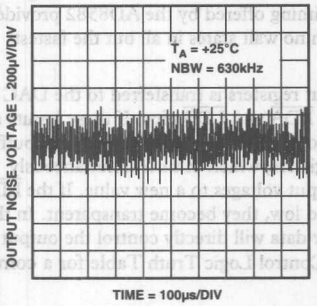


Figure 8. Broadband Noise

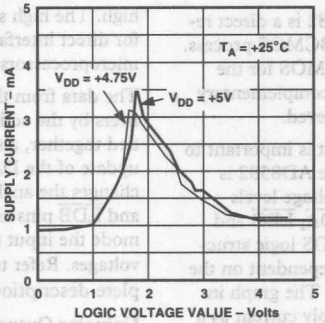


Figure 9. Supply Current vs. Logic Input Voltage

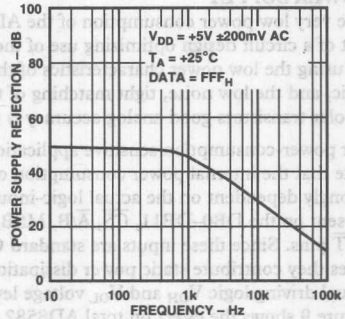


Figure 10. Power Supply Rejection vs. Frequency

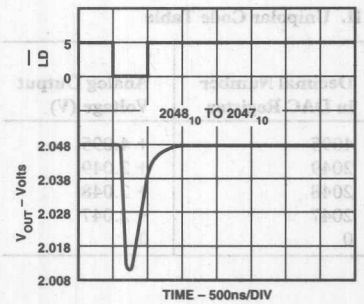


Figure 11. Midscale Transition Performance

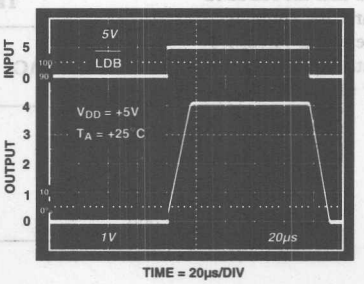


Figure 12. Large Signal Settling Time

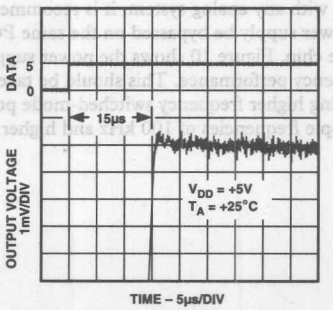


Figure 13. Output Voltage Rise Time Detail

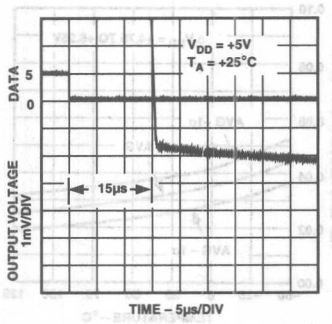


Figure 14. Output Voltage Fall Time Detail

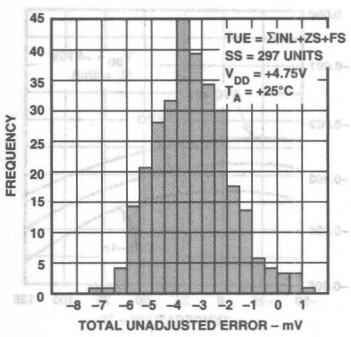


Figure 15. Total Unadjusted Error Histogram

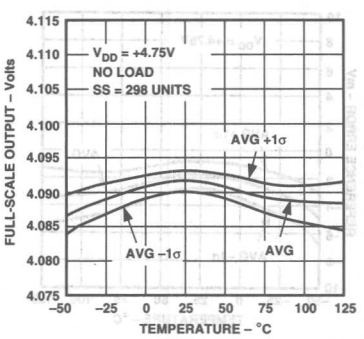


Figure 16. Full-Scale Voltage vs. Temperature

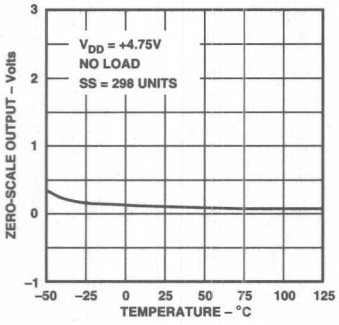


Figure 17. Zero-Scale Voltage vs. Temperature

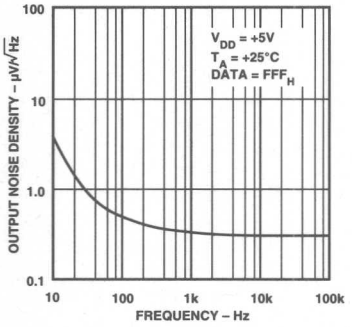


Figure 18. Output Voltage Noise Density vs. Frequency

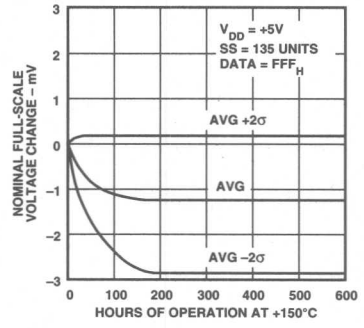


Figure 19. Long-Term Drift Accelerated by Burn-In

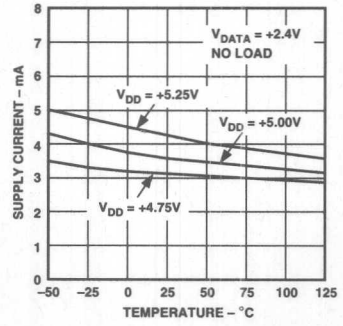


Figure 20. Supply Current vs. Temperature

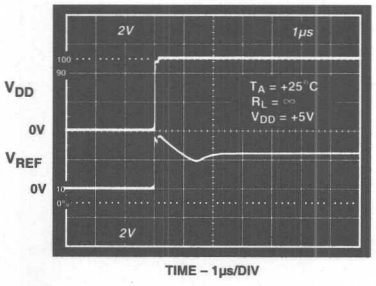


Figure 21. Reference Startup vs. Time

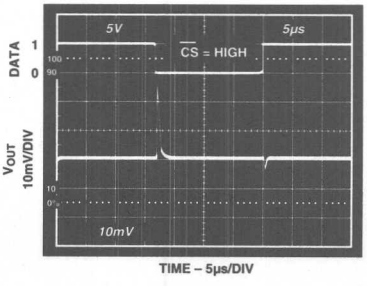


Figure 22. Digital Feedthrough vs. Time

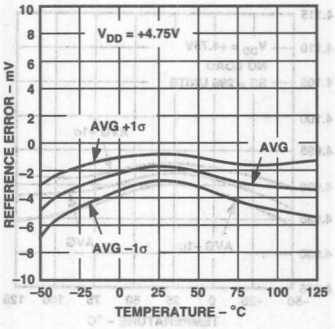


Figure 23. Reference Error vs. Temperature

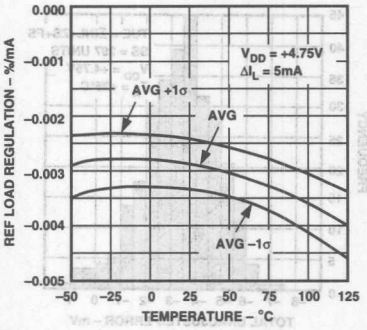


Figure 24. Reference Load Regulation vs. Temperature

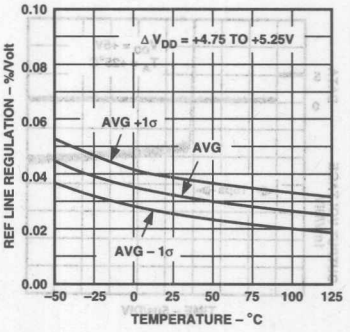


Figure 25. Reference Line Regulation vs. Temperature

16-Channel, 8-Bit Multiplying DAC

AD8600*

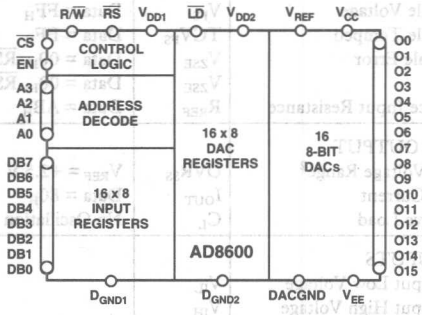
FEATURES

- 16 Independently Addressable Voltage Outputs
- Full-Scale Set by External Reference
- 2 µs Settling Time
- Double Buffered 8-Bit Parallel Input
- High Speed Data Load Rate
- Data Readback
- Operates from Single +5 V
- Optional ±6 V Supply Extends Output Range

APPLICATIONS

- Phased Array Ultrasound & Sonar
  - Power Level Setting
  - Receiver Gain Setting
- Automatic Test Equipment
- LCD Clock Level Setting

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8600 contains 16 independent voltage output digital-to-analog converters that share a common external reference input voltage. Each DAC has its own DAC register and input register to allow double buffering. An 8-bit parallel data input, four address pins, a $\overline{CS}$ select, a $\overline{LD}$, $\overline{EN}$, R/$\overline{W}$, and $\overline{RS}$ provide the digital interface.

The AD8600 is constructed in a monolithic CBCMOS process which optimizes use of CMOS for logic and bipolar for speed and precision. The digital-to-analog converter design uses voltage mode operation ideally suited to single supply operation. The internal DAC voltage range is fixed at DACGND to V_{REF}. The voltage buffers provide an output voltage range that approaches ground and extends to 1.0 V below V_{CC}. Changes in reference voltage values and digital inputs will settle within ±1 LSB in 2 µs.

Data is preloaded into the input registers one at a time after the internal address decoder selects the input register. In the write mode (R/$\overline{W}$ low) data is latched into the input register during the positive edge of the $\overline{EN}$ pulse. Pulses as short as 40 ns can be used to load the data. After changes have been submitted to the input registers, the DAC registers are simultaneously updated by a common load $\overline{EN} \times \overline{LD}$ strobe. The new analog output voltages simultaneously appear on all 16 outputs.

At system power up or during fault recovery the reset ($\overline{RS}$) pin forces all DAC registers into the zero state which places zero volts at all DAC outputs.

The AD8600 is offered in the PLCC-44 package. The device is designed and tested for operation over the extended industrial temperature range of –40°C to +85°C.

*Patent pending.

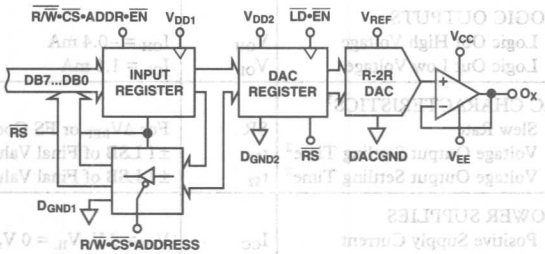
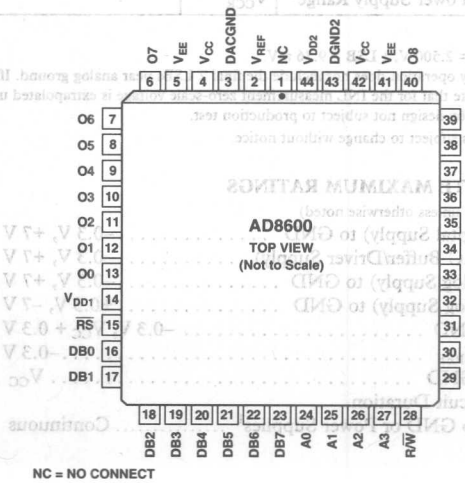


Figure 1. Equivalent DAC Channel

PIN CONFIGURATION



NC = NO CONNECT

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE[1]						
Resolution	N		8			Bits
Relative Accuracy[2]	INL		–1	±1/2	+1	LSB
Differential Nonlinearity[2]	DNL	Guaranteed Monotonic	–1	±1/4	+1	LSB
Full-Scale Voltage	V_{FS}	Data = FF_H	2.480	2.490	2.500	V
Full-Scale Tempco	TCV_{FS}	Data = FF_H		±20		ppm/°C
Zero Scale Error	V_{ZSE}	Data = 00_H, $\overline{RS}$ = "0," T_A = +25°C			+3.5	LSB
	V_{ZSE}	Data = 00_H, $\overline{RS}$ = "0"			+5	LSB
Reference Input Resistance	R_{REF}	Data = AB_H	1.2	2		kΩ
ANALOG OUTPUT						
Output Voltage Range[2]	OVR_{SS}	V_{REF} = +2.5 V	0.000		2.500	V
Output Current	I_{OUT}	Data = 80_H		±2		mA
Capacitive Load	C_L	No Oscillation		50		pF
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Logic Input Current	I_{IL}				10	µA
Logic Input Capacitance[3]	C_{IL}				10	pF
LOGIC OUTPUTS						
Logic Out High Voltage	V_{OH}	I_{OH} = –0.4 mA	3.5			V
Logic Out Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
AC CHARACTERISTICS[3]						
Slew Rate	SR	For ΔV_{REF} or FS Code Change	4	7		V/µs
Voltage Output Settling Time[2]	t_{S1}	±1 LSB of Final Value, Full-Scale Data Change		2		µs
Voltage Output Settling Time[2]	t_{S2}	±1 LSB of Final Value, ΔV_{REF} = 1 V, Data = FF_H		2		µs
POWER SUPPLIES						
Positive Supply Current	I_{CC}	V_{IH} = 5 V, V_{IL} = 0 V, No Load		24	35	mA
Logic Supply Currents	$I_{DD1\&2}$	V_{IH} = 5 V, V_{IL} = 0 V, No Load			0.1	mA
Power Dissipation	P_{DISS}	V_{IH} = 5 V, V_{IL} = 0 V, No Load		120	175	mW
Power Supply Sensitivity	PSS	ΔV_{CC} = ±5%			0.007	%/%
Logic Power Supply Range	V_{DDR}		4.75		5.25	V
Positive Power Supply Range[3]	V_{CCR}		V_{DD}		7.0	V

NOTES

[1]When V_{REF} = 2.500 V, 1 LSB = 9.76 mV.

[2]Single supply operation does not include the final 2 LSBs near analog ground. If this performance is critical, use a negative supply (V_{EE}) pin of at least –0.7 V to –5.25 V. Note that for the INL measurement zero-scale voltage is extrapolated using codes 7_{10} to 80_{10}.

[3]Guaranteed by design not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A= +25°C unless otherwise noted)

V_{DD1} (Digital Supply) to GND ..... –0.3 V, +7 V
V_{DD2} (DAC Buffer/Driver Supply) ..... –0.3 V, +7 V
V_{CC} (Analog Supply) to GND ..... –0.3 V, +7 V
V_{EE} (Analog Supply) to GND ..... +0.3 V, –7 V
V_{REF} to GND ..... –0.3 V, V_{CC} + 0.3 V
V_{DD2} to V_{REF} ..... –0.3 V
V_{OUT} to GND ..... V_{CC}
Short Circuit Duration
V_{OUT} to GND or Power Supplies[1] ..... Continuous
Digital Input/Output Voltage to GND ... –0.3 V, V_{DD} + 0.3 V
Thermal Resistance–Theta Junction-to-Ambient (θ_{JA})
PLCC-44 ..... 47°C/W
Package Power Dissipation ..... $(T_J - T_A)/\theta_{JA}$
Maximum Junction Temperature T_J max ..... 150°C
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

NOTE

[1]No more than four outputs may be shorted to power or GND simultaneously.

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE[1]						
Resolution	N		8			Bits
Total Unadjusted Error	TUE	All Other DACs Loaded with Data = 55_H	–1	±3/4	+1	LSB
Relative Accuracy	INL		–1	±1/2	+1	LSB
Differential Nonlinearity	DNL	Guaranteed Monotonic	–1	±1/4	+1	LSB
Full-Scale Voltage	V_{FS}	Data = FF_H, V_{REF} = +3.5 V	3.473	3.486	3.500	V
Full-Scale Voltage Error	V_{FSE}	Data = FF_H, V_{REF} = +3.5 V	–1		+1	LSB
Full-Scale Tempco	TCV_{FS}	Data = FF_H, V_{REF} = +3.5 V		±20		ppm/°C
Zero Scale Error	V_{ZSE}	Data = 00_H, $\overline{RS}$ = "0," T_A = +25°C	–2	±1	+2	mV
Zero Scale Error	V_{ZSE}	Data = 00_H, All Other DACs Data = 00_H	–1		+1	LSB
Zero Scale Error	V_{ZSE}	Data = 00_H, All Other DACs Data = 55_H		±1/2		LSB
Zero Scale Tempco	TCV_{ZS}	Data = 00_H, V_{CC} = +5 V, V_{EE} = –5 V		±10		µV/°C
Reference Input Resistance	R_{REF}	Data = AB_H	1.2	2		kΩ
Reference Input Capacitance[2]	C_{REF}	Data = AB_H			240	pF
ANALOG OUTPUT						
Output Voltage Range	OVR_1	V_{REF} = +3.5 V	0.000		3.500	V
Output Voltage Range[2]	OVR_2	$V_{CC} = V_{DD2}$ = +7 V, V_{EE} = –0.7 V, V_{REF} = 5 V	0.000		5.000	V
Output Current	I_{OUT}	Data = 80_H		±2		mA
Capacitive Load[2]	C_L	No Oscillation		50		pF
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Logic Input Current	I_{IL}				10	µA
Logic Input Capacitance[2]	C_{IL}				10	pF
LOGIC OUTPUTS						
Logic Out High Voltage	V_{OH}	I_{OH} = –0.4 mA	3.5			V
Logic Out Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
AC CHARACTERISTICS[2]						
Reference In Bandwidth	BW	–3 dB Frequency, V_{REF} = 2.5 V_{DC} + 0.1 V_{AC}	500			kHz
Slew Rate	SR	For ΔV_{REF} or FS Code Change	4	7		V/µs
Voltage Noise Density	e_N	f = 1 kHz, V_{REF} = 0 V		46		$nV/\sqrt{Hz}$
Digital Feedthrough	FT	Digital Inputs to DAC Outputs		10		nVs
Voltage Output Settling Time[3]	t_{S1}	±1 LSB of Final Value, FS Data Change		1	2	µs
Voltage Output Settling Time[3]	t_{S2}	±1 LSB of Final Value, ΔV_{REF} = 1 V, Data = FF_H		1	2	µs
POWER SUPPLIES						
Positive Supply Current	I_{CC}	V_{IH} = 5 V, V_{IL} = 0 V, V_{EE} = –5 V, No Load		22	35	mA
Negative Supply Current	I_{EE}	V_{IH} = 5 V, V_{IL} = 0 V, V_{EE} = –5 V, No Load		22	35	mA
Logic Supply Currents	$I_{DD1\&2}$	V_{IH} = 5 V, V_{IL} = 0 V, V_{EE} = –5 V, No Load			0.1	mA
Power Dissipation[4]	P_{DISS}	V_{IH} = 5 V, V_{IL} = 0 V, V_{EE} = –5 V, No Load		225	350	mW
Power Supply Sensitivity	PSS	ΔV_{CC} & ΔV_{EE} = ±5%			0.007	%/%
Logic Power Supply Range	V_{DDR}		4.75		5.25	V
Pos Power Supply Range[2]	V_{CCR}		V_{DD}		7.0	V
Neg Power Supply Range[2]	V_{EER}		–5.25		0.0	V

NOTES
[1]When V_{REF} = +3.500 V, 1 LSB = 13.67 mV.
[2]Guaranteed by design not subject to production test.
[3]Settling time test is performed using R_L = 50 kΩ and C_L = 35 pF.
[4]Power Dissipation is calculated using 5 V × (I_{DD} + |I_{SS}| + I_{DD1} + I_{DD2}).
Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8600 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ELECTRICAL CHARACTERISTICS (@ $V_{DD1} = V_{DD2} = V_{CC} = +5\ V \pm 5\%$, $V_{EE} = -5\ V$, $V_{REF} = +3.500\ V$, $-40°C \le T_A \le +85°C$, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
INTERFACE TIMING[1, 2]						
Clock ($\overline{EN}$) Frequency	f_{CLK}	Data Loading			12.5	MHz
Clock ($\overline{EN}$) High Pulse Width	t_{CH}		40			ns
Clock ($\overline{EN}$) LowPulse Width	t_{CL}		40			ns
Data Setup Time	t_{DS}		40			ns
Data Hold Time	t_{DH}		10			ns
Address Setup Time	t_{AS}		0			ns
Address Hold Time	t_{AH}		0			ns
Valid Address to Data Valid	t_{AD}				160	ns
Load Enable Setup Time	t_{LS}		0			ns
Load Enable Hold Time	t_{LH}		0			ns
Read/Write to Clock ($\overline{EN}$)	t_{RWC}		30			ns
Read/Write to DataBus Hi-Z	t_{RWZ}				120	ns
Read/Write to DataBus Active	t_{RWD}				120	ns
Clock ($\overline{EN}$) to Read/Write	t_{TWH}		0			ns
Clock ($\overline{EN}$) to Chip Select	t_{TCH}		0			ns
Chip Select to Clock ($\overline{EN}$)	t_{CSC}		30			ns
Chip Select to Data Valid	t_{CSD}				120	ns
Chip Select to DataBus Hi-Z	t_{CSZ}				150	ns
Reset Pulse Width	t_{RS}		25			ns

NOTES
[1]Guaranteed by design not subject to production test.
[2]All logic input signals have maximum rise and fall times of 2 ns.
Specifications subject to change without notice.

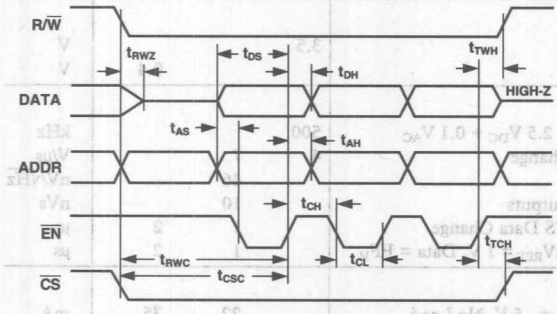


Figure 2. Write Timing

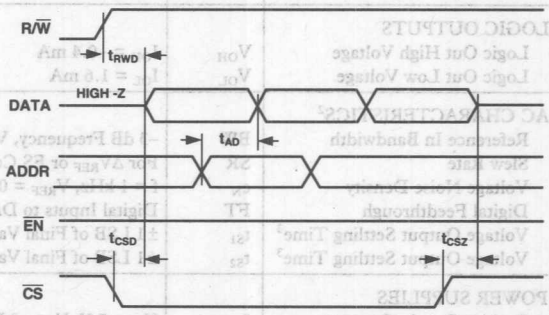


Figure 3. Readback Timing

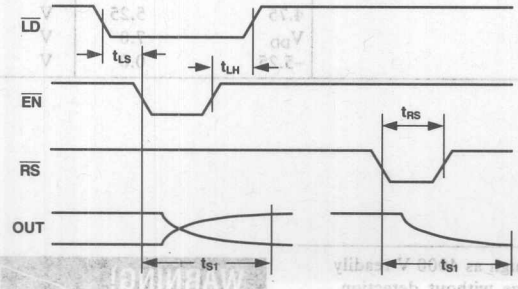


Figure 4. Write to DAC Register & Voltage Output Settling Timing (CS= High, Prevents Input Register Changes)

ORDERING GUIDE

Model	Temperature	Package Description	Package Option[1]
AD8600AP	–40°C to +85°C	44-Lead PLCC	P-44A
AD8600Chips	+25°C	Die[2]	

NOTES
[1]For outline information see Package Information section.
[2]For die specifications contact your local Analog Devices sales office.
The AD8600 contains 5782 transistors.

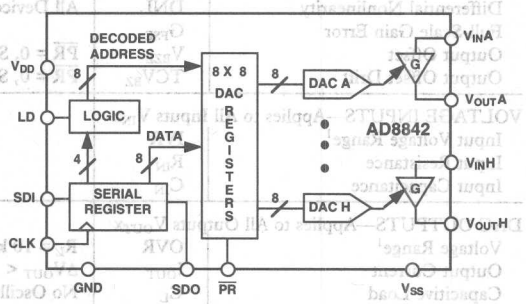
8-Bit Octal, 4-Quadrant Multiplying, CMOS TrimDAC

AD8842

FEATURES
Low Cost
Replaces 8 Potentiometers
50 kHz 4-Quadrant Multiplying Bandwidth
Low Zero Output Error
Eight Individual Channels
3-Wire Serial Input
500 kHz Update Data Loading Rate
±3 V Output Swing
Midscale Preset, Zero Volts Out

APPLICATIONS
Automatic Adjustment
Trimmer Replacement
Vertical Deflection Amplitude Adjustment
Waveform Generation and Modulation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8842 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC® capability allows replacement of the mechanical trimmer function in new designs. The AD8842 is ideal for ac or dc gain control of up to 50 kHz bandwidth signals. The four-quadrant multiplying capability is useful for signal inversion and modulation often found in video vertical deflection circuitry.

Internally the AD8842 contains eight voltage output digital-to-analog converters, each with separate voltage inputs. A new current conveyor amplifier design performs the four-quadrant multiplying function with a single amplifier at the output of the current steering digital-to-analog converter. This approach offers an improved constant input resistance performance versus previous voltage switched DACs used in TrimDAC circuits, eliminating the need for additional input buffer amplifiers.

Each DAC has its own DAC register that holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register that is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy chaining in multiple DAC applications without additional external decoding logic.

The AD8842 consumes only 95 mW from ±5 V power supplies. For single 5 V supply applications consult the DAC-8841. The AD8842 is pin compatible with the 1 MHz multiplying bandwidth DAC8840. The AD8842 is available in 24-pin plastic DIP and surface mount SOL-24 packages.

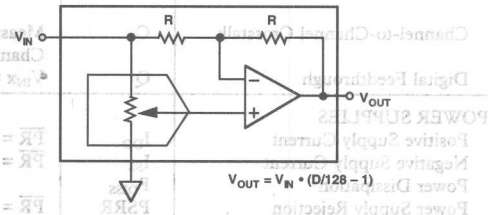


Figure 1. Functional Circuit of One 4-Quadrant Multiplying Channel

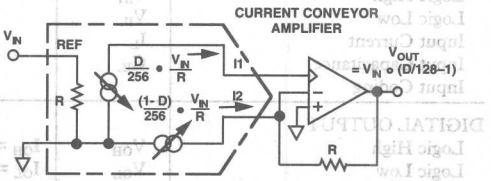


Figure 2. Actual Current Conveyor Implementation of Multiplying DAC Channel

TrimDAC is a registered trademark of Analog Devices, Inc.
The current conveyor amplifier is a patented circuit belonging to Analog Devices, Inc.

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AD8842–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = +5 V, V_{SS} = –5 V, All $V_{IN}x$ = +3 V, T_A = –40°C to +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY—All Specifications Apply for DACs A, B, C, D, E, F, G, H						
Resolution	N		8			Bits
Integral Nonlinearity Error	INL			±0.2	±1	LSB
Differential Nonlinearity	DNL	All Devices Monotonic		±0.4	±1	LSB
Full-Scale Gain Error	G_{FSE}			2		LSB
Output Offset	V_{BZE}	$\overline{PR}$ = 0, Sets D = 80_H		5	25	mV
Output Offset Drift	TCV_{BZ}	$\overline{PR}$ = 0, Sets D = 80_H		5		µV/°C
VOLTAGE INPUTS—Applies to All Inputs $V_{IN}x$						
Input Voltage Range[1]	IVR		±3	±4		V
Input Resistance	R_{IN}		12	19		kΩ
Input Capacitance	C_{IN}			9		pF
DAC OUTPUTS—Applies to All Outputs $V_{OUT}x$						
Voltage Range[1]	OVR	R_L = 10 kΩ	±3	±4		V
Output Current	I_{OUT}	ΔV_{OUT} < 1.5 LSB	±3			mA
Capacitive Load	C_L	No Oscillation		500		pF
DYNAMIC PERFORMANCE—Applies to All DACs						
Full Power Gain Bandwidth[1]	GBW	$V_{IN}x$ = ±3 V_P, R_L = 2 kΩ, C_L = 10 pF	10	50		kHz
Slew Rate		Measured 10% to 90%				
Positive	SR+	$\Delta V_{OUT}x$ = +5.5 V	0.5	1.0		V/µs
Negative	SR–	$\Delta V_{OUT}x$ = –5.5 V	1.0	1.8		V/µs
Total Harmonic Distortion	THD	$V_{IN}x$ = 4 V p-p, D = FF_H, f = 1 kHz, f_{LPF} = 80 kHz, R_L = 1 kΩ		0.01		%
Spot Noise Voltage	e_N	f = 1kHz, V_{IN} = 0 V		78		nV/√Hz
Output Settling Time	t_S	±1 LSB Error Band, D = 00_H to FF_H		2.9		µs
		D = FF_H to 00_H		5.4		µs
Channel-to-Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz		72		dB
Digital Feedthrough	Q	$V_{IN}x$ = 0 V, D = 0 to 255_{10}		5		nV-s
POWER SUPPLIES						
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V		10	14	mA
Negative Supply Current	I_{SS}	$\overline{PR}$ = 0 V		9	13	mA
Power Dissipation[2]	P_{DISS}			95	135	mW
Power Supply Rejection	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%		0.0001	0.01	%/%
Power Supply Range	PSR	V_{DD}, $\lvert V_{SS} \rvert$	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	µA
Input Capacitance	C_{IL}			7		pF
Input Coding				Offset Binary		
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = –0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
TIMING SPECIFICATIONS[1]						
Input Clock Pulse Width	t_{CH}, t_{CL}		60			ns
Data Setup Time	t_{DS}		40			ns
Data Hold Time	t_{DH}		20			ns
CLK to SDO Propagation Delay	t_{PD}				80	ns
DAC Register Load Pulse Width	t_{LD}		70			ns
Preset Pulse Width	t_{PR}		50			ns
Clock Edge to Load Time	t_{CKLD}		30			ns
Load Edge to Next Clock Edge	t_{LDCK}		60			ns

NOTES
[1]Guaranteed by design, not subject to production test.
[2]Calculated limit = 5 V × (I_{DD} + I_{SS}).
Specifications subject to change without notice.

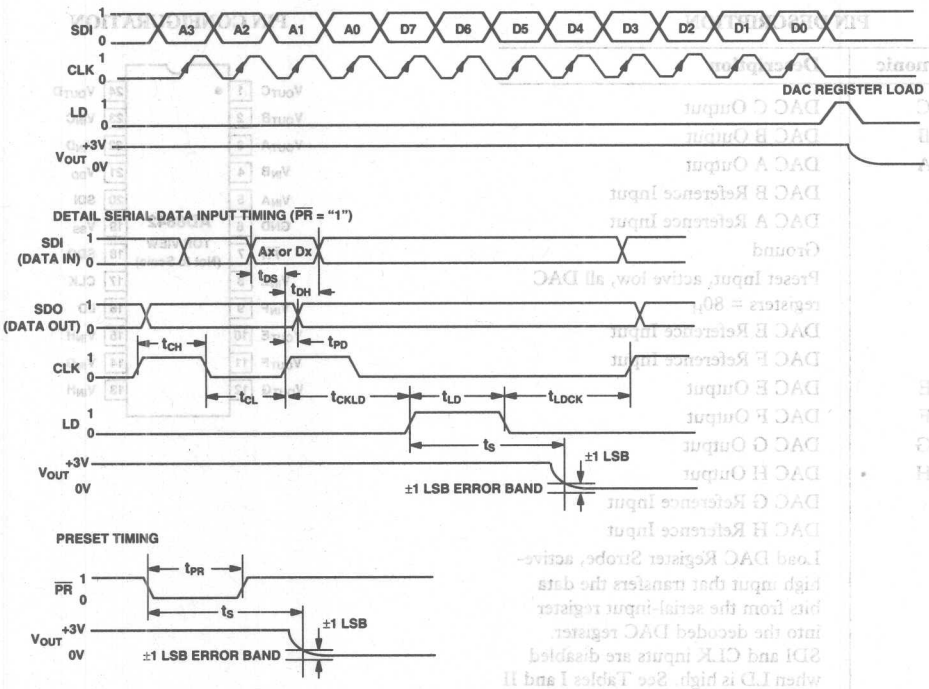


Figure 3. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... –0.3 V, +7 V
V_{SS} to GND ..... +0.3 V, –7 V
$V_{IN}x$ to GND ..... V_{DD}, V_{SS}
$V_{OUT}x$ to GND ..... V_{DD}, V_{SS}
Short Circuit $I_{OUT}x$ to GND ..... Continuous
Digital Input & Output Voltage to GND ..... V_{DD}, 0 V
Operating Temperature Range .....–40°C to +85°C
Maximum Junction Temperature (T_J Max) ..... +150°C
Storage Temperature .....–65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... (T_J Max–T_A)/θ_{JA}
Thermal Resistance θ_{JA},
SOIC (SOL-24) ..... 70°C/W
P-DIP (N-24) ..... 57°C/W

ORDERING GUIDE

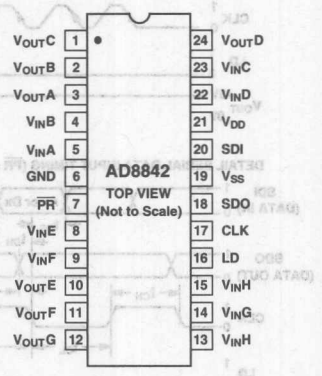
Model	Temperature Range[1]	Package Description	Package Option[2]
AD8842AN	XIND	24-Pin 300mil P-DIP	N-24
AD8842AR	XIND	24-Pin 300mil SOIC	SOL-24

NOTES
[1]XIND = –40°C to +85°C. The AD8842 contains 2452 transistors.
[2]For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8842 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

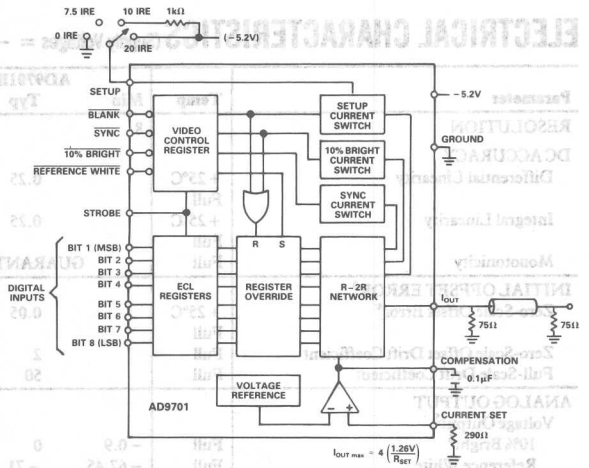
Pin	Mnemonic	Description
1	$V_{OUT}C$	DAC C Output
2	$V_{OUT}B$	DAC B Output
3	$V_{OUT}A$	DAC A Output
4	$V_{IN}B$	DAC B Reference Input
5	$V_{IN}A$	DAC A Reference Input
6	GND	Ground
7	$\overline{PR}$	Preset Input, active low, all DAC registers = 80_H
8	$V_{IN}E$	DAC E Reference Input
9	$V_{IN}F$	DAC F Reference Input
10	$V_{OUT}E$	DAC E Output
11	$V_{OUT}F$	DAC F Output
12	$V_{OUT}G$	DAC G Output
13	$V_{OUT}H$	DAC H Output
14	$V_{IN}G$	DAC G Reference Input
15	$V_{IN}H$	DAC H Reference Input
16	LD	Load DAC Register Strobe, active-high input that transfers the data bits from the serial-input register into the decoded DAC register. SDI and CLK inputs are disabled when LD is high. See Tables I and II
17	CLK	Serial Clock Input, positive edge triggered
18	SDO	Serial Data Output, active totem pole output
19	V_{SS}	Negative 5 V Power Supply
20	SDI	Serial Data Input
21	V_{DD}	Positive 5 V Power Supply
22	$V_{IN}D$	DAC D Reference Input
23	$V_{IN}C$	DAC C Reference Input
24	$V_{OUT}D$	DAC D Output



FEATURES
250MSPS Update Rate
Low Glitch Impulse
Complete Composite Functions
Internal Voltage Reference
Single −5.2V Supply

APPLICATIONS
Raster Scan Displays
Color Graphics
Automated Test Equipment
TV Video Reconstruction

FUNCTIONAL BLOCK DIAGRAM



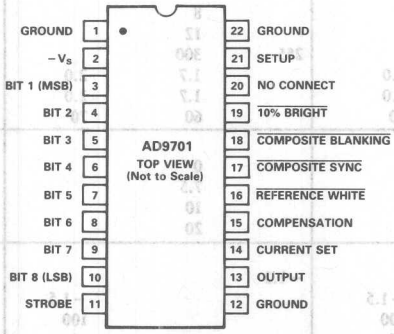
GENERAL DESCRIPTION

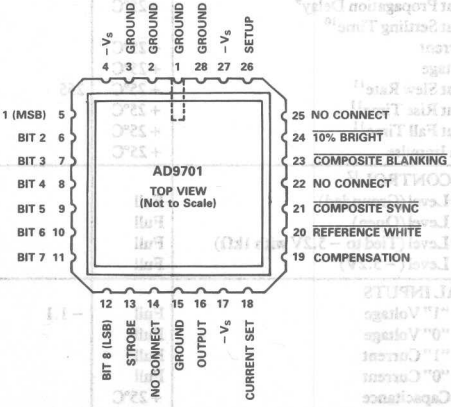
The AD9701 is a high-speed, 8-bit digital-to-analog converter with fully integrated composite video functions. High-speed ECL input registers provide synchronous operation of data and control functions up to 250MSPS.

The AD9701 incorporates on-board control functions including horizontal sync, blanking, reference white level, and a 10% bright signal for highlighting. The setup level is also adjustable from 0 IRE units to 20 IRE units, through the control pin. An internal voltage reference allows the AD9701 to operate as a stand-alone video reconstruction DAC.

The AD9701 is available as an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both grades of the AD9701 are packaged in a 22-pin ceramic DIP, with the extended temperature device also available in a 28-pin LCC package.

PIN CONFIGURATIONS





This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9701 – SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($-V_S$) . . . . . −7V
Digital Input Voltages (including STROBE, SYNC, BLANKING, 10% BRIGHT, and REFERENCE WHITE) . . . . . 0V to $-V_S$
Analog Output Current 37mA
Power Dissipation (+25°C Free Air)[2] 780mW
Operating Temperature Range
AD9701BQ . . . . . −25°C to +85°C
AD9701SQ/SE . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages = −5.2V; R_L = 37.5Ω; Setup = 0V, unless otherwise stated)

Parameter	Temp	AD9701BQ Min	AD9701BQ Typ	AD9701BQ Max	AD9701SQ/SE Min	AD9701SQ/SE Typ	AD9701SQ/SE Max	Units
RESOLUTION		8			8			Bits
DC ACCURACY								
Differential Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Integral Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Monotonicity	Full		GUARANTEED			GUARANTEED		
INITIAL OFFSET ERROR[3]								
Zero-Scale Offset Error[4]	+25°C		0.05	0.9		0.05	0.9	mV
	Full			0.9			0.9	mV
Zero-Scale Offset Drift Coefficient	Full		2			2		µV/°C
Full-Scale Drift Coefficient	Full		50			50		µV/°C
ANALOG OUTPUT								
Voltage Output[5]								
10% Bright[6]	Full	−0.9	0		−0.9	0		mV
Reference White	Full	−67.45	−71	−74.55	−67.45	−71	−74.55	mV
Blanking (Setup = 0 IRE)[7]	Full	−698.55	−708.5	−718.45	−698.55	−708.5	−718.45	mV
Sync (Setup = 0 IRE)[8]	Full	−979.25	−993.5	−1007.75	−979.25	−993.5	−1007.75	mV
Current Output[5]								
10% Bright[6]	Full	−0.024	0		−0.024	0		mA
Reference White	Full	−1.805	−1.9	−1.996	−1.805	−1.9	−1.995	mA
Blanking (Setup = 0 IRE)[7]	Full	−18.63	−18.9	−19.16	−18.63	−18.9	−19.16	mA
Sync (Setup = 0 IRE)[8]	Full	−26.11	−26.5	−26.87	−26.11	−26.5	−26.87	mA
Output Compliance Range	Full		−1.6; +0.1			−1.6; +0.1		V
Output Resistance	+25°C	640	800		640	800		Ω
DYNAMIC PERFORMANCE								
Update Rate	+25°C	225	250		225	250		MSPS
Output Propagation Delay[9]	+25°C		5	6		5	6	ns
Output Settling Time[10]								
Current	+25°C		8			8		ns
Voltage	+25°C		12			12		ns
Output Slew Rate[11]	+25°C	255	300		255	300		V/µs
Output Rise Time[11]	+25°C		1.7	2.0		1.7	2.0	ns
Output Fall Time[11]	+25°C		1.7	2.0		1.7	2.0	ns
Glitch Impulse	+25°C		60	70		60	70	pV-s
SETUP CONTROL[12]								
Setup Level (Grounded)	Full		0			0		IRE
Setup Level (Open)	Full		7.5			7.5		IRE
Setup Level (Tied to −5.2V with 1kΩ)	Full		10			10		IRE
Setup Level (−5.2V)	Full		20			20		IRE
DIGITAL INPUTS								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
Logic "1" Current	Full			100			100	µA
Logic "0" Current	Full			15			15	µA
Input Capacitance	+25°C		4	5.5		4	5.5	pF
Data Setup Time	+25°C	0.1			0.1			ns
Data Hold Time	+25°C	1.4			1.4			ns
POWER SUPPLY[13]								
Supply Current (−5.2V)	+25°C		140	160		140	160	mA
	Full			160			160	mA
Nominal Power Dissipation	+25°C		728			728		mW
Power Supply Rejection Ratio[14]	Full		3	6		3	6	mV/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Typical thermal impedance . . .

22-Pin Ceramic $\theta_{ja} = 64°C/W$; $\theta_{jc} = 16°C/W$

28-Pin Ceramic LCC $\theta_{ja} = 70°C/W$; $\theta_{jc} = 21°C/W$

[3]SYNC, BLANKING, and REFERENCE WHITE are inactive (Logic "1"). $I_{SET} \approx 1.26V/R_{SET}$.

[4]All bits at logic HIGH.

[5]All values are relative to full-scale output, after being normalized to nominal value. Typical variation in full-scale output from device to device can reach ±10%, for a fixed R_{SET} resistor.

[6]The effect of 10% BRIGHT algebraically adds to the output waveform.

[7]The output level with BLANKING active (Logic "0"), is determined by the setup control level.

[8]In normal operation, the BLANKING input is activated (Logic "0") prior to or in conjunction with the SYNC input. The effect of the SYNC output is relative to the setup level.

[9]Measured from edge of STROBE to 50% transition point of the output signal.

[10]Measured with full-scale change in output level, from the 10% transition level to within ±0.2% of the final output value.

[11]Measured from 10% to 90% transition point for full-scale step output.

[12]An IRE unit is 1% of the Grey Scale (GS range) with a 0 IRE setup level.

[13]Supply Voltage should remain stable within ±5% for normal operation.

[14]Measured at ±5% of $-V_S$.

Specifications subject to change without notice.

3

DIGITAL INPUTS VS. ANALOG OUTPUT

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	10% Bright	Ref. White	Blanking	Comp. Sync	Analog Output (mV)
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	−71
1	0	0	0	0	0	0	0	0	1	1	1	−320
0	0	0	0	0	0	0	0	0	1	1	1	−637.5
0	0	0	0	0	0	0	0	1	1	1	1	−708.5
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	X	1	0	1	1	−71
X	X	X	X	X	X	X	X	0	1	0	1	−637.50[1]
X	X	X	X	X	X	X	X	0	1	0	1	−690.75[2]
X	X	X	X	X	X	X	X	0	1	0	1	−708.50[3]
X	X	X	X	X	X	X	X	0	1	0	1	−779.50[4]
X	X	X	X	X	X	X	X	0	1	0	0	−922.50[1]
X	X	X	X	X	X	X	X	0	1	0	0	−975.75[2]
X	X	X	X	X	X	X	X	0	1	0	0	−993.50[3]
X	X	X	X	X	X	X	X	0	1	0	0	−1064.50[4]
X	X	X	X	X	X	X	X	1	1	0	0	−993.50[1]
X	X	X	X	X	X	X	X	1	1	0	0	−1046.75[2]
X	X	X	X	X	X	X	X	1	1	0	0	−1064.50[3]
X	X	X	X	X	X	X	X	1	1	0	0	−1135.50[4]

NOTES

1. Setup (Pin 21) grounded (0 IRE units).
2. Setup (Pin 21) open (7.5 IRE units).
3. Setup (Pin 21) to −5.2V through 1k (0 IRE units).
4. Setup (Pin 21) to −5.2V (20 IRE units).

ORDERING GUIDE

Device	Temperature Range	Description	Package Option*
AD9701BQ	−25°C to +85°C	22-Pin DIP, Industrial Temperature	Q-22
AD9701SE	−55°C to +125°C	28-Pin LCC, Extended Temperature	E-28A
AD9701SQ	−55°C to +125°C	22-Pin DIP, Extended Temperature	Q-22

*E = Leadless Ceramic Chip Carrier; Q = Cerdip. For outline information see Package Information section.

AD9712B/AD9713B

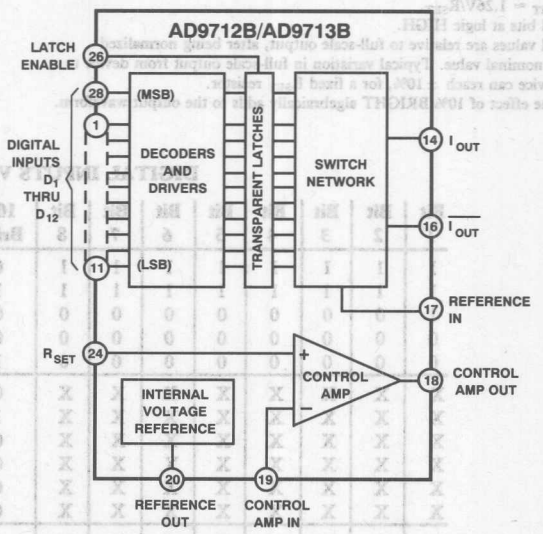
FEATURES
100 MSPS Update Rate
ECL/TTL Compatibility
SFDR @ 1 MHz: 70 dBc
Low Glitch Impulse: 28 pV-s
Fast Settling: 27 ns
Low Power: 725 mW
1/2 LSB DNL (B Grade)
40 MHz Multiplying Bandwidth

APPLICATIONS
ATE
Signal Reconstruction
Arbitrary Waveform Generators
Digital Synthesizers
Signal Generators

GENERAL DESCRIPTION

The AD9712B and AD9713B D/A converters are replacements for the AD9712 and AD9713 units which offer improved ac and dc performance. Like their predecessors, they are 12-bit, high speed digital-to-analog converters fabricated in an advanced oxide isolated bipolar process. The AD9712B is an ECL-compatible device featuring update rates of 100 MSPS minimum; the TTL-compatible AD9713B will update at 80 MSPS minimum.

FUNCTIONAL BLOCK DIAGRAM



Designed for direct digital synthesis, waveform reconstruction, and high resolution imaging applications, both devices feature low glitch impulse of 28 pV-s and fast settling times of 27 ns. Both units are characterized for dynamic performance and have excellent harmonic suppression.

The AD9712B and AD9713B are available in 28-pin plastic DIPs and PLCCs, with an operating temperature range of −25°C to +85°C. Both are also available for extended temperature ranges of −55°C to +125°C in cerdips and 28-pin LCC packages.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter (Conditions)	Temp	Test Level	AD9712B/AD9713B AN/AP Min	Typ	Max	AD9712B/AD9713B BN/BP Min	Typ	Max	AD9712B/AD9713B SE/SQ Min	Typ	Max	AD9712B/AD9713B TE/TQ Min	Typ	Max	Units
RESOLUTION				12			12			12			12		Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I	−1.25	1.0	+1.25	−0.75	0.5	+0.75	−1.5	1.0	+1.5	−1.0	0.5	+1.0	LSB
	Full	VI	−2.0		2.0	−1.5		1.5	−2.0		2.0	−1.5		1.5	LSB
Integral Nonlinearity	+25°C	I	−1.5	1.0	1.5	−1.0	0.75	1.0	−1.75	1.5	1.75	−1.25	1.0	1.25	LSB
("Best Fit" Straight Line)	Full	VI	−2.0		2.0	−1.75		1.75	−2.0		2.0	−1.75		1.75	LSB

Parameter (Conditions)	Temp	Test Level	AD9712B AN/AP/BN/BP/SE/SQ/TE/TQ Min	Typ	Max	AD9713B AN/AP/BN/BP/SE/SQ/TE/TQ Min	Typ	Max	Units
INITIAL OFFSET ERROR									
Zero-Scale Offset Error	+25°C	I		0.5	2.5		0.5	2.5	µA
	Full	VI			5.0			5.0	µA
Full-Scale Gain Error[1]	+25°C	I		1.0	5		1.0	5	%
	Full	VI			8			8	%
Offset Drift Coefficient	+25°C	V		0.01			0.01		µA/°C
REFERENCE/CONTROL AMP									
Internal Reference Voltage	+25°C	I	−1.14	−1.18	−1.22	−1.14	−1.18	−1.22	V
	Full	VI	−1.12		−1.24	−1.12		−1.24	V
Internal Reference Voltage Drift	Full	V		50			50		ppm/°C
Internal Reference Output Current	Full	IV	−50		+500	−50		+500	µA
Amplifier Input Impedance	+25°C	V		50			50		kΩ
Amplifier Bandwidth	+25°C	V		300			300		kHz
REFERENCE INPUT[2]									
Reference Input Impedance	+25°C	V		3			3		kΩ
Reference Multiplying Bandwidth[3]	+25°C	V		40			40		MHz
DYNAMIC PERFORMANCE									
Full-Scale Output Current[4]	+25°C	V		20.48			20.48		mA
Output Compliance Range	+25°C	IV	−1.2		+2	−1.2		+2	V
Output Resistance	+25°C	IV	2.0	2.5	3.0	2.0	2.5	3.0	kΩ
Output Capacitance	+25°C	V		15			15		pF
Output Update Rate[5]	+25°C	IV	100	110		80	100		MSPS
Output Settling Time (t_{ST})[6]	+25°C	V		27			27		ns
Output Propagation Delay (t_{PD})[7]	+25°C	V		6			7		ns
Glitch Impulse[8]	+25°C	V		28			28		pV-s
Output Rise Time[9]	+25°C	V		2			2		ns
Output Fall Time[9]	+25°C	V		2			2		ns
DIGITAL INPUTS									
Logic "1" Voltage	Full	VI	−1.0	−0.8		2.0			V
Logic "0" Voltage	Full	VI		−1.7	−1.5			0.8	V
Logic "1" Current	Full	VI			20			20	µA
Logic "0" Current	Full	VI			10			600	µA
Input Capacitance	+25°C	V		3			3		pF
Input Setup Time (t_S)[10]	+25°C	IV	0.5	−0.3		0.5	−0.3		ns
	Full	IV	0.8			0.8			ns
Input Hold Time (t_H)[11]	+25°C	IV	1.8	1.2		1.8	1.2		ns
	Full	IV	2.0			2.0			ns
Latch Pulse Width (t_{LPW}) (LOW)	+25°C	IV	2.5	1.7		2.5	1.7		ns
(Transparent)	Full		2.8			2.8			ns
AC LINEARITY[12]									
Spurious-Free Dynamic Range (SFDR)									
1.23 MHz; 10 MSPS; 2 MHz Span	+25°C	V		70			70		dB
5.055 MHz; 20 MSPS; 2 MHz Span	+25°C	V		72			72		dB
10.1 MHz; 50 MSPS; 2 MHz Span	+25°C	V		68			68		dB
16 MHz; 40 MSPS; 10 MHz Span	+25°C	V		68			68		dB

Parameter (Conditions)	Test Temp	Test Level	AD9712B AN/AP/BN/BP/SE/SQ/TE/TQ Min	Typ	Max	AD9713B AN/AP/BN/BP/SE/SQ/TE/TQ Min	Typ	Max	Units
POWER SUPPLY[13]									
Positive Supply Current (+5.0 V)	+25°C	I					6	12	mA
	Full	VI						14	mA
Negative Supply Current (−5.2 V)[14]	+25°C	I		140	178		145	184	mA
	Full	VI			183			188	mA
Nominal Power Dissipation	+25°C	V		728			784		mW
Power Supply Rejection Radio (PSRR)[15]	+25°C	I		30	100		30	100	μA/V

NOTES
[1]Measured as error in ratio of full-scale current to current through R_{SET} (160 μA nominal); ratio is nominally 128.
[2]Full-scale variations among devices are higher when driving REFERENCE INPUT directly.
[3]Frequency at which the gain is flat ±0.5 dB; R_L = 50 Ω; 50% modulation at midscale.
[4]Based on I_{FS} = 128 (V_{REF}/R_{SET}) when using internal amplifier.
[5]Data registered into DAC accurately at this rate; does not imply settling to 12-bit accuracy.
[6]Measured as voltage settling at midscale transition to ±0.024%; R_L = 50 Ω.
[7]Measured as the time between the 50% point of the falling edge of LATCH ENABLE and the point where the output signal has left a 1 LSB error band around its previous value.
[8]Peak glitch impulse is measured as the largest area under a single positive or negative transient.
[9]Measured with R_L = 50 Ω and DAC operating in latched mode.
[10]Data must remain stable for specified time prior to falling edge of LATCH ENABLE signal.
[11]Data must remain stable for specified time after rising edge of LATCH ENABLE signal.
[12]SFDR is defined as the difference in signal energy between the fundamental and worst case spurious frequencies in the output spectrum window, which is centered at the fundamental frequency and covers the indicated span.
[13]Supply voltages should remain stable within ±5% for normal operation.
[14]108 mA typ on Digital $-V_S$, 37 mA typ on Analog $-V_S$.
[15]Measured at ±5% of $+V_S$ (AD9713B only) and $-V_S$ (AD9712B or AD9713B) using external reference.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) (AD9713B Only) . . . . . +6 V
Negative Supply Voltage ($-V_S$) . . . . . −7 V
Analog-to-Digital Ground Voltage Differential . . . . . 0.5 V
Digital Input Voltages (D_1–D_{12}, LATCH ENABLE)
AD9712B . . . . . 0 V to $-V_S$
AD9713B . . . . . −0.5 V to $+V_S$
Internal Reference Output Current . . . . . 500 μA
Control Amplifier Input Voltage Range . . . . . 0 V to −4 V
Control Amplifier Output Current . . . . . ±2.5 mA
Reference Input Voltage Range (V_{REF}) . . . . . 0 V to $-V_S$
Analog Output Current . . . . . 30 mA
Operating Temperature Range
AD9712B/AD9713BAN/AP/BN/BP . . . . . −25°C to +85°C
AD9712B/AD9713BSE/SQ/TE/TQ . . . . . −55°C to +125°C
Maximum Junction Temperature[2]
AD9712B/AD9713BAN/AP/BN/BP . . . . . +150°C
AD9712B/AD9713BSE/SQ/TE/TQ . . . . . +175°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances with parts soldered in place: 28-pin plastic DIP: θ_{JA} = 37°C/W, θ_{JC} = 10°C/W; 28-pin PLCC: θ_{JA} = 44°C/W, θ_{JC} = 14°C/W; Cerdip: θ_{JA} = 32°C/W, θ_{JC} = 10°C/W; LCC: θ_{JA} = 41°C/W, θ_{JC} = 13°C/W. No air flow.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9712BAN	−25°C to +85°C	28-Pin PDIP	N-28
AD9712BBN	−25°C to +85°C	28-Pin PDIP	N-28
AD9712BAP	−25°C to +85°C	28-Pin PLCC	P-28A
AD9712BBP	−25°C to +85°C	28-Pin PLCC	P-28A
AD9712BSQ	−55°C to +125°C	28-Pin Cerdip	Q-28
AD9712BSE	−55°C to +125°C	28-Pin LCC	E-28A
AD9712BTQ	−55°C to +125°C	28-Pin Cerdip	Q-28
AD9712BTE	−55°C to +125°C	28-Pin LCC	E-28A
AD9713BAN	−25°C to +85°C	28-Pin PDIP	N-28
AD9713BBN	−25°C to +85°C	28-Pin PDIP	N-28
AD9713BAP	−25°C to +85°C	28-Pin PLCC	P-28A
AD9713BBP	−25°C to +85°C	28-Pin PLCC	P-28A
AD9713BSQ	−55°C to +125°C	28-Pin Cerdip	Q-28
AD9713BSE	−55°C to +125°C	28-Pin LCC	E-28A
AD9713BTQ	−55°C to +125°C	28-Pin Cerdip	Q-28
AD9713BTE	−55°C to +125°C	28-Pin LCC	E-28A

*For outline information see Package Information section.

EXPLANATION OF TEST LEVELS

Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

PIN DESCRIPTIONS

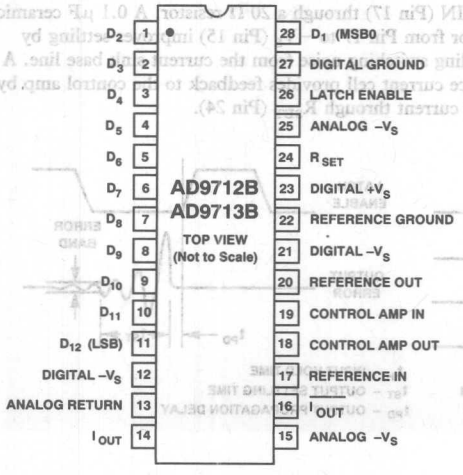
Pin #	Name	Function
1–10	D_2–D_{11}	Ten bits of twelve-bit digital input word.
11	D_{12} (LSB)	Least Significant Bit (LSB) of digital input word.
12	DIGITAL $-V_S$	One of two negative digital supply pins; nominally −5.2 V.
13	ANALOG RETURN	Analog ground return. This point and the reference side of the DAC load resistors should be connected to the same potential (nominally ground).
14	I_{OUT}	Analog current output; full-scale output occurs with digital inputs at all "1."
15	ANALOG $-V_S$	One of two negative analog supply pins; nominally −5.2 V.
16	$\overline{I_{OUT}}$	Complementary analog current output; zero scale output occurs with digital inputs at all "1."
17	REFERENCE IN	Normally connected to CONTROL AMP OUT (Pin 18). Direct line to DAC current source network. Voltage changes at this point have a direct effect on the full-scale output value of unit. Full-scale current output = 128 (Reference voltage/R_{SET}) when using internal amplifier.
18	CONTROL AMP OUT	Normally connected to REFERENCE INPUT (Pin 17). Output of internal control amplifier, which provides a temperature-compensated drive level to the current switch network.
19	CONTROL AMP IN	Normally connected to REFERENCE OUT (Pin 20) if not connected to external reference.
20	REFERENCE OUT	Normally connected to CONTROL AMP IN (Pin 19). Internal voltage reference, nominally −1.18 V.
21	DIGITAL $-V_S$	One of two negative digital supply pins; nominally −5.2 V.
22	REFERENCE GROUND	Ground return for the internal voltage reference and amplifier.
23	DIGITAL $+V_S$	Positive digital supply pin, used only on the AD9713B; nominally +5 V. No connection to this pin on AD9712B.
24	R_{SET}	Connection for external resistance reference. Full-scale current out = 128 (Reference voltage/R_{SET}) when using internal amplifier. Nominally 7.5 kΩ.
25	ANALOG $-V_S$	One of two negative analog supply pins; nominally −5.2 V.
26	LATCH ENABLE	Transparent latch control line. Register is transparent when LATCH ENABLE is LOW.
27	DIGITAL GROUND	Digital ground return.
28	D_1 (MSB)	Most Significant Bit (MSB) of digital input word.

Input Coding vs. Current Output

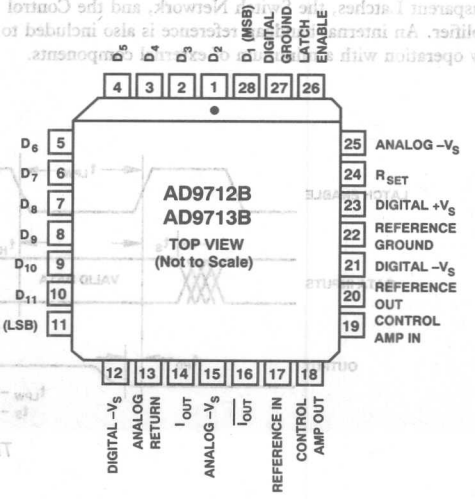
Input Code D_1–D_{12}	I_{OUT} (mA)	$\overline{I_{OUT}}$ (mA)
1111111111	−20.475	0
0000000000	0	−20.475

PIN CONFIGURATIONS

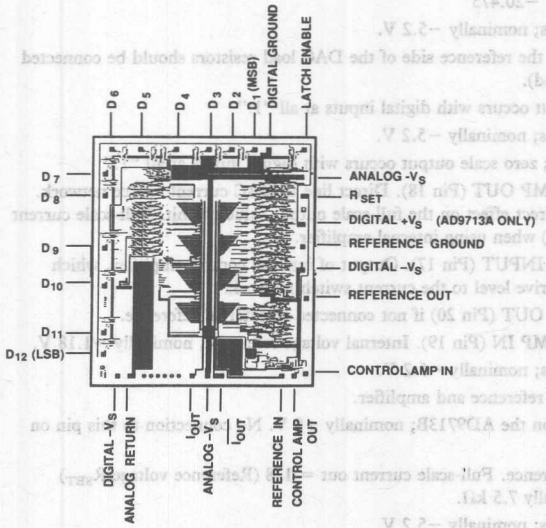
DIP



PLCC/LCC



Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride



THEORY AND APPLICATIONS

The AD9712B and AD9713B high speed digital-to-analog converters utilize Most Significant Bit (MSB) decoding and segmentation techniques to reduce glitch impulse and maintain 12-bit linearity without trimming.

As shown in the functional block diagram, the design is based on four main subsections: the Decoder/Driver circuits, the Transparent Latches, the Switch Network, and the Control Amplifier. An internal bandgap reference is also included to allow operation with a minimum of external components.

thresholds. On the AD9713B, a TTL translator is added at each input; with this exception, the AD9712B and AD9713B are identical.

In the Decoder/Driver section, the four MSBs (D_1–D_4) are decoded to 15 "thermometer code" lines. An equalizing delay is included for the eight Least Significant Bits (LSBs) and LATCH ENABLE. This delay minimizes data skew, and data setup and hold times at the latch inputs; this is important when operating the latches in the transparent mode. Without the delay, skew caused by the decoding circuits would degrade glitch impulse.

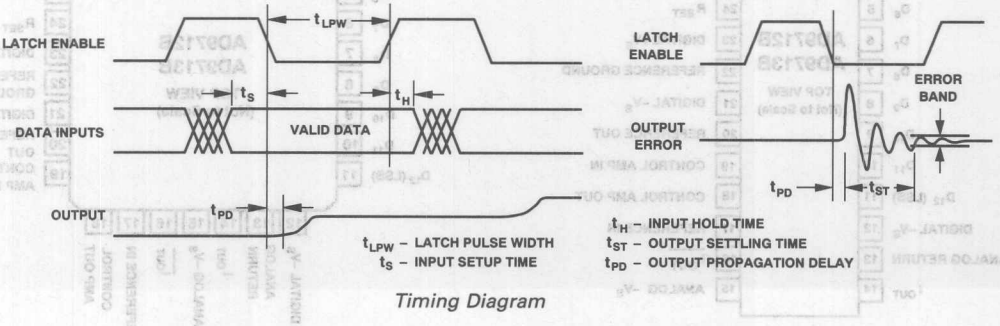
The latches operate in their transparent mode when LATCH ENABLE (Pin 26) is at logic level "0." The latches should be used to synchronize data to the current switches by applying a narrow LATCH ENABLE pulse with proper data setup and hold times as shown in the Timing Diagram. An external latch at each data input, clocked out of phase with the Latch Enable, operates the AD9712B/AD9713B in a master slave (edge-triggered) mode. This is the optimum way to operate the DAC because data is always stable at the DAC input. An external latch eases timing constraints when using the converter.

Although the AD9712B/AD9713B chip is designed to provide isolation from digital inputs to the outputs, some coupling of digital transitions is inevitable, especially with TTL or CMOS inputs applied to the AD9713B. Digital feedthrough can be reduced by forming a low-pass filter using a (200 Ω) series resistor in series with the capacitance of each digital input; this rolls off the slew rate of the digital inputs.

References

As shown in the functional block diagram, the internal band-gap reference, control amplifier, and reference input are pinned out for maximum user flexibility when setting the reference.

When using the internal reference, REFERENCE OUT (Pin 20) should be connected to CONTROL AMP IN (Pin 19). CONTROL AMP OUT (Pin 18) should be connected to REFERENCE IN (Pin 17) through a 20 Ω resistor. A 0.1 μF ceramic capacitor from Pin 17 to $-V_S$ (Pin 15) improves settling by decoupling switching noise from the current sink base line. A reference current cell provides feedback to the control amp by sinking current through R_{SET} (Pin 24).



Timing Diagram

Full-scale output current is determined by CONTROL AMP IN and R_{SET} according to the equation:

$$I_{OUT}\,(FS) = (CONTROL\ AMP\ IN/R_{SET}) \times 128$$

The internal reference is nominally −1.18 V with a tolerance of ±3.5% and typical drift over temperature of 50 ppm/°C. If greater accuracy or better temperature stability is required, an external reference can be utilized. The AD589 reference shown in Figure 1 features ±10 ppm/°C drift over temperatures from 0°C to +70°C.

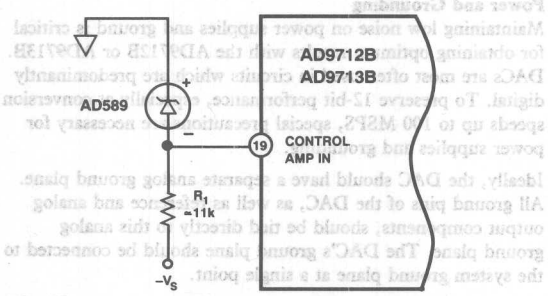


Figure 1. Use of AD589 as External Reference

Two modes of multiplying operation are possible with the AD9712B/AD9713B. Signals with small signal bandwidths up to 300 kHz and input swings of 100 mV, or dc signals from −0.6 V to −1.2 V can be applied to the CONTROL AMP input as shown in Figure 2. Because the control amplifier is internally compensated, the 0.1 μF capacitor at Pin 17 can be reduced to 0.01 μF to maximize the multiplying bandwidth. However, it should be noted that settling time for changes to the digital inputs will be degraded.

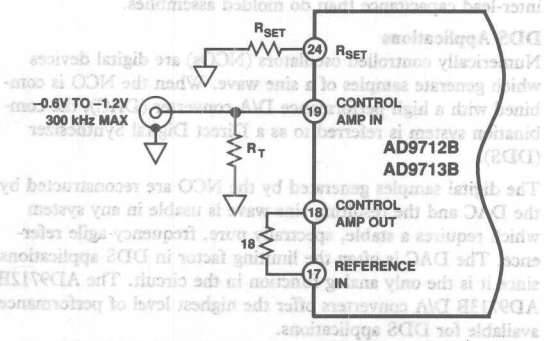


Figure 2. Low Frequency Multiplying Circuit

The REFERENCE IN pin can also be driven directly for wider bandwidth multiplying operation, The analog signal for this mode of operation must have a signal swing in the range of −3.75 V to −4.25 V. This can be implemented by capacitively coupling into REFERENCE IN a signal with a dc bias of −3.75 V to −4.25 V, as shown in Figure 3; or by driving REFERENCE IN with a low impedance op amp whose signal swing is limited to the stated range.

Outputs

As indicated earlier, D_1–D_4 (four MSBs) are decoded and drive 15 discrete current sinks. D5 and D6 are binarily weighted; and D_7–D_{12} are applied to the R-2R network. This segmented architecture reduces frequency domain errors due to glitch impulse.

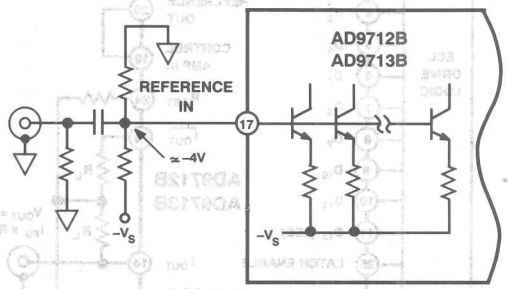
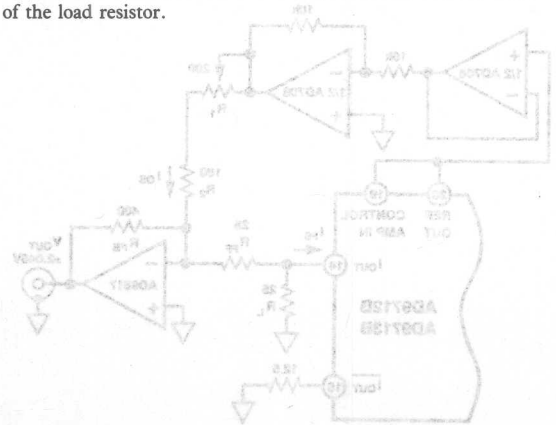


Figure 3. Wideband Multiplying Circuit

The Switch Network provides complementary current outputs I_{OUT} and $\overline{I_{OUT}}$. These current outputs are based on statistical current source matching which provides 12-bit linearity without trim. Current is steered to either I_{OUT} or $\overline{I_{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full-scale output current minus one LSB.

The current output can be converted to a voltage by resistive loading as shown in Figure 4. Both I_{OUT} and $\overline{I_{OUT}}$ should be loaded equally for best overall performance. The voltage which is developed is the product of the output current and the value of the load resistor.



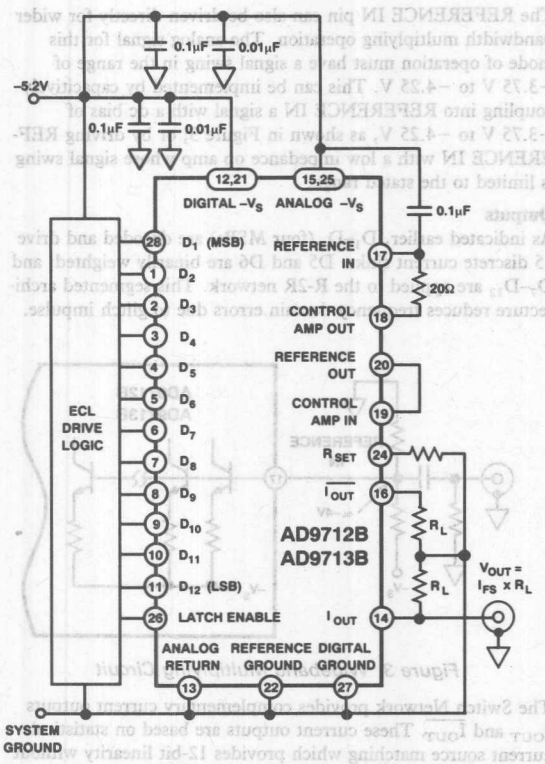


Figure 4. Typical Resistive Load Connection

An operational amplifier can also be used to perform the I to V conversion of the DAC output. Figure 5 shows an example of a circuit which uses the AD9617, a high speed, current feedback amplifier.

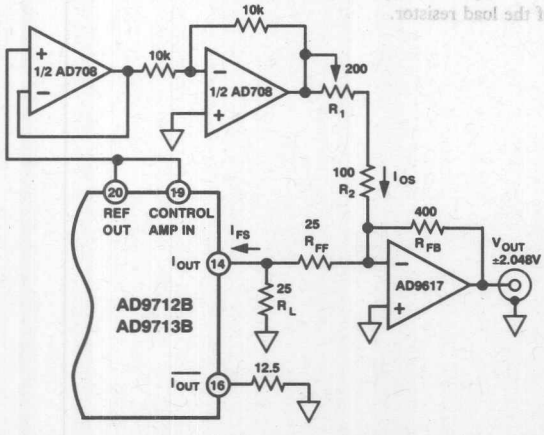


Figure 5. I/V Conversion Using Current Feedback

DAC current across feedback resistor R_{FB} determines the AD9617 output swing. A current divider formed by R_L and R_{FF} limits the current used in the I-to-V conversion, and provides an output voltage swing within the specifications of the AD9617. Current through R_2 provides dc offset at the output of the AD9617. Adjusting the value of R_1 adjusts the value of offset current. This offset current is based on the reference of the AD9712B/AD9713B, to avoid coupling noise into the output signal.

The resistor values in Figure 5 provide a 4.096 V swing, centered at ground, at the output of the AD9617 amplifier.

Power and Grounding

Maintaining low noise on power supplies and ground is critical for obtaining optimum results with the AD9712B or AD9713B. DACs are most often used in circuits which are predominantly digital. To preserve 12-bit performance, especially at conversion speeds up to 100 MSPS, special precautions are necessary for power supplies and grounding.

Ideally, the DAC should have a separate analog ground plane. All ground pins of the DAC, as well as reference and analog output components, should be tied directly to this analog ground plane. The DAC's ground plane should be connected to the system ground plane at a single point.

Ferrite beads such as the Stackpole 57-1392 or Amidon FB-43B-101, along with high frequency, low-inductance decoupling capacitors, should be used for the supply connections to isolate digital switching currents from the DAC supply pins. Separate isolation networks for the digital and analog supply connections will further reduce supply noise coupling to the output.

Molded socket assemblies should be avoided even when prototyping circuits with the AD9712B or AD9713B. When the DAC cannot be directly soldered into the board, individual pin sockets such as AMP #6-330808-0 (knock-out end), or #60330808-3 (open end) should be used. These have much less effect on inter-lead capacitance than do molded assemblies.

DDS Applications

Numerically controlled oscillators (NCOs) are digital devices which generate samples of a sine wave. When the NCO is combined with a high performance D/A converter (DAC), the combination system is referred to as a Direct Digital Synthesizer (DDS).

The digital samples generated by the NCO are reconstructed by the DAC and the resulting sine wave is usable in any system which requires a stable, spectrally pure, frequency-agile reference. The DAC is often the limiting factor in DDS applications, since it is the only analog function in the circuit. The AD9712B/AD9713B D/A converters offer the highest level of performance available for DDS applications.

DC linearity errors of a DAC are the dominant effect in low-frequency applications and can affect both noise and harmonic content in the output waveform. Differential Nonlinearity (DNL) errors determine the quantization error between adjacent codes, while Integral Nonlinearity (INL) is a measure of how closely the overall transfer function of the DAC compares with an ideal device. Together, these errors establish the limits of phase and amplitude accuracy in the output waveform.

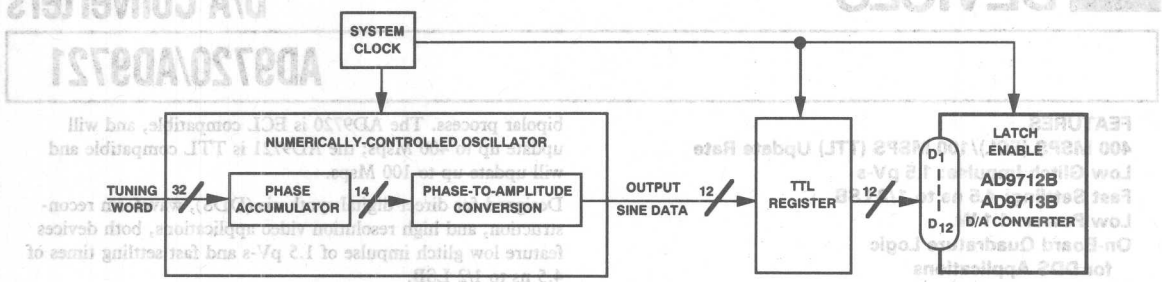


Figure 6. Direct Digital Synthesizer Block Diagram

When the analog frequency (f_A) is exactly f_C/N and N is an even integer, the DDS continually uses a small subset of the available DAC codes. The DNL of the converter is effectively the DNL error of the codes used, and is typically worse than the error measured against all available DAC codes. This increase in DNL is translated into higher harmonic and noise levels at the output.

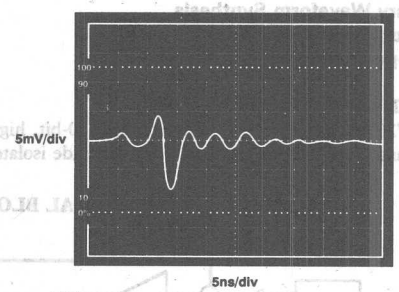


Figure 7. AD9712B/AD9713B Glitch Impulse

Glitch impulse, often considered a figure of merit in DDS applications, is simply the initial transient response of the DAC as it moves between two output levels. This nonlinearity is commonly associated with external data skew, but this effect is minimized by using the on-board registers of the AD9712B/AD9713B converters (see Digital Inputs/Timing section). The majority of the glitch impulse, shown below, is produced as the current in the R-2R ladder network settles, and is fairly constant over the full-scale range of the DAC. The fast transients which form the glitch impulse appear as high-frequency spurs in the output spectrum.

While it is difficult to predict the effects of glitch on the output waveform, slew rate limitations translate directly into harmonics. This makes slew rate the dominant effect in ac linearity of the DAC. Applications in which the ratio of analog frequency (f_A) to clock frequency (f_C) is relatively high will benefit from the high slew rate and low output capacitance of the AD9712B/AD9713B devices.

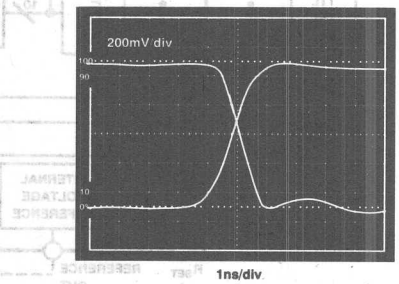


Figure 8. Rise and Fall Characteristics

Another concern in DDS applications is the presence of aliased harmonics in the output spectrum. Aliased harmonics appear as spurs in the output spectrum at frequencies which are determined by:

$$MfA \pm Nf_C$$

where M and N are integers.

The effects of these spurs are most easily observed in applications where f_A is nearly equal to an integer fraction of the clock rate. This condition causes the aliased harmonics to fold near the fundamental output frequency.

10-Bit, 400 MSPS D/A Converters

AD9720/AD9721

FEATURES
400 MSPS (ECL)/100 MSPS (TTL) Update Rate
Low Glitch Impulse: 1.5 pV-s
Fast Settling: 4.5 ns to 1/2 LSB
Low Power: 1.1 W
On-Board Quadrature Logic for DDS Applications
Differential Clock (ECL)

APPLICATIONS
Direct Digital Synthesis
Arbitrary Waveform Synthesis
Waveform Reconstruction
High Speed Imaging

GENERAL DESCRIPTION

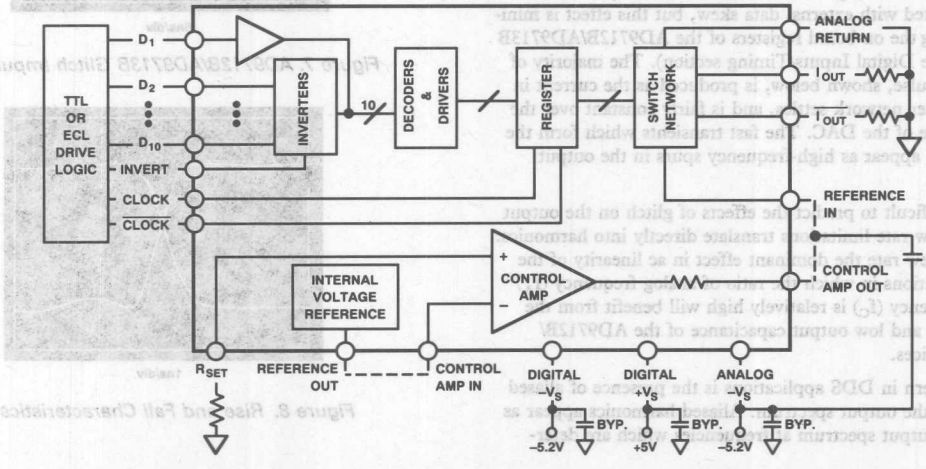
The AD9720 and AD9721 D/A converters are 10-bit, high speed digital-to-analog converters constructed in an oxide isolated bipolar process. The AD9720 is ECL compatible, and will update up to 400 Msps; the AD9721 is TTL compatible and will update up to 100 Msps.

Designed for direct digital synthesis (DDS), waveform reconstruction, and high resolution video applications, both devices feature low glitch impulse of 1.5 pV-s and fast settling times of 4.5 ns to 1/2 LSB.

Both converters are characterized for dynamic performance, and have excellent harmonic suppression and spectral purity in waveform generation applications.

The units are available in 28-pin DIPs, LCCs and SOICs. Industrial temperature range devices are packaged in plastic for operation from −25°C to +25°C; extended temperature range devices for operation from −55°C to +125°C are in hermetic ceramic packages. Contact the factory for information about the availability of MIL-STD-883 devices.

FUNCTIONAL BLOCK DIAGRAM AND CONNECTIONS



SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

($-V_S = -5.2$ V; $+V_S = +5$ V [AD9721 only]; Reference Voltage = -1.25 V; $R_{SET} = 1{,}960\ \Omega$, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9720BN/BR Min	AD9720BN/BR Typ	AD9720BN/BR Max	AD9720TE/TQ Min	AD9720TE/TQ Typ	AD9720TE/TQ Max	AD9721BN/BR Min	AD9721BN/BR Typ	AD9721BN/BR Max	AD9721TE/TQ Min	AD9721TE/TQ Typ	AD9721TE/TQ Max	Units
RESOLUTION				10			10			10			10		Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I		0.25	0.75		0.6	1.0		0.25	0.75		0.6	1.0	LSB
	Full	VI			1.0			1.5			1.0			1.5	LSB
Integral Nonlinearity	+25°C	I		0.5	1.0		0.7	1.5		0.5	1.0		0.7	1.5	LSB
("Best Fit" Straight Line)	Full	VI			1.5			2.0			1.5			2.0	LSB
INITIAL OFFSET ERROR															
Zero-Scale Offset Error	+25°C	I		16	60		16	60		16	60		16	60	µA
	Full	VI		20	75		20	75		20	75		20	75	µA
Full-Scale Gain Error[1]	+25°C	I		2	15		2	15		2	15		2	15	%
	Full	VI			15			15			15			15	%
Offset Drift Coefficient	+25°C	V		0.04			0.04			0.04			0.04		µA/°C
REFERENCE/CONTROL AMP															
Internal Reference Voltage	+25°C	I	−1.15	−1.25	−1.35	−1.15	−1.25	−1.35	−1.15	−1.25	−1.35	−1.15	−1.25	−1.35	V
	Full	VI	−1.15		−1.35	−1.15		−1.35	−1.15		−1.35	−1.15		−1.35	V
Internal Reference Voltage Drift	Full	V		100			100			100			100		µV/°C
Internal Reference Output Current	Full	IV	−50		+500	−50		+500	−50		+500	−50		+500	µA
Amplifier Input Impedance	+25°C	V		50			50			50			50		kΩ
Amplifier Bandwidth	+25°C	V		1			1			1			1		MHz
REFERENCE INPUT[2]															
Reference Input Impedance	+25°C	V		4.6			4.6			4.6			4.6		kΩ
Reference Multiplying Bandwidth[3]	+25°C	V		75			75			75			75		MHz
OUTPUT PERFORMANCE															
Full-Scale Output Current[2, 4]	+25°C	V		20.48			20.48			20.48			20.48		mA
Output Compliance Range	+25°C	IV	−1.5		+3	−1.5		+3	−1.5		+3	−1.5		+3	V
Output Resistance	+25°C	V		210			210			210			210		Ω
Output Capacitance	+25°C	V		6			6			6			6		pF
Output Update Rate	+25°C	V		400			400			100			100		Msps
Voltage Settling Time (1/2 LSB)[5]	+25°C	V		4.5			4.5			4.5			4.5		ns
Propagation Delay (t_{PD})[6]	+25°C	V		4.0			4.0			4.5			4.5		ns
Glitch Impulse[7]	+25°C	V		1.5			1.5			1.5			1.5		pV-s
Output Slew Rate[8]	+25°C	V		1,000			1,000			1,000			1,000		V/µs
Output Rise Time[8]	+25°C	V		675			675			675			675		ps
Output Fall Time[8]	+25°C	V		470			470			470			470		ps
DIGITAL INPUTS															
Logic "1" Voltage	Full	VI	−1.0			−0.9			2.0			2.0			V
Logic "0" Voltage	Full	VI			−1.5			−1.6			0.8			0.8	V
Logic "1" Current	Full	VI			50			50			400			400	µA
Logic "0" Current	Full	VI			2			2			700			700	µA
Input Capacitance	+25°C	V		3			3			3			3		pF
Input Setup Time (t_S)[9]	+25°C	IV	1.0	0.4		1.0	0.4		1.0	0.5		1.0	0.5		ns
	Full	IV	1.2			1.2			1.2			1.2			ns
Input Hold Time (t_H)[10]	+25°C	IV	1.6	1.2		1.6	1.2		2.0	1.25		2.0	1.25		ns
	Full	IV	2.8			2.8			2.3			2.3			ns
Clock Pulse Width (Low)	+25°C	IV	1.1	0.85		1.1	0.85		1.0	0.85		1.0	0.85		ns
Clock Pulse Width (High)	+25°C	IV	1.4	0.85		1.4	0.85		1.1	0.85		1.1	0.85		ns
DYNAMIC PERFORMANCE															
Spurious-Free Dynamic Range (SFDR)[11]															
2.02 MHz; 100 Msps; 2 MHz Span	+25°C	V		75			75			75			75		dBc
25.01 MHz; 100 Msps; 2 MHz Span	+25°C	V		66			66			66			66		dBc
10.02 MHz; 250 Msps; 5 MHz Span	+25°C	V		70			70			N/A			N/A		dBc
62.54 MHz; 250 Msps; 5 MHz Span	+25°C	V		55			55			N/A			N/A		dBc
70 MHz; 220 Msps; 10 MHz Span	+25°C	V		70			70			N/A			N/A		dBc

3

Negative Supply Current (−5.2 V)[13]	+25°C	I	210	280	210	280	210	270	210	270	mA
	Full	VI		290		290		300		300	mA
Positive Supply Current (+5.0 V)	+25°C	I	N/A		N/A		14	30	14	30	mA
	Full	VI	N/A		N/A			30		30	mA
Nominal Power Dissipation	+25°C	V	1.1		1.1		1.2		1.2		W
Power Supply Rejection Ratio (PSRR)[14]	+25°C	V	50		50		50		50		μA/V

NOTES
[1]Measured as error in ratio of full-scale current to current through R_{SET} (640 μA nominal); ratio is nominally 32. DAC load is virtual ground.
[2]Full-scale current variations among devices are higher when driving REFERENCE IN directly.
[3]Frequency at which a 3 dB change in output of DAC is observed; R_L = 50 Ω; 100 mV modulation at midscale.
[4]Based on I_{FS} = 32 (CONTROL AMP IN/R_{SET}) when using internal control amplifier. DAC load is virtual ground.
[5]Measured as voltage settling at midscale transition to ±0.1%; R_L = 50 Ω.
[6]Measured from 50% point of rising edge of CLOCK signal to 1/2 LSB change in output signal.
[7]Peak glitch impulse is measured as the largest area under a single positive or negative transient.
[8]Measured with R_L = 50 Ω and DAC operating in latched mode.
[9]Data must remain stable for specified time prior to rising edge of CLOCK.
[10]Data must remain stable for specified time after rising edge of CLOCK.
[11]SFDR is defined as the difference in signal energy between the fundamental and worst case spurious frequencies in the output spectrum window, which is centered at the fundamental frequency and covers the indicated span.
[12]Supply voltages should remain stable within ±5% for normal operation.
[13]190 mA typ on Digital $-V_S$, 30 mA typ on Analog $-V_S$.
[14]Measured at ±5% of $+V_S$ (AD9721 only) and $-V_S$ (AD9720 or AD9721) using external reference.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) (AD9721 Only) . . . . . +6 V
Negative Supply Voltage ($-V_S$) (AD9720 and AD9721) . −7 V
Digital Input Voltages (D_1–D_{10}, CLOCK, $\overline{\text{CLOCK}}$)
AD9720 . . . . . 0 V to $-V_S$
AD9721 . . . . . −0.5 V to $+V_S$
Internal Reference Output Current . . . . . 500 μA
Control Amplifier Input Voltage Range . . . . . 0 V to −4 V
Control Amplifier Output Current . . . . . ±2.5 mA
Reference Input Voltage Range (V_{REF}) . . . . . 0 V to $-V_S$
Analog Output Current . . . . . 30 mA
Operating Temperature Range
AD9720/AD9721BN/BR . . . . . −25°C to +85°C
AD9720/AD9721TE/TQ . . . . . −55°C to +125°C
Maximum Junction Temperature[2]
AD9720/AD9721BN/BR . . . . . +150°C
AD9720/AD9721TE/TQ . . . . . +175°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: 28-pin plastic DIP: θ_{JA} = 37°C/W, θ_{JC} = 10°C/W; 28-pin LCC: θ_{JA} = 41°C/W, θ_{JC} = 13°C/W; 28-pin SOIC: θ_{JA} = 46°C/W, θ_{JC} = 10°C/W; Cerdip: θ_{JA} = 35°C/W, θ_{JC} = 10°C/W. Soldered to board; no air flow.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9720BN	−25°C to +85°C	28-Pin PDIP	N-28
AD9720BR	−25°C to +85°C	28-Pin SOIC	R-28
AD9720TE	−55°C to +125°C	28-Pin LCC	E-28A
AD9720TQ	−55°C to +125°C	28-Pin Cerdip	Q-28
AD9721BN	−25°C to +85°C	28-Pin PDIP	N-28
AD9721BR	−25°C to +85°C	28-Pin SOIC	R-28
AD9721TE	−55°C to +125°C	28-Pin LCC	E-28A
AD9721TQ	−55°C to +125°C	28-Pin Cerdip	Q-28

For outline information see Package Information section.

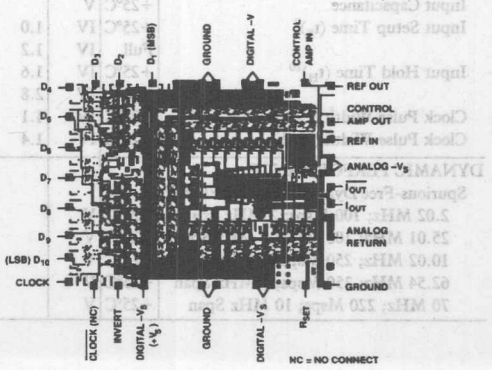
EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

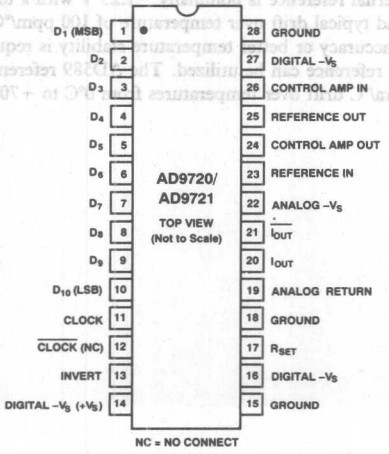
DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions . . . . . 199 × 165 × 15 (±2) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Aluminum
Backing . . . . . None
Substrate Potential . . . . . $-V_S$
Passivation . . . . . Nitride

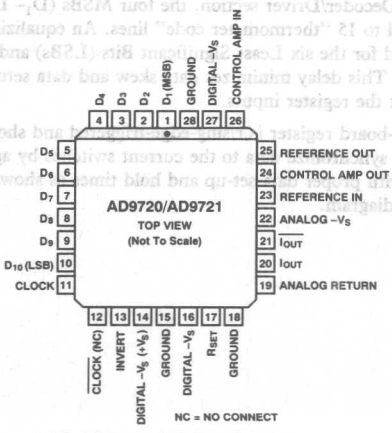


PIN DESCRIPTIONS

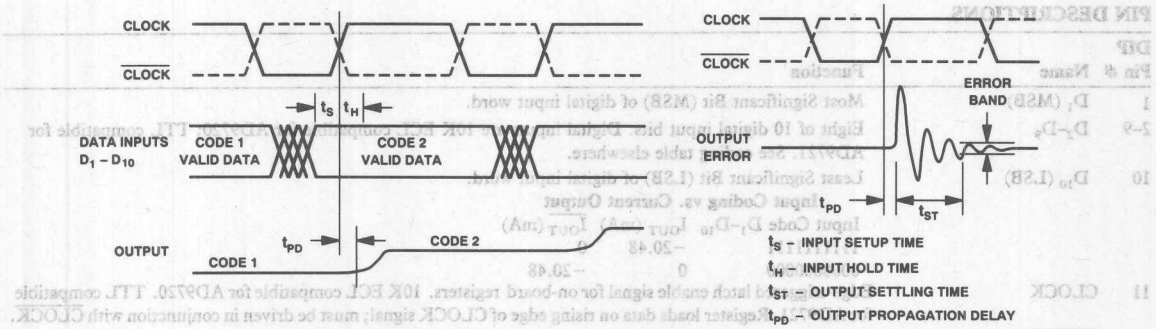
DIP Pin #	Name	Function
1	D_1 (MSB)	Most Significant Bit (MSB) of digital input word.
2–9	D_2–D_9	Eight of 10 digital input bits. Digital inputs are 10K ECL compatible for AD9720; TTL compatible for AD9721. See coding table elsewhere.
10	D_{10} (LSB)	Least Significant Bit (LSB) of digital input word.
		Input Coding vs. Current Output
		Input Code D_1–D_{10} I_{OUT} (mA) $\overline{I_{OUT}}$ (mA)
		1111111111 −20.48 0
		0000000000 0 −20.48
11	CLOCK	Edge-triggered latch enable signal for on-board registers. 10K ECL compatible for AD9720. TTL compatible for AD9721. Register loads data on rising edge of CLOCK signal; must be driven in conjunction with $\overline{\text{CLOCK}}$.
12	$\overline{\text{CLOCK}}$/NC	Complementary edge-triggered latch enable signal for on-board registers. 10K ECL compatible for AD9720; not connected (NC) for AD9721.
13	INVERT	Normally connected to logic LOW; inverters are transparent in this mode. Logic High inverts the 9 LSBs (D_2–D_{10}) when the MSB is LOW. No internal pull-down resistor.
14	DIGITAL $-V_S/+V_S$	One of three digital supply pins; nominally −5.2 V for AD9720; +5 V for AD9721.
15	GROUND	Converter ground return.
16	DIGITAL $-V_S$	One of three negative digital supply pins; nominally −5.2 V.
17	R_{SET}	Connection for external resistance reference; nominally 1,960 Ω. Full-scale current out = 32 × (CONTROL AMP IN/R_{SET}) when using internal amplifier. DAC load is virtual ground.
18	GROUND	Converter ground return.
19	ANALOG RETURN	Analog current return. This point and the reference side of the DAC load resistors should be connected to the same potential (nominally ground).
20	I_{OUT}	Analog current output; full-scale output occurs with digital inputs at all "1." With external load resistor, output voltage = $I_{OUT} \times (R_{LOAD} \parallel R_{INTERNAL})$. $R_{INTERNAL}$ is nominally 210 Ω.
21	$\overline{I_{OUT}}$	Complementary analog current output; zero-scale output occurs with digital inputs at all "1."
22	ANALOG $-V_S$	Negative analog supply; nominally −5.2 V.
23	REFERENCE IN	Normally connected to CONTROL AMP OUT (Pin 24). Direct line to DAC current source network. Voltage changes (noise) at this point have a direct effect on the full-scale output current of DAC. Full-scale current output = 32 × (CONTROL AMP IN/R_{SET}) when using internal amplifier. DAC load is virtual ground.
24	CONTROL AMP OUT	Normally connected to REFERENCE INPUT (Pin 23). Output of internal control amplifier, which provides a reference for the current switch network.
25	REFERENCE OUT	Normally connected to CONTROL AMP IN (Pin 26). Internal voltage reference, nominally −1.25 V.
26	CONTROL AMP IN	Normally connected to REFERENCE OUT (Pin 25) if not connected to external reference.
27	DIGITAL $-V_S$	One of three negative digital supply pins; nominally −5.2 V.
28	GROUND	Converter ground return.



Pinouts (SOIC Pin Numbering is Same as DIP)



LCC AD9720 (AD9721) Pinouts



AD9720/AD9721 Timing Diagram

THEORY AND APPLICATIONS

The AD9720/AD9721 high speed digital-to-analog converters utilize Most Significant Bit (MSB) decoding and segmentation techniques to reduce glitch impulse and maintain 10-bit linearity without trimming.

As shown in the functional block diagram, the design is based on four main subsections: the Decoder/Driver circuits, the Edge Triggered Data Register, the Switch Network, and the Control Amplifier. An internal bandgap reference is also included to allow operation with a minimum of external components. The block labeled "Inverters" is transparent in normal operation, but can be used to minimize the external components requirements in DDS applications using the AD9950, a 300 Msps phase accumulator (see AD9950 data sheet).

Digital Inputs/Timing

The AD9720 employs single-ended ECL-compatible inputs for data inputs D_1–D_{10} and the differential clock signals CLOCK and $\overline{\text{CLOCK}}$. The internal ECL midpoint reference is designed to match 10K ECL device thresholds. On the AD9721, a TTL translator is added at each input and the clock becomes single ended; with these exceptions, the AD9720 and AD9721 are identical. (NOTE: Pin 14 is $+V_S$ on AD9721; $-V_S$ on AD9720.)

In the Decoder/Driver section, the four MSBs (D_1– D_4) are decoded to 15 "thermometer code" lines. An equalizing delay is included for the six Least Significant Bits (LSBs) and the clock signals. This delay minimizes data skew and data setup and hold times at the register inputs.

The on-board register is rising-edge-triggered and should be used to synchronize data to the current switches by applying a pulse with proper data set-up and hold times as shown in the timing diagram.

Although the AD9720/AD9721 chip is designed to provide isolation from digital inputs to the outputs, some coupling of digital transitions is inevitable, especially with TTL or CMOS inputs applied to the AD9721. Digital feedthrough can be reduced by forming a low-pass filter using a resistor in series with the capacitance of each digital input; this rolls off the slew rate of the digital inputs.

References

As shown in the functional block diagram, the internal band-gap reference, control amplifier, and reference input are pinned out for maximum user flexibility when setting the reference.

When using the internal reference, REFERENCE OUT (Pin 25) should be connected to CONTROL AMP IN (Pin 26). CONTROL AMP OUT (Pin 24) should be connected to REFERENCE IN (Pin 23). A 0.1 μF ceramic capacitor from Pin 23 to ANALOG $-V_S$ (Pin 22) improves settling by decoupling switching noise from the current sink base line. A reference current cell provides feedback to the control amp by sinking current through R_{SET} (Pin 17).

Full-scale output current is determined by CONTROL AMP IN and R_{SET} according to the equation:

$$I_{OUT}\,(FS) = (CONTROL\ AMP\ IN/R_{SET}) \times 32$$

The internal reference is nominally −1.25 V with a tolerance of ±8% and typical drift over temperature of 100 ppm/°C. If greater accuracy or better temperature stability is required, an external reference can be utilized. The AD589 reference features ±10 ppm/°C drift over temperatures from 0°C to +70°C.

Two modes of multiplying operation are possible with the AD9720/9721. Signals with bandwidths up to 1 MHz and input swings from −0.6 V to −1.2 V can be applied to the CONTROL AMP input as shown in Figure 1. Because the control amplifier is internally compensated, the 0.1 μF capacitor discussed above can be reduced to maximize the multiplying bandwidth. However, it should be noted that settling time for changes to the digital inputs will be degraded.

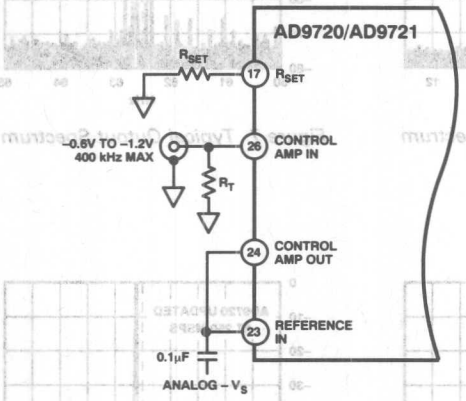


Figure 1. Low Frequency Multiplying Circuit

The REFERENCE IN pin can also be driven directly for wider bandwidth multiplying operation. The analog signal for this mode of operation must have a signal swing in the range of −3.3 V to −4.25 V. This can be implemented by capacitively coupling into REFERENCE IN a signal with a dc bias of −3.3 V (I_{OUT} ~ 22.5 mA) to −4.25 V (I_{OUT} ~ 3 mA), as shown in Figure 2, or by driving REFERENCE IN with a low impedance op amp whose signal swing is limited to the stated range.

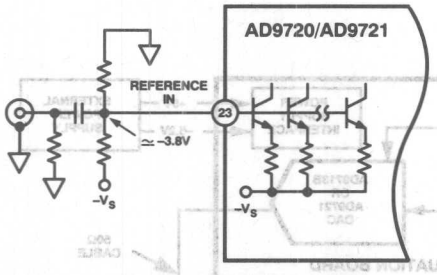


Figure 2. Wideband Multiplying Circuit

Outputs

The Switch Network provides complementary current outputs I_{OUT} and $\overline{I_{OUT}}$. The design of the AD9720/AD9721 is based on statistical current source matching which provides 10-bit linearity without trim. Current is steered to either I_{OUT} or $\overline{I_{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full-scale output current minus one LSB.

The current output can be converted to a voltage by resistive loading as shown in the block diagram. Both I_{OUT} and $\overline{I_{OUT}}$ should be loaded equally for best overall performance. The voltage which is developed is the product of the output current and the value of the load resistor.

An operational amplifier can also be used to perform the I to V conversion of the DAC output. Figure 3 shows an example of a circuit which uses the AD9617, a high speed, current feedback amplifier. The resistor values in Figure 3 provide a 4.096 V swing, centered at ground, at the output of the AD9617 amplifier.

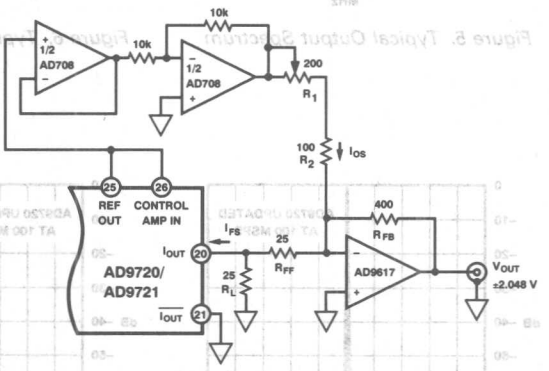


Figure 3. I/V Conversion Using Current Feedback Amp

DDS Applications

The performance characteristics of the AD9720/AD9721 make it ideally suited for direct digital synthesis (DDS) and other waveform generation applications. Since the aliased distortion of the DAC collects around the fundamental when generating frequencies which are nearly integer fractions of the clock rate, these are often considered worst case conditions.

Please contact the factory for information concerning the availability of an evaluation board or for additional characterization data.

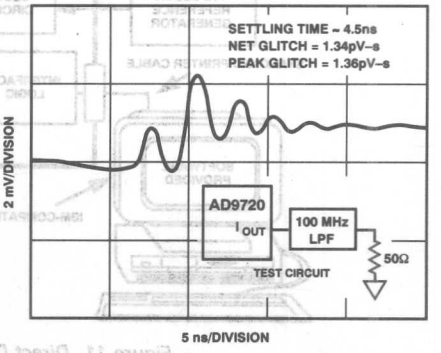


Figure 4. AD9720 Glitch Impulse

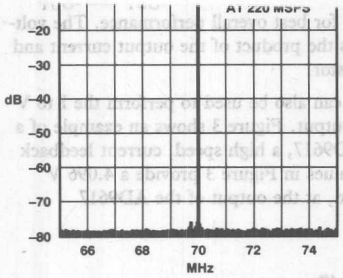


Figure 5. Typical Output Spectrum

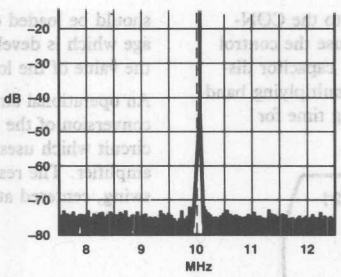


Figure 6. Typical Output Spectrum

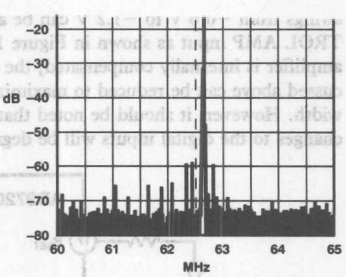


Figure 7. Typical Output Spectrum

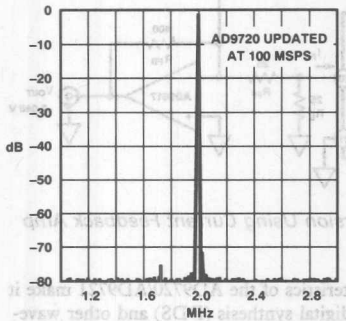


Figure 8. Typical Output Spectrum

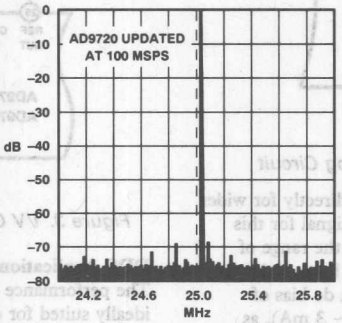


Figure 9. Typical Output Spectrum

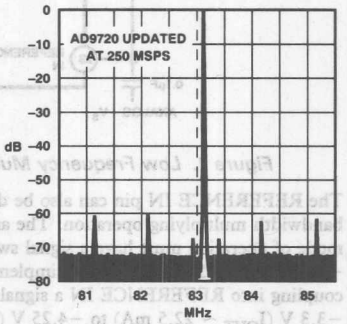


Figure 10. Typical Output Spectrum

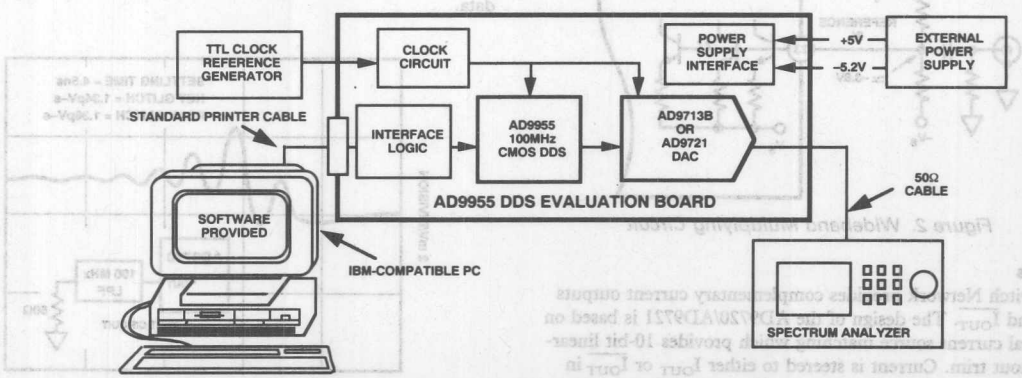


Figure 11. Direct Digital Synthesis System Diagram

FEATURES

5ns Settling Time
100MSPS Update Rate
20mA Output Current
ECL-Compatible
40MHz Multiplying Mode

APPLICATIONS

Raster Scan & Vector Graphic Displays
High Speed Waveform Generation
Digital VCOs
Ultra-Fast Digital Attenuators

GENERAL DESCRIPTION

The Analog Devices AD9768SD D/A converter is a monolithic current-output converter which can accept 8 bits of ECL-level digital input voltages and convert them into analog signals at update rates as high as 100MSPS. In addition to its use as a standard D/A converter, it can also be utilized as a two-quadrant multiplying D/A at multiplying bandwidths as high as 40MHz.

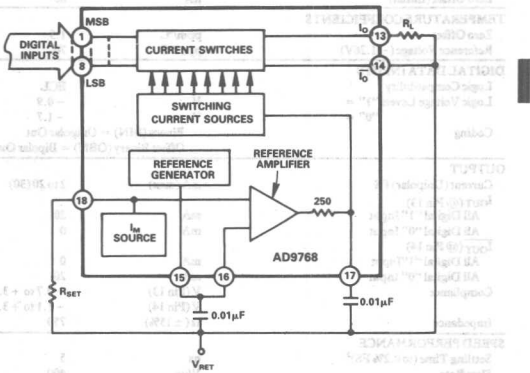
An inherently low glitch design is used, and the complementary current outputs are suitable for driving transmission lines directly. Nominal full-scale output is 20mA, which corresponds to a 1-volt drop across a 50Ω load, or ±1 volt across 100Ω returned to +1 volt. The actual output current is determined by the on-chip reference voltage ($V_{REF} \approx -1.26V$) and an external current setting resistor, R_{SET}.

Full-scale output current I_{OUT} with digital "1" at all inputs is calculated with the equation:

$$I_{OUT} = 4 \times \frac{V_{RET} - V_{REF}}{R_{SET}}$$

The setting resistor R_{SET} and the output load resistor should both have low temperature coefficients. A complementary $\overline{I_{OUT}}$ is also provided.

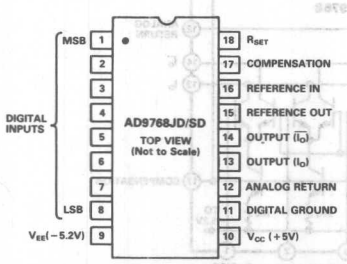
FUNCTIONAL BLOCK DIAGRAM



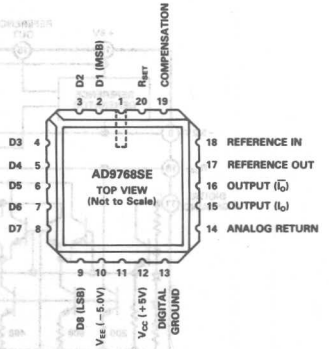
The reference voltage source is a modified bandgap type and is nominally −1.26 volts. This reference supply requires no external regulation. To reduce the possibility of noise generation and/or instability, pin 15 (REFERENCE OUT) can be decoupled using a high-quality ceramic chip capacitor. Stabilization of the internal loop amplifier is by a single capacitor connected from pin 17 (COMPENSATION) to ground. The minimum value for this capacitor is 3900pF, although a 0.01μF ceramic chip capacitor is recommended.

The incredible speed characteristics of the AD9768SD D/A converter make it attractive for a wide range of high speed applications. The ability of the unit to operate as a two-quadrant multiplying D/A converter adds another dimension to its usefulness and makes the AD9768SD a truly versatile device.

AD9768JD/SD PIN CONNECTIONS



AD9768SE PIN CONNECTIONS



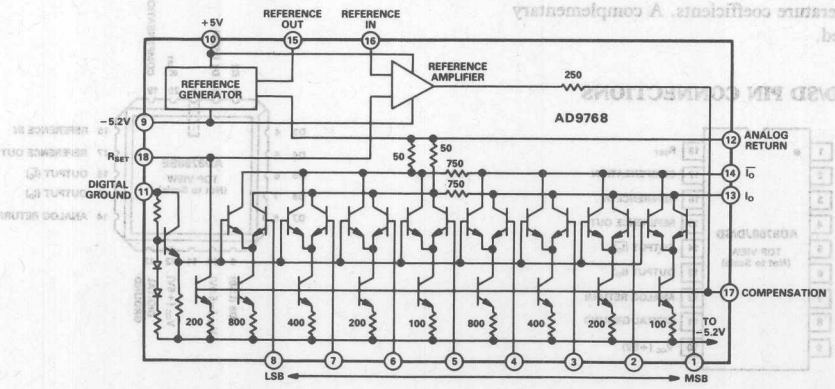
This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9768 – SPECIFICATIONS (typical @ +25°C under following conditions unless otherwise noted; nominal digital input levels; nominal power supplies; $R_L = 50\Omega$; $R_{SET} = 220\Omega$; $V_{REF} = 0V$)

Parameter	Unit	AD9768SJD/SD/SE
RESOLUTION (FS = FULL SCALE)	Bits	8
LSB WEIGHT (CURRENT)	μA	78
ACCURACY[1]		
Differential Nonlinearity	± % FS	0.2
Integral Nonlinearity	± % FS	0.2
Monotonicity		Guaranteed
Zero Offset (Initial)	μA	60
TEMPERATURE COEFFICIENTS		
Zero Offset	ppm/°C	1.5
Reference Voltage (−1.26V)	ppm/°C	70
DIGITAL DATA INPUTS		
Logic Compatibility		ECL
Logic Voltage Levels "1" =	V	−0.9
"0" =	V	−1.7
Coding		Binary (BIN) = Unipolar Out Offset Binary (OBN) = Bipolar Out
OUTPUT		
Current (Unipolar) FS	mA (max)	2 to 20 (30)
I_{OUT} (@ Pin 13)		
All Digital "1" Input	mA	20
All Digital "0" Input	mA	0
$\overline{I_{OUT}}$ (@ Pin 14)		
All Digital "1" Input	mA	0
All Digital "0" Input	mA	20
Compliance	V (Pin 13)	−0.7 to +3.0
	V (Pin 14)	−1.1 to +3.0
Impedance	Ω (±15%)	750
SPEED PERFORMANCE		
Settling Time (to 0.2% FS)[2]	ns	5
Slew Rate	V/μs	400
Update Rate	MSPS	100
Rise Time	ns	1.8
Glitch Energy	pV-sec	200
REFERENCE		
Internal, Monolithic[3]	V	−1.26
External, Variable[4]		
Voltage-Multiplying Mode	V (max)	0 to −1.1 (−2)
Current-Multiplying Mode	mA (max)	0 to −5 (−7.5)
VOLTAGE-MULTIPLYING MODE[4] (See Figure 2)		
V_M Range (at Pin 16)	V	±0.5
V_M Center	V	−0.6
Resistance (at Pin 16)	kΩ	800
Transfer Function –		Measured at Pin 13; Digital "0" Applied to Bits 1-8: $-0.1\ V_M$ Input = 0mA I_{OUT} $-1.1\ V_M$ Input = 0mA I_{OUT} Measured at Pin 13; Digital "1" Applied to Bits 1-8: $-0.1\ V_M$ Input = 1mA I_{OUT} $-1.1\ V_M$ Input = 20mA I_{OUT}
Large Signal Bandwidth (−3dB Point)	kHz	250

Parameter	Unit	AD9768SJD/SD/SE
CURRENT-MULTIPLYING MODE (See Figure 4)		
I_M Range (at Pins 17 & 18)	mA	0 to 5
Resistance (at Pin 18)	Ω	160
Transfer Function –		Measured at Pin 13; Digital "0" Applied to Bits 1-8: 1mA I_M Input = 0mA I_{OUT} 5mA I_M Input = 0mA I_{OUT} Measured at Pin 13; Digital "1" Applied to Bits 1-8: 1mA I_M Input = 4mA I_{OUT} 5mA I_M Input = 20mA I_{OUT}
Large Signal Bandwidth (−3dB Point)	MHz	40
POWER REQUIREMENTS		
−5.2V ±0.25	mA (max)	66 (70)
+5.0V ±0.25	mA (max)	14 (15)
Power Dissipation	mW (max)	410 (430)
Power Supply Sensitivity[5]	%/%	0.07
TEMPERATURE RANGES[6]		
Operating		
AD9768JD	°C	0 to +70
AD9768SD/SE	°C	−55 to +125
Storage	°C	−55 to +150
THERMAL RESISTANCE[7]		
Junction to Air, θ_{JA} (Free Air)	°C/W	90
Junction to Case, θ_{JA}	°C/W	20
PACKAGE OPTION[8]		
Ceramic (D-18)		AD9768JD AD9768SD
LCC (E-20A)		AD9768SE

NOTES
[1]Relative to FS, including linearity (within voltage compliance limits).
[2]Worst case settling time; includes FS and Most Significant Bit (MSB) transitions.
[3]Applies when operating AD9768 as standard D/A.
[4]Based on $R_L = 50$ ohms; $R_{SET} = 220$ ohms; $V_{REF} = 0V$.
[5]1% change in either power supply voltage causes 0.07% change in analog output.
[6]Case temperature.
[7]Maximum junction temperature 125°C.
[8]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier. For outline information see Package Information section.
Specifications subject to change without notice.



AD9768SD D/A Schematic

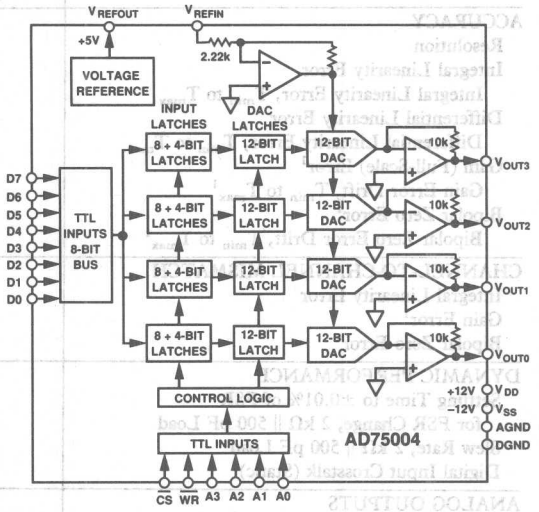
Quad 12-Bit D/A Converter

AD75004

FEATURES

4 Complete 12-Bit D/A Functions
Double-Buffered Latches
Simultaneous Update of All DACs Possible
±5 V Output Range
High Stability Bandgap Reference
Monolithic BiMOS Construction
Guaranteed Monotonic over Temperature
3/4 LSB Linearity Guaranteed over Temperature
4 µs max Settling Time to 0.01%
Operates with ±12 V Supplies
Low Power: 720 mW max Including Reference
TTL/5 V CMOS Compatible Logic Inputs
8-Bit Microprocessor Interface
24-Pin PDIP or 28-Lead PLCC Package

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD75004 contains four complete, voltage output, 12-bit digital-to-analog converters, a high stability bandgap reference, and double-buffered input latches on a single chip. The converters use 12 precision high speed bipolar current steering switches and laser-trimmed thin-film resistor networks to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latches. The design of the input latches allows direct interface to 8-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 50 ns, allowing use with fast microprocessors.

The functional completeness and high performance of the AD75004 results from a combination of advanced switch design, the BiMOS II fabrication process, and proven laser trimming technology. BiMOSII is an epitaxial BiCMOS process optimized for analog and converter functions. The AD75004 is trimmed at the wafer level and is specified to ±1/2 LSB maximum linearity error at 25°C and ±3/4 LSB over the full operating temperature range. The on-chip output amplifiers provide an output range of ±5 V, with 1 LSB equal to 2.44 mV.

The bandgap reference on the chip has low noise, long term stability and temperature drift characteristics comparable to discrete reference diodes. The absolute value of the reference is laser trimmed to +5.00 V with 0.6% maximum error. Its temperature coefficient is also laser trimmed.

Typical full-scale gain TC is 15 ppm/°C. With guaranteed monotonicity over the full temperature range, the AD75004 is well suited for wide temperature range performance.

AD75004—SPECIFICATIONS (T_A = +25°C, ±12.0 V power supplies unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
DIGITAL INPUTS (D0–D7, A0–A3, $\overline{CS}$, $\overline{WR}$)					
Logic Levels (TTL Compatible)					
Input Voltage, Logic "1"	V_{IH}	2.0		5.5	V
Input Voltage, Logic "0"	V_{IL}	0		0.8	V
Input Current, V_{IH} = 5.5 V	I_{IH}			10	μA
Input Current, V_{IL} = 0.8 V	I_{IL}			10	μA
Input Capacitance	C_{IN}			10	pF
ACCURACY					
Resolution				12	Bits
Integral Linearity Error			±1/4	±1/2	LSB
Integral Linearity Error, T_{min} to T_{max}			±1/2	±3/4	LSB
Differential Linearity Error			±1/2	±3/4	LSB
Differential Linearity Error, T_{min} to T_{max}			Guaranteed Monotonic		
Gain (Full-Scale) Error[1]			±2	±10	LSB
Gain Error Drift, T_{min} to T_{max}[1]			±15	±30	ppm/°C
Bipolar Zero Error[1]			±1	±2	LSB
Bipolar Zero Error Drift, T_{min} to T_{max}[1]			±3	±7	ppm/°C
CHANNEL-TO-CHANNEL MISMATCH					
Integral Linearity Error			±1/2	±1	LSB
Gain Error[1]			±1	±4	LSB
Bipolar Zero Error[1]			±1	±2	LSB
DYNAMIC PERFORMANCE					
Settling Time to ±0.01% of FSR for FSR Change, 2 kΩ || 500 pF Load			2	4	μs
Slew Rate, 2 kΩ || 500 pF Load		5			V/μs
Digital Input Crosstalk (Static)[2]				–50	dB
ANALOG OUTPUTS					
Full-Scale Range (FSR)	V_{OUT}		±5		V
Output Current	I_{OUT}	±5			mA
Short Circuit Limit Current				±40	mA
VOLTAGE REFERENCE					
Reference Output Voltage	V_{REFOUT}	4.97	5.00	5.03	V
Temperature Coefficient			±15	±25	ppm/°C
Reference Output Current[3]		3.0	5.0		mA
Reference Input Voltage	V_{REFIN}	4.5	5.0	5.5	V
Reference Input Current @ 5.0 V	I_{REFIN}			3.0	mA
POWER SUPPLY GAIN SENSITIVITY					
$\Delta Gain/\Delta V_{DD}$, V_{DD} = +10.8 to +13.2 V dc[4]			±15	±25	ppm of FSR/%
$\Delta Gain/\Delta V_{SS}$, V_{SS} = −10.8 to −13.2 V dc[4]			±15	±25	ppm of FSR/%
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}, V_{SS}	±10.8	±12	±13.2	V
Supply Currents	I_{DD}, I_{SS}		±25	±30	mA
TEMPERATURE RANGE					
Specification	T_{min}, T_{max}	0		+70	°C
Storage		−65		+150	°C

NOTES

[1]Gain and bipolar zero errors are measured using internal voltage reference and include its errors.

[2]Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} into a 2 kΩ || 500 pF load by means of varying the digital input code.

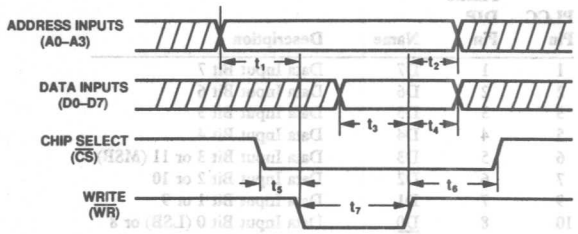
[3]The internal voltage reference is intended to drive on-chip only; buffer it if using it externally.

[4]All minimum and maximum specifications are guaranteed, and specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (T_A = +25°C, ±12.0 V power supplies unless otherwise noted)

Parameter	Symbol	Min	Units
Address Setup Time	t_1	30	ns
Address Hold Time	t_2	10	ns
Data Setup Time	t_3	10	ns
Data Hold Time	t_4	45	ns
Chip Select to Write Setup Time	t_5	0	ns
Write to Chip Select Hold Time	t_6	0	ns
Write Pulse Width	t_7	50	ns



NOTES
[1]Timing measurement reference level is 1.5 V.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS* (T_A = +25°C unless otherwise noted)

	Min	Max	Units	Conditions
V_{DD} to DGND	−0.3	+18	V	
V_{SS} to DGND	−18	+0.3	V	
V_{DD} to V_{SS}	−0.3	+26.4	V	
V_{REFIN} to AGND	−0.3	V_{DD}	V	
Digital Inputs to DGND	−0.3	V_{DD}	V	
AGND to DGND	−0.3	+0.3	V	
Short to AGND on Analog Outputs		Indefinite	sec	
Power Dissipation		1.0	W	$T_A \leq$ 75°C
Specification Temperature Range	0	+70	°C	
Storage Temperature	−65	+150	°C	
Lead Temperature		+300	°C	Soldering, 10 seconds

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE

Control and Address Lines						
$\overline{CS}$	$\overline{WR}$	A3	A2	A1	A0	Operation
1	X	X	X	X	X	No operation
X	1	X	X	X	X	No operation
0	0	0	0	A1*	A0*	8 LSBs → one input latch
0	0	0	1	A1*	A0*	4 MSBs → one input latch
0	0	1	0	A1*	A0*	Update one DAC latch
0	0	1	1	X	X	Update all 4 DAC latches

NOTE
*The A1 and A0 inputs specify the relevant channel.

A1	A0	Channel
0	0	0
0	1	1
1	0	2
1	1	3

CAUTION

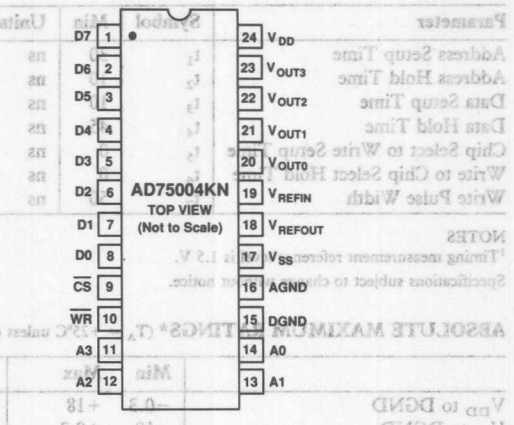
ESD (electrostatic discharge) sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN DESCRIPTIONS

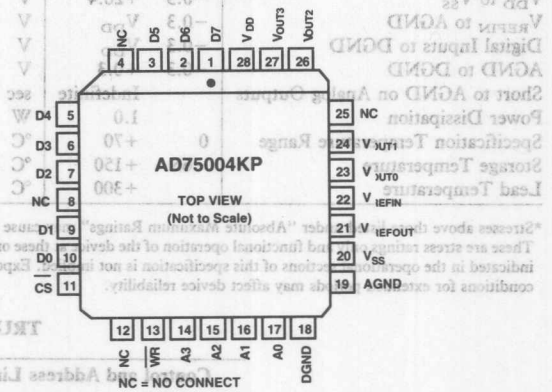
PLCC Pin	Plastic DIP Pin	Name	Description
1	1	D7	Data Input Bit 7
2	2	D6	Data Input Bit 6
3	3	D5	Data Input Bit 5
5	4	D4	Data Input Bit 4
6	5	D3	Data Input Bit 3 or 11 (MSB)
7	6	D2	Data Input Bit 2 or 10
9	7	D1	Data Input Bit 1 or 9
10	8	D0	Data Input Bit 0 (LSB) or 8
11	9	$\overline{CS}$	Chip Select Input; Active Low
13	10	$\overline{WR}$	Write Input; Active Low
14	11	A3	Address Input Bit 3 (MSB)
15	12	A2	Address Input Bit 2
16	13	A1	Address Input Bit 1
17	14	A0	Address Input Bit 0 (LSB)
18	15	DGND	Digital Ground
19	16	AGND	Analog Ground
20	17	V_{SS}	−12 V Power Supply
21	18	V_{REFOUT}	+5 V Reference Output
22	19	V_{REFIN}	Reference Input
23	20	V_{OUT0}	Analog Output 0
24	21	V_{OUT1}	Analog Output 1
26	22	V_{OUT2}	Analog Output 2
27	23	V_{OUT3}	Analog Output 3
28	24	V_{DD}	+12 V Power Supply
4	–	NC	No Internal Connection
8	–	NC	No Internal Connection
12	–	NC	No Internal Connection
25	–	NC	No Internal Connection

PIN CONFIGURATIONS

24-Pin Plastic DIP



28-Pin PLCC



BINARY CODE TABLE

Twos Complement Value in DAC Latch			Analog Output Voltage
MSB		LSB	
0111	1111	1111	(2047/2048) * V_{REFIN}
0000	0000	0001	(1/2048) * V_{REFIN}
0000	0000	0000	0 V
1111	1111	1111	− (1/2048) * V_{REFIN}
1000	0000	0000	$-V_{REFIN}$

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD75004KN	0°C to +70°C	N-24A
AD75004KP	0°C to +70°C	P-28A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

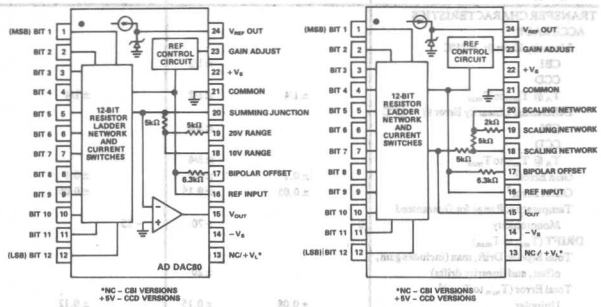
Complete Low Cost 12-Bit D/A Converters

AD DAC80/AD DAC85/AD DAC87

FEATURES

- Single Chip Construction
- On-Board Output Amplifier
- Low Power Dissipation: 300mW
- Monotonicity Guaranteed over Temperature
- Guaranteed for Operation with ±12V Supplies
- Improved Replacement for Standard DAC80, DAC800 HI-5680
- High Stability, High Current Output Buried Zener Reference
- Laser Trimmed to High Accuracy: ±1/2LSB max Nonlinearity
- Low Cost Plastic Packaging

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD DAC80 Series is a family of low cost 12-bit digital-to-analog converters with both a high stability voltage reference and output amplifier combined on a single monolithic chip. The AD DAC80 Series is recommended for all low cost 12-bit D/A converter applications where reliability and cost are of paramount importance.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional DAC80 devices. Innovative circuit design reduces the total power consumption to 300mW which not only improves reliability but also improves long term stability.

The AD DAC80 incorporates a fully differential, non-saturating precision current switching cell structure which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in lower differential nonlinearity errors. A low noise, high stability, subsurface Zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature drift characteristics which challenge the best discrete Zener references.

The AD DAC80 Series is available in three performance grades and two package types. The AD DAC80 is specified for use over the 0 to +70°C temperature range and is available in both plastic and ceramic DIP packages. The AD DAC85 and AD DAC87 are available in hermetically sealed ceramic packages and are specified for the −25°C to +85°C and −55°C to +125°C temperature ranges.

PRODUCT HIGHLIGHTS

1. The AD DAC80 series of D/A converters directly replaces all other devices of this type with significant increases in performance.
2. Single chip construction and low power consumption provides the optimum choice for applications where low cost and high reliability are major considerations.
3. The high speed output amplifier has been designed to settle within 1/2LSB for a 10V full scale transition in 2.0μs, when properly compensated.
4. The precision buried Zener reference can supply up to 2.5mA for use elsewhere in the application.
5. The low TC binary ladder guarantees that all units are monotonic over the specified temperature range.
6. System performance upgrading is possible without redesign.

PRODUCT OFFERING

Analog Devices has developed a number of technologies to support products within the data acquisition market. In serving the market new products are implemented with the technology best suited to the application. The DAC80 series of products was first implemented in hybrid form and now it is available in a single monolithic chip. We will provide both the hybrid and monolithic versions of the family so that in existing designs changes to documentation or product qualification will not have to be done. Specifications and ordering information for both versions are delineated in this data sheet.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TECHNOLOGY		Monolithic			Monolithic			Monolithic		
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
BCD – CCD		–			–			–		Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)			250			250			250	μA
I_{IL} (V_{IL} = 0.8V)			100			100			100	μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C										
CBI			±1/2			±1/2			±1/2	LSB[1]
CCD										LSB
T_A @ T_{min} to T_{max}		±1/4	±1/2		±1/4	±1/2		±1/2	±3/4	LSB
Differential Linearity Error @ +25°C										
CBI			±3/4			±3/4			±3/4	LSB
CCD										LSB
T_A @ T_{min} to T_{max}			±3/4			±1			±1	LSB
Gain Error[2]		±0.1	±0.3		±0.1	±0.2		±0.1	±0.2	%FSR[3]
Offset Error[2]		±0.05	±0.15		±0.05	±0.1		±0.05	±0.1	%FSR[3]
Temperature Range for Guaranteed										
Monotonicity	0		+70	−25		+85	−55		+125	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±20			±20			±30	ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		±0.08	±0.15		±0.12	±0.2		±0.18	±0.3	% of FSR
Bipolar		±0.06	±0.10		±0.08	±0.12		±0.14	±0.24	% of FSR
Gain										
Including Internal Reference		±15	±30			±20			±20	ppm of FSR/°C
Excluding Internal Reference		±4	±7			±10			±10	ppm of FSR/°C
Unipolar Offset		±1	±3			±3			±3	ppm of FSR/°C
Bipolar Offset		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ‖500pF load)										
with 10kΩ Feedback		3	4		3	4		3	4	μs
with 5kΩ Feedback		2	3		2	3		2	3	μs
For LSB Change		1			1			1		μs
Slew Rate	10			10			10			V/μs
ANALOG OUTPUT										
Voltage Models										
Ranges – CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
– CCD										V
Output Current		±5			±5			±5		mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Current			40			40			40	mA
Internal Reference Voltage (V_R)	+6.23	+6.3	+6.37	+6.23	+6.3	+6.37	+6.23	+6.3	+6.37	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			+2.5			+2.5			+2.5	mA
Tempco of Drift		±10	±20		±10	±20			±10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ±10%, 5V supply when applicable			±0.002			±0.002			±0.002	% of FSR/%V_S
±12V ±5%			±0.002			±0.002			±0.002	% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15			±15			±15		V
Range										
Analog Supplies		±11.4[7]	±16.5		±11.4[7]	±16.5		±11.4[7]	±16.5	V
Logic Supplies									V	
Supply Drain										
+12, +15V		5	10		5	10		5	10	mA
−12, −15V		14	20		14	20		14	20	mA
TEMPERATURE RANGE										
Specification	0		+70	−25		+85	−55		+125	°C
Operating	−25		+85	−55		+125	−55		+125	°C
Storage	−25		+125	−65		+150	−65		+150	°C

NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3]FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V Range.
[4]Gain and offset errors adjusted to zero at +25°C.
[5]C_T = 0, see Figure 1a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]A minimum of ±12.3V is required for a ±10V full scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD DAC80			AD DAC85C			AD DAC85			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TECHNOLOGY		Hybrid			Hybrid			Hybrid		
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
BCD – CCD			3			3			3	Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)		+250			+250			+250		μA
I_{IL} (V_{IL} = 0.8V)		−100			−100			−100		μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C										
CBI		±1/4	±1/2			±1/2			±1/2	LSB[1]
CCD		±1/8	±1/4			±1/4			±1/4	LSB
T_A @ T_{min} to T_{max}		±1/4	±1/2		±1/4	±1/2		±1/2	±1/2	LSB
Differential Linearity Error @ +25°C										
CBI		±1/2	±3/4		±1/2			±1/2		LSB
CCD		±1/4	±1/2		±1/2			±1/2		LSB
T_A @ T_{min} to T_{max}			±1			±1			±1	LSB
Gain Error[2]		±0.1	±0.3		±0.1			±0.1		%FSR[3]
Offset Error[2]		±0.05	±0.15		±0.05			±0.05		%FSR[3]
Temperature Range for Guaranteed Monotonicity	0		+70	0		+70	−25		+85	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±20							ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		±0.08	±0.15							% of FSR
Bipolar		±0.06	±0.10							% of FSR
Gain										
Including Internal Reference		±15	±30			±20			±20	ppm of FSR/°C
Excluding Internal Reference		±5	±7			±10			±10	ppm of FSR/°C
Unipolar Offset		±1	±3		±1			±1		ppm of FSR/°C
Bipolar Offset		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ||500pF load)										
with 10kΩ Feedback		5			5			5		μs
with 5kΩ Feedback		3			3			3		μs
For LSB Change		1.5			1.5			1.5		μs
Slew Rate	10	15			20			20		V/μs
Current Model (I)										
Settling Time to ±0.01% of FSR for FSR Change 10 to 100Ω Load		300			300			300		ns
for 1kΩ Load		1			1			1		μs
ANALOG OUTPUT										
Voltage Models										
Ranges – CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
– CCD		±10			+10			+10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common			Indefinite to Common		
Current Models										
Ranges – Unipolar		−2.0			−2.0			−2.0		mA
– Bipolar		±1.0			±1.0			±1.0		mA
Output Impedance – Bipolar		3.2			3.2			3.2		kΩ
– Unipolar		6.6			6.6			6.6		kΩ
Compliance		−1.5, +10			−2.5, +10			−2.5, +10		V
Internal Reference Voltage (V_R)	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			+2.5			+2.5			+2.5	mA
Tempco of Drift		±10	±20		±10	±20		±10	±20	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ±10%, 5V supply when applicable		±0.002			±0.002			±0.002		% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15, 5			±15, 5			±15, 5		V
Range										
Analog Supplies	±14		±16	±14.5		±15.5	±14.5		±15.5	V
Logic Supplies	+4.5		+16	+4.5		+15.5	+4.5		+15.5	V
Supply Drain[7]										
+15V		10	20		15	20		15	20	mA
−15V		20	35		25	30		25	30	mA
+5V[8]		8	20		15	20		15	20	mA
TEMPERATURE RANGE										
Specification	0		+70	0		+70	−25		+85	°C
Operating	−25		+85	−25		+85	−55		+125	°C
Storage	−55		+130	−65		+150	−65		+150	°C

NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3]FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V range.
[4]Gain and offset errors adjusted to zero at +25°C.
[5]C_F = 0, see Figure 1a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]Including 5mA load.
[8]+5V supply required only for CCD versions.
Specifications subject to change without notice.

AD DAC80/AD DAC85/AD DAC87—SPECIFICATIONS

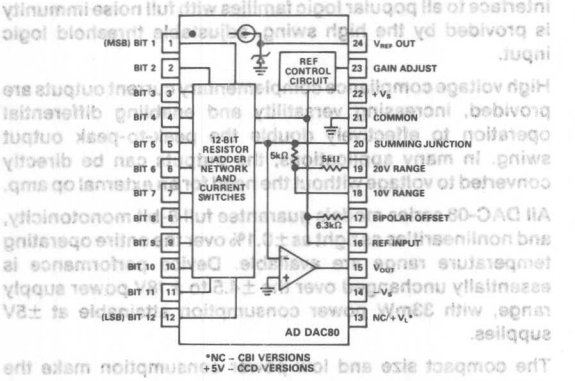
(T_A = +25°C, rated power supplies unless otherwise noted.)

Model	AD DAC85LD			AD DAC85MIL			AD DAC87			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TECHNOLOGY		Hybrid			Hybrid			Hybrid		
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
BCD – CCD		–			–			–		Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)		+250			+250			+250		μA
I_{IL} (V_{IL} = 0.8V)		−100			−100			−100		μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C										
CBI			±1/2			±1/2			±1/2	LSB[1]
CCD		–			–			–		LSB
T_A @ T_{min} to T_{max}			±1/2			±3/4			±3/4	LSB
Differential Linearity Error @ +25°C										
CBI		±1/2			±1/2			±1/2		LSB
CCD										LSB
T_A @ T_{min} to T_{max}			±1			±1			±1	LSB
Gain Error[2]		±0.1			±0.1			±0.1	±0.2	% FSR[3]
Offset Error[2]		±0.05			±0.05			±0.05	±0.1	%FSR[3]
Temperature Range for Guaranteed Monotonicity	−25		+85	−55		+125	−55		+125	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)		–			–			±15	±30	ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		–			–			±0.13	±0.30	% of FSR
Bipolar		–			–			±0.12	±0.24	% of FSR
Gain										
Including Internal Reference			±10			±20		±10	±25	ppm of FSR/°C
Excluding Internal Reference								±5	±10	ppm of FSR/°C
Unipolar Offset		±1			±2			±1	±3	ppm of FSR/°C
Bipolar Offset			±5			±10		±5	±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ||500pF load)										
with 10kΩ Feedback		5			5			5		μs
with 5kΩ Feedback		3			3			3		μs
For LSB Change		1.5			1.5			1.5		μs
Slew Rate		20			20			20		V/μs
Current Model (I)										
Settling Time to ±0.01% of FSR for FSR Change 10 to 100Ω Load		300			300			300		ns
for 1kΩ Load		1			1			1		μs
ANALOG OUTPUT										
Voltage Models										
Ranges – CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
– CCD										V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common			Indefinite to Common		
Current Models										
Ranges – Unipolar		−2.0			−2.0			−2.0		mA
– Bipolar		±1.0			±1.0			±1.0		mA
Output Impedance – Bipolar		3.2			3.2		2.5	3.2	4.1	kΩ
– Unipolar		6.6			6.6		5.0	6.6	8.2	kΩ
Compliance		−2.5, +10			−2.5, +10			−1.5, +10		V
Internal Reference Voltage (V_R)	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			+2.5			+2.5			+2.5	mA
Tempco of Drift		±10	20		10	20		±5	10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ±10%, 5V supply when applicable		±0.002			±0.002			±0.002	±0.003	% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15, 5			±15, 5			±15, 5		V
Range										
Analog Supplies	±14.5		±15.5	±14.5		±15.5	±13.5		±16.5	V
Logic Supplies	+4.5		+15.5	+4.5		+15.5	+4.5		+16.5	V
Supply Drain[7]										
+15V		15	20		15	20		10	20	mA
−15V		25	30		25	30		20	35	mA
+5V[8]		15	20		15	20		10	20	mA
TEMPERATURE RANGE										
Specification	−25		+85	−55		+125	−55		+125	°C
Operating	−55		+125	−55		+125	−55		+125	°C
Storage	−55		+125	−55		+120	−65		+150	°C

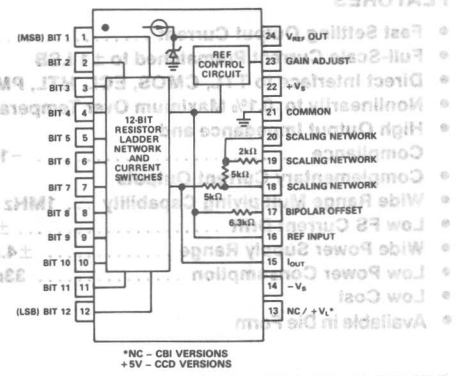
NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3]FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V range.
[4]Gain and offset errors adjusted to zero at +25°C.
[5]C_P = 0, see Figure 1a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]Including 5mA load.
[8]+5V supply required only for CCD versions.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to Power Ground	0V to +18V
$-V_S$ to Power Ground	0V to −18V
Digital Inputs (Pins 1 to 12) to Power Ground	−1.0V to +7V
Ref In to Reference Ground	±12V
Bipolar Offset to Reference Ground	±12V
10V Span R to Reference Ground	±12V
20V Span R to Reference Ground	±24V
Ref Out	Indefinite short to power ground or $+V_S$



Voltage Model Functional Diagram and Pin Configuration



Current Model Functional Diagram and Pin Configuration

ORDERING GUIDE

Model	Input Code	Output Mode	Technology	Temperature Range	Linearity Error	Package Option*
AD DAC80N-CBI-V	Binary	Voltage	Monolithic	0 to +70°C	±1/2LSB	N-24A
AD DAC80D-CBI-V	Binary	Voltage	Monolithic	0 to +70°C	±1/2LSB	D-24
AD DAC85D-CBI-V	Binary	Voltage	Monolithic	−25°C to +85°C	±1/2LSB	D-24
AD DAC87D-CBI-V	Binary	Voltage	Monolithic	−55°C to +125°C	±1/2LSB	D-24
AD DAC80-CBI-V	Binary	Voltage	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC80-CBI-I	Binary	Current	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC80-CCD-V	Binary Coded Decimal	Voltage	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC80-CCD-I	Binary Coded Decimal	Current	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC80Z-CBI-V**	Binary	Voltage	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC80Z-CBI-I**	Binary	Current	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC80Z-CCD-V**	Binary Coded Decimal	Voltage	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC80Z-CCD-I**	Binary Coded Decimal	Current	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC85C-CBI-V	Binary	Voltage	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC85C-CBI-I	Binary	Current	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC85-CBI-V	Binary	Voltage	Hybrid	−25°C to +85°C	±1/2LSB	DH-24A
AD DAC85-CBI-I	Binary	Current	Hybrid	−25°C to +85°C	±1/2LSB	DH-24A
AD DAC85LD-CBI-V	Binary	Voltage	Hybrid	−25°C to +85°C	±1/2LSB	DH-24A
AD DAC85LD-CBI-I	Binary	Current	Hybrid	−25°C to +85°C	±1/2LSB	DH-24A
AD DAC85MIL-CBI-V	Binary	Voltage	Hybrid	−55°C to +125°C	±1/2LSB	DH-24A
AD DAC85MIL-CBI-I	Binary	Current	Hybrid	−55°C to +125°C	±1/2LSB	DH-24A
AD DAC85C-CCD-V	Binary Coded Decimal	Voltage	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC85C-CCD-I	Binary Coded Decimal	Current	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC85-CCD-V	Binary Coded Decimal	Voltage	Hybrid	−25°C to +85°C	±1/4LSB	DH-24A
AD DAC85-CCD-I	Binary Coded Decimal	Current	Hybrid	−25°C to +85°C	±1/4LSB	DH-24A
AD DAC87-CBI-V	Binary	Voltage	Hybrid	−55°C to +125°C	±1/2LSB	DH-24A
AD DAC87-CBI-I	Binary	Current	Hybrid	−55°C to +125°C	±1/2LSB	DH-24A

*For outline information see Package Information section.

**Z-Suffix devices guarantee performance of 0 to +5V and ±5V spans with minimum supply voltages of ±11.4V.

8-Bit, High Speed, Multiplying D/A Converter (Universal Digital Logic Interface)

DAC08

FEATURES

- Fast Settling Output Current 85ns
- Full-Scale Current Prematched to ±1 LSB
- Direct Interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to 0.1% Maximum Over Temperature Range
- High Output Impedance and Compliance ..... −10V to +18V
- Complementary Current Outputs
- Wide Range Multiplying Capability ... 1MHz Bandwidth
- Low FS Current Drift ..... ±10ppm/°C
- Wide Power Supply Range ..... ±4.5V to ±18V
- Low Power Consumption ..... 33mW @ ±5V
- Low Cost
- Available in Die Form

GENERAL DESCRIPTION

The DAC-08 series of 8-bit monolithic digital-to-analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low "glitch" energy and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic input.

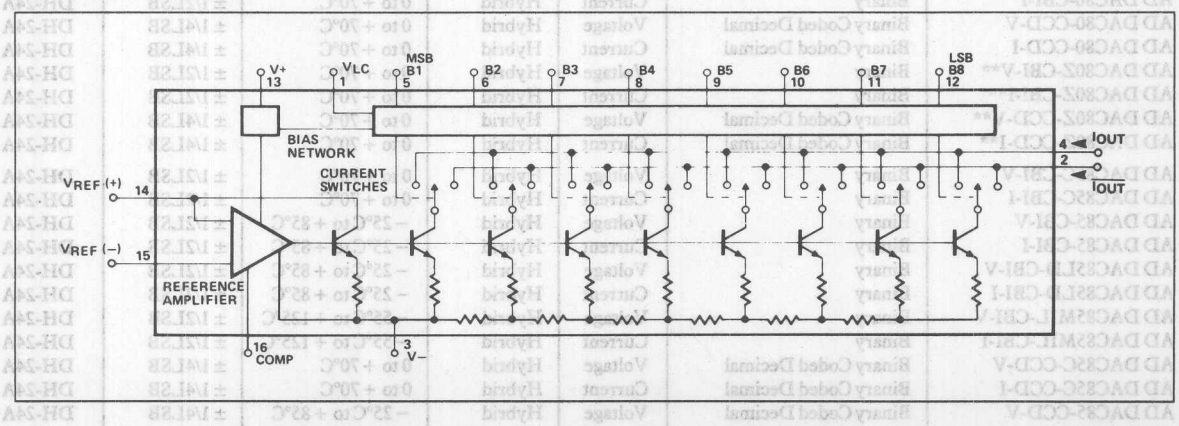
High voltage compliance complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5 to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883, Level B are available.

DAC-08 applications include 8-bit, 1μs A/D converters, servo motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature
- DAC-08AQ, Q ..... –55°C to +125°C
- DAC-08HQ, EQ, CQ, HP, EP, CP, CS ..... 0°C to +70°C

Junction Temperature (T_j) ..... –65°C to +150°C
Storage Temperature Q Package ..... –65°C to +150°C
Storage Temperature P Package ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
V+ Supply to V– Supply 36V
Logic Inputs ..... V– to V– plus 36V
V_{LC} ..... V– to V+
Analog Current Outputs (at V_S – = 15V) 4.25mA
Reference Input (V_{14} to V_{15}) ..... V– to V+
Reference Input Differential Voltage (V_{14} to V_{15}) ..... ±18V
Reference Input Current (I_{14}) 5.0mA

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	76	36	°C/W
16-Pin SO (S)	111	35	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

3

ELECTRICAL CHARACTERISTICS

at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $-55°C \le T_A \le +125°C$ for DAC-08/08A, $0°C \le T_A \le +70°C$ for DAC-08C, E & H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-08A/H MIN	DAC-08A/H TYP	DAC-08A/H MAX	DAC-08E MIN	DAC-08E TYP	DAC-08E MAX	DAC-08C MIN	DAC-08C TYP	DAC-08C MAX	UNITS
Resolution			8	—		8	—	—	8	—	—	Bits
Monotonicity			8	—	—	8	—	—	8	—	—	Bits
Nonlinearity	NL		—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Settling Time	t_S	To ±1/2 LSB, all bits switched ON or OFF, $T_A = 25°C$, (Note)	—	85	135	—	85	150	—	85	150	ns
Propagation Delay												
Each bit	t_{PLH}	$T_A = 25°C$ (Note)	—	35	60	—	35	60	—	35	60	ns
All bits switched	t_{PHL}		—	35	60	—	35	60	—	35	60	
Full-Scale Tempco (Note)	TCI_{FS}	DAC-08E	—	±10	±50	—	±10	±80	—	±10	±80	ppm/°C
			—	—	—	—	—	±50	—	—	—	
Output Voltage Compliance (True Compliance)	V_{OC}	Full-Scale current change <1/2 LSB, $R_{OUT} > 20M\Omega$ typical	–10	—	+18	–10	—	+18	–10	—	+18	V
Full Range Current	I_{FR4}	$V_{REF} = 10.000V$, $R_{14}, R_{15} = 5.000k\Omega$, $T_A = +25°C$	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	$I_{FR4} - I_{FR2}$	—	±0.5	±4	—	±1	±8	—	±2	±16	μA
Zero-Scale Current	I_{ZS}		—	0.1	1	—	0.2	2	—	0.2	4	μA
Output Current Range	IOR_1	$R_{14}, R_{15} = 5.000k\Omega$, $V_{REF} = +15.0V$, $V- = -10V$	2.1	—	—	2.1	—	—	2.1	—	—	mA
	IOR_2	$V_{REF} = +25.0V$, $V- = -12V$	4.2	—	—	4.2	—	—	4.2	—	—	
Output Current Noise		$I_{REF} = 2mA$	—	25	—	—	25	—	—	25	—	nA
Logic Input Levels												
Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	—	—	0.8	V
Logic Input "1"	V_{IL}		2	—	—	2	—	—	2	—	—	
Logic Input Current		$V_{LC} = 0V$										
Logic "0"	I_{IL}	$V_{IN} = -10V$ to $+0.8V$	—	–2	–10	—	–2	–10	—	–2	–10	μA
Logic Input "1"	I_{IH}	$V_{IN} = 2.0V$ to 18V	—	0.002	10	—	0.002	10	—	0.002	10	
Logic Input Swing	V_{IS}	$V- = -15V$	–10	—	+18	–10	—	+18	–10	—	+18	V
Logic Threshold Range	V_{THR}	$V_S = \pm 15V$, (Note)	–10	—	+13.5	–10	—	+13.5	–10	—	+13.5	V
Reference Bias Current	I_{15}		—	–1	–3	—	–1	–3	—	–1	–3	μA
Reference Input Slew Rate	dI/dt	$R_{EQ} = 200\Omega$ See fast pulsed $R_L = 100\Omega$ ref. info. $C_C = 0pF$ following. (Note)	4	8	—	4	8	—	4	8	—	mA/μs
Power Supply Sensitivity	$PSSI_{FS+}$	$V+ = 4.5V$ to 18V	—	±0.0003	±0.01	—	±0.0003	±0.01	—	±0.0003	±0.01	$\%\Delta I_O/\%\Delta V+$
	$PSSI_{FS-}$	$V- = -4.5V$ to $-18V$ $I_{REF} = 1.0mA$	—	±0.002	±0.01	—	±0.002	±0.01	—	±0.002	±0.01	$\%\Delta I_O/\%\Delta V-$

NOTE: Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $-55°C \leq T_A \leq +125°C$ for DAC-08/08A, $0°C \leq T_A \leq +70°C$ for DAC-08C, E & H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-08A/H MIN	DAC-08A/H TYP	DAC-08A/H MAX	DAC-08E MIN	DAC-08E TYP	DAC-08E MAX	DAC-08C MIN	DAC-08C TYP	DAC-08C MAX	UNITS
Power Supply Current	I+	$V_S = \pm 5V$, $I_{REF} = 1.0mA$	—	2.3	3.8	—	2.3	3.8	—	2.3	3.8	mA
	I−		—	−4.3	−5.8	—	−4.3	−5.8	—	−4.3	−5.8	
	I+	$V_S = +5V, -15V$, $I_{REF} = 2.0mA$	—	2.4	3.8	—	2.4	3.8	—	2.4	3.8	
	I−		—	−6.4	−7.8	—	−6.4	−7.8	—	−6.4	−7.8	
	I+	$V_S = \pm 15V$, $I_{REF} = 2.0mA$	—	2.5	3.8	—	2.5	3.8	—	2.5	3.8	
	I−		—	−6.5	−7.8	—	−6.5	−7.8	—	−6.5	−7.8	
Power Dissipation	P_d	$\pm 5V$, $I_{REF} = 1.0mA$	—	33	48	—	33	48	—	33	48	mW
		$+5V, -15V$, $I_{REF} = 2.0mA$	—	108	136	—	103	136	—	108	136	
		$\pm 15V$, $I_{REF} = 2.0mA$	—	135	174	—	135	174	—	135	174	

NOTE: Guaranteed by design.

ORDERING INFORMATION†

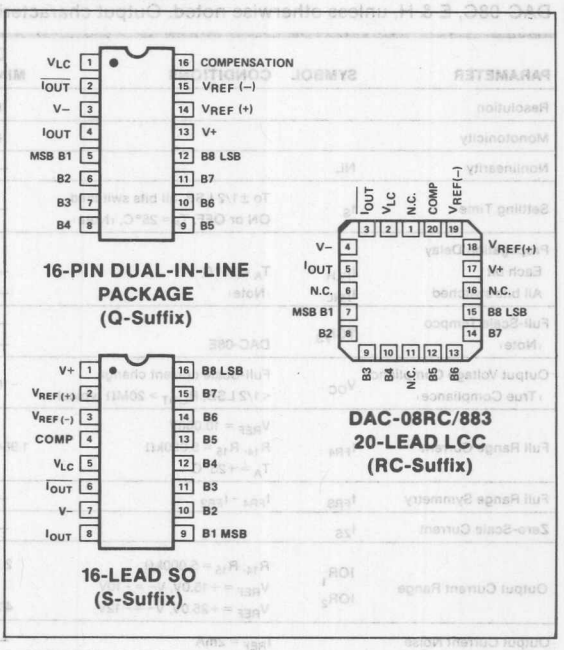
NL	16-PIN DUAL-IN-LINE PACKAGE HERMETIC	PLASTIC	LCC	OPERATING TEMPERATURE RANGE
0.1%	DAC08AQ*	—	—	MIL
	DAC08HQ	DAC08HP	—	COM
0.19%	DAC08Q*	—	DAC08RC/883	MIL
	DAC08EQ	DAC08EP	—	COM
0.39%	DAC08CQ	DAC08CP	—	COM
	—	DAC08CS††	—	

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS



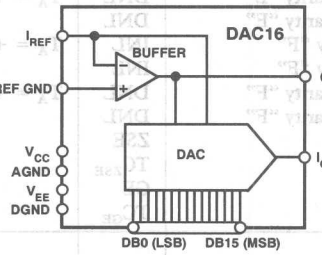
16-Bit High Speed Current-Output DAC

DAC16

FEATURES
- ±1 LSB Differential Linearity (max)
- Guaranteed Monotonic Over Temperature Range
- ±2 LSB Integral Linearity (max)
- 500 ns Settling Time
- 5 mA Full-Scale Output
- TTL/CMOS Compatible
- Low Power: 190 mW (typ)
- Available in Die Form

APPLICATIONS
- Communications
- ATE
- Data Acquisition Systems
- High Resolution Displays

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC16 is a 16-bit high speed current-output digital-to-analog converter with a settling time of 500 ns. A unique combination of low distortion, high signal-to-noise ratio, and high speed make the DAC16 ideally suited to performing waveform synthesis and modulation in communications, instrumentation, and ATE systems. Input reference current is buffered, with full-scale output current of 5 mA. The 16-bit parallel digital input bus is TTL/CMOS compatible. Operating from +5 V and −15 V supplies, the DAC16 consumes 190 mW (typ) and is available in a 24-pin epoxy DIP, epoxy surface-mount small outline (SOL), ceramic side brazed DIP, 28-pin leadless ceramic chip carrier (LCC) packages, and in die form.

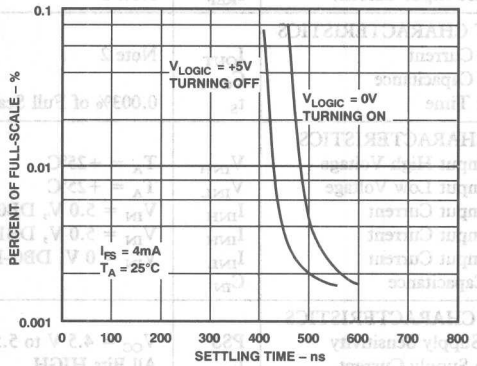


Figure 1. DAC16 Settling Time Accuracy vs. Percent of Full Scale

ORDERING GUIDE

Model	Grade DNL (max)	Temperature Range	Package Description	Package Option[1]
DAC16EP	±1	−40°C to +85°C	24-Pin PDIP	N-24
DAC16ES	±1	−40°C to +85°C	24-Pin SOL	R-24
DAC16FP	±2	−40°C to +85°C	24-Pin PDIP	N-24
DAC16FS	±2	−40°C to +85°C	24-Pin SOL	R-24
DAC16BVB[2]	±2	−55°C to +125°C	24-Pin Ceramic DIP	D-24A
DAC16BTC[2]	±2	−55°C to +125°C	28-Pin LCC	E-28A
DAC16GBC	±1	+25°C	Die	

NOTES
[1]For package outline information see Package Information section.
[2]Consult factory for availability.

DAC16—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{CC} = +5.0 V, V_{EE} = −15.0 V, I_{REF} = 0.5 mA, C_{COMP} = 47 µF, −40°C ≤ T_A ≤ +85°C unless otherwise noted. See Note 1 for supply variations.)

Parameter		Conditions	Min	Typ	Max	Units
Integral Linearity "E"	INL	T_A = +25°C	−2	±1.2	+2	LSB
Integral Linearity "E"	INL		−4	±1.6	+4	LSB
Differential Linearity "E"	DNL	T_A = +25°C	−1	±0.5	+1	LSB
Differential Linearity "E"	DNL		−1	±0.7	+1.5	LSB
Integral Linearity "F"	INL	T_A = +25°C	−4	±1.4	+4	LSB
Integral Linearity "F"	INL		−6	±2	+6	LSB
Differential Linearity "F"	DNL	T_A = +25°C	−1	±0.5	+1.5	LSB
Differential Linearity "F"	DNL		−1.5	±0.6	+2	LSB
Zero Scale Error	ZSE				1	LSB
Zero Scale Drift	TC_{ZSE}			0.025		ppm/°C
Gain Error	GE				±0.225	% FS
Gain Drift	TC_{GE}			5		ppm/°C
REFERENCE[2]						
Reference Input Current	I_{REF}	Note 2	350		625	µA
OUTPUT CHARACTERISTICS						
Output Current	I_{OUT}	Note 2	2.8		5.0	mA
Output Capacitance	C_{OUT}			10		pF
Settling Time	t_S	0.003% of Full Scale		500		ns
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}	T_A = +25°C	2.4			V
Logic Input Low Voltage	V_{INL}	T_A = +25°C			0.8	V
Logic Input Current	I_{INH}	V_{IN} = 5.0 V, DB0–DB10			7.5	µA
Logic Input Current	I_{INH}	V_{IN} = 5.0 V, DB11–DB15			100	µA
Logic Input Current	I_{INL}	V_{IN} = 0 V, DB0–DB15			1	µA
Input Capacitance	C_{IN}			8		pF
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSS	V_{CC} = 4.5 V to 5.5 V, V_{EE} = −13 V to −17 V			20	ppm/V
Positive Supply Current	I_{CC}	All Bits HIGH		15	22	mA
Positive Supply Current	I_{CC}	All Bits LOW		6	7.5	mA
Negative Supply Current	I_{EE}			7.5	10	mA
Power Dissipation	P_{DISS}			188	260	mW

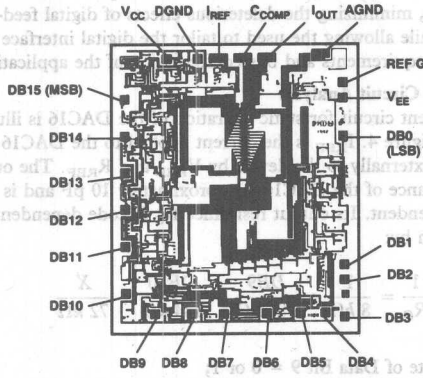
NOTES
[1]All supplies can be varied ±5% and operation is guaranteed. Device is tested with nominal supplies.
[2]Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed (see Figures 7 and 8).
Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_{CC} = +5.0 V, V_{EE} = −15.0 V, I_{REF} = 0.5 mA, C_{COMP} = 47 µF, T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Conditions	DAC16G Limit	Units
Integral Nonlinearity	INL		±3	LSB max
Differential Nonlinearity	DNL		±1	LSB max
Zero Scale Error	ZSE		±1	LSB max
Gain Error	GE		±0.12	% FS max
Logic Input High Voltage	V_{INH}		2.4	V min
Logic Input Low Voltage	V_{INL}		0.8	V max
Logic Input Current	I_{IN}		75	µA max
Positive Supply Current	I_{CC}		20	mA max
Negative Supply Current	I_{EE}		10	mA max
Power Dissipation	P_{DISS}		250	mW max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice, Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

DICE CHARACTERISTICS



Die Size 0.129 × 0.153 inch, 19,737 sq. mils
(3.277 × 3.886 mm, 12.73 sq. mm)
The DAC16 Contains 330 Transistors.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{CC} to V_{EE} . . . . . −0.3 V, +25.0 V
V_{CC} to DGND . . . . . −0.3 V, +7.0 V
V_{EE} to AGND . . . . . +0.3 V, −18.0 V
DGND to AGND . . . . . −0.3 V, +0.3 V
REF GND to AGND . . . . . −0.3 V, +1.0 V
I_{REF} . . . . . 1 mA
Analog Output Current . . . . . 8 mA
Digital Input Voltage to DGND . . . . . $\leq V_{CC}$
Operating Temperature Range
EP, FP, ES, FS . . . . . −40°C to +85°C
BTC, BVB . . . . . −55°C to +125°C
Dice Junction Temperature . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Power Dissipation . . . . . 1000 mW
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[1]	θ_{JC}	Units
24-Pin Plastic DIP (P)	62	32	°C/W
24-Lead Plastic SOL (S)	70	22	°C/W
24-Lead Size Brazed DIP (VB)	50	26	°C/W
28-Lead Hermetic LCC (TC)	78	30	°C/W

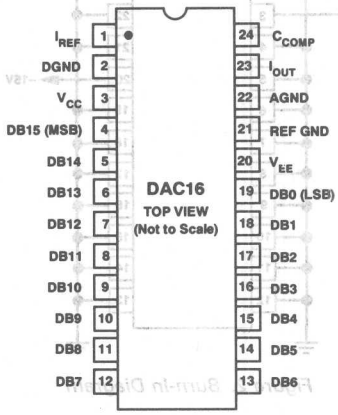
NOTE
[1]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket.

CAUTION

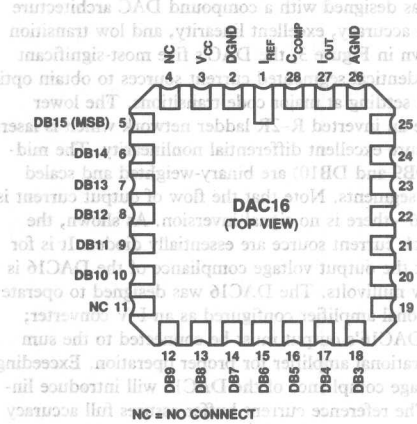
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected; however, permanent damage may occur on unprotected units from high energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures.
3. Remove power before inserting or removing units from their sockets.

PACKAGE PINOUTS

24-Pin DIP (P, S, VB)



28-Pin LCC (TC)



NC = NO CONNECT

PIN DESCRIPTION

Pin (P, S, VB)	(TC)	Name	Description
1	1	I_{REF}	Reference Current Input
2	2	DGND	Digital Ground
3	3	V_{CC}	+5 V Digital Supply
4–19	5–23	DB15–DB0	16-Bit Digital Input Bus. DB15 Is the MSB.
20	24	V_{EE}	−15 V Analog Supply
21	25	REF GND	Reference Current Return
22	26	AGND	Analog Ground/Output Reference
23	27	I_{OUT}	Current Output
24	28	C_{COMP}	Current Ladder Compensation
	4, 11, 19, 22	NC	No Connects

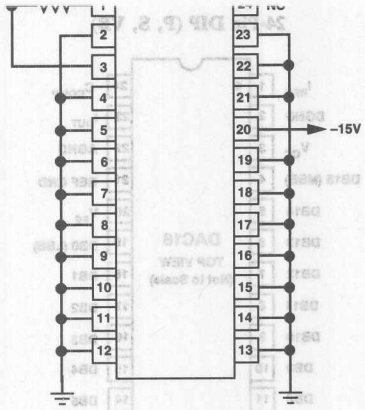


Figure 2. Burn-In Diagram

OPERATION

Novel DAC Architecture

The DAC16 was designed with a compound DAC architecture to achieve high accuracy, excellent linearity, and low transition errors. As shown in Figure 3, the DAC's five most-significant bits utilize 31 identical segmented current sources to obtain optimal high speed settling at major code transitions. The lower nine bits utilize an inverted R–2R ladder network which is laser-trimmed to ensure excellent differential nonlinearity. The middle two bits (DB9 and DB10) are binary-weighted and scaled from the MSB segments. Note that the flow of output current is into the DAC16—there is no signal inversion. As shown, the switches for each current source are essentially diodes. It is for this reason that the output voltage compliance of the DAC16 is limited to a few millivolts. The DAC16 was designed to operate with an operational amplifier configured as an I–V converter; therefore, the DAC16's output must be connected to the sum node of an operational amplifier for proper operation. Exceeding the output voltage compliance of the DAC16 will introduce linearity errors. The reference current buffer assures full accuracy unbuffered, minimizing the deleterious effects of digital feedthrough while allowing the used to tailor the digital interface to the speed requirements and bus configuration of the application.

Equivalent Circuit Analysis

An equivalent circuit for static operation of the DAC16 is illustrated in Figure 4. I_{REF} is the current applied to the DAC16 and is set externally to the device by V_{REF} and R_{REF}. The output capacitance of the DAC16 is approximately 10 pF and is code independent. Its output resistance R_O is code dependent and is given by:

$$\frac{1}{R_O} = \frac{1}{8\ k\Omega} + \frac{DB9}{288\ k\Omega} + \frac{DB10}{144\ k\Omega} + \frac{X}{72\ k\Omega}$$

where

DB9 = State of Data Bit 9 = 0 or 1;

DB10 = State of Data Bit 10 = 0 or 1; and

X = Decimal representation of the 5 MSBs (DB11– DB15) = 0 to 31.

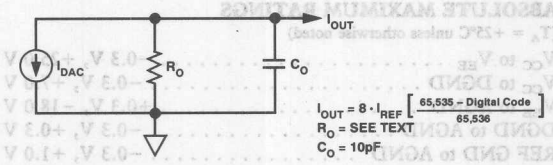


Figure 4. Equivalent Circuit for the DAC16

Table I provides the relationship between the input digital code and the output resistance of the DAC16.

Table I. DAC16 Output Resistance vs. Digital Code

Hex Digital Code	Scale	Output Resistance
FFFF	Zero	8 kΩ
BFFF	1/4	4.2 kΩ
7FFF	1/2	2.9 kΩ
3FFF	3/4	2.2 kΩ
0	Full – 1 LSB	1.8 kΩ

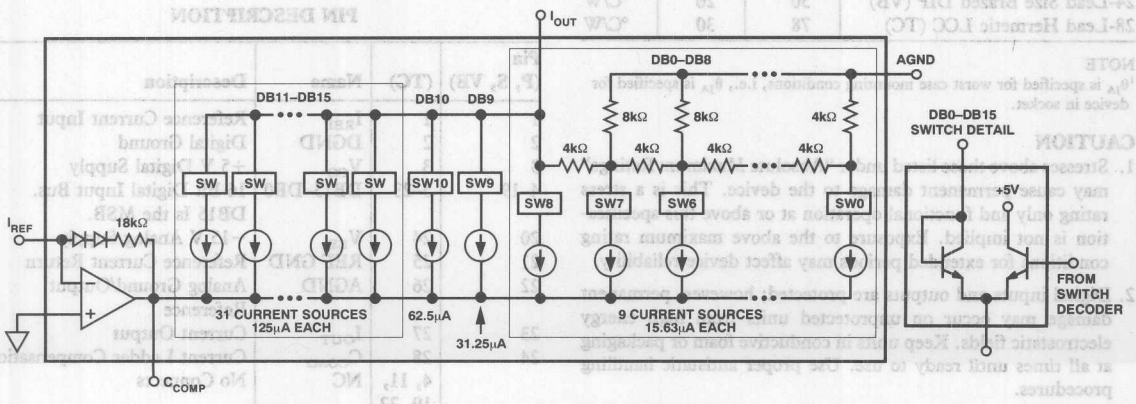


Figure 3. DAC16 Architecture

Digital Input Considerations

The threshold of the DAC16's digital input circuitry is set at 1.4 V, independent of supply voltage. Hence, the digital inputs can interface with any type of 5 V logic. Illustrated in Figure 5 is the equivalent circuit of the digital inputs. Note that the individual input capacitance is approximately 7 pF.

This input capacitance can be used in conjunction with an external R–C circuit for digital signal deskewing, if required. In applications where some of the DAC16's digital inputs are not used, the recommended procedure to turn off one or more inputs is to connect each input line to +5 V as shown in Figure 6.

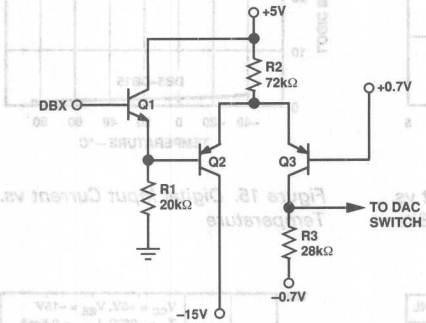


Figure 5. Equivalent Circuit of a DAC16 Digital Input

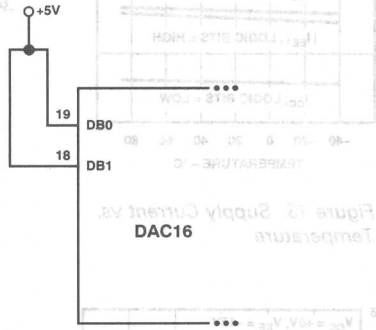


Figure 6. Handling Unused DAC16 Digital Inputs

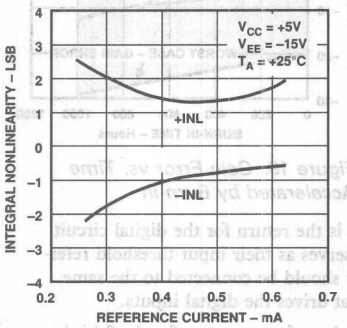


Figure 7. Integral Nonlinearity vs. I_{REF}

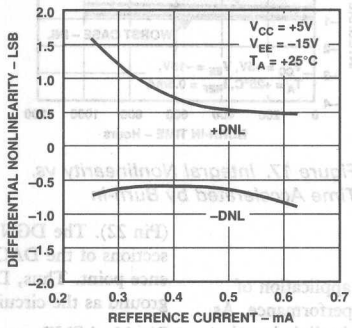


Figure 8. Differential Nonlinearity vs. I_{REF}

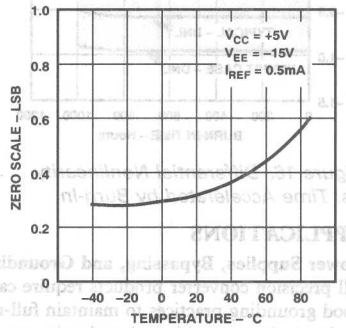


Figure 9. Zero Scale Output vs. Temperature

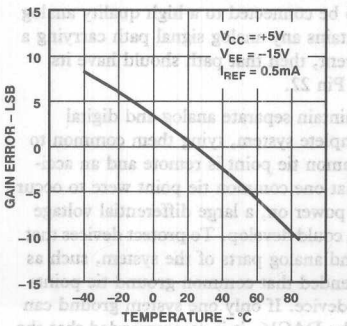


Figure 10. Gain Error vs. Temperature

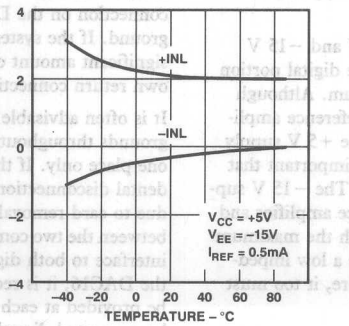


Figure 11. Integral Nonlinearity vs. Temperature

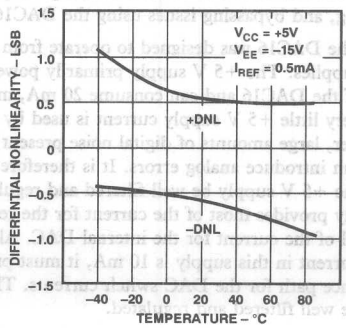


Figure 12. Differential Nonlinearity vs. Temperature

DAC16—Typical Performance Characteristics

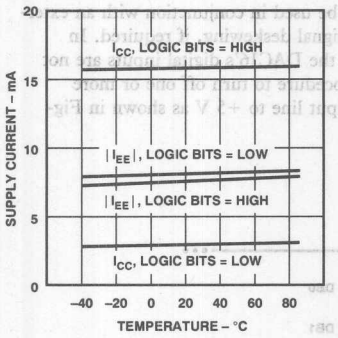


Figure 13. Supply Current vs. Temperature

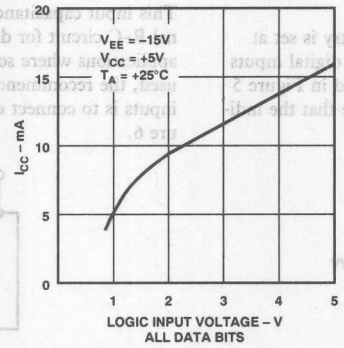


Figure 14. V_{CC} Supply Current vs. Logic Input Voltage, All Data Bits

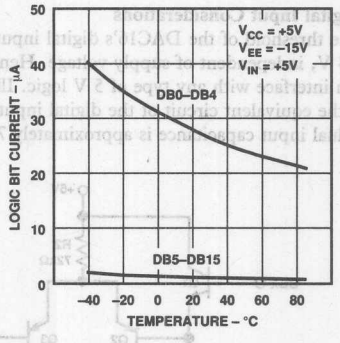


Figure 15. Digital Input Current vs. Temperature

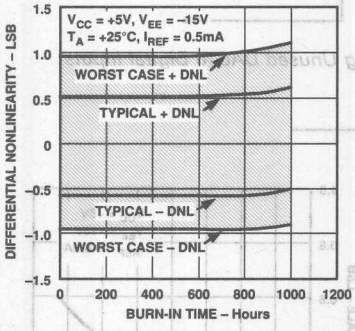


Figure 16. Differential Nonlinearity vs. Time Accelerated by Burn-In

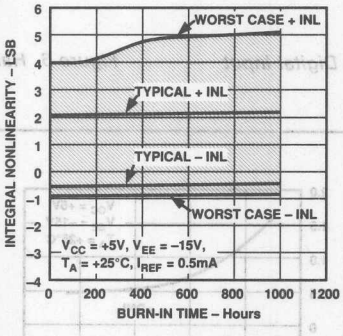


Figure 17. Integral Nonlinearity vs. Time Accelerated by Burn-In

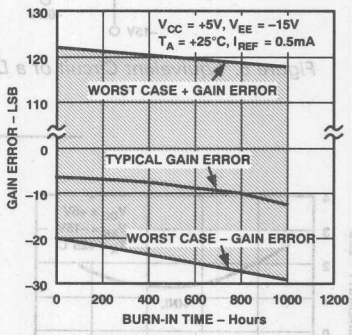


Figure 18. Gain Error vs. Time Accelerated by Burn-In

APPLICATIONS

Power Supplies, Bypassing, and Grounding

All precision converter products require careful application of good grounding practices to maintain full-rated performance. As is always the case with analog circuits operating in digital environments, digital noise is prevalent; therefore, special care must be taken to ensure that the DAC16's inherent precision is maintained. This means that particularly good engineering judgment should be exercised when addressing the power supply, grounding, and bypassing issues using the DAC16.

The DAC16 was designed to operate from +5 V and −15 V supplies. The +5 V supply primarily powers the digital portion of the DAC16 and can consume 20 mA, maximum. Although very little +5 V supply current is used by the reference amplifier, large amounts of digital noise present on the +5 V supply can introduce analog errors. It is therefore very important that the +5 V supply be well filtered and regulated. The −15 V supply provides most of the current for the reference amplifier and all of the current for the internal DAC. Although the maximum current in this supply is 10 mA, it must provide a low impedance path for the DAC switch currents. Therefore, it too must be well filtered and regulated.

The DAC16 includes two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (Pin 2) and AGND (Pin 22). The DGND pin is the return for the digital circuit sections of the DAC and serves as their input threshold reference point. Thus, DGND should be connected to the same ground as the circuitry that drives the digital inputs.

Pin 22, AGND, serves as the reference point for the 9-bit lower-order DAC as well as the common for the reference amplifier, REFGND (Pin 21). This pin should also serve as the reference point for all analog circuitry associated with the DAC16. Therefore, to minimize any errors, it is recommended that AGND connection on the DAC16 be connected to a high quality analog ground. If the system contains any analog signal path carrying a significant amount of current, then that path should have its own return connection to Pin 22.

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common to one place only. If the common tie point is remote and an accidental disconnection of that one common tie point were to occur due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the DAC16, it is recommended that common ground tie points be provided at each such device. If only one system ground can be connected directly to the DAC16, it is recommended that the analog common be used. If the system's AGND has suitable low impedance, then the digital signal currents flowing in it should

not seriously affect the ground noise. The amount of digital noise introduced by connecting the two grounds together at the device will not adversely affect system performance due to loss of digital noise immunity.

Generous bypassing of the DAC's supplies goes a long way in reducing supply-line induced errors. Even with well-filtered, well-regulated supplies, local bypassing consisting of 10 μF tantalum electrolytic shunted by a 0.1 μF ceramic is recommended. The decoupling capacitors should be connected between the DAC's supply pins (Pin 3 for +5 V, Pin 20 for −15 V) and the analog ground (Pin 22). Figure 19 shows how the DGND, AGND, and bypass connections should be made to the DAC16.

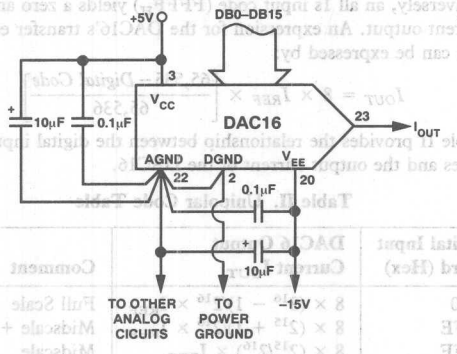


Figure 19. Recommended Grounding and Bypassing Scheme for the DAC16

Using the Right Capacitors

Probably the most important external components associated with high speed design are the capacitors used to bypass the power supplies and to provide compensation. Both selection and placement of these capacitors can be critical and, to a large extent, dependent upon the specifics of the system configuration. The dominant consideration in selection of bypass and compensation capacitors for the DAC16 is minimization of series resistance and inductance. Many capacitors begin to look inductive at 20 MHz and above—the very frequencies where rejection of interference is needed. Ceramic and film-type capacitors generally feature lower series inductance than tantalum or electrolytic types. A few general rules are of universal use when approaching the issue of compensation or bypassing.

Bypass capacitors should be installed on the printed circuit board with the shortest possible leads consistent with reliable construction. This helps to minimize series inductance in the leads. Chip capacitors are optimal in this respect. Where illustrated in the applications section, large tantalum electrolytic capacitors are shunted by low self-inductance ceramic capacitors. This technique reduces the self-resonance of the electrolytics while shifting the resonant frequency of the ceramics out-of-band.

Some series inductance between the DAC supply pins and the power supply plane often helps to filter out high frequency power supply noise. This inductance can be generated using a small ferrite bead as shown in Figure 20.

Reference Amplifier Considerations

The reference input current buffer is a high performance amplifier optimized for high accuracy and linearity. The design of the reference amplifier ensures fast settling times by tightly controlling the node common to all the current sources internal to the DAC with an external compensation capacitor (C_{COMP}). Since the primary design goal of the DAC16 is to achieve 16-bit performance, proper operation of the reference amplifier requires a

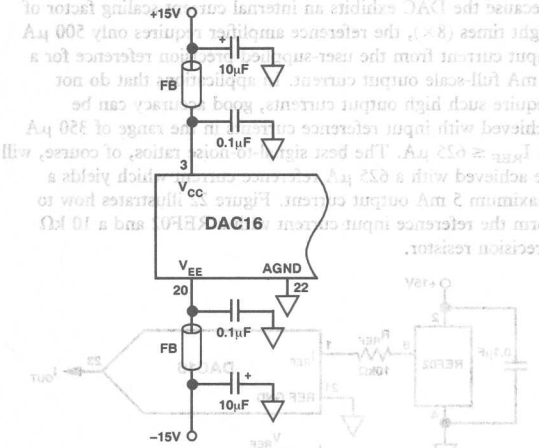


Figure 20. Using a Ferrite Bead as a High Frequency Filter

47 μF tantalum electrolytic capacitor shunted by a 0.1 μF ceramic capacitor, as shown in Figure 21. Increasing the capacitance at this node above the recommended values does not further reduce the analog transition current noise spikes at the output of the reference amplifier. Reducing the value of compensation, however, is not recommended as DAC linearity will degrade as a result. In most systems, the V_{EE} supply offers sufficiently low impedance to maintain a quiet return point for the reference amplifier. If this is not the case, the AGND point can also be used for the compensation capacitor return, as shown in Figure 21.

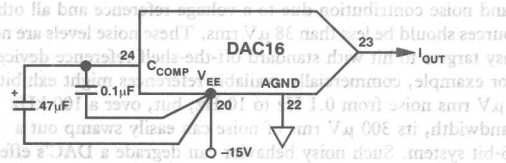


Figure 21a. Recommended Compensation Scheme to V_{EE}

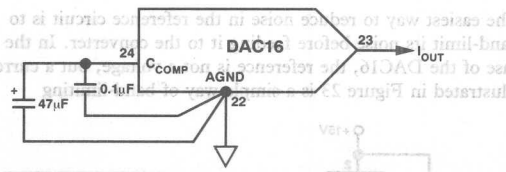


Figure 21b. Recommended Compensation Scheme to AGND

In applications where 16-bit multiplying performance is required, the DAC16 might appear to be a viable solution. However, the compensation capacitor network would have to be removed in these applications. The DAC16's reference amplifier was specifically designed for low frequency operation, with a compensation capacitor network. In fact, this network serves not only as a charge reservoir for the DAC's internal current sources

duce large linearity errors, reference amplifier instability, wideband reference amplifier noise, and poor settling time.

Because the DAC exhibits an internal current scaling factor of eight times (8×), the reference amplifier requires only 500 μA input current from the user-supplied precision reference for a 4 mA full-scale output current. In applications that do not require such high output currents, good accuracy can be achieved with input reference currents in the range of 350 μA $\leq I_{REF} \leq$ 625 μA. The best signal-to-noise ratios, of course, will be achieved with a 625 μA reference current which yields a maximum 5 mA output current. Figure 22 illustrates how to form the reference input current with a REF02 and a 10 kΩ precision resistor.

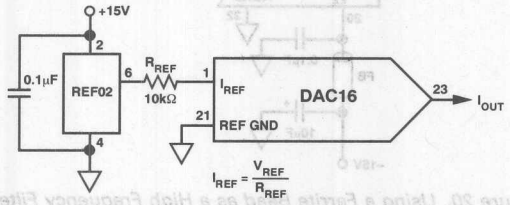


Figure 22. Generating the DAC16's Reference Input Current

Reducing Voltage Reference Noise

In data converters of 16-bit and greater resolution, noise is of critical importance. Surprisingly, the integrated voltage reference circuit used may contribute the dominant share of a system's noise floor, thereby degrading system dynamic range and signal-to-noise ratio. To maximize system dynamic range and SNR, all external noise contributions should be effectively much less than 1/2 LSB. For example, in a 5 V DAC16 application, one LSB is equivalent to 76 μV. This means that the total wideband noise contribution due to a voltage reference and all other sources should be less than 38 μV rms. These noise levels are not easy targets to hit with standard off-the-shelf reference devices. For example, commercially available references might exhibit 5 μV rms noise from 0.1 Hz to 10 Hz; but, over a 100 kHz bandwidth, its 300 μV rms of noise can easily swamp out a 16-bit system. Such noisy behavior can degrade a DAC's effective resolution by increasing its differential nonlinearity which, in turn, can lead to nonmonotonic behavior or analog errors.

The easiest way to reduce noise in the reference circuit is to band-limit its noise before feeding it to the converter. In the case of the DAC16, the reference is not a voltage, but a current. Illustrated in Figure 23 is a simple way of band-limiting

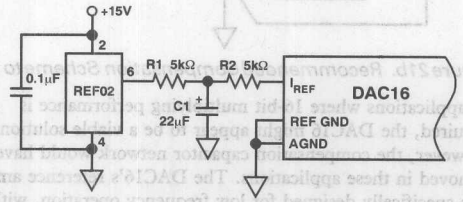


Figure 23. Filtering a Reference's Wideband Noise

thermally induced errors, R1 and R2 must be electrically and thermally well-matched. Thin-film resistor networks work well here. In this circuit, the parallel combination of R1 and R2 forms a 3 Hz low pass filter with C1. The only noise source that remains is the thermal noise of R2 which can be a significantly lower noise generator than the voltage reference.

Input Coding

The unipolar digital input coding of the DAC16 employs negative logic to control the output current; that is, an all zero input code (0000_H) yields an output current 1 LSB below full scale. Conversely, an all 1s input code ($FFFF_H$) yields a zero analog current output. An expression for the DAC16's transfer equation can be expressed by:

$$I_{OUT} = 8 \times I_{REF} \times \left[\frac{65{,}535 - Digital\ Code}{65{,}536}\right]$$

Table II provides the relationship between the digital input codes and the output current of the DAC16.

Table II. Unipolar Code Table

Digital Input Word (Hex)	DAC16 Output Current I_{OUT}	Comment
0000	$8 \times (2^{16} - 1)/2^{16} \times I_{REF}$	Full Scale
7FFE	$8 \times (2^{15} + 1)/2^{16} \times I_{REF}$	Midscale + 1 LSB
7FFF	$8 \times (2^{15}/2^{16}) \times I_{REF}$	Midscale
8000	$8 \times (2^{15} - 1)/2^{16} \times I_{REF}$	Midscale − 1 LSB
FFFF	0	Zero Scale

Since the DAC16 exhibits a small output voltage compliance on the order of a few millivolts, a high accuracy operational amplifier must be used to convert the DAC's output current to a voltage. Refer to the section on selecting operation amplifiers for the DAC16. The circuit shown in Figure 24 illustrates a unipolar output configuration. In symbolic form, the transfer equation for this circuit can be expressed by:

$$V_O = R3 \times 8 \times I_{REF} \left[\frac{65{,}535 - Digital\ Code}{65{,}536}\right]$$

In this example, the reference input current was set to 500 μA which produces a full-scale output current of 4 mA − 1 LSB. The DAC's output current was scaled by R3, a 1.25 kΩ resistor, to produce a 5 V full-scale output voltage. Bear in mind that to ensure the highest possible accuracy, matched thin-film resistor networks are almost a necessity, not an option. The resistors used in the circuit must have close tolerance and tight thermal tracking. Table III illustrates the relationship between the input digital code and the circuit's output voltage for the component values shown.

Table III. Unipolar Output Voltage vs. Digital Input Code

Digital Input Word (Hex)	Decimal Number in in DAC Decoder	Analog Output Voltage (V)
0000	65,535	4.999924
7FFE	32,769	2.500076
7FFF	32,768	2.500000
8000	32,767	2.499924
FFFF	0	0

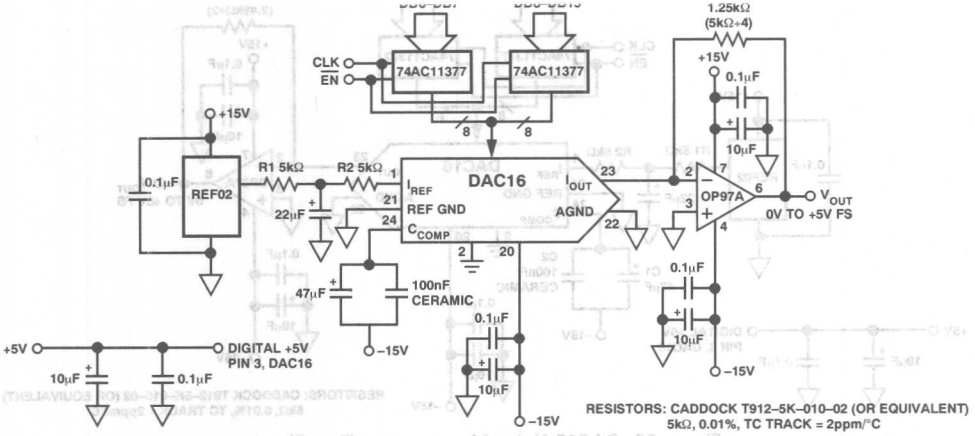


Figure 24. Unipolar Circuit Configuration

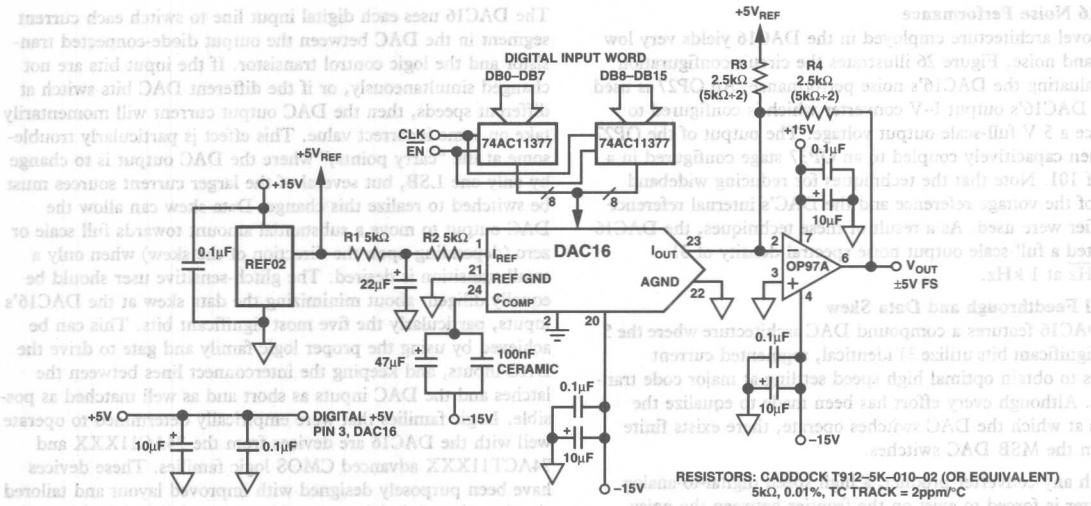


Figure 25. Bipolar Circuit Configuration

Bipolar Configuration

For applications that require a bipolar output voltage, the circuit in Figure 24 can be modified slightly by adding a resistor from the reference to the inverting sum node of the output amplifier to level shift the output signal. The transfer equation for the circuit now becomes:

$$V_O = R4 \times 8 \times I_{REF}\left[\frac{65{,}535 - Digital\ Code}{65{,}536}\right] - V_{REF} \times \left(\frac{R4}{R3}\right)$$

The circuit has the form shown in Figure 25, and Table IV provides the relationship between the digital input code and the circuit's output voltage for the component values shown.

Table IV. Bipolar Output Operation vs. Digital Input Code

Digital Input Word (Hex)	Decimal Number in DAC Decoder	Analog Output Voltage (V)
0000	65,535	4.999848
7FFE	32,769	152E-6
7FFF	32,768	0
8000	32,767	−152E-6
FFFF	0	−5.00000

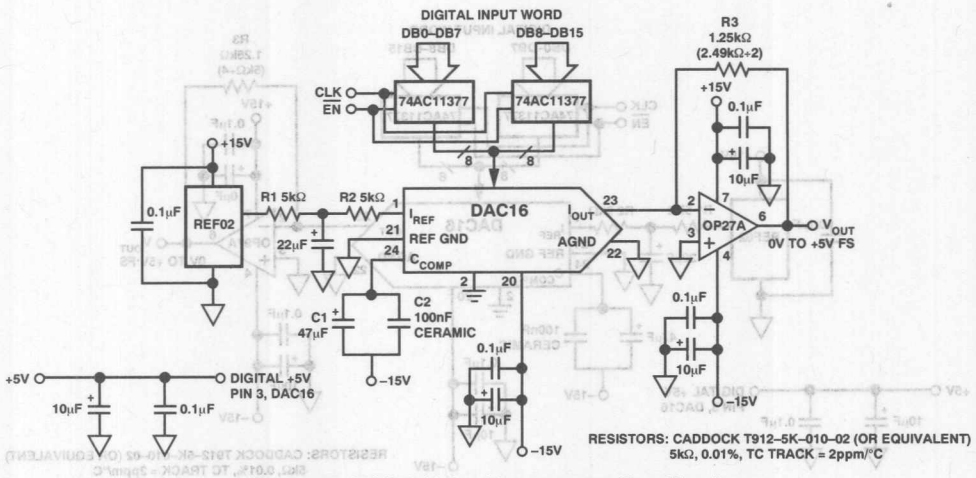


Figure 26. DAC16 Noise Measurement Test Circuit

DAC16 Noise Performance

The novel architecture employed in the DAC16 yields very low wideband noise. Figure 26 illustrates the circuit configuration for evaluating the DAC16's noise performance. An OP27 is used as the DAC16's output I–V converter which is configured to produce a 5 V full-scale output voltage. The output of the OP27 was then capacitively coupled to an OP37 stage configured in a gain of 101. Note that the techniques for reducing wideband noise of the voltage reference and the DAC's internal reference amplifier were used. As a result of these techniques, the DAC16 exhibited a full-scale output noise spectral density of 31 pA/$\sqrt{\text{Hz}}$ at 1 kHz.

Digital Feedthrough and Data Skew

The DAC16 features a compound DAC architecture where the 5 most significant bits utilize 31 identical, segmented current sources to obtain optimal high speed settling at major code transitions. Although every effort has been made to equalize the speeds at which the DAC switches operate, there exists finite skew in the MSB DAC switches.

As with any converter product, a high speed digital-to-analog converter is forced to exist on the frontier between the noisy environment of high speed digital logic and the sensitive analog domain. The problems of this interface are particularly acute when demands of high speed (greater than 10 MHz switching times) and high precision are combined. No amount of design effort can perfectly isolate the analog portions of a DAC from the spectral components of a digital input signal with a 2 ns rise time. Inevitably, once this digital signal is brought onto the chip, some of its higher frequency components will find their way to the sensitive analog nodes, producing a digital feedthrough glitch. To minimize the exposure to this effect, the DAC16 was designed to omit intentionally the on-board latches that are usually included in many slower DACs. This not only reduces the overall level of digital activity on chip, it also avoids bringing a latch clock pulse onto the IC, whose opposite edge inevitably produces a substantial glitch, even when the DAC is not supposed to be changing codes.

The DAC16 uses each digital input line to switch each current segment in the DAC between the output diode-connected transistor and the logic control transistor. If the input bits are not changed simultaneously, or if the different DAC bits switch at different speeds, then the DAC output current will momentarily take on some incorrect value. This effect is particularly troublesome at the "carry points," where the DAC output is to change by only one LSB, but several of the larger current sources must be switched to realize this change. Data skew can allow the DAC output to move a substantial amount towards full scale or zero (depending upon the direction of the skew) when only a small transition is desired. The glitch-sensitive user should be equally diligent about minimizing the data skew at the DAC16's inputs, particularly the five most significant bits. This can be achieved by using the proper logic family and gate to drive the DAC inputs, and keeping the interconnect lines between the latches and the DAC inputs as short and as well matched as possible. Logic families that were empirically determined to operate well with the DAC16 are devices from the 74AC11XXX and 74ACT11XXX advanced CMOS logic families. These devices have been purposely designed with improved layout and tailored rise times for minimizing ground bounce and digital feedthrough.

Deglitching

The output glitch of the DAC16 at the major carry ($7FFE_H$ to $7FFF_H$) is a not-insignificant 360 pA-sec, manifested as a momentary output transition to the negative rail for approximately 200 ns. Due to the inherent low-pass or time-sampled nature of many systems, this behavior in the DAC16 is not noticeable and does not detract from overall performance. Some applications however may prove so sensitive to glitch impulse that reduction by an order of magnitude or more is required. In order to realize low glitch impulses, some sort of sample-and-hold amplifier-based deglitching scheme must be used.

There are high speed SHAs available with specifications sufficient to deglitch the DAC16; however, most are hybrid in topology at costs which can be prohibitive. A high performance, low cost alternative shown in Figure 27 is a discrete SHA utilizing a high speed monolithic op amp and high speed DMOS FET switches.

This SHA circuit uses the inverting integrator structure. A 300 MHz gain-bandwidth product op amp, the AD841, is the heart of this fast SHA. The time constant formed by the 200 Ω resistor and the 100 pF capacitor determines the acquisition time and also band limits the output signal to eliminate slew-induced distortion.

A discrete drive circuit is used to achieve the best performance from the SD5000 quad DMOS switch. This switch-driving cell is composed of MPS571 RF NPN transistors and an MC10124 TTL-to-ECL translator. Using this technique provides both high speed and highly symmetrical drive signals for the SD5000 switches. The switches are arranged in a single-pole, double-throw (SPDT) configuration. The 500 pF "flyback" capacitor is switched to the op amp summing junction during the hold mode to keep switching transients from feeding to the output. This capacitor is grounded during sample mode to minimize its effect on acquisition time.

Careful circuit layout of the high speed SHA section is almost as important as the design itself. Double-sided printed circuit board, a compact layout, and short critical signal paths all ensure best performance.

Op Amp Selection

When selecting the amplifier to be used for the DAC16's I–V converter, there are two main application areas; those requiring high accuracy, and those seeking high speed. In high accuracy applications, three parameters are of prime importance: (1) input offset voltage, V_{OS}; (2) input bias current, $-I_B$; and (3) offset voltage drift, TCV_{OS}. In these applications where 16-bit performance must be maintained with an external reference at +5 V, an op amp's input offset voltage must be less than 15 μV (≈0.1 LSB) with a bias current less than 6 nA. The op amp must also exhibit high open-loop gain to keep the offset voltage below this limit over the specified full-scale output range. Thus, for an maximum output of 5 V, the op amp's open loop gain must be greater than 1300 V/mV.

For low frequency, high accuracy applications, Table IV lists selected compatible operational amplifiers available from Analog Devices. These operational amplifiers satisfy all the above requirements and in most all cases will not require offset voltage nulling.

Table V. Precision Operational Amplifiers for the DAC16

Model	V_{OS}	TCV_{OS}	I_B	A_{VOL}
OP177	10 μV	0.3 μV/°C	2 nA	12000 V/mV
OP77	25 μV	0.6 μV/°C	2.8 nA	2000 V/mV
OP27	25 μV	0.2 μV/°C	80 nA	1500 V/mV
OP97	25 μV	2 μV/°C	0.15 nA	2000 V/mV

In high speed applications where resolution is more important than absolute accuracy, operational amplifiers such as the AD843 offer the requisite settling time. Although these amplifiers are not specified for 16-bit performance, their settling times are two to three times faster than the DAC16 and will introduce negligible error to the overall circuit's settling time. It is possible to estimate the 16-bit settling time of an operational amplifier if its 12-bit settling time is known. Assuming that the op amp can be modeled by a single-pole response, then the ratio of the op amp's 16-bit settling time to its 12-bit settling can be expressed as:

$$\frac{t_S\ (16\text{-}bit)}{t_S\ (12\text{-}bit)} = 1.33$$

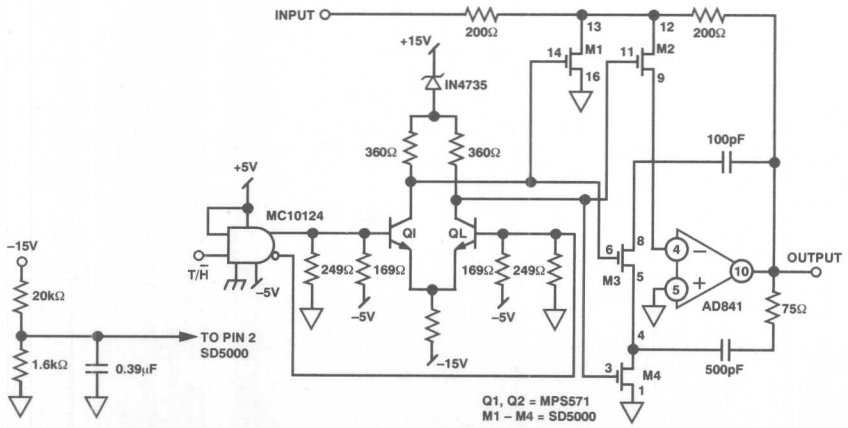


Figure 27. A High Performance Deglitching Circuit

Since many operational amplifier data sheets provide charts illustrating 0.01% settling time versus output voltage step size, all that is required to estimate an op amp's 16-bit settling time is to multiply the 12-bit settling time for the required full-scale voltage by 1.33. The circuit's overall settling time can then be approximated by the root-sum-square method:

$$t_S = \sqrt{(t_{DAC})^2 + (t_{OA})^2}$$

where

t_{DAC} = DAC16's specified full-scale settling time

t_{OA} = Op amp full-scale settling time

As a design aid, Table VI illustrates a high speed operational amplifier selector guide for devices compatible with the DAC16 for high speed applications. All these devices exhibit the requisite settling time, input offset voltage, and input bias current consistent with maximum performance.

Table VI. High Speed Operational Amplifiers for the DAC16

Model	t_S to %	V_{OS}	TCV_{OS}	I_B	A_{VOL}
OP467	200 ns −0.01	0.5 mV	3.5 μV/°C	0.5 μA	20 V/mV
AD817	70 ns −0.01	2 mV	10 μV/°C	6.6 μA	6 V/mV
AD829	90 ns −0.1	0.5 mV	0.3 μV/°C	7 μA	100 V/mV
AD841	110 ns −0.01	1 mV	35 μV/°C	5 μA	45 V/mV
AD843	135 ns −0.01	1 mV	12 μV/°C	0.001 μA	25 V/mV
AD845	350 ns −0.01	0.25 mV	5 μV/°C	0.001 μA	500 V/mV
AD847	120 ns −0.01	1 mV	15 μV/°C	5 μA	5.5 V/mV

In using high speed op amps, the output capacitance of the DAC16 appears across the inputs of the op amp where it and the op amp's input capacitance will set an additional pole in the op amp's loop gain response. The pole is formed with the feedback resistance and the output resistance of the DAC. This additional pole may adversely affect the transient response of the circuit due to the added phase shift. Placing a small capacitor across the feedback resistance, as shown in Figure 28, compensates for the additional pole. The value of the capacitor can be determined by setting $R_{FB}C_{FB} = R_O (C_O + C_{IN})$ and should be adjusted for optimum transient response.

The choice of amplifier depends entirely on the required system accuracy, the required temperature range, and the operating frequency.

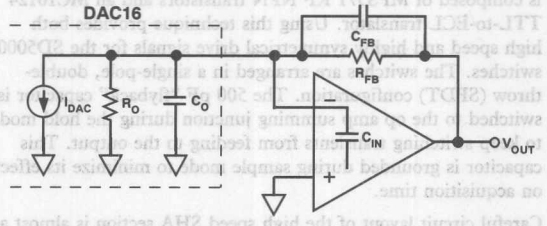
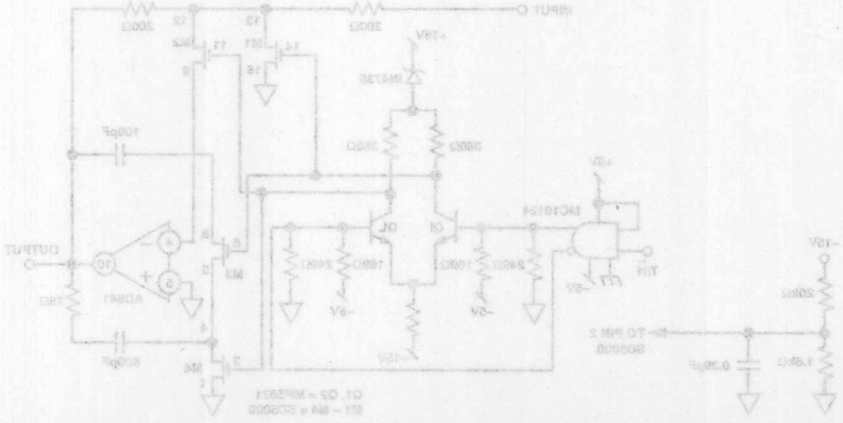


Figure 28. Compensating for the Feedback Pole



12-Bit High Speed Multiplying D/A Converter

DAC312

FEATURES

- Differential Nonlinearity ..... ±1/2LSB
- Nonlinearity 0.05%
- Fast Settling Time 250ns
- High Compliance ..... −5V to +10V
- Differential Outputs ..... 0 to 4mA
- Guaranteed Monotonicity ..... 12 Bits
- Low Full-Scale Tempco ..... 10ppm/°C
- Circuit Interface to TTL, CMOS, ECL, PMOS/NMOS
- Low Power Consumption 225mW
- Industry Standard AM6012 Pinout
- Available in Die Form

ORDERING INFORMATION †

DNL	PACKAGE: CERDIP 20-PIN	PACKAGE: PLASTIC 20-PIN	OPERATING TEMPERATURE RANGE
±1/2LSB	DAC312ER*	–	COM
±1LSB	DAC312FR	–	XIND
±1LSB	DAC312HR	–	XIND
±1LSB	–	DAC312HP	XIND
±1LSB	–	DAC312HS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

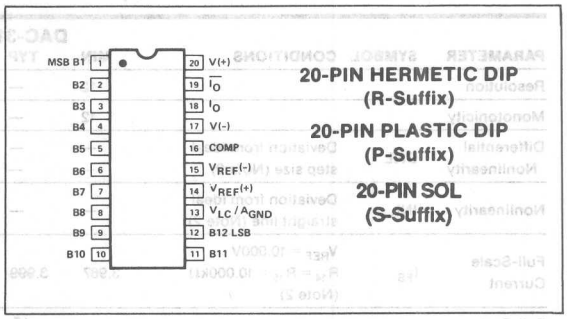
GENERAL DESCRIPTION

The DAC-312 series of 12-bit multiplying digital-to-analog converters provide high speed with guaranteed performance to 0.012% differential nonlinearity over the full commercial operating temperature range.

Based on the segmented design approach pioneered by PMI with the COMDAC® line of data converters, the DAC-312 combines a 9-bit master D/A converter with a 3-bit (MSB's) segment generator to form an accurate 12-bit D/A converter at low cost. This technique guarantees a very uniform step size (up to ±1/2 LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs. In order to provide the same performance with a 12-bit R-2R ladder design, an integral nonlinearity over temperature of 1/2 LSB (0.012%) would be required.

The 250ns settling time with low glitch energy and low power consumption are achieved by careful attention to the circuit design and stringent process controls. Direct interface with all popular logic families is achieved through the logic threshold terminal.

PIN CONNECTIONS

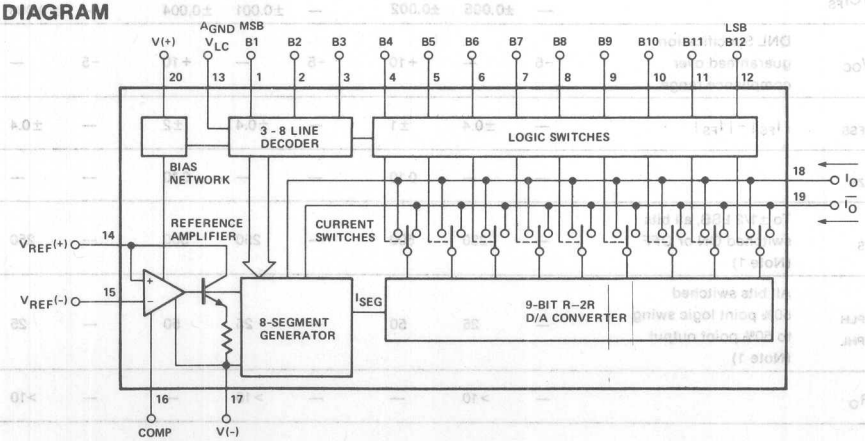


20-PIN HERMETIC DIP (R-Suffix)

20-PIN PLASTIC DIP (P-Suffix)

20-PIN SOL (S-Suffix)

FUNCTIONAL DIAGRAM



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

excellent power supply rejection ratio of ±.001% FS/%ΔV. Operating over a power supply range of +5/−11V to ±18V the device consumes 225mW at the lower supply voltages with an absolute maximum dissipation of 375mW at the higher supply levels.

With their guaranteed specifications, single chip reliability and low cost, the DAC-312 device makes excellent building blocks for A/D converters, data acquisition systems, video display drivers, programmable test equipment and other applications where low power consumption and complete input/output versatility are required.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature
DAC-312E ..... 0°C to +70°C
DAC-312F, DAC-312H ..... −40°C to +85°C
Junction Temperature ..... −65°C to +150°C
Storage Temperature (T_j) ..... −65°C to +125°C
Power Supply Voltage ..... ±18V
Logic Inputs ..... −5V to +18V
Analog Current Outputs ..... −8V to +12V
Reference Inputs V_{14}, V_{15} ..... V− to V+
Reference Input Differential Voltage (V_{14}, V_{15}) ..... ±18V
Reference Input Current (I_{14}) 1.25mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

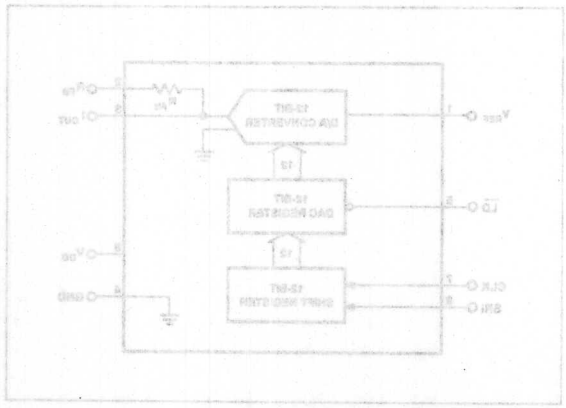
ELECTRICAL CHARACTERISTICS at V_S = ±15V, I_{REF} = 1.0mA, 0°C ≤ T_A ≤ 70°C for DAC-312E and −40°C ≤ T_A ≤ +85°C for DAC-312F, DAC-312H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

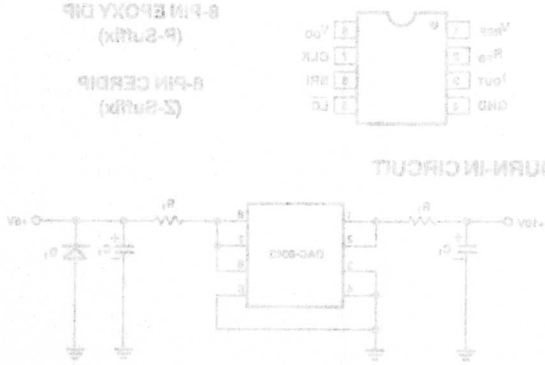
			DAC-312E			DAC-312F			DAC-312H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution			12	—	—	12	—	—	12	—	—	Bits
Monotonicity			12	—	—	12	—	—	12	—	—	Bits
Differential Nonlinearity	DNL	Deviation from ideal step size (Note 2)	—	—	±0.0125	—	—	±0.0250	—	—	±0.0250	%FS
			—	—	±0.5	—	—	±1	—	—	±1	LSB
Nonlinearity	INL	Deviation from ideal straight line (Note 2)	—	—	±0.05	—	—	±0.05	—	—	±0.05	%FS
Full-Scale Current	I_{FS}	V_{REF} = 10.000V $R_{14} = R_{15}$ = 10.000kΩ (Note 2)	3.967	3.999	4.031	3.935	3.999	4.063	3.935	3.999	4.063	mA
Full-Scale Tempco	TCI_{FS}		—	±5	±20	—	±10	±40	—	±80	—	ppm/°C
			—	±0.005	±0.002	—	±0.001	±0.004	—	±0.008	—	%FS/°C
Output Voltage Compliance	V_{OC}	DNL Specification guaranteed over compliance range	−5	—	+10	−5	—	+10	−5	—	+10	V
Full-Scale Symmetry	I_{FSS}	$\lvert I_{FS} \rvert - \lvert I_{FS} \rvert$	—	±0.4	±1	—	±0.4	±2	—	±0.4	±2	μA
Zero-Scale Current	I_{ZS}		—	—	0.10	—	—	0.10	—	—	0.10	μA
Settling Time	t_S	To ±1/2 LSB, all bits switched ON or OFF (Note 1)	—	250	500	—	250	500	—	250	500	ns
Propagation Delay — all bits	t_{PLH} t_{PHL}	All bits switched 50% point logic swing to 50% point output (Note 1)	—	25	50	—	25	50	—	25	50	ns
Output Resistance	R_O		—	>10	—	—	>10	—	—	>10	—	MΩ
Output Capacitance	C_{OUT}		—	20	—	—	20	—	—	20	—	pF

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 1.0mA$, $0°C \le T_A \le 70°C$ for DAC-312E and $-40°C \le T_A \le +85°C$ for DAC-312F, DAC-312H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-312E MIN	DAC-312E TYP	DAC-312E MAX	DAC-312F MIN	DAC-312F TYP	DAC-312F MAX	DAC-312H MIN	DAC-312H TYP	DAC-312H MAX	UNITS
Logic Input Levels "0"	V_{IL}	V_{LC} = GND	—	—	0.8	—	—	0.8	—	—	0.8	V
Logic Input Levels "1"	V_{IH}	V_{LC} = GND	2	—	—	2	—	—	2	—	—	V
Logic Input Current	I_{IN}	V_{IN} = −5 to +18V	—	—	40	—	—	40	—	—	40	μA
Logic Input Swing	V_{IS}		−5	—	+18	−5	—	+18	−5	—	+18	V
Reference Bias Current	I_{15}		0	−0.5	−2	0	−0.5	−2	0	−0.5	−2	μA
Reference Input Slew Rate	dI/dt	$R_{14(eq)} = 800\Omega$, C_C = 0pF (Note 1)	4	8	—	4	8	—	4	8	—	mA/μs
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = +13.5V to +16.5V, V− = −15V	—	±0.0005	±0.001	—	±0.0005	±0.001	—	±0.0005	±0.001	%FS/%ΔV
	$PSSI_{FS-}$	V− = −13.5V to −16.5V, V+ = +15V	—	±0.00025	±0.001	—	±0.00025	±0.001	—	±0.00025	±0.001	
Power Supply Range	V+	V_{OUT} = 0V	4.5	—	18	4.5	—	18	4.5	—	18	V
	V−		−18	—	−10.8	−18	—	−10.8	−18	—	−10.8	
Power Supply Current	I+	V+ = +5V, V− = −15V	—	3.3	7	—	3.3	7	—	3.3	7	mA
	I−		—	−13.9	−18	—	−13.9	−18	—	−13.9	−18	
	I+	V+ = +15V, V− = −15V	—	3.9	7	—	3.9	7	—	3.9	7	
	I−		—	−13.9	−18	—	−13.9	−18	—	−13.9	−18	
Power Dissipation	P_d	V+ = +5V, V− = −15V	—	225	305	—	225	305	—	225	305	mW
		V+ = +15V, V− = −15V	—	267	375	—	267	375	—	267	375	

NOTES:
1. Guaranteed by design.
2. T_A = 25°C for DAC-312H grade only.





12-Bit Serial Input Multiplying CMOS D/A Converter

DAC8043

FEATURES

- 12-Bit Accuracy in an 8-Pin Mini-Dip
- Fast Serial Data Input
- Double Data Buffers
- Low ±1/2 LSB Max INL and DNL
- Max Gain Error: ±1 LSB
- Low 5ppm/°C Max Tempco
- ESD Resistant
- Low Cost
- Available in Die Form

APPLICATIONS

- Auto-Calibration Systems
- Process Control and Industrial Automation
- Programmable Amplifiers and Attenuators
- Digitally-Controlled Filters

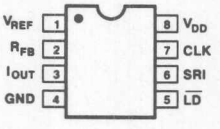
ORDERING INFORMATION†

	PACKAGE		
RELATIVE ACCURACY	MILITARY* TEMPERATURE –55°C TO +125°C	EXTENDED INDUSTRIAL TEMPERATURE –40°C TO +85°C	COMMERCIAL TEMPERATURE 0°C TO +70°C
±1/2 LSB	DAC8043AZ	DAC8043EZ	DAC8043GP
±1/2 LSB	DAC8043AZ/883	–	–
±1 LSB	–	DAC8043FZ	–
±1 LSB	–	DAC8043FP	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in.

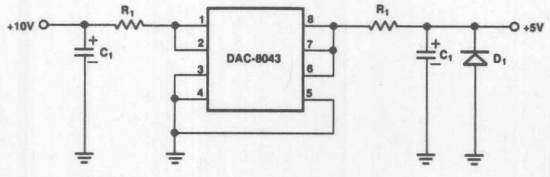
PIN CONNECTIONS



8-PIN EPOXY DIP
(P-Suffix)

8-PIN CERDIP
(Z-Suffix)

BURN-IN CIRCUIT



NOTES:
R_1 = 10Ω
C_1 = 10μF
D_1 = 1N4001 OR EQUIVALENT
MAXIMUM POWER SUPPLY CURRENT PER DEVICE IS +1.5mA, –0mA
POWER-UP SEQUENCE: +5V, +10V
POWER-DOWN SEQUENCE: +10V, +5V

GENERAL DESCRIPTION

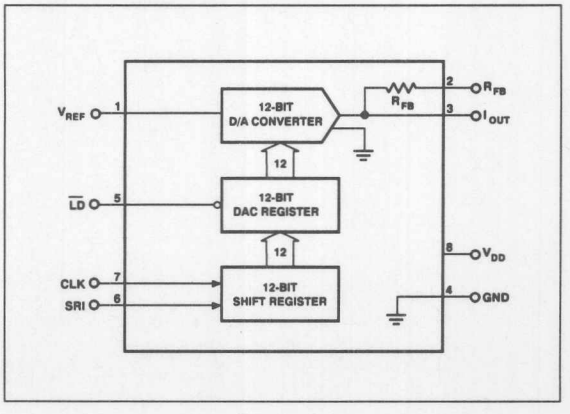
The DAC-8043 is a high accuracy 12-bit CMOS multiplying DAC in a space-saving 8-pin mini-DIP package. Featuring serial data input, double buffering, and excellent analog performance, the DAC-8043 is ideal for applications where PC board space is at a premium. Also, improved linearity and gain error performance permit reduced parts count through the elimination of trimming components. Separate input clock and load-DAC control lines allow full user control of data loading and analog output.

The circuit consists of a 12-bit serial-in, parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial data is clocked into the input register on the rising edge of the CLOCK pulse. When the new data word has been clocked in, it is loaded into the DAC register with the $\overline{LD}$ input pin. Data in the DAC register is converted to an output current by the D/A converter.

The DAC-8043's fast interface timing may reduce timing design considerations while minimizing microprocessor wait states. For applications requiring an asynchronous CLEAR function or more versatile microprocessor interface logic, refer to the PM-7543.

Operating from a single +5V power supply, the DAC-8043 is the ideal low power, small size, high performance solution to many application problems. It is available in plastic and cerdip packages that are compatible with auto-insertion equipment.

FUNCTIONAL BLOCK DIAGRAM



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted.)

V_{DD} to GND ..... +17V
V_{REF} to GND ..... ±25V
V_{RFB} to GND ..... ±25V
Digital Input Voltage Range ..... –0.3V to V_{DD}
Output Voltage (Pin 3) ..... –0.3V to V_{DD}
Operating Temperature Range
AZ Versions ..... –55°C to +125°C
EZ/FZ/FP Versions ..... –40°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 1) and R_{FB} (Pin 2).
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

3

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; I_{OUT} = GND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8043 MIN	DAC-8043 TYP	DAC-8043 MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	–	–	Bits
Nonlinearity	INL	DAC-8043A/E/G	–	–	±1/2	LSB
(Note 1)		DAC-8043F	–	–	1	
Differential Nonlinearity	DNL	DAC-8043A/E	–	–	±1/2	LSB
(Note 2)		DAC-8043F/G	–	–	±1	
Gain Error (Note 3)	G_{FSE}	T_A = +25°C DAC-8043A/E	–	–	1	LSB
		DAC-8043F/G	–	–	2	
		T_A = Full Temperature Range All Grades	–	–	2	
Gain Tempco (Δ Gain/Δ Temp) (Note 5)	TC_{GFS}		–	–	±5	ppm/°C
Power Supply Rejection Ratio (Δ Gain/Δ V_{DD})	PSRR	Δ V_{DD} = ±5%	–	±0.0006	±0.002	%/%
Output Leakage Current (Note 4)	I_{LKG}	T_A = +25°C	–	–	±5	nA
		T_A = Full Temperature Range DAC-8043A	–	–	±100	
		DAC-8043E/F/G	–	–	±25	
Zero Scale Error (Notes 7, 12)	I_{ZSE}	T_A = +25°C	–	–	0.03	LSB
		T_A = Full Temperature Range DAC-8043A	–	–	0.61	
		DAC-8043E/F/G	–	–	0.15	
Input Resistance (Note 8)	R_{IN}		7	11	15	kΩ
AC PERFORMANCE						
Output Current Settling Time (Notes 5, 6)	t_S	T_A = +25°C	–	0.25	1	µs

Absolute Maximum Ratings unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8043 MIN	TYP	MAX	UNITS
Digital to Analog Glitch Energy (Note 5,10)	Q	V_{REF} = 0V I_{OUT} Load = 100Ω C_{EXT} = 13pF DAC register loaded alternately with all 0s and all 1s	–	2	20	nVs
Feedthrough Error (V_{REF} to I_{OUT}) (Note 5, 11)	FT	V_{REF} = $20V_{p-p}$ @ f = 10kHz Digital Input = 0000 0000 0000 T_A = +25°C	–	0.7	1	mV_{p-p}
Total Harmonic Distortion (Note 5)	THD	V_{REF} = 6V RMS @ 1kHz DAC register loaded with all 1s	–	–85	–	dB
Output Noise Voltage Density (Notes 5, 13)	e_n	10Hz to 100kHz between R_{FB} and I_{OUT}	–	–	17	$nV/\sqrt{Hz}$
DIGITAL INPUTS						
Digital Input HIGH	V_{IH}		2.4	–	–	V
Digital Input LOW	V_{IL}		–	–	0.8	V
Input Leakage Current (Note 9)	I_{IL}	V_{IN} = 0V to +5V	–	–	±1	µA
Input Capacitance (Note 5, 11)	C_{IN}	V_{IN} = 0V	–	–	8	pF
ANALOG OUTPUTS						
Output Capacitance (Note 5)	C_{OUT}	Digital Inputs = V_{IH}	–	–	110	pF
		Digital Inputs = V_{IL}	–	–	80	
TIMING CHARACTERISTICS (NOTES 5, 14)						
Data Setup Time	t_{DS}	T_A = Full Temperature Range	40	–	–	ns
Data Hold Time	t_{DH}	T_A = Full Temperature Range	80	–	–	ns
Clock Pulse Width High	t_{CH}	T_A = Full Temperature Range	90	–	–	ns
Clock Pulse Width Low	t_{CL}	T_A = Full Temperature Range	120	–	–	ns
Load Pulse Width	t_{LD}	T_A = Full Temperature Range	120	–	–	ns
LSB Clock Into Input Register to Load DAC Register Time	t_{ASB}	T_A = Full Temperature Range	0	–	–	ns
POWER SUPPLY						
Supply Voltage	V_{DD}		4.75	5	5.25	V
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}	–	–	500	µA MAX
		Digital Inputs = 0V or V_{DD}	–	–	100	

NOTES:

1. ±1/2 LSB = ±0.012% of Full Scale.
2. All grades are monotonic to 12-bits over temperature.
3. Using internal feedback resistor.
4. Applies to I_{OUT}; All digital inputs = 0V.
5. Guaranteed by design and not tested.
6. I_{OUT} Load = 100Ω, C_{EXT} = 13pF, digital input = 0V to V_{DD} or V_{DD} to 0V. Extrapolated to 1/2 LSB: t_S = propagation delay (t_{PD}) + 9τ where τ = measured time constant of the final RC decay.
7. V_{REF} = +10V, all digital inputs = 0V.
8. Absolute temperature coefficient is less than +300ppm/°C.
9. Digital inputs are CMOS gates; I_{IN} is typically 1nA at +25°C.
10. V_{REF} = 0V, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
11. All digital inputs = 0V.
12. Calculated from worst case R_{REF}:
    I_{ZSE} (in LSBs) = $(R_{REF} \times I_{LKG} \times 4096)/V_{REF}$.
13. Calculations from en = $\sqrt{4KTRB}$ where:
    K = Boltzmann constant, J/°K, R = resistance, Ω
    T = resistor temperature, °K, B = bandwidth, Hz
14. Tested at V_{IN} = 0V or V_{DD}.

Dual 12-Bit Buffered Multiplying CMOS D/A Converter

DAC8221

FEATURES

- Two Matched 12-Bit DACs on One Chip
- Packaged in a Narrow 0.3" 24-Pin DIP
- Direct Parallel Load of All 12 Bits for High DataThroughput
- On-Chip Latches for Both DACs
- 12-Bit Endpont Linearity (±1/2 LSB) Over Temperature
- +5V to +15V Single Supply Operation
- DACs Matched to 0.2% Typically
- Four-Quadrant Multiplication
- Improved ESD Resistance
- Available in Die Form

APPLICATIONS

- Automatic Test Equipment
- Industrial Automation
- Robotics/Process Control
- Programmable Instrumentation Equipment
- Digital Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

ORDERING INFORMATION †

RELATIVE ACCURACY (+5V or +15V)	GAIN ERROR	PACKAGE MILITARY* TEMPERATURE –55°C to +125°C	PACKAGE INDUSTRIAL TEMPERATURE –40°C to +85°C	PACKAGE COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±1 LSB	DAC8221AW	DAC8221EW	–
±1/2 LSB	±2 LSB	–	–	DAC8221GP
±1 LSB	±4 LSB	–	DAC8221FW	DAC8221HP
±1 LSB	±4 LSB	–	DAC8221FP	DAC8221HS††

* For devices processed in total compliance to MIL-SDT-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

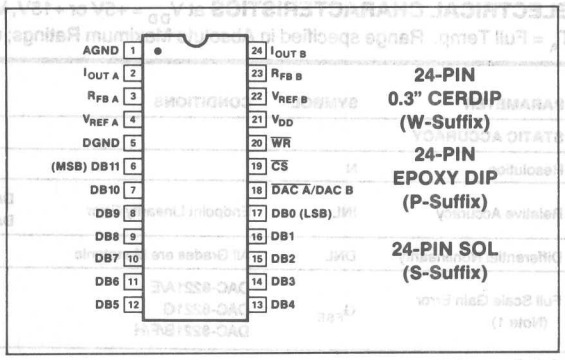
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

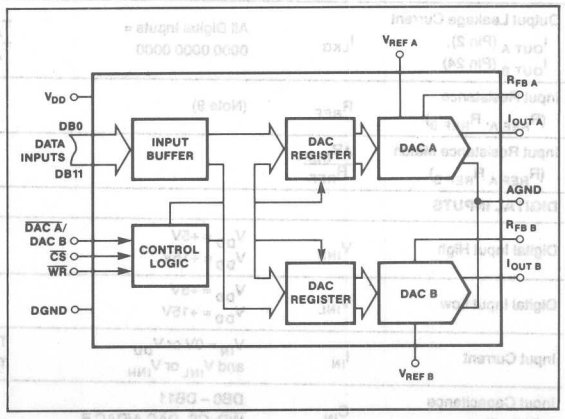
The DAC-8221 combines two identical 12-bit, multiplying, digital-to-analog converters into a single CMOS chip. This device is electrically similar to DAC-8212 with improved microprocessor interface timing and is packaged in a narrow 0.300" DIP. Monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The DAC-8221 consists of two thin-film R-2R resistor-ladder networks, two 12-bit data latches, one 12-bit input buffer, and control logic. The DAC-8221 operates on a single supply from +5V to +15V. Maximum power dissipation with 0V and +5V logic levels and a +5V supply is less than 0.5mW. The DAC-8221 is manufactured using PMI's highly-stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

A common 12-bit (TTL/CMOS compatible) input port is used to load a 12-bit-wide word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit or wider bus systems. With $\overline{WR}$ and $\overline{CS}$ lines at logic LOW, the input data registers are transparent. This allows direct unbuffered data to flow directly to the DAC output selected by $\overline{DAC\ A}$/DAC B control input. For applications requiring double-buffering, see the DAC-8222.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... –0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND ..... –0.3V, V_{DD} +0.3V
$I_{OUT\ A}$, $I_{OUT\ B}$ to AGND ..... –0.3V, V_{DD} +0.3V
$V_{REF\ A}$, $V_{REF\ B}$ to AGND ..... ±25V
$V_{RFB\ A}$, $V_{RFB\ B}$ to AGND ..... ±25V
Operating Temperature Range
AW Version ..... –55°C to +125°C
EW, FW, FP Versions ..... –40°C to +85°C
GP, HP, HS Versions ..... –0°C to +70°C
Junction Temperature ..... +150C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
24-Pin Hermetic DIP (W)	69	10	°C/W
24-Pin Plastic DIP (P)	62	32	°C/W
24-Pin SOL (S)	72	24	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:
1. Do no apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF\ A}$ = $V_{REF\ B}$ = +10V, $V_{OUT\ A}$ = $V_{OUT\ B}$ = 0V; AGND = DGND = 0V; T_A = Full Temp. Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.

PARAMETER	SYMBOL	CONDITIONS		DAC-8221 MIN	DAC-8221 TYP	DAC-8221 MAX	UNITS
STATIC ACCURACY							
Resolution	N			12	–	–	Bits
Relative Accuracy	INL	Endpoint Linearity Error	DAC-8221A/E/G	–	±0.2	±1/2	LSB
			DAC-8221B/F/H	–	±0.4	±1	
Differential Nonlinearity	DNL	All Grades are Monotonic		–	±0.2	±1	LSB
Full Scale Gain Error (Note 1)	G_{FSE}	DAC-8221A/E		–	±0.1	±1	LSB
		DAC-8221G		–	±0.4	±2	
		DAC-8221B/F/H		–	±0.6	±4	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG_{FS}	(Notes 2, 7)		–	±2	±5	ppm/°C
Output Leakage Current $I_{OUT\ A}$ (Pin 2), $I_{OUT\ B}$ (Pin 24)	I_{LKG}	All Digital Inputs = 0000 0000 0000	T_A = +25°C	–	±1	±10	nA
			T_A = Full Temp. Range	–	±2	±50	
Input Resistance ($R_{REF\ A}$, $R_{REF\ B}$)	R_{REF}	(Note 9)		8	22	15	kΩ
Input Resistance Match ($R_{REF\ A}$ $R_{REF\ B}$)	$\frac{\Delta R_{REF}}{R_{REF}}$			–	±0.2	±1	%
DIGITAL INPUTS							
Digital Input High	V_{INH}	V_{DD} = +5V		2.4	–	–	V
		V_{DD} = +15V		13.5	–	–	
Digital Input Low	V_{INL}	V_{DD} = +5V		–	–	0.8	V
		V_{DD} = +15V		–	–	1.5	
Input Current	I_{IN}	V_{IN} = 0V or V_{DD} and V_{INL} or V_{INH}	T_A = +25°C	–	±0.006	±1	μA
			T_A = Full Temp. Range	–	±0.1	±10	
Input Capacitance (Note 2)	C_{IN}	DB0 – DB11		–	–	10	pF
		WR, CS, DAC A/DAC B		–	–	15	

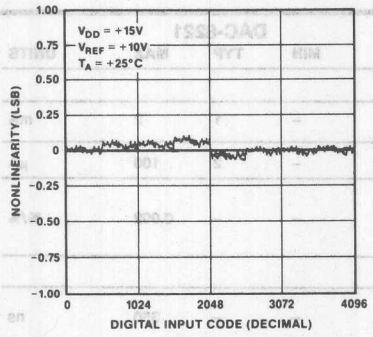
ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF\,A}$ = $V_{REF\,B}$ = +10V, $V_{OUT\,A}$ = $V_{OUT\,B}$ = 0V; AGND = DGND = 0V; T_A = Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.
Continued

PARAMETER	SYMBOL	CONDITIONS	DAC-8221 MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	–	1	2	mA
		All Digital Inputs 0V or V_{DD}	–	2	100	µA
DC Power Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$)	PSRR	ΔV_{DD} = ±5%	–	–	0.002	%/%
AC PERFORMANCE CHARACTERISTICS (Note 2)						
Propagation Delay (Notes 4, 5)	t_{pd}	T_A = +25°C	–	–	350	ns
Current Settling Time (Notes 5, 6)	t_s	T_A = +25°C	–	0.45	1	µs
Output Capacitance	$C_{OUT\,A}$	DAC Latches Loaded with 0000 0000 0000	–	30	90	pF
	$C_{OUT\,B}$		–	60	120	
	$C_{OUT\,A}$	DAC Latches Loaded with 1111 1111 1111	–	60	120	
	$C_{OUT\,B}$		–	30	90	
AC Feedthrough at $I_{OUT\,A}$ or $I_{OUT\,B}$	FT_A	$V_{REF\,A}$ to $I_{OUT\,A}$; $V_{REF\,A}$ = $20V_{p-p}$; f = 100kHz; T_A = +25°C	–	–	–70	dB
	FT_B	$V_{REF\,B}$ to $I_{OUT\,B}$; $V_{REF\,B}$ = $20V_{p-p}$; f = 100kHz; T_A = +25°C	–	–	–70	

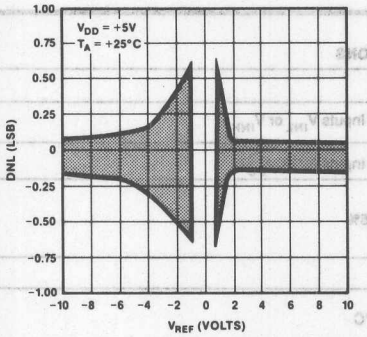
SWITCHING CHARACTERISTICS (Notes 2, 3)			V_{DD} = +5V +25°C	V_{DD} = +5V –40°C TO +85°C (Note 8)	V_{DD} = +5V –55°C TO +125°C	V_{DD} = +15V ALL TEMPS (Note 10)	
Chip Select to Write Set-Up Time	t_{CS}		130	160	160	70	ns MIN
Chip Select to Write Hold Time	t_{CH}		0	0	0	0	ns MIN
DAC Select to Write Set-Up Time	t_{AS}		120	140	160	70	ns MIN
DAC Select to Write Hold Time	t_{AH}		0	0	0	0	ns MIN
Data Valid to Write Set-Up Time	t_{DS}		190	210	220	90	ns MIN
Data Valid to Write Hold Time	t_{DH}		0	0	0	10	ns MIN
Write Pulse Width	t_{WR}		140	180	170	90	ns MIN

NOTES:
1. Measured using internal $R_{FB\,A}$ and $R_{FB\,B}$. Both DAC digital inputs = 1111 1111 1111.
2. Guaranteed and not tested.
3. See timing diagram.
4. From 50% of digital input to 90% of final analog output current. $V_{REF\,A}$ = $V_{REF\,B}$ = +10V; OUT A, OUT B load = 100Ω, C_{EXT} = 13pF.
5. $\overline{WR}$, $\overline{CS}$ = 0V; DB0 – DB11 = 0V to V_{DD} or V_{DD} to 0V.
6. Settling time is measured from 50% of the digital input change to where the output voltage settles within 1/2 LSB of full scale.
7. Gain TC is measured from +25°C to T_{MIN} or from +25°C to T_{MAX}.
8. These limits apply for the commercial and industrial grade products.
9. Absolute temperature coefficient is approximately +50ppm/°C.
10. These limits also apply as typical values for V_{DD} = +12V with +5V CMOS logic levels and T_A = +25°C.

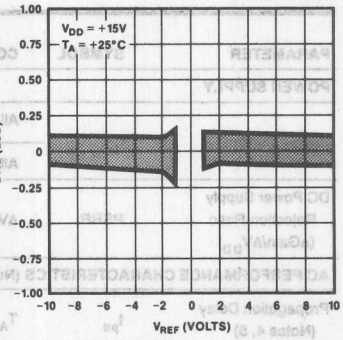
CHANNEL-TO-CHANNEL MATCHING (DAC A & B ARE SUPERIMPOSED)



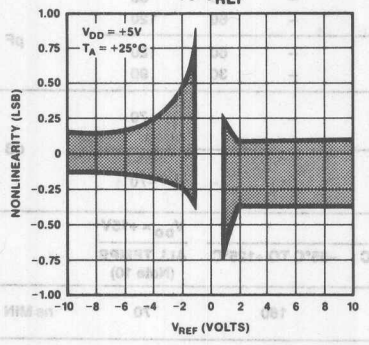
DIFFERENTIAL NONLINEARITY vs V_{REF}



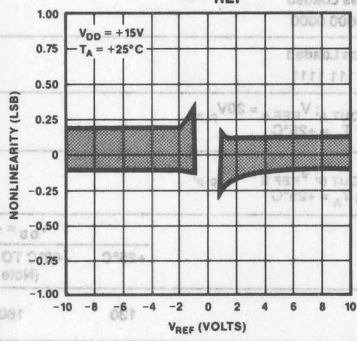
DIFFERENTIAL NONLINEARITY vs V_{REF}



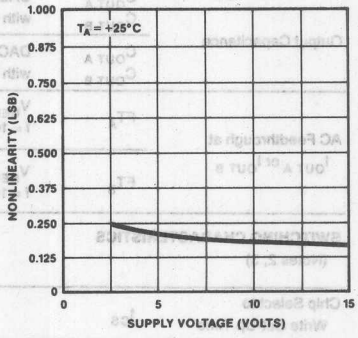
NONLINEARITY vs V_{REF}



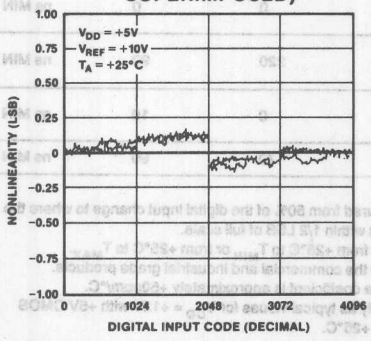
NONLINEARITY vs V_{REF}



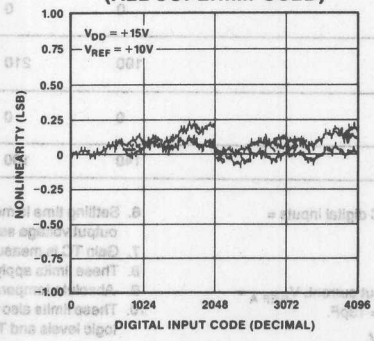
NONLINEARITY vs V_{DD}



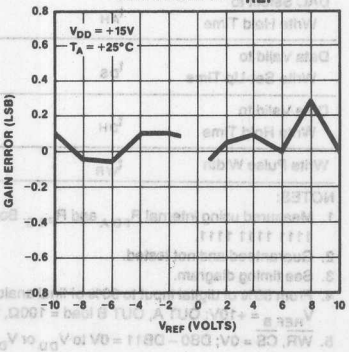
NONLINEARITY vs CODE (DAC A & B ARE SUPERIMPOSED)



NONLINEARITY vs CODE AT T_A = −55°C, +25°C, +125°C FOR DAC A & B (ALL SUPERIMPOSED)



ABSOLUTE GAIN ERROR CHANGE vs V_{REF}



Dual 12-Bit Double-Buffered Multiplying CMOS D/A Converter

DAC8222

FEATURES

- Two Matched 12-Bit DACs on One Chip
- Direct Parallel Load of All 12 Bits for High Data Throughput
- Double-Buffered Digital Inputs
- 12-Bit Endpont Linearity (±1/2 LSB) Over Temperature
- +5V to +15V Single Supply Operation
- DACs Matched to 1% Max
- Four-Quadrant Multiplication
- Improved ESD Resistance
- Packaged in a Narrow 0.3" 24-Pin DIP and 0.3" 24-Pin SOL package
- Available in Die Form

APPLICATIONS

- Automatic Test Equipment
- Robotics/Process Control/Automation
- Digital Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

ORDERING INFORMATION †

RELATIVE ACCURACY (+5V or +15V)	GAIN ERROR	PACKAGE MILITARY* TEMPERATURE –55°C to +125°C	PACKAGE INDUSTRIAL TEMPERATURE –40°C to +85°C	PACKAGE COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±1 LSB	DAC8222AW	DAC8222EW	–
±1/2 LSB	±2 LSB	–	–	DAC8222GP
±1 LSB	±4 LSB	–	DAC8222FW	DAC8222HP
±1 LSB	±4 LSB	–	DAC8222FP	DAC8222HS††

* For devices processed in total compliance to MIL-SDT-883, add /883 after part number. Consult factory for 883 data sheet.

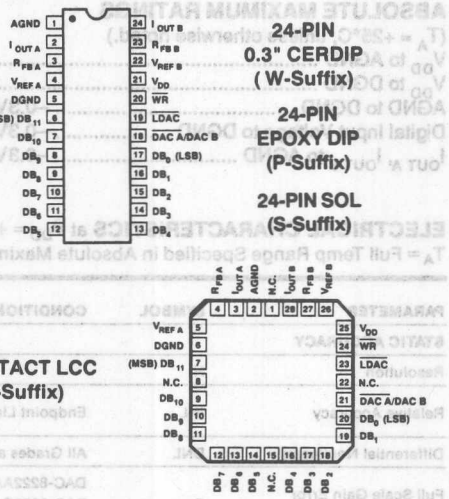
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

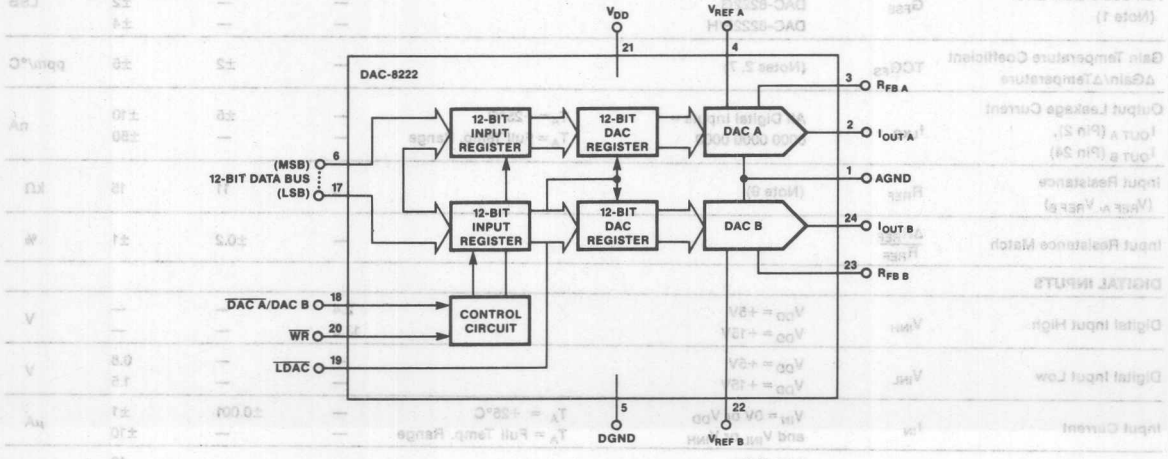
GENERAL DESCRIPTION

The DAC-8222 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has a 12-bit wide data port that allows a 12-bit word to be loaded directly. This achieves faster throughput time in stand-alone systems or when interfacing to a 16-bit processor. A common 12-bit input TTL/CMOS compatible data port is used to load the 12-bit word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit and 16-bit bus systems. (See PMI's DAC-8248 for a complete 8-bit data bus interface product.) A common bus allows the DAC-8222 to be packaged in a narrow 24-pin 0.3" DIP and save PCB space.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



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The DAC is controlled with two signals, $\overline{WR}$ and $\overline{LDAC}$. With logic low at these inputs, the DAC registers become transparent. This allows direct unbuffered data to flow directly to either DAC output selected by $\overline{DAC\ A}$/DAC B. Also, the DAC's double-buffered digital inputs will allow both DACs to be updated simultaneously.

DAC-8222's monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The chip consists of two thin-film R-2R resistor ladder networks, four 12-bit registers, and DAC control logic circuitry. The device has separate reference-input and feedback resistors for each DAC and operates on a single supply from +5V to +15V. Maximum power dissipation at +5V using zero or V_{DD} logic levels is less than 0.5mW.

The DAC-8222 is manufactured with PMI's highly stable thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS technology. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... –0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND ..... –0.3V, V_{DD} +0.3V
$I_{OUT\ A}$, $I_{OUT\ B}$ to AGND ..... –0.3V, V_{DD} +0.3V
$V_{REF\ A}$, $V_{REF\ B}$ to AGND ..... ±25V
$V_{RFB\ A}$, $V_{RFB\ B}$ to AGND ..... ±25V
Operating Temperature Range
AW Version ..... –55°C to +125°C
EW, FW, FP Versions ..... –40°C to +85°C
GP, HP, HS Versions ..... –0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
24-Pin Hermetic DIP (W)	69	10	°C/W
24-Pin Plastic DIP (P)	62	32	°C/W
24-Pin SOL (S)	72	24	°C/W

NOTES:

1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:

1. Do no apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Devices can suffer permanent damage and/or reliability degradation if stressed above the limits listed under Absolute Maximum Ratings for extended periods.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF\ A}$ = $V_{REF\ B}$ = +10V, $V_{OUT\ A}$ = $V_{OUT\ B}$ = 0V; AGND = DGND = 0V; T_A = Full Temp Range Specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.

PARAMETER	SYMBOL	CONDITIONS		DAC-8222 MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution	N			12	—	—	Bits
Relative Accuracy	INL	Endpoint Linearity Error	DAC-8222A/E/G	—	—	±1/2	LSB
			DAC-8222F/H	—	—	±1	
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic		—	—	±1	LSB
Full Scale Gain Error (Note 1)	G_{FSE}	DAC-8222A/E		—	—	±1	LSB
		DAC-8222G		—	—	±2	
		DAC-8222F/H		—	—	±4	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG_{FS}	(Notes 2, 7)		—	±2	±5	ppm/°C
Output Leakage Current $I_{OUT\ A}$ (Pin 2), $I_{OUT\ B}$ (Pin 24)	I_{LKG}	All Digital Inputs = 0000 0000 0000	T_A = +25°C	—	±5	±10	nA
			T_A = Full Temp. Range	—	—	±50	
Input Resistance ($V_{REF\ A}$, $V_{REF\ B}$)	R_{REF}	(Note 9)		8	11	15	kΩ
Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$			—	±0.2	±1	%
DIGITAL INPUTS							
Digital Input High	V_{INH}	V_{DD} = +5V		2.4	—	—	V
		V_{DD} = +15V		13.5	—	—	
Digital Input Low	V_{INL}	V_{DD} = +5V		—	—	0.8	V
		V_{DD} = +15V		—	—	1.5	
Input Current	I_{IN}	V_{IN} = 0V or V_{DD} and V_{INL} or V_{INH}	T_A = +25°C	—	±0.001	±1	µA
			T_A = Full Temp. Range	—	—	±10	
Input Capacitance (Note 2)	C_{IN}	DB0-DB11		—	—	10	pF
		$\overline{WR}$, $\overline{LDAC}$, $\overline{DAC\ A}$/DAC B		—	—	15	

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF\,A} = V_{REF\,B}$ = +10V, $V_{OUT\,A} = V_{OUT\,B}$ = 0V; AGND = DGND = 0V; T_A = Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8222 MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	–	–	2	mA
		All Digital Inputs 0V or V_{DD}	–	10	100	µA
DC Power Supply Rejection Ration ($\Delta Gain/\Delta V_{DD}$)	PSRR	ΔV_{DD} = ±5%	–	–	0.002	%/%
AC PERFORMANCE CHARACTERISTICS (Note 2)						
Propagation Delay (Notes 4, 5)	t_{PD}	T_A = +25°C	–	–	350	ns
Current Settling Time (Notes 5, 6)	t_s	T_A = +25°C	–	–	1	µs
Output Capacitance	C_O	Digital Inputs = All 0s $C_{OUT\,A}$, $C_{OUT\,B}$	–	–	90	pF
		Digital Inputs = All 1s $C_{OUT\,A}$, $C_{OUT\,B}$	–	–	120	
AC Feedthrough at $I_{OUT\,A}$ or $I_{OUT\,B}$	FT_A	$V_{REF\,A}$ to $I_{OUT\,A}$; $V_{REF\,A}$ = 20V_{p-p}; f = 100kHz; T_A = +25°C	–	–	–70	dB
	FT_B	$V_{REF\,B}$ to $I_{OUT\,B}$; $V_{REF\,B}$ = 20V_{p-p}; f = 100kHz; T_A = +25°C	–	–	–70	

SWITCHING CHARACTERISTICS (Notes 2, 3)		V_{DD} = +5V			V_{DD} = +15V	
		+25°C	–40°C TO +85°C (Note 8)	–55°C TO +125°C	ALL TEMPS (Note 10)	
DAC Select to Write Set-Up Time	t_{AS}	150	180	210	60	ns MIN
DAC Select to Write Hold Time	t_{AH}	0	0	0	0	ns MIN
LDAC to Write Set-Up Time	t_{LS}	80	100	120	60	ns MIN
LDAC to Write Hold Time	t_{LH}	20	20	20	20	ns MIN
Data Valid to Write Set-Up Time	t_{DS}	220	240	260	100	ns MIN
Data Valid to Write Hold Time	t_{DH}	0	0	0	10	ns MIN
Write Pulse Width	t_{WR}	130	160	170	90	ns MIN
LDAC Pulse Width	t_{LWD}	100	120	130	60	ns MIN

NOTES:
1. Measured using internal $R_{FB\,A}$ and $R_{FB\,B}$. Both DAC digital inputs = 1111 1111 1111.
2. Guaranteed and not tested.
3. See timing diagram.
4. From 50% of digital input to 90% of final analog output current. $V_{REF\,A}$ = $V_{REF\,B}$ = +10V; OUT A, OUT B load = 100Ω, C_{EXT} = 13pF.
5. $\overline{WR}$, $\overline{LDAC}$ = 0V; DB0 – DB11 = 0V to V_{DD} or V_{DD} to 0V.
6. Settling time is measured from 50% of the digital input change to where the output voltage settles within 1/2 LSB of full scale.
7. Gain TC is measured from +25°C to T_{MIN} or from +25°C to T_{MAX}.
8. These limits apply for the commercial and industrial grade products.
9. Absolute temperature coefficient is approximately +50ppm/°C.
10. These limits also apply as typical values for V_{DD} = +12V with +5V CMOS logic levels and T_A = +25°C.

Dual 8-Bit CMOS

FEATURES

- Two 8-Bit Voltage Out DACs in a Single Chip
- Fits 7528/7628 Sockets
- Adjustment Free Internal CMOS Op Amps
- Single +12V to +15V Operation
- TTL Compatible Over Full V_{DD} Range
- Fast Interface Timing ..... T_{WR} = 50ns
- Improved Resistance to ESD
- Available in Small Outline Package
- CerDIP and Epoxy Packages Come in the Extended Industrial Temperature Range of –40°C to +85°C
- Available in Die Form

APPLICATIONS

- Disk Drive Systems
- Automatic Test Equipment
- Process/Industrial Controls
- Energy Controls
- Programmable Instrumentation
- Multi-Channel Microprocessor-Controlled Systems
- Servo Control Systems

ORDERING INFORMATION †

		PACKAGE: 20-PIN DIP/SOL
RELATIVE ACCURACY	GAIN ERROR	EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C
±1/2 LSB	±2 LSB	DAC8228FR
±1/2 LSB	±2 LSB	DAC8228FP
±1/2 LSB	±2 LSB	DAC8228FS

† All commercial and industrial temperature range parts are available with burn-in.

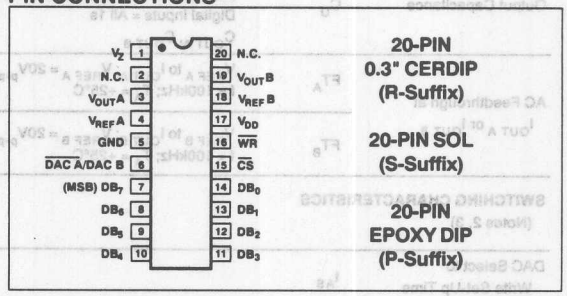
GENERAL DESCRIPTION

The DAC-8228 is a dual 8-bit, voltage output, CMOS, D/A converter in a single chip. It was designed to drop into AD7528/7628 sockets eliminating two external op amps in applications such as hard disk drives. These applications generally operate the AD7528/7628 with zero volts applied to V_{REF} and offset AGND to +2.5 or +5 volts. The DAC-8228 is tested under both these conditions.

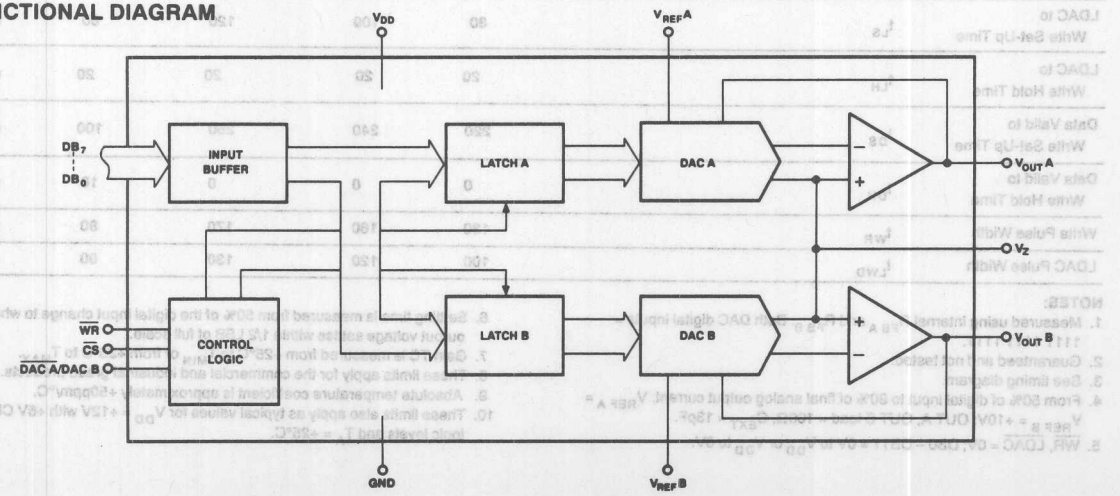
The DAC-8228 can also be used in those applications requiring a unipolar output voltage. It can deliver an output voltage between 0V and +10V with V_{DD} = +14V (maximum output voltage is V_{DD} –4V). The DAC-8228's reference input can accept a negative voltage from 0V to –10V (the DAC's internal unity-gain inverting amplifier inverts the input signal). Choose the DAC-8229 for bipolar operation.

Continued

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



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GENERAL DESCRIPTION *Continued*

The DAC-8228 offers CerDIP and plastic packaged devices in the extended industrial temperature range of –40°C to +85°C. Applications requiring the military temperature range should use the DAC-8229. To make the DAC-8229 pin and functionally compatible with the DAC-8228, AGND A and AGND B should be tied together to function as V_Z, and V_{SS} connected to GND.

The DAC-8228 consists of two CMOS voltage output amplifiers, two high-accuracy R-2R resistor ladder networks, interface control logic, and two 8-bit registers. An internal regulator maintains TTL logic compatibility and fast microprocessor interface timing over the full V_{DD} range.

The DAC-8228 dissipates only 90mW in the space saving 20-pin 0.3" DIP or the 20-lead SO surface mount package. Its compact size, low power, and economical cost per channel, makes it attractive for applications requiring multiple D/A converters without sacrificing circuit-board space. Reduced parts count also improves system reliability.

Using PMI's advanced oxide-isolated, silicon-gate CMOS process, coupled with its highly-stable thin-film resistor ladder, allows the DAC-8228 to offer superior matching and temperature tracking between DACs.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to V_Z or GND ..... –0.3V, +17V
V_Z to GND ..... –0.3V, V_{DD}
Digital Input Voltage to GND ..... –0.3V, V_{DD}
$V_{REF\ A}$, $V_{REF\ B}$ to GND ..... –17V, V_Z
$V_{OUT\ A}$, $V_{OUT\ B}$ to V_Z (Note 1) ..... –0.3V, V_{DD}
Operating Temperature Range
FR/FP/FS Versions ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES:

1. Outputs may be shorted to any terminal provided the package power dissipation is not exceeded. Typical output short-circuit current to GND is 50mA.
2. Use proper anti-static handling procedures when handling these devices.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_{DD} = +12V ±5%, V_{REF} = 0V, V_Z = +2.5V and V_{DD} = +15V ±5%, V_{REF} = 0V, V_Z = +5V. T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8228 MIN	TYP	MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		8	–	–	Bits
Relative Accuracy (Note 2)	INL		–	–	±1	LSB
Differential Nonlinearity (Note 3)	DNL		–	–	±1	LSB
Gain Error	G_{FSE}	DAC Latches Loaded with 1111 1111	–	–	±2	LSB
Gain Error Temperature Coefficient (Note 4)	TCG_{FS}		–	±0.0003	±0.002	%/°C
Zero Code Error	V_{ZSE}		–	–	±15	mV
Zero Code Error Temperature Coefficient (Note 4)	TCV_{ZS}		–	±10	–	µV/°C
REFERENCE INPUT (Note 8)						
Input Resistance (Note 5)	R_{IN}	Pin 4 and Pin 18	7	–	15	kΩ
Input Resistance Match ($V_{REF}A/V_{REF}B$)	$\frac{\Delta R_{IN}}{R_{IN}}$		–	±0.1	±1	%
Input Capacitance (Note 4)	C_{IN}		–	9	20	pF
V_Z Input Resistance (Note 10)	R_{VZ}	Digital Inputs = 0V	2	–	–	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +12V ±5%, V_{REF} = 0V, V_Z = +2.5V and V_{DD} = +15V ±5%, V_{REF} = 0V, V_Z = +5V. T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

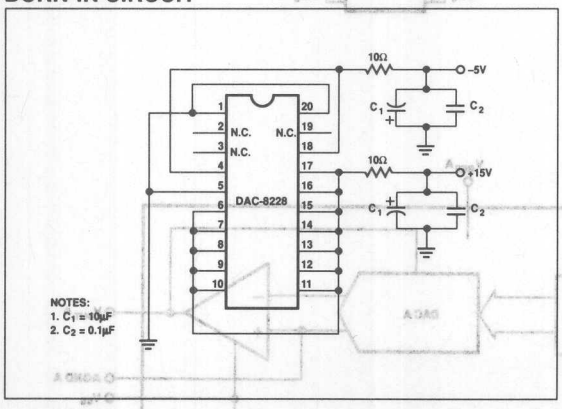
PARAMETER	SYMBOL	CONDITIONS	DAC-8228 MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Digital Input High	V_{INH}		2.4	–	–	V
Digital Input Low	V_{INL}		–	–	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	–	–	±1	µA
Input Capacitance (Note 4)	C_{IN}		–	4	8	pF
POWER SUPPLIES						
Supply Current (Note 6)	I_{DD}		–	–	7	mA
Power Dissipation	P_D	V_{DD} = +12V 12 x 7mA	–	–	84	mW
		V_{DD} = +15V 15 x 7mA	–	–	105	
DC Power Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$)	PSRR	ΔV_{DD} = ±5%	–	–	0.01	%/%
DYNAMIC PERFORMANCE						
Slew Rate (V_{OUT}) (Note 4)	SR	T_A = +25°C Digital Inputs = 0V to +5V	–	2.5	–	V/µs
Settling Time (V_{OUT}) Positive or Negative (Note 4, 7)	t_s	Digital Inputs = 0V to +5V	–	2	5	µs
Channel-to-Channel Isolation (Note 4)	CCI	T_A = +25°C $V_{REF}B$ to $V_{OUT}A$ or $V_{REF}A$ to $V_{OUT}B$ $V_{REF}B = V_{REF}A = 20V_{p-p}$ @ f = 10kHz	–	–80	–	dB
Digital Crosstalk (Notes 4, 9)	Q	T_A = +25°C For Code Transition 0000 0000 to 1111 1111	–	4	10	nVs
Digital Charge Injection	Q	T_A = +25°C For Code Transition 0000 0000 to 1111 1111	–	100	–	nVs
AC Feedthrough (Notes 4, 11)	FT		–	–	–70	dB
Harmonic Distortion	THD	T_A = +25°C $V_{IN} = 6V_{RMS}$ @ f = 1kHz	–	–85		dB

ELECTRICAL CHARACTERISTICS at V_{DD} = +12V ±5%, V_{REF} = 0V, V_Z = +2.5V and V_{DD} = +15V ±5%, V_{REF} = 0V, V_Z = +5V. T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8228 MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4)						
Chip Select to Write Set-Up Time	t_{CS}		60	–	–	ns
Chip Select to Write Hold Time	t_{CH}		10	–	–	ns
DAC Select to Write Set-Up Time	t_{AS}		60	–	–	ns
DAC Select to Write Hold Time	t_{AH}		10	–	–	ns
Data Valid to Write Set-Up Time	t_{DS}		60	–	–	ns
Data Valid to Write Hold Time	t_{DH}		10	–	–	ns
Write Pulse Width	t_{WR}		50	–		ns

NOTES:
1. Specifications apply to both DAC A and DAC B.
2. This is an endpoint linearity specification.
3. All devices are guaranteed to be monotonic over the full operating temperature range.
4. These characteristics are for design guidance only and not subject to production test.
5. Input resistance temperature coefficient = +300ppm/°C.
6. $V_{IN} = V_{INL}$ or V_{INH}; outputs unloaded.
7. V_{REF} = ±2.5V; to where output settles to ±1/2 LSB.
8. V_{REF} voltage range is 0V to –10V; the absolute maximum negative value is: $|V_{REF}| = V_{DD} - 4V$.
9. Digital crosstalk is a measure of the amount of digital input pulse appearing at the analog output of the unselected DAC while applying it to the digital inputs of the other DAC.
10. Resistance looking into the V_Z terminal.
11. $V_{REF}A$, $V_{REF}B$ = 20V_{p-p} Sinewave @ f = 10kHz; $V_{REF}A$ to $V_{OUT}A$ or $V_{REF}B$ to $V_{OUT}B$, both DAC latches loaded with 0000 0000.

BURN-IN CIRCUIT



Dual 8-Bit CMOS D/A Converter with Voltage Output

DAC8229

FEATURES

- Two 8-Bit DACs In A Single Chip
- Adjustment-Free Internal CMOS Amplifiers
- Single or Dual Supply Operation
- TTL Compatible Over Full V_{DD} Range
- 5 Microsecond Settling Time
- Fast Interface Timing ..... t_{WR} = 50ns
- Improved Resistance to ESD
- Fits AD/PM-7528 And AD/PM-7628 Sockets
- Available In Small Outline Package
- –40°C to +85°C for the Extended Industrial Temperature Range
- Available In Die Form

APPLICATIONS

- Automatic Test Equipment
- Process/Industrial Controls
- Energy Controls
- Programmable Instrumentation
- Disk Drive Systems
- Multi-Channel Microprocessor-Controlled Systems

GENERAL DESCRIPTION

The DAC-8229 is a dual 8-bit, voltage output, multiplying CMOS D/A converter. Its reference input accepts a ±2.5V signal, inverts and delivers it to the output with an internal amplifier. It can also accept –10V at V_{REF} with a corresponding +10V output (the maximum positive input signal that it can accept is +2.5V).

The DAC-8229 was designed to operate with dual supplies; however, it can be operated with a single supply by connecting

Continued

ORDERING INFORMATION†

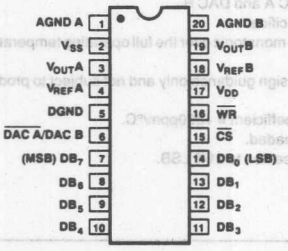
		PACKAGE: 20-PIN DIP/SOL	
RELATIVE ACCURACY	GAIN ERROR	MILITARY* TEMPERATURE –55°C to +125°C	EXTENDED†† INDUSTRIAL TEMPERATURE –40°C to +85°C
±1/2LSB	±2LSB	DAC8229AR	DAC8229ER
±1/2LSB	±2LSB	——	DAC8229FP
±1/2LSB	±2LSB	——	DAC8229FS

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in.

†† Cerdip and epoxy packaged devices available in the extended industrial temperature range.

PIN CONNECTIONS

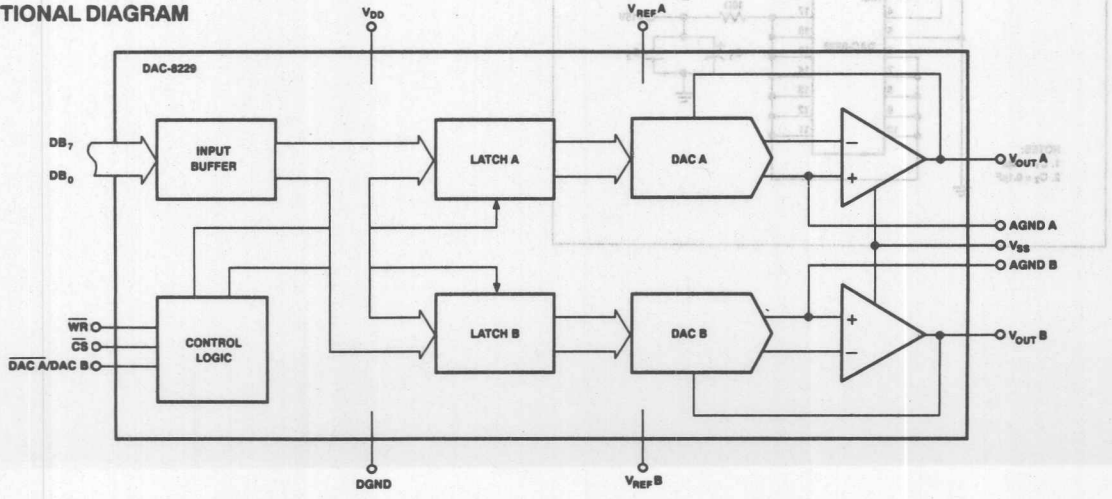


20-PIN 0.3"CERDIP (R-Suffix)

20-PIN SOL (S-Suffix)

20-PIN EPOXY DIP (P-Suffix)

FUNCTIONAL DIAGRAM



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ELECTRICAL CHARACTERISTICS at V_{DD} = +11.4V or +15.75V; V_{SS} = –5V ±10%; V_{REF} = ±2.5V; AGND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8229 MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Digital Input High	V_{INH}		2.4	–	–	V
Digital Input Low	V_{INL}		–	–	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	–	–	±1	µA
Input Capacitance (Note 4)	C_{IN}		–	4	8	pF
POWER SUPPLIES						
Positive Supply Current (Note 6)	I_{DD}		–	–	6	mA
Negative Supply Current (Note 6)	I_{SS}		–	–	5	mA
DC Power Supply Rejection Ratio (Δ Gain/ΔV_{DD}) (Note 10)	PSRR	ΔV_{DD} = ±5%	–	–	0.01	%/%
DYNAMIC PERFORMANCE						
Slew Rate (V_{OUT}) (Note 4)	SR	T_A = 25°C V_{REF} = –2.5V Digital Inputs = 0V to +5V	–	2.5	–	V/µs
Settling Time (V_{OUT}) Positive or Negative (Notes 4,7)	t_S	V_{REF} = –2.5V Digital Inputs = 0V to +5V	–	2	5	µs
Channel-to-Channel Isolation (Note 4)	CCI	V_{REF}B to V_{OUT}A or V_{REF}A to V_{OUT}B V_{REF}B = V_{REF}A = 20V_{p-p} @ f = 10kHz	–	–80	–	dB
Digital Crosstalk (Notes 4, 9)	Q	For Code Transition 0000 0000 to 1111 1111	–	4	10	nVs
AC Feedthrough (Notes 4, 11)	F_T	T_A = 25°C T_A = Full Temp. Range	– –	– –	–70 –65	dB
SWITCHING CHARACTERISTICS (Note 4)						
Chip Select to Write Set-Up Time	t_{CS}		60	–	–	ns
Chip Select to Write Hold Time	t_{CH}		10	–	–	ns
DAC Select to Write Set-Up Time	t_{AS}		60	–	–	ns
DAC Select to Write Hold Time	t_{AH}		10	–	–	ns
Data Valid to Write Set-Up Time	t_{DS}		60	–	–	ns
Data Valid to Write Hold Time	t_{DH}		10	–	–	ns
Write Pulse Width	t_{WR}		50	–	–	ns

NOTES:
1. Specifications apply to both DAC A and DAC B.
2. This is an endpoint linearity specification.
3. All devices are guaranteed to be monotonic over the full operating temperature range.
4. These characteristics are for design guidance only and are not subject to production test.
5. Input resistance temperature coefficient = +300 ppm/°C.
6. V_{IN} = V_{INL} or V_{INH}; outputs unloaded.
7. V_{REF} = ±2.5V; to where output settles to ±1/2 LSB.
8. V_{REF} voltage range is +3V to –10V; the absolute maximum negative value is: $|V_{REF}| = V_{DD} - 4V$.
9. Digital crosstalk is a measure of the amount of digital input pulse appearing at the analog output of the unselected DAC while applying it to the digital inputs of the other DAC.
10. V_{REF} = +2.5V, $R_{PULLDOWN}$ = 20kΩ (a pulldown resistor to V_{SS} is used for these tests).
11. V_{REF}A, V_{REF}B = 20V_{p-p} Sinewave @ f = 10kHz; V_{REF}A to V_{REF}B or V_{REF}B to V_{REF}A.

GENERAL DESCRIPTION *Continued*

V_{SS}, AGND A, and AGND B to ground. Its operating characteristics will then be similar to that of the DAC-8228 (whose pin-out allows it to drop into the AD/PM-7528 and AD/PM-7628 sockets).

An internal regulator provides TTL logic compatibility and fast microprocessor interface timing over the full V_{DD} range. Also, each DAC input latch is addressable for easy microprocessor interfacing.

The DAC-8229 dissipates less than 109mW in the space-saving 20-pin 0.3" DIP or the 20-lead SO surface-mount package. Its compact size, low power, and economical cost per channel, make it attractive for applications requiring multiple D/A converters without sacrificing circuit-board space. Reduced parts count also improves system reliability.

PMI's advanced oxide-isolated, silicon-gate CMOS process, coupled with PMI's highly-stable thin-film R-2R resistor ladder, offers superior matching and temperature tracking between DACs.

The DAC-8229 offers cerdip or epoxy packaged devices in the extended industrial temperature range of –40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND or DGND ..... –0.3V, +17
VV_{SS} to AGND or DGND ..... –7V, V_{DD}
V_{DD} to V_{SS} ..... –0.3V, +24V
AGND to DGND ..... –0.3V, V_{DD}
Digital Input Voltage to GND ..... –0.3V, V_{DD}
V_{REF} to AGND ..... –17V, +4V
V_{OUT} to AGND (Note 1) ..... V_{SS}, V_{DD}
Operating Temperature Range
  DAC-8229AR Version ..... –55°C to +125°C
  DAC-8229ER/FP/FS Versions ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES:
1. Outputs may be shorted to any terminal provided the package power dissipation is not exceeded. Typical output short-circuit current to AGND is 50mA.
2. Use proper antistatic handling procedures when handling these devices.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_{DD} = +11.4V or +15.75V; V_{SS} = –5V ±10%; V_{REF} = ±2.5V; AGND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8229 MIN	TYP	MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		8	–	–	Bits
Relative Accuracy (Note 2,10)	INL		–	–	±1/2	LSB
Differential Nonlinearity (Note 3, 10)	DNL		–	–	±1	LSB
Gain Error (Note 10)	G_{FSE}		–	–	±2	LSB
Gain Error Temperature Coefficient (Note 4, 10)	TCG_{FS}		–	±0.0008	±0.002	%/°C
Zero Gain Error (Note 10)	V_{ZSE}		–	–	±10	mV
Zero Code Error Temperature Coefficient (Note 4, 10)	TCV_{ZS}		–	±5	–	µV/°C
REFERENCE INPUT (Note 8)						
Input Resistance (Note 5)	R_{IN}		7	–	15	kΩ
Input Resistance Match ($V_{REF}A/V_{REF}B$)	$\frac{\Delta R_{IN}}{R_{IN}}$		–	±0.1	±1	%
Input Capacitance (Note 4)	C_{IN}		–	9	20	pF

Dual 12-Bit (8-Bit Byte) Double-Buffered CMOS D/A Converter

DAC8248

FEATURES

- Two Matched 12-Bit DACs on One Chip
- 12-Bit Resolution with an 8-Bit Data Bus
- Direct Interface with 8-Bit Microprocessors
- Double-Buffered Digital Inputs
- RESET to Zero Pin
- 12-Bit Endpont Linearity (±1/2 LSB) Over Temperature
- +5V to +15V Single Supply Operation
- Latch-Up Resistant
- Improved ESD Resistance
- Packaged in a Narrow 0.3" 24-Pin DIP and 0.3" 24-Pin SOL package
- Available in Die Form

APPLICATIONS

- Multi-Channel Microprocessor-Controlled Systems
- Robotics/Process Control/Automation
- Automatic Test Equipment
- Programmable Attenuator, Power Supplies, Window Comparators
- Instrumentation Equipment
- Battery Operated Equipment

GENERAL DESCRIPTION

The DAC-8248 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has an 8-bit wide input data port that interfaces directly with 8-bit microprocessors. It loads a 12-bit word in two bytes using a single control; it can accept either a least significant byte or most significant byte first. For designs with a 12-bit or 16-bit wide data path, choose the DAC-8222 or DAC-8221.

The DAC-8248's double-buffered digital inputs allow both DAC's analog output to be updated simultaneously. This is particularly useful in multiple DAC systems where a common $\overline{\text{LDAC}}$ signal updates all DACs at the same time. A single $\overline{\text{RESET}}$ pin resets both outputs to zero.

ORDERING INFORMATION†

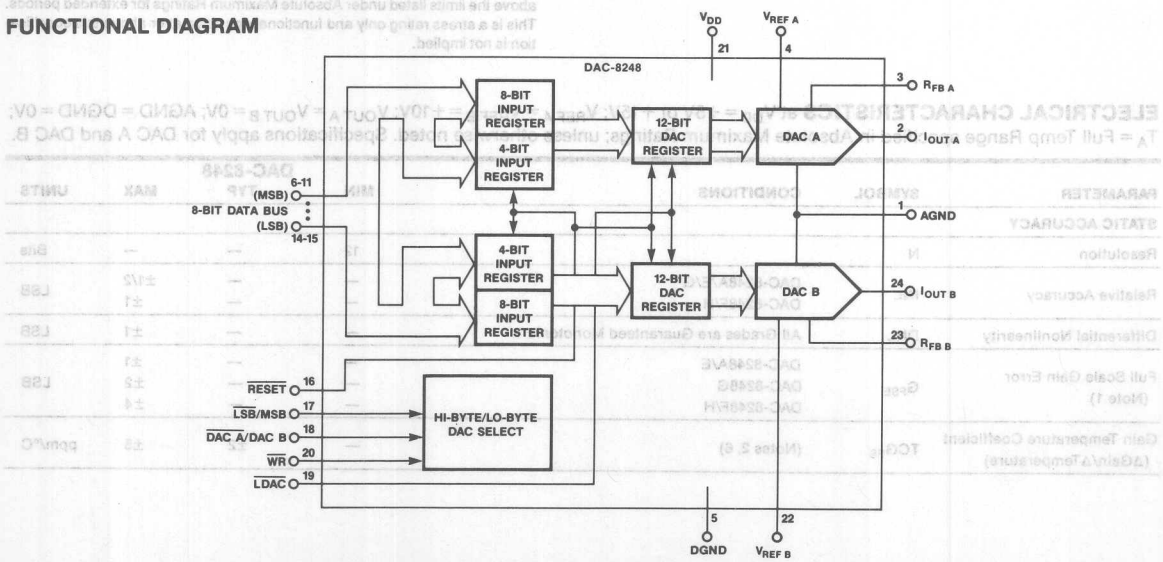
RELATIVE ACCURACY (+5V or +15V)	GAIN ERROR	PACKAGE: MILITARY* TEMPERATURE −55°C to +125°C	PACKAGE: INDUSTRIAL TEMPERATURE −40°C to +85°C	PACKAGE: COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±1 LSB	DAC8248AW	DAC8248EW	—
±1/2 LSB	±2 LSB	—	—	DAC8248GP
±1 LSB	±4 LSB	—	DAC8248FW	DAC8248HP
±1 LSB	±4 LSB	—	DAC8248FP	DAC8248HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

FUNCTIONAL DIAGRAM



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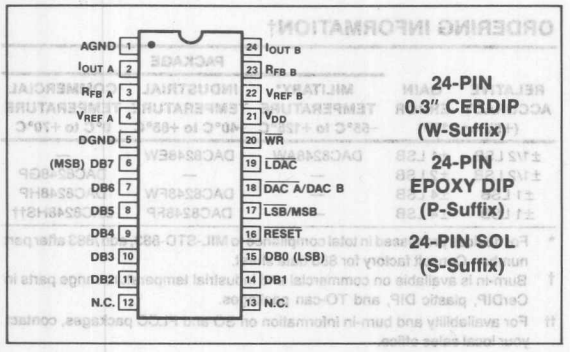
DAC8248

The DAC-8248's monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The DAC consists of two thin-film R-2R resistor ladder networks, two 12-bit, two 8-bit, and two 4-bit data registers, and control logic circuitry. Separate reference input and feedback resistors are provided for each DAC. The DAC-8248 operates on a single supply from +5V to +15V, and it dissipates less than 0.5mW at +5V (using zero or V_{DD} logic levels). The device is packaged in a space-saving 0.3", 24-pin DIP.

The DAC-8248 is manufactured with PMI's highly-stable thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS technology. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

PIN CONNECTIONS



24-PIN 0.3" CERDIP (W-Suffix)

24-PIN EPOXY DIP (P-Suffix)

24-PIN SOL (S-Suffix)

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... –0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND ..... –0.3V, V_{DD} +0.3V
$I_{OUT\ A}$, $I_{OUT\ B}$ to AGND ..... –0.3V, V_{DD} +0.3V
$V_{REF\ A}$, $V_{REF\ B}$ to AGND ..... ±25V
$V_{RFB\ A}$, $V_{RFB\ B}$ to AGND ..... ±25V
Operating Temperature Range
AW Version ..... –55°C to +125°C
EW, FW, FP Versions ..... –40°C to +85°C
GP, HP, HS Versions ..... –0°C to +70°C
Junction Temperature ..... +150C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
24-Pin Hermetic DIP (W)	69	10	°C/W
24-Pin Plastic DIP (P)	62	32	°C/W
24-Pin SOL (S)	72	24	°C/W

NOTE:

1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:

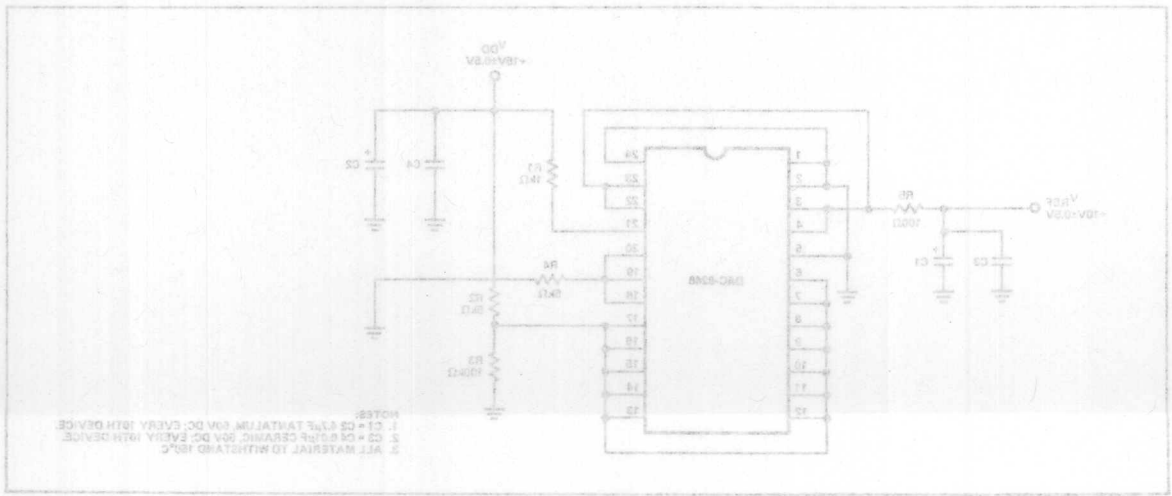
1. Do no apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Devices can suffer permanent damage and/or reliability degradation if stressed above the limits listed under Absolute Maximum Ratings for extended periods. This is a stress rating only and functional operation at or above this specification is not implied.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V; $V_{REF\ A} = V_{REF\ B}$ = +10V; $V_{OUT\ A} = V_{OUT\ B}$ = 0V; AGND = DGND = 0V; T_A = Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.

PARAMETER	SYMBOL	CONDITIONS	DAC-8248 MIN	DAC-8248 TYP	DAC-8248 MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	—	—	Bits
Relative Accuracy	INL	DAC-8248A/E/G	—	—	±1/2	LSB
		DAC-8248F/H	—	—	±1	
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic	—	—	±1	LSB
Full Scale Gain Error (Note 1)	G_{FSE}	DAC-8248A/E	—	—	±1	LSB
		DAC-8248G	—	—	±2	
		DAC-8248F/H	—	—	±4	
Gain Temperature Coefficient (ΔGain/ΔTemperature)	TCG_{FS}	(Notes 2, 6)	—	±2	±5	ppm/°C

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V; $V_{REF\,A}$ = $V_{REF\,B}$ = +10V; $V_{OUT\,A}$ = $V_{OUT\,B}$ = 0V; AGND = DGND = 0V; T_A = Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B. (Continued)

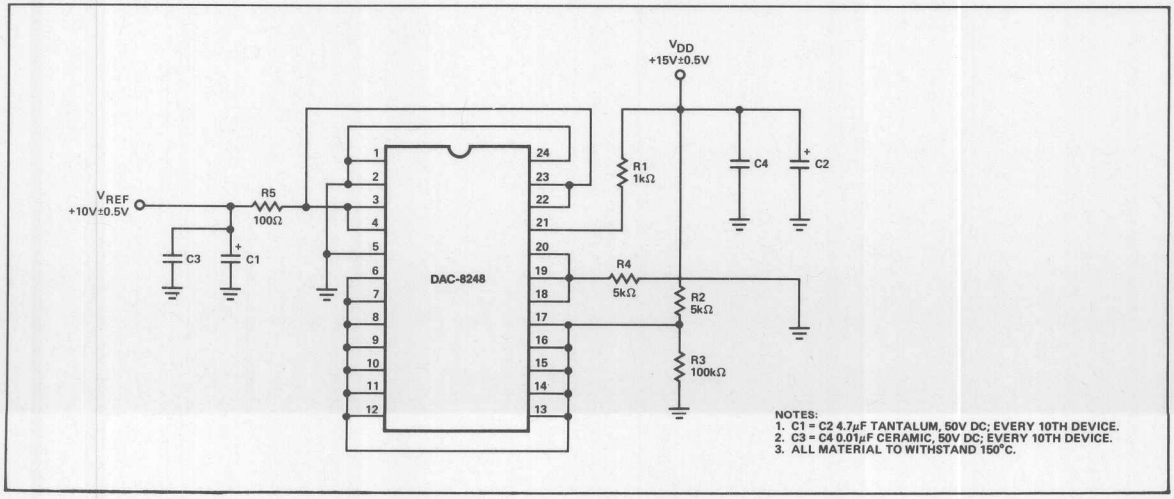
PARAMETER	SYMBOL	CONDITIONS	DAC-8248 MIN	DAC-8248 TYP	DAC-8248 MAX	UNITS
Output Leakage Current $I_{OUT\,A}$ (Pin 2), $I_{OUT\,B}$ (Pin 24)	I_{LKG}	All Digital Inputs = 0s T_A = +25°C T_A = Full Temp. Range	— —	±5 —	±10 ±50	nA
Input Resistance ($V_{REF\,A,\,REF\,B}$)	R_{REF}	(Note 9)	8	11	15	kΩ
Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$		—	±0.2	±1	%
DIGITAL INPUTS						
Digital Input High	V_{INH}	V_{DD} = +5V V_{DD} = +15V	2.4 13.5	— —	— —	V
Digital Input Low	V_{INL}	V_{DD} = +5V V_{DD} = +15V	— —	— —	0.8 1.5	V
Input Current (V_{IN} = 0V or V_{DD} and V_{INL} or V_{INH})	I_{IN}	T_A = +25°C T_A = Full Temp. Range	— —	±0.001 —	±1 ±10	μA
Input Capacitance (Note 2)	C_{IN}	DB0-DB11 $\overline{WR}$, $\overline{LDAC}$, DAC A/$\overline{DAC\ B}$, LSB/$\overline{MSB}$, $\overline{RESET}$	— —	— —	10 15	pF
POWER SUPPLY						
Supply Current	I_{DD}	Digital Inputs = V_{INL} or V_{INH} Digital Inputs = 0V or V_{DD}	— —	— 10	2 100	mA μA
DC Power Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$)	PSRR	ΔV_{DD} = ±5%	—	—	0.002	%/%
AC PERFORMANCE CHARACTERISTICS (Note 2)						
Propagation Delay (Notes 3, 4)	t_{PD}	T_A = +25°C	—	—	350	ns
Output Current Settling Time (Notes 4, 5)	t_s	T_A = +25°C	—	—	1	μs
Output Capacitance	C_O	Digital Inputs = all 0s $C_{OUT\,A}$, $C_{OUT\,B}$ Digital Inputs = all 1s $C_{OUT\,A}$, $C_{OUT\,B}$	— —	— —	90 120	pF
AC Feedthrough at $I_{OUT\,A}$ or $I_{OUT\,B}$	FT_A	$V_{REF\,A}$ to $I_{OUT\,A}$; $V_{REF\,A}$ = $20V_{p-p}$ f = 100kHz; T_A = +25°C	—	—	−70	dB
	FT_B	$V_{REF\,B}$ to $I_{OUT\,B}$; $V_{REF\,B}$ = $20V_{p-p}$ f = 100kHz; T_A = +25°C	—	—	−70	



PARAMETER	SYMBOL	CONDITIONS	DAC-8248				UNITS
			V_{DD} = +5V			V_{DD} = +15V	
SWITCHING CHARACTERISTICS (Notes 2, 7)			+25°C	–40°C TO +85°C (Note 8)	–55°C TO +125°C	ALL TEMPS (Note 10)	
LSB/MSB Select to Write Set-Up Time	t_{CBS}		130	170	180	80	ns MIN
LSB/MSB Select to Write Hold Time	t_{CBH}		0	0	0	0	ns MIN
DAC Select to Write Set-Up Time	t_{AS}		180	210	220	80	ns MIN
DAC Select to Write Hold Time	t_{AH}		0	0	0	0	ns MIN
LDAC to Write Set-Up Time	t_{LS}		120	150	160	80	ns MIN
LDAC to Write Hold Time	t_{LH}		0	0	0	0	ns MIN
Data Valid to Write Set-Up Time	t_{DS}		160	210	220	70	ns MIN
Data Valid to Write Hold Time	t_{DH}		0	0	0	10	ns MIN
Write Pulse Width	t_{WR}		130	150	170	90	ns MIN
LDAC Pulse Width	t_{LWD}		100	110	130	60	ns MIN
Reset Pulse Width	t_{RWD}		80	90	90	60	ns MIN

NOTES:
1. Measured using internal $R_{FB\,A}$ and $R_{FB\,B}$. Both DAC digital inputs = 1111 1111 1111.
2. Guaranteed and not tested.
3. From 50% of digital input to 90% of final analog output current. $V_{REF\,A}$ = $V_{REF\,B}$ = +10V; OUT A, OUT B load = 100Ω, C_{EXT} = 13pF.
4. $\overline{WR}$, $\overline{LDAC}$ = 0V; DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V.
5. Settling time is measured from 50% of the digital input change to where the output settles within 1/2 LSB of full scale.
6. Gain TC is measured from +25°C to T_{MIN} or from +25°C to T_{MAX}.
7. See Timing Diagram.
8. These limits apply for the commercial and industrial grade products.
9. Absolute Temperature Coefficient is approximately +50 ppm/°C.
10. These limits also apply as typical values for V_{DD} = +12V with +5V CMOS logic levels and T_A = +25°C.

BURN-IN CIRCUIT



NOTES:
1. C1 = C2 4.7μF TANTALUM, 50V DC; EVERY 10TH DEVICE.
2. C3 = C4 0.01μF CERAMIC, 50V DC; EVERY 10TH DEVICE.
3. ALL MATERIAL TO WITHSTAND 150°C.

FEATURES

- Four DACs in a 28 Pin, 0.6 Inch Wide DIP or 28 Pin JEDEC Plastic Chip Carrier
- ±1/4 LSB End-Point Linearity
- Guaranteed Monotonic
- DACs Matched to Within 1%
- Microprocessor Compatible
- Read/Write Capability (with Memory)
- TTL/CMOS Compatible
- Four-Quadrant Multiplication
- Single-Supply Operation (+5V)
- Low Power Consumption
- Latch-Up Resistant
- Available in Die Form

APPLICATIONS

- Voltage Set Points in Automatic Test Equipment
- Systems Requiring Data Access for Self-Diagnostics
- Industrial Automation
- Multi-Channel Microprocessor-Controlled Systems
- Digitally Controlled Op Amp Offset Adjustment
- Process Control
- Digital Attenuators

GENERAL DESCRIPTION

The DAC-8408 is a monolithic quad 8-bit multiplying digital-to-analog CMOS converter. Each DAC has its own reference input, feedback resistor, and on-board data latches that feature read/write capability. The readback function serves as memory for those systems requiring self-diagnostics.

A common 8-bit TTL/CMOS compatible input port is used to load data into any of the four DAC data-latches. Control lines $\overline{DS1}$, $\overline{DS2}$, and A/B determine which DAC will accept data. Data loading is similar to that of a RAM's write cycle. Data can be read back onto the same data bus with control line R/$\overline{W}$. The DAC-8408 is bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80. The DAC-8408 operates on a single +5 volt supply and dissipates less than 20mW. The DAC-8408 is manufactured using PMI's highly stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

ORDERING INFORMATION †

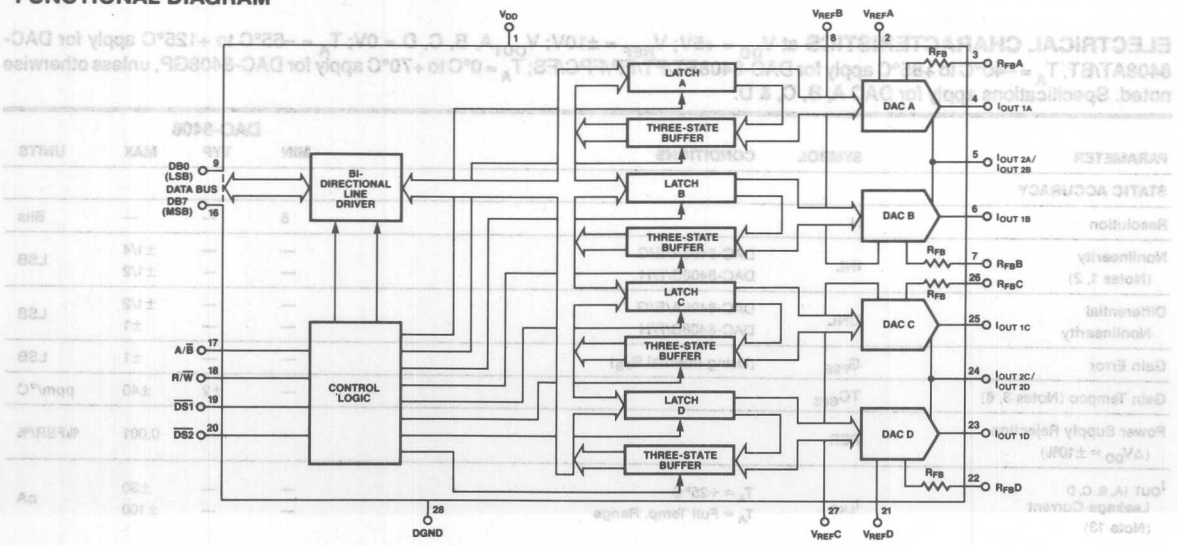
		PACKAGE		
		COMMERCIAL	EXTENDED INDUSTRIAL	MILITARY*
		TEMPERATURE	TEMPERATURE	TEMPERATURE
INL	DNL	0°C to +70°C	−40°C to +85°C	−55°C to +125°C
±1/4LSB	±1/2LSB	DAC8408GP	DAC8408ET	DAC8408AT
±1/2LSB	±1LSB	–	DAC8408FT	DAC8408BT
±1/2LSB	±1LSB	–	DAC8408FPC††	–
±1/2LSB	±1LSB	–	DAC8408FS	–
±1/2LSB	±1LSB	–	DAC8408FP	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

FUNCTIONAL DIAGRAM



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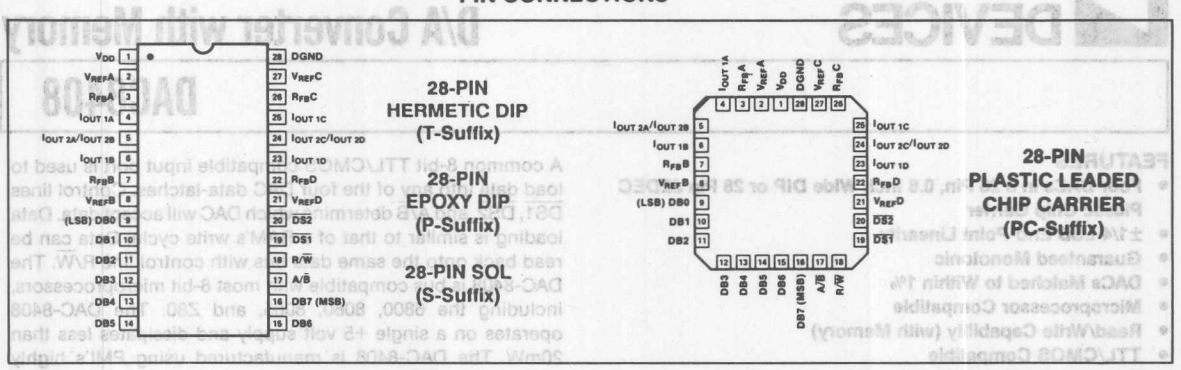
PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

V_{DD} to $I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$ ..... 0, +7V
V_{DD} to DGND ..... 0, +7V
$I_{OUT\ 1A}$, $I_{OUT\ 1B}$,
$I_{OUT\ 1C}$, $I_{OUT\ 1D}$ to DGND ..... –0.3V to V_{DD} + 0.3V
$R_{FB}A$, $R_{FB}B$, $R_{FB}C$, $R_{FB}D$ to I_{OUT} ..... ±25V
$I_{OUT\ 2A}$, $I_{OUT\ 2B}$,
$I_{OUT\ 2C}$, $I_{OUT\ 2D}$ to DGND ..... –0.3V to V_{DD} + 0.3V
DB0 through DB7 to DGND ..... –0.3V to V_{DD} + 0.3V
Control Logic
Input Voltage to DGND ..... –0.3V + V_{DD} + 0.3V
$V_{REF}A$, $V_{REF}B$, $V_{REF}C$, $V_{REF}D$ to
$I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$ ..... ±25V
Operating Temperature Range
Commercial Grade (GP) ..... 0°C to +70°C
Industrial Grade (ET, FT, FP, FPC, FS) ..... –40°C to +85°C
Military Grade (AT, BT) ..... –55°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
28-Pin Hermetic DIP (T)	55	10	°C/W
28-Pin Plastic DIP (P)	53	27	°C/W
28-Pin SOL (S)	68	23	°C/W
28-Contact PLCC (PC)	66	29	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} + 0.3V or less than –0.3V potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high-energy electrostatic fields. Keep in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = ±10V; V_{OUT}A, B, C, D = 0V; T_A = –55°C to +125°C apply for DAC-8408AT/BT, T_A = –40°C to +85°C apply for DAC-8408ET/FT/FP/FPC/FS; T_A = 0°C to +70°C apply for DAC-8408GP, unless otherwise noted. Specifications apply for DAC A, B, C, & D.

PARAMETER	SYMBOL	CONDITIONS	DAC-8408 MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		8	—	—	Bits
Nonlinearity (Notes 1, 2)	INL	DAC-8408A/E/G	—	—	±1/4	LSB
		DAC-8408B/F/H	—	—	±1/2	
Differential Nonlinearity	DNL	DAC-8408A/E/G	—	—	±1/2	LSB
		DAC-8408B/F/H	—	—	±1	
Gain Error	G_{FSE}	(Using Internal R_{FB})	—	—	±1	LSB
Gain Tempco (Notes 3, 6)	TC_{GFS}		—	±2	±40	ppm/°C
Power Supply Rejection (ΔV_{DD} = ±10%)	PSR		—	—	0.001	%FSR/%
$I_{OUT\ 1A, B, C, D}$ Leakage Current (Note 13)	I_{LKG}	T_A = +25°C	—	—	±30	nA
		T_A = Full Temp. Range	—	—	±100	

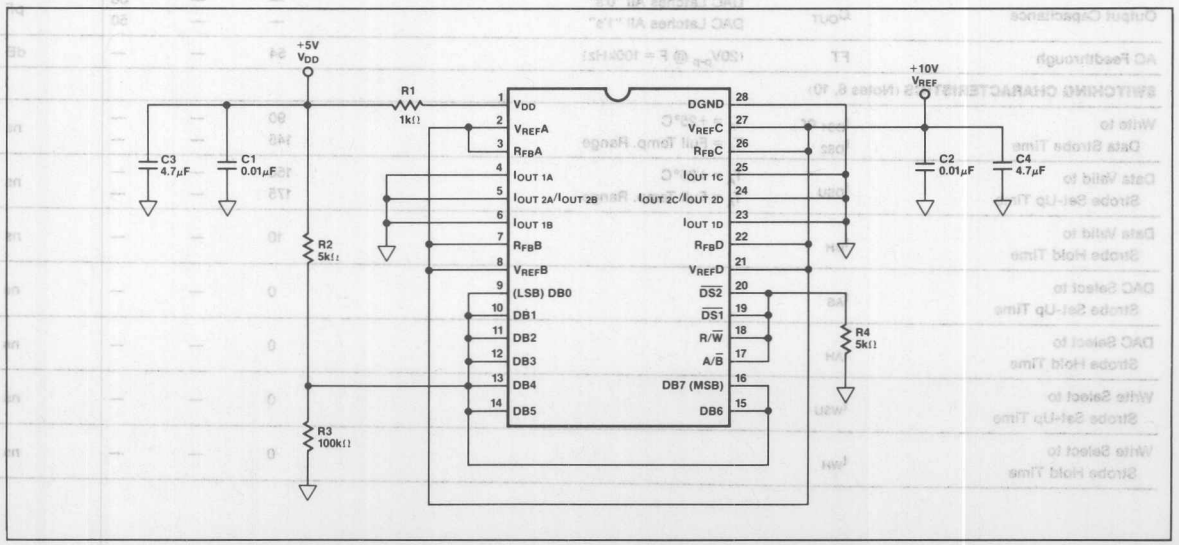
ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = ±10V; V_{OUT}A, B, C, D = 0V; T_A = –55°C to +125°C apply for DAC-8408AT/BT, T_A = –40°C to +85°C apply for DAC-8408ET/FT/FP/FPC/FS; T_A = 0°C to +70°C apply for DAC-8408GP, unless otherwise noted. Specifications apply for DAC A, B, C, & D. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8408 MIN	TYP	MAX	UNITS
REFERENCE INPUT						
Input Voltage Range			—	—	±20	V
Input Resistance Match (Note 4)		$R_{A, B, C, D}$	—	—	±1	%
Input Resistance	R_{IN}		6	10	14	kΩ
DIGITAL INPUTS						
Digital Input Low	V_{IL}		—	—	0.8	V
Digital Input High	V_{IH}		2.4	—	—	V
Input Current (Note 5)	I_{IN}	T_A = +25°C T_A = Full Temp. Range	— —	±0.01 —	±1.0 ±10.0	µA
Input Capacitance (Note 6)	C_{IN}		—	—	8	pF
DATA BUS OUTPUTS						
Digital Output Low	V_{OL}	1.6mA Sink	—	—	0.4	V
Digital Output High	V_{OH}	400µA Source	4	—	—	V
Output Leakage Current	I_{LKG}	T_A = +25°C T_A = Full Temp. Range	— —	±0.005 ±0.075	±1.0 ±10.0	µA
DAC OUTPUTS (Note 6)						
Propagation Delay (Note 7)	t_{pD}		—	150	180	ns
Settling Time (Notes 11, 12)	t_s		—	190	250	ns
Output Capacitance	C_{OUT}	DAC Latches All "0's" DAC Latches All "1's"	— —	— —	30 50	pF
AC Feedthrough	FT	($20V_{p-p}$ @ F = 100kHz)	54	—	—	dB
SWITCHING CHARACTERISTICS (Notes 6, 10)						
Write to Data Strobe Time	t_{DS1} or t_{DS2}	T_A = +25°C T_A = Full Temp. Range	90 145	— —	— —	ns
Data Valid to Strobe Set-Up Time	t_{DSU}	T_A = +25°C T_A = Full Temp. Range	150 175	— —	— —	ns
Data Valid to Strobe Hold Time	t_{DH}		10	—	—	ns
DAC Select to Strobe Set-Up Time	t_{AS}		0	—	—	ns
DAC Select to Strobe Hold Time	t_{AH}		0	—	—	ns
Write Select to Strobe Set-Up Time	t_{WSU}		0	—	—	ns
Write Select to Strobe Hold Time	t_{WH}		0	—	—	ns

PARAMETER	SYMBOL	CONDITIONS	DAC-8408 MIN	TYP	MAX	UNITS
Read to Data Strobe Width	t_{RDS}	T_A = +25°C	220	—	—	ns
		T_A = Full Temp. Range	350	—	—	
Data Strobe to Output Valid Time	t_{CO}	T_A = +25°C	320	—	—	ns
		T_A = Full Temp. Range	430	—	—	
Output Data to Deselect Time	t_{OTD}	T_A = +25°C	200	—	—	ns
		T_A = Full Temp. Range	270	—	—	
Read Select to Strobe Set-Up Time	t_{RSU}		0	—	—	ns
Read Select to Strobe Hold Time	t_{RH}		0	—	—	ns
POWER SUPPLY						
Voltage Range	V_{DD}		4.5	—	5.5	V
Supply Current (Note 8)	I_{DD}		—	—	50	µA
Supply Current (Note 9)	I_{DD}	T_A = +25°C	—	—	1.0	mA
		T_A = Full Temp. Range	—	—	1.5	

NOTES:
1. This is an end-point linearity specification.
2. Guaranteed to be monotonic over the full operating temperature range.
3. ppm/°C of FSR (FSR = Full Scale Range = V_{REF} – 1 LSB.)
4. Input Resistance Temperature Coefficient = +300ppm/°C.
5. Logic Inputs are MOS gates. Typical input current at +25°C is less than 10nA.
6. Guaranteed by design.
7. From Digital Input to 90% of final analog output current.
8. All Digital Inputs "0" or V_{DD}.
9. All Digital Inputs V_{IH} or V_{IL}.
10. See Timing Diagram.
11. Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
12. Extrapolated: t_s (1/2 LSB) = t_{pD} + 6.2τ where τ = the measured first time constant of the final RC decay.
13. All Digital Inputs = 0V; V_{REF} = +10V.

BURN-IN CIRCUIT



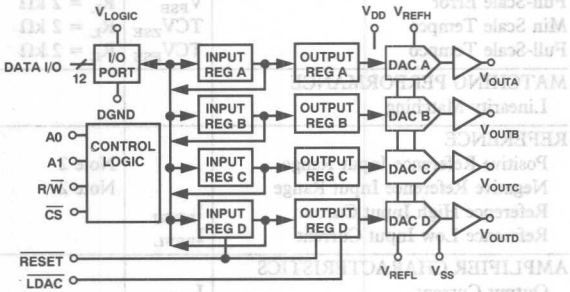
FEATURES

- +5 to ±15 Volt Operation
- Unipolar or Bipolar Operation
- True Voltage Output
- Double-Buffered Inputs
- Reset to Min or Center Scale
- Fast Bus Access Time
- Readback

APPLICATIONS

- Automatic Test Equipment
- Digitally Controlled Calibration
- Servo Controls
- Process Control Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC-8412 and DAC-8413 are quad, 12-bit, voltage output DACs with readback capability. Built using a complementary BiCMOS process, these monolithic DACs offer the user very high package density.

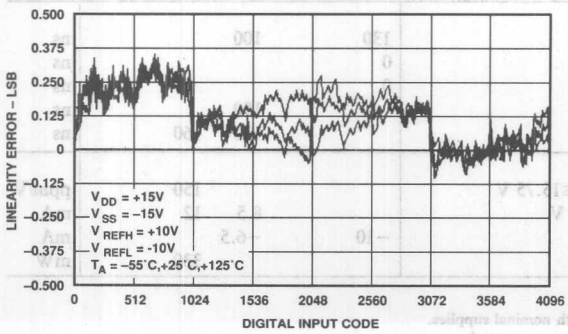
Output voltage swing is set by the two reference inputs V_{REFH} and V_{REFL}. By setting the V_{REFL} input to 0 volts and V_{REFH} to a positive voltage, the DAC will provide a unipolar positive output range. A similar configuration with V_{REFH} at 0 volts and V_{REFL} at a negative voltage will provide a unipolar negative output range. Bipolar outputs are configured by connecting both V_{REFH} and V_{REFL} to nonzero voltages. This method of setting output voltage range has advantages over other bipolar offsetting methods because it is not dependent on internal and external resistors with different temperature coefficients.

Digital controls allow the user to load or read back data from any DAC, load any DAC and transfer data to all DACs at one time.

An active low $\overline{\text{RESET}}$ loads all DAC output registers to mid-scale for the DAC-8412 and zero scale for the DAC-8413.

The DAC-8412/DAC-8413 are available in 28-pin plastic DIP, cerdip, PLCC and LCC packages. They can be operated from a wide variety of supply and reference voltages with supplies ranging from single +5 volt to ±15 volts, and references from +2.5 to ±10 volts. Power dissipation is less than 330 mW with ±15 volt supplies and only 60 mW with a +5 volt supply.

For MIL-STD-883 applications, contact your local ADI sales office for the DAC-8412/DAC-8413/883 data sheet which specifies operation over the −55°C to +125°C temperature range. All 883 parts are also available as Standard Military Drawings 5962-91-76401MXA through -76404M3A.



INL VS. CODE OVER TEMPERATURE

ORDERING INFORMATION[1]

INL (LSB)	Military[2] Temperature −55°C to +125°C	Extended Industrial[2] Temperature −40°C to +85°C	Package	Package Option[3]
±1		DAC8412FPC	PLCC	P-28A
±1.5	DAC8412BTC/883		LCC	E-28A
±0.5		DAC8412ET	Cerdip	Q-28
±0.75	DAC8412AT/883		Cerdip	Q-28
±1		DAC8412FT	Cerdip	Q-28
±1.5	DAC8412BT/883		Cerdip	Q-28
±0.5		DAC8412EP	Plastic	N-28
±1		DAC8412FP	Plastic	N-28
±1		DAC8412GBC	Dice	
±1		DAC8413FPC	PLCC	P-28A
±1.5	DAC8413BTC/883		LCC	E-28A
±0.5		DAC8413ET	Cerdip	Q-28
±0.75	DAC8413AT/883		Cerdip	Q-28
±1		DAC8413FT	Cerdip	Q-28
±1.5	DAC8413BT/883		Cerdip	Q-28
±0.5		DAC8413EP	Plastic	N-28
±1		DAC8413FP	Plastic	N-28
±1		DAC8413GBC	Dice	

NOTES

[1]Burn-in is available on extended industrial temperature range parts in cerdip.

[2]A complete /883 data sheet is available. For availability and burn-in information, contact your local sales office.

[3]For outline information see Package Information section.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

DAC8412/DAC8413—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

($@ V_{DD} = +15.0$ V, $V_{SS} = -15.0$ V, $V_{LOGIC} = +5.0$ V, $V_{REFH} = +10.0$ V, $V_{REFL} = -10.0$ V, $-40°C \le T_A \le +85°C$ unless otherwise specified. See Note 1 for supply variations.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Integral Linearity "E"	INL			0.25	±0.5	LSB
Integral Linearity "F"	INL				±1	LSB
Differential Linearity	DNL	Monotonic Over Temperature	−1			LSB
Min Scale Error	V_{ZSE}	$R_L = 2$ kΩ			±2	LSB
Full-Scale Error	V_{FSE}	$R_L = 2$ kΩ			±2	LSB
Min Scale Tempco	TCV_{ZSE}	$R_L = 2$ kΩ		15		ppm/°C
Full-Scale Tempco	TCV_{FSE}	$R_L = 2$ kΩ		20		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching				±1		LSB
REFERENCE						
Positive Reference Input Range		Note 2	$V_{REFL} + 2.5$		$V_{DD} - 2.5$	V
Negative Reference Input Range		Note 2	−10		$V_{REFH} - 2.5$	V
Reference High Input Current	I_{REFH}		−2.75	+1.5	+2.75	mA
Reference Low Input Current	I_{REFL}		0	+2	+2.75	mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}		−5		+5	mA
Settling Time	t_S	to 0.01%		6		µsec
Slew Rate	SR	10% to 90%		2.2		V/µsec
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}	$T_A = +25°C$	2.4			V
Logic Input Low Voltage	V_{INL}	$T_A = +25°C$			0.8	V
Logic Output High Voltage	V_{OH}	$I_{OH} = +0.4$ mA	2.4			V
Logic Output Low Voltage	V_{OL}	$I_{OL} = -1.6$ mA			0.4	V
Logic Input Current	I_{IN}				1	µA
Input Capacitance	C_{IN}			8		pF
Crosstalk				>72		dB
Large Signal Bandwidth		−3 dB, V_{REFH} = 0 to +10 V p–p		160		kHz
LOGIC TIMING CHARACTERISTICS		Note 3				
WRITE						
Chip Select Write Pulse Width	t_{WCS}		80	40		ns
Write Setup	t_{WS}	$t_{WCS} = 80$ ns	0			ns
Write Hold	t_{WH}	$t_{WCS} = 80$ ns	0			ns
Address Setup	t_{AS}		0			ns
Address Hold	t_{AH}		0			ns
Load Setup	t_{LS}		70	30		ns
Load Hold	t_{LH}		30	10		ns
Write Data Setup	t_{WDS}	$t_{WCS} = 80$ ns	20			ns
Write Data Hold	t_{WDH}	$t_{WCS} = 80$ ns	0			ns
Load Pulse Width	t_{LWD}		170	130		ns
Reset Pulse Width	t_{RESET}		140	100		ns
READ						
Chip Select Read Pulse Width	t_{RCS}		130	100		ns
Read Data Hold	t_{RDH}	$t_{RCS} = 130$ ns	0			ns
Read Data Setup	t_{RDS}	$t_{RCS} = 130$ ns	0			ns
Data to Hi Z	t_{DZ}	$C_L = 10$ pF		150		ns
Chip Select to Data	t_{CSD}	$C_L = 100$ pF		120	160	ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSS	$14.25 \text{ V} \le V_{DD} \le 15.75$ V			150	ppm/V
Positive Supply Current	I_{DD}	$V_{REFH} = +2.5$ V		8.5	12	mA
Negative Supply Current	I_{SS}		−10	−6.5		mA
Power Dissipation	P_{DISS}				330	mW

NOTES

[1]All supplies can be varied ±5%, and operation is guaranteed. Device is tested with nominal supplies.

[2]Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

[3]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

(@ $V_{DD} = V_{LOGIC} = +5.0$ V ±5%, $V_{SS} = 0.0$ V, $V_{REFH} = 2.5$ V, $V_{REFL} = 0.0$ V, and $V_{SS} = -5.0$ V ±5%, $V_{REFL} = -2.5$ V, $-40°C \le T_A \le +85°C$ unless otherwise specified. See Note 1 for supply variations.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Integral Linearity "E"	INL			1/2	±1	LSB
Integral Linearity "F"	INL				±2	LSB
Integral Linearity "E"	INL	$V_{SS} = 0.0$ V; Note 2			±2	LSB
Integral Linearity "F"	INL	$V_{SS} = 0.0$ V; Note 2			±4	LSB
Differential Linearity	DNL	Monotonic Over Temp	−1			LSB
Min Scale Error	V_{ZSE}	$V_{SS} = -5.0$ V			±4	LSB
Full-Scale Error	V_{FSE}	$V_{SS} = -5.0$ V			±4	LSB
Min Scale Error	V_{ZSE}	$V_{SS} = 0.0$ V			±8	LSB
Full-Scale Error	V_{FSE}	$V_{SS} = 0.0$ V			±8	LSB
Min Scale Tempco	TCV_{ZSE}			100		ppm/°C
Full-Scale Tempco	TCV_{FSE}			100		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching				±1		LSB
REFERENCE						
Positive Reference Input Range		Note 3	$V_{REFL} + 2.5$		$V_{DD} - 2.5$	V
Negative Reference Input Range		$V_{SS} = 0.0$ V	0		$V_{REFH} - 2.5$	V
Negative Reference Input Range		$V_{SS} = -5.0$ V	−2.5		$V_{REFH} - 2.5$	V
Reference High Input Current	I_{REFH}	Code 000H	−1.0		+1.0	mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}		−1.25		+1.25	mA
Settling Time	t_S	to 0.01%		6		µs
Slew Rate	SR	10% to 90%		2.2		V/µs
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}	$T_A = +25°C$	2.4			V
Logic Input Low Voltage	V_{INL}	$T_A = +25°C$			0.8	V
Logic Output High Voltage	V_{OH}	$I_{OH} = +0.4$ mA	2.4			V
Logic Output Low Voltage	V_{OL}	$I_{OL} = -1.6$ mA			0.45	V
Logic Input Current	I_{IN}				1	µA
Input Capacitance	C_{IN}			8		pF
LOGIC TIMING CHARACTERISTICS		Note 4				
WRITE						
Chip Select Write Pulse Width	t_{WCS}		150	90		ns
Write Setup	t_{WS}	$t_{WCS} = 150$ ns	0			ns
Write Hold	t_{WH}	$t_{WCS} = 150$ ns	0			ns
Address Setup	t_{AS}		0			ns
Address Hold	t_{AH}		0			ns
Load Setup	t_{LS}		70	30		ns
Load Hold	t_{LH}		50	20		ns
Write Data Setup	t_{WDS}	$t_{WCS} = 150$ ns	20			ns
Write Data Hold	t_{WDH}	$t_{WCS} = 150$ ns	0			ns
Load Pulse Width	t_{LWD}		180	130		ns
Reset Pulse Width	t_{RESET}		150	110		ns
READ						
Chip Select Read Pulse Width	t_{RCS}		170	120		ns
Read Data Hold	t_{RDH}	$t_{RCS} = 170$ ns	20			ns
Read Data Setup	t_{RDS}	$t_{RCS} = 170$ ns	0			ns
Data to Hi Z	t_{DZ}	$C_L = 10$ pF		200		ns
Chip Select to Data	t_{CSD}	$C_L = 100$ pF		220	320	ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSS			100		ppm/V
Positive Supply Current	I_{DD}			7	12	mA
Negative Supply Current	I_{SS}	$V_{SS} = -5.0$ V	−10			mA

NOTES

[1]All supplies can be varied ±5%, and operation is guaranteed. Device is tested with $V_{DD} = +4.75$ V.

[2]For single supply operation only ($V_{REFL} = 0.0$ V, $V_{SS} = 0.0$ V): Due to internal offset errors, INL and DNL are measured beginning at code 2 (002_H).

[3]Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

[4]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

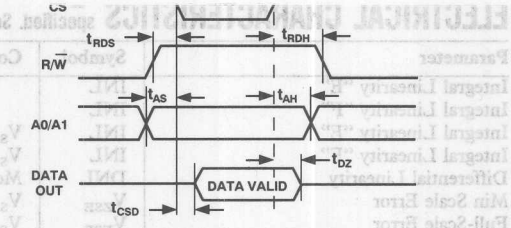
Specifications subject to change without notice.

V_{SS} to V_{DD} . . . . . −0.3 V, +33.0 V
V_{SS} to V_{LOGIC} . . . . . −0.3 V, +33.0 V
V_{LOGIC} to DGND . . . . . −0.3 V, +18.0 V
V_{SS} to V_{REFL} . . . . . −0.3 V, $+V_{SS}$−2.0 V
V_{REFH} to V_{DD} . . . . . +2.0 V, +33.0 V
V_{REFH} to V_{REFL} . . . . . +2.0 V, V_{SS}−V_{DD}
Current into Any Pin[4] . . . . . ±15 mA
Digital Input Voltage to DGND . . . . −0.3 V, V_{LOGIC} +0.3 V
Digital Output Voltage to DGND . . . . . −0.3 V, +7.0 V
Operating Temperature Range
ET, FT, EP, FP, FPC . . . . . −40°C to +85°C
AT, BT, BTC . . . . . −55°C to +125°C
Dice Junction Temperature . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Power Dissipation Package . . . . . 1000 mW
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

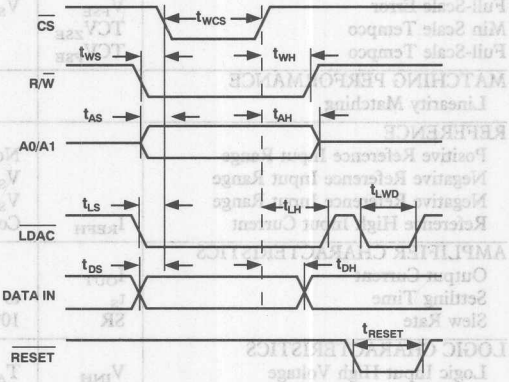
Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Units
28-Pin Hermetic DIP (T)	50	7	°C/W
28-Pin Plastic DIP (P)	48	22	°C/W
28-Lead Hermetic Leadless Chip Carrier (TC)	70	28	°C/W
28-Lead Plastic Leaded Chip Carrier (PC)	63	25	°C/W

NOTE
[1]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket.



Data Output (Read) Timing



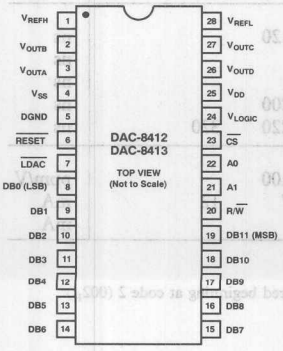
Data WRITE (Input and Output Registers) Timing

CAUTION

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures.
3. Remove power before inserting or removing units from their sockets.
4. Analog outputs are protected from short circuit to ground or either supply.

PIN CONFIGURATIONS

DIP



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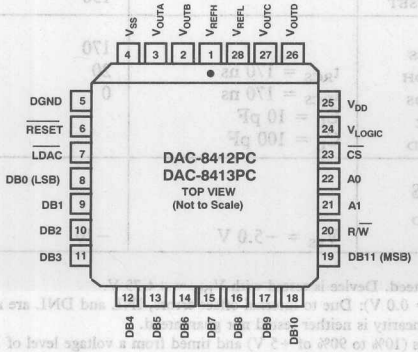
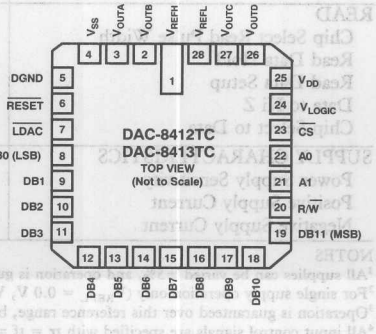


LCC



Quad 12-Bit Serial Voltage-Output DAC

DAC8420

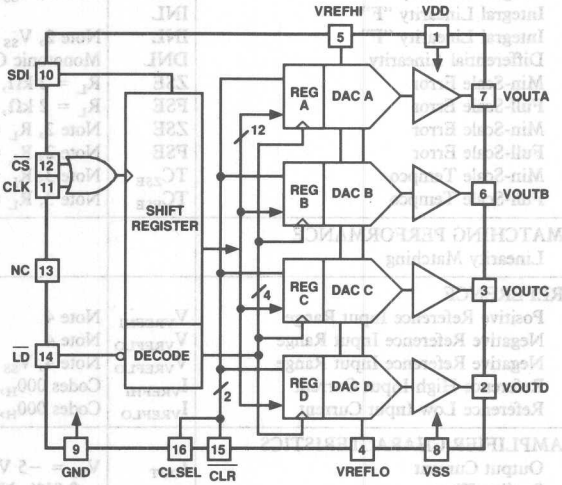
FEATURES

Guaranteed Monotonic Over Temperature
Excellent Matching Between DACs
Unipolar or Bipolar Operation
Buffered Voltage Outputs
High Speed Serial Digital Interface
Reset to Zero- or Center-Scale
Wide Supply Range, +5 V-Only to ±15 V
Low Power Consumption (35 mW max)
Available in 16-Pin DIP and SOL Packages

APPLICATIONS

Software Controlled Calibration
Servo Controls
Process Control and Automation
ATE

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC-8420 is a quad, 12-bit voltage-output DAC with serial digital interface, in a 16-pin package. Utilizing BiCMOS technology, this monolithic device features unusually high circuit density and low power consumption. The simple, easy-to-use serial digital input and fully buffered analog voltage outputs require no external components to achieve specified performance.

The three-wire serial digital input is easily interfaced to microprocessors running at 10 MHz rates, with minimal additional circuitry. Each DAC is addressed individually by a 16-bit serial word consisting of a 12-bit data word and an address header. The user-programmable reset control $\overline{CLR}$ forces all four DAC outputs to either zero- or midscale, asynchronously overriding the current DAC register values. The output voltage range, determined by the inputs VREFHI and VREFLO, is set by the user for positive or negative unipolar or bipolar signal swings within the supplies allowing considerable design flexibility.

The DAC-8420 is available in 16-pin epoxy DIP, cerdip, and wide-body SOL (small-outline surface mount) packages. Operation is specified with supplies ranging from +5 V-only to ±15 V, with references of +2.5 V to ±10 V respectively. Power dissipation when operating from ±15 V supplies is less than 255 mW (max), and only 35 mW (max) with a +5 V supply.

For applications requiring product meeting MIL-STD-883, contact your local sales office for the DAC-8420/883 data sheet, which specifies operation over the −55°C to +125°C temperature range.

DAC8420—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (at V_{DD} = +5.0 V ± 5%, V_{SS} = 0.0 V, V_{VREFHI} = +2.5 V, V_{VREFLO} = 0.0 V, and V_{SS} = −5.0 V ± 5%, V_{VREFLO} = −2.5 V, −40°C ≤ T_A ≤ +85°C unless otherwise noted. See Note 1 for supply variations.)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC ACCURACY						
Integral Linearity "E"	INL			±1/4	±1	LSB
Integral Linearity "E"	INL	Note 2, V_{SS} = 0 V		±1/2	±3	LSB
Integral Linearity "F"	INL			±3/4	±2	LSB
Integral Linearity "F"	INL	Note 2, V_{SS} = 0 V		±1	±4	LSB
Differential Linearity	DNL	Monotonic Over Temperature		±1/4	±1	LSB
Min-Scale Error	ZSE	R_L = 2 kΩ, V_{SS} = −5 V			±4	LSB
Full-Scale Error	FSE	R_L = 2 kΩ, V_{SS} = −5 V			±4	LSB
Min-Scale Error	ZSE	Note 2, R_L = 2 kΩ, V_{SS} = 0 V			+8	LSB
Full-Scale Error	FSE	Note 2, R_L = 2 kΩ, V_{SS} = 0 V			±8	LSB
Min-Scale Tempco	TC_{ZSE}	Note 3, R_L = 2 kΩ, V_{SS} = −5 V		±10		ppm/°C
Full-Scale Tempco	TC_{FSE}	Note 3, R_L = 2 kΩ, V_{SS} = −5 V		±10		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching				±1		LSB
REFERENCE						
Positive Reference Input Range	V_{VREFHI}	Note 4	V_{VREFLO}+2.5		V_{DD} −2.5	V
Negative Reference Input Range	V_{VREFLO}	Note 4	V_{SS}		V_{VREFHI} −2.5	V
Negative Reference Input Range	V_{VREFLO}	Note 4, V_{SS} = 0 V	0		V_{VREFHI} −2.5	V
Reference High Input Current	I_{VREFHI}	Codes 000_H, 555_H	−0.75	±0.25	+0.75	mA
Reference Low Input Current	I_{VREFLO}	Codes 000_H, 555_H, V_{SS} = −5 V	−1.0	−0.6		mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}	V_{SS} = −5 V	−1.25		+1.25	mA
Settling Time	t_S	to 0.01%, Note 5		8		µs
Slew Rate	SR	10% to 90%, Note 5		1.5		V/µs
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}				10	µA
Input Capacitance	C_{IN}	Note 3		13		pF
LOGIC TIMING CHARACTERISTICS[3, 6]						
Data Setup Time	t_{DS}		25			ns
Data Hold	t_{DH}		55			ns
Clock Pulse Width HIGH	t_{CH}		90			ns
Clock Pulse Width LOW	t_{CL}		120			ns
Select Time	t_{CSS}		90			ns
Deselect Delay	t_{CSH}		5			ns
Load Disable Time	t_{LD1}		130			ns
Load Delay	t_{LD2}		35			ns
Load Pulse Width	t_{LDW}		80			ns
Clear Pulse Width	t_{CLRW}		150			ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSRR			0.002	0.01	%/%
Positive Supply Current	I_{DD}			4	7	mA
Negative Supply Current	I_{SS}		−6	−3		mA
Power Dissipation	P_{DISS}	V_{SS} = 0 V		20	35	mW

NOTES

[1]All supplies can be varied ±5% and operation is guaranteed. Device is tested with V_{DD} = +4.75 V.

[2]For single-supply operation (V_{VREFLO} = 0 V, V_{SS} = 0 V), due to internal offset errors INL and DNL are measured beginning at code 003_H.

[3]Guaranteed but not tested.

[4]Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

[5]V_{OUT} swing between +2.5 V and −2.5 V with V_{DD} = 5.0 V.

[6]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[7]Typical values indicate performance measured at +25°C.

Specifications subject to change without notice.

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC ACCURACY						
Integral Linearity "E"	INL			±1/4	±1/2	LSB
Integral Linearity "F"	INL			±1/2	±1	LSB
Differential Linearity	DNL	Monotonic Over Temperature		±1/4	±1	LSB
Min-Scale Error	ZSE	R_L = 2 kΩ			±2	LSB
Full-Scale Error	FSE	R_L = 2 kΩ			±2	LSB
Min-Scale Tempco	TC_{ZSE}	Note 2, R_L = 2 kΩ		±4		ppm/°C
Full-Scale Tempco	TC_{FSE}	Note 2, R_L = 2 kΩ		±4		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching				±1		LSB
REFERENCE						
Positive Reference Input Range	V_{VREFHI}	Note 3	V_{VREFLO} +2.5		V_{DD} −2.5	V
Negative Reference Input Range	V_{VREFLO}	Note 3	−10		V_{VREFHI} −2.5	V
Reference High Input Current	I_{VREFHI}	Code 000_H, 555_H	−2.0	±1.0	+2.0	mA
Reference Low Input Current	I_{VREFLO}	Code 000_H, 555_H	−3.5	−2.0		mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}		−5		+5	mA
Settling Time	t_S	to 0.01%, Note 4		13		µs
Slew Rate	SR	10% to 90%, Note 4		2		V/µs
DYNAMIC PERFORMANCE						
Analog Crosstalk		Note 2		>64		dB
Digital Feedthrough		Note 2		>72		dB
Large Signal Bandwidth		−3 dB, V_{VREFHI} = 5 V + 10 V p-p, V_{VREFLO} = −10 V, Note 2		90		kHz
Glitch Impulse		Code Transition = $7FF_H$ to 800_H, Note 2		64		nV-s
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}				10	µA
Input Capacitance	C_{IN}	Note 2		13		pF
LOGIC TIMING CHARACTERISTICS[2, 5]						
Data Setup Time	t_{DS}		25			ns
Data Hold	t_{DH}		20			ns
Clock Pulse Width HIGH	t_{CH}		30			ns
Clock Pulse Width LOW	t_{CL}		50			ns
Select Time	t_{CSS}		55			ns
Deselect Delay	t_{CSH}		15			ns
Load Disable Time	t_{LD1}		40			ns
Load Delay	t_{LD2}		15			ns
Load Pulse Width	t_{LDW}		45			ns
Clear Pulse Width	t_{CLRW}		70			ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSRR			0.002	0.01	%/%
Positive Supply Current	I_{DD}			6	9	mA
Negative Supply Current	I_{SS}		−8	−5		mA
Power Dissipation	P_{DISS}				255	mW

NOTES
[1]All supplies can be varied ±5% and operation is guaranteed.
[2]Guaranteed but not tested.
[3]Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.
[4]V_{OUT} swing between +10 V and −10 V.
[5]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[6]Typical values indicate performance measured at +25°C.
Specifications subject to change without notice.

WAFER TEST LIMITS (at V_{DD} = +15.0 V, V_{SS} = −15.0 V, V_{REFHI} = +10.0 V, V_{REFLO} = −10.0 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	DAC-8420G Limit	Units
Integral Linearity	INL		±1	LSB max
Differential Linearity	DNL		±1	LSB max
Min-Scale Offset			±1	LSB max
Max-Scale Offset			±1	LSB max
Logic Input High Voltage	V_{INH}		2.4	V min
Logic Input Low Voltage	V_{INL}		0.8	V max
Logic Input Current	I_{IN}		1	µA max
Positive Supply Current	I_{DD}		8	mA max
Negative Supply Current	I_{SS}		7	mA max

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

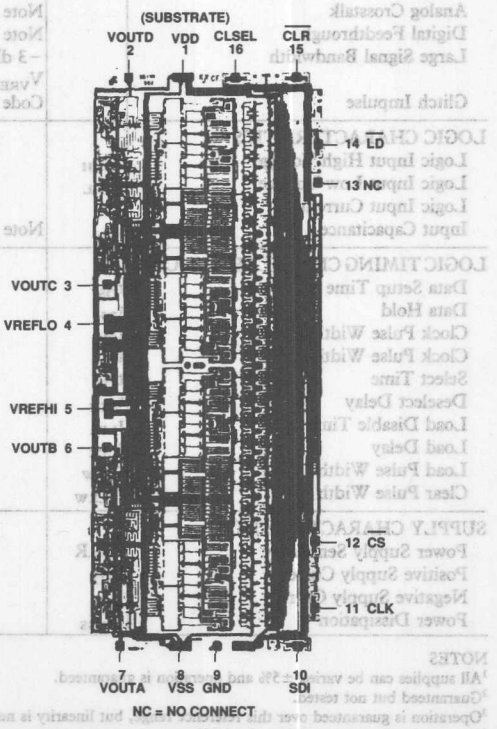
VDD to GND . . . . . −0.3 V, +18.0 V
VSS to GND . . . . . +0.3 V, −18.0 V
VSS to VDD . . . . . −0.3 V, +36.0 V
V_{SS} to V_{VREFLO} . . . . . −0.3 V, V_{SS} − 2.0 V
V_{VREFHI} to V_{VREFLO} . . . . . +2.0 V, V_{DD} − V_{SS}
V_{VREFHI} to V_{DD} . . . . . +2.0 V, +33.0 V
I_{VREFHI}, I_{VREFLO} . . . . . 10 mA
Digital Input Voltage to GND . . . . . −0.3 V, V_{DD} +0.3 V
Output Short Circuit Duration . . . . . Indefinite
Operating Temperature Range
EP, FP, ES, FS, EQ, FQ . . . . . −40°C to +85°C
Dice Junction Temperature . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Power Dissipation . . . . . 1000 mW
Lead Temperature (Soldering, 60 sec) . . . . . 300°C

Package Type	Thermal Resistance θ_{JA}	θ_{JC}	Units
16-Pin Plastic DIP (P)	70[1]	27	°C/W
16-Pin Hermetic DIP (Q)	82[1]	9	°C/W
16-Lead Small Outline Surface Mount (S)	86[2]	22	°C/W

NOTES
[1]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket.
[2]θ_{JA} is specified for device on board.

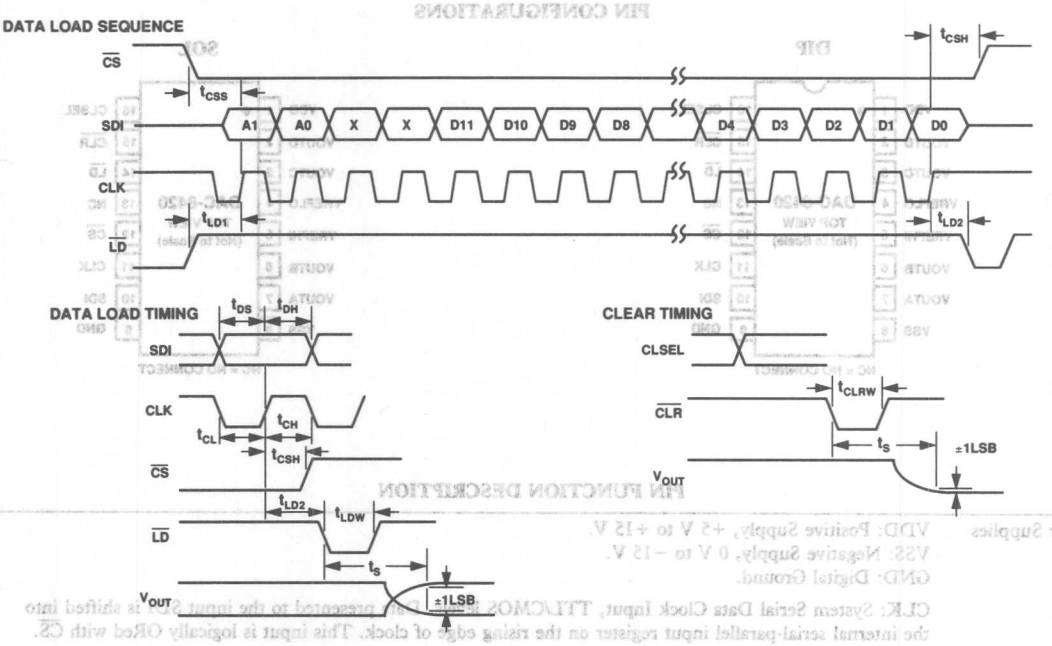
CAUTION
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures.
3. Remove power before inserting or removing units from their sockets.
4. Analog Outputs are protected from short circuits to ground or either supply.

DICE CHARACTERISTICS

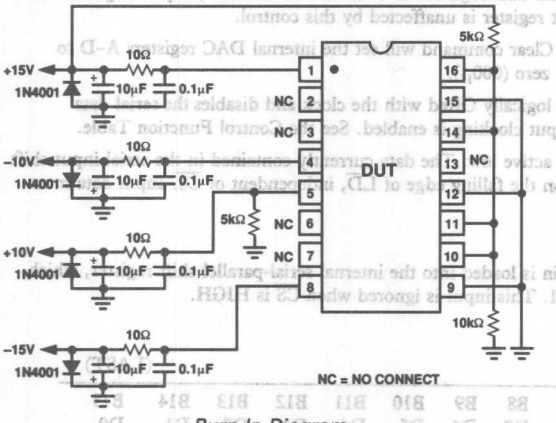


Die Size 0.119 × 0.283 inch, 33,677 sq. mils
(3.023 X 7.188 mm, 21.73 sq. mm)
Transistor Count 2,207

For additional DICE ordering information, refer to databook.



Timing Diagram

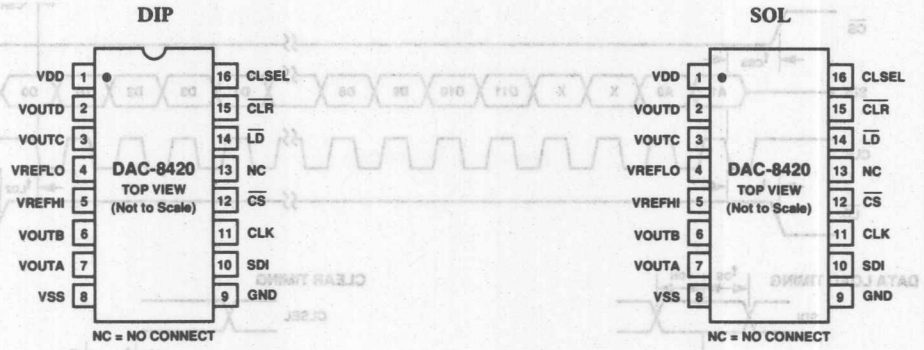


Burn-In Diagram

ORDERING GUIDE

Model[1]	Temperature Range	INL (±LSB)	Package Description	Package Option[2]
DAC8420EP	–40°C to +85°C	0.5	Plastic DIP	N-16
DAC8420EQ	–40°C to +85°C	0.5	Cerdip	Q-16
DAC8420ES	–40°C to +85°C	0.5	SOIC	SOL-16
DAC8420FP	–40°C to +85°C	1.0	Plastic DIP	N-16
DAC8420FQ	–40°C to +85°C	1.0	Cerdip	Q-16
DAC8420FS	–40°C to +85°C	1.0	SOIC	SOL-16
DAC8420GBC	–40°C to +85°C	1.0	Dice[3]	

NOTES
[1]A complete /883 data sheet is available. For availability and burn-in information, contact your local sales office.
[2]PMI division letter designator. For outline information see Package Information section.
[3]Dice tested at 25°C only.



PIN FUNCTION DESCRIPTION

Power Supplies

VDD: Positive Supply, +5 V to +15 V.
VSS: Negative Supply, 0 V to −15 V.
GND: Digital Ground.

Clock

CLK: System Serial Data Clock Input, TTL/CMOS levels. Data presented to the input SDI is shifted into the internal serial-parallel input register on the rising edge of clock. This input is logically ORed with $\overline{CS}$.

Control Inputs

(All are CMOS/TTL compatible.)

$\overline{CLR}$: Asynchronous Clear, active low. Sets internal data registers A–D to zero or midscale, depending on current state of CLSEL. The data in the serial input shift register is unaffected by this control.

CLSEL: Determines action of $\overline{CLR}$. If HIGH, a Clear command will set the internal DAC registers A–D to midscale (800_H). If LOW, the registers are set to zero (000_H).

$\overline{CS}$: Device Chip Select, active low. This input is logically ORed with the clock and disables the serial data register input when HIGH. When LOW, data input clocking is enabled. See the Control Function Table.

$\overline{LD}$: Asynchronous DAC Register Load Control, active low. The data currently contained in the serial input shift register is shifted out to the DAC data registers on the falling edge of $\overline{LD}$, independent of $\overline{CS}$. Input data must remain stable while $\overline{LD}$ is LOW.

Data Input

(All are CMOS/TTL compatible.)

SDI: Serial Data Input. Data presented to this pin is loaded into the internal serial-parallel shift register, which shifts data in beginning with DAC address Bit A1. This input is ignored when $\overline{CS}$ is HIGH.

The format of the 16-bit serial word is:

(FIRST)															(LAST)
B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
A1	A0	NC	NC	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
—Address Word—				(MSB)			—DAC Data Word—								(LSB)

NC = Don't Care.

Reference Inputs

VREFHI: Upper DAC ladder reference voltage input. Allowable range is (V_{DD} −2.5 V) to (V_{VREFLO} +2.5 V).

VREFLO: Lower DAC ladder reference voltage input, equal to zero scale output. Allowable range is V_{SS} to (V_{VREFHI} −2.5 V).

Analog Outputs

VOUTA through VOUTD: Four buffered DAC voltage outputs.

Table I. Control Function Logic Table

CLK[1]	$\overline{CS}$[1]	$\overline{LD}$	$\overline{CLR}$	CLSEL	Serial Input Shift Register	DAC Registers A–D
NC	H	H	L	H	No Change	Loads Midscale Value (800_H)
NC	H	H	L	L	No Change	Loads Zero-Scale Value (000_H)
NC	H	H	↑	H/L	No Change	Latches Value
↑	L	H	H	NC	Shifts Register One Bit.	No Change
L	↑	H	H	NC	Shifts Register One Bit.	No Change
H	NC (↑)	↓	H	NC	No Change	Loads the Serial Data Word[2]
H	NC	L	H	NC	No Change	Transparent[3]
NC	H	H	H	NC	No Change	No Change

NC = Don't Care.

NOTES
[1]$\overline{CS}$ and CLK are interchangeable.
[2]Returning $\overline{CS}$ HIGH while CLK is HIGH avoids an additional "false clock" of serial input data. See Note 1.
[3]Do not clock in serial data while $\overline{LD}$ is LOW.

OPERATION

Introduction

The DAC-8420 is a quad, voltage-output 12-bit DAC with serial digital input, capable of operating from a single +5 V supply. The straightforward serial interface can be connected directly to most popular microprocessors and microcontrollers, and can accept data at a 10 MHz clock rate when operating from ±15 V supplies. A unique voltage reference structure assures maximum utilization of DAC output resolution by allowing the user to set the zero- and full-scale output levels within the supply rails. The analog voltage outputs are fully buffered, and are capable of driving a 2 kΩ load. Output glitch impulse during major code transitions is a very low 64 nV-s (typ).

Digital Interface Operation

The serial input of the DAC-8420, consisting of $\overline{CS}$, SDI, and $\overline{LD}$, is easily interfaced to a wide variety of microprocessor serial ports. As shown in Table I and the Timing Diagram, while $\overline{CS}$ is LOW the data presented to the input SDI is shifted into the internal serial/parallel shift register on the rising edge of the clock, with the address MSB first, data LSB last. The data format, shown above, is two bits of DAC address and two "don't care" fill bits, followed by the 12-bit DAC data word. Once all 16 bits of the serial data word have been input, the load control $\overline{LD}$ is strobed and the word is parallel-shifted out onto the internal data bus. The two address bits are decoded and used to route the 12-bit data word to the appropriate DAC data register. See the Applications Information.

Correct Operation of $\overline{CS}$ and CLK

As mentioned in Table I, the control pins CLK and $\overline{CS}$ require some attention during a data load cycle. Since these two inputs are fed to the same logical "OR" gate, their operation is in fact identical. The user must take care to operate them accordingly in order to avoid clocking in false data bits. As shown in the Timing Diagram, CLK must be either halted HIGH, or $\overline{CS}$ brought HIGH during the last HIGH portion of the CLK following the rising edge which latched in the last data bit. Otherwise, an additional rising edge is generated by $\overline{CS}$ rising while CLK is LOW, causing $\overline{CS}$ to act as the clock and allowing a false data bit into the serial input register. The same issue must be considered in the beginning of the data load sequence also.

Using $\overline{CLR}$ and CLSEL

The CLEAR ($\overline{CLR}$) control allows the user to perform an asynchronous reset function. Asserting $\overline{CLR}$ loads all four DAC data word registers, forcing the DAC outputs to either zero-scale (000_H) or midscale (800_H), depending on the state of CLSEL as shown in the Digital Function Table. The CLEAR function is asynchronous and is totally independent of $\overline{CS}$. When $\overline{CLR}$ returns HIGH, the DAC outputs remain latched at the reset value until $\overline{LD}$ is strobed, reloading the individual DAC data word registers with either the data held in the serial input register prior to the reset, or new data loaded through the serial interface.

Table II. DAC Address Word Decode Table

A1	A0	DAC Addressed
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

Programming the Analog Outputs

The unique differential reference structure of the DAC-8420 allows the user to tailor the output voltage range precisely to the needs of the application. Instead of spending DAC resolution on an unused region near the positive or negative rail, the DAC-8420 allows the user to determine both the upper and lower limits of the analog output voltage range. Thus, as shown in Table III and Figure 1, the outputs of DACs A through D range between VREFHI and VREFLO, within the limits specified in the Electrical Characteristics tables. Note also that VREFHI must be greater than VREFLO.

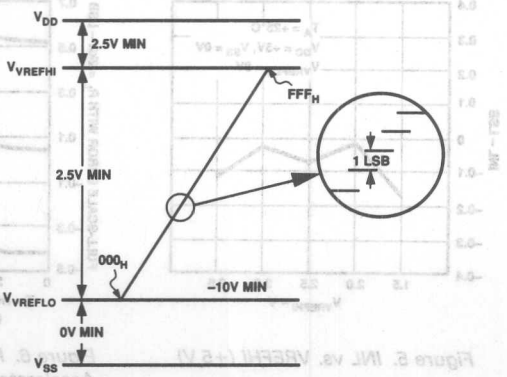


Figure 1. Output Voltage Range Programming

Table III. Analog Output Code

DAC Data Word (HEX)	V_{OUT}	Note
FFF	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 4095$	Full-Scale Output
801	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 2049$	Midscale + 1
800	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 2048$	Midscale
7FF	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 2047$	Midscale − 1
000	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 0$	Zero-Scale

Typical Performance Characteristics

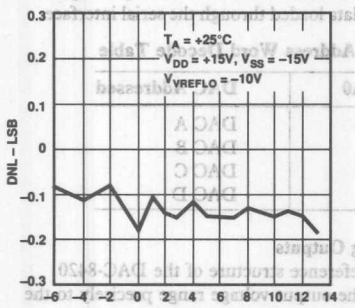


Figure 2. Differential Linearity vs. VREFHI (±15 V)

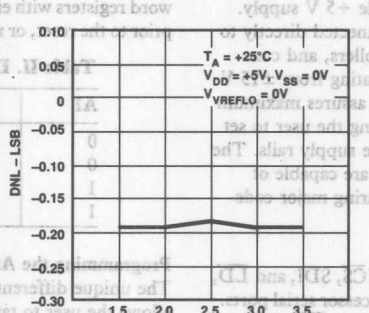


Figure 3. Differential Linearity vs. VREFHI (+5 V)

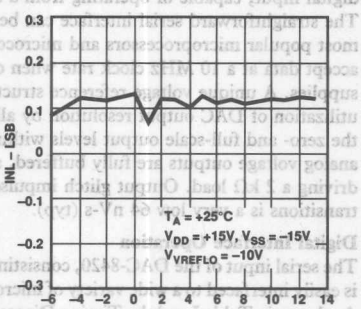


Figure 4. INL vs. VREFHI (±15 V)

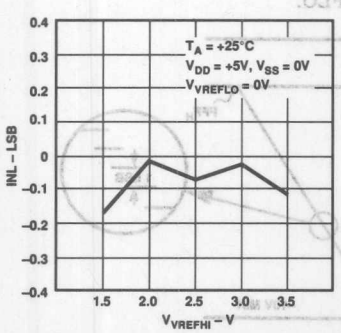


Figure 5. INL vs. VREFHI (+5 V)

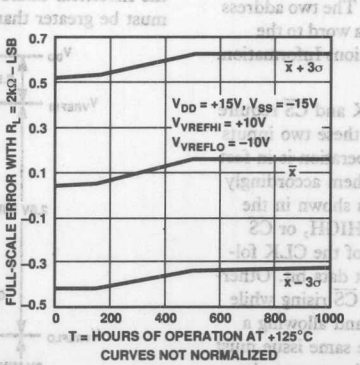


Figure 6. Full-Scale Error vs. Time Accelerated by Burn-In

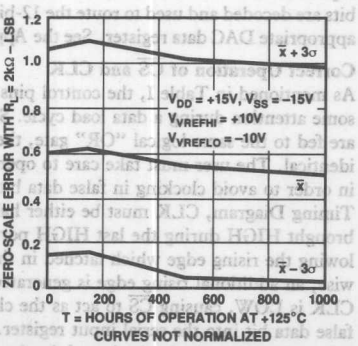


Figure 7. Zero-Scale Error vs. Time Accelerated by Burn-In

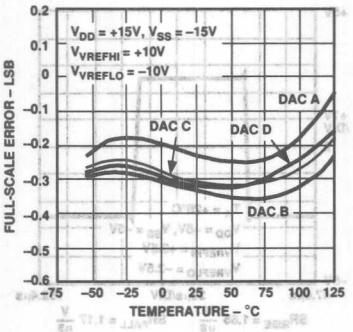


Figure 8. Full-Scale Error vs. Temperature

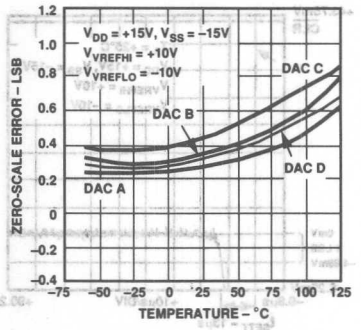


Figure 9. Zero-Scale Error vs. Temperature

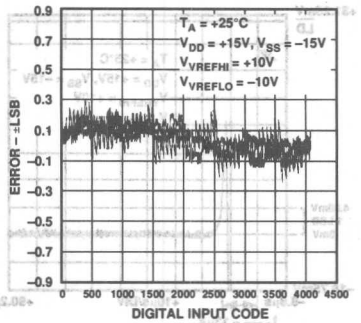


Figure 10. Channel-to-Channel Matching ±15/±10

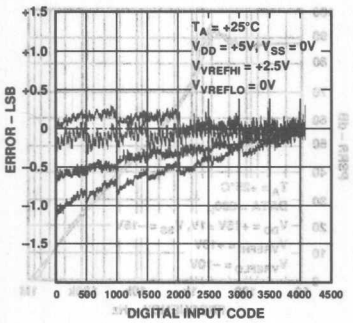


Figure 11. Channel-to-Channel Matching +5/+2.5

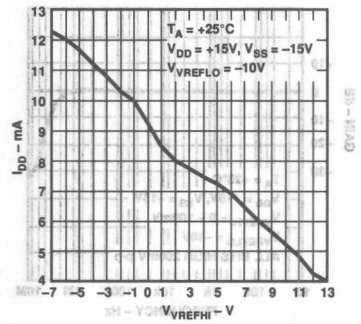


Figure 12. I_{DD} vs. V_{VREFHI}, All DACs HIGH

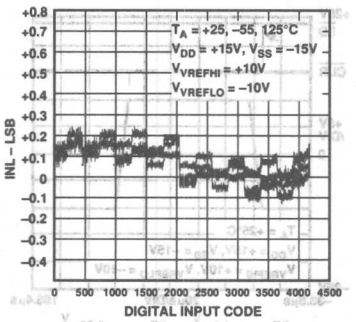


Figure 13. INL vs. Code ±15/±10

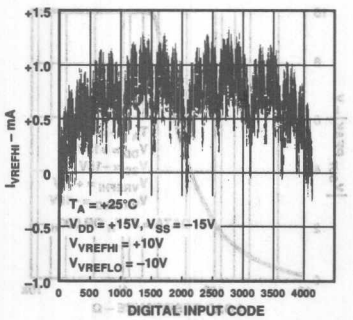


Figure 14. I_{VREFHI} vs. Code

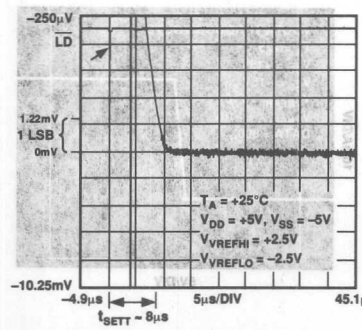


Figure 15. Settling Time (+)(±5 V)

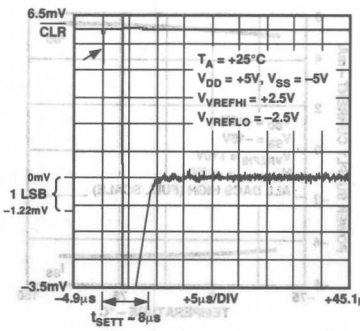


Figure 16. Settling Time (–)(±5 V)

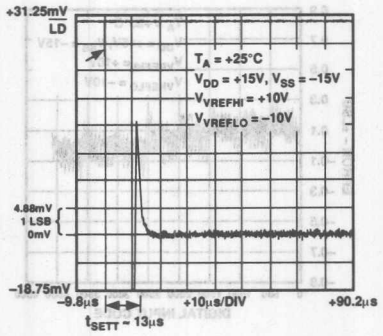


Figure 17. Settling Time (+)(±15 V)

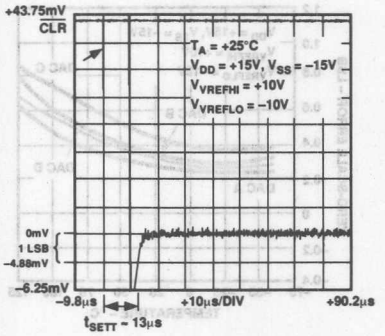


Figure 18. Settling Time (–)(±15 V)

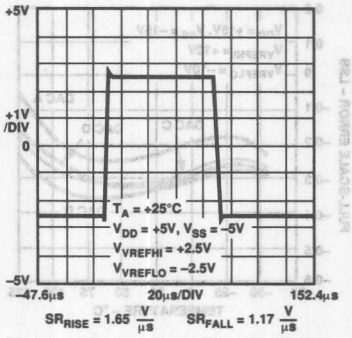


Figure 19. Slew Rate (±5 V)

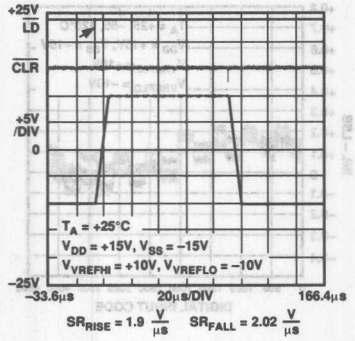


Figure 20. Slew Rate (±15 V)

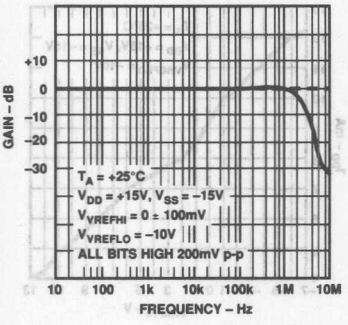


Figure 21. Small-Signal Response

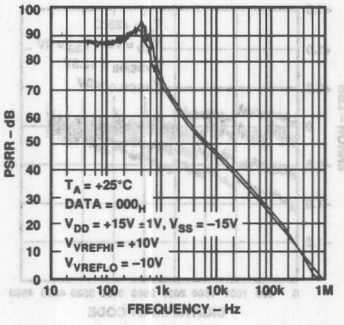


Figure 22. PSRR vs. Frequency

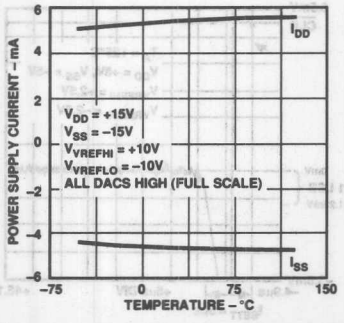


Figure 23. Power Supply Current vs. Temperature

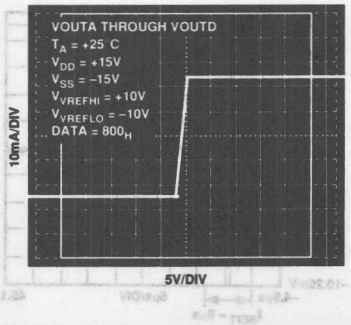


Figure 24. DAC Output Current vs. VOUTX

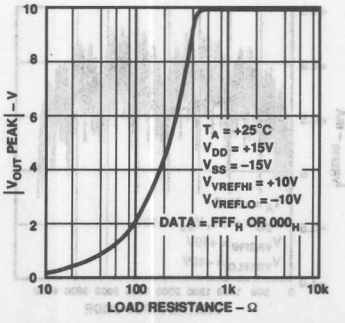


Figure 25. Output Swing vs. Load Resistance

VREFHI Input Requirements

The DAC-8420 utilizes a unique, patented DAC switch driver circuit which compensates for different supply, reference voltage, and digital code inputs. This ensures that all DAC ladder switches are always biased equally, ensuring excellent linearity under all conditions. Thus, as indicated in the specifications, the VREFHI input of the DAC-8420 will require both sourcing and sinking current capability from the reference voltage source. Many positive voltage references are intended as current sources only, and offer little sinking capability. The user should consider references such as the AD584, AD586, AD587, AD588, AD780, and REF-43 in this application.

APPLICATIONS

Power Supply Bypassing and Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The DAC-8420 has a single ground pin that is internally connected to the digital section as the logic reference level. The first thought may be to connect this pin to the digital ground; however, in large systems the digital ground is often noisy because of the switching currents of other digital circuitry. Any noise that is introduced at the ground pin could couple into the analog output. Thus, to avoid error causing digital noise in the sensitive analog circuitry, the ground pin should be connected to the system analog ground. The ground path (circuit board trace) should be as wide as possible to reduce any effects of parasitic inductance and ohmic drops. A ground plane is recommended if possible. The noise immunity of the on-board digital circuitry, typically in the hundreds of millivolts, is well able to reject the common-mode noise typically seen between system analog and digital grounds. Finally, the analog and digital ground should be connected together at a single point in the system to provide a common reference. This is preferably done at the power supply.

Good grounding practice is essential to maintaining analog performance in the surrounding analog support circuitry as well. With two reference inputs, and four analog outputs capable of moderate bandwidth and output current, there is a significant potential for ground loops. Again, a ground plane is recommended as the most effective solution to minimizing errors due to noise and ground offsets.

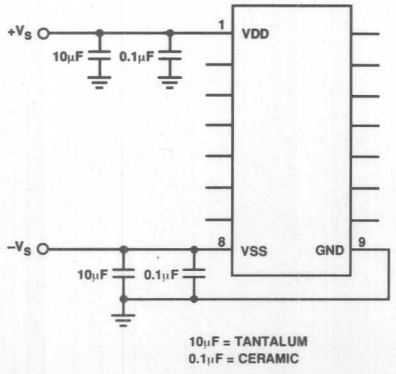


Figure 26. Recommended Supply Bypassing Scheme

The DAC-8420 should have ample supply bypassing, located as close to the package as possible. Figure 26 shows the recommended capacitor values of 10 µF in parallel with 0.1 µF. The 0.1 µF cap should have low "Effective Series Resistance" (ESR) and "Effective Series Inductance" (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching. In order to preserve the specified analog performance of the device, the supply should be as noise free as possible. In the case of 5 V only systems it is desirable to use the same 5 V supply for both the analog circuitry and the digital portion of the circuit. Unfortunately, the typical 5 V supply is extremely noisy due to the fast edge rates of the popular CMOS logic families which induce large inductive voltage spikes, and busy microcontroller or microprocessor busses which commonly have large current spikes during bus activity. However, by properly filtering the supply as shown in Figure 27, the digital 5 V supply can be used. The inductors and capacitors generate a filter that not only rejects noise due to the digital circuitry, but also filters out the lower frequency noise of switch mode power supplies. The analog supply should be connected as close as possible to the origin of the digital supply to minimize noise pick-up from the digital section.

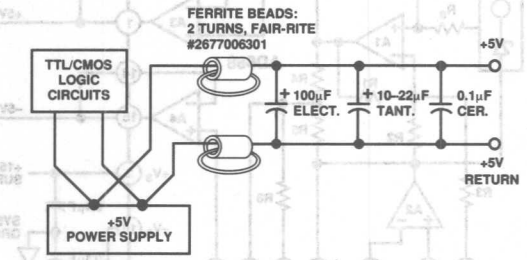


Figure 27. Single-Supply Analog Supply Filter

Analog Outputs

The DAC-8420 features buffered analog voltage outputs capable of sourcing and sinking up to 5 mA when operating from ±15 V supplies, eliminating the need for external buffer amplifiers in most applications while maintaining specified accuracy over the rated operating conditions. The buffered outputs are simply an op amp connected as a voltage follower, and thus have output characteristics very similar to the typical operational amplifier. These amplifiers are short-circuit protected. The designer should verify that the output load meets the capabilities of the device, in terms of both output current and load capacitance. The DAC-8420 is stable with capacitive loads up to 2 nF typical. However, any capacitive load will increase the settling time, and should be minimized if speed is a concern.

The output stage includes a p-channel MOSFET to pull the output voltage down to the negative supply. This is very important in single supply systems, where VREFLO usually has the same potential as the negative supply. With no load, the zero-scale output voltage in these applications will be less than 500 µV typically, or less than 1 LSB when V_{VREFHI} = 2.5 V. However, when sinking current this voltage does increase because of the finite impedance of the output stage. The effective value of the pull-down resistor in the output stage is typically 320 Ω. With a 100 kΩ resistor connected to +5 V, the resulting zero-scale output voltage is 16 mV. Thus, the best single supply operation is obtained with the output load connected to ground, so the output stage does not have to sink current.

Like all amplifiers, the DAC-8420 output buffers do generate voltage noise, 52 nV/$\sqrt{\text{Hz}}$ typically. This is easily reduced by adding a simple RC low-pass filter on each output.

Reference Configuration

The two reference inputs of the DAC-8420 allow a great deal of flexibility in circuit design. The user must take care, however, to observe the minimum voltage input levels on VREFHI and VREFLO to maintain the accuracy shown in the data sheet. These input voltages can be set anywhere across a wide range within the supplies, but must be a minimum of 2.5 V apart in any case. See Figure 1. A wide output voltage range can be obtained with ±5 V references, which can be provided by the AD588 as shown in Figure 28. Many applications utilize the DACs to synthesize symmetric bipolar wave forms, which requires an accurate, low drift bipolar reference. The AD588 provides both voltages and needs no external components. Additionally, the part is trimmed in production for 12-bit accuracy over the full temperature range without user calibration. Performing a Clear with the reset select CLSEL HIGH allows the user to easily reset the DAC outputs to midscale, or zero volts in these applications.

When driving the reference inputs VREFHI and VREFLO, it is important to note that VREFHI both sinks and sources current, and that the input currents of both are code dependent. Many voltage reference products have limited current sinking capability and must be buffered with an amplifier to drive VREFHI, in order to maintain overall system accuracy. The input VREFLO, however, has no such requirement.

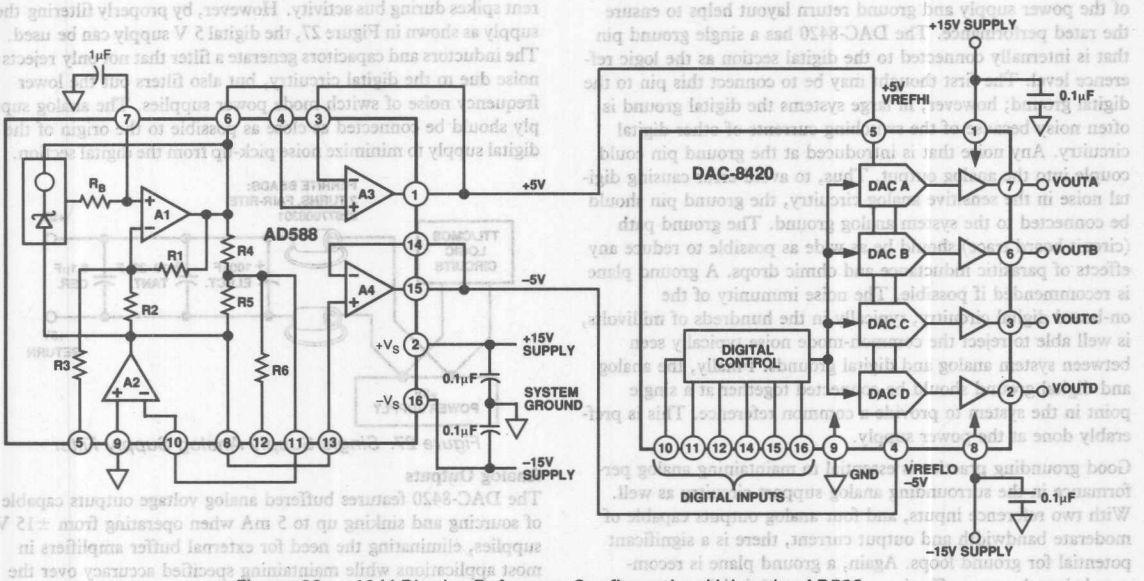


Figure 28. ±10 V Bipolar Reference Configuration Using the AD588

For a single 5 V supply, V_{VREFHI} is limited to at most 2.5 V, and must always be at least 2.5 V less than the positive supply to ensure linearity of the device. For these applications, the REF-43 is an excellent low drift 2.5 V reference that consumes only 450 μA (max). It works well with the DAC-8420 in a single 5 V system as shown in Figure 29.

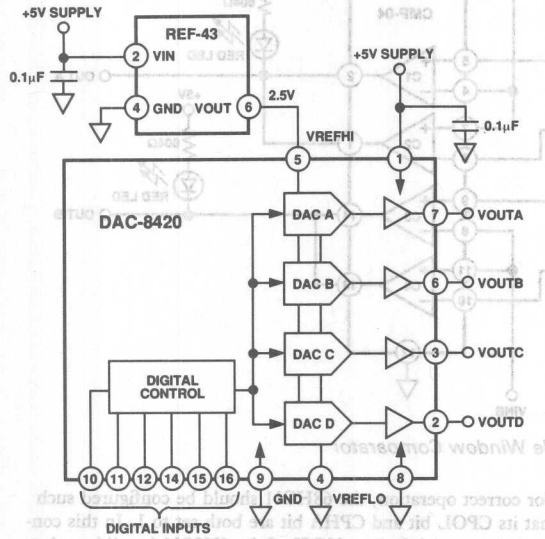


Figure 29. +5 V Single Supply Operation Using REF-43

Isolated Digital Interface

Because the DAC-8420 is ideal for generating accurate voltages in process control and industrial applications, due to noise, safety requirements, or distance, it may be necessary to isolate it from the central controller. This can be easily achieved by using opto-isolators, which are commonly used to provide electrical isolation in excess of 3 kV. Figure 30 shows a simple 3-wire interface scheme to control the clock, data, and load pulse. For normal operation, $\overline{CS}$ is tied permanently LOW so that the DAC-8420 is always selected. The resistor and capacitor on the $\overline{CLR}$ pin provide a power-on reset with 10 ms time constant. The three opto-isolators are used for the SDI, CLK, and $\overline{LD}$ lines.

One opto-isolated line ($\overline{LD}$) can be eliminated from this circuit by adding an inexpensive 4-bit TTL Counter to generate the Load pulse for the DAC-8420 after 16 clock cycles. The counter is used to count of the number of clock cycles loading serial data to the DAC-8420. After all 16 bits have been clocked into the converter, the counter resets, and a load pulse is generated on clock 17. In either circuit, the DAC-8420's serial interface provides a simple, low cost method of isolating the digital control.

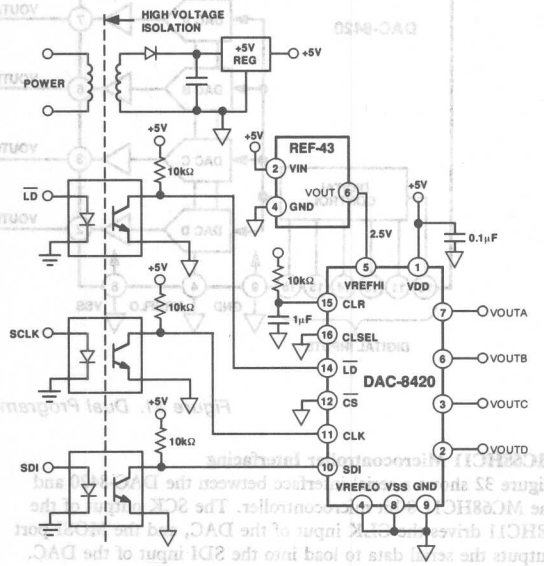


Figure 30. Opto-Isolated 3-Wire Interface

Dual Window Comparator

Often a comparator is needed to signal an out-of-range warning. Combining the DAC-8420 with a quad comparator such as the CMP-04 provides a simple dual window comparator with adjustable trip points as shown in Figure 31. This circuit can be operated with either a dual or a single supply. For the A input channel, DAC B sets the low trip point and DAC A sets the upper trip point. The CMP-04 has open-collector outputs that are connected together in "Wired-OR" configuration to generate an out-of-range signal. For example, when VINA goes below the trip point set by DAC B, comparator C2 pulls the output down, turning the red LED on. The output can also be used as a logic signal for further processing.

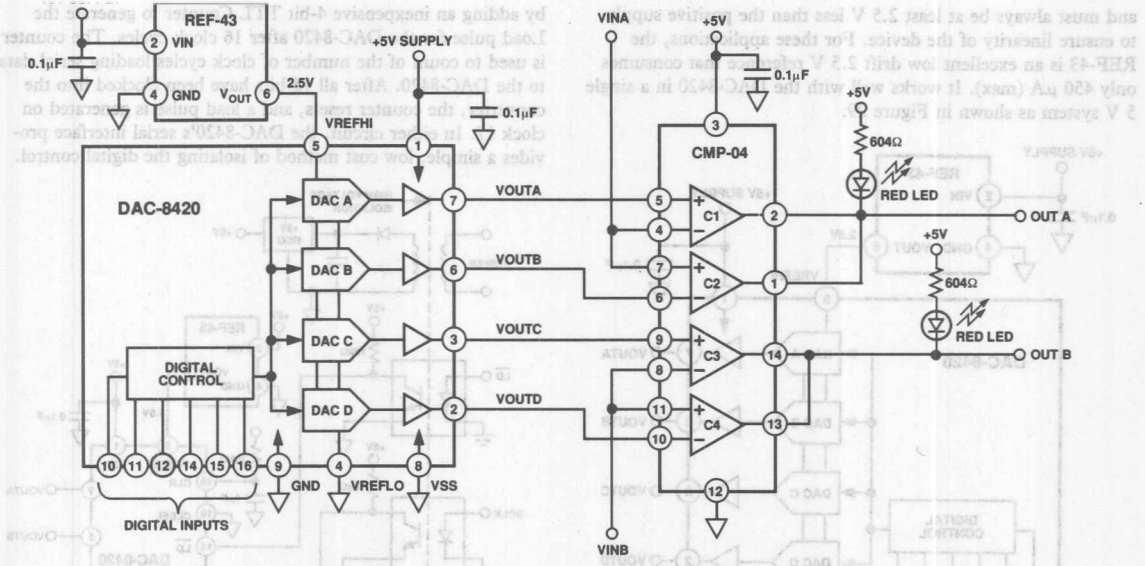


Figure 31. Dual Programmable Window Comparator

MC68HC11 Microcontroller Interfacing

Figure 32 shows a serial interface between the DAC-8420 and the MC68HC11 8-bit microcontroller. The SCK output of the 68HC11 drives the CLK input of the DAC, and the MOSI port outputs the serial data to load into the SDI input of the DAC. The port lines PD5, PC0, PC1, and PC2 provide the controls to the DAC as shown.

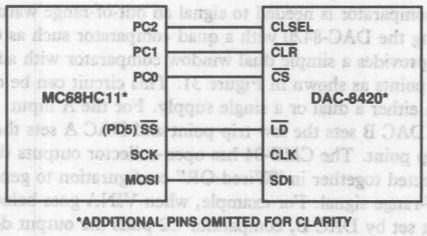
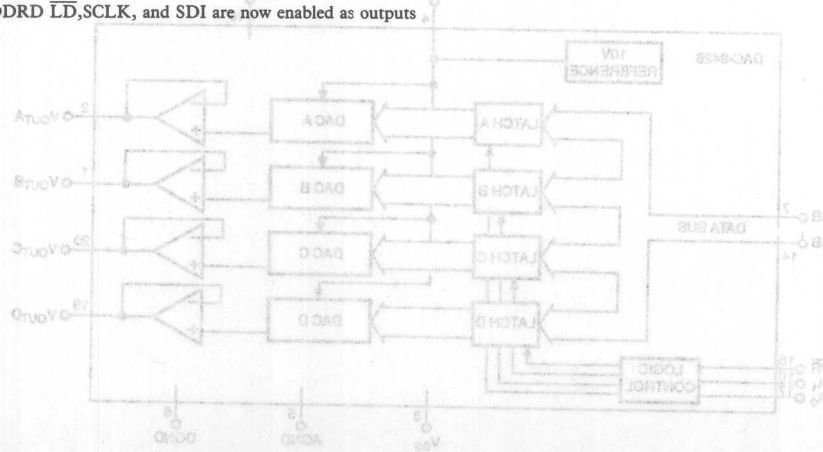


Figure 32. MC68HC11 Microcontroller Interface

For correct operation, the 68HC11 should be configured such that its CPOL bit and CPHA bit are both set to 1. In this configuration, serial data on MOSI of the 68HC11 is valid on the rising edge of the clock, which is the required timing for the DAC-8420. Data is transmitted in 8-bit bytes (MSB first), with only eight rising clock edges occurring in the transmit cycle. To load data to the DAC-8420's input register, PC0 is taken low and held low during the entire loading cycle. The first 8 bits are shifted in address first, immediately followed by another 8 bits in the second least-significant byte to load the complete 16-bit word. At the end of the second byte load, PC0 is then taken high. To prevent an additional advancing of the internal shift register, SCK must already be asserted before PC0 is taken high. To transfer the contents of the input shift register to the DAC register, PD5 is then taken low, asserting the $\overline{LD}$ input of the DAC and completing the loading process. PD5 should return high before the next load cycle begins. The DAC-8420's $\overline{CLR}$ input, controlled by the output PC1, provides an asynchronous clear function.

DAC-8420 to M68HC11 Interface Assembly Program

```
* M68HC11 Register Definitions
PORTC EQU $1003 Port C control register
*       "0,0,0,0;0,CLSEL,CLR,CS"
DDRC EQU $1007 Port C data direction
PORTD EQU $1008 Port D data register
*       "0,0,LD,SCLK;SDI,0,0,0"
DDRD EQU $1009 Port D data direction
SPCR EQU $1028 SPI control register
*       "SPIE,SPE,DWOM,MSTR;CPOL,CPHA,SPR1,SPR0"
SPSR EQU $1029 SPI status register
*       "SPIF,WCOL,0,MODF;0,0,0,0"
SPDR EQU $102A SPI data register; Read-Buffer; Write-Shifter
*
* SDI RAM variables: SDI1 is encoded from 0 (Hex) to CF (Hex)
* To select:  DAC A – Set SDI1 to $0X
*         DAC B – Set SDI1 to $4X
*         DAC C – Set SDI1 to $8X
*         DAC D – Set SDI1 to $CX
*         SDI2 is encoded from 00 (Hex) to FF (Hex)
*         DAC requires two 8-bit loads – Address + 12 bits
SDI1 EQU $00 SDI packed byte 1 "A1,A0,0,0;MSB,DB10,DB9,DB8"
SDI2 EQU $01 SDI packed byte 2
"DB7,DB6,DB5,DB4;DB3,DB2,DB1,DB0"
* Main Program
ORG $C000 Start of user's RAM in EVB
INIT LDS #$CFFF Top of C page RAM
* Initialize Port C Outputs
    LDAA #$07 0,0,0,0;0,1,1,1
*       CLSEL-Hi, CLR-Hi, CS-Hi
*       To reset DAC to ZERO-SCALE, set CLSEL-Lo ($03)
*       To reset DAC to MID-SCALE, set CLSEL-Hi ($07)
    STAA PORTC Initialize Port C Outputs
    LDAA #$07 0,0,0,0;0,1,1,1
    STAA DDRC CLSEL, CLR, and CS are now enabled as outputs
* Initialize Port D Outputs
    LDAA #$30 0,0,1,1;0,0,0,0
*       LD-Hi,SCLK-Hi,SDI-Lo
    STAA PORTD Initialize Port D Outputs
    LDAA #$38 0,0,1,1;1,0,0,0
    STAA DDRD LD,SCLK, and SDI are now enabled as outputs
* Initialize SPI Interface
    LDAA #$5F
    STAA SPCR SPI is Master,CPHA=1,CPOL=1,Clk rate=E/32
* Call update subroutine
    BSR UPDATE Xfer 2 8-bit words to DAC-8420
    JMP $E000 Restart BUFFALO
* Subroutine UPDATE
UPDATE PSHX   Save registers X, Y, and A
    PSHY
    PSHA
* Enter Contents of SDI1 Data Register (DAC# and 4 MSBs)
    LDAA #$80 1,0,0,0;0,0,0,0
    STAA SDI1 SDI1 is set to 80 (Hex)
* Enter Contents of SDI2 Data Register
    LDAA #$00 0,0,0,0;0,0,0,0
    STAA SDI2 SDI2 is set to 00 (Hex)
    LDX #SDI1 Stack pointer at 1st byte to send via SDI
    LDY #$1000 Stack pointer at on-chip registers
* Clear DAC output to zero
    BCLR PORTC,Y $02 Assert CLR
    BSET PORTC,Y $02 Deassert CLR
* Get DAC ready for data input
    BCLR PORTC,Y $01 Assert CS
TFRLP LDAA 0,X   Get a byte to transfer via SPI
    STAA SPDR Write SDI data reg to start xfer
WAIT LDAA SPSR Loop to wait for SPIF
    BPL WAIT SPIF is the MSB of SPSR
*   (when SPIF is set, SPSR is negated)
    INX          Increment counter to next byte for xfer
    CPX #SDI2+1 Are we done yet ?
    BNE TFRLP If not, xfer the second byte
* Update DAC output with contents of DAC register
    BCLR PORTD,Y $20 Assert LD
    BSET PORTD,Y $20 Latch DAC register
    BSET PORTC,Y $01 De-assert CS
    PULA When done, restore registers X, Y & A
    PULY
    PULX
    RTS       ** Return to Main Program **
```



Quad 8-Bit Voltage Out CMOS DAC Complete with Internal 10V Reference

DAC8426

FEATURES

- **No Adjustments Required, Total Error ± 1LSB Max Over Temperature**
- **Four Voltage-Output DACs on a Single Chip**
- **Internal 10V bandgap Reference**
- **Operates from Single +15V Supply**
- **Fast 50ns Data Load Time, All Temperatures**
- **Pin-for-Pin Replacement for PM-7226 and AD7226, Eliminates External Reference**

APPLICATIONS

- **Process Controls**
- **Multi-Channel Microprocessor Controlled:**
  - **System Calibration**
  - **Op Amp Offset and Gain Adjust**
  - **Level and Threshold Setting**

GENERAL DESCRIPTION

The DAC-8426 is a complete quad voltage output D/A converter with internal reference. This product fits directly into any existing 7226 socket where the user currently has a 10V external reference. The external reference is no longer necessary. The internal reference of the DAC-8426 is laser-trimmed to ±0.4% offering a 25ppm/°C temperature coefficient and 5mA of external load driving capability.

The DAC-8426 contains four 8-bit voltage-output CMOS D/A converters on a single chip. A 10V output bandgap reference sets the output full-scale voltage. The circuit also includes four input latches and interface control logic.

One of the four latches, selected by the address inputs, is loaded from the 8-bit data bus input when the write strobe is active low. All digital inputs are TTL/CMOS (5V) compatible. The on-board amplifiers can drive up to 10mA from either a single or dual supply. The on-board reference that is always connected to the internal DACs has 5mA available to drive external devices.

Continued

ORDERING INFORMATION†

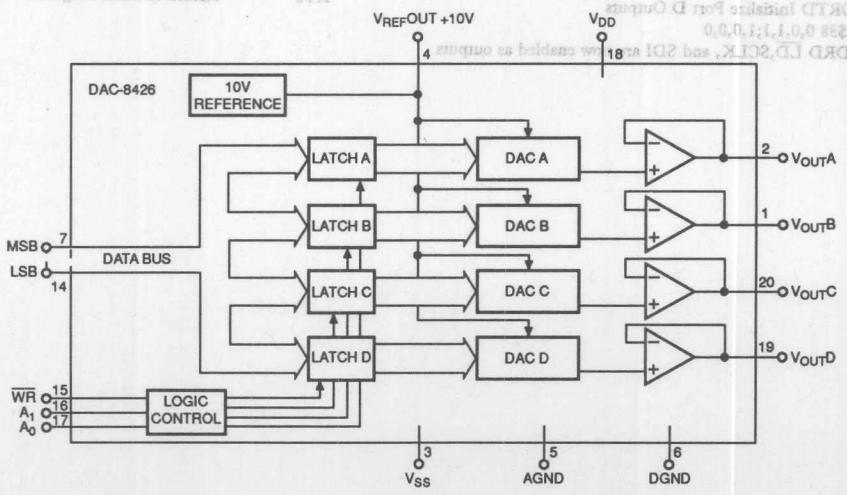
TOTAL UNADJUSTED ERROR (LSB)	MIL TEMP –55°C to +125°C	XIND TEMP –40°C to +85°C
±1	DAC8426AR	DAC8426ER
±1	–	DAC8426EP
±2	DAC8426BR	DAC8426FR
±2	–	DAC8426FP
±2	–	DAC8426FS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

SIMPLIFIED SCHEMATIC



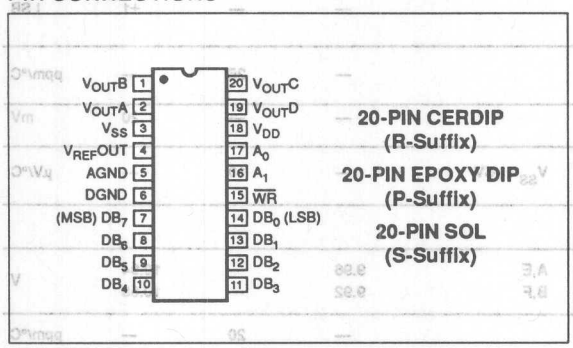
This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

GENERAL DESCRIPTION *Continued*

Its compact size, low power, and economical cost-per-channel, make the DAC-8426 attractive for applications requiring multiple D/A converters without sacrificing circuit-board space. System reliability is also increased due to reduced parts count.

PMI's advanced oxide-based, silicon-gate, CMOS process allows the DAC-8426's analog and digital circuitry to be manufactured on the same chip. This, coupled with PMI's highly stable thin-film R-2R resistor ladder, aids in matching and temperature tracking between DACs.

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND or DGND ..... –0.3V, +17V
V_{SS} to AGND or DGND ..... –7V, V_{DD}
V_{DD} to V_{SS} ..... –0.3V, +24V
AGND to DGND ..... –0.3V, +5V
Digital Input Voltage to DGND ..... –0.3V, V_{DD}
V_{REF}OUT to AGND (Note 1) ..... –0.3V, V_{DD}
V_{OUT} to AGND (Note 1) ..... V_{SS}, V_{DD}
Operating Temperature
Military AR/BR ..... –55°C to +125°C
Extended Industrial ER/EP/FR/FP/FS ..... –40°C to +85°C
Maximum Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

THERMAL RESISTANCE

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
20-Pin CerDIP (R)	70	7	°C/W
20-Pin Plastic DIP (P)	61	24	°C/W
20-Pin SOL (S)	80	22	°C/W

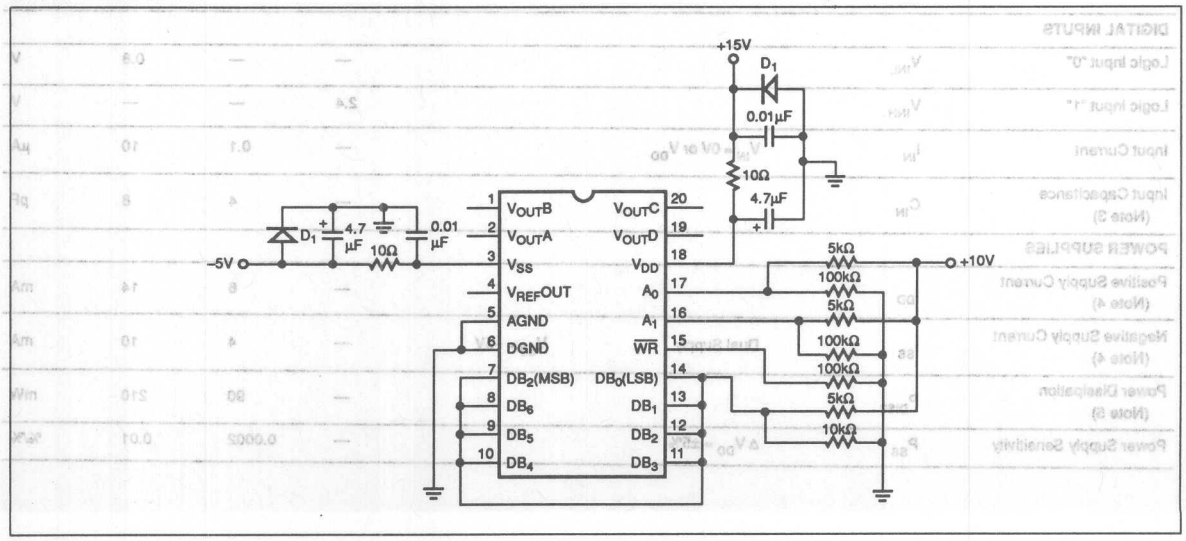
NOTES:

1. Outputs may be shorted to any terminal provided the package power dissipation is not exceeded. Typical output short-circuit current to AGND is 50mA.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than V_{SS} potential on any terminal.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets. Remove power before insertion or removal.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to device.

BURN-IN CIRCUIT

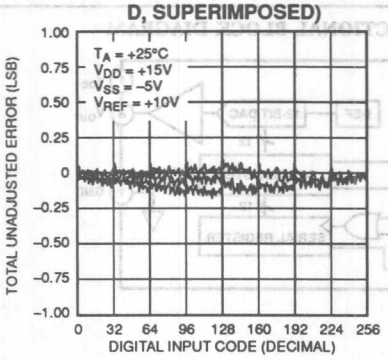


ELECTRICAL CHARACTERISTICS: V_{DD} = +15V ±10%, AGND = DGND = 0V, V_{SS} = 0V, T_A = –55°C to +125°C applies for DAC-8426AR/BR, T_A = –40°C to +85°C applies for DAC-8426ER/EP/FR/FP/FS, unless otherwise noted.

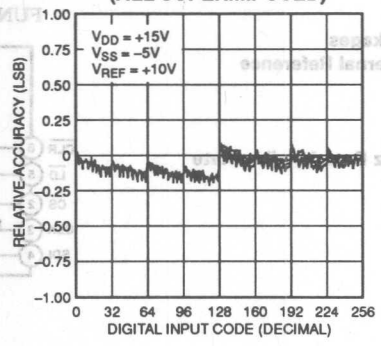
				DAC-8426			
PARAMETER	**SYMBOL**	**CONDITIONS**		**MIN**	**TYP[6]**	**MAX**	**UNITS**
STATIC PERFORMANCE							
Resolution	N			8	—	—	Bits
Total Unadjusted Error (Note 1)	TUE	Includes Reference	A,E	—	—	±1	LSB
			B,F	—	—	±2	
Relative Accuracy	INL		A,E	—	—	±1/2	LSB
			B,F	—	—	±1	
Differential Nonlinearity (Note 2)	DNL			—	—	±1	LSB
Full-Scale Temperature Coefficient	TCG_{FS}	Includes Reference		—	25	—	ppm/°C
Zero Scale Error	V_{ZSE}			—	—	20	mV
Zero Scale Error Temperature Coefficient	TCV_{ZS}	Dual Supply	V_{SS} = –5V	—	10	—	µV/°C
REFERENCE OUTPUT							
Output Voltage	$V_{REF}OUT$	No Load	A,E	9.96	—	10.04	V
			B,F	9.92	—	10.08	
Temperature Coefficient	$TCV_{REF}OUT$			—	20	—	ppm/°C
Load Regulation	LD_{REG}	ΔI_L = 5mA		—	0.02	0.1	%/mA
Line Regulation	LN_{REG}	ΔV_{DD} ±10%		—	0.008	0.04	%/V
Output Noise (Note 3)	e_{NRMS}	f = 0.1 to 10Hz		—	3	10	μV_{p-p}
Output Current	$I_{REF}OUT$	$\Delta V_{REF}OUT$ < 40mV		5	7	—	mA
DIGITAL INPUTS							
Logic Input "0"	V_{INL}			—	—	0.8	V
Logic Input "1"	V_{INH}			2.4	—	—	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}		—	0.1	10	µA
Input Capacitance (Note 3)	C_{IN}			—	4	8	pF
POWER SUPPLIES							
Positive Supply Current (Note 4)	I_{DD}			—	6	14	mA
Negative Supply Current (Note 4)	I_{SS}	Dual Supply	V_{SS} = –5V	—	4	10	mA
Power Dissipation (Note 5)	P_{DISS}			—	90	210	mW
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = ±5%		—	0.0002	0.01	%/%

TYPICAL PERFORMANCE CHARACTERISTICS

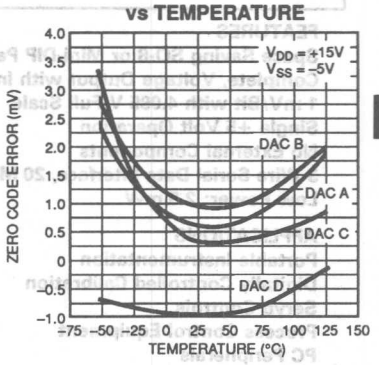
CHANNEL-TO-CHANNEL MATCHING (DACs A, B, C, D, SUPERIMPOSED)



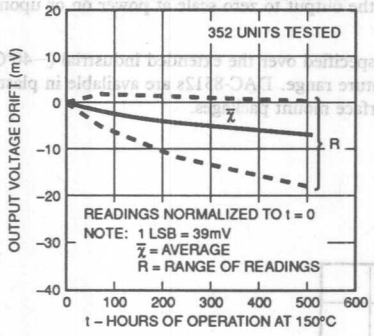
RELATIVE ACCURACY vs CODE AT T_A = –55°C, +25°C, +125°C (ALL SUPERIMPOSED)



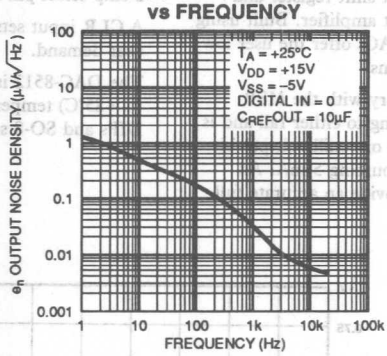
ZERO CODE ERROR vs TEMPERATURE



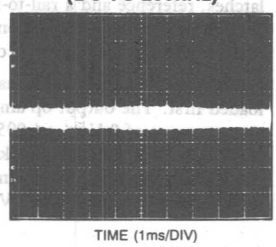
LONG TERM DRIFT ACCELERATED BY BURN-IN



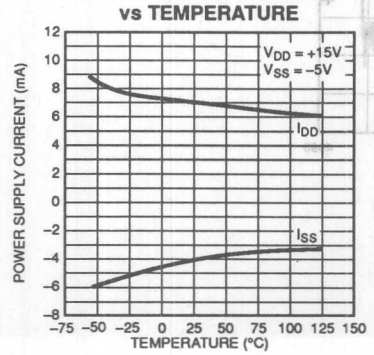
V_{OUT} NOISE DENSITY vs FREQUENCY



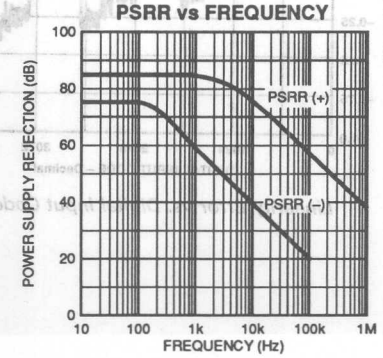
BROADBAND NOISE (DC TO 200kHz)



POWER SUPPLY CURRENT vs TEMPERATURE



PSRR vs FREQUENCY



$$PSRR(+) = -20\ LOG\left(\frac{V_{OUT}\ (0)}{\Delta V_{DD}}\right),$$
V_{DD} = +15V ±1V_p, V_{SS} = 0V

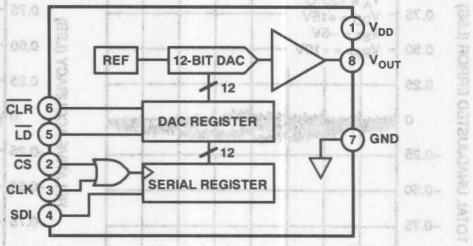
$$PSRR(-) = -20\ LOG\left(\frac{V_{OUT}\ (0)}{\Delta V_{SS}}\right),$$
V_{DD} = +15V , V_{SS} = –4V ±1V_p

DAC8512

FEATURES
Space Saving SO-8 or Mini-DIP Packages
Complete, Voltage Output with Internal Reference
1 mV/Bit with 4.095 V Full Scale
Single +5 Volt Operation
No External Components
3-Wire Serial Data Interface, 20 MHz Data Loading Rate
Low Power: 2.5 mW

APPLICATIONS
Portable Instrumentation
Digitally Controlled Calibration
Servo Controls
Process Control Equipment
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

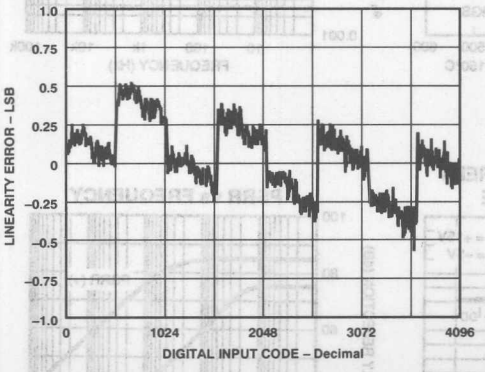
The DAC-8512 is a complete serial input, 12-bit, voltage output digital-to-analog converter designed to operate from a single +5 V supply. It contains the DAC, input shift register and latches, reference and a rail-to-rail output amplifier. Built using a CBCMOS process, these monolithic DACs offer the user low cost, and ease of use in +5 V only systems.

Coding for the DAC-8512 is natural binary with the MSB loaded first. The output op amp can swing to either rail and is set to a range of 0 V to +4.095 V—for a one-millivolt-per-bit resolution. It is capable of sinking and sourcing 5 mA. An on-chip reference is laser trimmed to provide an accurate full-scale output voltage of 4.095 V.

Serial interface is high speed, three-wire, DSP compatible with data in (SDI), clock (CLK) and load strobe (LD). There is also a chip-select pin for connecting multiple DACs.

A CLR input sets the output to zero scale at power on or upon user demand.

The DAC-8512 is specified over the extended industrial (−40°C to +85°C) temperature range. DAC-8512s are available in plastic DIPs and SO-8 surface mount packages.



Linearity Error vs. Digital Input Code

Parameter	Symbol	Condition		Min	Typ	Max	Units
STATIC PERFORMANCE							
Resolution	N	Note 2			12		Bits
Relative Accuracy	INL		E Grade		−1	±1/4	+1 LSB
			F Grade		−2	±3/4	+2 LSB
Differential Nonlinearity	DNL	No Missing Codes			−1	±3/4	+1 LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H				+1/2	+3 LSB
Full-Scale Voltage	V_{FS}	Data = FFF_H[3]	E Grade	4.087	4.095	4.103	V
			F Grade	4.079	4.095	4.111	V
Full-Scale Tempco	TCV_{FS}	Notes 3, 4				16	ppm/°C
ANALOG OUTPUT							
Output Current	I_{OUT}	Data = 800_H			±5	±7	mA
Load Regulation at Full Scale	L_{REG}	R_L = 402 Ω to ∞, Data = 800_H				1 3	LSB
Capacitive Load	C_L	No Oscillation[4]				500	pF
LOGIC INPUTS							
Logic Input Low Voltage	V_{IL}					0.8	V
Logic Input High Voltage	V_{IH}			2.4			V
Input Leakage Current	I_{IL}					10	µA
Input Capacitance	C_{IL}					10	pF
INTERFACE TIMING SPECIFICATIONS[1, 4]							
Clock Width High	t_{CH}			30	10		ns
Clock Width Low	t_{CL}			30	10		ns
Load Pulse Width	t_{LDW}			20			ns
Data Setup	t_{DS}			15	10		ns
Data Hold	t_{DH}			15	5		ns
Clear Pulse Width	t_{CLRW}			30	20		ns
Load Setup	t_{LD1}			15			ns
Load Hold	t_{LD2}			10			ns
Select	t_{CSS}			30			ns
Deselect	t_{CSH}			20			ns
AC CHARACTERISTICS[4]							
Voltage Output Settling Time	t_S	To ±1 LSB of Final Value[5]			16		µs
DAC Glitch					15		nV s
Digital Feedthrough					15		nV s
SUPPLY CHARACTERISTICS							
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V, No Load			1.5	2.5	mA
		V_{DD} = 5 V, V_{IL} = 0 V, No Load			0.5	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V, No Load			7.5	12.5	mW
		V_{DD} = 5 V, V_{IL} = 0 V, No Load			2.5	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%			0.002	0.004	%/%

NOTES

[1]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]1 LSB = 1 mV for 0 V to +4.095 V output range.

[3]Includes internal voltage reference error.

[4]These parameters are guaranteed by design and not subject to production testing.

[5]The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_{DD} = +5.0 V ± 5%, T_A = +25°C, applies to part number DAC8512GBC only, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Relative Accuracy	INL		−2	±3/4	+2	LSB
Differential Nonlinearity	DNL	No Missing Codes	−1	±0.7	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+1/2	+3	LSB
Full-Scale Voltage	V_{FS}	Data = FFF_H	4.085	4.095	4.105	V
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V, No Load		1.5	2.5	mA
		V_{DD} = 5 V, V_{IL} = 0 V, No Load		0.5	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V, No Load		7.5	12.5	mW
		V_{DD} = 5 V, V_{IL} = 0 V, No Load		2.5	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND . . . . . −0.3 V, +10 V
Logic Inputs to GND . . . . . −0.3 V, V_{DD} + 0.3 V
V_{OUT} to GND . . . . . −0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND . . . . . 50 mA
Package Power Dissipation . . . . . $(T_J \text{ max} - T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
8-Pin Plastic DIP Package (P) . . . . . 103°C/W
8-Lead SOIC Package (S) . . . . . 158°C/W
Maximum Junction Temperature (T_J max) . . . . . +150°C
Operating Temperature Range . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

Model	INL (LSB)	Temperature Range	Package Description	Package Option*
DAC8512EP	±1	−40°C to +85°C	8-Pin P-DIP	N-8
DAC8512FP	±2	−40°C to +85°C	8-Pin P-DIP	N-8
DAC8512FS	±2	−40°C to +85°C	8-Lead SOIC	SO-8
DAC8512GBC	±2	+25°C	Dice	

*For outline information see Package Information section.

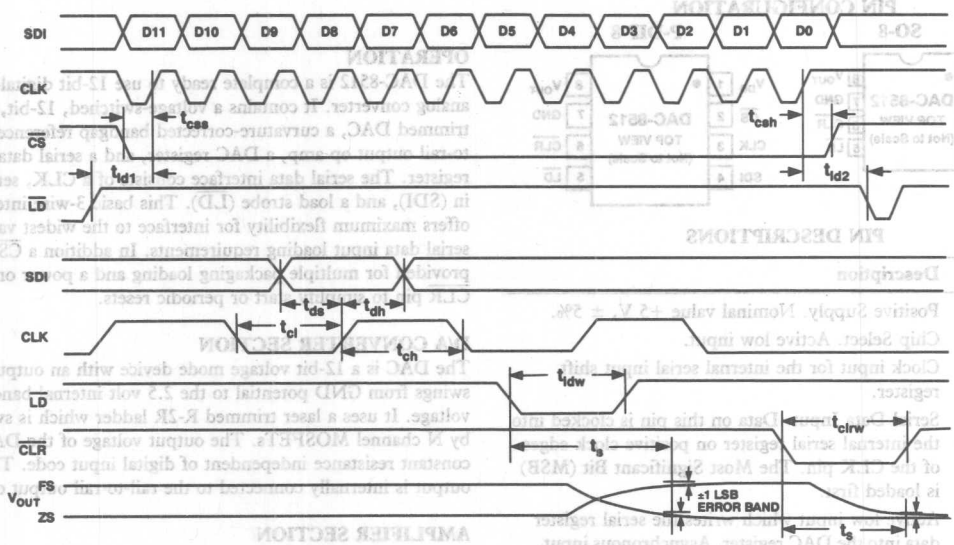


Figure 1. Timing Diagram

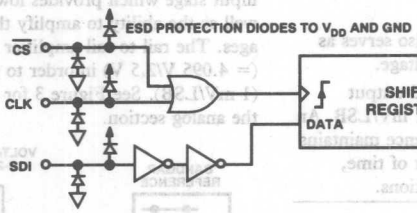
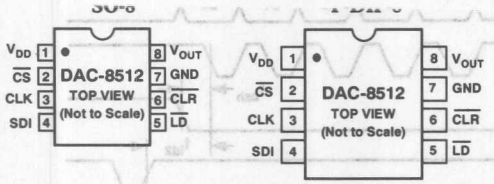


Figure 2. Equivalent Clock Input Logic

Table I. Control-Logic Truth Table

$\overline{CS}$[2]	CLK[2]	$\overline{CLR}$	$\overline{LD}$	Serial Shift Register Function	DAC Register Function
H	X	H	H	No Effect	Latched
L	L	H	H	No Effect	Latched
L	H	H	H	No Effect	Latched
L	↑+	H	H	Shift-Register-Data Advanced One Bit	Latched
↑+	L	H	H	Shift-Register-Data Advanced One Bit	Latched
H	X	H	↓−	No Effect	Updated with Current Shift Register Contents
H	X	H	L	No Effect	Transparent
H	X	L	X	No Effect	Loaded with All Zeros
H	X	↑+	H	No Effect	Latched All Zeros

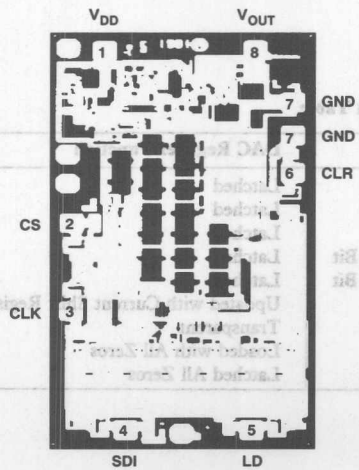
NOTES
[1]↑+ positive logic transition; ↓− negative logic transition; X = Don't Care.
[2]$\overline{CS}$ and CLK are interchangeable.
[3]Returning $\overline{CS}$ HIGH avoids an additional "false clock" of serial data input.
[4]Do not clock in serial data while $\overline{LD}$ is LOW.



PIN DESCRIPTIONS

Pin	Name	Description
1	V_{DD}	Positive Supply. Nominal value +5 V, ± 5%.
2	$\overline{CS}$	Chip Select. Active low input.
3	CLK	Clock input for the internal serial input shift register.
4	SDI	Serial Data Input. Data on this pin is clocked into the internal serial register on positive clock edges of the CLK pin. The Most Significant Bit (MSB) is loaded first.
5	$\overline{LD}$	Active low input which writes the serial register data into the DAC register. Asynchronous input.
6	$\overline{CLR}$	Active low digital input that clears the DAC register to zero, setting the DAC to minimum scale. Asynchronous input.
7	GND	Analog ground for the DAC. This also serves as the digital logic ground reference voltage.
8	V_{OUT}	Voltage output from the DAC. Fixed output voltage range of 0 V to 4.095 V with 1 mV/LSB. An internal temperature stabilized reference maintains a fixed full-scale voltage independent of time, temperature and power supply variations.

DICE CHARACTERISTICS



SUBSTRATE IS COMMON WITH V_{DD}.

NUMBER OF TRANSISTORS: 642
DIE SIZE: 0.055 inch × 0.106 inch; 5830 sq mils

OPERATION

The DAC-8512 is a complete ready to use 12-bit digital-to-analog converter. It contains a voltage-switched, 12-bit, laser-trimmed DAC, a curvature-corrected bandgap reference, a rail-to-rail output op amp, a DAC register, and a serial data input register. The serial data interface consists of a CLK, serial data in (SDI), and a load strobe ($\overline{LD}$). This basic 3-wire interface offers maximum flexibility for interface to the widest variety of serial data input loading requirements. In addition a $\overline{CS}$ select is provided for multiple packaging loading and a power on reset $\overline{CLR}$ pin to simplify start or periodic resets.

D/A CONVERTER SECTION

The DAC is a 12-bit voltage mode device with an output that swings from GND potential to the 2.5 volt internal bandgap voltage. It uses a laser trimmed R-2R ladder which is switched by N channel MOSFETs. The output voltage of the DAC has a constant resistance independent of digital input code. The DAC output is internally connected to the rail-to-rail output op amp.

AMPLIFIER SECTION

The DAC's output is buffered by a low power consumption precision amplifier. This amplifier contains a differential PNP pair input stage which provides low offset voltage and low noise, as well as the ability to amplify the zero-scale DAC output voltages. The rail-to-rail amplifier is configured in a gain of 1.6384 (= 4.095 V/2.5 V) in order to set the 4.095 volt full-scale output (1 mV/LSB). See Figure 3 for an equivalent circuit schematic of the analog section.

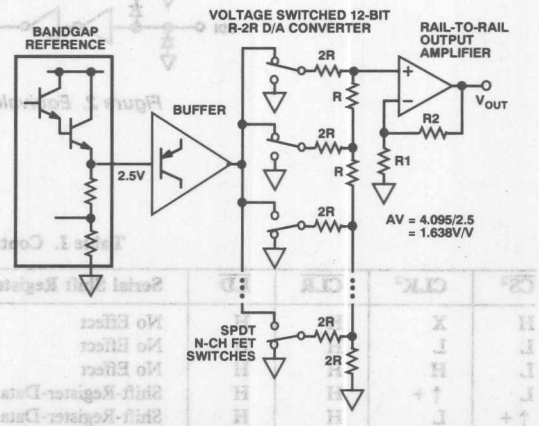


Figure 3. Equivalent DAC-8512 Schematic of Analog Portion

The op amp has a 16 μs typical settling time to 0.01%. There are slight differences in settling time for negative slewing signals vs. positive. See the oscilloscope photos in the typical performances section of this data sheet.

to provide precision performance while operating near either power supply.

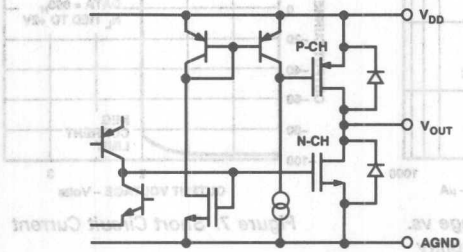


Figure 4. Equivalent Analog Output Circuit

Figure 4 shows an equivalent output schematic of the rail-to-rail amplifier with its N channel pull down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P channel pull up device that can supply GND terminated loads, especially at the low supply tolerance values of 4.75 volts. Figures 5 and 6 provide information on output swing performance near ground and full-scale as a function of load. In addition to resistive load driving capability the amplifier has also been carefully designed and characterized for up to 500 pF capacitive load driving capability.

POWER SUPPLY

The very low power consumption of the DAC-8512 is a direct result of a circuit design optimizing use of the CBCMOS process. By using the low power characteristics of the CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors good analog accuracy is achieved.

For power consumption sensitive applications it is important to note that the internal power consumption of the DAC-8512 is strongly dependent on the actual logic input voltage levels present on the SDI, $\overline{CS}$, $\overline{LD}$, and $\overline{CLR}$ pins. Since these inputs are standard CMOS logic structures they contribute static power dissipation dependent on the actual driving logic V_{OH} and V_{OL} voltage levels. The graph in Figure 9 shows the effect on total DAC-8512 supply current as a function of the actual value of input logic voltage. Consequently use of CMOS logic vs. TTL minimizes power dissipation in the static state. A V_{IL} = 0 V on the SDI, $\overline{CS}$ and CLR pins provides the lowest standby power dissipation of 2.5 mW (500 μA × 5 V).

8512 power supply be bypassed on the same PC card that contains the chip. Figure 10 shows the power supply rejection versus frequency performance. This should be taken into account when using higher frequency switched mode power supplies with ripple frequencies of 100 kHz and higher.

One advantage of the rail-to-rail output amplifier used in the DAC-8512 is the wide range of usable supply voltage. The part is fully specified and tested over temperature for operation from +4.75 V to +5.25 V. If reduced linearity and source current capability near full scale can be tolerated, operation of the DAC-8512 is possible down to +4.3 volts. The minimum operating supply voltage versus load current plot, in Figure 11, provides information for operation below V_{DD} = +4.75 V.

TIMING AND CONTROL

The DAC-8512 has a separate serial input register from the 12-bit DAC register that allows preloading of a new data value into the serial register without disturbing the present DAC output voltage. After the new value is fully loaded in the serial input register it can be asynchronously transferred to the DAC register by strobing the $\overline{LD}$ pin. The DAC register uses a level sensitive $\overline{LD}$ strobe that should be returned high before any new data is loaded into the serial input register. At any time the contents of the DAC register can be reset to zero by strobing the $\overline{CLR}$ pin which causes the DAC output voltage to go to zero volts. All of the timing requirements are detailed in Figure 1 along with the Table I Control-Logic Truth Table.

DAC8512—Typical Performance Characteristics

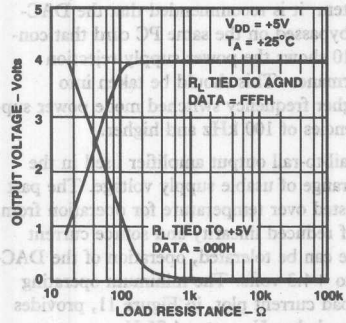


Figure 5. Output Swing vs. Load

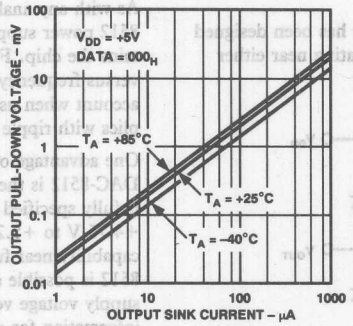


Figure 6. Pull-Down Voltage vs. Output Sink Current Capability

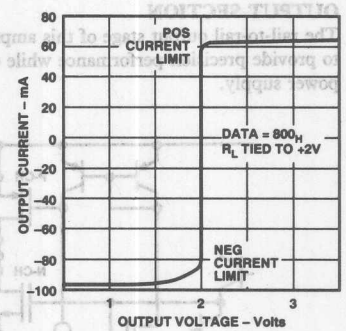


Figure 7. Short Circuit Current

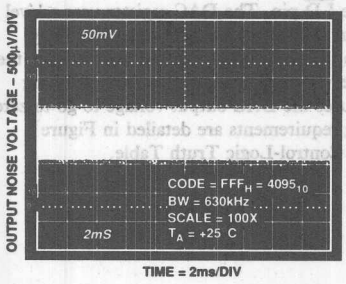


Figure 8. Broadband Noise

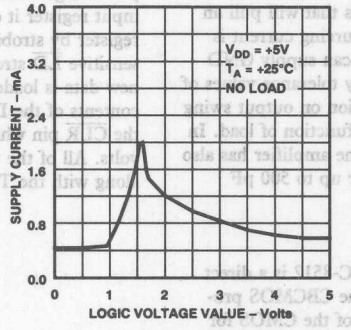


Figure 9. Supply Current vs. Logic Input Voltage

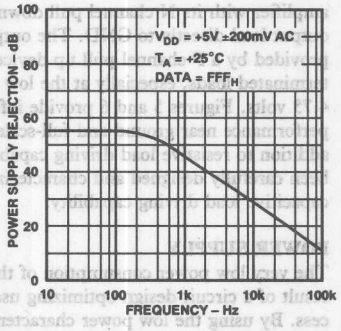


Figure 10. Power Supply Rejection vs. Frequency

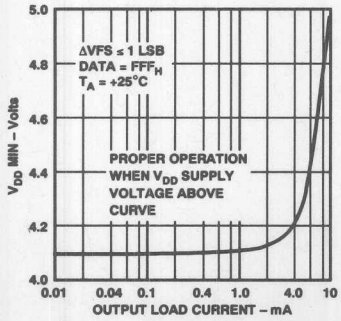


Figure 11. Minimum Supply Voltage vs. Load

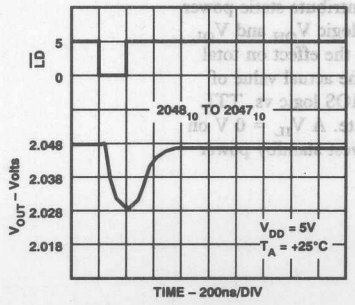


Figure 12. Midscale DAC Glitch Performance

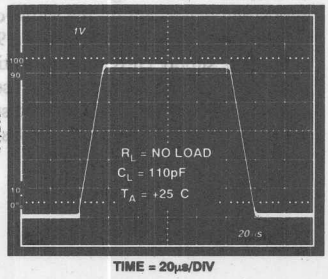


Figure 13. Large Signal Settling Time

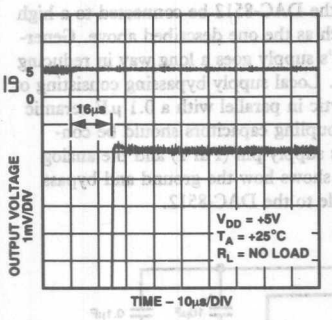


Figure 14. Rise Time Detail

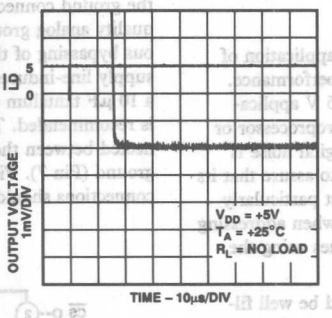


Figure 15. Fall Time Detail

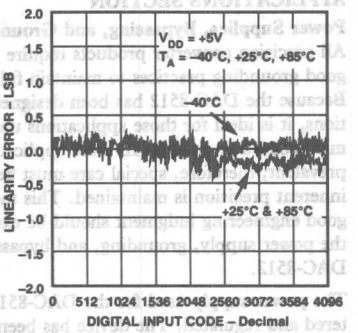


Figure 16. Linearity Error vs. Digital Code

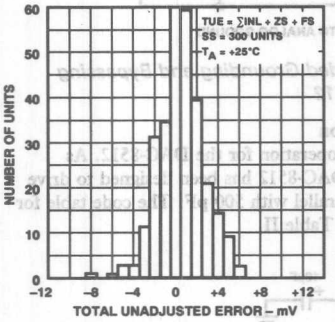


Figure 17. Total Unadjusted Error Histogram

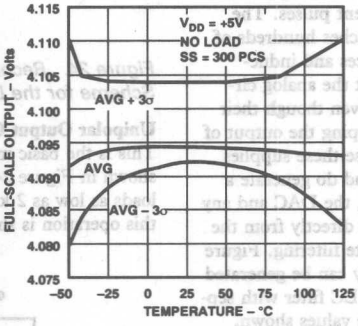


Figure 18. Full-Scale Voltage vs. Temperature

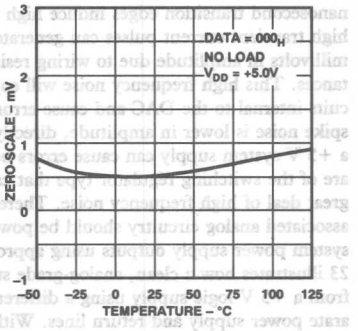


Figure 19. Zero-Scale Voltage vs. Temperature

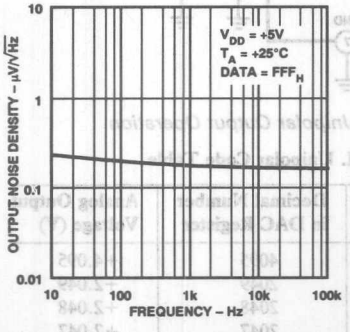


Figure 20. Output Voltage Noise vs. Frequency

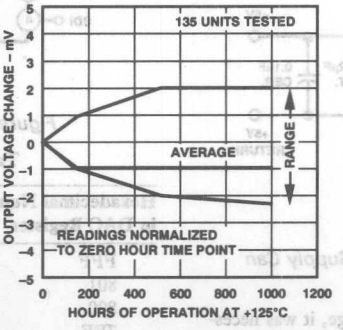


Figure 21. Long Term Drift Accelerated by Burn-In

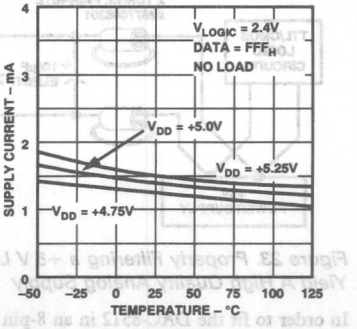


Figure 22. Supply Current vs. Temperature

Power Supplies, Bypassing, and Grounding

All precision converter products require careful application of good grounding practices to maintain full rated performance. Because the DAC-8512 has been designed for +5 V applications, it is ideal for those applications under microprocessor or microcomputer control. In these applications, digital noise is prevalent; therefore, special care must be taken to assure that its inherent precision is maintained. This means that particularly good engineering judgment should be exercised when addressing the power supply, grounding, and bypassing issues using the DAC-8512.

The power supply used for the DAC-8512 should be well filtered and regulated. The device has been completely characterized for a +5 V supply with a tolerance of ±5%. Since a +5 V logic supply is almost universally available, it is not recommended to connect the DAC directly to an unfiltered logic supply without careful filtering. Because it is convenient, a designer might be inclined to tap a logic circuit's supply for the DAC's supply. Unfortunately, this is not wise because fast logic with nanosecond transition edges induce high current pulses. The high transient current pulses can generate glitches hundreds of millivolts in amplitude due to wiring resistances and inductances. This high frequency noise will corrupt the analog circuits internal to the DAC and cause errors. Even though their spike noise is lower in amplitude, directly tapping the output of a +5 V system supply can cause errors because these supplies are of the switching regulator type that can and do generate a great deal of high frequency noise. Therefore, the DAC and any associated analog circuitry should be powered directly from the system power supply outputs using appropriate filtering. Figure 23 illustrates how a clean, analog-grade supply can be generated from a +5 V logic supply using a differential LC filter with separate power supply and return lines. With the values shown, this filter can easily handle 100 mA of load current without saturating the ferrite cores. Higher current capacity can be achieved with larger ferrite cores. For lowest noise, all electrolytic capacitors should be low ESR (Equivalent Series Resistance) type.

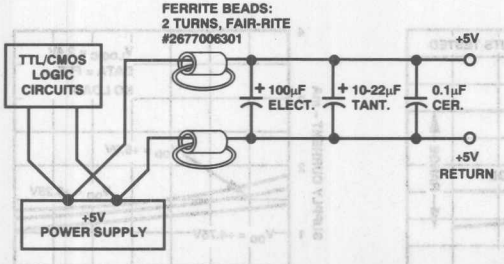


Figure 23. Properly Filtering a +5 V Logic Supply Can Yield A High Quality Analog Supply

In order to fit the DAC-8512 in an 8-pin package, it was necessary to use only one ground connection to the device. The ground connection of the DAC serves as the return path for supply currents as well as the reference point for the digital input thresholds. The ground connection also serves as the supply rail for the internal voltage reference and the output amplifier. Therefore, to minimize any errors, it is recommended that quality analog ground, such as the one described above. Generous bypassing of the DAC's supply goes a long way in reducing supply line-induced errors. Local supply bypassing consisting of a 10 µF tantalum electrolytic in parallel with a 0.1 µF ceramic is recommended. The decoupling capacitors should be connected between the DAC's supply pin (Pin 1) and the analog ground (Pin 7). Figure 24 shows how the ground and bypass connections should be made to the DAC-8512.

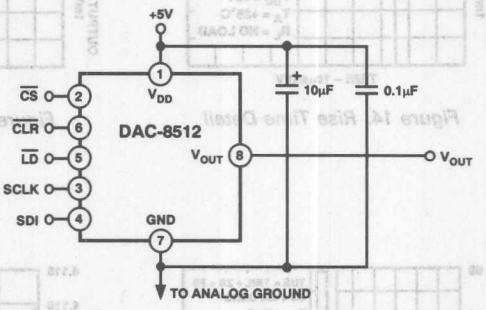


Figure 24. Recommended Grounding and Bypassing Scheme for the DAC-8512

Unipolar Output Operation

This is the basic mode of operation for the DAC-8512. As shown in Figure 24, the DAC-8512 has been designed to drive loads as low as 2 kΩ in parallel with 500 pF. The code table for this operation is shown in Table II.

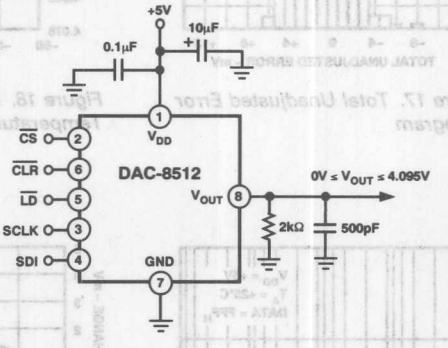


Figure 25. Unipolar Output Operation

Table II. Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	+4.095
801	2049	+2.049
800	2048	+2.048
7FF	2047	+2.047
000	0	0

gle, +5 V supply, a single +5 V supply may not be available in many applications. Since the DAC-8512 consumes no more than 2.5 mA, maximum, then an integrated voltage reference, such as the REF-02, can be used as the DAC-8512 +5 V supply. The configuration of the circuit is shown in Figure 26. Notice that the reference's output voltage requires no trimming because of the REF-02's excellent load regulation and tight initial output voltage tolerance. Although the maximum supply current of the DAC-8512 is 2.5 mA, local bypassing of the REF-02's output with at least 0.1 μF at the DAC's voltage supply pin is recommended to prevent the DAC's internal digital circuits from affecting the DAC's internal voltage reference.

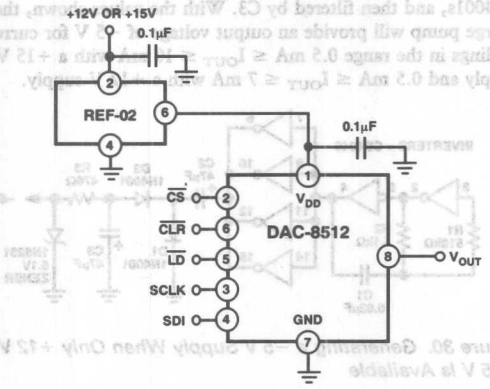


Figure 26. Operating the DAC-8512 on +12 V or +15 V Supplies Using a REF-02 Voltage Reference

Measuring Offset Error

One of the most commonly specified end-point errors associated with real world nonideal DACs is offset error.

In most DAC testing, the offset error is measured by applying the zero-scale code and measuring the output deviation from 0 volt. There are some DACs where offset errors may be present but not observable at the zero scale because of other circuit limitations (for example, zero coinciding with single-supply ground). In these DACs, nonzero output at zero code cannot be read as the offset error. In the DAC-8512, for example, the zero-scale error is specified to be ±3 LSBs. Since zero scale coincides with zero volt, it is not possible to measure negative offset error.

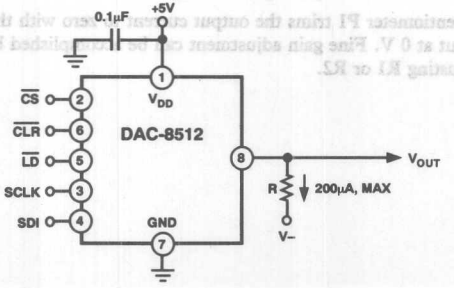


Figure 27. Measuring Zero-Scale or Offset Error

can now be read at zero code. This configuration forces the output p-channel MOSFET to source current to the negative supply thereby allowing the designer to determine in which direction the offset error appears. The value of the resistor should be such that, at zero code, current through the resistor is 200 μA, maximum.

Bipolar Output Operation

Although the DAC-8512 has been designed for single-supply operation, bipolar operation is achievable using the circuit illustrated in Figure 28. The circuit uses a single-supply, rail-to-rail OP-295 op amp and the REF-03 to generate the −2.5 V reference required to level-shift the DAC output voltage. Note that the −2.5 V reference was generated without the use of precision resistors. The circuit has been configured to provide an output voltage in the range $-5\ V \le V_{OUT} \le +5\ V$ and is coded in complementary offset binary. Although each DAC LSB corresponds to 1 mV, each output LSB has been scaled to 2.44 mV. Table III provides the relationship between the digital codes and output voltage.

The transfer function of the circuit is given by:

$$V_O = -1\ mV \times Digital\ Code \times \frac{R4}{R1} + 2.5 \times \frac{R4}{R2}$$

and, for the circuit values shown, becomes:

$$V_O = -2.44\ mV \times Digital\ Code + 5\ V$$

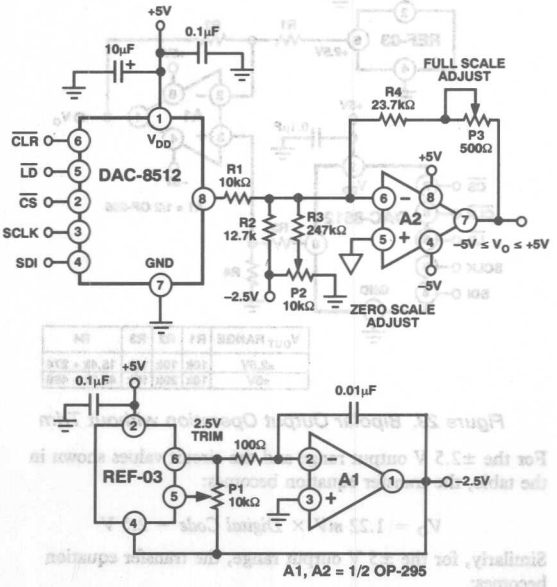


Figure 28. Bipolar Output Operation

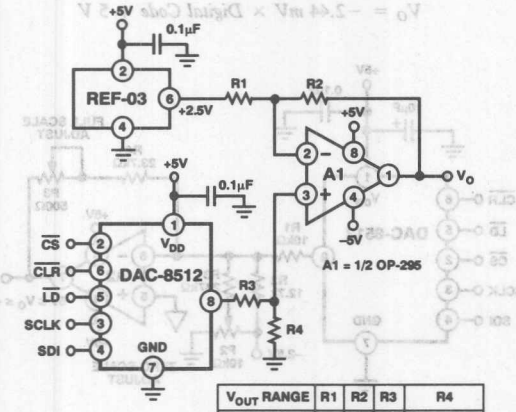
Table III. Bipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	−4.9976
801	2049	−2.44E−3
800	2048	0
7FF	2047	+2.44E−3
000	0	+5

To maintain monotonicity and accuracy, R1, R2, and R4 should be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R1 and R2 causes offset and gain errors while an R4 to R1 and R2 mismatch yields gain errors.

For applications that do not require high accuracy, the circuit illustrated in Figure 29 can also be used to generate a bipolar output voltage. In this circuit, only one op amp is used and no potentiometers are used for offset and gain trim. The output voltage is coded in offset binary and is given by:

$$V_O = 1\,mV \times Digital\ Code \times \left(\frac{R4}{R3 + R4}\right) \times \left(1 + \frac{R2}{R1}\right) - 2.5 \times \frac{R2}{R1}$$



V_{OUT} RANGE	R1	R2	R3	R4
±2.5V	10k	10k	10k	15.4k + 274
±5V	10k	20k	10k	43.2k + 499

Figure 29. Bipolar Output Operation without Trim

For the ±2.5 V output range and the circuit values shown in the table, the transfer equation becomes:

$$V_O = 1.22\,mV \times Digital\ Code - 2.5\,V$$

Similarly, for the ±5 V output range, the transfer equation becomes:

$$V_o = 2.44\,mV \times Digital\ Code - 5\,V$$

Generating a Negative Supply Voltage

Some applications may require bipolar output configuration but only have a single power supply rail available. This is very common in data acquisition systems using microprocessor-based systems. In these systems, +12 V, +15 V, and/or +5 V are only available. Shown in Figure 30 is a method of generating a negative supply voltage using one CD4049, a CMOS hex inverter, operating on +12 V or +15 V. The circuit is essentially a charge pump where two of the six are used as an oscillator. For the values shown, the frequency of oscillation is approximately 3.5 kHz and is fairly insensitive to supply voltage because R1 > 2 × R2. The remaining four inverters are wired in parallel for higher output current. The square wave output is level translated by C2 to a negative-going signal, rectified using a pair of 1N4001s, and then filtered by C3. With the values shown, the charge pump will provide an output voltage of −5 V for current loadings in the range 0.5 mA ≤ I_{OUT} ≤ 10 mA with a +15 V supply and 0.5 mA ≤ I_{OUT} ≤ 7 mA with a +12 V supply.

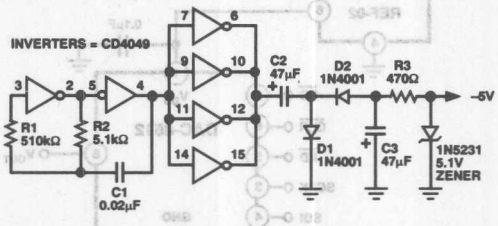


Figure 30. Generating a −5 V Supply When Only +12 V or +15 V Is Available

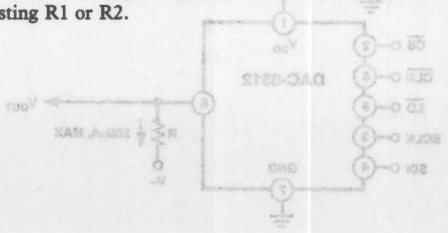
A High-Compliance, Digitally Controlled Precision Current Source

The circuit in Figure 31 shows the DAC-8512 controlling a high-compliance precision current source using an AMP-05 instrumentation amplifier. The AMP-05's reference pin becomes the input, and the "old" inputs now monitor the voltage across a precision current sense resistor, R_{CS}. Voltage gain is set to unity, so the transfer function is given by the following equation:

$$I_{OUT} = \frac{V_{IN}}{R_{CS}}$$

If R_{CS} equals 100 Ω, the output current is limited to +10 mA with a 1 V input. Therefore, each DAC LSB corresponds to 2.4 µA. If a bipolar output current is required, then the circuit in Figure 28 can be modified to drive the AMP-05's reference pin with a ±1 V input signal.

Potentiometer P1 trims the output current to zero with the input at 0 V. Fine gain adjustment can be accomplished by adjusting R1 or R2.



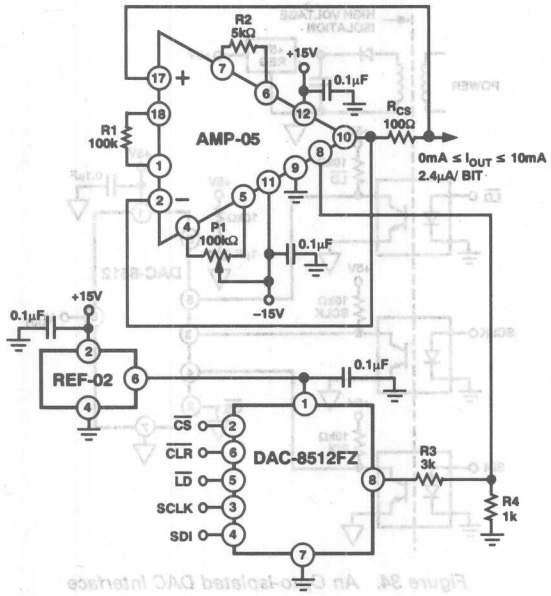


Figure 31. A High-Compliance, Digitally Controlled Precision Current Source

A Single-Supply, Programmable Current Source

The circuit in Figure 32 shows how the DAC-8512 can be used with an OP-295 single-supply, rail-to-rail output op amp to provide a digitally programmable current sink from V_{SOURCE} that consumes less than 3.8 mA, maximum. The DAC's output voltage is applied across R1 by placing the 2N2222 transistor in the OP-295's feedback loop. For the circuit values shown, the full-scale output current is 1 mA which is given by the following equation:

$$I_{OUT} = \frac{DW \times 4.095\ V}{R1}$$

where DW = DAC-8512's binary digital input code.

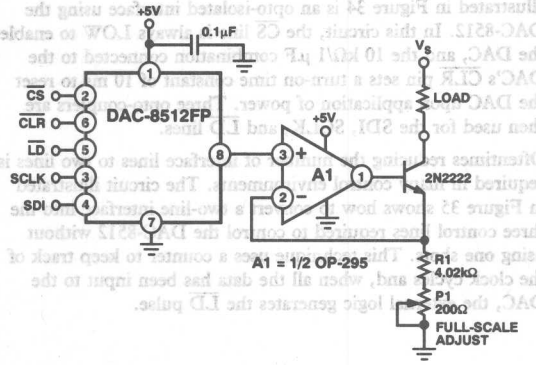


Figure 32. A Single-Supply, Programmable Current Source

The usable output voltage range of the current sink is +5 V to +60 V. The low limit of the range is controlled by transistor saturation, and the high limit is controlled by the collector-base breakdown voltage of the 2N2222.

A Digitally Programmable Window Detector

A digitally programmable, upper/lower limit detector using two DAC-8512s is shown in Figure 33. The required upper and lower limits for the test are loaded into each DAC individually by controlling HDAC/$\overline{LDAC}$. If a signal at the test input is not within the programmed limits, the output will indicate a logic zero which will turn the red LED on.

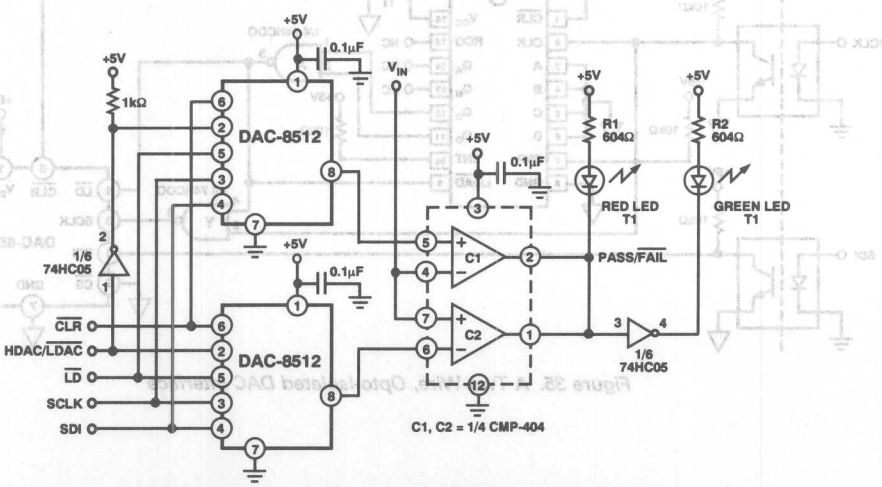


Figure 33. A Digitally Programmable Window Detector

Opto-Isolated Interfaces for Process Control Environments

In many process control type applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled. Opto-isolators can provide isolation in excess of 3 kV. The serial loading structure of the DAC-8512 makes it ideal for optoisolated interfaces as the number of interface lines is kept to a minimum.

Illustrated in Figure 34 is an opto-isolated interface using the DAC-8512. In this circuit, the $\overline{CS}$ line is always LOW to enable the DAC, and the 10 kΩ/1 µF combination connected to the DAC's $\overline{CLR}$ pin sets a turn-on time constant of 10 ms to reset the DAC upon application of power. Three opto-couplers are then used for the SDI, SCLK, and $\overline{LD}$ lines.

Oftentimes reducing the number of interface lines to two lines is required in many control environments. The circuit illustrated in Figure 35 shows how to convert a two-wire interface into the three control lines required to control the DAC-8512 without using one shots. This technique uses a counter to keep track of the clock cycles and, when all the data has been input to the DAC, the external logic generates the $\overline{LD}$ pulse.

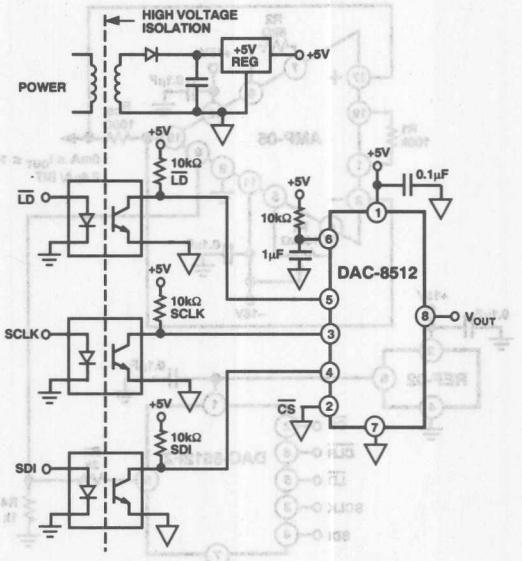


Figure 34. An Opto-Isolated DAC Interface

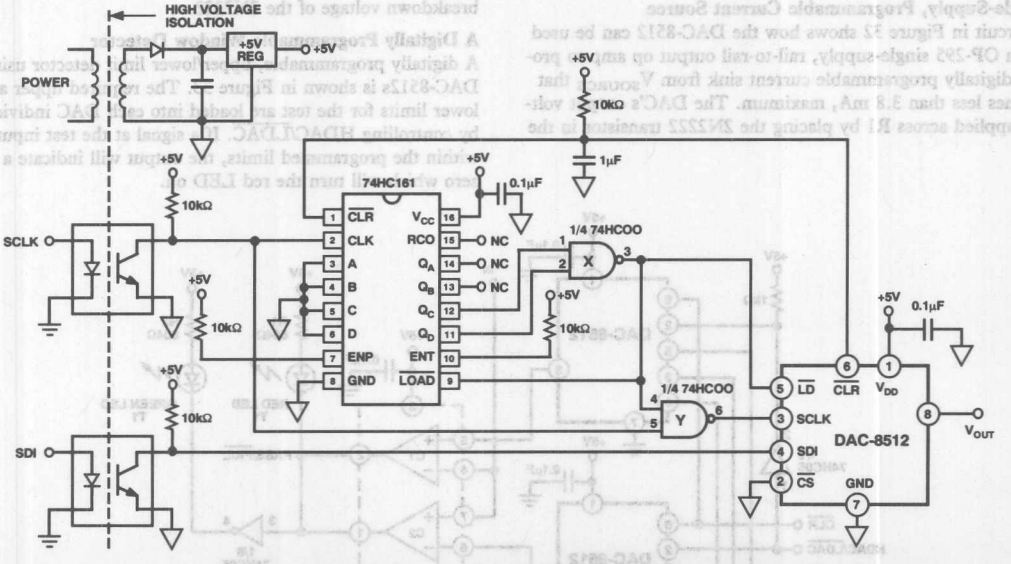


Figure 35. A Two-Wire, Opto-Isolated DAC Interface

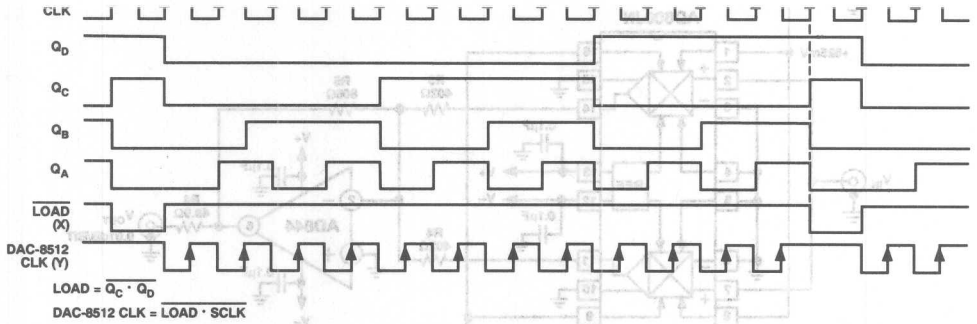


Figure 36. Opto-Isolated Two-Wire Serial Interface Timing Diagram

The timing diagram of Figure 36 can be used to understand the operation of the circuit. Only two opto-couplers are used in the circuit; one for SCLK and one for SDI. The 74HC161 counter in incremented on every rising edge of the clock. Additionally, the data is loaded into the DAC-8512 on the falling edge of the clock by inverting the serial clock using gate "Y." The timing diagram shows that after the twelfth bit has been clocked the output of the counter is binary 1011. On the very next rising clock edge, the output of the counter changes to binary 1100 upon which the output of gate "X" goes LOW to generate the $\overline{LD}$ pulse. The $\overline{LD}$ signal is connected to both the DAC's $\overline{LD}$ and the counter's LOAD pins to prevent the thirteenth rising clock edge from advancing the DAC's internal shift register. This prevents false loading of data into the DAC-8512. Inverting the DAC's serial clock allows sufficient time from the CLK edge to the $\overline{LD}$ edge, and from the $\overline{LD}$ edge to the next clock pulse all of which satisfies the timing requirements for loading the DAC-8512.

After loading one address of the DAC, the entire process can repeated to load another address. If the loading is complete, then the clock must stop after the thirteenth pulse of the final load. The DAC's clock input will be pulled high and the counter reset to zero. As was shown in Figure 35, both the 74HC161's and the DAC-8512's $\overline{CLR}$ pins are connected to a simple R-C timing circuit that resets both ICs when the power in turned on. The circuit's time constant should be set longer than the power supply turn-on time and, in this circuit, is set to 10 ms, which should be adequate for most systems. This same two-wire interface can be used for other three-wire serial input DACs.

Decoding Multiple DAC-8512s

The $\overline{CS}$ function of the DAC-8512 can be used in applications to decode a number of DACs. In this application, all DACs receive the same input data; however, only one of the DAC's $\overline{CS}$ input is asserted to transfer its serial input register contents into the destination DAC register. In this circuit, shown in Figure 37, the $\overline{CS}$ timing is generated by a 74HC139 decoder and should follow the DAC-8512's standard timing requirements. To prevent timing errors, the 74HC139 should not be activated by its ENABLE input while the coded address inputs are changing. A simple timing circuit, R1 and C1, connected to the DACs' $\overline{CLR}$ pins resets all DAC outputs to zero during power-up.

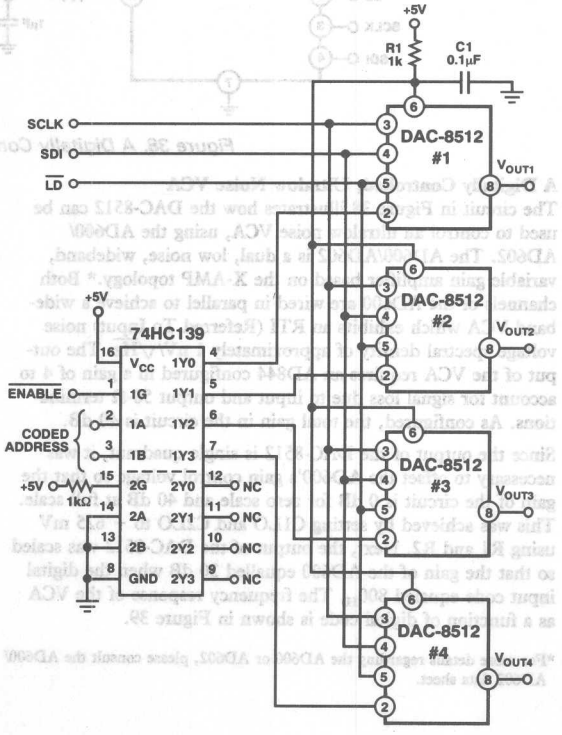


Figure 37. Decoding Multiple DAC-8512s Using the $\overline{CS}$ Pin

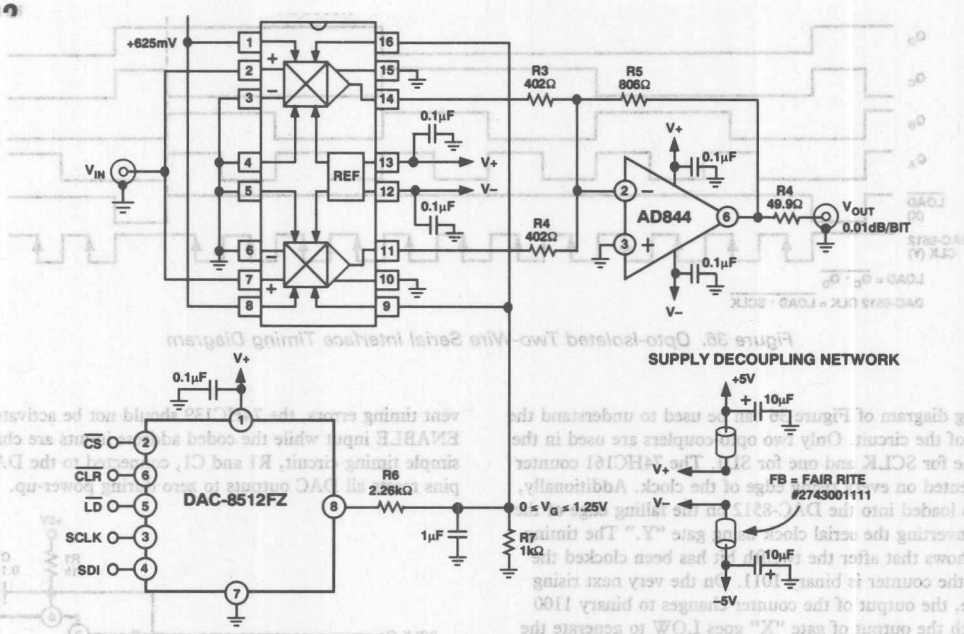


Figure 38. A Digitally Controlled, Ultralow Noise VCA

A Digitally Controlled, Ultralow Noise VCA

The circuit in Figure 38 illustrates how the DAC-8512 can be used to control an ultralow noise VCA, using the AD600/AD602. The AD600/AD602 is a dual, low noise, wideband, variable gain amplifier based on the X-AMP topology.* Both channels of the AD600 are wired in parallel to achieve a wideband VCA which exhibits an RTI (Referred To Input) noise voltage spectral density of approximately 1 nV/$\sqrt{Hz}$. The output of the VCA requires an AD844 configured in a gain of 4 to account for signal loss due to input and output 50-Ω terminations. As configured, the total gain in the circuit is 40 dB.

Since the output of the DAC-8512 is single quadrant, it was necessary to offset the AD600's gain control voltage so that the gain of the circuit is 0 dB for zero scale and 40 dB at full scale. This was achieved by setting C1LO and C2LO to + 625 mV using R1 and R2. Next, the output of the DAC-8512 was scaled so that the gain of the AD600 equalled 20 dB when the digital input code equaled 800_H. The frequency response of the VCA as a function of digital code is shown in Figure 39.

*For more details regarding the AD600 or AD602, please consult the AD600/AD602 data sheet.

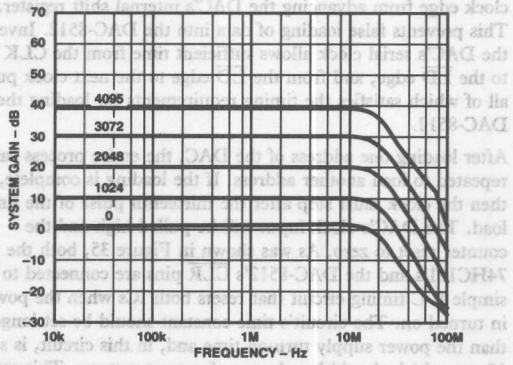


Figure 39. VCA Frequency Response vs. Digital Code

A Serial DAC, Audio Volume Control

The DAC-8512 is well suited to control digitally the gain or attenuation of a voltage controlled amplifier. In professional audio mixing consoles, music synthesizers, and other audio processors, VCAs, such as the SSM-2018, adjust audio channel gain and attenuation from front panel potentiometers. The VCA provides a clean gain transition control of the audio level when the slew rate of the analog input control voltage, V_C, is properly chosen. The circuit in Figure 40 illustrates a volume control application using the DAC-8512 to control the attenuation of the SSM-2018.

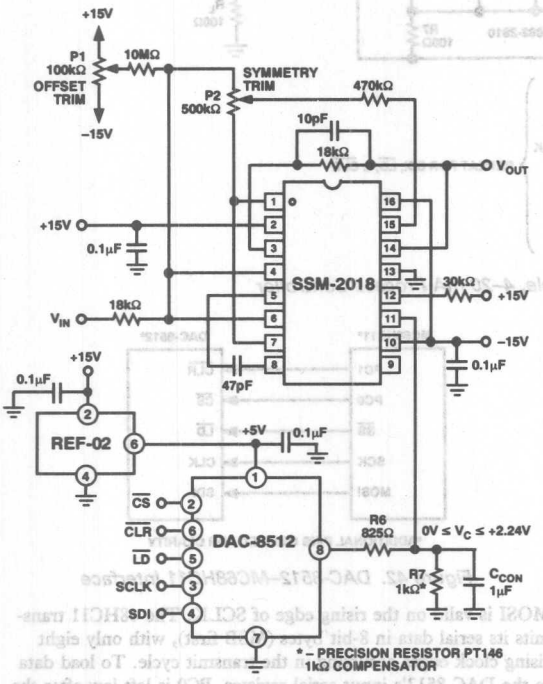


Figure 40. A Serial DAC, Audio Volume Control

Since the supply voltage available in these systems is typically ±15 V or ±18 V, a REF-02 is used to supply the +5 V required to power the DAC. No trimming of the reference is required because of the reference's tight initial tolerance and low supply current consumption of the DAC-8512. The SSM-2018 is configured as a unity-gain buffer when its control voltage equals 0 volt. This corresponds to a 000_H code from the DAC-8512. Since the SSM-2018 exhibits a gain constant of −28 mV/dB (typical), the DAC's full-scale output voltage has to be scaled down by R6 and R7 to provide 80 dB of attenuation when the digital code equals FFF_H. Therefore, every DAC LSB corresponds to 0.02 dB of attenuation. Table IV illustrates the attenuation vs. digital code of the volume control circuit.

Table IV. SSM-2018 VCA Attenuation vs. DAC-8512 Input Code

Hexadecimal Number in DAC Register	Control Voltage (V)	VCA Attenuation (dB)
000	0	0
400	+0.56	20
800	+1.12	40
C00	+1.68	60
FFF	+2.24	80

To compensate for the SSM-2018's gain constant temperature coefficient of −3300 ppm/°C, a 1 kΩ, temperature-sensitive resistor (R7) manufactured by the Precision Resistor Company with a temperature coefficient of +3500 ppm/°C is used. A C_{CON} of 1 μF provides a control transition time of 1 ms which yields a click-free change in the audio channel attenuation. Symmetry and offset trimming details of the VCA can be found in the SSM-2018 data sheet.

Information regarding the PT146 1 kΩ "Compensator" can be obtained by contacting:

Precision Resistor Company, Incorporated
10601 75th Street North
Largo, Fl 34647
(813) 541-5771

An Isolated, Programmable, 4–20 mA Process Controller

In many process control system, applications, two-wire current transmitters are used to transmit analog signals through noisy environments. These current transmitters use a "zero-scale" signal current of 4 mA that can be used to power the transmitter's signal conditioning circuitry. The "full-scale" output signal in these transmitters is 20 mA. The converse approach to process control can also be used; a low-power, programmable current source can be used to control remotely located sensors or devices in the loop.

A circuit that performs this function is illustrated in Figure 41. Using the DAC-8512 as the controller, the circuit provides a programmable output current of 4 mA to 20 mA, proportional to the DAC's digital code. Biasing for the controller is provided by the REF-02 and requires no external trim for two reasons:

(1) the REF-02's tight initial output voltage tolerance and (2) the low supply current consumption of both the OP-90 and the DAC-8512. The entire circuit, including opto-couplers, consumes less than 3 mA from the total budget of 4 mA. The OP-90 regulates the output current to satisfy the current summation at the noninverting node of the OP-90. The KCL equation at Pin 3 is given by:

$$I_{OUT} = \frac{1}{R7} \times \left(\frac{1\,mV \times Digital\ Code \times R3}{R1} + \frac{V_{REF} \times R3}{R2} \right)$$

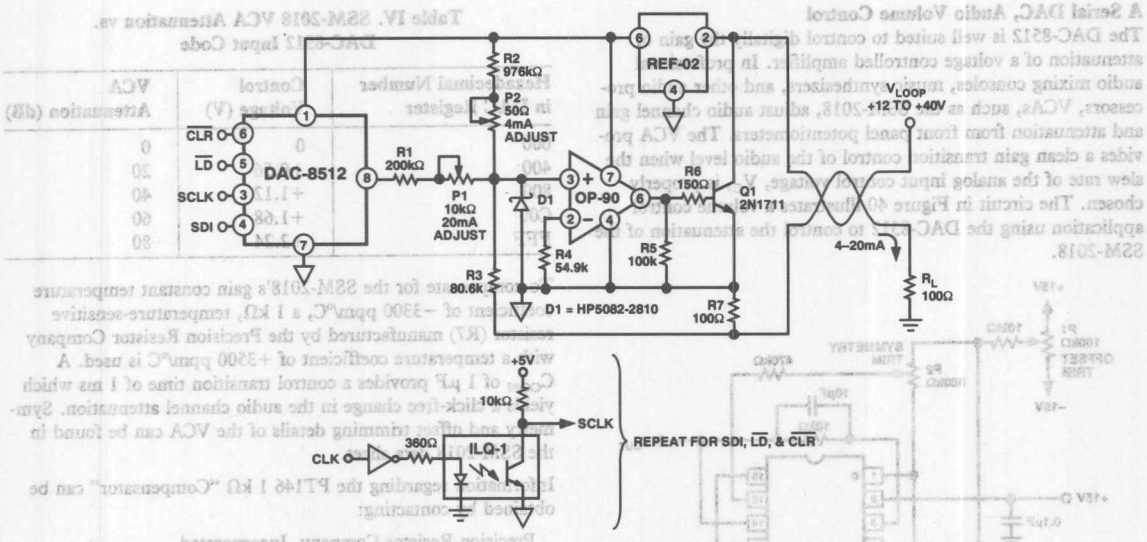


Figure 41. An Isolated, Programmable, 4–20 mA Process Controller

For the values shown in Figure 41,

$$I_{OUT} = 3.9\ \mu A \times Digital\ Code + 4\ mA$$

giving a full-scale output current of 20 mA when the DAC-8512's digital code equals FFF_H. Offset trim at 4 mA is provided by P2, and P1 provides the circuit's gain trim at 20 mA. These two trims do not interact because the noninverting input of the OP-90 is at virtual ground. The Schottky diode, D1, is required in this circuit to prevent loop supply power-on transients from pulling the noninverting input of the OP-90 more than 300 mV below its inverting input. Without this diode, such transients could cause phase reversal of the OP-90 and possible latchup of the controller. The loop supply voltage compliance of the circuit is limited by the maximum applied input voltage to the REF-02 and is from +12 V to +40 V.

MICROPROCESSOR INTERFACING

DAC-8512–MC68HC11 Interface

The circuit illustrated in Figure 42 shows a serial interface between the DAC-8512 and the MC68HC11 8-bit microcontroller. SCK of the 68HC11 drives SCLK of the DAC-8512, while the MOSI output drives the serial data line, SDI, of the DAC-8512. The DAC's $\overline{CLR}$, $\overline{LD}$, and $\overline{CS}$ signals are derived from port lines PC1, PD5, and PC0, respectively, as shown.

For correct operation of the serial interface, the 68HC11 should be configured such that its CPOL bit is set to 1 and its CPHA bit is also set to 1. When the serial data is to be transmitted to the DAC, PC0 is taken low, asserting the DAC's $\overline{CS}$ input. When the 68HC11 is configured in this manner, serial data on

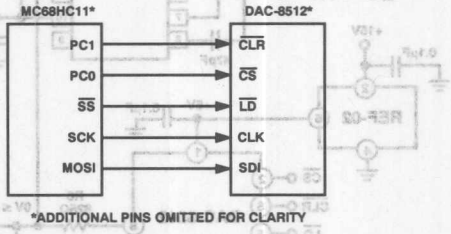


Figure 42. DAC-8512–MC68HC11 Interface

MOSI is valid on the rising edge of SCLK. The 68HC11 transmits its serial data in 8-bit bytes (MSB first), with only eight rising clock edges occurring in the transmit cycle. To load data to the DAC-8512's input serial register, PC0 is left low after the first eight bits are transferred, and a second byte of data is then transferred serially to the DAC-8512. During the second byte load, the first four most significant bits of the first byte are pushed out of the DAC's input shift register. At the end of the second byte load, PC0 is then taken high. To prevent an accidental advancing of the internal shift register, SCLK must already be asserted before PC0 is taken high. To transfer the contents of the input shift register to the DAC register, PD5 is taken low, asserting the DAC's $\overline{LD}$ input. The DAC's $\overline{CLR}$ input, controlled by the 68HC11's PC1 port, provides an asynchronous clear function, setting the DAC output to zero. Included in this section is the source code for operating the DAC-8512—M68HC11 interface.

DAC-8512–M68HC11 Interface Program Source Code

```
*
PORTC   EQU   $1003     Port C control register                    *
*                       "0,0,0,0;0,0,CLR/,CS/"
DDRC    EQU   $1007     Port C data direction
PORTD   EQU   $1008     Port D data register                       *
*                       "0,0,LD/,SCLK;SDI,0,0,0
DDRD    EQU   $1009     Port D data direction
SPCR    EQU   $1028     SPI control register
*                       "SPIE,SPE,DWOM,MSTR;CPOL,CPHA,SPR1,SPR0"  *
SPSR    EQU   $1029     SPI status register                        *
*                       "SPIF,WCOL,0,MODF;0,0,0,0"
SPDR    EQU   $102A     SPI data register; Read-Buffer; Write-Shifter
*
* SDI RAM variables:    SDI1 is encoded from 0 (Hex) to F (Hex)    *
*                       SDI2 is encoded from 00 (Hex) to FF (Hex)
*                       DAC requires two 8-bit loads; upper 4 bits of SDI1
*                       are ignored.
*
SDI1    EQU   $00       SDI packed byte 1 "0,0,0,0;MSB,DB10,DB9,DB8"
SDI2    EQU   $01       SDI packed byte 2 "DB7,DB6,DB5,DB4;DB3,DB2,DB1,DB0"
*
        ORG   $C000     Start of user's RAM in EVB
INIT    LDS   #$CFFF    Top of C page RAM
*
        LDAA  #$03      0,0,0,0;0,0,1,1
*                       CLR/-Hi, CS/-Hi
        STAA  PORTC     Initialize Port C Outputs
        LDAA  #$03      0,0,0,0;0,0,1,1
        STAA  DDRC      CLR/ and CS/ are now enabled as outputs
*
        LDAA  #$30      0,0,1,1;0,0,0,0
*                       LD/-Hi,SCLK-Hi,SDI-Lo
        STAA  PORTD     Initialize Port D Outputs
        LDAA  #$38      0,0,1,1;1,0,0,0
        STAA  DDRD      LD/,SCLK, and SDI are now enabled as outputs
*
        LDAA  #$5F
        STAA  SPCR      SPI is Master,CPHA=1,CPOL=1,Clk rate=E/32
*
        BSR   UPDATE    Xfer 2 8-bit words to DAC-8512
        JMP   $E000     Restart BUFFALO
*
UPDATE  PSHX            Save registers X, Y, and A
        PSHY
        PSHA
*
        LDAA  #$0A      0,0,0,0;1,0,1,0
        STAA  SDI1      SDI1 is set to 0A (Hex)
*
        LDAA  #$AA      1,0,1,0;1,0,1,0
        STAA  SDI2      SDI2 is set to AA (Hex)
*
        LDX   #SDI1     Stack pointer at 1st byte to send via SDI
        LDY   #$1000    Stack pointer at on-chip registers
*
        BCLR  PORTC,Y   $02  Assert CLR/
        BSET  PORTC,Y   $02   De-assert CLR/
*
        BCLR  PORTC,Y   $01  Assert CS/
*
```

```
WAIT    LDAA   SPSR          Loop to wait for SPIF
        BPL    WAIT          SPIF is the MSB of SPSR
*                            (when SPIF is set, SPSR is negated)
        INX                  Increment counter to next byte for xfer
        CPX    #SDI2+1       Are we done yet ?
        BNE    TFRLP         If not, xfer the second byte
*
*Update DAC output with contents of DAC register
*
        BCLR   PORTD,Y  $20  Assert LD/
        BSET   PORTD,Y  $20  Latch DAC register
*
        BSET   PORTC,Y  $01  De-assert CS/
        PULA When done, restore registers X, Y & A
        PULY
        PULX
        RTS             ** Return to Main Program **
```

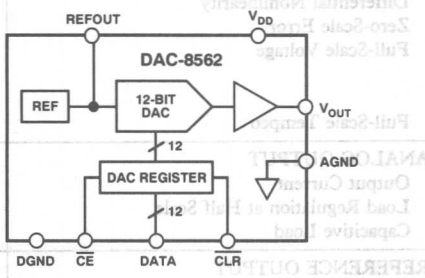
+5 Volt, Parallel Input Complete 12-Bit DAC

DAC8562

FEATURES
- Complete 12-Bit DAC
- No External Components
- Single +5 Volt Operation
- 1 mV/Bit with 4.095 V Full Scale
- True Voltage Output, ±5 mA Drive
- Very Low Power −3 mW

APPLICATIONS
- Digitally Controlled Calibration
- Servo Controls
- Process Control Equipment
- PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC-8562 is a complete, parallel input, 12-bit, voltage output DAC designed to operate from a single +5 volt supply. Built using a CBCMOS process, these monolithic DACs offer the user low cost, and ease-of-use in +5 volt only systems.

Included on the chip, in addition to the DAC, is a rail-to-rail amplifier, latch and reference. The reference (REFOUT) is trimmed to 2.5 volts, and the on-chip amplifier gains up the DAC output to 4.095 volts full scale. The user needs only supply a +5 volt supply.

The DAC-8562 is coded straight binary. The op amp output swings from 0 to +4.095 volts for a one millivolt per bit resolution, and is capable of driving ±5 mA. Built using low temperature-coefficient silicon-chrome thin-film resistors, excellent linearity error over temperature has been achieved as shown below in the linearity error versus digital input code plot.

Digital interface is parallel and high speed to interface to the fastest processors without wait states. The interface is very simple requiring only a single $\overline{CE}$ signal. An asynchronous $\overline{CLR}$ input sets the output to zero scale.

The DAC-8562 is available in two different 20-pin packages, plastic DIP and SOL-20. Each part is fully specified for operation over −40°C to +85°C, and the full +5 V ± 5% power supply range.

For MIL-STD-883 applications, contact your local ADI sales office for the DAC-8562/883 data sheet which specifies operation over the −55°C to +125°C temperature range.

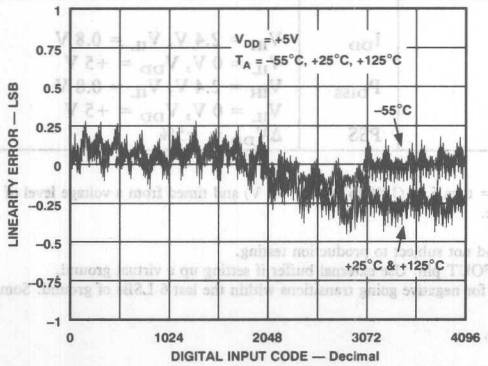


Figure 1. Linearity Error vs. Digital Input Code Plot

DAC8562—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5.0 V ± 5%, R_L = No Load, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N	Note 2	12			Bits
Relative Accuracy	INL	E Grade	−1/2	±1/4	+1/2	LSB
		F Grade	−1	±3/4	+1	LSB
Differential Nonlinearity	DNL	No Missing Codes	−1	±3/4	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+1/2	+3	LSB
Full-Scale Voltage	V_{FS}	Data = FFF_H[3]				
		E Grade	4.087	4.095	4.103	V
		F Grade	4.079	4.095	4.111	V
Full-Scale Tempco	TCV_{FS}	Notes 3, 4		±16		ppm/°C
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = 800_H		±5	±7	mA
Load Regulation at Half Scale	LD_{REG}	R_L = 402 Ω to ∞, Data = 800_H		1	3	LSB
Capacitive Load	C_L	No Oscillation[4]		500		pF
REFERENCE OUTPUT						
Output Voltage	V_{REF}		2.484	2.500	2.516	V
Output Source Current	I_{REF}	Note 5	5	7		mA
Line Rejection	LN_{REJ}				0.08	%/V
Load Regulation	LD_{REG}	I_{REF} = 0 to 5 mA			0.1	%/mA
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance	C_{IL}	Note 4			10	pF
INTERFACE TIMING SPECIFICATIONS[1, 4]						
Chip Enable Pulse Width	t_{CEW}		30			ns
Data Setup	t_{DS}		30			ns
Data Hold	t_{DH}		10			ns
Clear Pulse Width	t_{CLRW}		20			ns
AC CHARACTERISTICS[4]						
Voltage Output Settling Time[6]	t_S	To ±1 LSB of Final Value		16		µs
Digital Feedthrough				35		nV sec
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		3	6	mA
		V_{IL} = 0 V, V_{DD} = +5 V		0.6	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		15	30	mW
		V_{IL} = 0 V, V_{DD} = +5 V		3	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTES

[1]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]1 LSB=1 mV for 0 to +4.095 V output range.

[3]Includes internal voltage reference error.

[4]These parameters are guaranteed by design and not subject to production testing.

[5]Very little sink current is available at the REFOUT pin. Use external buffer if setting up a virtual ground.

[6]The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

Specifications subject to change without notice.

WAFER TEST LIMITS

(@ V_{DD} = +5.0 V ± 5%, R_L = No Load, T_A = +25°C, applies to part number DAC8562GBC only, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Relative Accuracy	INL		−1	±3/4	+1	LSB
Differential Nonlinearity	DNL	No Missing Codes	−1	±3/4	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+1/2	+3	LSB
Full-Scale Voltage	V_{FS}	Data = FFF_H	4.085	4.095	4.105	V
Reference Output Voltage	V_{REF}		2.490	2.500	2.510	V
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		3	6	mA
		V_{IL} = 0 V, V_{DD} = +5 V		0.6	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		15	30	mW
		V_{IL} = 0 V, V_{DD} = +5 V		3	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTE

[1]Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to DGND and AGND . . . . . −0.3 V, +10 V
Logic Inputs to DGND . . . . . −0.3 V, V_{DD} + 0.3 V
V_{OUT} to AGND . . . . . −0.3 V, V_{DD} + 0.3 V
V_{REFOUT} to AGND . . . . . −0.3 V, V_{DD} + 0.3 V
AGND to DGND . . . . . −0.3 V, V_{DD}
I_{OUT} Short Circuit to GND . . . . . 50 mA
Package Power Dissipation . . . . . (T_J max−T_A)/θ_{JA}
Thermal Resistance θ_{JA}
20-Pin Plastic DIP Package (P) . . . . . 74°C/W
20-Lead SOIC Package (S) . . . . . 89°C/W
Maximum Junction Temperature (T_J max) . . . . . 150°C
Operating Temperature Range . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

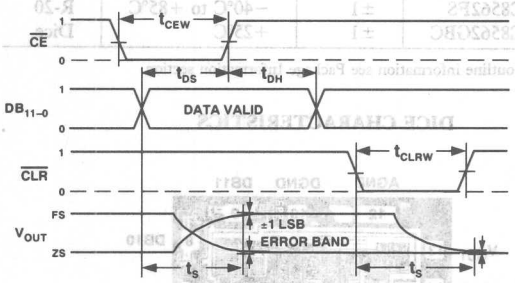


Figure 2. Timing Diagram

Table I. Control Logic Truth Table

$\overline{CE}$	$\overline{CLR}$	DAC Register Function
H	H	Latched
L	H	Transparent
↑ +	H	Latched with New Data
X	L	Loaded with All Zeros
H	↑ +	Latched All Zeros

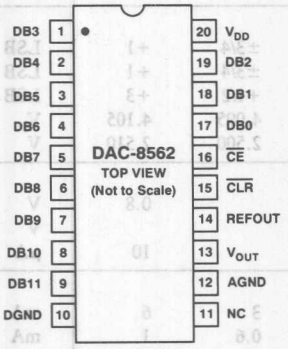
↑ + Positive Logic Transition; X Don't Care.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

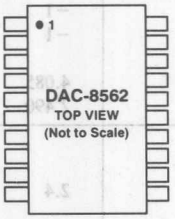
PIN CONFIGURATIONS

20-Pin P-DIP (N-20)



NC = NO CONNECT

SOL-20 (R-20)

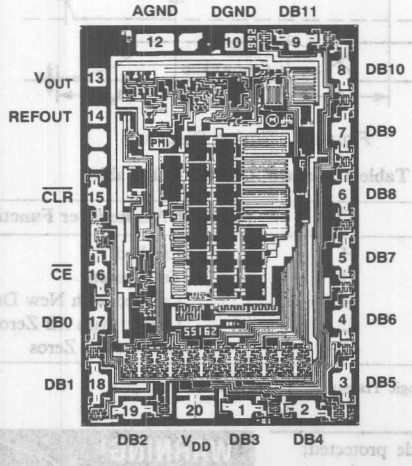


ORDERING GUIDE

Model	INL (LSB)	Temperature Range	Package Option*
DAC8562EP	±1/2	−40°C to +85°C	N-20
DAC8562FP	±1	−40°C to +85°C	N-20
DAC8562FS	±1	−40°C to +85°C	R-20
DAC8562GBC	±1	+25°C	Dice

*For outline information see Package Information section.

DICE CHARACTERISTICS



SUBSTRATE IS COMMON WITH V_{DD}.
TRANSISTOR COUNT: 524
DIE SIZE: 0.070 INCH x 0.105 INCH; 7350 SQ MILS

Table II. Nominal Output Voltage vs. Input Code

Binary	Hex	Decimal	Output (V)	
0000 0000 0000	000	0	0.000	Zero Scale
0000 0000 0001	001	1	0.001	
0000 0000 0010	002	2	0.002	
0000 0000 1111	00F	15	0.015	
0000 0001 0000	010	16	0.016	
0000 1111 1111	0FF	255	0.255	
0001 0000 0000	100	256	0.256	
0001 1111 1111	1FF	511	0.511	
0010 0000 0000	200	512	0.512	
0011 1111 1111	3FF	1023	1.023	
0100 0000 0000	400	1024	1.024	
0111 1111 1111	7FF	2047	2.047	
1000 0000 0000	800	2048	2.048	Half Scale
1100 0000 0000	C00	3072	3.072	
1111 1111 1111	FFF	4095	4.095	Full Scale

PIN DESCRIPTIONS

Pin	Name	Description
20	V_{DD}	Positive supply. Nominal value +5 volts, ±5%.
1–9 17–19	DB0–DB11	Twelve Binary Data Bit inputs. DB11 is the MSB and DB0 is the LSB.
16	$\overline{CE}$	Chip Enable. Active low input.
15	$\overline{CLR}$	Active low digital input that clears the DAC register to zero, setting the DAC to minimum scale.
8	DGND	Digital ground for input logic.
12	AGND	Analog Ground. Ground reference for the internal bandgap reference voltage, the DAC, and the output buffer.
13	V_{OUT}	Voltage output from the DAC. Fixed output voltage range of 0 V to 4.095 V with 1 mV/LSB. An internal temperature stabilized reference maintains a fixed full-scale voltage independent of time, temperature and power supply variations.
14	REFOUT	Nominal 2.5 V reference output voltage. This node must be buffered if required to drive external loads.
11	NC	No Connection. Leave pin floating.

operation. It contains a voltage-switched, 12-bit, laser-trimmed digital-to-analog converter, a curvature-corrected bandgap reference, a rail-to-rail output op amp, and a DAC register. The parallel data interface consists of 12 data bits, DB0–DB11, and a active low $\overline{CE}$ strobe. In addition, an asynchronous $\overline{CLR}$ pin will set all DAC register bits to zero causing the V_{OUT} to become zero volts. This function is useful for power on reset or system failure recovery to a known state.

D/A CONVERTER SECTION

The internal DAC is a 12-bit voltage-mode device with an output that swings from AGND potential to the 2.5 volt internal bandgap voltage. It uses a laser trimmed R-2R ladder which is switched by N channel MOSFETs. The output voltage of the DAC has a constant resistance independent of digital input code. The DAC output (not available to the user) is internally connected to the rail-to-rail output op amp.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. This low power amplifier contains a differential PNP pair input stage which provides low offset voltage and low noise, as well as the ability to amplify the zero-scale DAC output voltages. The rail-to-rail amplifier is configured in a gain of 1.6384 (= 4.095 V/2.5 V) in order to set the 4.095 volt full-scale output (1 mV/LSB). See Figure 3 for an equivalent circuit schematic of the analog section.

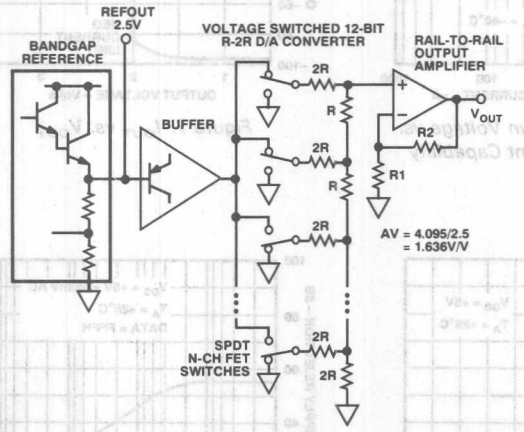


Figure 3. Equivalent DAC-8562 Schematic of Analog Portion

The op amp has a 16 μs typical settling time to 0.01%. There are slight differences in settling time for negative slewing signals versus positive. See the oscilloscope photos in the Typical Performances section of this data sheet.

OUTPUT SECTION

The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 4 shows an equivalent output schematic of the rail-to-rail amplifier with its N channel pull down FETs that supply tolerance value of 4.75 volts.

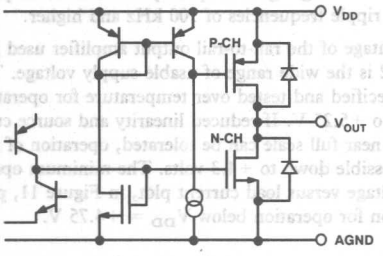


Figure 4. Equivalent Analog Output Circuit

Figures 5 and 6 in the typical performance characteristics section provide information on output swing performance near ground and full scale as a function of load. In addition to resistive load driving capability, the amplifier has also been carefully designed and characterized for up to 500 pF capacitive load driving capability.

REFERENCE SECTION

The internal 2.5 V curvature-corrected bandgap voltage reference is laser trimmed for both initial accuracy and low temperature coefficient. The voltage generated by the reference is available at the REFOUT pin. Since REFOUT is *not* intended to drive external loads, it must be buffered—refer to the applications section for more information. The equivalent emitter follower output circuit of the REFOUT pin is shown in Figure 3.

Bypassing the REFOUT pin is not required for proper operation. Figure 7 shows broadband noise performance.

POWER SUPPLY

The very low power consumption of the DAC-8562 is a direct result of a circuit design optimizing use of the CBCMOS process. By using the low power characteristics of the CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors, good analog accuracy is achieved.

For power-consumption sensitive applications it is important to note that the internal power consumption of the DAC-8562 is strongly dependent on the actual logic-input voltage-levels present on the DB0–DB11, $\overline{CE}$ and $\overline{CLR}$ pins. Since these inputs are standard CMOS logic structures, they contribute static power dissipation dependent on the actual driving logic V_{OH} and V_{OL} voltage levels. The graph in Figure 9 shows the effect on total DAC-8562 supply current as a function of the actual value of input logic voltage. Consequently for optimum dissipation use of CMOS logic versus TTL provides minimal dissipation in the static state. A V_{INL} = 0 V on the DB0–DB11 pins provides the lowest standby dissipation of 600 μA with a +5 V power supply.

As with any analog system, it is recommended that the DAC-8562 power supply be bypassed on the same PC card that contains the chip. Figure 10 shows the power supply rejection versus frequency performance. This should be taken into account when using higher frequency switched-mode power supplies with ripple frequencies of 100 kHz and higher.

One advantage of the rail-to-rail output amplifier used in the DAC-8562 is the wide range of usable supply voltage. The part is fully specified and tested over temperature for operation from +4.75 V to +5.25 V. If reduced linearity and source current capability near full scale can be tolerated, operation of the DAC-8562 is possible down to +4.3 volts. The minimum operating supply voltage versus load current plot, in Figure 11, provides information for operation below V_{DD} = +4.75 V.

TIMING AND CONTROL

The DAC-8562 has a 12-bit DAC register that simplifies interface to a 12-bit (or wider) data bus. The latch is controlled by the Chip Enable ($\overline{CE}$) input. If the application does not involve a data bus, wiring $\overline{CE}$ low allows direct operation of the DAC.

The data latch is level triggered and acquires data from the data bus during the time period when $\overline{CE}$ is low. When $\overline{CE}$ goes high, the data is latched into the register and held until $\overline{CE}$ returns low. The minimum time required for the data to be present on the bus before $\overline{CE}$ returns high is called the data setup time (t_{DS}) as seen in Figure 2. The data hold time (t_{DH}) is the amount of time that the data has to remain on the bus after $\overline{CE}$ goes high. The high speed timing offered by the DAC-8562 provides for direct interface with no wait states in all but the fastest microprocessors.

Typical Performance Characteristics

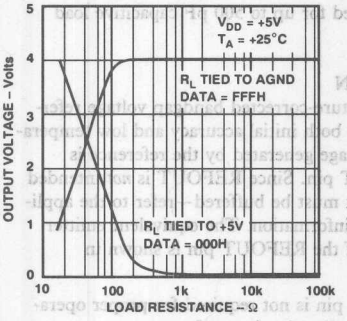


Figure 5. Output Swing vs. Load

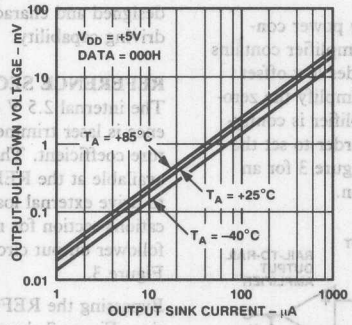


Figure 6. Pull-Down Voltage vs. Output Sink Current Capability

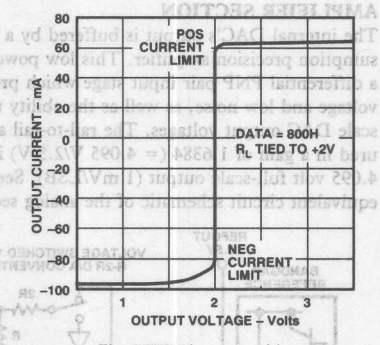


Figure 7. I_{OUT} vs. V_{OUT}

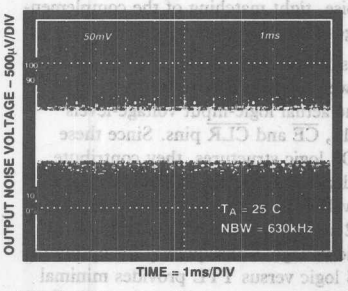


Figure 8. Broadband Noise

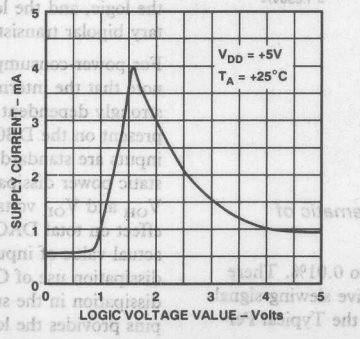


Figure 9. Supply Current vs. Logic Input Voltage

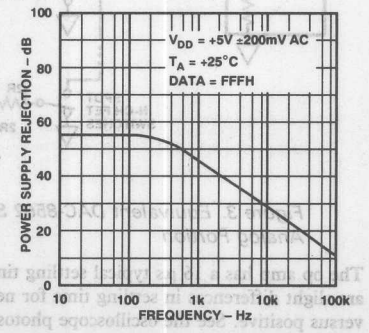


Figure 10. Power Supply Rejection vs. Frequency

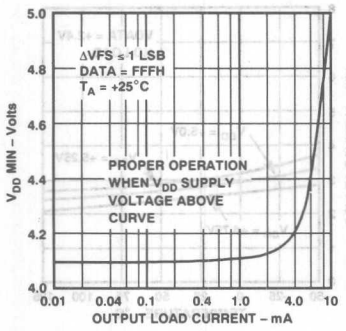


Figure 11. Minimum Supply Voltage vs. Load

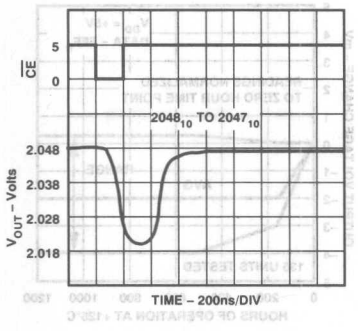


Figure 12. Midscale Transition Performance

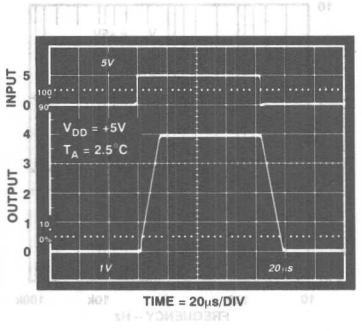


Figure 13. Large Signal Settling Time

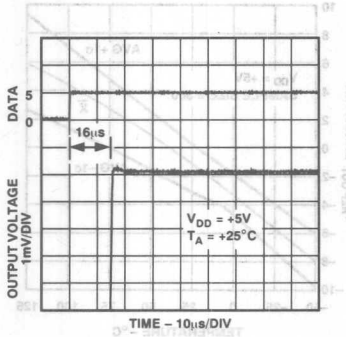


Figure 14. Output Voltage Rise Time Detail

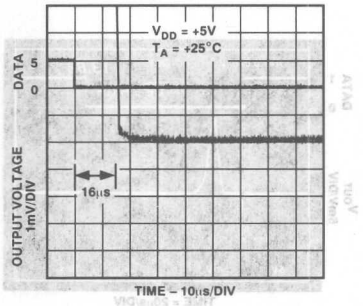


Figure 15. Output Voltage Fall Time Detail

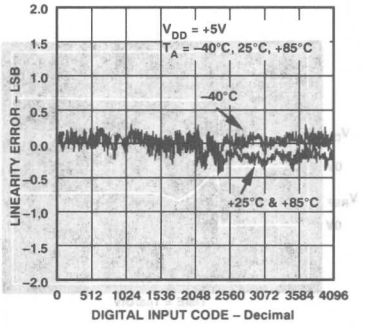


Figure 16. Linearity Error vs. Digital Code

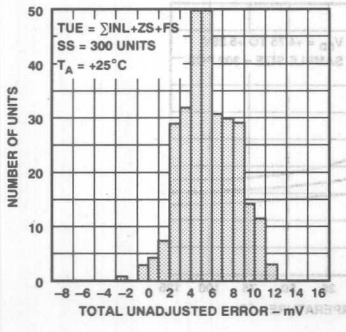


Figure 17. Total Unadjusted Error Histogram

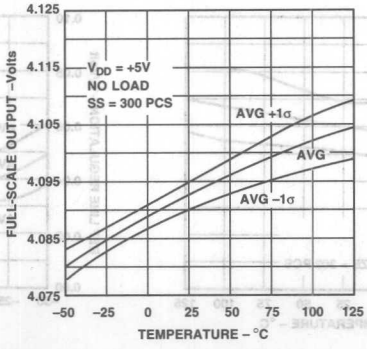


Figure 18. Full-Scale Voltage vs. Temperature

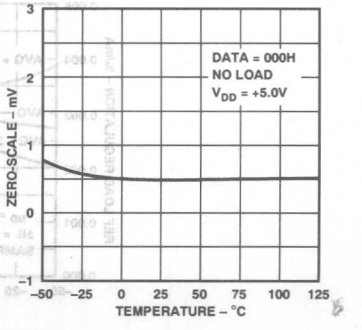


Figure 19. Zero-Scale Voltage vs. Temperature

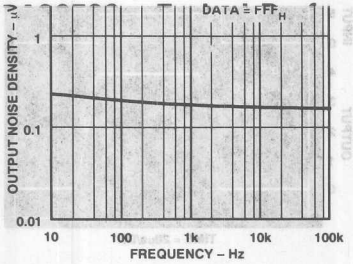


Figure 20. Output Voltage Noise Density vs. Frequency

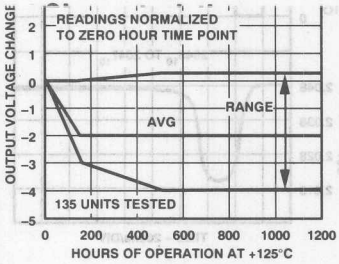


Figure 21. Long-Term Drift Accelerated by Burn-In

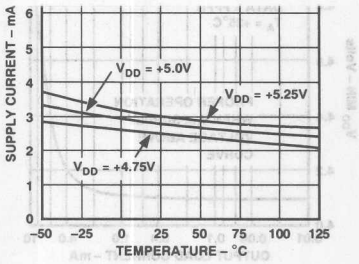


Figure 22. Supply Current vs. Temperature

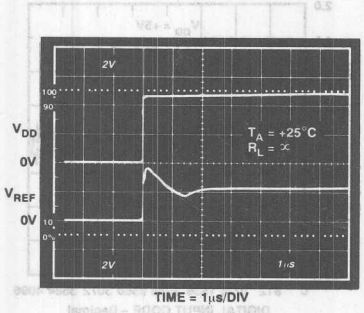


Figure 23. Reference Startup vs. Time

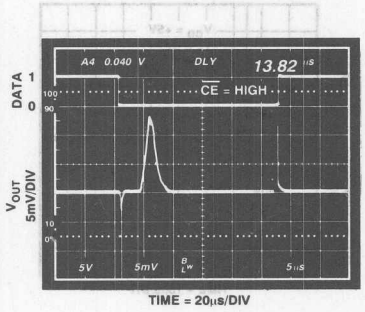


Figure 24. Digital Feedthrough vs. Time

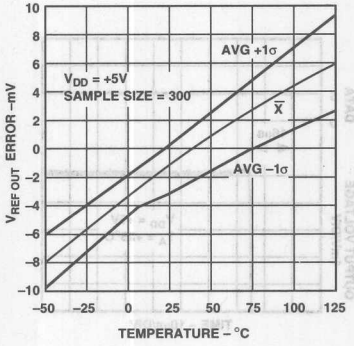


Figure 25. Reference Error vs. Temperature

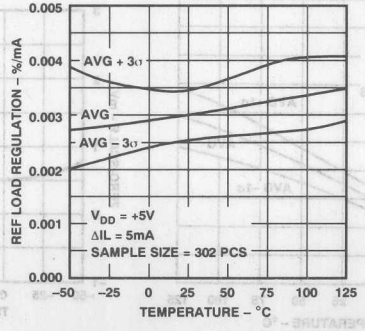


Figure 26. Reference Load Regulation vs. Temperature

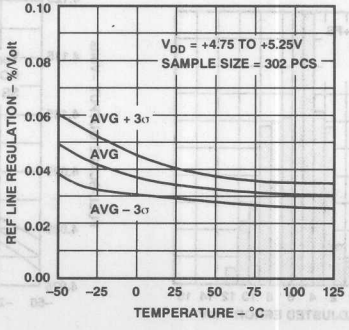


Figure 27. Reference Line Regulation vs. Temperature

APPLICATIONS SECTION

Power Supplies, Bypassing, and Grounding

All precision converter products require careful application of good grounding practices to maintain full-rated performance. Because the DAC-8562 has been designed for +5 V applications, it is ideal for those applications under microprocessor or microcomputer control. In these applications, digital noise is prevalent; therefore, special care must be taken to assure that its inherent precision is maintained. This means that particularly good engineering judgment should be exercised when addressing the power supply, grounding, and bypassing issues using the DAC-8562.

The power supply used for the DAC-8562 should be well filtered and regulated. The device has been completely characterized for a +5 V supply with a tolerance of ±5 %. Since a +5 V logic supply is almost universally available, it is not recommended to connect the DAC directly to an unfiltered logic supply without careful filtering. Because it is convenient, a designer might be inclined to tap a logic circuit's supply for the DAC's supply. Unfortunately, this is not wise because fast logic with nanosecond transition edges induces high current pulses. The high transient current pulses can generate glitches hundreds of millivolts in amplitude due to wiring resistances and inductances. This high frequency noise will corrupt the analog circuits internal to the DAC and cause errors. Even though their spike noise is lower in amplitude, directly tapping the output of a +5 V system supplies can cause errors because these supplies are of the switching regulator type that can and do generate a great deal of high frequency noise. Therefore, the DAC and any associated analog circuitry should be powered directly from the system power supply outputs using appropriate filtering. Figure 28 illustrates how a clean, analog-grade supply can be generated from a +5 V logic supply using a differential LC filter with separate power supply and return lines. With the values shown, this filter can easily handle 100 mA of load current without saturating the ferrite cores. Higher current capacity can be achieved with larger ferrite cores. For lowest noise, all electrolytic capacitors should be low ESR (Equivalent Series Resistance) type.

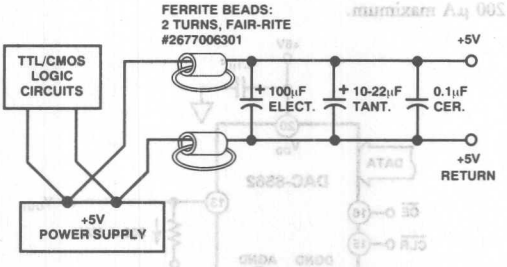


Figure 28. Properly Filtering a +5 V Logic Supply Can Yield a High Quality Analog Supply

The DAC-8562 includes two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (Pin 10) and AGND (Pin 12). The DGND pin is the return for the digital circuit sections of the DAC and serves as their input threshold reference point. Thus DGND should be connected to the same ground as the circuitry that drives the digital inputs.

Pin 12, AGND, serves as the supply rail for the internal voltage reference and the output amplifier. This pin should also serve as the reference point for all analog circuitry associated with the DAC-8562. Therefore, to minimize any errors, it is recommended that the AGND connection of the DAC-8562 be connected to a high quality analog ground. If the system contains any analog signal path carrying a significant amount of current, then that path should have its own return connection to Pin 12.

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common to one place only. If the common tie point is remote and an accidental disconnection of that one common tie point were to occur due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the DAC-8562, it is recommended that the common ground tie points be provided at each such device. If only one system ground can be connected directly to the DAC-8562, it recommended that the analog common be used. If the system's AGND has suitably low impedance, then the digital signal currents flowing in it should not seriously affect the ground noise. The amount of digital noise introduced by connecting the two grounds together at the device will not adversely affect system performance due to loss of digital noise immunity.

Generous bypassing of the DAC's supply goes a long way in reducing supply line-induced errors. Local supply bypassing consisting of a 10 µF tantalum electrolytic in parallel with a 0.1 µF ceramic is recommended. The decoupling capacitors should be connected between the DAC's supply pin (Pin 20) and the analog ground (Pin 12). Figure 29 shows how the DGND, AGND, and bypass connections should be made to the DAC-8562.

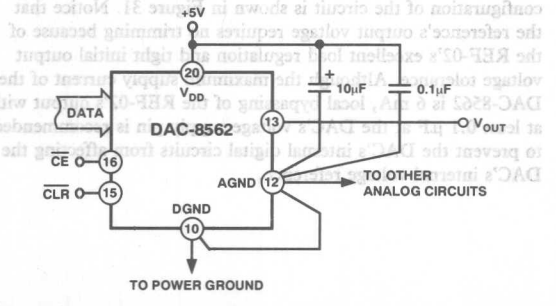


Figure 29. Recommended Grounding and Bypassing Scheme for the DAC-8562

Unipolar Output Operation

This is the basic mode of operation for the DAC-8562. As shown in Figure 30, the DAC-8562 has been designed to drive loads as low as 820 Ω in parallel with 500 pF. The code table for this operation is shown in Table III.

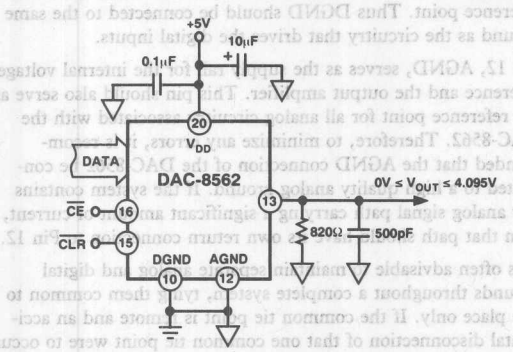


Figure 30. Unipolar Output Operation

Table III. Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	+4.095
801	2049	+2.049
800	2048	+2.048
7FF	2047	+2.047
000	0	0

Operating the DAC-8562 on +12 V or +15 V Supplies Only

Although the DAC-8562 has been specified to operate on a single, +5 V supply, a single +5 V supply may not be available in many applications. Since the DAC-8562 consumes no more than 6 mA, maximum, then an integrated voltage reference, such as the REF-02, can be used as the DAC-8562 +5 V supply. The configuration of the circuit is shown in Figure 31. Notice that the reference's output voltage requires no trimming because of the REF-02's excellent load regulation and tight initial output voltage tolerance. Although the maximum supply current of the DAC-8562 is 6 mA, local bypassing of the REF-02's output with at least 0.1 µF at the DAC's voltage supply pin is recommended to prevent the DAC's internal digital circuits from affecting the DAC's internal voltage reference.

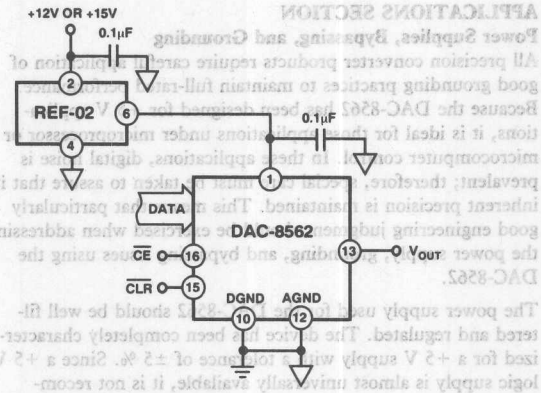


Figure 31. Operating the DAC-8562 on +12 V or +15 V Supplies Using a REF-02 Voltage Reference

Measuring Offset Error

One of the most commonly specified endpoint errors associated with real-world nonideal DACs is offset error.

In most DAC testing, the offset error is measured by applying the zero-scale code and measuring the output deviation from 0 volt. There are some DACs where offset errors may be present but not observable at the zero scale because of other circuit limitations (for example, zero coinciding with single supply ground). In these DACs, nonzero output at zero code cannot be read as the offset error. In the DAC-8562, for example, the zero-scale error is specified to be +3 LSBs. Since zero scale coincides with zero volt, it is not possible to measure negative offset error. By adding a pull-down resistor from the output of the DAC-8562 to a negative supply as shown in Figure 32, offset errors can now be read at zero code. This configuration forces the output P-channel MOSFET to source current to the negative supply thereby allowing the designer to determine in which direction the offset error appears. The value of the resistor should be such that, at zero code, current through the resistor is 200 µA maximum.

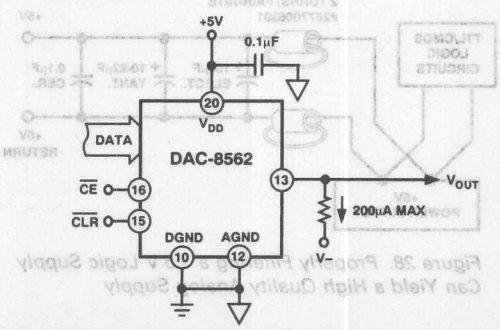


Figure 32. Measuring Zero-Scale or Offset Error

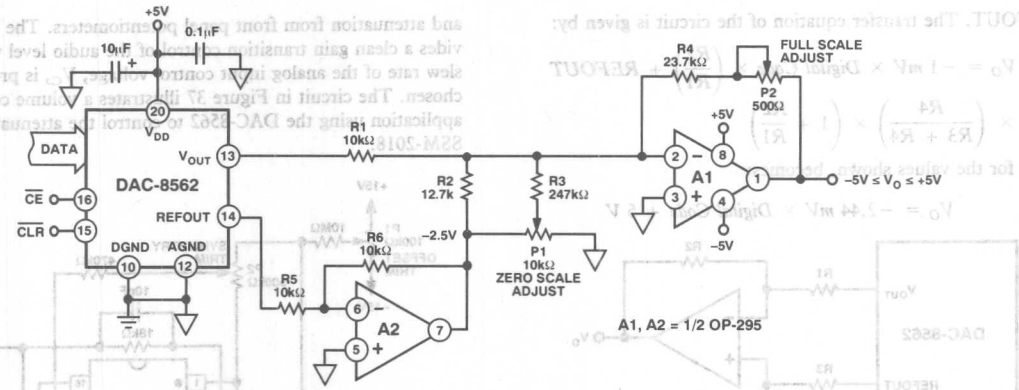


Figure 33. Bipolar Output Operation

Bipolar Output Operation

Although the DAC-8562 has been designed for single supply operation, bipolar operation is achievable using the circuit illustrated in Figure 33. The circuit uses a single supply, rail-to-rail OP-295 op amp and the DAC's internal +2.5 V reference to generate the −2.5 V reference required to level-shift the DAC output voltage. The circuit has been configured to provide an output voltage in the range $-5\ V \le V_{OUT} \le +5\ V$ and is coded in complementary offset binary. Although each DAC LSB corresponds to 1 mV, each output LSB has been scaled to 2.44 mV. Table IV provides the relationship between the digital codes and output voltage.

The transfer function of the circuit is given by:

$$V_O = -1\ mV \times Digital\ Code \times \left(\frac{R4}{R1}\right) + 2.5 \times \left(\frac{R4}{R2}\right)$$

and, for the circuit values shown, becomes:

$$V_O = -2.44\ mV \times Digital\ Code + 5\ V$$

Table IV. Bipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	−4.9976
801	2049	−2.44E−3
800	2048	0
7FF	2047	+2.44E−3
000	0	+5

To maintain monotonicity and accuracy, R1, R2, R4, R5, and R6 should be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R1 and R2 causes offset and gain errors while an R4 to R1 and R2 mismatch yields gain errors.

For applications that do not require high accuracy, the circuit illustrated in Figure 34 can also be used to generate a bipolar output voltage. In this circuit, only one op amp is used and no potentiometers are used for offset and gain trim. The output voltage is coded in offset binary and is given by:

$$V_O = 1\ mV \times Digital\ Code \times \left(\frac{R4}{R3 + R4}\right) \times \left(1 + \frac{R2}{R1}\right) - REFOUT \times \left(\frac{R2}{R1}\right)$$

For the ±2.5 V output range and the circuit values shown in the table, the transfer equation becomes:

$$V_O = 1.22\ mV \times Digital\ Code - 2.5\ V$$

Similarly, for the ±5 V output range, the transfer equation becomes:

$$V_O = 2.44\ mV \times Digital\ Code - 5\ V$$

Note that, for ±5 V output voltage operation, R5 is required as a pull-down for REFOUT. Or, REFOUT can be buffered by an op amp configured as a follower that can source and sink current.

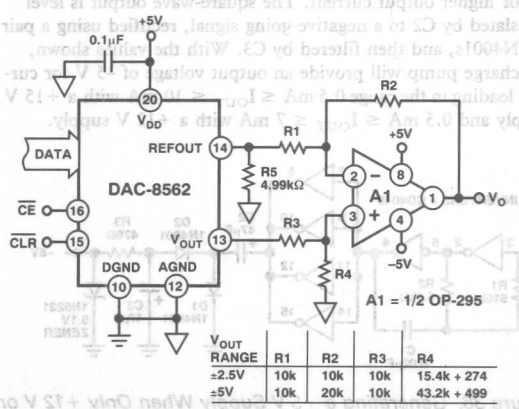


Figure 34. Bipolar Output Operation Without Trim Version 1

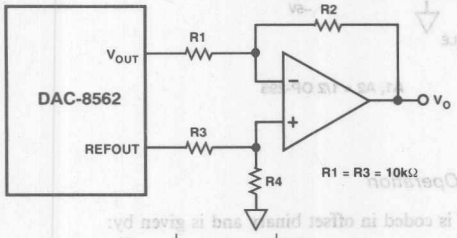
Alternatively, the output voltage can be coded in complementary offset binary using the circuit in Figure 35. This configuration eliminates the need for a pull-down resistor or an op amp for

REFOUT. The transfer equation of the circuit is given by:

$$V_O = -1\,mV \times Digital\ Code \times \left(\frac{R2}{R1}\right) + REFOUT \times \left(\frac{R4}{R3 + R4}\right) \times \left(1 + \frac{R2}{R1}\right)$$

and, for the values shown, becomes:

$$V_O = -2.44\,mV \times Digital\ Code + 5\ V$$



V_O RANGE	R2	R4
±5V	23.7k + 715	13.7k + 169Ω

Figure 35. Bipolar Output Operation Without Trim Version 2

Generating a Negative Supply Voltage

Some applications may require bipolar output configuration, but only have a single power supply rail available. This is very common in data acquisition systems using microprocessor-based systems. In these systems, only +12 V, +15 V, and/or +5 V are available. Shown in Figure 36 is a method of generating a negative supply voltage using one CD4049, a CMOS hex inverter, operating on +12 V or +15 V. The circuit is essentially a charge pump where two of the six are used as an oscillator. For the values shown, the frequency of oscillation is approximately 3.5 kHz and is fairly insensitive to supply voltage because R1 > 2 × R2. The remaining four inverters are wired in parallel for higher output current. The square-wave output is level translated by C2 to a negative-going signal, rectified using a pair of 1N4001s, and then filtered by C3. With the values shown, the charge pump will provide an output voltage of –5 V for current loading in the range 0.5 mA ≤ I_{OUT} ≤ 10 mA with a +15 V supply and 0.5 mA ≤ I_{OUT} ≤ 7 mA with a +12 V supply.

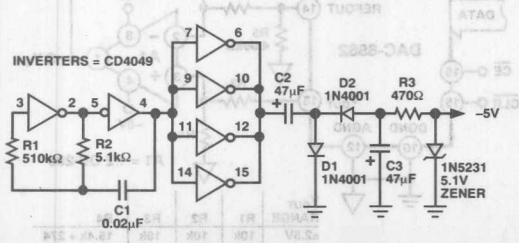


Figure 36. Generating a −5 V Supply When Only +12 V or +15 V Are Available

Audio Volume Control

The DAC-8562 is well suited to control digitally the gain or attenuation of a voltage controlled amplifiers. In professional audio mixing consoles, music synthesizers, and other audio processors, VCAs, such as the SSM-2018, adjust audio channel gain and attenuation from front panel potentiometers. The VCA provides a clean gain transition control of the audio level when the slew rate of the analog input control voltage, V_C, is properly chosen. The circuit in Figure 37 illustrates a volume control application using the DAC-8562 to control the attenuation of the SSM-2018.

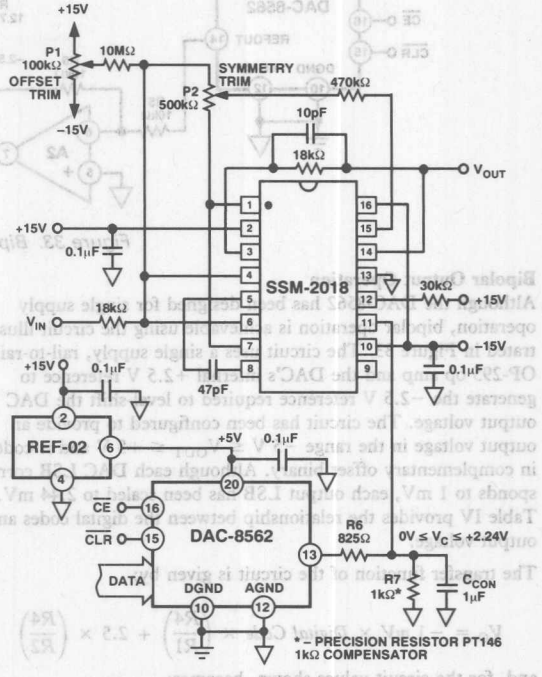


Figure 37. Audio Volume Control

Since the supply voltage available in these systems is typically ±15 V or ±18 V, a REF-02 is used to supply the +5 V required to power the DAC. No trimming of the reference is required because of the reference's tight initial tolerance and low supply current consumption of the DAC-8562. The SSM-2018 is configured as a unity-gain buffer when its control voltage equals 0 volt. This corresponds to a 000_H code from the DAC-8562. Since the SSM-2018 exhibits a gain constant of −28 mV/dB (typical), the DAC's full-scale output voltage has to be scaled down by R6 and R7 to provide 80 dB of attenuation when the digital code equals FFF_H. Therefore, every DAC LSB corresponds to 0.02 dB of attenuation. Table V illustrates the attenuation versus digital code of the volume control circuit.

Table V. SSM-2018 VCA Attenuation vs. DAC-8562 Input Code

Hexadecimal Number in DAC Register	Control Voltage (V)	VCA Attenuation (dB)
000	0	0
400	+0.56	20
800	+1.12	40
C00	+1.68	60
FFF	+2.24	80

To compensate for the SSM-2018's gain constant temperature coefficient of –3300 ppm/°C, a 1 kΩ, temperature-sensitive resistor (R7) manufactured by the Precision Resistor Company with a temperature coefficient of +3500 ppm/°C is used. A C_{CON} of 1 μF provides a control transition time of 1 ms which yields a click-free change in the audio channel attenuation. Symmetry and offset trimming details of the VCA can be found in the SSM-2018 data sheet.

Information regarding the PT146 1 kΩ "Compensator" can be obtained by contacting:

Precision Resistor Company, Incorporated
10601 75th Street North
Largo, Fl 34647
(813) 541-5771

A High-Compliance, Digitally Controlled Precision Current Source

The circuit in Figure 38 shows the DAC-8562 controlling a high-compliance, precision current source using an AMP-05 instrumentation amplifier. The AMP-05's reference pin becomes the input, and the "old" inputs now monitor the voltage across a precision current sense resistor, R_{CS}. Voltage gain is set to unity, so the transfer function is given by the following equation:

$$I_{OUT} = \frac{V_{IN}}{R_{CS}}$$

If R_{CS} equals 100 Ω, the output current is limited to +10 mA with a 1 V input. Therefore, each DAC LSB corresponds to 2.4 μA. If a bipolar output current is required, then the circuit in Figure 33 can be modified to drive the AMP-05's reference pin with a ±1 V input signal.

Potentiometer P1 trims the output current to zero with the input at 0 V. Fine gain adjustment can be accomplished by adjusting R1 or R2.

A Digitally Programmable Window Detector

A digitally programmable, upper/lower limit detector using two DAC-8562s is shown in Figure 39. The required upper and lower limits for the test are loaded into each DAC individually by controlling HDAC/$\overline{LDAC}$. If a signal at the test input is not within the programmed limits, the output will indicate a logic zero which will turn the red LED on.

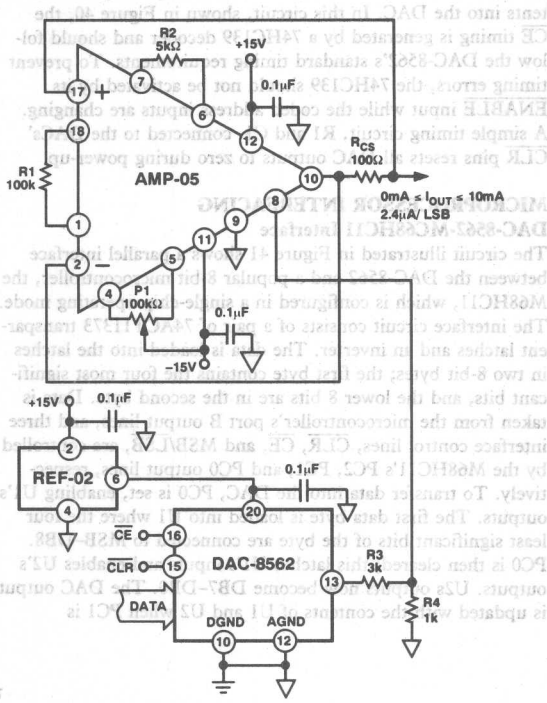


Figure 38. A High-Compliance, Digitally Controlled Precision Current Source

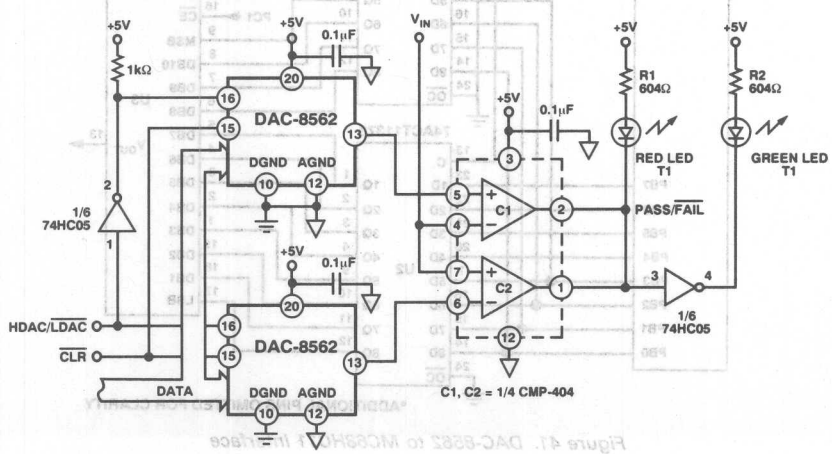


Figure 39. A Digitally Programmable Window Detector

Decoding Multiple DAC-8562s

The $\overline{CE}$ function of the DAC-8562 can be used in applications to decode a number of DACs. In this application, all DACs receive the same input data; however, only one of the DACs' $\overline{CE}$ input is asserted to transfer its parallel input register contents into the DAC. In this circuit, shown in Figure 40, the $\overline{CE}$ timing is generated by a 74HC139 decoder and should follow the DAC-8562's standard timing requirements. To prevent timing errors, the 74HC139 should not be activated by its $\overline{ENABLE}$ input while the coded address inputs are changing. A simple timing circuit, R1 and C1, connected to the DACs' $\overline{CLR}$ pins resets all DAC outputs to zero during power-up.

MICROPROCESSOR INTERFACING

DAC-8562-MC68HC11 Interface

The circuit illustrated in Figure 41 shows a parallel interface between the DAC-8562 and a popular 8-bit microcontroller, the M68HC11, which is configured in a single-chip operating mode. The interface circuit consists of a pair of 74ACT11373 transparent latches and an inverter. The data is loaded into the latches in two 8-bit bytes; the first byte contains the four most significant bits, and the lower 8 bits are in the second byte. Data is taken from the microcontroller's port B output lines, and three interface control lines, $\overline{CLR}$, $\overline{CE}$, and MSB/$\overline{LSB}$, are controlled by the M68HC11's PC2, PC1, and PC0 output lines, respectively. To transfer data into the DAC, PC0 is set, enabling U1's outputs. The first data byte is loaded into U1 where the four least significant bits of the byte are connected to MSB–DB8. PC0 is then cleared; this latches U1's inputs and enables U2's outputs. U2s outputs now become DB7–DB0. The DAC output is updated with the contents of U1 and U2 when PC1 is cleared. The DAC's $\overline{CLR}$ input, controlled by the M68HC11's PC2 output line, provides an asynchronous clear function that sets the DAC's output to zero. Included in this section is the source code for operating the DAC-8562–M68HC11 interface.

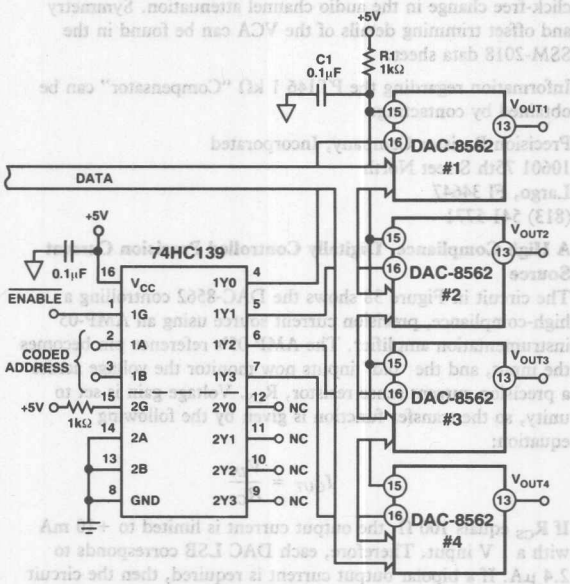


Figure 40. Decoding Multiple DAC-8562s Using the $\overline{CE}$ Pin

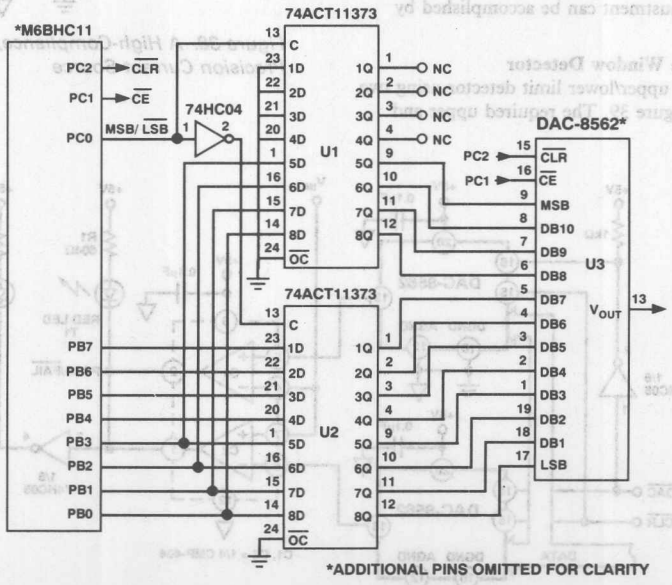


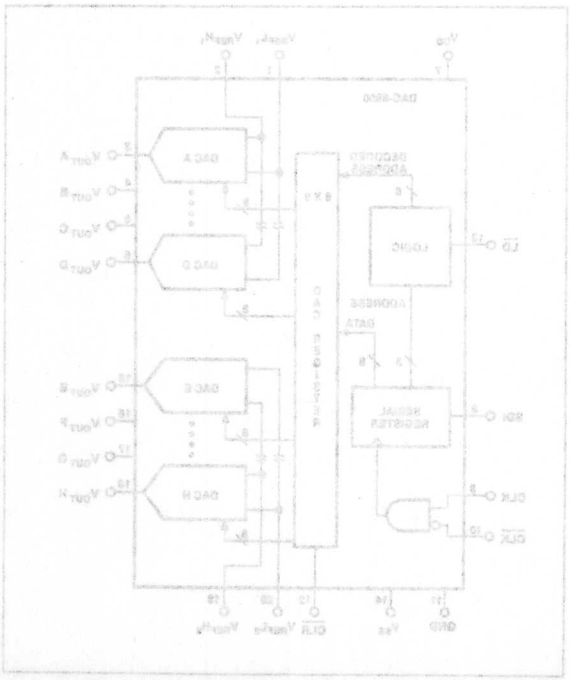
Figure 41. DAC-8562 to MC68HC11 Interface

DAC-8562 — M68HC11 Interface Program Source Code

```
*
* DAC-8562 to M68HC11 Interface Assembly Program
* Adolfo A. Garcia
* September 14, 1992
*
* M68HC11 Register definitions
*
PORTB   EQU   $1004
PORTC   EQU   $1003          Port C control register
*                            "0,0,0,0;0,CLR/,CE/,MSB-LSB/"
DDRC    EQU   $1007          Port C data direction
*
* RAM variables:             MSBS are encoded from 0 (Hex) to F (Hex)
*                            LSBS are encoded from 00 (Hex) to FF (Hex)
*                            DAC requires two 8-bit loads
*
MSBS    EQU   $00            Hi-byte: "0,0,0.0;MSB,DB10,DB9,DB8"
LSBS    EQU   $01            Lo-byte: "DB7,DB6,DB5,DB4;DB3,DB2,
                             DB1,DB0"
*
* Main Program
*
        ORG   $C000          Start of user's RAM in EVB
INIT    LDS   #$CFFF         Top of C page RAM
*
* Initialize Port C Outputs
*
        LDAA  #$07           0,0,0,0;0,1,1,1
        STAA  DDRC           CLR/ ,CE/, and MSB-LSB/ are now enabled
                             as outputs
        LDAA  #$06           0,0,0,0;0,1,1,0
*                            CLR/-Hi, CE/-Hi, MSB-LSB/-Lo
        STAA  PORTC          Initialize Port C Outputs
*
* Call update subroutine
*
        BSR   UPDATE         Xfer 2 8-bit words to DAC-8562
        JMP   $E000          Restart BUFFALO
*
* Subroutine UPDATE
*
UPDATE  PSHX                 Save registers X, Y, and A
        PSHY
        PSHA
*
* Enter contents of the Hi-byte input register
*
        LDAA  #$0A           0,0,0,0;1,0,1,0
        STAA  MSBS           MSBS are set to 0A (Hex)
*
* Enter Contents of Lo-byte input register
*
        LDAA  #$AA           1,0,1,0;1,0,1,0
        STAA  LSBS           LSBS are set to AA (Hex)
*
        LDX   #MSBS          Stack pointer at 1st byte to send via Port B
        LDY   #$1000         Stack pointer at on-chip registers
*
* Clear DAC output to zero
*
        BCLR  PORTC,Y $04    Assert CLR/
        BSET  PORTC,Y $04    De-assert CLR/
*
* Loading input buffer latches
*
        BSET  PORTC,Y $01    Set hi-byte register load
TFRLP   LDAA  0,X            Get a byte to transfer via Port B
        STAA  PORTB          Write data to input register
        INX                  Increment counter to next byte for transfer
        CPX   #LSBS+1        Are we done yet ?
        BEQ   DUMP           If yes, update DAC output
        BCLR  PORTC,Y $01    Latch hi-byte register and set lo-byte register load
        BRA   TFRLP
*
```

DAC-8562–M68HC11 Interface Program Source Code (Continued)

```
* Update DAC output with contents of input registers
*
DUMP    BCLR  PORTC,Y $02    Assert CE/
        BSET  PORTC,Y $02    Latch DAC register
*
        PULA                 When done, restore registers X, Y & A
        PULY
        PULX
        RTS                  ** Return to Main Program **
```



Octal 8-Bit CMOS D/A Converter

DAC8800

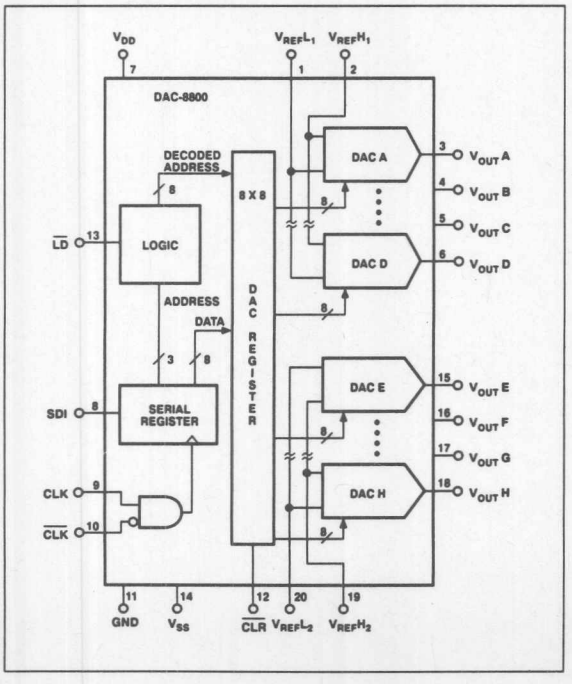
FEATURES

- ±1/2 LSB Total Unadjusted Error
- 2μs Settling Time
- Serial Data Input
- ±Full-Scale Output Set by $V_{REF}H$ and $V_{REF}L$
- Unipolar and Bipolar Operation
- TTL Input Compatible
- 20-Pin DIP or SOL Package
- Low Cost

APPLICATIONS

- Voltage Set Point Control
- Digital Offset & Gain Adjustment
- Microprocessor Controlled Calibration
- General Purpose Trimming Adjustments

FUNCTIONAL DIAGRAM



GENERAL DESCRIPTION

The DAC-8800 TrimDAC™ is designed to be a general purpose digitally controlled voltage adjustment device. The output voltage range can be independently set for each set of four D/A converters. In addition, both unipolar and bipolar output voltage ranges are easy to establish by external reference input high and low terminals. The digitally-programmed output voltages are ideal for op amp trimming, voltage-controlled amplifier gain setting and any general purpose trimming tasks.

A three-wire serial digital interface loads the contents of eight internal DAC registers which establish the output voltage levels. An asynchronous Clear ($\overline{CLR}$) input places all DACs in a zero code output condition, very handy for system power-up. An internal regulator provides TTL input compatibility over a wide range of V_{DD} supply voltages. Single supply operation is available by connecting V_{SS} to GND.

ORDERING INFORMATION †

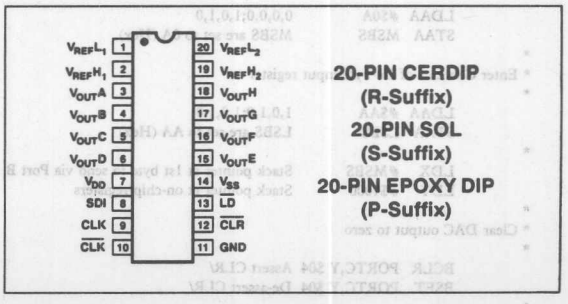
PACKAGE			
CERDIP 20-PIN	PLASTIC 20-PIN	SO 20-PIN	OPERATING TEMPERATURE RANGE
DAC8800BR*	–	–	–55°C to +125°C
DAC8800FR	DAC8800FP	DAC8800FS††	–40°C to +85°C

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages.

†† For availability and burn-in information on SO package, contact your local sales office.

PIN CONNECTIONS



20-PIN CERDIP (R-Suffix)

20-PIN SOL (S-Suffix)

20-PIN EPOXY DIP (P-Suffix)

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ELECTRICAL CHARACTERISTICS: (Note 1) Unless otherwise noted, SINGLE SUPPLY: V_{DD} = +12V, V_{SS} = 0V, $V_{REF}H$ = +5V, $V_{REF}L$ = 0V; or DUAL SUPPLY: V_{DD} = +12V, V_{SS} = –5V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = –2.5V; F GRADE: –40°C ≤ T_A ≤ +85°C; B GRADE: –55°C ≤ T_A ≤ +125°C.

PARAMETER	SYMBOL	CONDITIONS	DAC-8800 MIN	TYP	MAX	UNITS
STATIC ACCURACY	All specifications apply for DACs A, B, C, D, E, F, G, H					
Resolution	N		8	–	–	Bits
Total Unadjusted Error (Note 2)	TUE		–	–	±1/2	LSB
Differential Nonlinearity (Note 3)	DNL		–	–	±1	LSB
Full Scale Error	G_{FSE}		–	–	±1/2	LSB
Zero Code Error	V_{ZSE}		–	–	±1/2	LSB
DAC Output Resistance	R_{OUT}		8	12	16	kΩ
DAC Output Resistance Match	$\Delta R_{OUT}/R_{OUT}$		–	0.5	–	%
REFERENCE INPUT						
Voltage Range (Note 5)	$V_{REF}H$	Pins 2 & 19	$V_{REF}L$	–	(V_{DD} – 4)	V
	$V_{REF}L$	Pins 1 & 20	V_{SS}	–	$V_{REF}H$	
Input Resistance	$V_{REF}H$	Digital Inputs = 55_H	2	3	–	kΩ
Input Resistance Match	$\Delta R_{REF}H/R_{REF}H$	Digital Inputs = 55_H	–	0.5	–	%
Reference Input Capacitance (Note 4)	C_{REF}	Digital Inputs All Zeros	–	50	75	pF
		Digital Inputs All Ones	–	75	100	
DIGITAL INPUTS						
Logic High	V_{INH}		2.4	–	–	V
Logic Low	V_{INL}		–	–	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or +5V	–	–	±1	µA
Input Capacitance (Note 4)	C_{IN}		–	4	8	pF
Input Coding				BINARY		
POWER SUPPLIES (Note 6)						
Positive Supply Current	I_{DD}	Dual Supply TTL	–	1	2	mA
		Dual Supply CMOS	–	0.2	0.4	
Negative Supply Current	I_{SS}	Dual Supply	–	0.01	0.2	mA
Power Dissipation	P_{DISS}	Single Supply Operation	–	12	24	mW
		Dual Supply Operation	–	12	25	
DC Power Supply Rejection Ratio	PSRR	ΔV_{DD} =±5%	–	0.001	0.01	%/%
DYNAMIC PERFORMANCE (Note 4)						
V_{OUT} Settling Time	t_S	±1/2 LSB Error Band	–	0.8	2	µs
Channel-to-Channel Crosstalk (Note 7)	CT	Measured Between Adjacent DAC Outputs	–	80	–	nVs

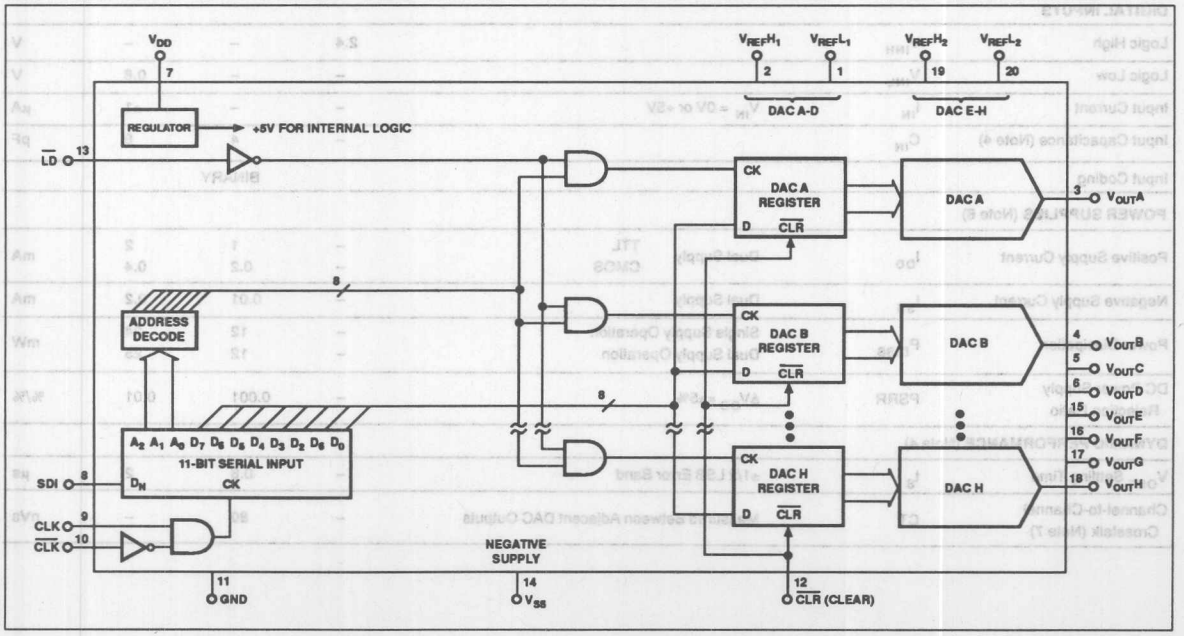
$-55°C \le T_A \le +125°C$. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8800 MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Notes 4, 8)						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock Level High or Low	60	–	–	ns
Data Setup Time	t_{DS}		30	–	–	ns
Data Hold Time	t_{DH}		30	–	–	ns
DAC Register Load Pulse Width	t_{LD}		50	–	–	ns
Clear Pulse Width	t_{CLR}		50	–	–	ns
Clock Edge to Load Time	t_{CKLD}		50	–	–	ns
Load Edge to Next Clock Edge Time	t_{LDCK}		50	–	–	ns

NOTES:

1. Testing performed in SINGLE SUPPLY mode, except I_{DD}, I_{SS}, and PSRR which are tested in DUAL SUPPLY mode.
2. Includes Full Scale Error, Relative Accuracy, and Zero Code Error.
3. All devices guaranteed monotonic over the full operating temperature range.
4. Guaranteed by design and not subject to production test.
5. V_{DD} – 4 volts is the maximum reference voltage for the above specifications. Also $V_{REF}H \ge V_{REF}L$.
6. Digital Input voltages $V_{IN} = V_{INL}$ or V_{INH} for TTL condition; V_{IN} = 0V or +5V for CMOS condition. DAC outputs unloaded. P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
7. Measured at V_{OUT} pin where an adjacent V_{OUT} pin is making a full-scale voltage change.
8. See timing diagram for location of measured values.

DETAILED DAC-8800 BLOCK DIAGRAM



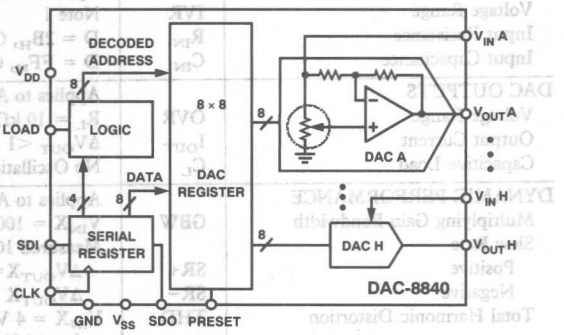
8-Bit, Octal, 4-Quadrant Multiplying, CMOS TrimDAC

DAC8840

FEATURES
Replaces 8 Potentiometers
1 MHz 4-Quadrant Multiplying Bandwidth
No Signal Inversion
Low Zero Output Error
Eight Individual Channels
3-Wire Serial Input
500 kHz Update Data Loading Rate
±3 Volt Output Swing
Midscale Preset, Zero Volts Out

APPLICATIONS
Automatic Adjustment
Trimmer Replacement
Dynamic Level Adjustment
Special Waveform Generation and Modulation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC-8840 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC® capability allows replacement of the mechanical trimmer function in new designs. The DAC-8840 is ideal for ac or dc gain control of up to 1 MHz bandwidth signals. The 4-quadrant multiplying capability is useful for signal inversion and modulation often found in video convergence circuitry.

Internally the DAC-8840 contains eight voltage output CMOS digital-to-analog converters, each with separate reference inputs. Each DAC has its own DAC register which holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register which is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in multiple DAC applications without additional external decoding logic.

TrimDAC is a registered trademark of Analog Devices, Inc.

The DAC-8840 consumes only 190 mW from ±5 V power supplies. For single 5 V supply applications consult the DAC-8841.

The DAC-8840 is available in 24-pin plastic DIP, cerdip, and SOIC-24 packages.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

DAC8840—SPECIFICATIONS (V_{DD} = +5 V, V_{SS} = −5 V, All $V_{IN}X$ = +3 V, T_A = −40°C to +85°C apply for DAC-8840F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY		All Specifications Apply for DACs A, B, C, D, E, F, G, H				
Resolution	N		8			Bits
Integral Nonlinearity	INL			±1/4	±1	LSB
Differential Nonlinearity	DNL	All Devices Monotonic			±1	LSB
Output Offset	V_{BZE}	$\overline{PR}$ = 0, Sets D = 80_H		3	25	mV
Output Offset Drift	TCV_{BZ}	$\overline{PR}$ = 0, Sets D = 80_H		10		µV/°C
REFERENCE INPUTS		Applies to All Inputs $V_{IN}X$				
Voltage Range	IVR	Note 1	±3			V
Input Resistance	R_{IN}	D = $2B_H$, Code Dependent	3	6		kΩ
Input Capacitance	C_{IN}	D = FF_H, Code Dependent		19	30	pF
DAC OUTPUTS		Applies to All Outputs $V_{OUT}X$				
Voltage Range	OVR	R_L = 10 kΩ	±3			V
Output Current	I_{OUT}	ΔV_{OUT} <1 LSB	±5	±10		mA
Capacitive Load	C_L	No Oscillation			200	pF
DYNAMIC PERFORMANCE		Applies to All DACs				
Multiplying Gain Bandwidth	GBW	$V_{IN}X$ = 100 mV p–p	1	2.5		MHz
Slew Rate		Measured 10% to 90%				
Positive	SR+	$\Delta V_{OUT}X$= +6 V	1.3	4.0		V/µs
Negative	SR−	$\Delta V_{OUT}X$ = −6 V	1.3	2.5		V/µs
Total Harmonic Distortion	THD	$V_{IN}X$ = 4 V p–p, D = FF_H, f = 1 kHz, f_{LP} = 80 kHz		0.01		%
Spot Noise Voltage	e_N	f = 1 kHz		0.17		µV/√Hz
Output Settling Time	t_S	±1 LSB Error Band, D = 0 to FF_H		3.5	6	µs
Channel-to-Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz	60	80		dB
Digital Feedthrough	Q	V_{INX} = 0 V, D = 0 to 255_{10}		6		nVs
POWER SUPPLIES						
Power Supply Current	I_{DD}	$\overline{PR}$ = 0 V		19	26	mA
Negative Supply Current	I_{SS}	$\overline{PR}$ = 0 V		19	26	mA
Power Dissipation	P_{DISS}			190	260	mW
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%		0.0002	0.01	%/%
Power Supply Range	PSR	V_{DD}, $\lvert V_{SS}\rvert$	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	µA
Input Capacitance	C_{IL}			7	10	pF
Input Coding				Offset Binary		
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = −0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V

NOTE
[1]Maximum input voltage is always 2 V less than V_{DD}.
Specifications subject to change without notice.

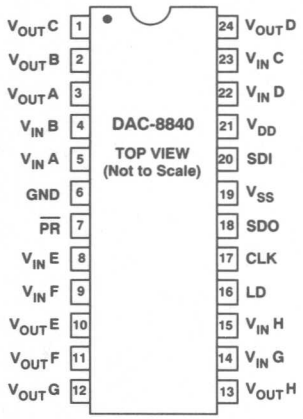
TIMING SPECIFICATIONS (V_{DD} = +5 V, V_{SS} = −5 V, All $V_{IN}X$ = +3 V, T_A = −40°C to +85°C apply for DAC-8840F, unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Clock Pulse Width	t_{CH}, t_{CL}	80		ns
Data Setup Time	t_{DS}	40		ns
Data Hold Time	t_{DH}	20		ns
CLK to SDO Propagation Delay	t_{PD}		120	ns
DAC Register Load Pulse Width	t_{LD}	70		ns
Preset Pulse Width	t_{PR}	50		ns
Clock Edge to Load Time	t_{CKLD}	30		ns
Load Edge to Next Clock Edge	t_{LDCK}	60		ns

PIN DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	$V_{OUT}C$	DAC C Output
2	$V_{OUT}B$	DAC B Output
3	$V_{OUT}A$	DAC A Output
4	$V_{IN}B$	DAC B Reference Input
5	$V_{IN}A$	DAC A Reference Input
6	GND	Ground
7	$\overline{PR}$	Preset Input, Active Low, All DAC Registers = 80_H
8	$V_{IN}E$	DAC E Reference Input
9	$V_{IN}F$	DAC F Reference Input
10	$V_{OUT}E$	DAC E Output
11	$V_{OUT}F$	DAC F Output
12	$V_{OUT}G$	DAC G Output
13	$V_{OUT}H$	DAC H Output
14	$V_{IN}G$	DAC G Reference Input
15	$V_{IN}H$	DAC H Reference Input
16	LD	Load DAC Register Strobe, Active High Input That Transfers the Data Bits from the Serial Input Register into the Decoded DAC Register. See Table I.
17	CLK	Serial Clock Input, Positive Edge Triggered
18	SDO	Serial Data Output, Active Totem Pole Output
19	V_{SS}	Negative 5 V Power Supply
20	SDI	Serial Data Input
21	V_{DD}	Positive 5 V Power Supply
22	$V_{IN}D$	DAC D Reference Input
23	$V_{IN}C$	DAC C Reference Input
24	$V_{OUT}D$	DAC D Output

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

V_{DD} to GND . . . . . −0.3, +7 V
V_{SS} to GND . . . . . +0.3, −7 V
$V_{IN}X$ to GND . . . . . V_{DD}, V_{SS}
$V_{OUT}X$ to GND . . . . . V_{DD}, V_{SS}
Short Circuit $I_{OUT}X$ to GND . . . . . Continuous
Digital Input & Output Voltage to GND . . . . . V_{DD}, V_{SS}
Operating Temperature Range
Extended Industrial: DAC8840F . . . . . −40°C to +85°C
Maximum Junction Temperature (T_J max) . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Package Power Dissipation . . . . . (T_J Max $-T_A$)/θ_{JA}
Thermal Resistance θ_{JA}
Cerdip . . . . . 64°C/W
P-DIP . . . . . 57°C/W
SOIC-24 . . . . . 70°C/W

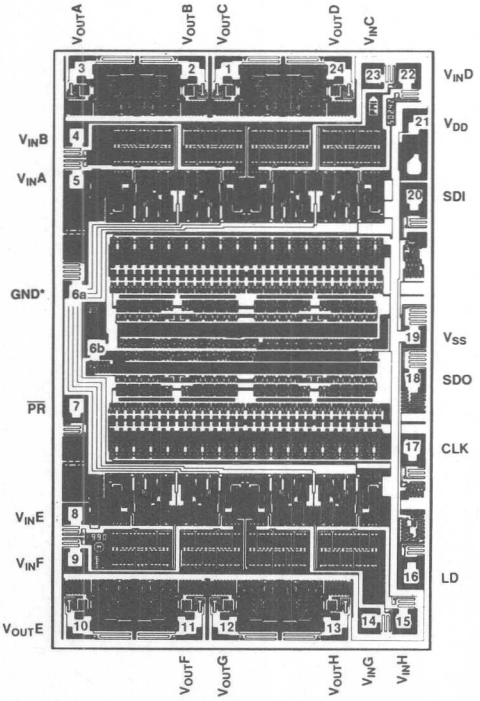
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
DAC8840FP	−40°C to +85°C	Plastic DIP	N-24
DAC8840FW	−40°C to +85°C	Cerdip	Q-24
DAC8840FS	−40°C to +85°C	SOL-24	R-24
DAC8840GBC	25°C	DICE	

*For outline information see Package Information section.

DICE CHARACTERISTICS

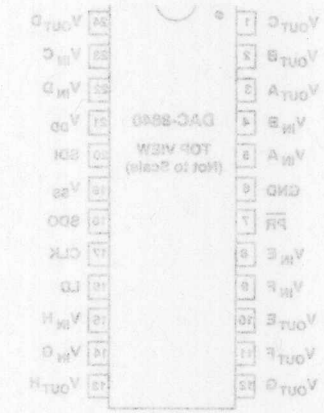
DIE SIZE 0.117 × 0.185 inch, 21,645 sq. mils
(2.9718 × 4.699 mm, 13.964 sq. mm)
The die backside is electrically common to V_{DD}.
The DAC8840 contains 3236 transistors.



*BOTH GND PADS (6a, 6b) ARE BONDED TO PIN 6 OF PACKAGE.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



PIN	MNEMONIC	DESCRIPTION
1	$V_{OUT}C$	DAC C Output
2	$V_{OUT}B$	DAC B Output
3	$V_{OUT}A$	DAC A Output
4	$V_{IN}B$	DAC B Reference Input
5	$V_{IN}A$	DAC A Reference Input
6	GND	Ground
7	$\overline{PR}$	Preset Input, Active Low. All DAC Registers = 80H
8	$V_{IN}E$	DAC E Reference Input
9	$V_{IN}F$	DAC F Reference Input
10	$V_{OUT}E$	DAC E Output
11	$V_{OUT}F$	DAC F Output
12	$V_{OUT}G$	DAC G Output
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17	CLK	Serial Clock Input. Positive Edge Triggered
18	SDO	Serial Data Output. Active Totem Pole Output
19	V_{SS}	Negative 5 V Power Supply
20	SDI	Serial Data Input
21	V_{DD}	Positive 5 V Power Supply
22	$V_{IN}D$	DAC D Reference Input
23	$V_{IN}C$	DAC C Reference Input
24	$V_{OUT}D$	DAC D Output

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

V_{DD} to GND ..... −0.3, +7 V
V_{SS} to GND ..... +0.3, −7 V
$V_{IN}X$ to GND ..... V_{DD}, V_{SS}
$V_{OUT}X$ to GND ..... V_{DD}, V_{SS}
Short Circuit $I_{OUT}X$ to GND ..... Continuous
Digital Input & Output Voltage to GND ..... V_{DD}, V_{SS}
Operating Temperature Range
Extended Industrial: DAC8840F ..... −40°C to +85°C
Maximum Junction Temperature (T_J max) ..... +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... (T_J Max − T_A)/θ_{JA}
Thermal Resistance θ_{JA}
Cerdip ..... 64°C/W
P-DIP ..... 57°C/W
SOIC-24 ..... 70°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
DAC8840FP	−40°C to +85°C	Plastic DIP	N-24
DAC8840FQ	−40°C to +85°C	Cerdip	Q-24
DAC8840FS	−40°C to +85°C	SOL-24	R-24
DAC8840GRC	25°C	DICE	

*For ordering information see Package Information section.

DICE CHARACTERISTICS

DIE SIZE 0.117 × 0.185 inch, 21,645 sq. mils
(2.9718 × 4.699 mm, 13.964 sq. mm)
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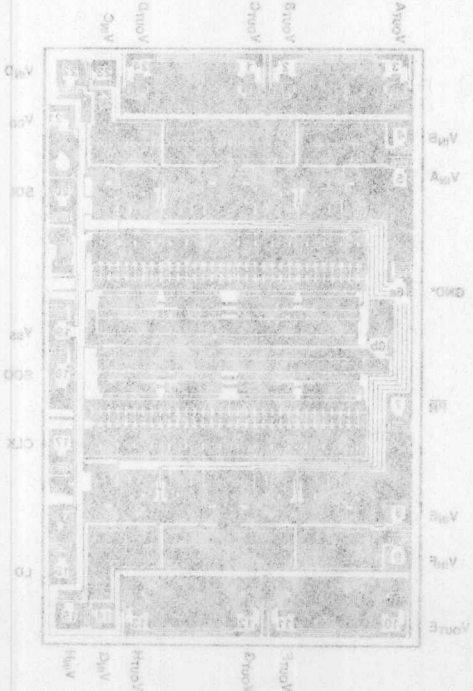

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

V/F and F/V Converters
Contents

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AD654 – Low Cost Monolithic Voltage-to-Frequency Converter	4–14

4

Selection Tree — V/F and F/V Converters

V/F AND F/V CONVERTERS

- AD537 (50 kHz)
- AD654 (500 kHz)
- AD650 (1 MHz)
- **Synchronous**
  - AD652 (2 MHz)

Selection Guides—V/F and F/V Converters

Voltage-to-Frequency Converters

Model	Full-Scale Frequency MHz	Linearity % max	FS Calib Error % typ	Output Format	Input Range V	Package Options[1]	Temp Ranges[2]	Page[3]	Comments
AD652	**2**	**0.005–0.05**	**0.25–0.5**	**Pulse Train**	**0 to 10, ±5 0 to −10**	**E, P, Q**	**C, I, M/**	**4–10**	**Synchronous, Multiple Input Ranges, Low Linearity, Single Supply**
AD650	**1**	**0.005–0.1**	**5–10**	**Pulse Train**	**0 to 10, ±5 0 to −10**	**D, N, P**	**C, I, M**	**4–7**	**Low Nonlinearity, Multiple Input Ranges**
AD654	**0.5**	**0.1–0.4**	**10**	**Square Wave**	**0 to (V_S)**	**N, R**	**C**	**4–14**	**Single Supply, Low Cost**
AD537	**0.15**	**0.07–0.25**	**5**	**Square Wave**	**$-V_S$ to ($+V_S$ −4)**	**D, H**	**C, M/**	**4–5**	**Single Supply, Military Grade**

Frequency-to-Voltage Converters

Model	Linearity Input Range kHz	Response Time % max	ms typ	Package Options[1]	Temp Ranges[2]	Page[3]	Comments
451	0 to 10	0.03–0.008	4	Module	I	D	Complete, No External Components
453	0 to 100	0.03–0.008	0.8	Module	I	D	Complete, No External Components
AD650	**0 to 1000**	**0.005–0.1**	**–**	**D, N, P**	**C, I, M/**	**4–14**	**Low Nonlinearity**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]D = Data Sheet. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Integrated Circuit Voltage-to-Frequency Converter

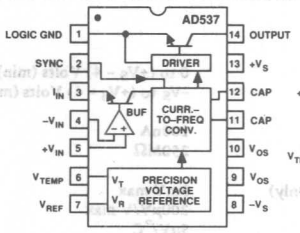
AD537*

FEATURES

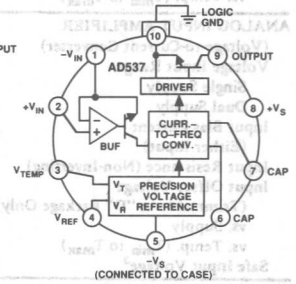
- Low Cost A-D Conversion
- Versatile Input Amplifier
  - Positive or Negative Voltage Modes
  - Negative Current Mode
  - High Input Impedance, Low Drift
- Single Supply, 5 to 36 Volts
- Linearity: ±0.05% FS
- Low Power: 1.2mA Quiescent Current
- Full Scale Frequency up to 100kHz
- 1.00 Volt Reference
- Thermometer Output (1mV/K)
- F-V Applications
- F-V Applications
- MIL-STD-883 Compliant Versions Available

PIN CONFIGURATIONS

"D" Package – TO-116



"H" Package – TO-100



PRODUCT DESCRIPTION

The AD537 is a monolithic V-F converter consisting of an input amplifier, a precision oscillator system, an accurate internal reference generator and a high current output stage. Only a single external RC network is required to set up any full scale (F.S.) frequency up to 100kHz and any F.S. input voltage up to ±30V. Linearity error is as low as ±0.05% for 10kHz F.S., and operation is guaranteed over an 80dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±30ppm/°C. The AD537 operates from a single supply of 5 to 36V and consumes only 1.2mA quiescent current.

A temperature-proportional output, scaled to 1.00mV/K, enables the circuit to be used as a reliable temperature-to-frequency converter; in combination with the fixed reference output of 1.00V, offset scales such as 0°C or 0°F can be generated.

The low drift (1μV/°C typ) input amplifier allows operation directly from small signals (e.g., thermocouples or strain gages) while offering a high (250MΩ) input resistance. Unlike most V-F converters, the AD537 provides a square-wave output, and can drive up to 12 TTL loads, LEDs, very long cables, etc.

The excellent temperature characteristics and long-term stability of the AD537 are guaranteed by the primary band-gap reference generator and the low T.C. silicon chromium thin film resistors used throughout.

The device is available in either a TO-116 ceramic DIP or a TO-100 metal can; both are hermetically sealed packages.

The AD537 is available in three performance/temperature grades; the J and K grades are specified for operation over the 0 to +70°C range while the AD537S is specified for operation over the extended temperature range, −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD537 is a complete V-F converter requiring only an external RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full-scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, f = V/10RC.
2. The power supply requirements are minimal, only 1.2mA quiescent current is drawn from a single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to ($+V_S$ - 4) volts. Negative inputs can easily be connected for below ground operation.
3. F-V converters with excellent characteristic are also easy to build by connecting the AD537 in a phase-locked loop. Application particulars are shown in Figure 6.
4. The versatile open-collector NPN output stage can sink up to 20mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.
5. The AD537 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Product Databook or current AD537/883B data sheet for detailed specifications.

*Protected by Patent Nos. 3,887,963 and RE 30,586.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD537—SPECIFICATIONS (typical @ +25°C with V_S (total) = 5 to 36V, unless otherwise noted.)

MODEL	AD537JH	AD537JD	AD537KD AD537KH	AD537SD[1] AD537SH[1]
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0 to 150kHz	•	•	•
Nonlinearity[1]				
f_{max} = 10kHz	0.15% max (0.1% typ)	•	0.07% max	••
f_{max} = 100kHz	0.25% max (0.15% typ)	•	0.1% max	••
Full Scale Calibration Error				
C = 0.01μF, I_{IN} = 1.000mA	±10% max	±7% max	±5% max	••
vs. Supply (f_{max} < 100kHz)	±0.1%/V max (0.01% typ)	•	•	•
vs. Temp. (T_{min} to T_{max})	±150ppm/°C max (50ppm typ)	•	50ppm/°C max (30ppm typ)[2]	250ppm/°C max
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0 to (+V_S – 4) Volts (min)	•	•	•
Dual Supply	–V_S to (+V_S – 4) Volts (min)	•	•	•
Input Bias Current				
(Either Input)	100nA	•	•	•
Input Resistance (Non-Inverting)	250MΩ	•	•	•
Input Offset Voltage				
(Trimmable in "D" Package Only)	5mV max	•	2mV max	••
vs. Supply	200μV/V max	100μV/V max	100μV/V max	••
vs. Temp. (T_{min} to T_{max})	5μV/°C	•	1μV/°C	10μV/°C max
Safe Input Voltage[3]	±V_S	•	•	•
REFERENCE OUTPUTS				
Voltage Reference				
Absolute Value	1.00 Volt ±5% max	•	•	•
vs. Temp. (T_{min} to T_{max})	50ppm/°C	•	100ppm/°C max	••
vs. Supply	±0.03%/V max	•	•	•
Output Resistance[4]	380Ω	•	•	•
Absolute Temperature Reference[5]				
Nominal Output Level	1.00mV/K	•	•	•
Initial Calibration @ +25°C	298mV (±5mV)	•	298mV (±5mV max)	••
Slope Error from 1.00mV/K	±0.02mV/K	•	•	•
Slope Nonlinearity	±0.1K	•	•	•
Output Resistance[5]	900Ω	•	•	•
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"				
V_{OUT} = 0.4V max, T_{min} to T_{max})	20mA min	20mA min	20mA min	10mA min
Output Leakage Current in Logic "1"				
(T_{min} to T_{max})	200nA max	•	•	2μA max
Logic Common Level Range	–V_S to (+V_S – 4) Volts	•	•	•
Rise/Fall Times (C_T = 0.01μF)				
I_{IN} = 1mA	0.2μs	•	•	•
I_{IN} = 1μA	1μs	•	•	•
POWER SUPPLY				
Voltage, Rated Performance				
Single Supply	4.5V to 36V	•	•	•
Dual Supply	±5 to ±18V	•	•	•
Quiescent Current	1.2mA (2.5mA max)	•	•	•
TEMPERATURE RANGE				
Rated Performance	0 to +70°C	•	•	–55°C to +125°C
Storage	–65°C to +150°C	•	•	•
PACKAGE OPTIONS[6,7]				
TO-116 Ceramic DIP (D-14)		AD537JD	AD537KD	AD537SD
TO-100 Header (H-10A)	AD537JH		AD537KH	AD537SH

NOTES

*Specifications same as AD537JH.

**Specifications same as AD537K.

Specifications subject to change without notice.

[1] Nonlinearity is specified for a current input level (I_{IN}) to the converter from 0.1 to 1000μA. Converter has 100% overrange capability up to I_{IN} = 2000μA with slightly reduced linearity. Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

[2] Guaranteed not tested.

[3] Maximum voltage input level is equal to the supply on either input terminal. However, large negative voltage levels can be applied to the negative terminal if the input is scaled to a nominal 1mA full scale through an appropriate value resistor (see Figure 2).

[4] Loading the 1.0 volt or 1mV/K outputs can cause a significant change in overall circuit performance, as indicated in the applications section. To maintain normal operation, these outputs should be operated into the external buffer or an external amplifier.

[5] Temperature reference output performance is specified from 0 to +70°C for "J" and "K" devices, –55°C to +125°C for "S" model.

[6] D = Ceramic DIP; H = Hermetic Metal Can. For outline information see Package Information section.

[7] For AD537/883B specifications, refer to Analog Devices Military Products Databook.

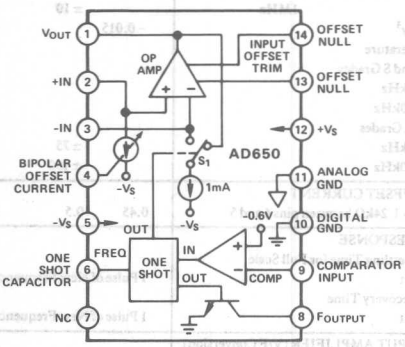
Voltage-to-Frequency and Frequency-to-Voltage Converter

AD650

FEATURES

- V/F Conversion to 1MHz
- Reliable Monolithic Construction
- Very Low Nonlinearity
  - 0.002% typ at 10kHz
  - 0.005% typ at 100kHz
  - 0.07% typ at 1MHz
- Input Offset Trimmable to Zero
- CMOS or TTL Compatible
- Unipolar, Bipolar, or Differential V/F
- V/F or F/V Conversion
- Available in Surface Mount
- MIL-STD-883-Compliant Versions Available

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD650 V/F/V (voltage-to-frequency or frequency-to-voltage converter) provides a combination of high frequency operation and low nonlinearity previously unavailable in monolithic form. The inherent monotonicity of the V/F transfer function makes the AD650 useful as a high-resolution analog-to-digital converter. A flexible input configuration allows a wide variety of input voltage and current formats to be used, and an open-collector output with separate digital ground allows simple interfacing to either standard logic families or opto-couplers.

The linearity error of the AD650 is typically 20ppm (0.002% of full scale) and 50ppm (0.005%) maximum at 10kHz full scale. This corresponds to approximately 14-bit linearity in an analog-to-digital converter circuit. Higher full-scale frequencies or longer count intervals can be used for higher resolution conversions. The AD650 has a useful dynamic range of six decades allowing extremely high resolution measurements. Even at 1MHz full scale, linearity is guaranteed less than 1000ppm (0.1%) on the AD650KN, KP, BD and SD grades.

In addition to analog-to-digital conversion, the AD650 can be used in isolated analog signal transmission applications, phased-locked-loop circuits, and precision stepper motor speed controllers. In the F/V mode, the AD650 can be used in precision tachometer and FM demodulator circuits.

The input signal range and full-scale output frequency are user-programmable with two external capacitors and one resistor. Input offset voltage can be trimmed to zero with an external potentiometer.

The AD650JN and AD650KN are offered in a plastic 14-pin DIP package. The AD650JP and AD650KP are available in a 20-pin plastic leaded chip carrier (PLCC). Both plastic packaged versions of the AD650 are specified for the commerical (0 to +70°C) temperature range. For industrial temperature range (−25°C to +85°C) applications, the AD650AD and AD650BD are offered in a ceramic package. The AD650SD is specified for the full −55°C to +125°C extended temperature range.

PRODUCT HIGHLIGHTS

1. In addition to very high linearity, the AD650 can operate at full scale output frequency up to 1MHz. The combination of these two features makes the AD650 an inexpensive solution for applications requiring high resolution monotonic A/D conversion.
2. The AD650 has a very versatile architecture that can be configured to accommodate bipolar, unipolar, or differential input voltages, or unipolar input currents.
3. TTL or CMOS compatibility is achieved using an open collector frequency output. The pullup resistor can be connected to voltages up to +30V, or +15V or +5V for conventional CMOS or TTL logic levels.
4. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the AD650.
5. The AD650 provides separate analog and digital grounds. This feature allows prevention of ground loops in real-world applications.
6. The AD650 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD650/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD650—SPECIFICATIONS (@ +25°C with V_S = ±15V unless otherwise noted)

Model	AD650J/AD650A Min	Typ	Max	AD650K/AD650B Min	Typ	Max	AD650S Min	Typ	Max	Units
DYNAMIC PERFORMANCE										
Full Scale Frequency Range			1			1			1	MHz
Nonlinearity[1] f_{max} = 10kHz		0.002	0.005		0.002	0.005		0.002	0.005	%
100kHz		0.005	**0.02**		0.005	**0.02**		0.005	**0.02**	%
500kHz		0.02	0.05		0.02	0.05		0.02	0.05	%
1MHz		0.1			0.05	**0.1**		0.05	**0.1**	%
Full Scale Calibration Error[2], 100kHz		±5			±5			±5		%
1MHz		±10			±10			±5		%
vs. Supply[3]	−0.015		**+0.015**	−0.015		**+0.015**	−0.015		**+0.015**	% of FSR/V
vs. Temperature										
A, B, and S Grades										
at 10kHz			±75			±75			±75	ppm/°C
at 100kHz			±150			±150			±150	ppm/°C
J and K Grades										
at 10kHz		±75			±75					ppm/°C
at 100kHz		±150			±150					ppm/°C
BIPOLAR OFFSET CURRENT										
Activated by 1.24kΩ between pins 4 and 5	0.45	0.5	0.55	0.45	0.5	0.55	0.45	0.5	0.55	mA
DYNAMIC RESPONSE										
Maximum Settling Time for Full Scale Step Input	1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			
Overload Recovery Time Step Input	1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			
ANALOG INPUT AMPLIFIER (V/F Conversion)										
Current Input Range (Figure 1)	0		+0.6	0		+0.6	0		+0.6	mA
Voltage Input Range (Figure 5)	−10		0	−10		0	−10		0	V
Differential Impedance		2MΩ‖10pF			2MΩ‖10pF			2MΩ‖10pF		
Common Mode Impedance		1000MΩ‖10pF			1000MΩ‖10pF			1000MΩ‖10pF		
Input Bias Current										
Noninverting Input		40	**100**		40	**100**		40	**100**	nA
Inverting Input		±8	±20		±8	±20		±8	±20	nA
Input Offset Voltage (Trimmable to Zero)			±4			±4			±4	mV
vs. Temperature (T_{min} to T_{max})		±30				±30			±30	µV/°C
Safe Input Voltage		$\pm V_S$			$\pm V_S$			$\pm V_S$		C
COMPARATOR (F/V Conversion)										
Logic "0" Level	$-V_S$		−1	$-V_S$		−1	$-V_S$		+1	V
Logic "1" Level	0		$+V_S$	0		$+V_S$	0		$+V_S$	V
Pulse Width Range[4]	0.1		$(0.3 \times t_{OS})$	0.1		$(0.3 \times t_{OS})$	0.1		$(0.3 \times t_{OS})$	µs
Input Impedance		250			250			250		kΩ
OPEN COLLECTOR OUTPUT (V/F Conversion)										
Output Voltage in Logic "0" $I_{SINK} \leq 8mA$, T_{min} to T_{max}			0.4			0.4			0.4	V
Output Leakage Current in Logic "1"			**100**			**100**			**100**	nA
Voltage Range[5]	0		+36	0		+36	0		+36	V
AMPLIFIER OUTPUT (F/V Conversion)										
Voltage Range (1500Ω min load resistance)	0		+10	0		+10	0		+10	V
Source Current (750Ω max load resistance)	10			10			10			mA
Capacitive Load (Without Oscillation)			100			100			100	pF
POWER SUPPLY										
Voltage, Rated Performance	±9		±18	±9		±18	±9		±18	V
Quiescent Current			8			8			8	mA
TEMPERATURE RANGE										
Rated Performance – N Package	0		+70	0		+70				°C
D Package	−25		+85	−25		+85	−55		+125	°C
Storage – N Package	−25		+85	−25		+85				°C
D Package	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTIONS[6]										
PLCC (P-20A)		AD650JP			AD650KP					
Plastic DIP (N-14)		AD650JN			AD650KN					
Ceramic DIP (D-14)		AD650AD			AD650BD			AD650SD		

NOTES

[1]Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a fraction of full scale.

[2]Full scale calibration error adjustable to zero.

[3]Measured at full scale output frequency of 100kHz.

[4]Refer to F/V conversion section of the text.

[5]Referred to digital ground.

[6]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Unipolar Operation

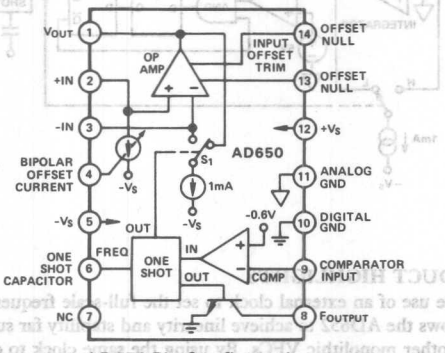
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Storage Temperature Ceramic . . . . . −55°C to +165°C
Plastic . . . . . −25°C to +125°C
Differential Input Voltage (Pins 2 & 3) . . . . . ±10V
Maximum Input Voltage . . . . . $\pm V_S$
Open Collector Output Voltage Above Digital GND . . 36V
Current 50mA
Amplifier Short Ckt to Ground . . . . . Indefinite
Comparator Input Voltage (Pin 9) . . . . . $\pm V_S$

ORDERING GUIDE

Model[1]	Gain Tempco ppm/°C 100kHz	1MHz Linearity	Specified Temperature Range °C	Package
AD650JN	150 typ	0.1% typ	0 to +70	Plastic DIP
AD650KN	150 typ	0.1% max	0 to +70	Plastic DIP
AD650JP	150 typ	0.1% typ	0 to +70	PLCC
AD650KP	150 typ	0.1% max	0 to +70	PLCC
AD650AD	150 max	0.1% typ	−25 to +85	Ceramic
AD650BD	150 max	0.1% max	−25 to +85	Ceramic
AD650SD	150 max	0.1% max	−55 to +125	Ceramic

NOTE
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD650/883B data sheet.



AD650 Pin Configuration

CIRCUIT OPERATION

UNIPOLAR CONFIGURATION

The AD650 is a *charge balance* voltage-to-frequency converter. In the connection diagram shown in Figure 1, or the block diagram of Figure 2a, the input signal is converted into an equivalent current by the input resistance R_{IN}. This current is *exactly* balanced by an internal feedback current delivered in short, timed bursts from the switched 1mA internal current source. These bursts of current may be thought of as precisely defined packets of charge. The required number of charge packets, each producing one pulse of the output transistor, depends upon the amplitude of the input signal. Since the number of charge packets delivered per unit time is dependent on the input signal amplitude, a linear voltage-to-frequency transformation will be accomplished. The frequency output is furnished via an open collector transistor.

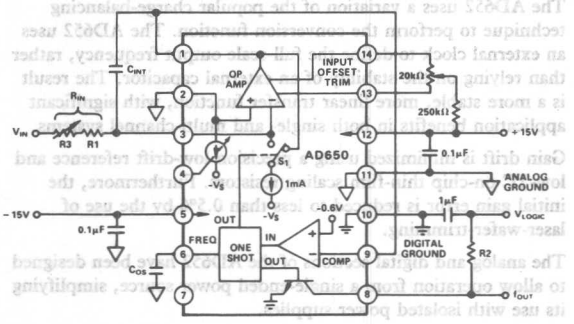


Figure 1. Connection Diagram for V/F Conversion, Positive Input Voltage

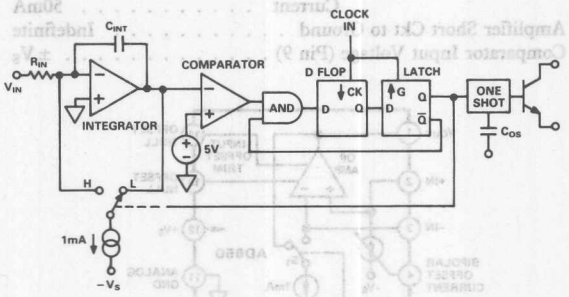
Voltage-to-Frequency Converter

AD652

FEATURES

- Full-Scale Frequency (Up to 2MHz) Set by External System Clock
- Extremely Low Linearity Error (0.005% max at 1MHz FS, 0.02% max at 2MHz FS)
- No Critical External Components Required
- Accurate 5V Reference Voltage
- Low Drift (25ppm/°C max)
- Dual or Single Supply Operation
- Voltage or Current Input
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD652 Synchronous Voltage-to-Frequency Converter (SVFC) is a powerful building block for precision analog-to-digital conversion, offering typical nonlinearity of 0.002% (0.005% maximum) at a 100kHz output frequency. The inherent monotonicity of the transfer function and wide range of clock frequencies allows the conversion time and resolution to be optimized for specific applications.

The AD652 uses a variation of the popular charge-balancing technique to perform the conversion function. The AD652 uses an external clock to define the full-scale output frequency, rather than relying on the stability of an external capacitor. The result is a more stable, more linear transfer function, with significant application benefits in both single- and multi-channel systems.

Gain drift is minimized using a precision low-drift reference and low-TC on-chip thin-film scaling resistors. Furthermore, the initial gain error is reduced to less than 0.5% by the use of laser-wafer-trimming.

The analog and digital sections of the AD652 have been designed to allow operation from a single-ended power source, simplifying its use with isolated power supplies.

The AD652 is available in five performance grades. The 20-pin PLCC packaged JP and KP grades are specified for operation over the 0 to +70°C commercial temperature range. The 16-pin cerdip-packaged AQ and BQ grades are specified for operation over the −40°C to +85°C industrial temperature range, and the AD652SQ is available for operation over the full −55°C to +125°C extended temperature range.

PRODUCT HIGHLIGHTS

1. The use of an external clock to set the full-scale frequency allows the AD652 to achieve linearity and stability far superior to other monolithic VFCs. By using the same clock to drive the AD652 and (through a suitable divider) also set the counting period, conversion accuracy is maintained independent of variations in clock frequency.
2. The AD652 Synchronous VFC requires only a single external component (a noncritical integrator capacitor) for operation.
3. The AD652 includes a buffered, accurate 5V reference which is available to the user.
4. The clock input of the AD652 is TTL and CMOS compatible and can also be driven by sources referred to the negative power supply. The flexible open-collector output stage provides sufficient current sinking capability for TTL and CMOS logic, as well as for optical couplers and pulse transformers. A capacitor-programmable one-shot is provided for selection of optimum output pulse width for power reduction.
5. The AD652 can also be configured for use as a synchronous F/V converter for isolated analog signal transmission.
6. The AD652 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD652/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (typical @ T_A = +25°C, V_S = ±15V, unless otherwise noted)

Parameter	AD652JP/AQ/SQ Min	AD652JP/AQ/SQ Typ	AD652JP/AQ/SQ Max	AD652KP/BQ Min	AD652KP/BQ Typ	AD652KP/BQ Max	Units
VOLTAGE-TO-FREQUENCY MODE							
Gain Error							
f_{CLOCK} = 200kHz		±0.5	±1		±0.25	±0.5	%
f_{CLOCK} = 1MHz		±0.5	**±1**		±0.25	**±0.5**	%
f_{CLOCK} = 4MHz		±0.5	**±1.5**		±0.25	**±0.75**	%
Gain Temperature Coefficient							
f_{CLOCK} = 200kHz		±25	±50		±15	±25	ppm/°C
f_{CLOCK} = 1MHz		±25	**±50**		±15	**±25**	ppm/°C
		±10	**±50**		±10	**±30**	ppm/°C[1]
f_{CLOCK} = 4MHz		±25	**±75**		±15	**±50**	ppm/°C
Power Supply Rejection Ratio		0.001	**0.01**		0.001	**0.01**	%/V
Linearity Error							
f_{CLOCK} = 200kHz		±0.002	±0.02		±0.002	±0.005	%
f_{CLOCK} = 1MHz		±0.002	**±0.02**		±0.002	**±0.005**	%
f_{CLOCK} = 2MHz		±0.01	±0.02		±0.002	±0.005	%
f_{CLOCK} = 4MHz		±0.02	**±0.05**		±0.01	**±0.02**	%
Offset (Transfer Function, RTI)		±1	**±3**		±1	**±2**	mV
Offset Temperature Coefficient		±10	**±50**		±10	**±25**	µV/°C
Response Time	One Period of New Output Frequency Plus One Clock Period.						
FREQUENCY-TO-VOLTAGE MODE							
Gain Error							
f_{IN} = 100kHz FS		±0.5	±1		±0.25	±0.5	%
Linearity Error							
f_{IN} = 100kHz FS		±0.002	±0.02		±0.002	±0.01	%
INPUT RESISTORS							
Cerdip (Figure 1a.) (0 to +10V FS Range)	19.8	20	20.2	19.8	20	20.2	kΩ
PLCC (Figure 1b.)							
Pin 8 to Pin 7	9.9	10	10.1	9.9	10	10.1	kΩ
Pin 7 to Pin 5 (0 to +5V FS Range)	9.9	10	10.1	9.9	10	10.1	kΩ
Pin 8 to Pin 5 (0 to +10V FS Range)	19.8	20	20.2	19.8	20	20.2	kΩ
Pin 9 to Pin 5 (0 to +8V FS Range)	15.8	16	16.2	15.8	16	16.2	kΩ
Pin 10 to Pin 5 (Auxiliary Input)	19.8	20	20.2	19.8	20	20.2	kΩ
Temperature Coefficient (All)		±50	**±100**		±50	**±100**	ppm/°C
INTEGRATOR OP AMP							
Input Bias Current							
Inverting Input (Pin 5)		±5	**±20**		±5	**±20**	nA
Noninverting Input (Pin 6)		20	**50**		20	**50**	nA
Input Offset Current		20	**70**		20	**70**	nA
Input Offset Current Drift		1	3		1	2	nA/°C
Input Offset Voltage		±1	**±3**		±1	**±2**	mV
Input Offset Voltage Drift		±10	±25		±10	±15	µV/°C
Open Loop Gain		86			86		dB
Common-Mode Input Range	$-V_S+5$		$+V_S-5$	$-V_S+5$		$+V_S-5$	V
CMRR	80			80			dB
Bandwidth	14	95		14	95		MHz
Output Voltage Range (Referred to Pin 6, R_1 >= 5k)	−1		$(+V_S-4)$	−1		$(+V_S-4)$	V
COMPARATOR							
Input Bias Current		0.5	5		0.5	5	µA
Common-Mode Voltage	$-V_S+4$		$+V_S-4$	$-V_S+4$		$+V_S-4$	V
CLOCK INPUT							
Maximum Frequency	4	5		4	5		MHz
Threshold Voltage (Referred to Pin 12)		1.2			1.2		V
T_{min}-T_{max}	0.8		2.0	0.8		2.0	V
Input Current							
$(-V_S<V_{CLK}<+V_S)$		5	**20**		5	**20**	µA
Voltage Range	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Rise Time			2			2	µs

4

Parameter	AD652JP/AQ/SQ Min	AD652JP/AQ/SQ Typ	AD652JP/AQ/SQ Max	AD652KP/BQ Min	AD652KP/BQ Typ	AD652KP/BQ Max	Units
OUTPUT STAGE							
V_{OL} (I_{OUT} = 10mA)			**0.4**			**0.4**	V
I_{OL}							
V_{OL}<0.8V			**15**			**15**	mA
V_{OL}<0.4V, T_{min}-T_{max}			**8**			**8**	mA
I_{OH} (Off Leakage)		0.01	**10**		0.01	**10**	µA
Delay Time, Positive Clock Edge to Output Pulse	**150**	200	**250**	**150**	200	**250**	ns
Fall Time (Load = 500pF and I_{SINK} = 5mA)		100			100		ns
Output Capacitance		5			5		pF
OUTPUT ONE-SHOT							
Pulse Width							
C_{OS} = 300pF	**1**	1.5	**2**	**1**	1.5	**2**	µs
C_{OS} = 1000pF	**4**	5	**6**	**4**	5	**6**	µs
REFERENCE OUTPUT							
Voltage	**4.950**	5.0	**5.050**	**4.975**	5.0	**5.025**	V
Drift			**100**			**50**	ppm/°C
Output Current							
Source	**10**			**10**			mA
Sink	**100**	500		**100**	500		µA
Power Supply Rejection (Supply Range = ± 12.5V to ± 17.5V)			0.015			0.015	%/V
Output Impedance (Sourcing Current)		0.3	**2**		0.3	**2**	Ω
POWER SUPPLY							
Rated Voltage		± 15			± 15		V
Operating Range							
Dual Supplies	± 6	± 15	± 18	± 6	± 15	± 18	V
Single Supply ($-V_S$ = 0)	+ 12		+ 36	+ 12		+ 36	V
Quiescent Current		± 11	**± 15**		± 11	**± 15**	mA
Digital Common	$-V_S$		$+V_S-4$	$-V_S$		$+V_S-4$	V
Analog Common	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
TEMPERATURE RANGE							
Specified Performance							
JP, KP Grade	0		+ 70	0		+ 70	°C
AQ, BQ Grade	− 40		+ 85	− 40		+ 85	°C
SQ Grade	− 55		+ 125				°C

NOTES
[1]Referred to internal V_{REF}. In PLCC package, tested on 10V input range only.
Specifications in **boldface** are 100% tested at final test and are used to measure outgoing quality levels.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Maximum Input Voltage (Figure 6) 36V
Maximum Output Current (Open Collector Output) . . 50mA
Amplifier Short Circuit to Ground . . . . . Indefinite
Storage Temperature Range: Cerdip . . . . −65°C to +150°C
PLCC . . . . −65°C to +150°C

DEFINITIONS OF SPECIFICATIONS

GAIN ERROR – The gain of a voltage-to-frequency converter is that scale factor setting that provides the nominal conversion relationship, e.g. 1MHz full scale. The "gain error" is the difference in slope between the actual and ideal transfer functions for the V-F converter.

LINEARITY ERROR – The "linearity error" of a V-F is the deviation of the actual transfer function from a straight line passing through the endpoints of the transfer function.

GAIN TEMPERATURE COEFFICIENT – The gain temperature coefficient is the rate of change in full-scale frequency as a function of the temperature from +25°C to T_{min} or T_{max}.

ORDERING GUIDE

Part Number[1]	Gain Drift ppm/°C 100 kHz	1 MHz Linearity %	Specified Temperature Range °C	Package Options[2]
AD652JP	50 max	0.02 max	0 to +70	PLCC (P-20A)
AD652KP	25 max	0.005 max	0 to +70	PLCC (P-20A)
AD652AQ	50 max	0.02 max	−40 to +85	Cerdip (Q-16)
AD652BQ	25 max	0.005 max	−40 to +85	Cerdip (Q-16)
AD652SQ	50 max	0.02 max	−55 to +125	Cerdip (Q-16)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD652/883 data sheet.
[2]P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

PIN CONFIGURATIONS

PIN	"Q" CERDIP	"P" PLCC
1	$+V_S$	NC
2	TRIM	$+V_S$
3	TRIM	NC
4	OP AMP OUT	OP AMP OUT
5	OP AMP "−"	OP AMP "−"
6	OP AMP "+"	OP AMP "+"
7	10 VOLT INPUT	5 VOLT INPUT
8	$-V_S$	10 VOLT INPUT
9	C_{OS}	8 VOLT INPUT
10	CLOCK INPUT	OPTIONAL 10V INPUT
11	FREQ OUT	$-V_S$
12	DIGITAL GND	C_{OS}
13	ANALOG GND	CLOCK INPUT
14	COMP "−"	FREQ OUT
15	COMP "+"	DIGITAL GROUND
16	COMP REF	ANALOG GND
17		COMP "−"
18		COMP "+"
19		NC
20		COMP REF

4

THEORY OF OPERATION

A synchronous VFC is similar to other voltage-to-frequency converters in that an integrator is used to perform a charge-balance of the input signal with an internal reference current. However, rather than using a one-shot as the primary timing element which requires a high quality and low drift capacitor, a synchronous voltage-to-frequency converter (SVFC) uses an external clock; this allows the designer to determine the system stability and drift based upon the external clock selected. A crystal oscillator may also be used if desired.

The SVFC architecture provides other system advantages besides low drift. If the output frequency is measured by counting pulses gated to a signal which is derived from the clock, the clock stability is unimportant and the device simply performs as a voltage controlled frequency divider, producing a high resolution A/D. If a large number of inputs must be monitored simultaneously in a system, the controlled timing relationship between the frequency output pulses and the user supplied clock greatly simplifies this signal acquisition. Also, if the clock signal is provided by a VFC, then the output frequency of the SVFC will be proportional to the product of the two input voltages. Hence, multiplication and A-to-D conversion on two signals are performed simultaneously.

The pinouts of the AD652 SVFC are shown in Figure 1.

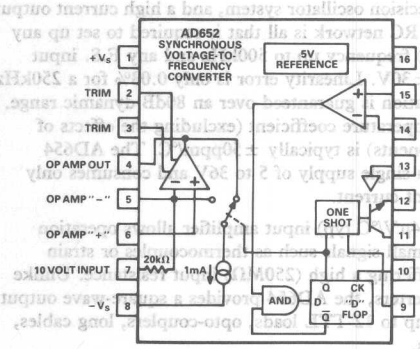


Figure 1a. AD652 Cerdip Pin Configuration

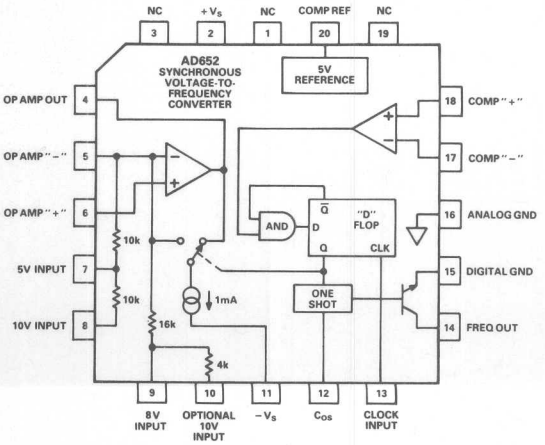
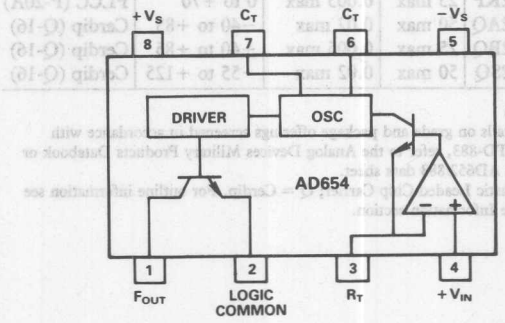


Figure 1b. AD652 PLCC Pin Configuration

FEATURES

- **Low Cost**
- **Single or Dual Supply, 5 to 36 Volts, ±5V to ±18V**
- **Full Scale Frequency Up to 500kHz**
- **Minimum Number of External Components Needed**
- **Versatile Input Amplifier**
  - **Positive or Negative Voltage Modes**
  - **Negative Current Mode**
  - **High Input Impedance, Low Drift**
- **Low Power: 2.0mA Quiescent Current**
- **Low Offset: 1mV**

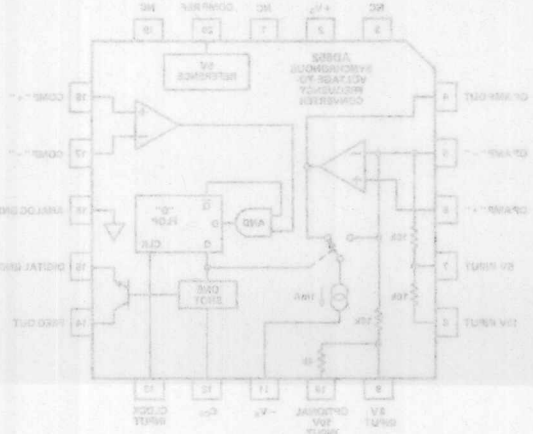
FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD654 is a monolithic V/F converter consisting of an input amplifier, a precision oscillator system, and a high current output stage. A single RC network is all that is required to set up any full scale (F.S.) frequency up to 500kHz and any F.S. input voltage up to ±30V. Linearity error is only 0.03% for a 250kHz F.S., and operation is guaranteed over an 80dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±50ppm/°C. The AD654 operates from a single supply of 5 to 36V and consumes only 2.0mA quiescent current.

The low drift (4μV/°C typ) input amplifier allows operation directly from small signals such as thermocouples or strain gauges while offering a high (250MΩ) input resistance. Unlike most V/F converters, the AD654 provides a square-wave output, and can drive up to 12 TTL loads, opto-couplers, long cables, or similar loads.



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. Packaged in both an 8-pin mini-DIP and an 8-pin SOIC package, the AD654 is a complete V/F converter requiring only an RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of the timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, $f = V/10RC$.
2. A minimum number of low cost external components are necessary. A single RC network is all that is required to set up any full scale frequency up to 500kHz and any full scale input voltage up to ±30V.
3. Plastic packaging allows low cost implementation of the standard VFC applications: A/D conversion, isolated signal transmission, F/V conversion, phase-locked loops, and tuning switched-capacitor filters.
4. Power supply requirements are minimal; only 2.0mA of quiescent current is drawn from the single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to $(+V_S - 4)$ volts. Negative inputs can easily be connected for below ground operation.
5. The versatile open-collector output stage can sink more than 10mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.

SPECIFICATIONS (T_A = +25°C and V_S (total) = 5 to 16.5V, unless otherwise noted. All testing done @ V_S = +5V).

Model	AD654JN/JR Min	Typ	Max	Units
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0		500	kHz
Nonlinearity[1]				
f_{max} = 250kHz		0.06	**0.1**	%
f_{max} = 500kHz		0.20	0.4	%
Full Scale Calibration Error				
C = 390pF, I_{IN} = 1.000mA	**−10**		**10**	%
vs. Supply ($f_{max} \leq$ 250kHz)				
V_S = +4.75 to +5.25V		0.20	**0.40**	%/V
V_S = +5.25 to +16.5V		0.05	**0.10**	%/V
vs. Temp (0 to 70°C)		50		ppm/°C
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0		(+V_S −4)	V
Dual Supply	−V_S		(+V_S −4)	V
Input Bias Current				
(Either Input)		30	**50**	nA
Input Offset Current		5		nA
Input Resistance (Non-Inverting)		250		MΩ
Input Offset Voltage		0.5	**1.0**	mV
vs. Supply				
V_S = +4.75 to +5.25V		0.1	**0.25**	mV/V
V_S = +5.25 to +16.5V		0.03	**0.1**	mV/V
vs. Temp (0 to 70°C)		4		µV/°C
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"[2]				
V_{OUT} = 0.4V max, 25°C	**10**	20		mA
V_{OUT} = 0.4V max, 0 to 70°C	5	10		mA
Output Leakage Current in Logic "1"		10	**100**	nA
0 to 70°C		50	500	nA
Logic Common Level Range	−V_S		(+V_S −4)	V
Rise/Fall Times (C_T = 0.01µF)				
I_{IN} = 1mA		0.2		µs
I_{IN} = 1µA		1		µs
POWER SUPPLY				
Voltage, Rated Performance	4.5		16.5	V
Voltage, Operating Range				
Single Supply	4.5		36	V
Dual Supply	±5		±18	V
Quiescent Current				
V_S (Total) = 5V		1.5	2.5	mA
V_S (Total) = 30V		2.0	3.0	mA
TEMPERATURE RANGE				
Operating Range	−40		85	°C
PACKAGE OPTIONS[3]				
SOIC (R-8)		AD654JR		
Plastic DIP (N-8)		AD654JN		

NOTES

[1]At f_{max} = 250kHz; R_T = 1kΩ, C_T = 390pF, I_{IN} = 0-1mA.
f_{max} = 500kHz; R_T = 1kΩ, C_T = 200pF, I_{IN} = 0-1mA.

[2]The sink current is the amount of current that can flow into Pin 1 of the AD654 while maintaining a maximum voltage of 0.4V between Pin 1 and Logic Common.

[3]N = Plastic DIP; R = SOIC. For outline information see Package Information section.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Maximum Input Voltage
(Pins 3, 4) to $-V_S$ . . . . . $-300mV$ to $+V_S$
Maximum Output Current
Instantaneous 50mA
Sustained 25mA
Logic Common to $-V_S$ . . . . . $-500mV$ to $(+V_S - 4)$
Storage Temperature Range . . . . . $-65°C$ to $+150°C$

CIRCUIT OPERATION

The AD654's block diagram appears in Figure 1. A versatile operational amplifier serves as the input stage; its purpose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full scale input voltage, a 1mA drive current is delivered to the current-to-frequency converter (an astable multivibrator). The drive current provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 100nA to 2mA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a level other than $-V_S$.

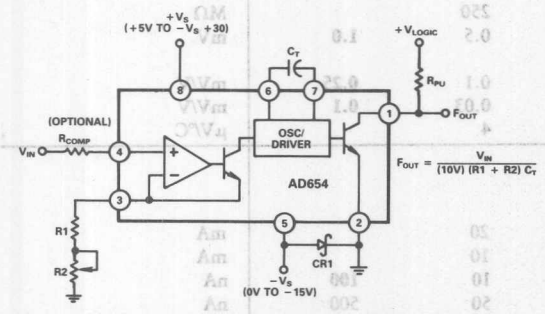


Figure 1. Standard V-F Connection for Positive Input Voltages

V/F CONNECTION FOR POSITIVE INPUT VOLTAGES

In the connection scheme of Figure 1, the input amplifier presents a very high (250MΩ) impedance to the input voltage, which is converted into the proper drive current by the scaling resistors at pin 3. Resistors R1 and R2 are selected to provide a 1mA full scale current with enough trim range to accommodate the AD654's 10% FS error and the components' tolerances. Full scale currents other than 1mA can be chosen, but linearity will be reduced; 2mA is the maximum allowable drive. The AD654's positive input voltage range spans from $-V_S$ (ground in single supply operation) to four volts below the positive supply. Power supply rejection degrades as the input exceeds $(+V_S - 3.75V)$ and at $(+V_S - 3.5V)$ the output frequency goes to zero.

As indicated by the scaling relationship in Figure 1, a 0.01μF timing capacitor will give a 10kHz full scale frequency, and 0.001μF will give 100kHz with a 1mA drive current. Good V/F linearity requires the use of a capacitor with low dielectric absorption (DA), while the most stable operation over temperature calls for a component having a small tempco. Polystyrene, polypropylene, or Teflon* capacitors are preferred for tempco and dielectric absorption; other types will degrade linearity. The capacitor should be wired very close to the AD654. In Figure 1, Schottky diode CR1 (MBD101) prevents logic common from dropping more than 500mV below $-V_S$. This diode is not required if $-V_S$ is equal to logic common.

V/F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

The AD654 can accommodate a wide range of negative input voltages with proper selection of the scaling resistor, as indicated in Figure 2. This connection, unlike the buffered positive connection, is not high impedance because the signal source must supply the 1mA F.S. drive current. However, large negative voltages beyond the supply can be handled easily by modifying the scaling resistors appropriately. If the input is a true current source, R1 and R2 are not used. Again, diode CR1 prevents latch-up by insuring Logic Common does not drop more than 500mV below $-V_S$. The clamp diode (MBD101) protects the AD654 input from "below $-V_S$" inputs.

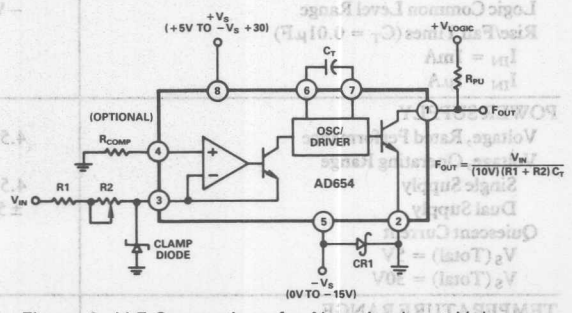


Figure 2. V-F Connections for Negative Input Voltages or Current

*Teflon is a trademark of E. I. Du Pont de Nemours & Co.

Data Acquisition Subsystems
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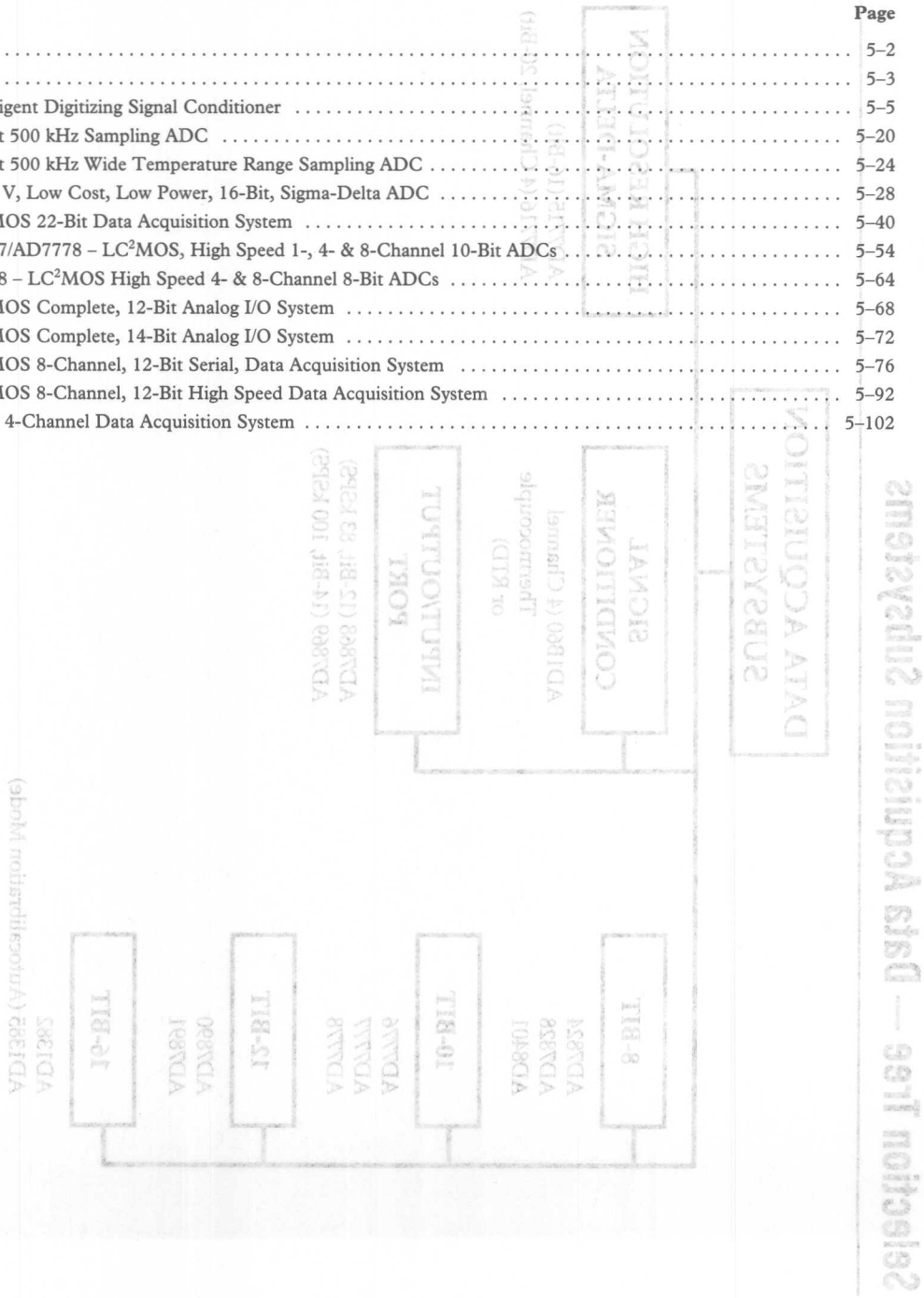
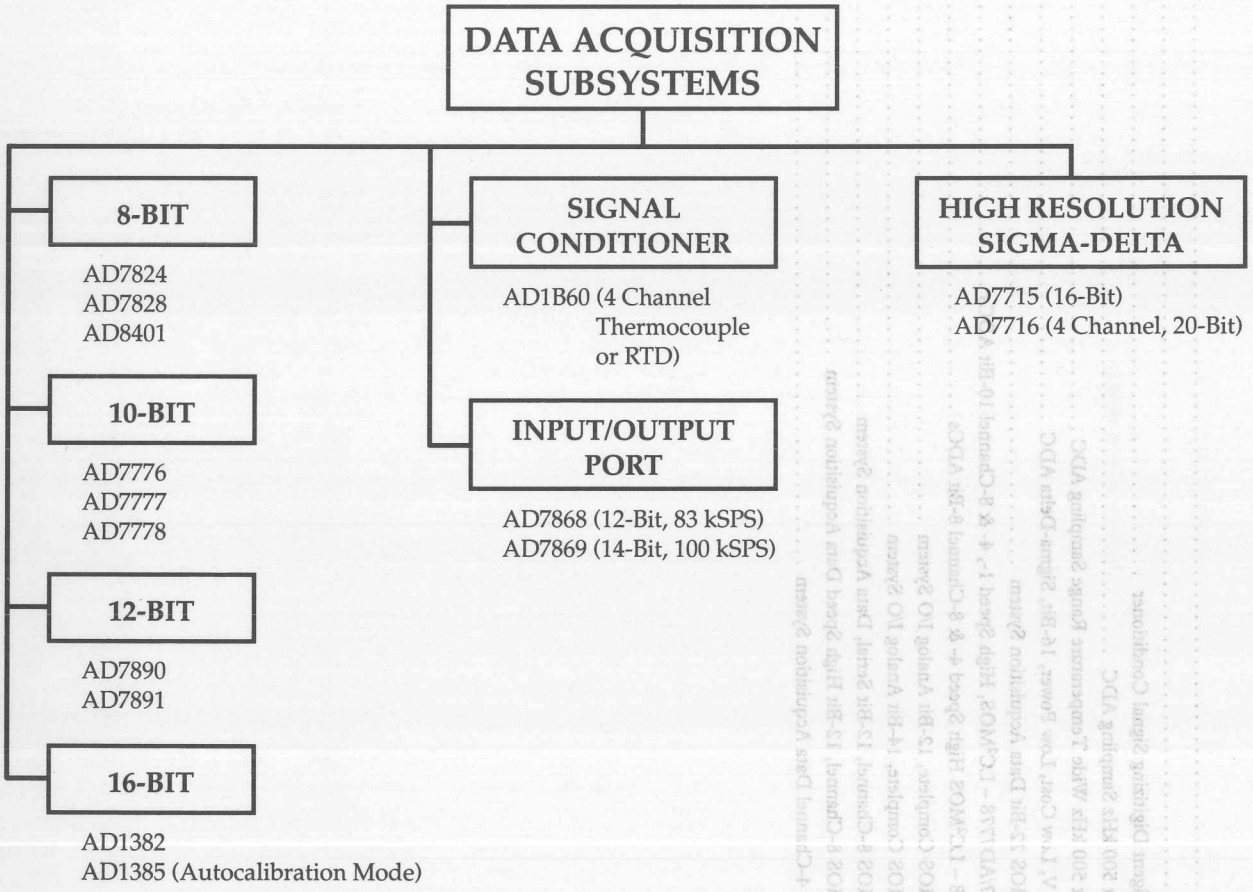


Selection Tree — Data Acquisition Subsystems



Selection Guide—Data Acquisition Subsystems

Model	Resolution Bits	Throughput Rate kHz	No. Channels	Bus Interface	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
AD7716	**22**	**0.30**	**4**	**Serial**	**P, S**	**I**	**Quad 22-Bit Sigma-Delta ADC, Low Power**	**5–40**
AD1382	**16**	**500**	**1**	**8, µP**	**D**	**C**	**High Speed Sampling ADC**	**5–20**
AD1385	**16**	**500**	**1**	**8, µP**	**D**	**C, M**	**Autocalibrated, Wide Temp Sampling ADC**	**5–24**
AD7715	**16**	**20–200 Hz**	**1**	**Serial, µP**	**N, R**	**I**	**Sigma-Delta ADC, PGA Gain 1–128, 3 V or 5 V Supply**	**5–28**
AD1B60	**16**	**100 Hz**	**4**	**Serial, µP**	**J, S**	**I**	**Complete Sensor-to-Digital Conditioning and Conversion**	**5–5**
AD7869	**14**	**83**	**1**	**Serial, µP**	**N, Q, R**	**C, I**	**Complete Analog I/O with DAC**	**5–72**
AD7891	**12**	**600**	**8**	**8/12, Serial, µP**	**P, S**	**I**	**5 V Supply, CMOS, High Speed**	**5–92**
AD1341	12	150	16/8	16	Z	C, M/	Complete, Programmable DAS with Fast Bus Interface	CII 7–5
AD7890	**12**	**100**	**8**	**Serial**	**N, Q, R**	**I, M**	**5 V Supply, CMOS, Sampling ADC**	**5–76**
AD7868	**12**	**83**	**1**	**Serial, µP**	**N, Q, R**	**I**	**Complete Analog I/O with DAC**	**5–68**
AD363R	12	25	16/8	12	D	C, M	16-Channel 12-Bit DAS	CII 7–5
AD364R	12	20	16/8	12	D	C, M	High Speed 16-Channel 12-Bit DAS	CII 7–5
AD7850	12	10	1	Serial	N, P	C	Small Signal DAS with Instrumentation Amplifiers and Reference	D
AD7776	**10**	**400**	**1**	**10, µP**	**R**	**I**	**Single Supply, CMOS, Offset Reference**	**5–54**
AD7777	**10**	**400**	**4**	**10, µP**	**N, R**	**I**	**Single Supply, CMOS, Dual Sampling**	**5–54**
AD7778	**10**	**400**	**8**	**10, µP**	**S**	**I**	**Single Supply, CMOS, Dual Sampling**	**5–54**
AD8401	**8**	**500**	**4**	**8, µP**	**R**	**I**	**5 V Complete I/O Subsystem with DAC**	**5–102**
AD7824	**8**	**400**	**4**	**8, µP**	**N, Q, R**	**C, I, M**	**CMOS, 4-Channel Sampling ADC**	**5–64**
AD7828	**8**	**400**	**8**	**8, µP**	**E, N, P, Q**	**C, I, M**	**CMOS, 8-Channel Sampling ADC**	**5–64**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]CII = *Data Converter Reference Manual, Volume II*; D = Data Sheet. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Selection Guide — Data Acquisition Subsystems

Model	Resolution Bits	Throughput Rate kHz	No. Channels	Bus Interface	Package Options[1]	Features[2]	Temp Ranges[3]	Comments	Page[4]
ADT7IS	22	0.30	4	Serial	P, S	1	C	Quad 22-Bit Sigma-Delta ADC, Low Power	5–40
ADL7382	16	500	1		D		C	High Speed Sampling ADC	5–20
ADL7385	16	500	1		D		C, M	Anti-aliasfiltered, Wide Temp Sampling ADC	5–24
ADL7715	16	20–200 kHz	1	Serial, µP	N, R	1		Sigma-Delta ADC, RCA Qwik 1-ICB, 3 V or 5 V Supply	5–28
ADL7840	16	100 kHz	4	Serial, µP	J, S	1		Complete Sensor-to-Digital Conditioning and Conversion	5–5
ADL7890	14	83	1	Serial, µP	N, Q, R	C, I		Complete Analog I/O with DAC	5–72
ADL7901	12	660	8	8/12, Serial, µP	P, S	1		5 V Supply, CMOS, High Speed	5–92
ADL7941	12	150	16/8		2	C, M/		Complete, Programmable DAS with Fast Bus Interface	CI17-5
ADL7960	12	100	8	Serial	N, Q, R	I, M		5 V Supply, CMOS, Sampling ADC	5–76
ADL7988	12	83	1	Serial, µP	N, Q, R	I		Complete Analog I/O with DAC	5–68
ADS8XR	12	21	16/8	12	D	C, M		16-Channel 12-Bit DAS	CI17-5
ADS8XR	12	20	16/8	12	D	C, M		High Speed 16-Channel 12-Bit DAS	CI17-5
ADT850	12	10	1	Serial	N, P	C		Small Signal DAS with Instrumentation Amplifiers and Reference	D
ADT7I6	16	400	1	10, µP	R	1		Single Supply, CMOS, Offset Reference	5–54
ADT7I7	16	400	4	10, µP	N, R	1		Single Supply, CMOS, Dual Sampling	5–54
ADT7I8	16	400	8	10, µP		1		Single Supply, CMOS, Dual Sampling	5–54
ADP801	8	500	4	8, µP	R	1		5 V Complete NO Subsystem with DAC	5–102
ADT854	8	400	4	8, µP	N, Q, R	C, I, M		CMOS, 4-Channel Sampling ADC	5–54
ADT858	8	400	8	8, µP	E, N, P, Q	C, I, M		CMOS, 8-Channel Sampling ADC	5–54

"Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; P = Ceramic Plastic; Q = Ceramic Flat Pack; Army; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; N = Hermetic Metal Can DIP; P = Plastic or Epoxy Sealed DIP; R = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-99—Thin Small Outline Package; W = Monochromatic Ceramic Side "SB" Package; Z = Ceramic Leaded Chip Carrier.

"Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, –40°C to +85°C (Some older products –25°C to +70°C); M = Military, –55°C to +125°C. If a device has military grade dice, the M designation designates Military Temperature Range Reference Element. Versions with be followed by: / to indicate 883B, per JAN, or for space level.

"CI = Data Conversion Reference, Volume II; D = Data Sheet. All other entries refer to this volume.

Boldface Types: Data about innovation in blue modules.

Intelligent Digitizing Signal Conditioner

AD1B60

FEATURES

- Complete Sensor-to-Digital Signal Conditioning and Data Conversion
- Multiple Input Ranges
  Thermocouples: J, K, T, E, R, S, and B
  RTDs: 100 Ω Platinum (α = 385 and 392)
  Voltage: Ten Ranges from ±10 mV to ±10 V
  Two Custom Ranges (User Defined)
- High Resolution: ±0.15°C (Typical, Temperature Input) or ±0.0015% (Typical, Voltage Input)
- High Accuracy: ±0.2°C (Typical, RTD Input) or ±0.005% (Typical, Voltage Input)
- Cold Junction Compensation for Thermocouples
- Open Thermocouple Detection
- RTD Excitation
- Lead Resistance Compensation for RTDs
- Autozeroing, Data Scaling, and Linearization
- Data Output in Engineering Units
- 2-Wire Asynchronous Communication I/O Port
- High Speed Synchronous Data Output Port
- Eight Integration Times: 2 ms to 200 ms
- Internal EEPROM Stores Calibration and Configuration Parameters

APPLICATIONS

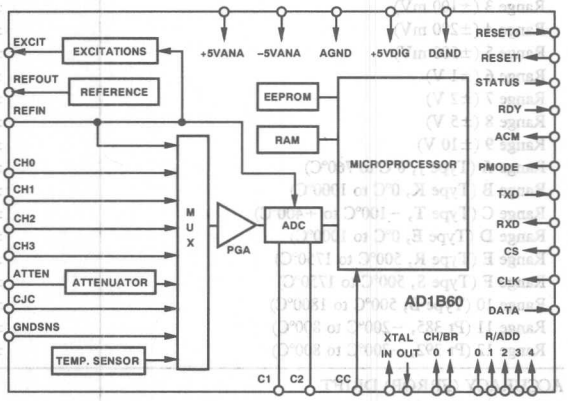
Industrial Temperature Measurement Systems
Process Control Systems
Multichannel Thermocouple/RTD Systems
Analytical Instruments

GENERAL DESCRIPTION

The AD1B60 is an intelligent, microcontroller-based device that performs signal conditioning, excitation, compensation, linearization, and analog-to-digital conversion for a variety of low bandwidth industrial and analytical signals. Due to its highly integrated, mixed-signal design, the AD1B60 is small and inexpensive, offering designers increased flexibility and performance.

The AD1B60 is suited primarily for use with thermocouples and resistance temperature detectors (RTDs), but also accepts a broad range of low and high level voltage inputs. The AD1B60 converts sensor inputs to compensated, linearized, scaled, and autozeroed outputs represented in engineering units: degrees Celsius or volts.

FUNCTIONAL BLOCK DIAGRAM



Four modes of cold junction compensation (CJC) are supported for thermocouple applications. The AD1B60 also provides lead resistance compensation for 3-wire or 4-wire RTD connections.

Data is transmitted serially to simplify use of external optical and/or magnetic isolation devices. The AD1B60 has a bidirectional asynchronous communications port for control and for data output. Data is also available via a high-speed synchronous data output port.

Configuration parameters such as the input range and integration time of the AD1B60 can be programmed, both prior to installation and in the application. The AD1B60 incorporates EEPROM to store default and user-specified configuration and calibration values. No battery backups, potentiometers, or user-developed calibration software routines are required and no recalibration is necessary when the input range is changed.

AD1B60—SPECIFICATIONS (@ T_A = −25°C to +85°C and power supplies of ±5 V ± 5% unless otherwise noted)

Parameter	AD1B60BS, AD1B60BJ Min	Typ	Max	Unit	Notes
ACCURACY (ERROR)					
Range 0 (±10 mV)		±0.06	±0.11	% FSR	Notes 1 and 2 (All Ranges); at +25°C
Range 1 (±20 mV)		±0.03	±0.06	% FSR	
Range 2 (±50 mV)		±0.015	±0.03	% FSR	
Range 3 (±100 mV)		±0.008	±0.015	% FSR	
Range 4 (±200 mV)		±0.005	±0.008	% FSR	
Range 5 (±500 mV)		±0.005	±0.007	% FSR	
Range 6 (±1 V)		±0.005	±0.007	% FSR	
Range 7 (±2 V)		±0.005	±0.007	% FSR	
Range 8 (±5 V)		±0.007	±0.010	% FSR	
Range 9 (±10 V)		±0.005	±0.010	% FSR	
Range A (Type J, 0°C to 760°C)		±0.25	±0.45	°C	Note 3 (Temperature Ranges)
Range B (Type K, 0°C to 1000°C)		±0.55	±0.75	°C	
Range C (Type T, −100°C to +400°C)		±0.25	±0.45	°C	
Range D (Type E, 0°C to 1000°C)		±0.20	±0.35	°C	
Range E (Type R, 500°C to 1750°C)		±1.00	±1.75	°C	
Range F (Type S, 500°C to 1750°C)		±1.15	±2.05	°C	
Range 10 (Type B, 500°C to 1800°C)		±1.15	±2.15	°C	
Range 11 (Pt 385, −200°C to 800°C)		±0.20	±0.40	°C	
Range 12 (Pt 392, −200°C to 800°C)		±0.20	±0.40	°C	
ACCURACY (ERROR) DRIFT					
Range 0 (±10 mV)		−40	−100	ppm/°C	Notes 4 and 5 (All Ranges)
Range 1 (±20 mV)		−20		ppm/°C	
Range 2 (±50 mV)		−10		ppm/°C	
Range 3 (±100 mV)		−5		ppm/°C	
Range 4 (±200 mV)		−5		ppm/°C	
Range 5 (±500 mV)		−5		ppm/°C	
Range 6 (±1 V)		−5		ppm/°C	
Range 7 (±2 V)		−5		ppm/°C	
Range 8 (±5 V)		−5		ppm/°C	
Range 9 (±10 V)		−5		ppm/°C	
Range A (Type J, 0°C to 760°C)		−10		ppm/°C	
Range B (Type K, 0°C to 1000°C)		−10		ppm/°C	
Range C (Type T, −100°C to +400°C)		−20		ppm/°C	
Range D (Type E, 0°C to 1000°C)		−10		ppm/°C	
Range E (Type R, 500°C to 1750°C)		−20		ppm/°C	
Range F (Type S, 500°C to 1750°C)		−40		ppm/°C	
Range 10 (Type B, 500°C to 1800°C)		−40		ppm/°C	
Range 11 (Pt 385, −200°C to 800°C)		±10	±25	ppm/°C	Note 6 (RTD Ranges)
Range 12 (Pt 392, −200°C to 800°C)		±10	±25	ppm/°C	
RESOLUTION					
Range 0 (±10 mV)		±0.035		% FSR	Notes 2 and 5 (All Ranges)
Range 1 (±20 mV)		±0.02		% FSR	
Range 2 (±50 mV)		±0.01		% FSR	
Range 3 (±100 mV)		±0.004		% FSR	
Range 4 (±200 mV)		±0.002		% FSR	
Range 5 (±500 mV)		±0.0015		% FSR	
Range 6 (±1 V)		±0.0015		% FSR	
Range 7 (±2 V)		±0.0015		% FSR	
Range 8 (±5 V)		±0.0015		% FSR	
Range 9 (±10 V)		±0.0015		% FSR	
Range A (Type J, 0°C to 760°C)		±0.15		°C	
Range B (Type K, 0°C to 1000°C)		±0.2		°C	
Range C (Type T, −100°C to +400°C)		±0.15		°C	
Range D (Type E, 0°C to 1000°C)		±0.1		°C	
Range E (Type R, 500°C to 1750°C)		±0.55		°C	
Range F (Type S, 500°C to 1750°C)		±0.6		°C	
Range 10 (Type B, 500°C to 1800°C)		±0.7		°C	
Range 11 (Pt 385, −200°C to +800°C)		±0.15		°C	
Range 12 (Pt 392, −200°C to +800°C)		±0.15		°C	

Parameter	AD1B60BS, AD1B60BJ Min	Typ	Max	Unit	Notes
INPUT CHARACTERISTICS					
Normal Mode Rejection (@ 50 Hz or 60 Hz)		66		dB	At Integration Time ≥ 100 ms
		50		dB	Note 2
Input Bias Current		−0.5	−3	nA	At T_A = +25°C
		−0.5		nA	At −25°C ≤ T_A ≤ +85°C
Input Impedance					
Channel 0-3		10		MΩ	
Attenuator Input	35	50	65	kΩ	
RTD & THERMOCOUPLE CHANNELS					
RTD Excitation Current Output (EXCIT)	−150	−200	−250	μA	Note 7; at T_A = +25°C
vs. Temperature		±75	±300	ppm/°C	Note 6
Open Thermocouple Detection Current (EXCIT)		−10		nA	
CJC Excitation Current Output (CJC)	−15	−20	−25	μA	Note 8; at T_A = +25°C
REFERENCE					
Internal Reference Output Voltage	2.360	2.500	2.640	V	
vs. Temperature		±25	±50	ppm/°C	
Internal Reference Voltage Noise		0.01		% p-p	
Ref In Current		350		μA	
TIMING					
Conversion Throughput Rate	2.5		100	conv/sec	Note 9
Integration Time (User Configurable)	2		200	ms	See Table IV
Integration Capacitor	1	2.2	3	nF	Note 10
Oscillator Frequency		11.0592		MHz	Notes 10 and 11
Integration Latency			100	μs	See Figure 2B
CLK-to-DATA Delay, Synchronous Port		30		ns	See Figure 4
Minimum CS High Time	400			μs	See Figure 4
Reset Input Pulse Width (RESETI)	5			μs	
DIGITAL LEVELS					At +25°C
Inputs					
Logic 0 Voltage			0.8	V	
Logic 1 Voltage (Except RESETI)	2.0			V	
Logic 1 Voltage (RESETI)	0.7* (+5VDIG) + 0.1			V	
Outputs					
Logic 0 Voltage (I_{SINK} = 1.6 mA)			0.45	V	
Logic 1 Voltage (I_{SOURCE} = −60 μA)	2.4			V	
Input Current (CC, RXD, CH/BR0-1, ACM, PMODE)					
Logic 0			−75	μA	At V_{IN} = 0.45 V
Logic 1-to-0 Transition			−750	μA	At V_{IN} = 2.0 V
Input Current (R/ADD0-4, CLK, CS)			±10	μA	At 0.45 ≤ V_{In} ≤ +5VDIG
Input Pulldown Resistor (RESETI)	50		150	kΩ	
POWER REQUIREMENTS					At +25°C
+V Analog (+5VANA)	4.75	5.00	5.25	V	
		7	15	mA	At +5VANA = 5.0 V
−V Analog (−5VANA)	−5.25	−5.00	−4.75	V	
		−7	−15	mA	At −5VANA = −5.0 V
+V Digital (+5VDIG)	4.75	5.00	5.25	V	Note 12
		10	30	mA	At +5VDIG = 5.0 V
Power Supply Rejection Ratio		−70		dB	
BROWNOUT DETECTOR					
±V Analog Threshold		±3.9		V	
+V Digital Threshold		3.5		V	
TEMPERATURE RANGE					
Rated Performance	−25		+85	°C	
Operating	−40		+85	°C	
Storage	−40		+85	°C	

5

AD1B60—SPECIFICATIONS

NOTES

[1]Accuracy specifications include factory calibration errors but do not include reference noise. Also, accuracy specifications for thermocouple ranges do not include CJC calculation errors, which depend on the calculation method chosen. To calculate total measurement error, add reference noise expressed as a percentage of the reference voltage to the specified accuracy error. Because reference noise results in a gain error, its effect is a percentage of reading. For example, a measurement made using the ±1 V input range and a reference with ±0.01% maximum noise would have a maximum error of ±0.007% FSR ± 0.01% of reading. FSR = Full-Scale Range, i.e., span of input values. For thermocouple ranges, also add to the measurement error the values in Table A corresponding to the selected CJC type. For example, a measurement made with a Type J thermocouple, downloaded CJC temperature, and a reference with ±0.01% maximum noise would have a maximum error of ±0.456 °C ± 0.01 % of reading.

[2]At integration time ≥ 33.3 ms and equal to an integral number of power-line cycles.

[3]Temperature ranges use the International Practical Temperature Scale of 1968 (IPTS-68). Thermocouple accuracy specifies conformance to NIST Monograph 125. RTD accuracy specifies conformance to JIS C 1604, DIN 43760, and IEC 751.

[4]Errors expressed as ppm (parts per million) of reading.

[5]Excluding reference noise and drift.

[6]RTD measurement drift is digitally compensated to 25 ppm/°C of reading (maximum), including effects of reference, excitation current, and gain drift.

[7]RTD measurement accuracy is digitally compensated to values shown on first page of specification table.

[8]CJC excitation current is enabled only when the "Thermistor" CJC mode is selected; see Table V.

[9]Minimum throughput occurs at T_{INT} = 200 ms for any range selection. Maximum throughput occurs at T_{INT} = 2 ms for voltage ranges (ranges 0 through 9) only; see Table IV.

[10]User-supplied.

[11]Specified performance obtained with frequency of 11.0592 MHz ± 0.1%.

[12]−0.2 V < (+5VANA − +5VDIG) < 0.5 V for specified performance.

[13]Typical values are not tested or guaranteed. Operation which is specified without explicit reference to variation in operating conditions may differ as these conditions are altered.

Table A. Maximum Thermocouple CJC Calculation Error

CJC Calculation	Thermistor		1 mV/K		Downloaded	Disabled
CJC Mode	00		01		10	11
Thermocouple Type	Ambient Temperature of AD1B60					
	−25°C to +85°C	25°C	−25°C to +85°C	25°C	−25°C to +85°C	−25°C to +85°C
J	0.6°C	0.1°C	0.4°C	0.3°C	0.006°C	0°C
K	0.6°C	0.1°C	0.4°C	0.3°C	0.012°C	0°C
T	0.8°C	0.2°C	0.6°C	0.4°C	0.028°C	0°C
E	0.6°C	0.1°C	0.4°C	0.3°C	0.024°C	0°C
R	0.4°C	0.1°C	0.3°C	0.2°C	0.007°C	0°C
S	0.4°C	0.1°C	0.3°C	0.2°C	0.007°C	0°C
B	0.3°C	0.3°C	0.3°C	0.3°C	0.250°C	0°C

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

+5VDIG to DGND	−0.3 V to +6 V
+5VANA to AGND	−0.3 V to +6 V
−5VANA to AGND	−6 V to +0.3 V
+5VDIG to +5VANA	−6 V to +0.3 V
+5VANA to −5VANA	0 V to 12 V
AGND to DGND	±0.3 V
Analog Inputs to AGND (Exc. ATTEN)	±5VANA ± 0.3 V
ATTEN Input to AGND	±15 V
REFOUT, EXCIT to AGND	−0.3 V to +5VANA + 0.3 V
Digital Inputs to DGND	−0.3 V to +5VDIG + 0.3 V
Digital Outputs to DGND	−0.3 V to +5VDIG + 0.3 V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Power Dissipation to 75°C	1,000 mW
Derate Above +75°C by	10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings apply individually only, not in combination.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD1B60BS	−40°C to +85°C	S-64
AD1B60BJ	−40°C to +85°C	J-44
AD1B60/EB	−40°C to +85°C	Printed Circuit Board

NOTES

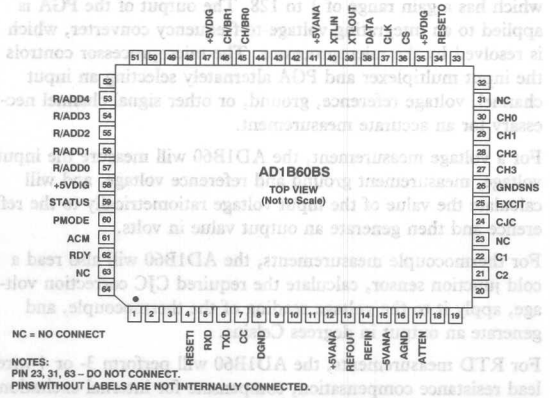
*S = Plastic Quad Flat Pack (PQFP), J = J-leaded Ceramic Chip Carrier, /EB = Evaluation Board with AD1B60BJ & Software. Consult factory for availability. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1B60 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table I. Pin Functions

BS #	BJ #	Name	Connection
4	18	RESETI	Reset input; active high. Initializes the AD1B60 to the pin-strapped and EEPROM default values. Connect to RESETO.
5	19	RXD	Receive data input for asynchronous port.
6	20	TXD	Transmit data output for asynchronous port.
7	21	CC	Continuous Conversion input. Enables synchronous signal integration or continuous conversion. While low, the AD1B60 waits in "idle mode." When CC goes high, the AD1B60 starts converting. While held high, the AD1B60 continuously converts input data.
8	22	DGND	Digital ground.
12	23	+5VANA	+5 V, ± 5% analog power supply.
13	24	REFOUT	Output from internal reference (+2.5 V).
14	25	REFIN	Reference input; may be connected directly to REFOUT.
15	26	−5VANA	−5 V, ± 5% analog power supply.
16	27	AGND	Analog ground.
17	28	ATTEN	5:1 attenuator input for ±5 V and ±10 V input voltages.
21	29	C2	External integration capacitor (nominally 2.2 nF).
22	30	C1	External integration capacitor.
23	31	NC	Make no connection (factory test).
24	32	CJC	External CJC sensor input. Also outputs 20 μA excitation current in thermistor CJC mode.
25	33	EXCIT	Excitation Output: provides 10 nA for open thermocouple detection if a thermocouple range is selected, or 200 μA excitation if an RTD range is selected.
26	34	GNDSNS	Sense input for ground potential. Connect to AGND (typical).
27	35	CH3	Channel 3 signal input.
28	36	CH2	Channel 2 signal input.
29	37	CH1	Channel 1 signal input.
30	38	CH0	Channel 0 signal input.
31	39	NC	Make no connection (factory test).
34	40	RESETO	Output from the power-on reset/brownout detect/watchdog timer circuit; active high. Connect to RESETI.
35	41	+5VDIG	+5 V, ± 5% digital power supply; connect also to other +5 VDIG pins.
36	42	CS	Chip select input (low to select). Connect to DGND if not used.
37	43	CLK	Synchronous serial shift clock input. Connect to DGND if not used.
38	44	DATA	Synchronous serial data output.
39	1	XTLOUT	External crystal (11.0592 MHz).
40	2	XTL1N	External crystal (11.0592 MHz) or external logic-level clock input.
41	3	+5VANA	+5 V, ± 5% analog power supply.
45, 46	4, 5	CH/BR0-1	Channel select inputs when PMODE is low at reset. Baud rate select inputs when PMODE is high at reset.
47	6	+5VDIG	+5 V, ± 5% digital power supply; connect also to other +5 VDIG pins.
53–57	7–11	R/ADD4-0	Range select inputs if PMODE is low at reset. Address select inputs if PMODE and ACM are high at reset. External pull-ups are required.
58	12	+5VDIG	+5 V, ± 5% digital power supply; connect also to other +5 VDIG pins.
59	13	STATUS	Computation status output. If Status is high, results from the previous signal integration are being computed; if STATUS is low, results are available.
60	14	PMODE	Mode select input for CH/BR and R/ADDR pins; high or low state sensed at power-up and reset. Specifies whether input range, input channel, device address, and baud rate are determined by external pins or by values in EEPROM.
61	15	ACM	Addressed Communication Mode input. When ACM is high, address and CRC are enabled.
62	16	RDY	Ready (integration status) output. If RDY is high, the AD1B60 is integrating the signal; if RDY is low, the AD1B60 is integrating a background input.
63	17	NC	Make no connection (factory test).



AD1B60 Pin Assignments

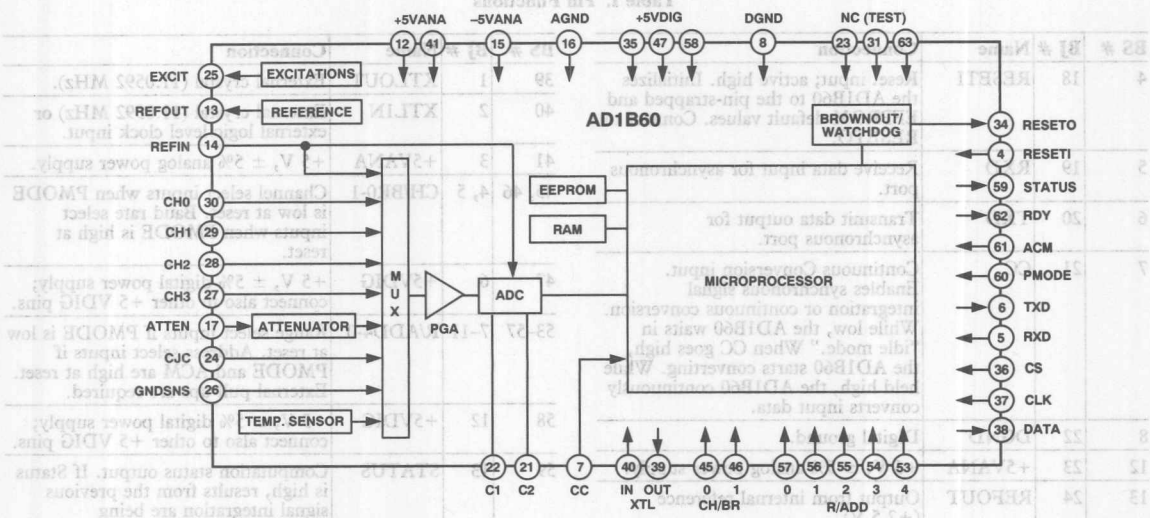


Figure 1. Functional Block Diagram

FUNCTIONAL DESCRIPTION

The AD1B60 is a complete data acquisition subsystem in a single package which interfaces directly to a sensor and a host processor (see Figure 1). The sensor is applied to one or more of the multiplexer inputs and amplified by the programmable gain amplifier. Excitation currents for RTDs, open thermocouple input detection, and cold junction compensation sensors are provided.

The AD1B60 has an input multiplexer with four channels for low level input signals and one channel with an attenuator for high level inputs. There are also reference and zero inputs, a cold junction compensation channel, and an internal temperature sense channel on the multiplexer. Voltage input ranges are ±10 mV full scale to ±10 V full scale.

The multiplexer feeds a programmable gain amplifier (PGA), which has a gain range of 1 to 128. The output of the PGA is applied to an integrating voltage-to-frequency converter, which is resolved by the microprocessor. The microprocessor controls the input multiplexer and PGA alternately selecting an input channel, voltage reference, ground, or other signal channel necessary for an accurate measurement.

For a voltage measurement, the AD1B60 will measure the input voltage, measurement ground and reference voltage, and will calculate the value of the input voltage ratiometrically to the reference and then generate an output value in volts.

For thermocouple measurements, the AD1B60 will also read a cold junction sensor, calculate the required CJC correction voltage, apply it to the voltage reading of the thermocouple, and generate an output in degrees Celsius.

For RTD measurements, the AD1B60 will perform 3- or 4-wire lead resistance compensation, compensate for internal excitation and gain drifts and generate an output in degrees Celsius.

The AD1B60's standard input ranges include the seven NIST thermocouple standards, two platinum RTD ranges, and ten voltage ranges.

In addition, the AD1B60 can use two ranges stored in internal EEPROM. These "custom" ranges are easily created by the user through use of the AD1B60 Custom Range Generation Software included with every Evaluation Board. Several example files, such as a Type N thermocouple range, are also included with the software.

With each conversion, the AD1B60 reports status information, input channel, and an overflow flag. The AD1B60 communicates via one or both of its serial ports: a 2-wire asynchronous I/O port up to 19.2 kbaud, and a 3-wire synchronous data output port up to 5 Mbps.

The AD1B60 contains a brownout detector and watchdog monitor circuit. If any of the power supplies falls below a threshold, or if the internal microprocessor fails to trigger the watchdog timer, this circuit will generate a reset output.

CONFIGURABLE PARAMETERS

You can set the following parameters of the AD1B60:

- Device Address
- Baud Rate
- Channel Selection
- Input Range
- Integration Time
- Cold Junction Compensation Mode
- RTD Connection Mode

Depending on the parameter, you can change values in the following ways:

- Execute AD1B60 commands to change values in EEPROM.
- Set specified pins on the AD1B60.
- Execute AD1B60 commands to change values in RAM.

The factory-programmed default values of the configurable parameters are listed in Table II.

If the default values for the device address and baud rate do not match those in your application, you must reset the AD1B60 with the PMODE pin high and the desired device address and baud rate set by AD1B60 pins. Using AD1B60 commands, you can change the EEPROM-based defaults, and then power up the AD1B60 with PMODE low to use the new default values from EEPROM.

The following section describes the configurable parameters. The COMMAND SET section describes the commands used to change parameter settings.

Table II. Configurable Parameters and their Default Values

Configurable Parameter	Factory Default Value	For Details, See
Device Address	0	Table I
Baud Rate	9600	Table VII
Channel Selection	0	Figure 5
Input Range	Type J Thermocouple	Table III
Integration Time	100 ms	Table IV
Cold Junction Compensation Mode	Direct Connection of a Thermistor	Table V
RTD Connection Mode	3-Wire	Figure 6

CONFIGURATION PARAMETER DESCRIPTIONS

Device Address

In Addressed Communication Mode (ACM pin high), you can connect a cluster of up to 32 AD1B60s to a single communication port. Each AD1B60 in a cluster must have a unique address from 0 to 31 (0 to 1F hex).

When the AD1B60 is reset with PMODE high, the address is read from R/ADD 4–0 pins. Refer to Table I for more information on using the pins of the AD1B60.

When the AD1B60 is reset with PMODE low, the address is read from EEPROM. You can change the default address stored in EEPROM by executing the WR_EPM_PARS command.

Baud Rate

You can set one of the following baud rates for the AD1B60: 2400, 4800, 9600 (the factory default), or 19200.

When the AD1B60 is reset with PMODE low, the baud rate is read from EEPROM. You can change the default baud rate stored in EEPROM by executing the WR_EPM_PARS command.

When the AD1B60 is reset with PMODE high, the baud rate is read from the CH/BR 0–1 pins.

Channel Selection

Although the AD1B60 is optimized for single-channel applications, you can use up to five input channels on one device. The AD1B60 checks the input channel selection before each conversion. Note that selecting an RTD or high voltage input range also determines the channel(s).

If the AD1B60 is powered up with PMODE high, Channel 0 is selected. For thermocouple and low level voltage ranges, you can select an input channel using the SEL_CH command. Check the channel address in the ADSTAT byte returned with the data to ensure that the data represents the correct channel. Also check ADSTAT's Valid Data flag after changing channels. You may have to wait up to two integration times for valid data when changing channels on the same input range. Refer to the COMMAND SET section for more information on SEL_CH.

If the AD1B60 is reset with PMODE low, the input channel is determined by the CH/BR 0–1 pins.

Input Ranges

The AD1B60 supports the input ranges listed in Table III.

If the standard input ranges (numbered 00 through 12 hex) do not meet the requirements of your application, you can download up to two additional user defined custom input ranges into the AD1B60. Custom ranges are generated by the user with the Custom Range Generation Software. Refer to the following subsection for more information on downloading input ranges.

The input range is determined by the R/ADD 4–0 pins when the AD1B60 is reset with PMODE low.

Table III. Input Ranges

Input Range	Range Code (In Hex)
±10 mV	00
±20 mV	01
±50 mV	02
±100 mV	03
±200 mV	04
±500 mV	05
±1 V	06
±2 V	07
±5 V (ATTEN Input)	08
±10 V (ATTEN Input)	09
Type J Thermocouple, 0°C to 760°C*	0A*
Type K Thermocouple, 0°C to 1000°C	0B
Type T Thermocouple, −100°C to +400°C	0C
Type E Thermocouple, 0°C to 1000°C	0D
Type R Thermocouple, 500°C to 1750°C	0E
Type S Thermocouple, 500°C to 1750°C	0F
Type B Thermocouple, 500°C to 1800°C	10
Platinum RTD, 100 Ω, α = 0.00385, −200°C to +800°C	11
Platinum RTD, 100 Ω, α = 0.00392, −200°C to +800°C	12
Not Used	13 to 1D
User Range 1	1E
User Range 2	1F

NOTE
*Default Configuration

The input range is read from EEPROM when the AD1B60 is reset with PMODE high. To change the input range stored in EEPROM, execute the WR_EPM_PARS command. You can also change the input range by using the WR_RAM_PARS command. This command changes the range immediately and does not affect values in EEPROM. You can issue the RD_RAM_PARS command to read the current configuration.

You can use only one input range at a time. When you change the input range, you may have to wait up to 13 integration times to ensure that the output data is valid, as indicated by the Valid Data flag in the ADSTAT byte. Therefore, you should only change the input range in applications having very low bandwidth.

to download into the AD1B60's EEPROM at any time. A range is typically generated by a user in order to accept a sensor or input signal not supported by the standard AD1B60 internal ranges or to provide a range that optimizes the output data for easier calculations or other considerations.

Ranges can be simply made by using the IBM PC compatible, Windows version "AD1B60 Custom Range Generation Software." All AD1B60 software is included free of charge with each Evaluation Board.

To download an input range to EEPROM, execute the LOAD_RNG command. You must execute LOAD_RNG eight times to download the entire input range to EEPROM. Refer to the COMMAND SET section for more information on this command.

Reading User-Downloaded Input Ranges

To verify a user-downloaded input range, execute the GET_RNG command. You must execute GET_RNG eight times to read the entire input range from EEPROM.

Integration Time

You can set the integration time used by the AD1B60's A/D converter. The integration time and the input range affect the overall conversion rate. Table IV shows available integration times and the range of corresponding conversion rates, as well as line frequencies that have high normal mode rejection (NMR). Voltage ranges have the fastest conversion rates. Because of the extensive calculation required for linearization and compensation, the conversion rate for Type K thermocouples is the slowest of the AD1B60's standard ranges.

Setting the integration time equal in duration to an integral number of power line cycles will cause high normal mode rejection at the line frequency. The fastest available integration times for 50 Hz and 60 Hz are 40 ms and 33.3 ms, respectively; each time is equal to two power line cycles. The default integration time, 100 ms, is an integral multiple of both power line periods.

You can change the default integration time stored in EEPROM by executing the WR_EPM_PARS command. You can change the integration time without changing values in EEPROM by executing

Cold Junction Compensation Mode

The AD1B60 provides four different CJC modes for thermocouple ranges, described in Table V.

You can change the default CJC mode stored in EEPROM by executing the WR_EPM_PARS command.

You can change the CJC mode without changing the EEPROM default by executing the WR_RAM_PARS command. To read the current CJC mode from RAM, execute the RD_RAM_PARS command. To read the current value of the CJC temperature from RAM, execute the RD_CJC command.

RTD Connection Mode

The AD1B60 supports 3-wire and 4-wire RTD connection modes (see Figures 10, 11, and 12); 3-wire is the default configuration.

You can change the default RTD connection mode stored in EEPROM by executing the WR_EPM_PARS command.

You can change the RTD connection mode without changing the EEPROM default by executing the WR_RAM_PARS command. To read back the current configuration stored in RAM, execute the RD_RAM_PARS command.

Table IV. Integration Times

Integration Time	Conversion Rate	High NMR Frequency	AUX Byte Bits B2–B0
200 ms	2.5 per second	50 or 60 Hz	000
100*	5*	50 or 60	001*
60	8.3	50	010
50	9.9	60	011
40	12.3	50	100
33.3	14.8	60	101
5	44† to 87.5‡		110
2	48† to 100‡		111

NOTES
*Default Configuration
†Type K thermocouple with thermistor CJC (mode 00)
‡Voltage range with CJC disabled (Mode 11)

Table V. Cold Junction Compensation Modes

CJC Sensor Type	CJC Mode Description	CJC Excitation Current	Cold Junction Temperature Range	AUX Byte Code, Bits B6–B5
Thermistor*	Direct connection of a 10K3A1 thermistor made by Betatherm (Shrewsbury, Massachusetts, and Galway, Ireland). At +25°C, this thermistor's R = 10 kΩ, alpha = −4.4%/°C, and beta = 3892.	Enabled	−25°C to +70°C	00*
1 mV/K	A 1 mV/K external sensor is connected at the input. This mode allows the use of silicon sensors, such as the Analog Devices AD592 with a 1 kΩ resistor (see Figure 9).	Disabled	−25°C to +85°C	01
Downloaded	A user-defined value of an externally derived cold junction temperature is downloaded over the asynchronous communication port using the WR CJC command.	Disabled	–25°C to +85°C	10
CJC Calculation Disabled	No CJC calculations are performed by the AD1B60. An analog CJC, such as the Analog Devices AC1226, is connected at the input. This type of sensor must be externally configured for the specific thermocouple type.	Disabled	User-defined; must be in −25°C to +85°C range	11

NOTE
*Default Configuration

CONVERSION TIMING AND CONTROL

In normal operation, the Continuous Conversion (CC) Pin is high, and the AD1B60 performs continuous conversions, alternating between signal conversions and background conversions, such as autozero or cold junction compensation (see Figure 2a).

The RDY pin and the Ready flag in the ADSTAT byte are high while the AD1B60 integrates the input signal. The STATUS pin and Status flag in the ADSTAT byte are high while the AD1B60 computes the result of the signal integration. When STATUS goes low, the data is available at the Asynchronous Communication Port. When RDY goes high again for the next signal integration, the data from the prior conversion is available at the Synchronous Data Output Port.

When CC is low, signal conversions are suspended. After CC goes high, a signal conversion will start. This allows synchronizing the conversions to external events, or synchronizing multiple AD1B60s (see Figure 2b). If you communicate with the AD1B60 using the Asynchronous Communications Port, the time spent in communications service may increase the latency between the trigger and the signal conversion.

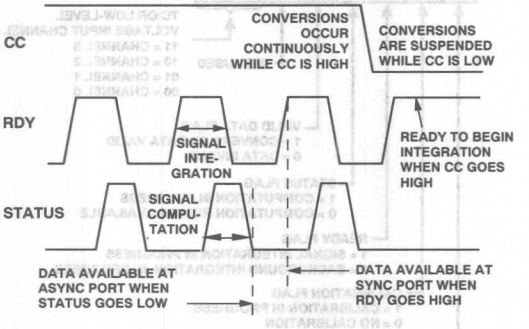


Figure 2a. Continuous Conversion

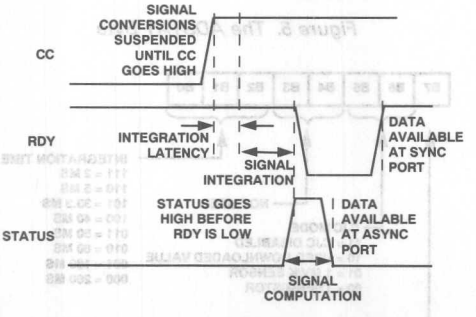


Figure 2b. Synchronizing Conversion

SERIAL COMMUNICATION PORTS

Asynchronous Communication Port

The asynchronous communication port is a two-wire, half-duplex, input/output port. You can connect the asynchronous port to host systems either at +5 V logic levels or by using external level translation to communication standards such as RS-232 and RS-422. The AD1B60 responds to the commands listed in the COMMAND SET section.

The asynchronous port operates at 2400, 4800, 9600, or 19200 baud using eight data bits, no parity, and one stop bit. Bytes are transmitted least significant bit first.

In Addressed Communications Mode (ACM), the asynchronous port supports device addressing and CRC error checking. Device addressing enables clusters of up to 32 AD1B60s to share a single communication line (see Figure 3). Cyclic Redundancy Codes (CRC) improve communication reliability in noisy environments. The AD1B60 uses CRC-16 ($x^{16} + x^{15} + x^2 + 1$) as a generator polynomial.

ACM is active when the ACM pin is high. When ACM is active, the address and CRC are required to accompany commands to the AD1B60, which will include address and CRC in its response. See the COMMAND PARAMETERS section for details on the format of address and CRC. The address and baud rate are read from either EEPROM or external pins at reset, depending on the state of the PMODE pin.

When the PMODE pin is low at reset, device address and async port baud rate are read from EEPROM, and input range and channel are read from R/ADD and CH/BR pins at reset. When PMODE is high at reset, address and baud rate are read from these pins, input range is read from EEPROM, and input channel is set to 0.

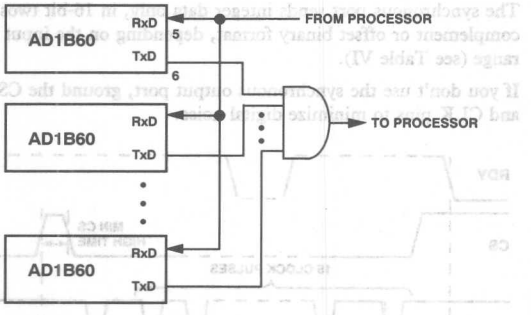


Figure 3. Connecting a Cluster of AD1B60s to a Communication Port

If you intend to use the AD1B60 with a device address or baud rate different from the values in EEPROM, reset the device with PMODE high and the desired address and baud rate selected through the R/ADD and CH/BR pins. You may then load the desired values of device address and baud rate into EEPROM to free these pins for selecting input range and channel.

If a message with an invalid address, command code, or CRC is received by an AD1B60, it will not respond to that message. The host may use a time-out to detect an AD1B60 that does not respond. If the host detects an error from an AD1B60, whether by invalid response or lack of response, it may issue a Break and retry the command.

The AD1B60 will detect Breaks to allow recovery from communications errors. The AD1B60 recognizes a Break when it receives a character with a zero (space) where the stop bit should be. The AD1B60 then resets its communications processes, and is ready to receive the next command. All AD1B60s on a line will recognize a Break.

Asynchronous communications with the AD1B60 are half-duplex. If a character is sent to an AD1B60 while it is transmitting, it ignores the character and continues transmitting. After its transmission is complete, the AD1B60 is ready to receive the next character.

Synchronous Data Output Port

The synchronous port is a 3-wire data output port. It is independent of the asynchronous port, and both can be accessed simultaneously, if desired.

Using the CS (chip select), CLK (clock input), and DATA (data output) pins of the AD1B60, you can read data at speeds up to 5 Mbps (see Figure 4). When RDY goes high at the beginning of a conversion cycle, the MSB of the previous data word appears at the DATA output (see Figures 2a and 2b). Bringing CS low freezes the data in the synchronous port buffer. Results of other conversions won't be transferred to the synchronous port buffer while CS is low. 15 CLK pulses will read out the remaining bits of the word in the synchronous port buffer. Further CLK pulses will continue to read out the same data bits from this circular buffer.

After all 16 bits are read, CS must be brought high and then low again to read the next word. CS must stay high for a minimum of 400 µs to allow the data buffer to be updated.

The synchronous port sends integer data only, in 16-bit twos complement or offset binary format, depending on the input range (see Table VI).

If you don't use the synchronous output port, ground the CS and CLK pins to minimize digital noise.

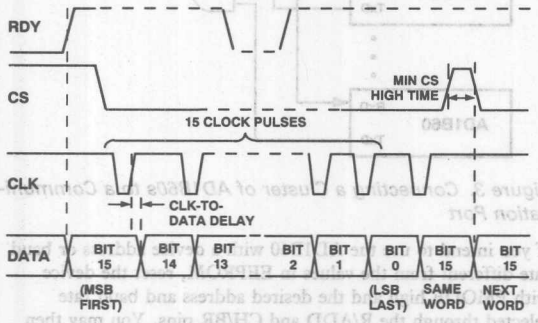


Figure 4. Reading Data from the Synchronous Port

Table VI. Integer Data Output Formats

Voltage Ranges (Twos Complement, in Hex)		Temperature Ranges (Offset Binary, in Hex)	
+Full Scale	7FFF	Top of Span	FFFF
Zero	0000		
Zero –1 LSB	FFFF		
–Full Scale	8000	Bottom of Span	0000

COMMAND PARAMETERS

This section describes the parameters of the AD1B60 commands, which are described in the next section. All values in <angle brackets> and [square brackets] are 8-bit bytes; values in [square brackets] are used only when ACM is active. Numbers followed by H are expressed in hexadecimal (hex) notation.

[Addr] represents the address of the AD1B60. It is required in the command and generated in the response only if ACM is active. Values for [addr] range from 00H to 1FH (0 to 31 decimal). The factory default value is 00H.

<ADSTAT>, shown in Figure 5, represents the status of the AD1B60. Values of ADSTAT range from 00H to FFH. ADSTAT's Valid Data flag and Input Channel should be checked on every measurement reading.

<Aux>, shown in Figure 6, represents the RTD connection mode, CJC mode, and integration time of the AD1B60. Values of <aux> range from 00H to FFH and may be read via the RD_RAM_PARS command.

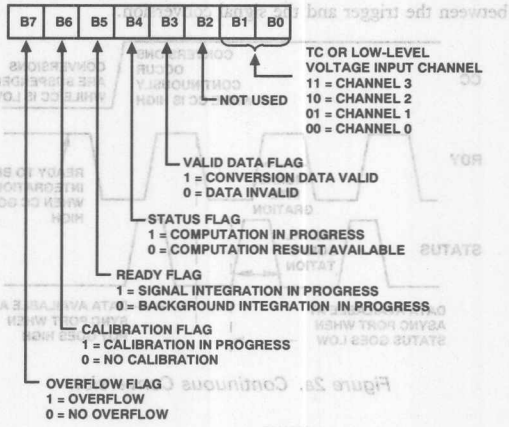


Figure 5. The ADSTAT Byte

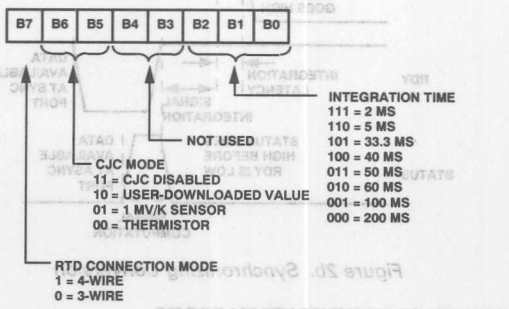


Figure 6. The Aux Byte

Table VII. Baud Rate Codes

Baud Rate	Baud Code (in Hex)
2400	00
4800	01
9600*	02*
19200	03

NOTE
*Default Configuration

<Baud> represents the baud rate code of the AD1B60. Table VII lists the codes associated the available baud rates.

<C0> through <C3> are four bytes that represent the CJC temperature, in ANSI/IEEE 754-single-precision floating-point format, and in degrees C. Values ranges from −25°C to +85°C. For example, in this format, a 25°C is expressed as 41 C8 00 00 (hexadecimal). <C0> contains the least significant byte of the mantissa, or 00H in this example; <C3> contains the sign bit and the 7 most significant bits of the exponent, or 41H in this example.

[CRC1] and [CRC2] represent the CRC-16 error checking value. These arguments are required in the command and generated in the response only if ACM is active. [CRC1] is the LSB; [CRC2] is the MSB.

<Device_addr> represents the new default address for the AD1B60. Values for <device_addr> range from 00H to 1FH (0 to 31 decimal).

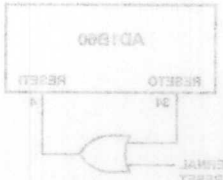
<D0> through <D7> comprise an 8-byte segment of the user-selected input range in EEPROM. <D0> is the low order byte; <D7> is the high order byte.

<F0> through <F3> are four bytes that represent the floating-point data, in IEEE 754 standard format. See the description of <C0> through <C3>, above, for information on this format.

<INT_LO> and <INT_HI> represent the lower and upper eight bits, respectively, of the 16-bit integer representation of the data. Values range from 00H to FFH; see Table VI for data formats.

<Range> represents the input range code. Refer to Table III for a list of the available input range codes. The current range may be read via the RD_RAM_PARS command.

<Range_addr> represents the address of the 8-byte segment of the 64-byte input range in EEPROM. Range addresses 00H to 07H correspond to the eight, 8-byte segments of User Range 1 (code 1EH); range addresses 08H to 0FH correspond to the eight, 8-byte segments of User Range 2 (code 1FH).



COMMAND SET

The AD1B60 commands allow you to configure the AD1B60, read converted data and status information, and calibrate input ranges over the asynchronous port. This section describes the commands in detail.

Configuration Commands

The AD1B60 Command Set provides the configuration commands listed below. Note that the data written into RAM by WR_RAM_PARS, WR_CJC, and SEL_CH will be cleared at power-up and reset.

- **RD_RAM_PARS**

Reads back the current value of the configuration parameters from RAM.

Command Syntax
[addr] <02H> [CRC1] [CRC2]

Response Syntax
[addr] <02H> <range> <aux> [CRC1] [CRC2]

- **WR_RAM_PARS**

Writes new values of the configuration parameters in RAM. These values take effect immediately and do not change the default values in EEPROM.

Command Syntax
[addr] <04H> <range> <aux> [CRC1] [CRC2]

Response Syntax
[addr] <04H> [CRC1] [CRC2]

- **WR_EPM_PARS**

Writes new values of the configuration parameters in EEPROM. The new values do not change currently selected values in RAM and only take effect when the AD1B60 is powered up or reset.

Command Syntax
[addr] <05H> <range> <aux> <device-addr> <baud> [CRC1] [CRC2]

Response Syntax
[addr] <05H> [CRC1] [CRC2]

- **GET_RNG**

Reads an 8-byte segment of a downloadable input range from EEPROM. See LOAD_RNG, below.

Command Syntax
[addr] <07H> <range-addr> [CRC1] [CRC2]

Response Syntax
[addr] <07H> <D0> <D1> <D2> <D3> <D4> <D5> <D6> <D7> [CRC1] [CRC2]

- **LOAD_RNG**

Writes an 8-byte segment of a downloadable input range into EEPROM. LOAD_RNG and GET_RNG must be executed 8 times to write or read an entire 64-byte range. Each successive time, <range-addr> must increment by 1 to address the next segment.

Command Syntax
[addr] <08H> <range-addr> <D0> <D1> <D2> <D3> <D4> <D5> <D6> <D7> [CRC1] [CRC2]

Response Syntax
[addr] <08H> [CRC1] [CRC2]

5

This value may have been measured by a thermistor or RTD sensor, or loaded via a WR_CJC command.

Command Syntax
[addr] <03H> [CRC1] [CRC2]

Response Syntax
[addr] <03H> <C0> <C1> <C2> <C3> [CRC1] [CRC2]

- **WR_CJC**

Downloads to RAM a CJC temperature in °C, obtained from an external source. Only used in Downloaded CJC mode (mode 10).

Command Syntax
[addr] <06H> <C0> <C1> <C2> <C3> [CRC1] [CRC2]

Response Syntax
[addr] <06H> [CRC1] [CRC2]

- **SEL_CH**

Selects an input channel on the AD1B60 and stores the channel address in RAM. This command is not meaningful if the PMODE pin is low, or if the input range is RTD or attenuator; for these ranges, the channel is selected automatically.

Command Syntax
[addr] <0AH> <chan> [CRC1] [CRC2]

Response Syntax
[addr] <0AH> <chan> [CRC1] [CRC2]

Read Data Commands

The AD1B60 Command Set includes the following read data commands:

- **RD_INTDATA**

Reads converted data, in 16-bit integer format (see Table VI), and the conversion status.

Command Syntax
[addr] <00H> [CRC1] [CRC2]

Response Syntax
[addr] <00H> <INT_LO> <INT_HI> <ADSTAT> [CRC1] [CRC2]

- **RD_FPDATA**

Reads converted data, in IEEE 754 floating point format and engineering units, and the conversion status.

Command Syntax
[addr] <01H> [CRC1] [CRC2]

Response Syntax
[addr] <01H> <F0> <F1> <F2> <F3> <ADSTAT> [CRC1] [CRC2]

Calibration Command

- **CAL**

Performs a calibration cycle for parameters related to the configured input range. See the Calibration section below.

Command Syntax
[addr] <09H> <09H> [CRC1] [CRC2]

Response Syntax
[addr] <09H> <09H> [CRC1] [CRC2]

tory prior to shipment. You can also calibrate the AD1B60 in your application, if desired. You should calibrate the AD1B60 if you use an external reference.

Calibrating the AD1B60 requires a precision reference excitation source for different input ranges. The accuracy of the AD1B60 depends on the accuracy of the calibration source. For best performance, calibrate the AD1B60 using the maximum integration time of 200 ms.

Note that calibrating certain input ranges, such as thermocouple ranges, depends on the prior calibration of one or more voltage ranges. Therefore, to properly calibrate all the input ranges and channels of the AD1B60, perform the following procedure for each step of the calibration sequence:

1. Using the WR_RAM_PARS command, configure the AD1B60 for the appropriate range listed in Table VIII. For example, in the first step of the calibration sequence, set the input range to ±2 V.
2. Apply the reference excitation specified for the input range, listed in Table VIII. For example, in the first step of the calibration sequence, apply a +2.00000 V excitation to channel 0.
3. Issue RD_FPDATA or RD_INTDATA commands and observe the readings. Allow the excitation source to stabilize, and check that the Valid Data flag in the ADSTAT byte is high.
4. Execute the CAL command.
5. Wait until the CAL flag in ADSTAT goes low.
6. Repeat operations 1 through 5 above, using the input ranges and reference excitations, listed in Table VIII, for the next step of the calibration sequence.

Note that you must complete Steps 1 through 8 in Table VIII. However, if your application does not require the attenuator input, you can skip Step 9. If your application does not require thermocouples, you can skip Step 10. If your application does not require RTDs, you can skip Step 11.

RESETTING THE AD1B60

The AD1B60 generates a reset signal (RESETO) at power-up, on detecting a low supply voltage (brown-out), or on missing an internal watchdog pulse. In normal operation, RESETO is tied to the reset input (RESETI). An external active-high reset signal may be used instead of, or in addition to, RESETO. Figure 7 shows how to OR internal and external signals to control RESETI.

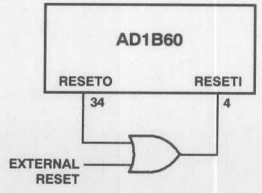


Figure 7. Resetting the AD1B60

Table VIII. Input Ranges and Reference Excitations for Each Iteration of the Calibration Sequence

Step	Input Range	Range Code	Reference Excitation	Channel to Which Reference Excitation Is Applied
1	±2 V	07	+2.00000 V	CH0 to Analog Gnd
2	±1 V	06	+1.00000 V	CH0 to Analog Gnd
3	±500 mV	05	+0.50000 V	CH0 to Analog Gnd
4	±200 mV	04	+0.20000 V	CH0 to Analog Gnd
5	±100 mV	03	+0.10000 V	CH0 to Analog Gnd
6	±50 mV	02	+50.000 mV	CH0 to Analog Gnd
7	±20 mV	01	+20.000 mV	CH0 to Analog Gnd
8	±10 mV	00	+10.000 mV	CH0 to Analog Gnd
9	±10 V	09	+10.00000 V	Attenuator Input to Analog Gnd
10	Type J Thermocouple	0A	100.000 kΩ	CJC Input to Analog Gnd
11	100 Ω Pt. RTD, α = 0.00385	11	250.000 Ω	250 Ω Reference Resistor Substituted for 4-Wire RTD (See Figure 10)

5

TYPICAL INPUT CONNECTIONS

Thermocouple Input Connections

Figure 8 shows the AD1B60 connections required for a typical, single thermocouple input. In this example, a thermistor CJC sensor is used; the AD1B60 provides the CJC sensor excitation current. The EXCIT output can be used to source current, nominally 10 nA, for open-circuit detection.

Figure 9 shows how four thermocouples may be connected, using a 1 mV/K CJC sensor. All thermocouple inputs must share a common ground.

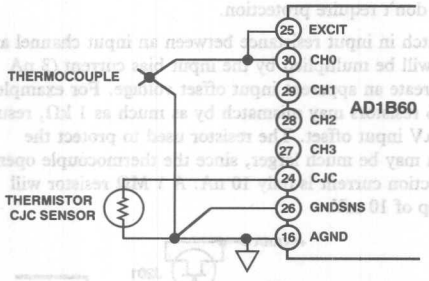


Figure 8. Typical Single-Channel Thermocouple Connection (with Thermistor CJC)

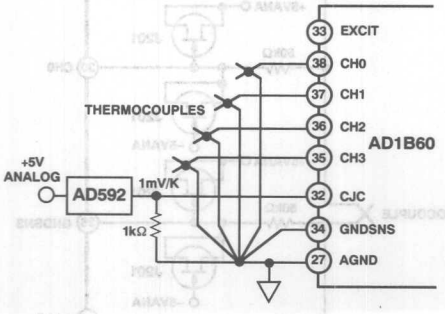


Figure 9. Typical Four-Channel Thermocouple Connection (with AD592 CJC)

Using the CJC Pin as a Digital Output

The CJC pin is normally used as an analog input for cold-junction compensation of thermocouples. When thermistor CJC mode is selected, this pin also outputs an excitation current (nominally 20 μA) for the CJC sensor. In other CJC modes, this output is switched off.

If thermocouples are not being used, the CJC pin may serve as a digital output. This may be especially useful if the AD1B60 is isolated, since providing an isolated control line by other means would be costly.

By placing a 330 kΩ resistor to AGND from this pin, a logic voltage can be generated (see Figure 11). The level can be switched from high (about +4 V) to low (AGND) by changing the CJC mode from thermistor (00) to any other, using the WR_RAM_PARS command.

RTD Input Connections

Typical 3-wire and 4-wire RTD input connections are shown in Figure 10. The EXCIT output supplies 200 μA excitation to the RTD. To maintain high accuracy, lead resistances must match and be less than 20 Ω for 3-wire RTDs, and must be less than 40 Ω for 4-wire RTDs. The 10 kΩ resistor in series with the excitation current source is not required, but will reduce power dissipation and self-heating errors in the AD1B60.

Two RTDs can be multiplexed using the CJC pin as a control line to select between them, as described in the previous subsection. Figures 11 and 12 show multiplexed 3-wire and 4-wire RTDs.

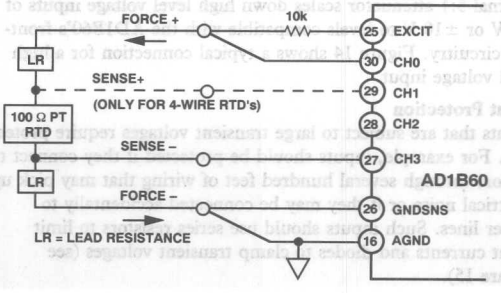


Figure 10. Typical Single-Channel RTD Connection

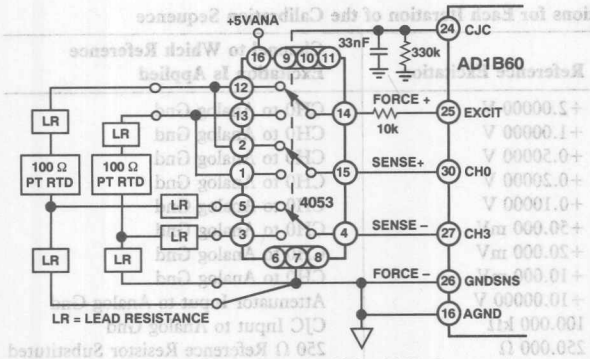


Figure 11. Typical Multiplexed 3-Wire RTD Connection

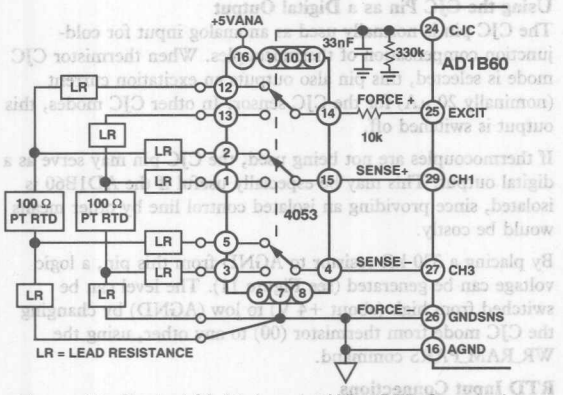


Figure 12. Typical Multiplexed 4-Wire RTD Connection

Low Level Voltage Input Connections

Single channel input connections for low level voltages of up to ±2 V are similar to those of thermocouple input connections, except that no CJC sensor is required. When connecting multiple-channel, low level voltage inputs, all four inputs must share a common ground, as shown in Figure 13. For fastest response when switching between channels, all inputs must share the same input range.

High Level Voltage Input Connections

High level voltages must be connected to the Attenuator pin. An internal 5:1 attenuator scales down high level voltage inputs of ±5 V or ±10 V to levels compatible with the AD1B60's front-end circuitry. Figure 14 shows a typical connection for a high level voltage input.

Input Protection

Inputs that are subject to large transient voltages require protection. For example, inputs should be protected if they connect to sensors through several hundred feet of wiring that may pick up electrical noise or if they may be connected accidentally to power lines. Such inputs should use series resistors to limit input currents and diodes to clamp transient voltages (see Figure 15).

The EXCIT, CH0-CH3, and GNDSNS pins may be subject to large transients and hence may require protection. The ATTEN

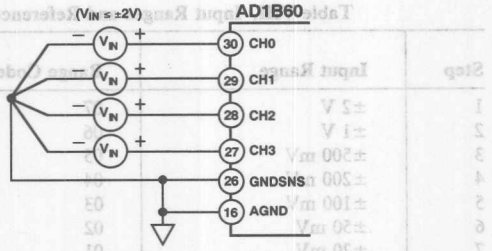


Figure 13. Typical Multiple-Channel Low Level Voltage Input

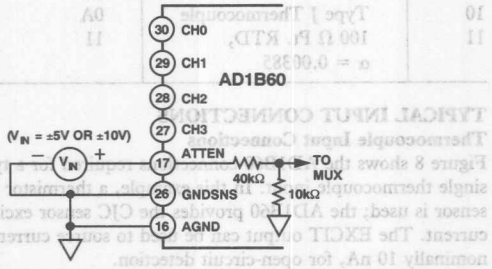


Figure 14. Typical High Level Voltage Input Connection

pin has an internal 40 kΩ resistor, and does not require an external resistor; however, clamp diodes may be required. Generally, the CJC, AGND, and other pins are connected only locally and don't require protection.

Any mismatch in input resistance between an input channel and GNDSNS will be multiplied by the input bias current (3 nA max) and create an apparent input offset voltage. For example, 50 kΩ, 1 % resistors may mismatch by as much as 1 kΩ, resulting in a 3 μV input offset. The resistor used to protect the EXCIT pin may be much larger, since the thermocouple open-circuit detection current is only 10 nA. A 1 MΩ resistor will cause a drop of 10 mV.

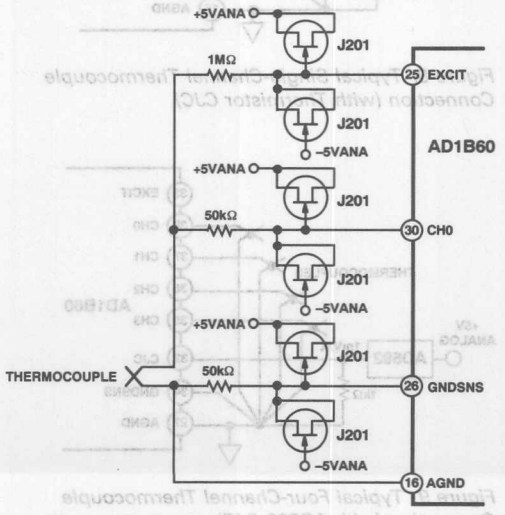


Figure 15. Typical Input Protection Circuitry

The AD1B60 side of the resistors must be clamped to suitable voltages, such as the supply rails (see the Absolute Maximum Ratings). Use low leakage, low capacitance diodes, such as diode-connected J201 JFETs. Note that the diodes' leakage current will flow through the protection resistors and create an offset voltage.

The resistors must be able to withstand the worst-case expected fault voltage, the clamp diodes must be able to pass the worst-case fault current, and the clamp voltages (e.g., the power supplies) must be able to absorb the fault current.

For a fully protected system, you must isolate the AD1B60 from ground. You may do so by using optoisolators on the communications port (RXD and TXD pins) and a dc-to-dc converter for the power supplies.

GENERAL CIRCUIT CONSIDERATIONS

In any system including logic and low level analog signals, care must be taken in the layout and bypassing of the components. Bypass the analog and digital supplies close to the package pins, with a 1.0 μF or 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor. Keep analog and digital grounds separate except at a single common point. Minimize stray capacitance between digital signals and any analog signal, including analog common. All analog grounds should be connected in a star pattern to a single point.

The integrating capacitor, C_{INT}, should be ceramic and of good quality (X7R dielectric or better). If the synchronous output port is not used, connect CS and CLK to DGND to minimize digital noise.

Figure 16 shows a typical hookup for the default configuration parameters: Type J thermocouple with thermistor CJC and device address 0. The AD232 translates between the TTL levels of the AD1B60 and RS-232 levels for the asynchronous I/O port.

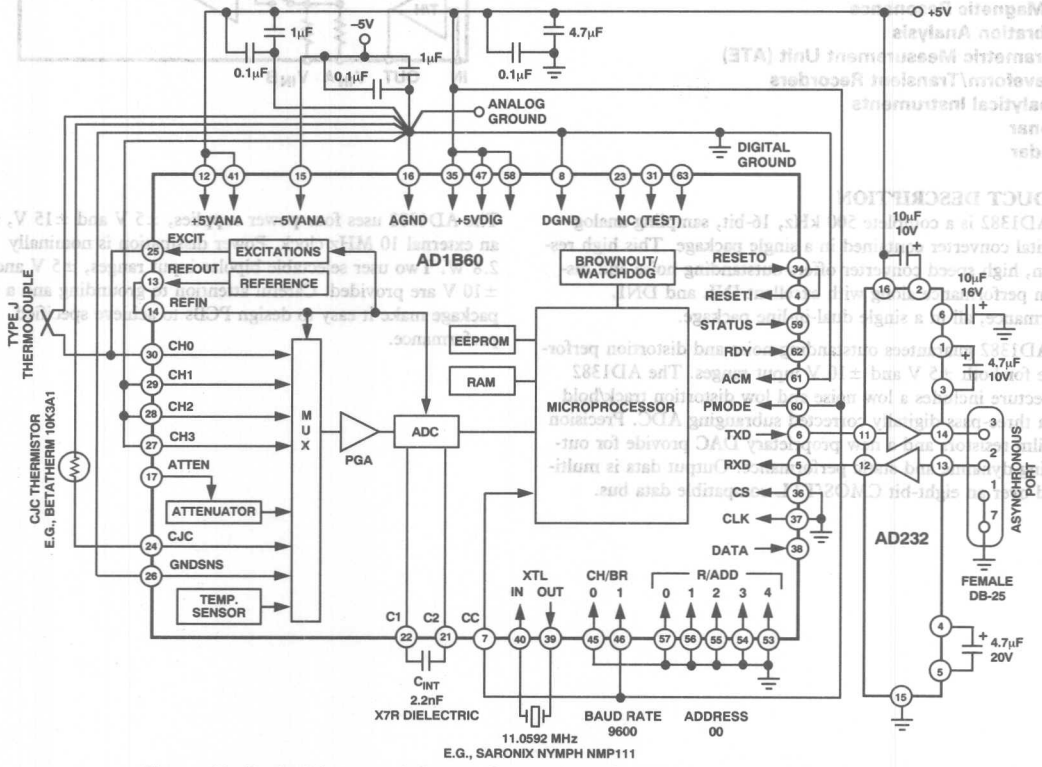


Figure 16. Typical Input and Output Connections for Thermocouple Application

EVALUATION BOARD

The AD1B60/EB evaluation board contains an AD1B60 and support circuitry which allows you to evaluate its functionality and performance using an IBM PC via an asynchronous RS-232 communications port (COM1 or COM2 only).

Included with the evaluation board is an AD1B60BJ device, Evaluation Board User's Manual, 3.5" diskette with the AD1B60 Demonstration Program for PC-DOS and a free copy of the AD1B60 Custom Range Generation Software for Windows.

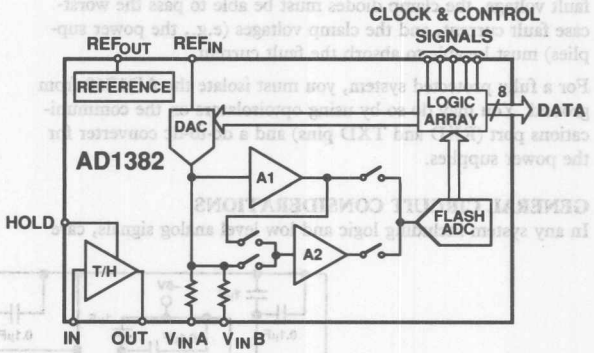
The menu-driven Demonstration Program allows you to configure and read data from the AD1B60. The Custom Range Generation Software allows generation of user defined ranges specific to your application without additional assistance required from Analog Devices. These range files may be downloaded into the EEPROM of the AD1B60 as required to optimize its performance in your specific application.

AD1382

PRODUCT FEATURES
Single Package
16-Bit Resolution
500 kHz Sampling Rate
SNR 90 dB @ 100 kHz (min)
THD −88 dB @ 100 kHz (min)
0.0015% FSR INL (typ)
±5, ±10 V Bipolar Input
Zero Offset Autocalibration

APPLICATIONS
Medical Imaging
CAT
Magnetic Resonance
Vibration Analysis
Parametric Measurement Unit (ATE)
Waveform/Transient Recorders
Analytical Instruments
Sonar
Radar

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1382 is a complete 500 kHz, 16-bit, sampling analog-to-digital converter contained in a single package. This high resolution, high speed converter offers outstanding noise and distortion performance along with excellent INL and DNL performance, all in a single dual-in-line package.

The AD1382 guarantees outstanding noise and distortion performance for both ±5 V and ±10 V input ranges. The AD1382 architecture includes a low noise and low distortion track/hold with a three-pass digitally corrected subranging ADC. Precision thin film resistors and a new proprietary DAC provide for outstanding dynamic and static performance. Output data is multiplexed over an eight-bit CMOS/TTL compatible data bus.

The AD1382 uses four power supplies, ±5 V and ±15 V, and an external 10 MHz clock. Power dissipation is nominally 2.8 W. Two user selectable bipolar input ranges, ±5 V and ±10 V are provided. Careful attention to grounding and a single package make it easy to design PCBs to achieve specified performance.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, V_{DD} = +5 V, V_{SS} = −5 V, 10 MHz External Clock, 5 Minute Warm-up, unless otherwise noted)

Parameter	AD1382KD Min	Typ	Max	Units
RESOLUTION	16			Bits
ANALOG INPUT				
Input Ranges		±5, ±10		V
Input Impedance	2.45	2.5	2.55	kΩ
TRANSFER CHARACTERISTICS				
(Combined ADC/Track/Hold)				
Integral Nonlinearity[1]		±0.0015		% FSR[2]
Differential Nonlinearity[1]		±0.0006	±0.0015	% FSR
Missing Codes			None	
Gain Error[3]		±0.07	±0.15	% FSR
Bipolar Zero[3]		±0.03	±0.10	% FSR
PSRR		±0.006	±0.10	% FSR/V
Noise[4]		55		μV RMS
DYNAMIC CHARACTERISTICS				
±5 V FSR, V_{IN} = −0.4 dB				
Sample Rate			500	kHz
Signal-to-Noise Ratio[5]				
f = 5 kHz	90	93		dB
f = 100 kHz	90	92		dB
f = 200 kHz	88	91		dB
Peak Distortion				
f = 5 kHz		−90	−98	dB
f = 100 kHz		−88	−93	dB
f = 200 kHz		−82	−85	dB
Total Harmonic Distortion[6]				
f = 5 kHz		−90	−96	dB
f = 100 kHz		−88	−92	dB
f = 200 kHz		−82	−85	dB
DYNAMIC CHARACTERISTICS				
±10 V FSR, V_{IN} = −0.4 dB				
Sample Rate			500	kHz
Signal-to-Noise Ratio[5]				
f = 5 kHz	90	95		dB
f = 100 kHz	90	94		dB
f = 200 kHz	88	93		dB
Peak Distortion				
f = 5 kHz		−90	−98	dB
f = 100 kHz		−80	−87	dB
f = 200 kHz		−74	−81	dB
Total Harmonic Distortion[6]				
f = 5 kHz		−90	−96	dB
f = 100 kHz		−80	−87	dB
f = 200 kHz		−74	−81	dB
DIGITAL INPUTS[9]				
Input Voltage				
V_{IL}			0.8	V
V_{IH}	2.0			V
Input Current			±200	μA
Input Capacitance		2		pF
Start Command				
Setup Time, t_{SCS}	10	3		ns
Hold Time, t_{SCH}	10	0		ns
Autozero				
Setup Time, t_{AZS}	10	0		ns
Hold Time, t_{AZH}	20	6		ns
Clock				
Frequency	2.5		10	MHz
Duty Cycle	40		60	%

5

Parameter	AD1382KD Min	Typ	Max	Units
DIGITAL INPUTS (Continued)				
Aperture Delay[7]		7		ns
DIGITAL OUTPUTS[8, 9]				
Output Voltage				
V_{OL} @ I_{OL} = 3.2 mA		0.2	0.4	V
V_{OH} @ I_{OH} = −3.2 mA	2.4	4.5		V
Output Capacitance		10		pF
Leakage, Outputs Disabled			±200	μA
Data Valid				
Setup Time, t_{DVS}	75	150		ns
Hold Time, t_{DVH}	25	50		ns
Hold Command Time, t_H		1300		ns
Hold Command Delay, t_{HD}		6		ns
Data Strobe Pulse Width, t_{DS}		200		ns
Data Strobe Delay, t_{DSD}		1650		ns
OUTPUT CODING	Complementary Offset Binary or Complementary Twos Complement			
PERFORMANCE OVER TEMPERATURE[8, 10]				
Operating Temperature Range	0		70	°C
Specified Temperature Range	10		40	°C
Missing Codes			None	
Gain Drift		8	15	ppm/°C
Offset Drift		5	15	ppm/°C
Differential Linearity		0.3		ppm/°C
INTERNAL REFERENCE				
Voltage	9.990		10.010	V
Current	2	10		mA
POWER REQUIREMENTS				
Operating Range				
$\pm V_S$	14.25		15.75	V
$+V_{DD}$	4.75		5.25	V
$-V_{SS}$	−5.25		−4.75	V
Current Drains				
$+V_S$		50	73	mA
$-V_S$		45	65	mA
$+V_{DD}$		115	160	mA
$-V_{SS}$		160	200	mA
Power Dissipation		2.8	3.9	Watts

NOTES
[1]Integral linearity is inferred from FFT. Differential linearity is derived from histogram.
[2]FSR, full-scale range.
[3]Adjustable to zero.
[4]Noise based on small signal FFT excluding quantization noise.
[5]SNR fundamental to noise minus harmonics 2–9.
[6]THD includes harmonics 2–9 of the fundamental.
[7]Aperture delay is the time from the rising edge on the Hold Command Input to the opening of the switch in the Track/Hold.
[8]Guaranteed but not 100% production tested.
[9]Timing based on 10 MHz clock. Refer to Figures 13 and 14.
[10]Case to ambient temperature is assumed to be 30°C. The AD1382 case temperature will stabilize about 30°C above ambient while operating in free air without a heat sink. Factory calibration is done in this condition. See the application section for further information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to AGND . . . . . 18 V
$-V_S$ to AGND . . . . . −18 V
V_{DD} to PGND . . . . . 7 V
V_{SS} to PGND . . . . . −7 V
AGND to PGND . . . . . ±0.3 V
Analog Inputs . . . . . $\pm V_S$
Digital Inputs . . . . . −0.3 V to V_{DD} + 0.3 V
Output Short Circuit Duration
  Reference Output . . . . . Indefinite
  Track/Hold Output . . . . . 1 sec
  Digital Outputs . . . . . 1 sec for Any One Output
Ambient Temperature (Operating) . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AD1382 PIN CONNECTIONS

The AD1382 is housed in a 48-pin bottom-brazed ceramic bathtub package. The pinout is as follows:

PIN	FUNCTION	PIN	FUNCTION
1	CLOCK IN	48	V_{DD2} (+5 V POWER)
2	POWER GROUND	47	POWER GROUND
3	B1/B9 MSB	46	V_{SS2} (−5 V POWER)
4	B2/B10	45	AUTOZERO
5	B3/B11	44	B1 SELECT
6	B4/B12	43	POWER GROUND
7	B5/B13	42	POWER GROUND
8	B6/B14	41	DNC
9	B7/B15	40	GAIN ADJUST
10	B8/B16 LSB	39	+10 V REFERENCE OUT
11	V_{DD1} (+5 V SIGNAL)	38	$-V_{S1}$ (−15 V)
12	POWER GROUND	37	SIGNAL GROUND
13	V_{SS1} (−5 V SIGNAL)	36	$+V_{S1}$ (+15 V)
14	SIGNAL GROUND	35	SIGNAL GROUND
15	DATA STROBE	34	DNC
16	HI/LO BYTE SELECT	33	DNC
17	OE DATA ENABLE	32	+10 V REFERENCE IN
18	START CONVERT	31	V_{IN} B
19	HOLD COMMAND OUT	30	V_{IN} A
20	SIGNAL GROUND	29	OFFSET ADJUST
21	$+V_{S2}$ (+15 V)	28	DNC
22	HOLD COMMAND IN	27	TRACK/HOLD OUTPUT
23	$-V_{S2}$ (−15 V)	26	SIGNAL GROUND
24	POWER GROUND	25	TRACK/HOLD INPUT

DNC = DO NOT CONNECT

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD1382KD	10°C to 40°C Ambient (40°C to 70°C Case)	DH-48A

*DH-48A = Hermetic Ceramic DIP. For outline information see Package Information section.

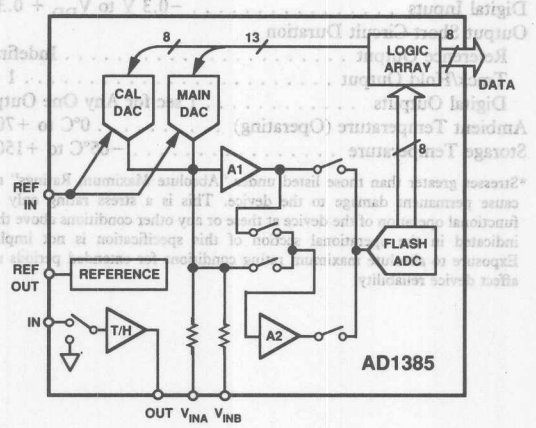
16-Bit 500 kHz Wide Temperature Range Sampling ADC

AD1385

PRODUCT FEATURES
16-Bit Resolution
500 kHz Sampling Rate
Differential Linearity Autocalibration
Specified over −55°C to +125°C Range
SNR 90 dB @ 100 kHz (min)
THD −88 dB @ 100 kHz (min)
0.0006% FSR DNL (typ)
0.0015% FSR INL (typ)
No Missing Codes
±5, ±10 V Bipolar Input Ranges
Zero Offset Autocalibration

APPLICATIONS
Medical Imaging
CAT
Magnetic Resonance
Radar
Vibration Analysis
Parametric Measurement Unit (ATE)
Digital Storage Oscilloscopes
Waveform Recorders
Analytical Instruments

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1385 is a complete 500 kHz, 16-bit, sampling analog-to-digital converter contained in a single package. Its differential linearity autocalibration feature allows this high resolution, high speed converter to offer outstanding noise and distortion performance, as well as excellent INL and DNL specifications, over the full military temperature range. Autocalibration effectively eliminates DNL drift over temperature.

The AD1385 architecture includes a low noise, low distortion track/hold, a three pass digitally corrected subranging ADC, and linearity calibration circuitry. A complete linearity calibration requires only 15 ms. Precision thin-film resistors and a proprietary DAC contribute to the part's outstanding dynamic and static performance.

The AD1385 uses four power supplies, ±5 V and ±15 V, and an external 10 MHz clock. Power dissipation is nominally 2.76 W. Two user selectable bipolar input ranges, ±5 V and ±10 V, are provided. Careful attention to grounding and a single package make it easy to design PCBs to achieve specified performance.

The AD1385's pinout is nearly identical to that of the AD1382, a factory calibrated 16-bit, 500 kHz SADC. Just two additional connections, to enable and monitor autocalibration, are required. This commonality provides an easy upgrade path to extend system performance and operating temperature range.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, V_{DD} = +5 V, V_{SS} = −5 V, 10 MHz External Clock, unless otherwise noted)

Parameter	AD1385KD Min	AD1385KD Typ	AD1385KD Max	AD1385TD Min	AD1385TD Typ	AD1385TD Max	Units
RESOLUTION	16			16			Bits
ANALOG INPUT							
Input Ranges		±5, ±10			±5, ±10		V
Input Impedance	2.45	2.5	2.55	2.45	2.5	2.55	kΩ
TRANSFER CHARACTERISTICS							
(Combined ADC/Track/Hold)							
Integral Nonlinearity[1, 2], T_{MIN} to T_{MAX}		±0.0015			±0.0015		% FSR[3]
Differential Nonlinearity[1]		±0.0006	±0.0015		±0.0006	±0.0015	% FSR
Drift, T_{MIN} to T_{MAX}		0.3			0.3		ppm/°C
Missing Codes, T_{MIN} to T_{MAX}			None			None	
Gain Error[4]		±0.05	±0.15		±0.05	±0.15	% FSR
Drift, T_{MIN} to T_{MAX}		8	15		8	15	ppm/°C
Bipolar Zero[4]		±0.05	±0.10		±0.05	±0.10	% FSR
Drift, T_{MIN} to T_{MAX}		5	15		5	15	ppm/°C
PSRR		±0.006	±0.10		±0.006	±0.10	% FSR/V
Noise		70			70		μV RMS
DYNAMIC CHARACTERISTICS[2]							
±5 V FSR, V_{IN} = −0.4 dB, T_{MIN} to T_{MAX}							
Sample Rate			500			500	kHz
Signal-to-Noise Ratio[5]							
f = 5 kHz	90	93		90	93		dB
f = 100 kHz	90	92		90	92		dB
f = 200 kHz	88	91		88	91		dB
Peak Distortion							
f = 5 kHz	−90	−107		−90	−107		dB
f = 100 kHz	−88	−95		−88	−95		dB
f = 200 kHz	−82	−88		−82	−88		dB
Total Harmonic Distortion[6]							
f = 5 kHz	−90	−105		−90	−105		dB
f = 100 kHz	−88	−95		−88	−95		dB
f = 200 kHz	−82	−88		−82	−88		dB
DYNAMIC CHARACTERISTICS[2]							
±10 V FSR, V_{IN} = −0.4 dB, T_{MIN} to T_{MAX}							
Sample Rate			500			500	kHz
Signal-to-Noise Ratio[5]							
f = 5 kHz	90	95		90	95		dB
f = 100 kHz	90	94		90	94		dB
f = 200 kHz	88	93		88	93		dB
Peak Distortion							
f = 5 kHz	−90	−108		−90	−108		dB
f = 100 kHz	−80	−87		−80	−87		dB
f = 200 kHz	−74	−82		−74	−82		dB
Total Harmonic Distortion[6]							
f = 5 kHz	−90	−105		−90	−105		dB
f = 100 kHz	−80	−87		−80	−87		dB
f = 200 kHz	−74	−82		−74	−82		dB
DIGITAL INPUTS							
Input Voltage							
V_{IL}			0.8			0.8	V
V_{IH}	2.25			2.25			V
Input Current			±200			±200	μA
Input Capacitance		2			2		pF
Clock							
Frequency		2.5–10			2.5–10		MHz
Duty Cycle		40–60			40–60		%
Aperture Delay[7]		7			7		ns
DIGITAL OUTPUTS							
Output Voltage							
V_{OL} @ I_{OL} = 3.2 mA		0.2	0.4		0.2	0.4	V
V_{OH} @ I_{OH} = −3.2 mA	2.4	4.5		2.4	4.5		V
Output Capacitance		4			4		pF
Leakage, Outputs Disabled			±200			±200	μA

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OUTPUT CODING	Complementary Offset Binary or Complementary Twos Complement						
INTERNAL REFERENCE							
Voltage	9.990		10.010	9.990		10.010	V
Current	2	5		2	5		mA
Drift		5	15		5	15	ppm/°C
TEMPERATURE RANGE, CASE							
Specified	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	°C
POWER REQUIREMENTS							
Specified Operating Range							
$\pm V_S$	14.25		15.75	14.25		15.75	V
$+V_{DD}$	4.75		5.25	4.75		5.25	V
$-V_{SS}$	−5.25		−4.75	−5.25		−4.75	V
Current Drains							
$+V_S$		52	80		52	80	mA
$-V_S$		48	75		48	75	mA
$+V_{DD}$		104	160		104	160	mA
$-V_{SS}$		148	200		148	200	mA
Power Dissipation		2.76	4.125		2.76	4.125	Watts

NOTES
[1]Integral linearity is inferred from FFTs. Differential linearity is derived from histograms.
[2]Performance over temperature is specified at the temperature at which the last calibration was performed.
[3]FSR = Full-Scale Range.
[4]Adjustable to zero.
[5]SNR excludes harmonics 2–9 of the fundamental.
[6]THD includes harmonics 2–9 of the fundamental.
[7]Aperture delay is the time from the rising edge on the Hold Command Input to the opening of the switch in the Track/Hold.
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1, 2] (T_A = −55°C to +125°C, V_S = ±15 V, V_{DD} = +5 V, V_{SS} = −5 V)

Parameter	Design Minimum	Typ	Unit	Description
START COMMAND				
t_{SCS}	10		ns	Setup Time
t_{SCH}	10		ns	Hold Time
AUTOZERO				
t_{AZS}	10		ns	Setup Time
t_{AZH}	20		ns	Hold Time
DATA VALID				
t_{DVS}		1.5	CP[3]	Setup Time
t_{DVH}		0.5	CP[3]	Hold Time
HOLD COMMAND				
t_H		13	CP[3]	Hold Time
t_D		7	ns	Delay Time
DATA STROBE				
t_{DS}		2	CP[3]	Pulse Width
t_{DSD}		16.5	CP[3]	Delay
CALIBRATE PULSE WIDTH	20		ns	
CALIBRATION STATUS		15	ms	Duration

NOTE
[1]Refer to Figures 17, 18 and 24.
[2]Design minimums are derived from worst case design analysis and/or simulation results. Typical values are based on characterization data. These specifications are not guaranteed or tested.
[3]The time duration for this parameter varies in direct proportion to the width of the Clock Pulse (CP).

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to AGND . . . . . 18 V
$-V_S$ to AGND . . . . . −18 V
V_{DD} to PGND . . . . . 7 V
V_{SS} to PGND . . . . . −7 V
AGND to PGND . . . . . ±0.3 V
Analog Inputs . . . . . $\pm V_S$
Reference Input . . . . . 0 V to +11 V
Digital Inputs . . . . . −0.3 V to V_{DD} + 0.3 V
Output Short Circuit Duration
  Reference Output . . . . . Indefinite
  Track/Hold Output . . . . . 1 sec
  Digital Outputs . . . . . 1 sec for Any One Output
Case Temperature (Operating) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range (Case)	Package Option*
AD1385KD	0°C to +70°C	DH-48A
AD1385TD	−55°C to +125°C	DH-48A
AD1385TD/883B	−55°C to +125°C	DH-48A

*DH-48A = Bottom Brazed Ceramic DIP. For outline information see Package Information section.

AD1385 PIN CONNECTIONS

The AD1385 is housed in a 48-pin bottom-brazed ceramic bathtub package. The pinout is as follows:

Pin	Function	Pin	Function
1	CLOCK IN	48	V_{DD2} (+5 V POWER)
2	POWER GROUND	47	POWER GROUND
3	B1/B9 (MSB)	46	V_{SS2} (−5 V POWER)
4	B2/B10	45	AUTOZERO
5	B3/B11	44	B1 SELECT
6	B4/B12	43	POWER GROUND
7	B5/B13	42	POWER GROUND
8	B6/B14	41	$\overline{CAL}$
9	B7/B15	40	GAIN ADJUST
10	B8/B16 (LSB)	39	+10 V REFERENCE OUT
11	V_{DD1} (+5 V SIGNAL)	38	$-V_{S1}$ (−15 V)
12	POWER GROUND	37	SIGNAL GROUND
13	V_{SS1} (−5 V SIGNAL)	36	$+V_{S1}$ (+15 V)
14	SIGNAL GROUND	35	SIGNAL GROUND
15	DATA STROBE	34	DNC
16	HI/LO BYTE SELECT	33	DNC
17	$\overline{OE}$ DATA ENABLE	32	+10 V REFERENCE IN
18	START CONVERT	31	V_{IN} B
19	HOLD COMMAND OUT	30	V_{IN} A
20	SIGNAL GROUND	29	OFFSET ADJUST
21	$+V_{S2}$ (+15 V)	28	CAL STATUS
22	HOLD COMMAND IN	27	TRACK/HOLD OUTPUT
23	$-V_{S2}$ (−15 V)	26	SIGNAL GROUND
24	POWER GROUND	25	TRACK/HOLD INPUT

DNC = DO NOT CONNECT

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

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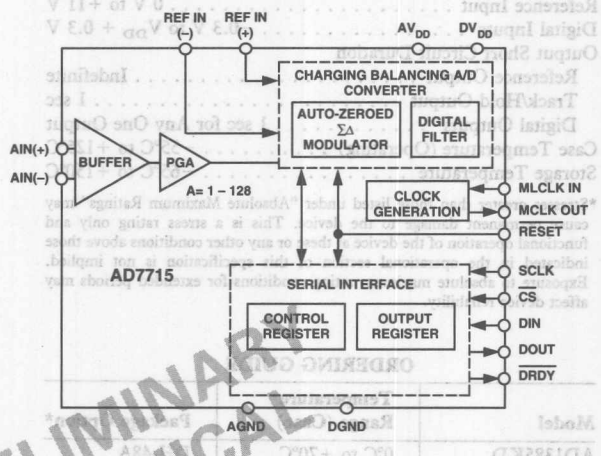
3 V/5 V, Low Cost, Low Power, 16-Bit, Sigma-Delta ADC

AD7715*

FEATURES
Charge-Balancing ADC
16 Bits No Missing Codes
0.0015% Nonlinearity
Programmable Gain Front End
Gains of 1, 2, 32 and 128
Differential Input Capability
Three-Wire Serial Interface
Ability to Buffer the Analog Input
3 V or 5 V Single Supply Operation
Low Supply Current: 500 µA max @ 3 V Supplies
Low-Pass Filter with Programmable Output Update
16-Pin SOIC/DIP

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7715 is a complete analog front end for low frequency measurement applications. The part can accept low level input signals directly from a transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 16 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and output update rate.

The AD7715 features a differential analog input as well as a differential reference input. It operates from a single supply (+3 V or +5 V). It can handle unipolar input signal ranges of 0 mV to +20 mV, 0 mV to +80 mV, 0 V to +1.25 V and 0 V to +2.5 V. It can also handle bipolar input signal ranges of ±20 mV, ±80 mV, ±1.25 V and ±2.5 V. These bipolar ranges are referenced to the negative input of the differential analog input. The AD7715 thus performs all signal conditioning and conversion for a single-channel system.

The AD7715 is ideal for use in smart, microcontroller or DSP based systems. It features a serial interface which can be configured for three-wire operation. Gain settings, signal polarity and update rate selection can be configured in software using the input serial port. The part contains self-calibration and system calibration options to eliminate gain and offset errors on the part itself or in the system.

CMOS construction ensures very low power dissipation and the power-down mode reduces the standby power consumption to 50 µW typ. The part is available in a 16-pin, 0.3 inch-wide, plastic and hermetic dual-in-line package (DIP) as well as a 16-lead small outline (SOIC) package.

***Protected by U.S. Patent No. 5,134,401.**

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. The AD7715 consumes less than 500 µA in total supply current at 3 V supplies and 1 MHz master clock, making it ideal for use in low-power systems. Standby current is less than 10 µA.
2. The programmable gain input allows the AD7715 to accept input signals directly from a strain gage or transducer removing a considerable amount of signal conditioning.
3. The AD7715 is ideal for microcontroller or DSP processor applications with a three-wire serial interface reducing the number of interconnect lines and reducing the number of opto-couplers required in isolated systems. The part contains an on-chip registers which allow software control over output update rate, input gain, signal polarity and calibration modes.
4. The part features excellent static performance specifications with 16-bit No Missing Codes, ±0.0015% accuracy and low rms noise (<450 nV). Endpoint errors and the effects of temperature drift are eliminated by on-chip self-calibration, which removes zero-scale and full-scale errors.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7715-5–SPECIFICATIONS

(AV_{DD} = +5 V, DV_{DD} = +3 V or +5 V, REF IN(+) = +2.5 V; REF IN(–) = AGND; $f_{CLK\ IN}$ = 2.4576 MHz unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	16	Bits min	Guaranteed by Design, for Filter Notches of 50, 60 Hz
Output Noise	See Tables III & IV		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.0015	% of FSR max	Filter Notches ≤ 60 Hz
Unipolar Offset Error[2]	See Note 3		
Unipolar Offset Drift[4]	2.5/GAIN	μV/°C typ	For Gains of 1 and 2
	0.3	μV/°C typ	For Gains of 32 and 128
Bipolar Zero Error[2]	See Note 3		
Bipolar Zero Drift[4]	2.5/GAIN	μV/°C typ	For Gains of 1 and 2
	0.3	μV/°C typ	For Gains of 32 and 128
Positive Full-Scale Error[2, 5]	See Note 3		
Full-Scale Drift[4, 6]	3/GAIN	μV/°C typ	For Gains of 1 and 2
	0.35	μV/°C typ	For Gains of 32 and 128
Gain Error[2, 7]	See Note 3		
Gain Drift[4, 8]	2	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error[2]	±0.0015	% of FSR max	Typically ±0.0004%
Bipolar Negative Full-Scale Drift[4]	4/GAIN	μV/°C typ	For Gains of 1 and 2
	0.5	μV/°C typ	For Gains of 32 and 128
ANALOG INPUTS/REFERENCE INPUTS			
Common-Mode Rejection (CMR)	100	dB min	At DC
Absolute/Common-Mode Range[9]	AGND to AV_{DD}	V min to V max	
Absolute/Common-Mode Range[9]	AGND + 50 mV to AV_{DD} – 1.5 V	V min to V max	Analog Inputs with BUF Bit of Setup Register = 1
Normal-Mode 50 Hz Rejection[10]	100	dB min	Filter Notch = 50 Hz (or 25 Hz with $f_{CLK\ IN}$ = 1 MHz)
Normal-Mode 60 Hz Rejection[10]	100	dB min	Filter Notch = 60 Hz (or 20 Hz with $f_{CLK\ IN}$ = 1 MHz)
Common-Mode 50 Hz Rejection[10]	150	dB min	Filter Notch = 50 Hz (or 25 Hz with $f_{CLK\ IN}$ = 1 MHz)
Common-Mode 60 Hz Rejection[10]	150	dB min	Filter Notch = 60 Hz (or 20 Hz with $f_{CLK\ IN}$ = 1 MHz)
Input Current[10]	1	nA max	BUF Bit of Setup Register = 1
DC Input Leakage Current[10]			BUF Bit of Setup Register = 0
@ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[10]	10	pF max	
Analog Inputs[11]			
Input Voltage Range[12]	0 to $+V_{REF}$/GAIN[13]	nom	Unipolar Input Range (B/U Bit of Setup Register = 1)
	$\pm V_{REF}$/GAIN	nom	Bipolar Input Range (B/U Bit of Setup Register = 0)
Input Sampling Rate, f_S	GAIN × $f_{CLK\ IN}$/128		For Gains of 1 and 2
	$f_{CLK\ IN}$/16		For Gains of 32 and 128
Reference Inputs			
REF IN(+) – REF IN(–) Voltage	+2.5	V nom	±5% for Specified Performance. Part Functions with Lower V_{REF} Voltages
Input Sampling Rate, f_S	$f_{CLK\ IN}$/128		
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = +5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = +3 V
V_{INH}, Input High Voltage	3.5	V min	DV_{DD} = +5 V
V_{INH}, Input High Voltage	2.5	V min	DV_{DD} = +3 V
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 800 μA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 μA. DV_{DD} = +5 V
V_{OH}, Output High Voltage	DV_{DD} – 0.4	V min	I_{SOURCE} = 200 μA. DV_{DD} = +3 V
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[14]	9	pF typ	

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	16	Bits min	Guaranteed by Design for Filter Notches of 50, 60 Hz
Output Noise	See Tables V & VI		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.003	% of FSR max	Filter Notches ≤ 60 Hz
Unipolar Offset Error[2]	See Note 3		
Unipolar Offset Drift[4]	2.5/GAIN	µV/°C typ	For Gains of 1 and 2
	0.3	µV/°C typ	For Gains of 32 and 128
Bipolar Zero Error[2]	See Note 3		
Bipolar Zero Drift[4]	2.5/GAIN	µV/°C typ	For Gains of 1 and 2
	0.3	µV/°C typ	For Gains of 32 and 128
Positive Full-Scale Error[2, 5]	See Note 3		For System Calibration @ All Gains and Self-Calibration @ Gains of 1 and 2
Positive Full-Scale Error[2, 5]	±0.01	% of FSR max	For Self-Calibration @ Gains of 32 and 128
Full-Scale Drift[4, 6]	3/GAIN	µV/°C typ	For Gains of 1 and 2
	0.35	µV/°C typ	For Gains of 32 and 128
Gain Error[2, 7]	See Note 3		
Gain Drift[4, 8]	2	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error[2]	±0.003	% of FSR max	Typically ±0.0004%
Bipolar Negative Full-Scale Drift[4]	4/GAIN	µV/°C typ	For Gains of 1 and 2
	0.5	µV/°C typ	For Gains of 32 and 128
ANALOG INPUTS/REFERENCE INPUTS			
Common-Mode Rejection (CMR)	94	dB min	At DC
Absolute/Common-Mode Range[6]	AGND to AV_{DD}	V min to V max	
Absolute/Common-Mode Range[6]	AGND + 50 mV to AV_{DD} – 1.5 V	V min to V max	Analog Inputs with BUF Bit of Setup Register = 1
Normal-Mode 50 Hz Rejection[7]	100	dB min	Filter Notches = 50 Hz (or 25 Hz with $f_{CLK\ IN}$ = 1 MHz)
Normal-Mode 60 Hz Rejection[7]	100	dB min	Filter Notches = 60 Hz (or 20 Hz with $f_{CLK\ IN}$ = 1 MHz)
Common-Mode 50 Hz Rejection[7]	150	dB min	Filter Notches = 50 Hz (or 25 Hz with $f_{CLK\ IN}$ = 1 MHz)
Common-Mode 60 Hz Rejection[7]	150	dB min	Filter Notches = 60 Hz (or 20 Hz with $f_{CLK\ IN}$ = 1 MHz)
Input Current[7]	1	nA max	BUF Bit of Setup Register = 1
DC Input Leakage Current[7]			BUF Bit of Setup Register = 0
@ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[7]	10	pF max	
Analog Inputs[8]			
Input Voltage Range[9]	0 to $+V_{REF}$/GAIN[10]	nom	Unipolar Input Range (B/U Bit of Setup Register = 1)
	$\pm V_{REF}$/GAIN	nom	Bipolar Input Range (B/U Bit of Setup Register = 0)
Input Sampling Rate, f_S	GAIN × $f_{CLK\ IN}$/128		For Gains of 1 and 2
	$f_{CLK\ IN}$/16		For Gains of 32 and 128
Reference Inputs			
REF IN(+) – REF IN(–) Voltage	+1.25	V nom	±5% for Specified Performance. Part Functions with Lower V_{REF} Voltages
Input Sampling Rate, f_S	$f_{CLK\ IN}$/128		
LOGIC INPUTS			
Input Current	±10	µA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.4	V max	
V_{INH}, Input High Voltage	2.5	V min	
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.2	V max	I_{SINK} = 800 µA
V_{OH}, Output High Voltage	DV_{DD} – 0.4	V min	I_{SOURCE} = 200 µA
Floating State Leakage Current	±10	µA max	
Floating State Output Capacitance[11]	9	pF typ	

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SPECIFICATIONS

(AV_{DD} = +3 V to +5 V, DV_{DD} = +3 V to +5 V, REF IN(+) = +1.25 V (AD7715-3) or +2.5 V (AD7715-5); REF IN(–) = AGND; MCLK IN =1 MHz to 2.4576 MHz unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version	Units	Conditions/Comments
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[15]	$(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1, 2, 32 or 128)
Negative Full-Scale Calibration Limit[15]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1, 2, 32 or 128)
Offset Calibration Limit[16]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1, 2, 32 or 128)
Input Span[16]	$0.8 \times V_{REF}/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1, 2, 32 or 128)
	$(2.1 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1, 2, 32 or 128)
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage (AD7715-3)	+2.7 to +3.6	V nom	For Specified Performance
AV_{DD} Voltage (AD7715-5)	+5	V nom	±5% for Specified Performance
DV_{DD} Voltage	+2.7 to +5.25	V nom	For Specified Performance. AV_{DD} must be ≥ DV_{DD}
Power Supply Currents			
AV_{DD} Current			AV_{DD} = 3 V or 5 V. Gain = 1 to 128 (f_{CLKIN} = 1 MHz) or Gain = 1 or 2 (f_{CLKIN} = 2.4576 MHz)
	0.3	mA max	Typically 0.2 mA. BUF Bit of Setup Register = 0
	0.6	mA max	Typically 0.4 mA. BUF Bit of Setup Register = 1
			AV_{DD} = 3 V or 5 V. Gain = 32 or 128 (f_{CLKIN} = 2.4576 MHz)[17]
	0.5	mA max	Typically 0.3 mA. BUF Bit of Setup Register = 0
	1	mA max	Typically 0.8 mA. BUF Bit of Setup Register = 1
DV_{DD} Current			Digital I/Ps = 0 V or DV_{DD}
	0.2	mA max	Typically 0.15 mA. DV_{DD} = 3 V. $f_{CLK\ IN}$ = 1 MHz
	0.4	mA max	Typically 0.3 mA. DV_{DD} = 5 V. $f_{CLK\ IN}$ = 1 MHz
	0.5	mA max	Typically 0.4 mA. DV_{DD} = 3 V. $f_{CLK\ IN}$ = 2.4576 MHz
	1	mA max	Typically 0.8 mA. DV_{DD} = 5 V. $f_{CLK\ IN}$ = 2.4576 MHz
Power Supply Rejection[18] (AV_{DD})	See Note 19	dB typ	
Normal Mode Power Dissipation			AV_{DD} = DV_{DD} = +3 V. Digital I/Ps = 0 V or DV_{DD}
	1.5	mW max	BUF Bit = 0. All Gains 1 MHz Clock, Gain 1 and 2 @ 2.4576 MHz
	2.4	mW max	BUF Bit = 1. All Gains 1 MHz Clock, Gain 1 and 2 @ 2.4576 MHz
	3	mW max	BUF Bit = 0. Gain = 32 or 128 @ f_{CLKIN} = 2.4576 MHz
	4.5	mW max	BUF Bit = 1. Gain = 32 or 128 @ f_{CLKIN} = 2.4576 MHz
Normal Mode Power Dissipation			AV_{DD} = DV_{DD} = +5 V. Digital I/Ps = 0 V or DV_{DD}
	3.5	mW max	BUF Bit = 0. All Gains 1 MHz Clock, Gain 1 and 2 @ 2.4576 MHz
	5	mW max	BUF Bit = 1. All Gains 1 MHz Clock, Gain 1 and 2 @ 2.4576 MHz
	7.5	mW max	BUF Bit = 0. Gain = 32 or 128 @ f_{CLKIN} = 2.4576 MHz
	10	mW max	BUF Bit = 1. Gain = 32 or 128 @ f_{CLKIN} = 2.4576 MHz
Standby (Power-Down) Dissipation	100	μW max	Typically 50 μW. STBY Bit of Setup Register = 1

NOTES

[1]Temperature ranges are as follows: A Version, –40°C to +85°C.

[2]Applies after calibration at the temperature of interest.

[3]These errors will be of the order of the output noise of the part as shown in Tables III to VI.

[4]Recalibration at any temperature will remove these drift errors.

[5]Positive Full-Scale Error includes Zero-Scale Errors (Unipolar Offset Error or Bipolar Zero Error) and applies to both unipolar and bipolar input ranges.

[6]Full-Scale Drift includes Zero-Scale Drift (Unipolar Offset Drift or Bipolar Zero Drift) and applies to both unipolar and bipolar input ranges.

[7]Gain Error does not include Zero-Scale Errors. It is calculated as Full-Scale Error—Unipolar Offset Error for unipolar ranges and Full Scale Error—Bipolar Zero Error for bipolar ranges.

[8]Gain Drift does not include Unipolar Offset Drift/Bipolar Zero Drift. It is effectively the drift of the part if zero scale calibrations only were performed.

[9]This common-mode voltage range is allowed provided that the input voltage on AIN(+) or AIN(–) does not go more positive than AV_{DD} + 30 mV or go more negative than AGND –30 mV.

[10]These numbers are guaranteed by design and/or characterization.

[11]The analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance depends on the selected gain.

[12]The analog input voltage range on AIN(+) is given here with respect to the voltage on AIN(–). The absolute voltage on the analog inputs should go more positive than go more positive than AV_{DD} + 30 mV or go more negative than AGND – 30 mV.

[13]V_{REF} = REFIN(+) – REFIN(–).

[14]Sample tested at +25°C to ensure compliance.

[15]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale then the device will output all 0s.

[16]These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed AV_{DD} + 30 mV or go more negative than AGND – 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

[17]Assumes CLK bit of Setup Register is set to correct status corresponding to the master clock frequency.

[18]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 5, 10, 25 or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 6, 10, 30 or 60 Hz.

[19]PSRR depends on gain: Gain of 1: 70 dB typ; Gain of 2: 75 dB typ; Gains of 32 and 128: 85 dB typ.

Specifications subject to change without notice.

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PRELIMINARY TECHNICAL DATA

TIMING CHARACTERISTICS[1, 2]

(DV_{DD} = +3 V to +5 V ± 5%; AV_{DD} = +3 V or +5 V ± 5%; AGND = DGND = 0 V; f_{CLKIN} = 2.4576 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD} unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (A Version)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	Master Clock Frequency: Crystal Oscillator or Externally Supplied
	2.5	MHz max	for Specified Performance
$t_{CLK\ IN\ LO}$	0.4 × $t_{CLK\ IN}$	ns min	Master Clock Input Low Time. $t_{CLK\ IN}$ = 1/$f_{CLK\ IN}$
$t_{CLK\ IN\ HI}$	0.4 × $t_{CLK\ IN}$	ns min	Master Clock Input High Time
t_r[5]	50	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	50	ns max	Digital Output Fall Time. Typically 20 ns
t_1	500 × $t_{CLK\ IN}$	ns nom	$\overline{DRDY}$ High Time
t_2	1000	ns min	$\overline{RESET}$ Pulse Width
Read Operation			
t_3	0	ns min	$\overline{DRDY}$ to $\overline{CS}$ Setup Time
t_4	20	ns min	$\overline{CS}$ Falling Edge to SCLK Falling Edge Setup Time
t_5[6]	0	ns min	SCLK Falling Edge to Data Valid Delay
	20	ns max	DV_{DD} = +5 V
	40	ns max	DV_{DD} = +3 V
t_6	200	ns min	SCLK High Pulse Width
t_7	200	ns min	SCLK Low Pulse Width
t_8	20	ns min	$\overline{CS}$ Rising Edge to SCLK Rising Edge Hold Time
t_9[7]	10	ns min	Bus Relinquish Time after SCLK Rising Edge.
	50	ns max	DV_{DD} = +5 V
	100	ns max	DV_{DD} = +3 V
t_{10}	50	ns max	SCLK Rising Edge to $\overline{DRDY}$ High[8]
Write Operation			
t_{11}	20	ns min	$\overline{CS}$ Falling Edge to SCLK Falling Edge Setup Time
t_{12}	30	ns min	Data Valid to SCLK Falling Edge Setup Time
t_{13}	20	ns min	Data Valid to SCLK Falling Edge Hold Time
t_{14}	200	ns min	SCLK High Pulse Width
t_{15}	200	ns min	SCLK Low Pulse Width
t_{16}	20	ns min	$\overline{CS}$ Rising Edge to SCLK Rising Edge Hold Time

PRELIMINARY TECHNICAL DATA

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.

[2]See Figures 2 and 3.

[3]CLKIN Duty Cycle range is 45% to 55%. CLKIN must be supplied whenever the AD7715 is not in Standby mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7715 is production tested with f_{CLKIN} at 2.4576 MHz (1 MHz for some I_{DD} tests). It is guaranteed by characterization to operate at 400 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

[7]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 100 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

[8]$\overline{DRDY}$ returns high after the first read from the device after an output update. The same data can be read again, if required, while $\overline{DRDY}$ is high although care should be taken that subsequent reads do not occur close to the next output update.

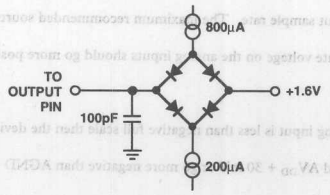

Figure 1. Load Circuit for Access Time and Bus Relinquish

ORDERING GUIDE

Model	AV_{DD} Supply	Temperature Range	Package Option*
AD7715AN-5	5 V	–40°C to +85°C	N-16
AD7715AR-5	5 V	–40°C to +85°C	R-16
AD7715AN-3	3 V	–40°C to +85°C	N-16
AD7715AR-3	3 V	–40°C to +85°C	R-16

*N = Plastic DIP; R = SOIC. For outline information see Package Information section.

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ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
AV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND ..... –0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND ..... –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
  Commercial (A Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 105°C/W
  Lead Temperature (Soldering, 10 sec) ..... +260°C
SOIC Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C
Power Dissipation (Any Package) to +75°C ..... 450 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PRELIMINARY TECHNICAL DATA

TERMINOLOGY

INTEGRAL NONLINEARITY

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full-scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

POSITIVE FULL-SCALE ERROR

Positive full-scale error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal AIN(+) voltage (AIN(–) + V_{REF}/GAIN – 3/2 LSBs). It applies to both unipolar and bipolar analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar offset error is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(–) + 0.5 LSB) when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal AIN(+) voltage (AIN(–) – 0.5 LSB) when operating in the bipolar mode.

GAIN ERROR

This is a measure of the span error of the ADC. It includes full-scale errors but not zero-scale errors. For unipolar input ranges it is defined as (full-scale error–unipolar offset error) while for bipolar input ranges it is defined as (full-scale error–bipolar zero error).

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(–) – V_{REF}/GAIN + 0.5 LSB) when operating in the bipolar mode.

POSITIVE FULL-SCALE OVERRANGE

Positive full-scale overrange is the amount of overhead available to handle input voltages on AIN(+) input greater than AIN(–) + V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages on AIN(+) below AIN(–) – V_{REF}/GAIN without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks even in the unipolar mode provided that AIN(+) is greater than AIN(–) and greater than AGND – 30 mV.

OFFSET CALIBRATION RANGE

In the system calibration modes, the AD7715 calibrates its offset with respect to the analog input. The offset calibration range specification defines the range of voltages that the AD7715 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7715 can accept in the system calibration mode and still calibrate full scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7715's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7715 can accept and still calibrate gain accurately.

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Mnemonic	Function
SCLK	Serial Clock. Logic Input. An external serial clock is applied to this input to access serial data from the AD7715. This serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7715 in smaller batches of data.
MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal or external clock. A crystal can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The clock input frequency is nominally either 2.5 MHz or 1 MHz.
MCLK OUT	When the master clock for the device is a crystal, the crystal is connected between MCLK IN and MCLK OUT. Note, the on-chip clock signal is not available at this pin.
$\overline{\text{RESET}}$	Logic Input. Active low input which resets the control logic, interface logic, digital filter and analog modulator of the part to power-on status.
AIN(+)	Analog Input. Positive input of the programmable gain differential analog input to the AD7715.
AIN(–)	Analog Input. Negative input of the programmable gain differential analog input to the AD7715.
AV_{DD}	Analog Positive Supply Voltage, +3 V nominal (AD7715-3) or +5 V nominal (AD7715-5).
REF IN(–)	Reference Input. Negative input of the differential reference input to the AD7715. The REF IN(–) can lie anywhere between AV_{DD} and AGND provided REF IN(+) is greater than REF IN(–).
REF IN(+)	Reference Input. Positive input of the differential reference input to the AD7715. The reference input is differential with the provision that REF IN(+) must be greater than REF IN(–). REF IN(+) can lie anywhere between AV_{DD} and AGND.
AGND	Ground reference point for analog circuitry.
$\overline{\text{CS}}$	Chip Select. Active low Logic Input used to select the AD7715. With this input hard-wired low, the AD7715 can operate in its three-wire interface mode with SCLK, DIN and DOUT used to interface to the device. $\overline{\text{CS}}$ can be used to select the device in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the AD7715.
$\overline{\text{DRDY}}$	Logic Output. A logic low on this output indicates that a new output word is available from the AD7715 data register. The $\overline{\text{DRDY}}$ pin will return high upon completion of a read operation of a full output word. If no data read has taken place, after an output update, the $\overline{\text{DRDY}}$ line will return high for 500 × $t_{CLK\ IN}$ cycles prior to the next output update. This gives an indication of when a read operation should not be attempted to avoid reading from the data register as it is being updated. $\overline{\text{DRDY}}$ is also used to indicate when the AD7715 has completed its on-chip calibration sequence.
DOUT	Serial Data Output with serial data being read from the output shift register on the part. This output shift register can contain information from the calibration registers, mode register, communications register, filter selection registers or data register depending on the register selection bits of the communications register.
DIN	Serial Data Input with serial data being written to the input shift register on the part. Data from this input shift register is transferred to the calibration registers, mode register, communications register or filter selection registers depending on the register selection bits of the communications register.
DV_{DD}	Digital Supply Voltage, +3 V or +5 V nominal.
DGND	Ground reference point for digital circuitry.

PRELIMINARY TECHNICAL DATA

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On-Chip Registers

The part contains four on-chip registers that can be accessed via the serial port on the part. The first of these is a communications register that decides whether the next operation is a read or write operation and also decides which register the read or write operation accesses The communication register also controls the standby mode and calibration modes of the part. The $\overline{DRDY}$ status is also available by reading from the communications register. All communication to any register on the device (including the data register) begins with a write to the communications register. The second register is a setup register that determines filter selection, gain setting and bipolar/unipolar operation. The third register is the data register from which the output data from the part is accessed. The final register is a test register which is accessed when testing the device. It is advised that the user does not attempt to access or change the contents of the test register as it may lead to unspecified operation of the device. The registers are discussed in mode detail in the following sections.

Communications Register (RS1, RS0 = 0, 0)

The communications register is an 8-bit register from which data can either be read or to which data can be written. On power-up or after a $\overline{RESET}$, the part is waiting for a write operation to the communications register. When the part has finished communicating with any of the other registers (either a read or write operation), it returns to the position of expecting a write to the communications register. This is the default state of the interface and in situations where the interface sequence is lost, if enough writes to the device (at least four bytes) take place with DIN high the part returns to its default state. Table I outlines the bit designations for the communications register.

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Table I. Communications Register

0/$\overline{DRDY}$	0	RS1	RS0	R/$\overline{W}$	STBY	MD1	MD0

0/$\overline{DRDY}$ For a read operation, this bit provides the status of the $\overline{DRDY}$ flag from the part. The status of this bit is the same as the $\overline{DRDY}$ output pin. For a write operation, a 0 must be written to this bit so that the write operation will be recognized by the register. If a 1 is written to the bit, the interface does not clock itself on and the part continues to sample this bit location, effectively waiting for a 0 before it will proceed to write any data to the communications register.

0 For a write operation, a 0 *must* be written to this bit for correct operation of the part. Failure to do this will result in unspecified operation of the device. For a read operation, a 0 will be read back from this bit location.

RS1–RS0 Register Selection Bits. These bits select to which one of four on-chip registers the next read or write operation takes place as follows. When the read or write to the selected register is complete, the part returns to where it is waiting for a write operation to the communications register. It does not remain in a state where it will continue to access the selected register.

RS1	RS0	Register	Register Size
0	0	Communications Register	8 Bit
0	1	Setup Register	8 Bit
1	0	Test Register	8 Bit
1	1	Data Register	16 Bit

R/$\overline{W}$ Read/Write Select. This bit selects whether the next operation is a read or write operation to the selected register. A 0 indicates a write cycle for the next operation to the appropriate register, while a 1 indicates a read operation from the appropriate register.

STBY Standby. Writing a 1 to this bit puts the part in its standby or power-down mode. In this mode, the part consumes only 50 µW of power. The part retains its calibration and control word information when in STANDBY. Writing a 0 to this bit places the part in its normal operating mode.

MD1	MD0	**Operating Mode**
0	0	Normal Mode; this is the normal mode of operation of the device whereby the device is performing normal conversions. This is the default condition of these bits after power-on or RESET.
0	1	Self-Calibration; this activates self-calibration on the part. This is a one step calibration sequence and when complete the part returns to normal mode. The $\overline{DRDY}$ output or bit indicates when this self-calibration is complete and a valid word is available in the data register. For this calibration type, the zero-scale calibration is done internally on shorted (zeroed) inputs and the full-scale calibration is done internally on V_{REF}.
1	0	Zero-Scale System Calibration; this activates zero-scale system calibration on the analog input. Calibration is performed on the analog input voltage provided at the analog input during this calibration sequence. The $\overline{DRDY}$ output or bit indicates when this zero-scale calibration is complete and the part returns to normal mode.
1	1	Full-Scale System Calibration; this activates full-scale system calibration on the analog input. Calibration is performed on the analog input voltage provided at the analog input during this calibration sequence. Once again, $\overline{DRDY}$ indicates when this full-scale calibration is complete. When this calibration is complete, the part returns to normal mode.

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Setup Register (RS1, RS0 = 0 , 1)

The setup register is an 8-bit register from which data can either be read or to which data can be written. This register controls the setup which the device is to operate in such as the gain, output rate, unipolar/bipolar operation etc. Table II outlines the bit designations for the mode register.

Table II. Setup Register

G1	G0	CLK	FS1	FS0	B/U	BUF	FSYNC

G2	G1	Gain Setting
0	0	1
0	1	2
1	0	32
1	1	128

CLK — Clock Bit. This bit should be set in accordance with the operating frequency of the AD7715. If the device has a master clock frequency of 2.4576 MHz, then this bit should be set to a 0. If the device has a master clock frequency of 1 MHz, then this bit should be set to a 1. This bit sets up the correct scaling currents for a given master clock and also chooses (along with FS1 and FS0) the output update rate for the device. If this bit is not set correctly for the master clock frequency of the device, then the device may not operate to specification.

FS1, FS0 — Filter Selection Bits. Along with the CLK bit, FS1 and FS0 determine the output update rate, filter first notch and –3 dB frequency as below. The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$) filter response. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device. Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables III through VI show the effect of the filter notch frequency and gain on the output noise and effective resolution of the part. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 500 Hz, a new word is available every 2 ms.

The settling time of the filter to a full-scale step input change is worst case 4 × 1/(output data rate). For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. If the first notch is at 500 Hz, the settling time of the filter to a full-scale input step is 8 ms max. This settling-time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with the $\overline{RESET}$ input low, the settling time will be 3 × 1/(output data rate) from when $\overline{RESET}$ returns high.

CLK	FS1	FS0	Output Update Rate	–3 dB Filter Cutoff
0	0	0	50 Hz	13.1 Hz
0	0	1	60 Hz	15.7 Hz
0	1	0	250 Hz	65.5 Hz
0	1	1	500 Hz	121 Hz
1	0	0	20 Hz	5.24 Hz
1	0	1	25 Hz	6.55 Hz
1	1	0	100 Hz	26.2 Hz
1	1	1	200 Hz	52.4 Hz

$\overline{B}$/U — Bipolar/Unipolar Operation. A 0 in this bit selects bipolar operation. This is the default (Power-On or $\overline{RESET}$) status of this bit. A 1 in this bit selects unipolar operation.

FSYNC — Filter Synchronization. When this bit is high, the nodes of the digital filter, the filter control logic and the calibration control logic are reset and the analog modulator is also held in its reset state. When this bit goes low, valid data is available in 3 × 1/(output update rate), i.e., the settling time of the filter.

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Test Register (RS1, RS0 = 1, 0)

The part contains a test register which is used in testing the device. The user is advised not to change the status of any of the bits in this register from the default (Power-On or RESET) status of all 0s as the part will be placed in one of its test modes and will not operate correctly. If the part enters one of its test modes, exercising RESET will exit the part from the mode.

Data Register (RS1, RS0 = 1, 1)

The data register on the part is a read-only register which contains the most up-to-date conversion result from the part. The register is 16 bits wide. If an attempt is made to write to this register, the data will not actually be written to any location of the part.

OUTPUT NOISE

AD7715-5

Table III shows the AD7715-5 output rms noise for the selectable notch and –3 dB frequencies for the part, as selected by FS1 and FS0 (see above). The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V. These numbers are typical and are generated at an analog input voltage of 0 V and for the BUF bit of the setup register = 0. Noise numbers for the two lower notch settings will typically be 10% higher than those in Table III for BUF Bit = 1.

Table IV meanwhile shows the output *peak-to-peak* noise for the selectable notch and –3 dB frequencies for the part. *It is important to note that these numbers represent the resolution for which there will be no code flicker. They are not calculated based on rms noise but on peak-to-peak noise.* The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V and for the BUF bit of the setup register = 0. These numbers are typical, are generated at an analog input voltage of 0 V and are rounded to the nearest LSB.

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Table III. Output RMS Noise vs. Gain and Output Update Rate for AD7715-5

Filter First Notch & O/P Data Rate		–3 dB Frequency		Typical Output RMS Noise in μV			
MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	GAIN = 1	GAIN = 2	GAIN = 32	GAIN = 128
50 Hz	20 Hz	13.1 Hz	5.24 Hz	7.5	3.8	0.5	0.45
60 Hz	25 Hz	15.72 Hz	6.55 Hz	8.5	4.1	0.5	0.45
250 Hz	100 Hz	65.5 Hz	26.2 Hz	130	75	4.0	1.7
500 Hz	200 Hz	131 Hz	52.4 Hz	600	260	25	8

Table IV. Effective (Peak-to-Peak) Resolution vs. Gain and Output Update Rate for AD7715-5

Filter First Notch & O/P Data Rate		–3 dB Frequency		Typical Effective Resolution in Bits			
MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	GAIN = 1	GAIN = 2	GAIN = 32	GAIN = 128
50 Hz	20 Hz	13.1 Hz	5.24 Hz	16	16	16	14
60 Hz	25 Hz	15.72 Hz	6.55 Hz	16	16	16	14
250 Hz	100 Hz	65.5 Hz	26.2 Hz	12	12	12	12
500 Hz	200 Hz	131 Hz	52.4 Hz	10	10	10	10

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

OUTPUT NOISE

AD7715-3

Table V shows the AD7715-3 output rms noise for the selectable notch and –3 dB frequencies for the part, as selected by FS1 and FS0 (see above). The numbers given are for the bipolar input ranges with a V_{REF} of +1.25 V and for the BUF bit of the setup register = 0. These numbers are typical and are generated at an analog input voltage of 0 V. Noise numbers for the two lower notch settings will typically be 10% higher than those in Table V for BUF Bit = 1.

Table VI meanwhile shows the output *peak-to-peak* noise for the selectable notch and -3 dB frequencies for the part. *It is important to note that these numbers represent the resolution for which there will be no code flicker. They are not calculated based on rms noise but on peak-to-peak noise.* The numbers given are for the bipolar input ranges with a V_{REF} of +1.25 V and for the BUF bit of the setup register = 0. These numbers are typical, are generated at an analog input voltage of 0 V and are rounded to the nearest LSB.

Table V. Output RMS Noise vs. Gain and Output Update Rate for AD7715-3

Filter First Notch & O/P Data Rate		–3 dB Frequency		Typical Output RMS Noise in μV			
MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	GAIN = 1	GAIN = 2	GAIN = 32	GAIN = 128
50 Hz	20 Hz	13.1 Hz	5.24 Hz	7.0	3.5	0.5	0.4
60 Hz	25 Hz	15.72 Hz	6.55 Hz	8.2	4.1	0.5	0.4
250 Hz	100 Hz	65.5 Hz	26.2 Hz	53	28	3.5	1.4
500 Hz	200 Hz	131 Hz	52.4 Hz	240	150	14	8

Table VI. Effective (Peak-to-Peak) Resolution vs. Gain and Output Update Rate for AD7715-3

Filter First Notch & O/P Data Rate		–3 dB Frequency		Typical Effective Resolution in Bits			
MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	MCLK IN = 2.4576 MHz	MCLK IN = 1 MHz	GAIN = 1	GAIN = 2	GAIN = 32	GAIN = 128
50 Hz	20 Hz	13.1 Hz	5.24 Hz	16	16	14	13
60 Hz	25 Hz	15.72 Hz	6.55 Hz	16	16	14	13
250 Hz	100 Hz	65.5 Hz	26.2 Hz	13	13	12	13
500 Hz	200 Hz	131 Hz	52.4 Hz	11	10	10	9

PRELIMINARY TECHNICAL DATA

CIRCUIT DESCRIPTION

The AD7715 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in industrial control or process control applications. It contains a sigma-delta (or charge-balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bidirectional serial communications port. The part consumes only 500 μA of power supply current, making it ideal for battery-powered or loop-powered instruments. The part comes in two versions, the AD7715-5 which is specified for operation from a +5 V analog supply (AV_{DD}) and the AD7715-3 which is specified for operation from a +3 V analog supply. The AD7715-5 can be operated with a digital supply (DV_{DD}) voltage of +3 V or +5 V.

The part contains a programmable gain fully differential analog input channel. The selectable gains on this input are 1, 2, 32 and 128 allowing the part to accept unipolar signals of between 0 mV to +20 mV and 0 V to +2.5 V or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals +2.5 V. With a reference voltage of +1.25 V, the input ranges are from 0 mV to +10 mV to 0 V to +1.25 V in unipolar mode and from ±10 mV to ±1.25 V in bipolar mode.

The input signal to the analog input is continuously sampled at a rate determined by the frequency of the master clock, MCLK IN, and the selected gain. A charge-balancing A/D converter (Sigma-Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma delta modulator with the input sampling frequency being modified to give the higher gains. A $sinc^3$ digital low-pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and hence its –3 dB frequency) can be programmed via the mode register bits FS0 and FS1. With a master clock frequency of 2.4576 MHz, the programmable range for this first notch frequency is from 50 Hz to 500 Hz giving a programmable range for the –3 dB frequency of 13.1 Hz to 131 Hz. With a master clock frequency of 1 MHz, the programmable range for this first notch frequency is from 20 Hz to 200 Hz giving a programmable range for the –3 dB frequency of 5.24 Hz to 52.4 Hz.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

DIGITAL INTERFACE

The part's serial interface can operate in three-wire mode by tying the $\overline{CS}$ input low. In this case, the SCLK, DIN and DOUT lines are used to communicate with the part and the status of $\overline{DRDY}$ can be obtained by interrogating the MSB of the communications register. $\overline{CS}$ can be used to decode the part in systems where a number of parts are connected to the serial bus. Figures 2 and 3 show timing diagrams for interfacing to the part with $\overline{CS}$ used to decode the part. Figure 2 is for a read operation from the part's output shift register while Figure 3 shows a write operation to the input shift register.

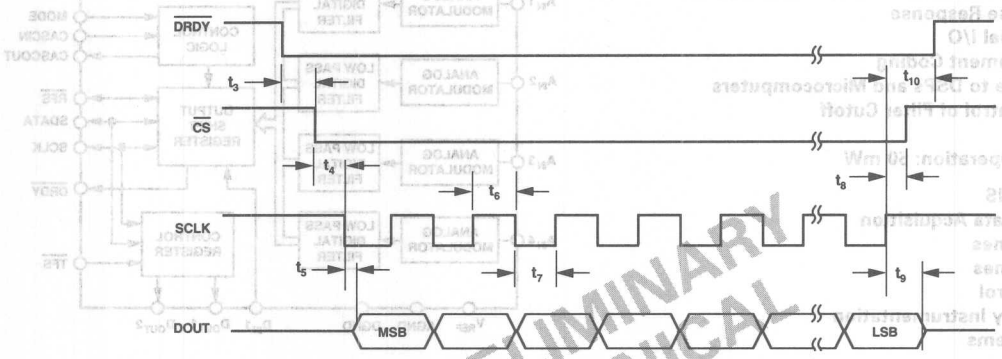


Figure 2. Read Cycle Timing Diagram

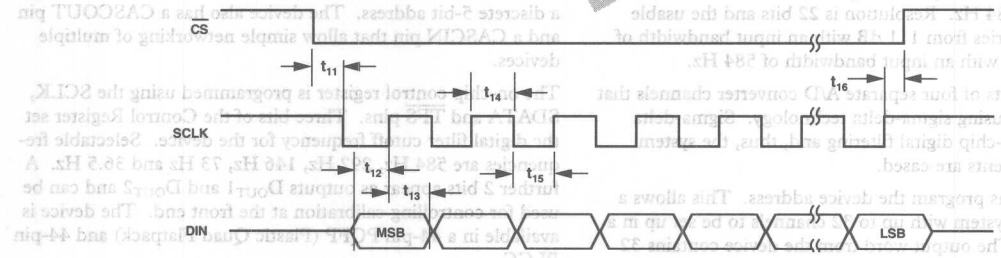


Figure 3. Write Cycle Timing Diagram

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

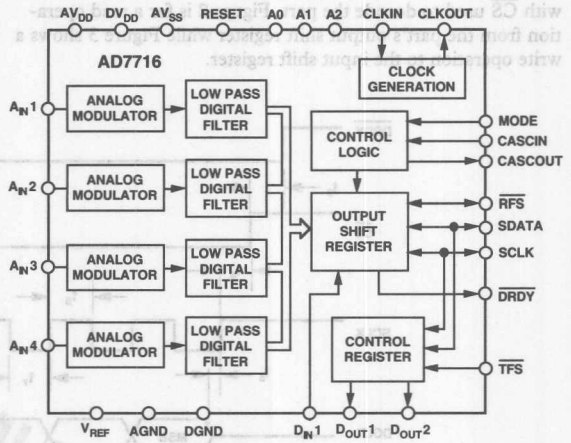
FEATURES

- 22-Bit Sigma-Delta ADC
  - Dynamic Range of 105 dB (146 Hz Input)
  - ±0.003% Integral Nonlinearity
- On-Chip Low-Pass Digital Filter
  - Cutoff Programmable from 584 Hz to 36.5 Hz
  - Linear Phase Response
- Five Line Serial I/O
- Twos Complement Coding
- Easy Interface to DSPs and Microcomputers
- Software Control of Filter Cutoff
- ±5 V Supply
- Low Power Operation: 50 mW

APPLICATIONS

- Biomedical Data Acquisition
  - ECG Machines
  - EEG Machines
- Process Control
- High Accuracy Instrumentation
- Seismic Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7716 is a signal processing block for data acquisition systems. It is capable of processing four channels with bandwidths of up to 584 Hz. Resolution is 22 bits and the usable dynamic range varies from 111 dB with an input bandwidth of 36.5 Hz to 99 dB with an input bandwidth of 584 Hz.

The device consists of four separate A/D converter channels that are implemented using sigma-delta technology. Sigma-delta ADCs include on-chip digital filtering and, thus, the system filtering requirements are eased.

Three address pins program the device address. This allows a data acquisition system with up to 32 channels to be set up in a simple fashion. The output word from the device contains 32 bits of data. One bit is determined by the state of the $D_{IN}1$ input and may be used, for example, in an ECG system with an external pacemaker detect circuit to indicate that the output word is invalid because of the presence of a pacemaker pulse. There are 22 bits of data corresponding to the analog input. Two bits contain the channel address and 3 bits are the device address. Thus, each channel in a 32-channel system would have a discrete 5-bit address. The device also has a CASCOUT pin and a CASCIN pin that allow simple networking of multiple devices.

The on-chip control register is programmed using the SCLK, SDATA and $\overline{TFS}$ pins. Three bits of the Control Register set the digital filter cutoff frequency for the device. Selectable frequencies are 584 Hz, 292 Hz, 146 Hz, 73 Hz and 36.5 Hz. A further 2 bits appear as outputs $D_{OUT}1$ and $D_{OUT}2$ and can be used for controlling calibration at the front end. The device is available in a 44-pin PQFP (Plastic Quad Flatpack) and 44-pin PLCC.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS[1, 2] (f_{CLKIN} = 8 MHz; MODE Pin Is High (Slave Mode Operation); AV_{DD} = DV_{DD} = +5 V ± 5%; AV_{SS} = –5 V ± 5%; AGND = DGND = 0 V; V_{REF} = 2.5 V; Filter Cutoff = 146 Hz; Noise Measurement Bandwidth = 146 Hz; A_{IN} Source Resistance = 750 Ω[2] with 1 nF to AGND at each A_{IN}. T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	B Version	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution	22	Bits	
Integral Linearity Error	0.003	% FSR typ	Guaranteed No Missed Codes to 21 Bits[3]
	0.006	% FSR max	
Gain Error	1	% FSR max	
Gain Match Between Channels	0.5	% FSR max	
Gain TC	30	μV/°C typ	
Offset Error	0.2	% FSR max	
Offset Match Between Channels	0.1	% FSR max	
Offset TC	4	μV/°C typ	
Noise	11	μV rms max	See Table I for Typical Noise Performance vs. Programmed Cutoff Frequency
DYNAMIC PERFORMANCE			
Sampling Rate	$f_{CLKIN}/14$		570 kHz for f_{CLKIN} = 8 MHz
Output Update Rate	$f_{CLKIN}/(14 \times 256 \times 2^N)$		N Is Decimal Equivalent of FC2, FC1, FC0 in Control Register
Filter Cutoff Frequency	$f_{CLKIN}/(3.81 \times 14 \times 256 \times 2^N)$		
Settling Time	$(3 \times 14 \times 256 \times 2^N/f_{CLKIN})$		
Usable Dynamic Range[4]	See Table I		
Total Harmonic Distortion	–90	dB typ	Input Frequency = 35 Hz
	–100	dB typ	A_{IN} = ±10 mV p-p
Absolute Group Delay[3]	$(3 \times 14 \times 256 \times 2^N)/2f_{CLKIN}$		
Differential Group Delay[3]	10	ns typ	
Channel-to-Channel Isolation	–85	dB typ	Feedthrough from Any One Channel to the Other Three, with 35 Hz Full-Scale Sine Wave Applied to that Channel
ANALOG INPUT			
Input Range	±2.5	Volts	
Input Capacitance	10	pF typ	
Input Bias Current	1	nA typ	
LOGIC INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{IN}, Input Current			
SDATA, $\overline{RFS}$	+10/-130	μA max	Internal 50 kΩ Pull-Up Resistors
$\overline{TFS}$	+10/-650	μA max	Internal 10 kΩ Pull-Up Resistor
All Other Inputs	±10	μA max	
C_{IN}, Input Capacitance[3]	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	2.4	V min	$\|I_{OUT}\| \leq 40$ μA
V_{OL}, Output Low Voltage	0.4	V max	$\|I_{OUT}\| \leq 1.6$ mA
POWER SUPPLIES			
Reference Input	2.4/2.6	V min/V max	
AV_{DD}	4.75/5.25	V min/V max	
DV_{DD}	4.75/5.25	V min/V max	
AV_{SS}	–4.75/–5.25	V min/V max	
I_{DD}	7.5	mA max	4.8 mA typ
I_{SS}	2.5	mA max	1.8 mA typ
Power Consumption	50	mW max	35 mW typ
Power Supply Rejection[5]	–70	dB typ	

NOTES
[1]Operating temperature ranges as follows : B Version; –40°C to +85°C.
[2]The A_{IN} pins present a very high impedance dynamic load which varies with clock frequency.
[3]Guaranteed by design and characterization. Digital filter has linear phase.
[4]Usable dynamic range is guaranteed by measuring noise and relating this to the full-scale input range.
[5]100 mV p-p, 120 Hz sine wave applied to each supply.
Specifications subject to change without notice.

5

Table I. Typical Usable Dynamic Range, RMS Noise and Filter Settling Time vs. Filter Cutoff Frequency

N	Programmed Cutoff Frequency (Hz)	Output Update Rate (Hz)	Usable Dynamic Range (dB)	RMS Noise (μV)	Filter Settling Time to ±0.0007% FS (ms)	Absolute Group Delay (ms)
0	584	2232	99	21	1.35	0.675
1	292	1116	102	14	2.7	1.35
2	146	558	105	10	5.4	2.7
3	73	279	108	7	10.8	5.4
4	36.5	140	111	5	21.6	10.8

NOTE
Usable Dynamic Range is defined as the ratio of the rms full-scale reading (sine wave input) to the rms noise of the converter.

CONTROL REGISTER TIMING CHARACTERISTICS[1, 2] (AV_{DD} = DV_{DD} = +5 V ± 5%; AV_{SS} = –5 V ± 5%; AGND = DGND = 0 V; f_{CLKIN} = 8 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD}; unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
t_1	$1/f_{CLKIN}$	ns min	SCLK Period
t_2	77	ns min	SCLK Width
t_3	30	ns min	$\overline{TFS}$ Setup Time
t_4	20	ns min	SDATA Setup Time
t_5	10	ns min	SDATA Hold Time
t_6	20	ns min	$\overline{TFS}$ Hold Time

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figure 2.
[3]CLKIN Duty Cycle range is 40% to 60%.

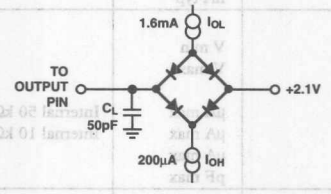


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

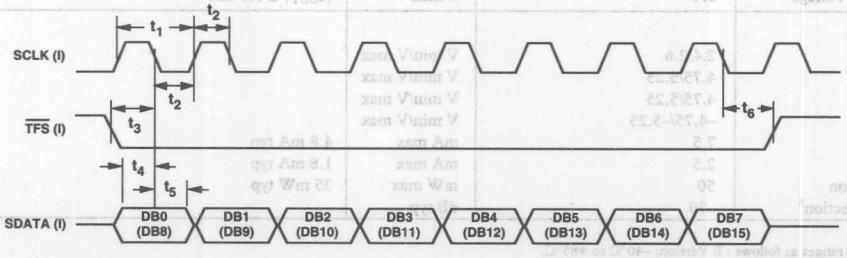


Figure 2. Control Register Timing Diagram

MASTER MODE TIMING CHARACTERISTICS[1, 2] (AV_{DD} = DV_{DD} = +5 V ± 5%; AV_{SS} = –5 V ± 5%; AGND = DGND = 0 V; f_{CLKIN} = 8 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD}; unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	CLKIN Frequency
	8	MHz max	
t_r[5]	40	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	40	ns max	Digital Output Fall Time. Typically 20 ns
t_7	$1/f_{CLKIN}$	ns min	CASCIN Pulse Width
t_8	$1/f_{CLKIN}$	ns min	CASCIN to $\overline{DRDY}$ Setup Time
t_9	$1/2f_{CLKIN}$ + 30	ns max	$\overline{DRDY}$ Low to SCLK Low Delay
t_{10}	50	ns max	CLKIN High to $\overline{DRDY}$ Low, SCLK Active, $\overline{RFS}$ Active
t_{11}	40	ns max	CLKIN High to SCLK High Delay
t_{12}	50	ns min	SCLK Width
t_{13}	$1/f_{CLKIN}$	ns	SCLK Period
t_{14}	40	ns max	SCLK High to $\overline{RFS}$ High Delay
t_{15}	$1/f_{CLKIN}$	ns	$\overline{RFS}$ Pulse Width
t_{16}[6]	45	ns max	SCLK High to SDATA Valid Delay
t_{17}[7]	$1/2f_{CLKIN}$ + 50	ns max	SCLK Low to SDATA High Impedance Delay
	$1/2f_{CLKIN}$ + 10	ns min	
t_{18}	$1/2f_{CLKIN}$ + 60	ns max	CLKIN High to $\overline{DRDY}$ High Delay
t_{19}	50	ns max	CLKIN High to $\overline{RFS}$ High Impedance, SCLK High Impedance
	20	ns min	
t_{20}	$1/2f_{CLKIN}$ + 50	ns max	SCLK Low to CASCOUT High Delay
t_{21}	$2/f_{CLKIN}$	ns	CASCOUT Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 1 and 3.
[3]CLKIN duty cycle range is 40% to 60%.
[4]The AD7716 is production tested with f_{CLKIN} at 8 MHz in the slave mode. It is guaranteed by characterization to operate at 400 kHz and 8 MHz in master mode.
[5]Specified using 10% and 90% points on waveform of interest.
[6]t_{16} is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[7]t_{17} is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

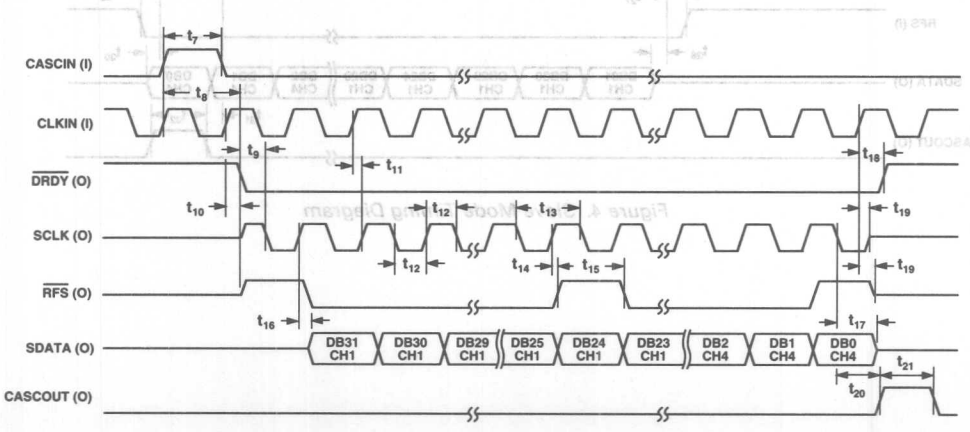


Figure 3. Master Mode Timing Diagram

(f_{CLKIN} = 8 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD}; unless otherwise noted)

Parameter	(B Version)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	CLKIN Frequency
	8	MHz max	
t_r[5]	40	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	40	ns max	Digital Output Fall Time. Typically 20 ns
t_{23}	$1/f_{CLKIN}$	ns min	CASCIN Pulse Width
t_{24}	50	ns min	SCLK Width
t_{25}	125	ns min	SCLK Period
t_{26}	$1/f_{CLKIN}$ +30	ns min	CASCIN High to $\overline{RFS}$ Setup Time
t_{27}	30	ns min	$\overline{RFS}$ Low to SCLK High Setup Time
t_{28}[6]	50	ns max	SCLK High to SDATA Valid Delay
t_{29}	50	ns min	$\overline{RFS}$ Hold Time After SCLK High
t_{30}[7]	50	ns max	SCLK High to SDATA High Impedance Delay
	0	ns min	
t_{31}	60	ns max	SCLK High to CASCOUT High Delay.
t_{32}	$2/f_{CLKIN}$	ns max	CASCOUT Pulse Width

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 1 and 4.

[3]CLKIN duty cycle range is 40% to 60%.

[4]The AD7716 is production tested with f_{CLKIN} at 8 MHz in the slave mode. It is guaranteed by characterization to operate at 400 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]t_{28} is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[7]t_{30} is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

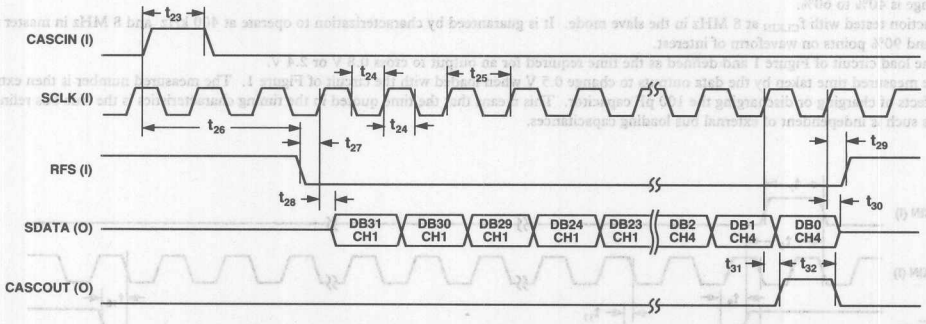


Figure 4. Slave Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND . . . . . –0.3 V to +7 V
AV_{SS} to AGND . . . . . +0.3 V to –7 V
AGND to DGND . . . . . –0.3 V to +0.3 V
AV_{DD} to DV_{DD} . . . . . –0.3 V to +0.3 V
Analog Inputs to AGND . . . . . AV_{SS} – 0.3 V to AV_{DD} + 0.3 V
V_{REF} to AGND . . . . . AV_{SS} – 0.3 V to AV_{DD} + 0.3 V
Digital Inputs to DGND[2] . . . . . –0.3 V to DV_{DD} + 0.3 V
Digital Outputs to DGND . . . . . –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Commercial Plastic (B Versions) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
PQFP Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 95°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
PLCC Package, Power Dissipation . . . . . 500 mW
θ_{JA} Thermal Impedance . . . . . 55°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

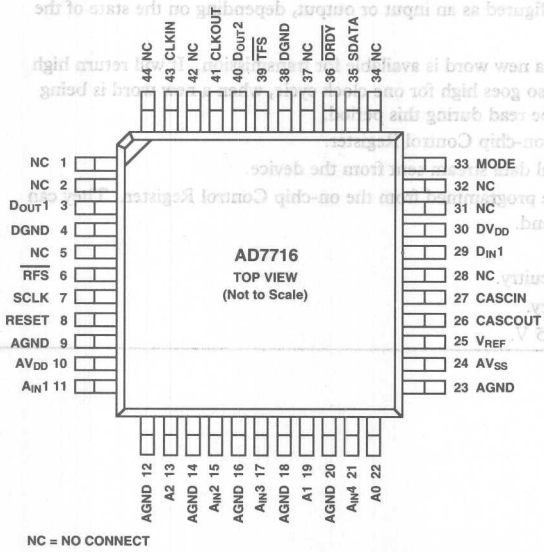
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

5

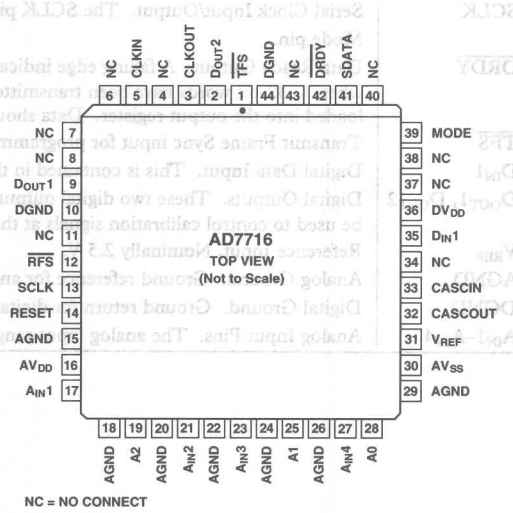
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PQFP PINOUT



PLCC PINOUT



ORDERING GUIDE

Model	Temperature Range	Output Noise (Filter: 146 Hz)	Package Option*
AD7716BP	–40°C to +85°C	11 μV rms	P-44
AD7716BS	–40°C to +85°C	11 μV rms	S-44

*P = PLCC (Plastic Leaded Chip Carrier); S = PQFP (Plastic Quad Flatpack). For outline information see Package Information section.

PIN DESCRIPTION

Pin	Description
AV_{DD}	Analog Positive Supply, +5 V Nominal. This supplies +ve power to the analog modulators. AV_{DD} & DV_{DD} must be tied together externally.
DV_{DD}	Digital Positive Supply, +5 V Nominal. This supplies +ve power to the digital filter and input/output registers.
AV_{SS}	Analog Negative Supply, –5 V nominal. This supplies –ve power to the analog modulators.
RESET	A high pulse on this input pin synchronizes the sampling point on the four input channels. It can be used in a multichannel system to ensure simultaneous sampling. This also resets the digital interface to a known state.
A0–A2	The three address input pins, A0, A1 and A2 give the device a unique address. This information is contained in the output data stream from the device.
CLKIN	Clock Input for External Clock.
CLKOUT	Clock Output which is used to generate an internal master clock by connecting a crystal between CLKOUT and CLKIN. If an external clock is used then CLKOUT is not connected.
MODE	This digital input determines the device interface mode. If it is hardwired low, then the Master Mode interface is enabled whereas if it is high, the Slave Mode interface is enabled.
CASCIN	This is an active-high, level-triggered digital input which is used to enable the output data stream. This input may be used to cascade several devices in a multichannel system.
CASCOUT	Digital output which goes high at the end of a complete 4-channel data transfer. This can be connected to the CASCIN of the next device in a multichannel system to ensure proper control of the data transfer.
$\overline{RFS}$	Receive Frame Synchronization signal for the serial output data stream. This can be an input or output depending on the interface mode.
SDATA	Serial Data Input/Output Pin.
SCLK	Serial Clock Input/Output. The SCLK pin is configured as an input or output, depending on the state of the Mode pin.
$\overline{DRDY}$	Data Ready Output. A falling edge indicates that a new word is available for transmission. It will return high when 4, 32-bit words have been transmitted. It also goes high for one clock cycle, when a new word is being loaded into the output register. Data should not be read during this period.
$\overline{TFS}$	Transmit Frame Sync input for programming the on-chip Control Register.
$D_{IN}1$	Digital Data Input. This is contained in the digital data stream sent from the device.
$D_{OUT}1$, $D_{OUT}2$	Digital Outputs. These two digital outputs can be programmed from the on-chip Control Register. They can be used to control calibration signals at the front end.
V_{REF}	Reference Input, Nominally 2.5 V.
AGND	Analog Ground. Ground reference for analog circuitry.
DGND	Digital Ground. Ground return for digital circuitry.
$A_{IN}1$–$A_{IN}4$	Analog Input Pins. The analog input range is ±2.5 V.

TERMINOLOGY

LINEARITY ERROR

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with Bipolar Zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

DIFFERENTIAL LINEARITY ERROR/NO MISSED CODES

This is the difference between any code's actual width and the ideal (1 LSB) width. Differential Linearity Error is expressed in LSBs. A differential linearity specification of ±1 LSB or less guarantees no missed codes to the full resolution of the device. The AD7716 has no missed codes guaranteed to 21 bits with a cutoff frequency of 146 Hz.

GAIN ERROR

Gain Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 1) from the ideal (V_{REF} –3/2 LSBs). It is expressed as a percentage of full scale.

GAIN TC

This is the variation of gain error with temperature and is expressed in µV/°C.

OFFSET ERROR

Offset Error is the deviation of the first code transition from the ideal ($-V_{REF}$ + 0.5 LSB). It is expressed as a percentage of full scale.

OFFSET TC

This is the variation of offset error with temperature and is expressed in µV/°C.

NOISE

This is the converter rms noise expressed in µV. Because of the digital filtering in the sigma delta converter, the noise performance is a function of the programmed filter cutoff.

SAMPLING RATE

This is the modulator sampling rate. For the AD7716, it is $f_{CLKIN}/14$.

OUTPUT UPDATE RATE

This is the rate at which the digital filter updates the output shift register. It is a function of the master clock frequency and the programmed filter cutoff frequency.

FILTER CUTOFF FREQUENCY

The digital filter of the AD7716 can be programmed, in binary steps, to 5 discrete cutoff frequencies, ranging from 584 Hz to 36.5 Hz (for a CLKIN frequency of 8 MHz).

SETTLING TIME

This is the settling time of the on-chip digital filter, to 0.0007% of FSR, in response to a full-scale step at the input of the ADC. It is proportional to the master clock frequency and the filter cutoff frequency.

USABLE DYNAMIC RANGE

The usable dynamic range is the ratio of the rms full-scale reading (sine wave input) to the rms noise of the converter, expressed in dBs. It determines the level to which it is possible to resolve the input signal. For example, at a bandwidth of 146 Hz, the rms noise of the converter is 11 µV. The full-scale rms is 1.77 volts. So, the usable dynamic range is 104 dB. Any signal below this level will be indistinguishable from noise unless extra post-filtering techniques are employed.

TOTAL HARMONIC DISTORTION

Total harmonic distortion (THD) is the ratio of the rms sum of the harmonics to the fundamental. For the AD7716, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through sixth harmonics.

ABSOLUTE GROUP DELAY

Absolute group delay is the rate of change of phase versus frequency, $d\phi/df$ and is expressed in seconds. For the AD7716, it is dependent on master clock frequency and filter cutoff frequency.

DIFFERENTIAL GROUP DELAY

Differential group delay is the total variation in absolute group delay in the specified bandwidth. Since the digital filter in the AD7716 has perfectly linear phase, the differential group delay is almost zero. This is important in many signal processing applications where excessive differential group delay can cause phase distortion.

5

range, low frequency signals such as those representing ECG, EEG, chemical, physical or biological processes. It contains four sigma delta ADCs, a clock oscillator and a serial communications port.

Each of the analog input signals to the AD7716 is continuously sampled at a rate determined by the frequency of the master clock, CLKIN. Four sigma-delta modulators convert the sampled signals into digital pulse trains whose duty cycles contain the digital information. These are followed by low-pass filters to process the output of the modulators and update the output register at a maximum rate of 2.2 kHz. The output data can be read from the serial port at any rate up to this.

THEORY OF OPERATION

The general block diagram of a delta-sigma ADC is shown in Figure 5. It contains the following elements.

1. Continuously Sampling Integrator
2. A Differential Amplifier or Subtracter
3. A 1-Bit A/D Converter (Comparator)
4. A 1-Bit DAC
5. A Digital Low-Pass Filter.

In operation, the sampled analog signal is fed to the subtracter, along with the output of the 1-bit DAC. The filtered difference signal is fed to the comparator, whose output samples the difference signal at a frequency many times that of the analog signal frequency (oversampling).

Oversampling is fundamental to the operation of delta-sigma ADCs. Using the quantization noise formula for an ADC:

$$SNR = (6.02 \times number\ of\ bits + 1.76)\ dB,$$

a 1-bit ADC or comparator yields an SNR of 7.78 dB.

When operating with a master clock of 8 MHz, the AD7716 samples the input signal at 570 kHz, which spreads the quantization noise from 0 kHz to 285 kHz. Since the specified analog input bandwidth of the AD7716 is only 584 Hz maximum (it can be programmed to be lower), the noise energy in this bandwidth would be only 1/488 of the total quantization noise, assuming that the noise energy was spread evenly throughout the spectrum. This very high sampling with respect to the input bandwidth is known as oversampling, and the ratio of 488:1 is called the oversampling ratio. The noise is reduced still further by analog filtering in the modulator loop, which shapes the quantization noise spectrum to move most of the noise energy to frequencies above 584 Hz. The SNR performance in the 0 Hz to 584 Hz range is conditioned to the 99 dB level in this fashion (see Table I). As the programmed bandwidth is reduced, the oversampling ratio increases and the usable dynamic range also increases. Thus, for example, with a programmed bandwidth of 73 Hz, the oversampling ratio is 3904:1, and the usable dynamic range is 108 dB which corresponds to greater than 17-bit resolution.

train appearing at the output of the comparator. It can be retrieved as a parallel binary data word using a digital filter.

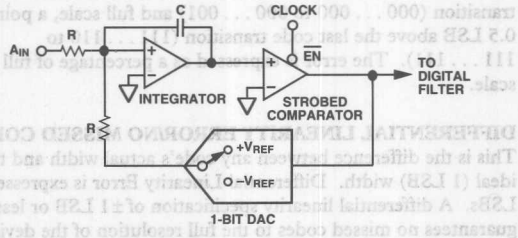


Figure 5. First Order Modulator

Sigma-delta ADCs are generally described by the order of the analog low-pass filter. A simple example of a first order sigma-delta ADC is shown in Figure 5. This contains only a first-order low-pass filter or integrator.

The AD7716 uses a second-order sigma-delta modulator and a digital filter that provides a rolling average of the sampled output. After power-up or if there is a step change in the input voltage, there is a settling time before valid data is obtained.

DIGITAL FILTERING

The AD7716's digital filter behaves like an analog filter, with a few minor differences.

First, since digital filtering occurs after the A-to-D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. If noise signals cause the input signal to exceed the specified range, consideration should be given to analog input filtering, or to reducing the gain in the input channel to bring the combination of signal and noise spike within the specified input range.

Filter Characteristics

The cutoff frequency of the digital filter is determined by bits FC2, FC1 and FC0 in the control register (See Table IV). The cutoff frequency of the filter is $f_{CLKIN}/(3.81 \times 14 \times 256 \times 2N)$, where N is the decimal equivalent of FC2, FC1, FC0. At the maximum clock frequency of 8 MHz, with all 0s loaded to FC2, FC1, FC0, the cutoff frequency of the filter is 584 Hz and the data update rate is 2232 Hz.

Since the AD7716 contains low-pass filtering, there is a settling time associated with step function inputs, and data will be invalid after a step change until the settling time has elapsed. The

relationship between input bandwidth and settling is given in Table I. Because of this settling time, most sigma delta ADCs are unsuitable for high speed multiplexing, where channels are switched and converted sequentially at high rates, as switching between channels can cause a step change in the input. However, the AD7716 is a sigma-delta solution to multichannel applications, since it can process four channels simultaneously. In addition, it is easy to cascade several devices in order to increase the number of channels being processed.

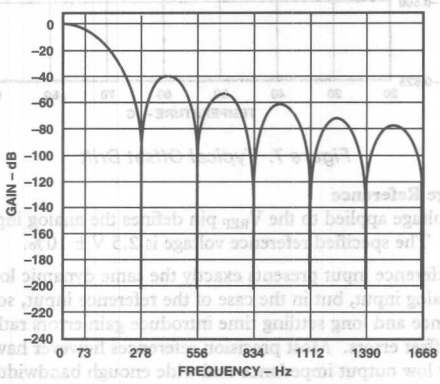


Figure 6. Frequency Response of AD7716 Filter

Figure 6 shows the filter frequency response for a cutoff frequency of 73 Hz. This is a $(\sin x/x)^3$ response (also called sinc^3) that provides greater than 100 dB rejection at the notch frequencies. The relationship between the programmed cutoff frequency and the first notch is constant ($f_{NOTCH} = 3.81 \times f_{CUTOFF}$). The first notch frequency is also the output data rate. The settling time to a full-scale step input is four times the output data period. Programming a different cutoff frequency via FC0–FC2 does not alter the profile of the filter response, it simply changes the frequency of the notches.

In Figure 6, the first notch is at 278 Hz. This is also the output data rate. Settling time to a full-scale step input is 10.8 ms.

The digital filter can be defined by the following equations.

$$H(z) = \left[\frac{1}{N} \times \frac{1 - Z^{-N}}{1 - Z^{-1}}\right]^3$$

$$|H(f)| = \left|\frac{1}{N} \times \frac{\sin(N \times \pi\, f/fs)}{\sin(\pi\, f/fs)}\right|^3$$

where N = *Oversampling Ratio*

fs = *Modulator Sampling Rate*

Post Filtering

In the AD7716, the on-chip modulator provides the digital filter with samples at a rate of 570 kHz. The filter decimates these samples to provide data at an output rate which corresponds to the programmed first notch frequency of the filter.

If the user wants to reduce the output noise from the device for bandwidths less than 36.5 Hz, then it is possible to employ extra filtering after the AD7716. This extra digital filtering is called post filtering. If a straight averaging filter is used, for example, a reduction in bandwidth by a factor of 2 results in $\sqrt{2}$ reduction in the rms noise. This additional filtering will also result in a longer settling time.

Antialias Considerations

The digital filter does not provide any rejection at integer multiples of the modulator sampling frequency (n × 570 kHz, where n = 1, 2, 3, . . .). This means that there are frequency bands, $\pm f_{3dB}$ wide (f_{3dB} is the cutoff frequency selected by FC0 to FC2) where noise passes unattenuated to the output. However, due to the AD7716's high oversampling ratio, these bands occupy only a small fraction of the spectrum and most broadband noise is filtered.

In spectral analysis applications, it is important to note that attenuation at half the output update rate is 16 dB. Extra front-end filtering or post filtering may be required to keep aliases in this frequency band at an acceptable level.

USING THE AD7716

SYSTEM DESIGN CONSIDERATIONS

The AD7716 operates differently from successive approximation ADCs or other integrating ADCs. Since it samples the signal continuously, like a tracking ADC, there is no need for a start convert command. The output register is updated at a rate dependent on the programmed cutoff frequency, and the output can be read at any time.

Input Signal Conditioning

The input range for the AD7716 is $\pm V_{REF}$, where V_{REF} = 2.5 V ± 10%. Other input ranges can be accommodated by input signal conditioning. This may take the form of gain to increase a smaller signal range, or passive attenuation to reduce a larger input voltage range.

Source Resistance

If passive attenuators are used in front of the AD7716, care must be taken to ensure that the source impedance is sufficiently low. The dc input resistance for the AD7716 is greater than 1 GΩ. In parallel with this there is a small sampling capacitor. The dynamic load presented by this varies with the clock frequency. The modulator sampling rate determines the amount of time available for the sampling capacitor to be charged. Any extra external impedances result in a longer overall charge time resulting in extra gain errors on the analog input. The AD7716 has a quite large gain error (1% FSR) due to the fact that there is no on-chip calibration. Thus, even an extra 10 kΩ source resistance and 50 pF source capacitance will have no significant effect on this.

Active signal conditioning circuits such as op amps generally do not suffer from problems of high source impedance. Their open-loop output resistance is normally only tens of ohms and, in any case, most modern general purpose op amps have sufficiently fast closed-loop settling time for this not to be a problem.

Accuracy

Sigma-delta ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no missing codes performance.

The AD7716 achieves excellent linearity by the use of high quality, on-chip silicon dioxide capacitors, which have a very low capacitance/voltage coefficient.

Drift Considerations

The AD7716 uses autozeroing techniques to minimize input offset drift. Charge injection in the analog switches and leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. Figure 7 indicates the typical offset due to temperature changes. Drift is relatively flat up to 85°C. Above this temperature, leakage current becomes the main source of offset drift. Since leakage current doubles approximately every 10°C, the offset drifts accordingly. The value of the voltage on the sample capacitor is updated at a rate determined by the master clock, therefore the amount of offset drift which occurs will be proportional to the elapsed time between samples.

Gain drift within the converter depends mainly upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

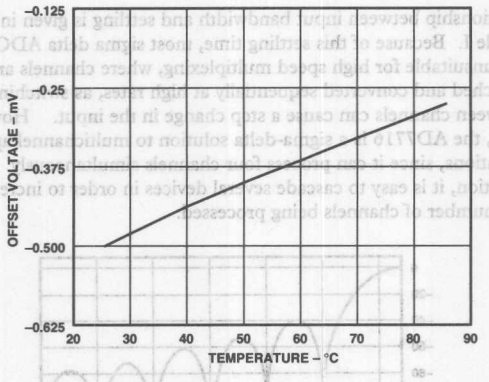


Figure 7. Typical Offset Drift

Voltage Reference

The voltage applied to the V_{REF} pin defines the analog input range. The specified reference voltage is 2.5 V ± 10%.

The reference input presents exactly the same dynamic load as the analog input, but in the case of the reference input, source resistance and long settling time introduce gain errors rather than offset errors. Most precision references however have sufficiently low output impedance and wide enough bandwidth to settle to the required accuracy in the time allowed by the AD7716.

The reference should be chosen to have minimal noise in the programmed passband. Recommended references are the AD780 or the REF43 from Analog Devices. These low noise references have typical noise spectral densities of 100 nV/√Hz at 600 Hz. This corresponds to an rms noise of 2.5 μV in this band and is more than adequate for the AD7716.

Clock Generation

The device operates from a master clock which must be provided either from a crystal source or an external clock source. If a crystal is used, it must be connected across the CLKIN and CLKOUT pins. Typical loading capacitors of 15 pF are required on CLKIN, CLKOUT. The crystal manufacturers data should be consulted for more information. An external clock can also be used to drive the CLKIN input directly with a CMOS compatible clock. In this case, CLKOUT is left unconnected. The nominal clock frequency for the device is 8 MHz.

CONTROL REGISTER DESCRIPTION

The 16-bit control register is programmed in two 8-bit bytes; the low byte is programmed first and the high byte second. The loading format is LSB first (DB0 for the Least Significant Byte; DB8 for the Most Significant Byte). Three control lines are used: $\overline{TFS}$, SCLK and SDATA. On initial application of power to the AD7716, the control register will come up in an undetermined state. Programming the control register requires an SCLK input, a $\overline{TFS}$ input and an SDATA input. The MODE pin on the device determines whether it is in the master interface mode or the slave interface mode. In either mode, a falling edge on $\overline{TFS}$ causes the part to relinquish control of the SDATA and SCLK lines. When $\overline{TFS}$ goes low, data on the SDATA line is clocked into the control register on each succeeding falling edge of SCLK. When 8 bits have been clocked in, the transfer automatically stops. Only when another negative going edge is detected on $\overline{TFS}$ will new information be written into the control register. The control register programming model is shown in Table II. Bits DB8 and DB0 allow the control register to identify whether the MS Byte or the LS Byte has been programmed. Only when DB8 is a 1 and DB0 is a 0 will the register recognize that a complete valid word has been programmed.

Control register bit, DB15 (A3), acts as an extra address bit which must always be set to 1 to enable programming of the AD7716. If it is set to 0, then the programmed word is ignored. This allows the user to bypass the AD7716 control register and use the serial stream from the DSP or microcomputer to program other serial peripheral devices.

When a valid word has been received, the device interrogates the M0 bit. If this is 0, then the digital filter cutoff frequencies are programmed to the appropriate value if the device address pins correspond to the A2, A1, A0 bits in the control register. If the device address pins do not correspond to the A2, A1, A0 bits then the FC2, FC1, FC0 bits are ignored. If M0 is 1, then the digital filter cutoff frequencies are programmed to the FC2, FC1, FC0 value irrespective of the address bits. In a multichannel system this allows the user to either program all AD7716s to have the same cutoff frequency or else to give each device a separate cutoff frequency.

Control register bits FC2, FC1, FC0 program the digital filter cutoff frequency, see Table VI.

Control register bits D2, D1 control the digital output pins D2 and D1. These are programmed in the same way as FC2, FC1, FC0.

Table II. Control Register Programming Model

Most Significant Byte								Least Significant Byte							
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
A3	A2	A1	A0	M0	FC2	FC1	1	FC0	DOUT2	DOUT1	X	X	X	X	0

Table III. M0 Truth Table

M0	Programming Mode
0	A2, A1, A0 determine which device is addressed and programmed with cutoff frequency and digital output.
1	A2, A1, A0 ignored. All devices are addressed and programmed with common cutoff frequency and digital output.

Table IV. Cutoff Frequency Truth Table

FC2	FC1	FC0	Cutoff Frequency (Hz)
0	0	0	584
0	0	1	292
0	1	0	146
0	1	1	73
1	0	0	36.6

high for at least four CLKIN cycles, the modulator sampling points and digital filter starting points are all synchronized. This synchronizes all devices which receive the RESET pulse and gives simultaneous sampling of all channels. It does not affect the control register but restarts the interface. Also, it is necessary to wait the requisite settling time after applying Reset to get valid data from the device.

CASCADING DEVICES

The AD7716 provides a facility for connecting multiple devices in series. The CASCIN and CASCOUT pins allow this. Connecting CASCOUT to CASCIN of the succeeding device means that the SDATA output of the second device will be disabled until the output register of the first device is empty.

In the case of the first device in the system, it is possible to drive CASCIN from CASCOUT of the last device or, alternatively, invert $\overline{DRDY}$ to drive it. If CASCIN is driven by CASCOUT, then a reset must be applied after every write to the control register. This also applies in single device systems that use CASCOUT to drive CASCIN

DATA OUTPUT INTERFACE MODES

When the control register has been programmed, the device begins conversion. There is an initial delay to allow the digital filters to settle. As already stated, these filters are $Sinc^3$, and so the filter output update rate is directly related to the programmed cutoff frequency. The ratio between these is 3.81. So, for a filter cutoff frequency of 584 Hz, the output update is 2.22 kHz. The falling edge of the $\overline{DRDY}$ output indicates that the output shift register has been updated. There are two interface modes. One is the master mode, where the AD7716 is the master in the system and the processor to which it is communicating is the slave. The other mode is the slave mode, where the AD7716 is the slave and the processor is the system master. In both of these modes the data output stream contains 4×32 bits, corresponding to the four input channels. The output data format is given in Table V. The conversion result DB21–DB0 occupies location DB31–DB10 of the output register. DB21 is the MSB and is transmitted first as shown in the timing diagrams. The channel address is given by CA0 and CA1 which occupy DB9 and DB8 of the output register. The channel address format is given in Table VI.

AD7716 by an internally generated serial clock and frame synchronization pulse. Two signals initiate the transfer. These are the input CASCIN and the internally generated $\overline{DRDY}$ signal. When a high level is detected on CASCIN, the device checks the state of $\overline{DRDY}$. Note, that on initial power-up or after a reset has been applied, the CASCIN input is not necessary on device 000 for the first data transfer but is required thereafter. If $\overline{DRDY}$ is low, then the 3-state output, $\overline{RFS}$ goes high on the next rising edge of CLKIN and stays high for one CLKIN cycle before going low again. The 3-state SCLK output is also activated on the same rising edge. As $\overline{RFS}$ goes low, DB31 is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK. Data is transmitted in 8-bit bytes. For each A_{IN}, there are 4, 8-bit bytes and 4 $\overline{RFS}$ pulses. When DB0 of A_{IN} 4 has been clocked out, SCLK goes back into 3-state and the CASCOUT output goes high for one master clock cycle. $\overline{DRDY}$ also goes high at this point. Successive devices can be networked together by tying the CASCOUT of one device to the CASCIN on the next one.

Note that on device 0 (A2, A1, A0 tied low), the CASCIN input should be driven by the inverse of the $\overline{DRDY}$ output. This is shown in the interface diagram of Figure 8.

The Master Mode interface is very suitable for loading data into a serial-to-parallel shift register or for DSPs which can accept a continuous stream of 8-bit bytes.

Slave Mode Interface

The device may be placed in the slave interface mode by tying the MODE pin high. In this mode, the master processor controls the transfer of data from the signal processing block. It starts the transfer by sending a frame synchronizations pulse and serial clock to the AD7716. This could be in response to an interrupt generated by the $\overline{DRDY}$ output on the AD7716. If the device has detected a high level on CASCIN or is device 000 on its first transfer, it starts to send out data on the next rising edge of SCLK. This data is then valid on the falling edge of SCLK. When all the data bits have been clocked out, the CASCOUT pin goes high for one CLKIN cycle and $\overline{DRDY}$ also goes high. The slave mode interface is suited to both microcomputers like the 8051 and 68HC11 and also DSPs like the TMS320C25, ADSP-2101 family and the DSP56000 family.

Table V. Output Data Word Format

DB31 . . . DB10	DB9 DB8	DB7 DB6 DB5	DB4	DB3	DB2 DB1 DB0
DB21 . . . DB0 Conversion Result	CA0 CA1 Channel Address	A0 A1 A2 Device Address	$D_{IN}1$ Pace Detect	OVFL Overflow	X X X Indeterminate

Table VI. Channel Address Format

Channel	CA1 (DB8)	CA0 (DB9)
A_{IN} 1	0	0
A_{IN} 2	0	1
A_{IN} 3	1	0
A_{IN} 4	1	1

MICROPROCESSOR INTERFACING

Interfacing the AD7716 to the ADSP-2100 Family

The ADSP-2100 family of microcomputers from Analog Devices are high speed, high performance digital signal processors. Many members of the family have serial ports (known as SPORTs) which are compatible with the AD7716. These include the ADSP-2101, ADSP-2105, ADSP-2111 and ADSP-2115. Full details of these are available in the *ADSP-2100 Family User's Manual* available from Analog Devices.

Figure 8 shows the hardware interface between two AD7716s and SPORT 0 of the ADSP-2101 DSP. This yields a very efficient 8-channel data acquisition system. The AD7716 is set up for slave interface mode by tying the MODE pin high. This means that the ADSP-2101 is the master in the system and supplies the necessary frame synchronization and SCLK Signals to the AD7716s when writing to and reading from the device.

On power up, the user should write to the AD7716 control register in order to set the filter cutoff frequencies. The appropriate SPORT 0 Control Register (0 × 3FF6) setting is "7EC7." This sets the transmit section for alternate inverted framing with a word length of 8 bits. Two 8-bit words should then be written to each AD7716 to program the filter cutoff frequencies. The control register programming model is given in Table II. Note that the LSB (DB0) must be loaded first as in the timing diagram of Figure 2.

When the write operation is complete, a reset pulse should be applied to both devices. This ensures that the sampling and interface timing of the device are synchronized. The reset can be under DSP control, in which case a flag output could be used.

After reset, the processor should jump to the read routine. For this read routine, there are several registers that need to be set.

The SPORT0 Control Register setting is "7FCF." This sets the receive section for internal SCLK, continuous receive with alternate inverted framing.

The SPORT0 SCLKDIV Register (0 × 3FF5) determines the SCLK frequency from the ADSP-2101. With "0000" loaded, the SCLK output is at its maximum (1/2 the master clock of 12.5 MHz).

In normal operation, a SPORT generates an interrupt when it has received a data word. Autobuffering provides a mechanism for receiving or transmitting an entire block of serial data before an interrupt is generated. Service routines can operate on the entire block of data, rather than on a single word, reducing overhead significantly. This is ideal for use with a device like the AD7716 where there is a requirement to read many bits of data (256 in this case) for each sampling instant. The SPORT0 Autobuffer Control Register (0 × 3FF3) is loaded with "0001" to enable the Receive Autobuffering.

The SPORT0 RFSDIV Register (0 × 3FF4) should be set to the minimum value of "000F." Finally the IRQ2 interrupt should be enabled.

The DSP will now wait for an interrupt from the AD7716. This interrupt is generated by the AD7716 $\overline{\text{DRDY}}$ line going low. If the interrupt service routine is set for autobuffered mode with a length of 16 (16-bit) words, then the DSP will read in the 256 bits from the two AD7716s in one continuous stream and then stop. The data from the two devices will be contained in the designated data memory area and the DSP can now go and operate on this as is necessary. Note that, because of the ADSP-2101 framing, a one-bit shift left will be necessary on the data in memory. For 16 data words, this will require 22 instruction cycles.

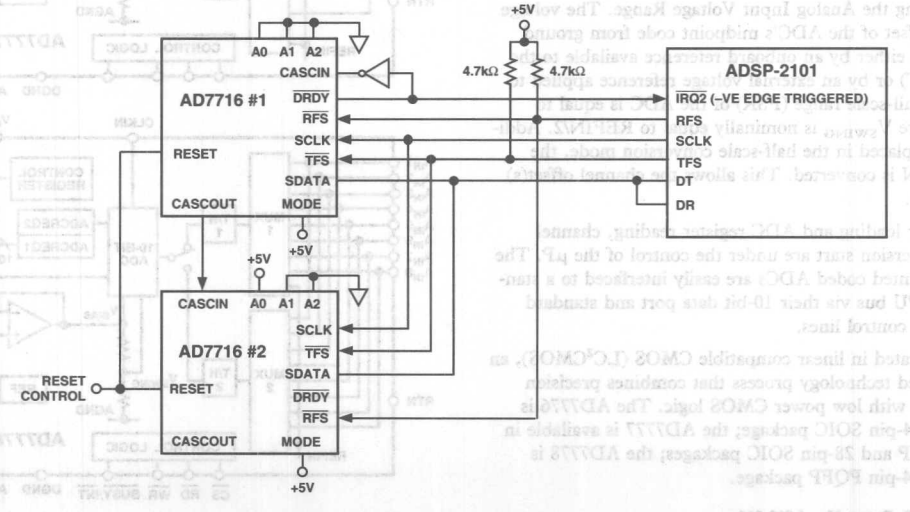


Figure 8. 8-Channel Data Acquisition System Using the ADSP-2101 Digital Signal Processor

LC²MOS, High Speed 1-, 4- & 8-Channel 10-Bit ADCs

AD7776/AD7777/AD7778*

FEATURES
AD7776: Single Channel
AD7777: 4-Channel
AD7778: 8-Channel
Fast 10-Bit ADC: 2.5 µs Worst Case
+5 V Only
Half-Scale Conversion Option
Fast Interface Port
Power-Down Mode

APPLICATIONS
HDD Servos
Instrumentation

GENERAL DESCRIPTION

The AD7776, AD7777 and AD7778 are a family of high speed, multichannel, 10-bit ADCs primarily intended for use in R/W head positioning servos found in high density hard disk drives. They have unique input signal conditioning features which make them ideal for use in such single supply applications.

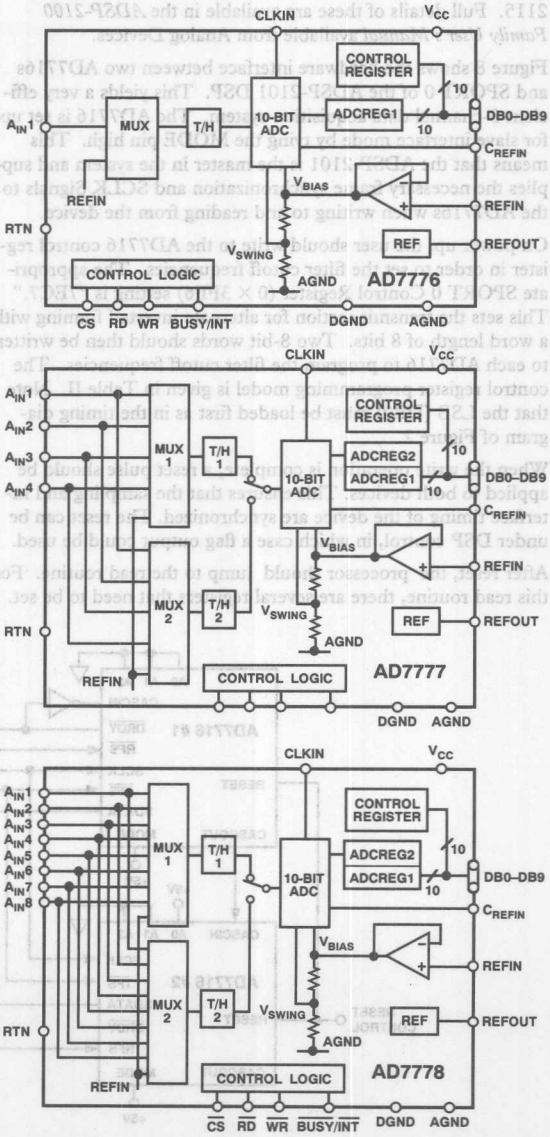
By setting a bit in a control register within both the four-channel version, AD7777, and eight-channel version, AD7778, the input channels can either be independently sampled or any two channels of choice can be simultaneously sampled. For all versions the specified input signal range is of the form $V_{BIAS} \pm V_{SWING}$. However, if the RTN pin is biased at, say, 2 V then the analog input signal range becomes 0 V to +2 V for all input channels. This is dealt with in more detail under the section Changing the Analog Input Voltage Range. The voltage V_{BIAS} is the offset of the ADC's midpoint code from ground and is supplied either by an onboard reference available to the user (REFOUT) or by an external voltage reference applied to REFIN. The full-scale range (FSR) of the ADC is equal to 2 V_{SWING} where V_{SWING} is nominally equal to REFIN/2. Additionally, when placed in the half-scale conversion mode, the value of REFIN is converted. This allows the channel offset(s) to be measured.

Control register loading and ADC register reading, channel select and conversion start are under the control of the µP. The twos complemented coded ADCs are easily interfaced to a standard 16-bit MPU bus via their 10-bit data port and standard microprocessor control lines.

They are fabricated in linear compatible CMOS (LC²CMOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The AD7776 is available in a 24-pin SOIC package; the AD7777 is available in both 28-pin DIP and 28-pin SOIC packages; the AD7778 is available in a 44-pin PQFP package.

*Protected by U.S. Patent No. 4,990,916.

FUNCTIONAL BLOCK DIAGRAMS



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (V_{CC} = +5 V ± 5%; AGND = DGND = 0 V; CLKIN = 8 MHz; RTN = 0 V; C_{REFIN} = 10 nF; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	Units	Conditions/Comments
DC ACCURACY			
Resolution[2]	10	Bits	
Relative Accuracy	±1	LSB max	See Terminology
Differential Nonlinearity	±1	LSB max	No Missing Codes; See Terminology
Bias Offset Error	±12	LSB max	See Terminology
Bias Offset Error Match	10	LSB max	Between Channels, AD7777/AD7778 Only; See Terminology
Plus or Minus Full-Scale Error	±12	LSB max	See Terminology
Plus or Minus Full-Scale Error Match	10	LSB max	Between Channels, AD7777/AD7778 Only; See Terminology
ANALOG INPUTS			
Input Voltage Range			
All Inputs	V_{BIAS} ± V_{SWING}	V min/V max	
Input Current	+200	µA max	V_{IN} = V_{BIAS} ± V_{SWING}; Any Channel
REFERENCE INPUT			
REFIN	1.9/2.1	V min/V max	For Specified Performance
REFIN Input Current	+200	µA max	
REFERENCE OUTPUT			
REFOUT	1.9/2.1	V min/V max	Nominal REFOUT = 2.0 V
DC Output Impedance	5	Ω typ	
Reference Load Change	±2	mV max	For Reference Load Current Change of 0 to ±500 µA
	±5	mV max	For Reference Load Current Change of 0 to ±1 mA
			Reference Load Should Not Change During Conversion
Short Circuit Current[3]	20	mA max	See Terminology
LOGIC OUTPUTS			
DB0–DB9, $\overline{BUSY/INT}$			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 µA
Floating State Leakage Current	±10	µA max	
Floating State Capacitance[3]	10	pF max	
ADC Output Coding	Twos Complement		
LOGIC INPUTS			
DB0–DB9, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, CLKIN			
Input Low Voltage, V_{INL}	0.8	V max	
Input High Voltage, V_{INH}	2.4	V min	
Input Leakage Current	10	µA max	
Input Capacitance[3]	10	pF max	
CONVERSION TIMING			
Acquisition Time	4.5 t_{CLKIN}	ns min	See Terminology
	5.5 t_{CLKIN} + 70	ns max	
Single Conversion	14 t_{CLKIN}	ns max	
Double Conversion	28 t_{CLKIN}	ns max	
t_{CLKIN}	125/500	ns min/ns max	Period of Input Clock CLKIN
t_{CLKIN} High	50	ns min	Minimum High Time for CLKIN
t_{CLKIN} Low	40	ns min	Minimum Low Time for CLKIN
POWER REQUIREMENTS			
V_{CC} Range	+4.75/+5.25	V min/V max	For Specified Performance
I_{CC}, Normal Mode	15	mA max	$\overline{CS}$ = $\overline{RD}$ = +5 V, CR8 = 0
I_{CC}, Power-Down Mode	1.5	mA max	CR8 = 1. All Linear Circuitry OFF
Power-Up Time to Operational Specifications	500	µs max	From Power-Down Mode
DYNAMIC PERFORMANCE			See Terminology
Signal to Noise and Distortion S/(N+D) Ratio	−57	dB min	V_{IN} = 99.88 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 380.95 kHz
Total Harmonic Distortion (THD)	−60	dB min	V_{IN} = 99.88 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 380.95 kHz
Intermodulation Distortion (IMD)	−75	dB typ	fa = 103.2 kHz, fb = 96.5 kHz with $f_{SAMPLING}$ = 380.95 kHz. Both Signals Are Sine Waves at Half-Scale Amplitude
Channel-to-Channel Isolation	−90	dB typ	V_{IN} = 100 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 380.95 kHz

NOTES
[1]Temperature range as follows: A = −40°C to +85°C.
[2]1 LSB = (2 × V_{SWING})/1024 = 1.95 mV for V_{SWING} = 1.0 V.
[3]Guaranteed by design, not production tested.
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1, 2] (V_{CC} = +5 V ± 5%; AGND = DGND = 0 V; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Label	Limit at T_{MIN} to T_{MAX}	Units	Test Conditions/Comments
INTERFACE TIMING				
$\overline{CS}$ Falling Edge to $\overline{WR}$ or $\overline{RD}$ Falling Edge	t_1	0	ns min	
$\overline{WR}$ or $\overline{RD}$ Rising Edge to $\overline{CS}$ Rising Edge	t_2	0	ns min	
$\overline{WR}$ Pulse Width	t_3	53	ns min	
$\overline{CS}$ or $\overline{RD}$ Active to Valid Data[3]	t_4	**60**	**ns max**	**Timed from Whichever Occurs Last**
Bus Relinquish Time after $\overline{RD}$[4]	t_5	**10**	**ns min**	
		45	**ns max**	
Data Valid to $\overline{WR}$ Rising Edge	t_6	55	ns min	
Data Valid after $\overline{WR}$ Rising Edge	t_7	10	ns min	
$\overline{WR}$ Rising Edge to $\overline{BUSY}$ Falling Edge	t_8	1.5 t_{CLKIN}	ns min	CR9 = 0
		2.5 t_{CLKIN} + 70	ns max	
$\overline{WR}$ Rising Edge to $\overline{BUSY}$ Rising Edge or $\overline{INT}$ Falling Edge	t_9	19.5 t_{CLKIN} + 70	ns max	Single Conversion, CR6 = 0
	t_{10}	33.5 t_{CLKIN} + 70	ns max	Double Conversion, CR6 = 1
$\overline{WR}$ or $\overline{RD}$ Falling Edge to $\overline{INT}$ Rising Edge	t_{11}	60	ns max	CR9 = 1

NOTES
[1]See Figures 1 to 3.
[2]Timing specifications in bold print are 100% production tested. All other times are guaranteed by design, not production tested. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[3]t_4 is measured with the load circuit of Figure 4 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]t_5 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 4. The measured time is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time t_5 quoted above is the true bus relinquish time of the device and, as such, is independent of the external bus loading capacitance.

Specifications subject to change without notice.

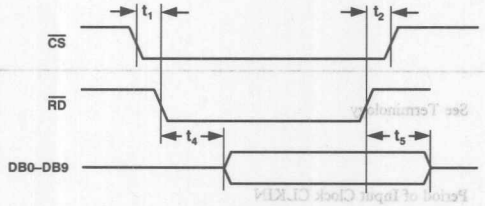


Figure 1. Read Cycle Timing

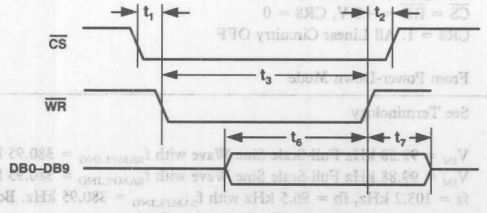


Figure 2. Write Cycle Timing

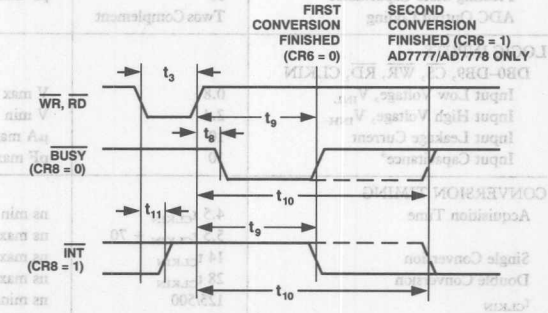


Figure 3. BUSY/INT Timing

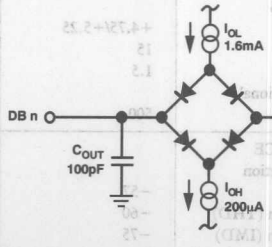


Figure 4. Load Circuit for Bus Timing Characteristics

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} to AGND or DGND . . . . . −0.3 V, + 7 V
AGND, RTN to DGND . . . . . −0.3 V, V_{CC} + 0.3 V
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CLKIN, DB0–DB9,
$\overline{BUSY/INT}$ to DGND . . . . . −0.3 V, V_{CC} + 0.3 V
Analog Input Voltage to AGND . . . . . −0.3 V, V_{CC} + 0.3 V
REFOUT to AGND . . . . . −0.3 V, V_{CC} + 0.3 V
REFIN to AGND . . . . . −0.3 V, V_{CC} + 0.3 V
Operating Temperature Range
All Versions . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +150°C
DIP Package, Power Dissipation . . . . . 875 mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering (10 sec) . . . . . +260°C
SOIC Packages, Power Dissipation . . . . . 875 mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
PQFP Package, Power Dissipation . . . . . 500 mW
θ_{JA} Thermal Impedance . . . . . 95°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

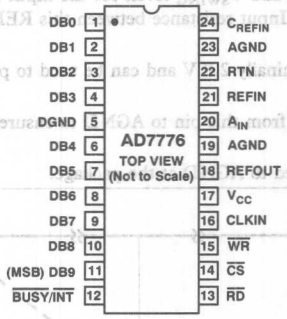
5

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V, which readily accumulate on the human body and on test equipment, can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper precautions are recommended to avoid any performance degradation or loss of functionality.

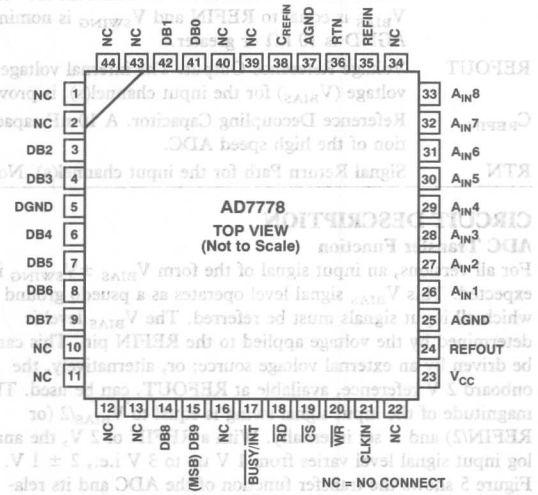
PIN CONFIGURATIONS

24-Pin SOIC



28-Pin DIP & SOIC

44-Pin PQFP



ORDERING GUIDE

Model	Temperature Range	No. of Channels	Package Option[1, 2]
AD7776AR[3]	−40°C to +85°C	1	R-24
AD7777AN	−40°C to +85°C	4	N-28
AD7777AR[3]	−40°C to +85°C	4	R-28
AD7778AS[3]	−40°C to +85°C	8	S-44

NOTES
[1]R = SOIC, N = Plastic DIP, S = PQFP.
[2]For outline information see Package Information section.
[3]Analog Devices reserves the right to ship devices branded with a J in place of the A, e.g., AD7776JR instead of AD7776AR. Temperature range remains −40°C to +85°C.

V_{CC}	+5 V Power Supply.
AGND	Analog Ground.
DGND	Digital Ground. Ground reference for digital circuitry.
DB0–DB9	Input/Output Data Bus. This is a bidirectional data port from which ADC output data may be read and to which control register data may be written.
$\overline{BUSY}/\overline{INT}$	Busy/Interrupt Output. Active low logic output indicating A/D converter status. This logic output has two modes of operation depending on whether location CR9 of the control register has been set low or high: If CR9 is set low, then the $\overline{BUSY}/\overline{INT}$ output will behave as a $\overline{BUSY}$ signal. The $\overline{BUSY}$ signal will go low and stay low for the duration of a single conversion, or if simultaneous sampling has been selected, $\overline{BUSY}$ will stay low for the duration of both conversions. If CR9 is set high, then the $\overline{BUSY}/\overline{INT}$ output behaves as an INTERRUPT signal. The $\overline{INT}$ signal will go low and remain low after either a single conversion is completed or after a double conversion is completed if simultaneous sampling has been selected. With CR9 high, the falling edge of $\overline{WR}$ or $\overline{RD}$ resets the $\overline{INT}$ line high.
$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
$\overline{WR}$	Write Input (Active Low). It is used in conjunction with $\overline{CS}$ to write data to the control register. Data is latched to the registers on the rising edge of $\overline{WR}$. Following the rising edge of $\overline{WR}$, the analog input is acquired and a conversion is started.
$\overline{RD}$	Read Input (Active Low). It is used in conjunction with $\overline{CS}$ to enable the data outputs from the ADC registers.
$A_{IN}1–8$	Analog Inputs 1–8. The analog input range is $V_{BIAS} \pm V_{SWING}$ where V_{BIAS} and V_{SWING} are defined by the reference voltage applied to REFIN. Input resistance between any of the analog input pins and AGND is 10 kΩ or greater.
REFIN	Voltage Reference Input. The AD7776/AD7777/AD7778 are specified over a voltage reference range of 1.9 V to 2.1 V with a nominal value of 2.0 V. This REFIN voltage provides the V_{BIAS} and V_{SWING} levels for the input channel(s). V_{BIAS} is equal to REFIN and V_{SWING} is nominally equal to REFIN/2. Input resistance between this REFIN pin and AGND is 10 kΩ or greater.
REFOUT	Voltage Reference Output. The internal voltage reference, which is nominally 2.0 V and can be used to provide the bias voltage (V_{BIAS}) for the input channel(s), is provided at this pin.
C_{REFIN}	Reference Decoupling Capacitor. A 10 nF capacitor must be connected from this pin to AGND to ensure correct operation of the high speed ADC.
RTN	Signal Return Path for the input channel(s). Normally RTN is connected to AGND at the package.

CIRCUIT DESCRIPTION

ADC Transfer Function

For all versions, an input signal of the form $V_{BIAS} \pm V_{SWING}$ is expected. This V_{BIAS} signal level operates as a psuedo ground to which all input signals must be referred. The V_{BIAS} level is determined by the voltage applied to the REFIN pin. This can be driven by an external voltage source; or, alternatively, the onboard 2 V reference, available at REFOUT, can be used. The magnitude of the input signal swing is equal to $V_{BIAS}/2$ (or REFIN/2) and is set internally. With a REFIN of 2 V, the analog input signal level varies from 1 V up to 3 V i.e., 2 ± 1 V. Figure 5 shows the transfer function of the ADC and its relationship to V_{BIAS} and V_{SWING}. The half-scale twos complement code of the ADC, 000 Hex (00 0000 0000 Binary), occurs at an input voltage equal to V_{BIAS}. The input full-scale range of the ADC is equal to 2 V_{SWING}, so that the Plus Full-Scale transition (1FE to 1FF) occurs at a voltage equal to $V_{BIAS} + V_{SWING} - 1.5$ LSBs and the minus full-scale code transition (200 to 201) occurs at a voltage $V_{BIAS} - V_{SWING} + 0.5$ LSBs.

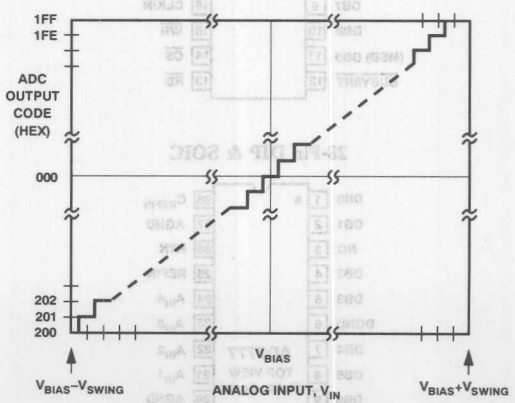


Figure 5. ADC Transfer Function

CONTROL REGISTER

The control register is 10-bits wide and can only be written to. On power-on, all locations in the control register are automatically loaded with 0s. For the single channel AD7776, locations CR0 to CR6 of the control register are "don't cares." For the quad channel AD7777, locations CR2 and CR5 are "don't cares." Individual bit functions are described below.

CR0–CR2: Channel Address Locations. Determines which channel will be selected and converted for single channel operation. For simultaneous sampling operation CR0–CR2 holds the address of one of the two channels to be sampled.

AD7776

CR2	CR1	CR0	Function
X*	X	X	Select $A_{IN}1$

*X = Don't Care

AD7777

CR2	CR1	CR0	Function
X*	0	0	Select $A_{IN}1$
X	0	1	Select $A_{IN}2$
X	1	0	Select $A_{IN}3$
X	1	1	Select $A_{IN}4$

*X = Don't Care

AD7778

CR2	CR1	CR0	Function
0	0	0	Select $A_{IN}1$
0	0	1	Select $A_{IN}2$
0	1	0	Select $A_{IN}3$
0	1	1	Select $A_{IN}4$
1	0	0	Select $A_{IN}5$
1	0	1	Select $A_{IN}6$
1	1	0	Select $A_{IN}7$
1	1	1	Select $A_{IN}8$

CR3–CR5: Channel Address Locations. Only applicable for simultaneous sampling with the AD7777 or AD7778 when CR3–CR5 holds the address of the second channel to be sampled.

AD7777

CR5	CR4	CR3	Function
X*	0	0	Select $A_{IN}1$
X	0	1	Select $A_{IN}2$
X	1	0	Select $A_{IN}3$
X	1	1	Select $A_{IN}4$

*X = Don't Care

AD7778

CR5	CR4	CR3	Function
0	0	0	Select $A_{IN}1$
0	0	1	Select $A_{IN}2$
0	1	0	Select $A_{IN}3$
0	1	1	Select $A_{IN}4$
1	0	0	Select $A_{IN}5$
1	0	1	Select $A_{IN}6$
1	1	0	Select $A_{IN}7$
1	1	1	Select $A_{IN}8$

CR6: Determines whether operation is on a single channel or simultaneous sampling on two channels. Location CR6 is a "don't care" for the AD7776.

CR6	Function
0	Single channel operation. Channel select address is contained in locations CR0–CR2.
1	Two channels simultaneously sampled and sequentially converted. Channel select addresses contained in locations CR0–CR2 and CR3–CR5.

CR7: Determines whether the device is in the normal operating mode or in the half-scale test mode.

CR7	Function
0	Normal Operating Mode
1	Half-Scale Test Mode

In the half-scale test mode REFIN is internally connected as an analog input(s). In this mode locations CR0-CR2 and CR3-CR5 are all "don't cares" since it is REFIN which will be converted. For the AD7777 and AD7778, the contents of location CR6 still determine whether a single or a double conversion is carried out on the REFIN level.

CR8: Determines whether the device is in the normal operating mode or in the power-down mode.

CR8	Function
0	Normal Operating Mode
1	Power-down Mode

In the power-down mode all linear circuitry is turned off and the REFOUT output is pulled weakly (5 kΩ) to AGND. The input impedance of the analog inputs and of the REFIN input remains the same in either normal mode or power-down mode. See under Circuit Description – Power-Down Mode.

CR9: Determines whether $\overline{\text{BUSY/INT}}$ output flag goes low and remains low during conversion(s) or else goes low and remains low after the conversion(s) is (are) complete.

CR9	$\overline{\text{BUSY/INT}}$ Functionality
0	Output goes low and remains low during conversion(s).
1	Output goes low and remains low after conversion(s) is (are) complete.

ADC Conversion Start Timing

Figure 6 shows the operating waveforms for the start of a conversion cycle. On the rising edge of $\overline{\text{WR}}$, the conversion cycle starts with the acquisition and tracking of the selected ADC channel, $A_{IN}1$–8. The analog input voltage is held 40 ns (typically) after the first rising edge of CLKIN following four complete CLKIN cycles. If t_D in Figure 6 is greater than 12 ns, then the falling edge of CLKIN as shown will be seen as the first falling clock edge. If t_D is less than 12 ns, the first falling clock edge to be recognized will not occur until one cycle later.

Following the "hold" on the analog input(s), two complete CLKIN cycles are allowed for settling purposes before the MSB decision is made. The actual decision point occurs approximately 40 ns after the rising edge of CLKIN as shown in Figure 6. A further two CLKIN cycles are allowed for the second MSB decision. The succeeding bit decisions are made approximately 40 ns after each rising edge of CLKIN until the conversion is complete. At the end of conversion, if a single conversion has been requested (CR6 = 0), the $\overline{\text{BUSY/INT}}$ line changes

state (as programmed by CR9), and the SAR contents are transferred to the first register ADCREG1. The SAR is then reset in readiness for a new conversion. If simultaneous sampling has been requested (CR6 = 1), no change occurs in the status of the $\overline{BUSY/INT}$ output and the ADC automatically starts the second conversion. At the end of this conversion the $\overline{BUSY/INT}$ line changes state (as programmed by CR9) and the SAR contents are transferred to the second register, ADCREG2.

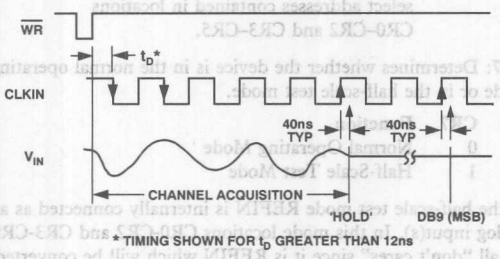


Figure 6. ADC Conversion Start Timing

Track-and-Hold

The track-and-hold (T/H) amplifiers on the analog input(s) of the AD7776/AD7777/AD7778 allow the ADC to accurately convert an input sine wave of 2 V peak-peak amplitude up to a frequency of 189 kHz, the Nyquist frequency of the ADC when operated at its maximum throughput rate of 378 kHz. This maximum rate of conversion includes conversion time and time between conversions. Because the input bandwidth of the track-and-hold is much greater than 189 kHz, the input signal should be band limited to avoid folding unwanted signals into the band of interest.

Power-Down

The AD7776/AD7777/AD7778 can be placed in a power-down mode simply by writing a logic high to location CR8 of the control register. The following changes are effected immediately on writing a "1" to location CR8:

- Any conversion that is in progress is terminated.
- If a conversion is in progress, then the leading edge of $\overline{WR}$ immediately drives the $\overline{BUSY/INT}$ output high.
- All the linear circuitry is turned off.
- The REFOUT output stops being driven and is pulled weakly (5 kΩ) to analog ground.

Control inputs $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ retain their purpose while the AD7776/AD7777/AD7778 is in power-down. If no conversions are in progress when the AD7776/AD7777/AD7778 is placed into the power-down modes, the contents of the ADC registers, ADCREG1 and ADCREG2, are retained during power-down and can be read as normal. On returning to normal operating mode a new conversion (or conversions, dependent on CR6) is automatically started. On completion, the invalid conversion results are loaded into the ADC registers losing the previous valid results.

In order to achieve the lowest possible power consumption in the power-down mode special attention must be paid to the state of the digital and analog inputs and outputs:

- Because each analog input channel sees a resistive divider to AGND, the input resistance of which does not change between normal and power-down modes, driving the analog input signals to 0 V or as close as possible to 0 V will minimize the power dissipated in the input signal conditioning circuitry.
- Similarly, the REFIN input sees a resistive divider to AGND, the input resistance of which does not change between normal and power-down modes. If an external reference is being used, then driving this reference input to 0 V or as close as possible to 0 V will minimize the power dissipated in the input signal conditioning circuitry.
- Since the REFOUT pin is pulled to AGND via, typically, a 5 kΩ resistor, any voltage above 0 V that this output may be pulled to by external circuitry will dissipate unnecessary power.
- Digital inputs $\overline{CS}$, $\overline{WR}$ & $\overline{RD}$ should all be held at V_{CC} or as close as possible. CLKIN should be held as close as possible to either 0 V or V_{CC}.
- Since the $\overline{BUSY/INT}$ output is actively driven to a logic high, any loading on this pin to 0 V will dissipate power.

The AD7776/AD7777/AD7778 comes out of the power-down mode when a Logic "0" is written to location CR8 of the control register. Note that the contents of the other locations in the control register are retained when the device is placed in power-down and are valid when power is restored. However coming out of power-down provides an opportunity to reload the complete contents of the control register without any extra instructions.

Microprocessor Interfacing Circuits

The AD7776/AD7777/AD7778 family of ADCs is intended to interface to DSP machines such as the ADSP-2101, ADSP-2105, the TMS320 family and microcontrollers such as the 80C196 family.

Figure 7 shows the AD7776/AD7777/AD7778 interfaced to the TMS320C10 @ 20.5 MHz and the TMS320C14 @ 25 MHz. Figure 8 shows the interface with the TMS320C25 @ 40 MHz. Note that one wait state is required with this interface. The ADSP-2101-50 and the ADSP-2105-40 interface is shown in Figure 9. One wait state is required with either of these machines.

Figure 10 shows the interface with the 80C196KB @ 12 MHz and the 80C196KC @ 16 MHz. One wait state is required with the 16 MHz machine. The 80C196 is configured to operate with a 16-bit multiplexed address/data bus.

Table I gives a truth table for the AD7776/AD7777/AD7778 and summarizes their microprocessor interfacing features. Note that a read instruction to any of the devices while a conversation is in progress will immediately stop that conversion and return unreliable data over the data bus.

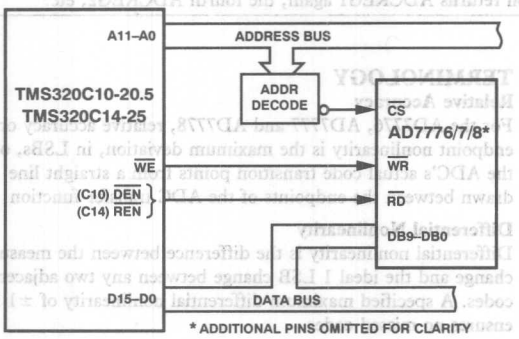


Figure 7. AD7776/AD7777/AD7778 to TMS320C10 and TMS320C14 Interface

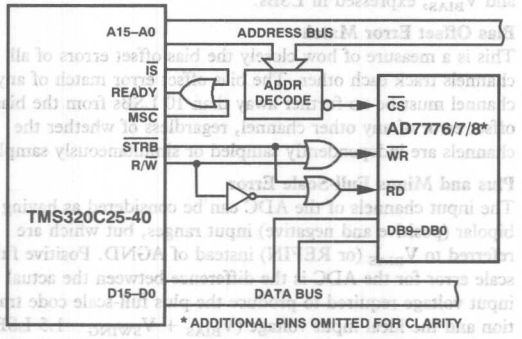


Figure 8. AD7776/AD7777/AD7778 to TMS320C25 Interface

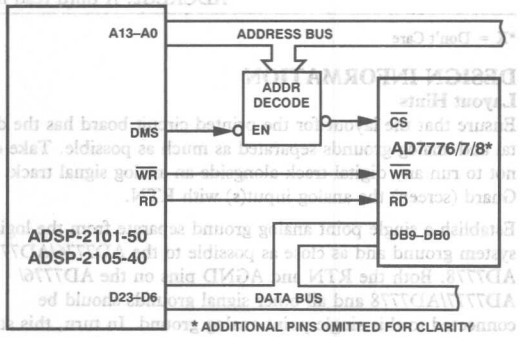


Figure 9. AD7776/AD7777/AD7778 to ADSP-2101 and ADSP-2105 Interface

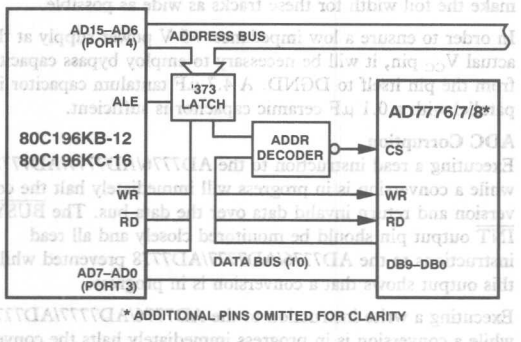


Figure 10. AD7776/AD7777/AD7778 to 80C196 Interface

CS	RD	WR	DB0–DB9	Function/Comments
1	X*	X*	High Z	Data Port High Impedance
0	1	↓	CR Data	Load control register (CR) data to control register and start a conversion.
0	↓	1	ADC Data	ADC data placed on data bus. Depending upon location CR6 of the control register, one or two Read instructions will be required. If CR6 is low, i.e., single channel conversion selected, a read instruction returns the contents of ADCREG1. Succeeding read instructions continue to return the contents of ADCREG1. If CR6 is high, i.e., simultaneous sampling (double conversion) selected, the first read instruction returns the contents of ADCREG1 while the second read instruction returns the contents of ADCREG2. A third read instruction returns ADCREG1 again, the fourth ADCREG2, etc.

*X = Don't Care

DESIGN INFORMATION

Layout Hints

Ensure that the layout for the printed circuit board has the digital and analog grounds separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input(s) with RTN.

Establish a single point analog ground separate from the logic system ground and as close as possible to the AD7776/AD7777/AD7778. Both the RTN and AGND pins on the AD7776/AD7777/AD7778 and all other signal grounds should be connected to this single point analog ground. In turn, this star ground should be connected to the digital ground at one point only—preferably at the low impedance power supply itself.

Low impedance analog and digital power supply common returns are important for correct operation of the devices, so make the foil width for these tracks as wide as possible.

In order to ensure a low impedance +5 V power supply at the actual V_{CC} pin, it will be necessary to employ bypass capacitors from the pin itself to DGND. A 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor is sufficient.

ADC Corruption

Executing a read instruction to the AD7776/AD7777/AD7778 while a conversion is in progress will immediately halt the conversion and return invalid data over the data bus. The $\overline{BUSY}$/$\overline{INT}$ output pin should be monitored closely and all read instructions to the AD7776/AD7777/AD7778 prevented while this output shows that a conversion is in progress.

Executing a write instruction to the AD7776/AD7777/AD7778 while a conversion is in progress immediately halts the conversion, the falling edge of $\overline{WR}$ driving the $\overline{BUSY}$/$\overline{INT}$ output high. The analog input(s) is sampled as normal and a new conversion sequence (dependent upon CR6) is started.

ADC Conversion Time

Although each conversion takes only 14 CLKIN cycles, it can take between 4.5 to 5.5 CLKIN cycles to acquire the analog input(s) after the $\overline{WR}$ input goes high and before any conversions start.

TERMINOLOGY

Relative Accuracy

For the AD7776, AD7777 and AD7778, relative accuracy or endpoint nonlinearity is the maximum deviation, in LSBs, of the ADC's actual code transition points from a straight line drawn between the endpoints of the ADC transfer function.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified maximum differential nonlinearity of ±1 LSB ensures no missed codes.

Bias Offset Error

For an ideal 10-bit ADC, the output code for an input voltage equal to V_{BIAS} should be midscale. The bias offset error is the difference between the actual midpoint voltage for midscale code and V_{BIAS}, expressed in LSBs.

Bias Offset Error Match

This is a measure of how closely the bias offset errors of all channels track each other. The bias offset error match of any channel must be no further away than 10 LSBs from the bias offset error of any other channel, regardless of whether the channels are independently sampled or simultaneously sampled.

Plus and Minus Full-Scale Error

The input channels of the ADC can be considered as having bipolar (positive and negative) input ranges, but which are referred to V_{BIAS} (or REFIN) instead of AGND. Positive full-scale error for the ADC is the difference between the actual input voltage required to produce the plus full-scale code transition and the ideal input voltage ($V_{BIAS} + V_{SWING} - 1.5$ LSB), expressed in LSBs. Minus full-scale error is similarly specified for the minus full-scale code transition, relative to the ideal input voltage for this transition ($V_{BIAS} - V_{SWING} + 0.5$ LSB). Note that the full-scale errors for the ADC input channels are measured after their respective bias offset errors have been adjusted out.

Plus and Minus Full-Scale Error Match

This is a measure of how closely the full-scale errors of all channels track each other. The full-scale error match of any channel must be no further away than 10 LSBs from the respective full-scale error of any other channel, regardless of whether the channels are independently sampled or simultaneously sampled.

This is defined as the maximum current which will flow either into or out of the REFOUT pin if this pin is shorted to any potential between 0 V and V_{CC}. This condition can be allowed for up to 10 seconds provided that the power dissipation of the package is not exceeded.

Signal-to-Noise and Distortion Ratio, S/(N+D)

Signal-to-noise and distortion ratio, S/(N+D), is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is given in decibels.

Total Harmonic Distortion, THD

Total harmonic distortion is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels. For the AD7776/AD7777/AD7778, Total harmonic distortion (THD) is defined as:

$$20\ log = \frac{(V2^2 + V3^2 + V4^2 + V5^2 + V6^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and *V2*, *V3*, *V4*, *V5* and *V6* are the rms amplitudes of the individual harmonics.

Intermodulation Distortion, IMD

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa + nfb, where m, n = 0, 1, 2, 3. Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms include (fa + fb) and (fa − fb) and the third order terms include (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb).

Channel-to-Channel Isolation

Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 100 kHz sine wave signal to any one of the input channels and monitoring the remaining channels. The figure given is the worst case across all channels.

DIGITAL SIGNAL PROCESSING APPLICATIONS

In digital signal processing (DSP) application areas like voice recognition, echo cancellation and adaptive filtering, the dynamic characteristics S/(N+D), THD & IMD of the ADC are critical. The AD7776/AD7777/AD7778 are specified dynamically as well as with standard dc specifications. Because the track/hold amplifier has a wide bandwidth, an antialiasing filter should be placed on the analog inputs to avoid aliasing of high frequency noise back into the bands of interest.

The dynamic performance of the ADC is evaluated by applying a sine wave signal of very low distortion to a single analog input which is sampled at a 380.95 kHz sampling rate. A fast Fourier transform (FFT) plot or histogram plot is then generated from which the signal to noise and distortion, harmonic distortion and dynamic differential nonlinearity data can be obtained. Similarly, for intermodulation distortion, an input signal consisting of two pure sine waves at different frequencies is applied to the AD7776/AD7777/AD7778.

the AD7778 with an input signal of 99.88 kHz. The SNR is 58.71 dB. It can be seen that most of the harmonics are buried in the noise floor. It should be noted that the harmonics are taken into account when calculating the S/(N+D).

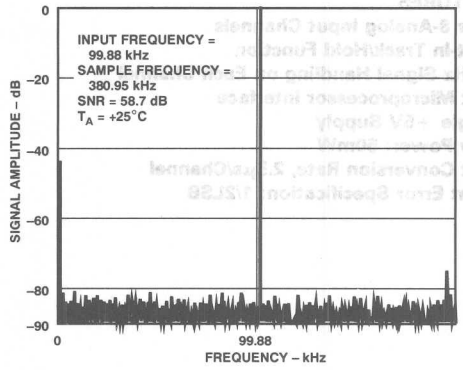


Figure 11. ADC FFT Plot

The relationship between S/(N+D) and resolution (n) is expressed by the following equation:

$$S/(N+D) = (6.02n + 1.76)\ dB$$

This is for an ideal part with no differential or integral linearity errors. These errors will cause a degradation in S/(N+D). By working backwards from the above equation, it is possible to get a measure of ADC performance expressed in effective number of bits (n).

$$n(effective) = \frac{S/(N+D)\ (dB) - 1.76}{6.02}$$

The effective number of bits plotted vs. frequency for a single channel of the AD7778 is shown in Figure 12. The effective number of bits is typically 9.5.

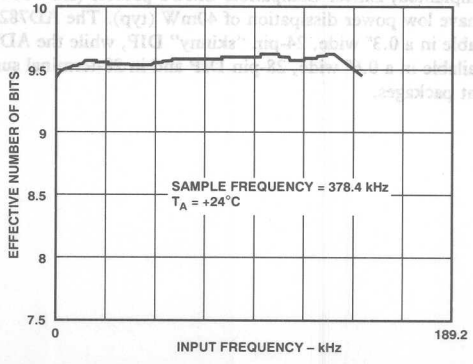


Figure 12. Effective Number of Bits vs. Frequency

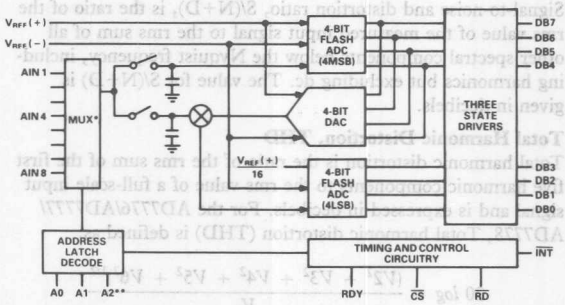
LC²MOS High Speed 4- & 8-Channel 8-Bit ADCs

AD7824/AD7828

FEATURES

- 4- or 8-Analog Input Channels
- Built-In Track/Hold Function
- 10kHz Signal Handling on Each Channel
- Fast Microprocessor Interface
- Single +5V Supply
- Low Power: 50mW
- Fast Conversion Rate, 2.5µs/Channel
- Tight Error Specification: 1/2LSB

FUNCTIONAL BLOCK DIAGRAM



*AD7824 – 4-CHANNEL MUX
AD7828 – 8-CHANNEL MUX
**A2 – AD7828 ONLY

GENERAL DESCRIPTION

The AD7824 and AD7828 are high-speed, multichannel, 8-bit ADCs with a choice of 4 (AD7824) or 8 (AD7828) multiplexed analog inputs. A half-flash conversion technique gives a fast conversion rate of 2.5µs per channel and the parts have a built-in track/hold function capable of digitizing full-scale signals of 10kHz (157mV/µs slew rate) on all channels. The AD7824 and AD7828 operate from a single +5V supply and have an analog input range of 0 to +5V, using an external +5V reference.

Microprocessor interfacing of the parts is simple, using standard Chip Select ($\overline{CS}$) and Read ($\overline{RD}$) signals to intitiate the conversion and read the data from the three-state data outputs. The half-flash conversion technique means that there is no need to generate a clock signal for the ADC. The AD7824 and AD7828 can be interfaced easily to most popular microprocessors.

The AD7824 and AD7828 are fabricated in an advanced, all ion-implanted, Linear-Compatible CMOS process (LC²MOS) and have low power dissipation of 40mW (typ). The AD7824 is available in a 0.3" wide, 24-pin "skinny" DIP, while the AD7828 is available in a 0.6" wide, 28-pin DIP and in 28-terminal surface mount packages.

PRODUCT HIGHLIGHTS

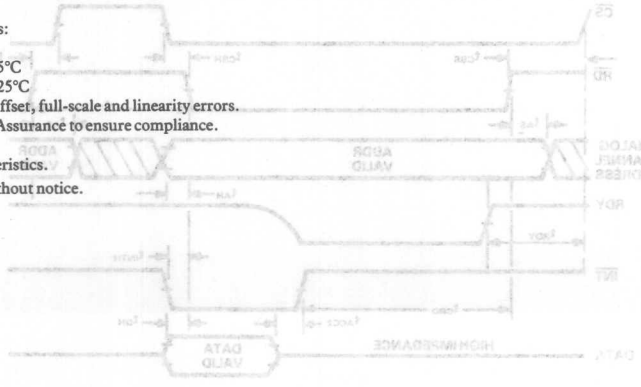
1. 4- or 8-channel input multiplexer gives cost-effective space-saving multichannel ADC system.
2. Fast conversion rate of 2.5µs/channel features a per channel sampling frequency of 100kHz for the AD7824 or 50kHz for the AD7828.
3. Built-in track-hold function allows handling of 4- or 8-channels up to 10kHz bandwidth (157mV/µs slew rate).
4. Tight total unadjusted error spec and channel-to-channel matching eliminate the need for user trims.
5. Single +5V supply simplifies system power requirements.
6. Fast, easy-to-use digital interface allows connection to most popular microprocessors with minimal external components. No clock signal is required for the ADC.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (V_{DD} = +5V, $V_{REF}(+)$ = +5V, $V_{REF}(-)$ = GND = 0V unless otherwise noted. All specifications T_{min} to T_{max} unless otherwise noted. Specifications apply for Mode 0.)

Parameter	K Version[1]	L Version	B, T Versions	C, U Versions	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[2]	±1	±1/2	±1	±1/2	LSB max	
Minimum Resolution for which						
No Missing Codes are guaranteed	8	8	8	8	Bits	
Channel to Channel Mismatch	±1/4	±1/4	±1/4	±1/4	LSB max	
REFERENCE INPUT						
Input Resistance	1.0/4.0	1.0/4.0	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
$V_{REF}(+)$ Input Voltage Range	$V_{REF}(-)$/ V_{DD}	$V_{REF}(-)$/ V_{DD}	$V_{REF}(-)$/ V_{DD}	$V_{REF}(-)$/ V_{DD}	V min/V max	
$V_{REF}(-)$ Input Voltage Range	GND/ $V_{REF}(+)$	GND/ $V_{REF}(+)$	GND/ $V_{REF}(+)$	GND/ $V_{REF}(+)$	V min/V max	
ANALOG INPUT						
Input Voltage Range	$V_{REF}(-)$/ $V_{REF}(+)$	$V_{REF}(-)$/ $V_{REF}(+)$	$V_{REF}(-)$/ $V_{REF}(+)$	$V_{REF}(-)$/ $V_{REF}(+)$	V min/V max	
Input Leakage Current	±3	±3	±3	±3	μA max	Analog Input Any Channel
Input Capacitance[3]	45	45	45	45	pF typ	0 to +5V
LOGIC INPUTS						
$\overline{RD}$, $\overline{CS}$, A0, A1 & A2						
V_{INH}	2.4	2.4	2.4	2.4	V min	
V_{INL}	0.8	0.8	0.8	0.8	V max	
I_{INH}	1	1	1	1	μA max	
I_{INL}	−1	−1	−1	−1	μA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5pF
LOGIC OUTPUTS						
DB0-DB7 & $\overline{INT}$						
V_{OH}	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 360μA
V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
I_{OUT} (DB0-DB7)	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5pF
RDY						
V_{OL}[4]	0.4	0.4	0.4	0.4	V max	I_{SINK} = 2.6mA
I_{OUT}	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance	8	8	8	8	pF max	Typically 5pF
SLEW RATE, TRACKING[3]	0.7	0.7	0.7	0.7	V/μs typ	
	0.157	0.157	0.157	0.157	V/μs max	
POWER SUPPLY						
V_{DD}	5	5	5	5	Volts	±5% for Specified Performance
I_{DD}[5]	16	16	20	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 2.4V
Power Dissipation	50	50	50	50	mW typ	
	80	80	100	100	mW max	
Power Supply Sensitivity	±1/4	±1/4	±1/4	±1/4	LSB max	±1/16LSB typ V_{DD} = 5V ±5%

NOTES
[1]Temperature Ranges are as follows:
K, L Versions; 0 to +70°C
B, C Versions; −40°C to +85°C
T, U Versions; −55°C to +125°C
[2]Total Unadjusted Error includes offset, full-scale and linearity errors.
[3]Sample tested at 25°C by Product Assurance to ensure compliance.
[4]RDY is an open drain output.
[5]See Typical Performance Characteristics.
Specifications subject to change without notice.



Parameter	Limit at 25°C (All Grades)	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Limit at T_{min}, T_{max} (T, U Grades)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{AS}	0	0	0	ns min	Multiplexer Address Setup Time
t_{AH}	30	35	40	ns min	Multiplexer Address Hold Time
t_{RDY}[2]	40	60	60	ns max	$\overline{CS}$ to RDY Delay. Pull-Up Resistor 5kΩ.
t_{CRD}	2.0	2.4	2.8	μs max	Conversion Time, Mode 0
t_{ACC1}[3]	85	110	120	ns max	Data Access Time after $\overline{RD}$
t_{ACC2}[3]	50	60	70	ns max	Data Access Time after $\overline{INT}$, Mode 0
t_{INTH}[2]	40	65	70	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay
	75	100	100	ns max	
t_{DH}[4]	60	70	70	ns max	Data Hold Time
t_P	500	500	600	ns min	Delay Time between Conversions
t_{RD}	60	80	80	ns min	Read Pulse Width, Mode 1
	600	500	400	ns max	

NOTES
[1]Sample tested at 25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]C_L = 50pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

AD7824 A1	AD7824 A0	AD7828 A2	AD7828 A1	AD7828 A0	CHANNEL
0	0	0	0	0	AIN 1
0	1	0	0	1	AIN 2
1	0	0	1	0	AIN 3
1	1	0	1	1	AIN 4
		1	0	0	AIN 5
		1	0	1	AIN 6
		1	1	0	AIN 7
		1	1	1	AIN 8

Table I. Truth Table for Input Channel Selection

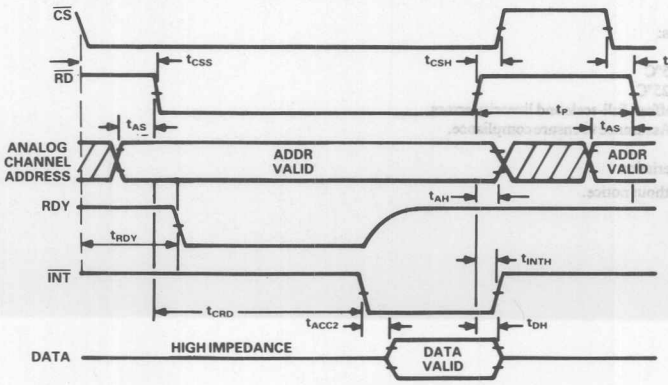


Figure 1. Mode 0 Timing Diagram

V_{DD} . . . . . 0V, +7V
Digital Input Voltage to GND
($\overline{RD}$, $\overline{CS}$, A0, A1 & A2) . . . . . −0.3V, V_{DD} +0.3V
Digital Output Voltage to GND
(DB0, DB7, RDY & $\overline{INT}$) . . . . . −0.3V, V_{DD} +0.3V
V_{REF} (+) to GND . . . . . V_{REF} (−), V_{DD} +0.3V
V_{REF} (−) to GND . . . . . 0V, V_{REF} (+)
Analog Input (Any Channel) . . . . . −0.3V, V_{DD} +0.3V
Operating Temperature Range
Commercial (K, L Versions) . . . . . 0 to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

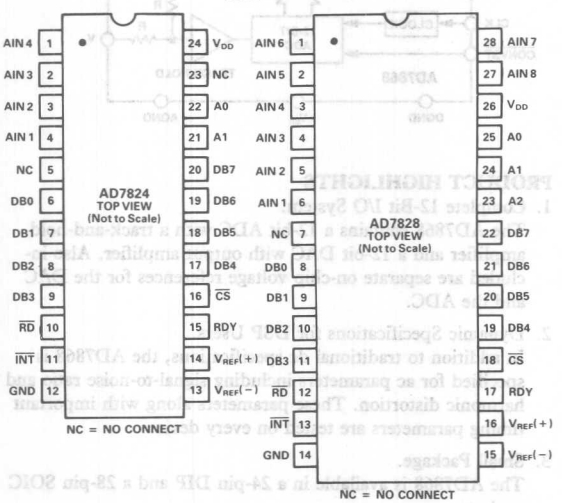
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

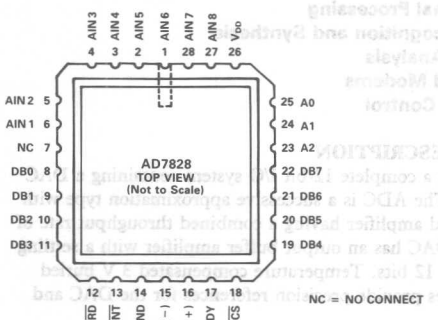
5

PIN CONFIGURATIONS

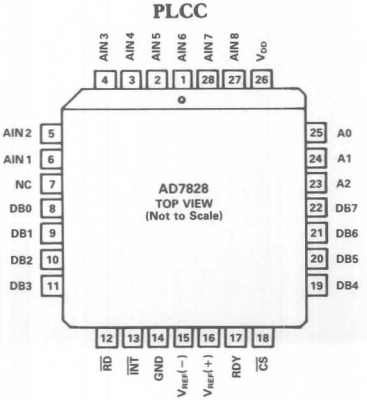
DIP



LCCC



PLCC



ORDERING GUIDE

Model	Temperature Range	Total Unadjusted Error (LSBs)	Package Option[1]
AD7824KN	0 to +70°C	±1	N-24
AD7824LN	0 to +70°C	±1/2	N-24
AD7824KR	0 to +70°C	±1	R-24
AD7824BQ	−40°C to +85°C	±1	Q-24
AD7824CQ	−40°C to +85°C	±1/2	Q-24
AD7824TQ[2]	−55°C to +125°C	±1	Q-24
AD7824UQ[2]	−55°C to +125°C	±1/2	Q-24
AD7828KN	0 to +70°C	±1	N-28
AD7828LN	0 to +70°C	±1/2	N-28
AD7828KP	0 to +70°C	±1	P-28A
AD7828LP	0 to +70°C	±1/2	P-28A
AD7828BQ	−40°C to +85°C	±1	Q-28
AD7828CQ	−40°C to +85°C	±1/2	Q-28
AD7828TQ[2]	−55°C to +125°C	±1	Q-28
AD7828UQ[2]	−55°C to +125°C	±1/2	Q-28
AD7828TE[2]	−55°C to +125°C	±1	E-28A
AD7828UE[2]	−55°C to +125°C	±1/2	E-28A

NOTES
[1]N = Plastic DIP; Q = Hermetic DIP, R = Small Outline IC; P = Plastic Leaded Chip Carrier; E = Leadless Ceramic Chip Carrier. For outline information see Package Information section.
[2]Available to /883B processing only. Contact our local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC Drawing #5692-88764.

LC²MOS
Complete, 12-Bit Analog I/O System
AD7868

FEATURES

Complete 12-Bit I/O System, Comprising:
- **12-Bit ADC with Track/Hold Amplifier**
  - **83 kHz Throughput Rate**
  - **72 dB SNR**
- **12-Bit DAC with Output Amplifier**
  - **3 μs Settling Time**
  - **72 dB SNR**
- **On-Chip Voltage Reference**

Operates from ±5 V Supplies
Low Power – 130 mW typ
Small 0.3" Wide DIP

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

GENERAL DESCRIPTION

The AD7868 is a complete 12-bit I/O system containing a DAC and an ADC. The ADC is a successive approximation type with a track-and-hold amplifier having a combined throughput rate of 83 kHz. The DAC has an output buffer amplifier with a settling time of 3 μs to 12 bits. Temperature compensated 3 V buried Zener references provide precision references for the DAC and ADC.

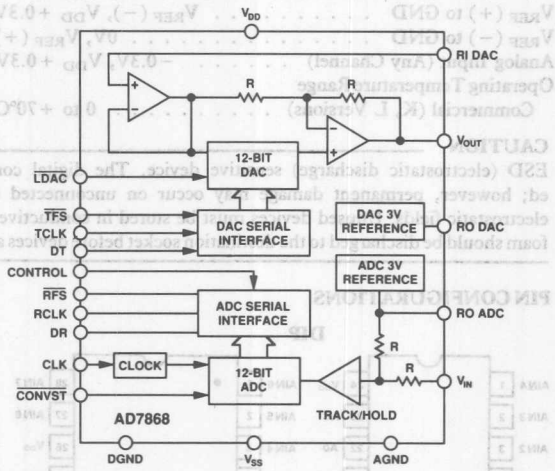
Interfacing to both the DAC and ADC is serial, minimizing pin count and giving a small 24-pin package size. Standard control signals allow serial interfacing to most DSP machines. Asynchronous ADC conversion control and DAC updating is made possible with the $\overline{\text{CONVST}}$ and $\overline{\text{LDAC}}$ logic inputs.

The AD7868 operates from ±5 V power supplies, the analog input/output range of the ADC/DAC is ±3 V. The part is fully specified for dynamic parameters such as signal-to-noise ratio and harmonic distortion as well as traditional dc specifications.

The part is available in a 24-pin, 0.3" wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin, plastic SOIC package.

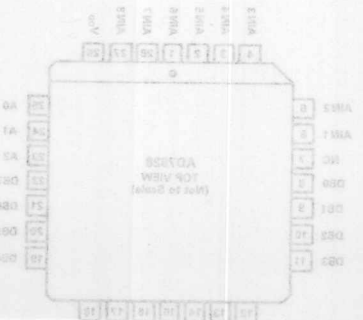
This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Complete 12-Bit I/O System.
   The AD7868 contains a 12-bit ADC with a track-and-hold amplifier and a 12-bit DAC with output amplifier. Also included are separate on-chip voltage references for the DAC and the ADC.
2. Dynamic Specifications for DSP Users.
   In addition to traditional dc specifications, the AD7868 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
3. Small Package.
   The AD7868 is available in a 24-pin DIP and a 28-pin SOIC package.



SPECIFICATIONS

ADC SECTION (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2.0 MHz external. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio[3, 4] (SNR) @ +25°C	70	72	70	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{min} to T_{max}	70	71	70	dB min	Typically 71.5 dB for 0<V_{IN}<41.5 kHz
Total Harmonic Distortion (THD)	−78	−78	−76	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz Typically −84 dB for 0<V_{IN}<41.5 kHz
Peak Harmonic or Spurious Noise	−78	−78	−76	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz Typically −84 dB for 0<V_{IN}<41.5 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	−78	−78	−76	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	2	μs max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	
Bipolar Zero Error	±5	±5	±5	LSB max	
Positive Gain Error[5]	±5	±5	±5	LSB max	
Negative Gain Error[5]	±5	±5	±5	LSB max	
ANALOG INPUT					
Input Voltage Range	±3	±3	±3	Volts	
Input Current	±1	±1	±1	mA max	
REFERENCE OUTPUT[6]					
RO ADC @ +25°C	2.99/3.01	2.99/3.01	2.99/3.01	V min/V max	
RO ADC TC	±25	±25	±25	ppm/°C typ	
RO ADC TC		±40	±50	ppm/°C max	
Reference Load Sensitivity (ΔRO ADC vs. ΔI)	−1.5	−1.5	−1.5	mV max	Reference Load Current Change (0–500 μA), Reference Load Should Not Be Changed During Conversion
LOGIC INPUTS (CONVST, CLK, CONTROL)					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Current[7] (CONTROL Input Only)	±10	±10	±10	μA max	V_{IN} = V_{SS} to DGND
Input Capacitance, C_{IN}[8]	10	10	10	pF max	
LOGIC OUTPUTS					
DR, RFS Outputs					
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA, Pull-Up Resistor = 4.7 kΩ
RCLK Output					
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 2.6 mA, Pull-Up Resistor = 2 kΩ
DR, RFS, RCLK Outputs					
Floating-State Leakage Current	±10	±10	±10	μA max	
Floating-State Output Capacitance[8]	15	15	15	pF max	
CONVERSION TIME					
External Clock	10	10	10	μs max	
Internal Clock	10	10	10	μs max	The Internal Clock Has a Nominal Value of 2.0 MHz
POWER REQUIREMENTS					For Both DAC and ADC
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	22	22	25	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	12	12	13	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	170	170	190	mW max	Typically 130 mW

NOTES
[1]Temperature ranges are as follows: A/B Versions, −40°C to +85°C; T Version, −55°C to +125°C.
V_{IN} = ±3 V.
[3]SNR calculation includes distortion and noise components.
[4]SNR degradation due to asynchronous DAC updating during conversion is 0.1 dB typ.
[5]Measured with respect to internal reference.
[6]For capacitive loads greater than 50 pF a series resistor is required (see INTERNAL REFERENCE section).
[7]Tying the CONTROL input to V_{DD} places the device in a factory test mode where normal operation is not exhibited.
[8]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

DAC SECTION (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, RI DAC = +3 V and decoupled as shown in Figure 2, V_{OUT} Load to AGND; R_L = 2 kΩ, C_L = 100 pF. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal to Noise Ratio[3] (SNR) @ +25°C	70	72	70	dB min	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{min} to T_{max}	70	71	70	dB min	Typically 71.5 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
Total Harmonic Distortion (THD)	−78	−78	−76	dB max	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 83 kHz
					Typically −84 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
Peak Harmonic or Spurious Noise	−78	−78	−76	dB max	V_{OUT} = 1 kHz, f_{SAMPLE} = 83 kHz
					Typically −84 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
DC ACCURACY					
Resolution	12	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±5	±5	±5	LSB max	
Positive Full-Scale Error[5]	±5	±5	±5	LSB max	
Negative Full-Scale Error[5]	±5	±5	±5	LSB max	
REFERENCE OUTPUT[6]					
RO DAC @ +25°C	2.99/3.01	2.99/3.01	2.99/3.01	V min/V max	
RO DAC TC	±25	±25	±25	ppm/°C typ	
RO DAC TC		±40	±50	ppm/°C max	
Reference Load Change					
(ΔRO DAC vs. ΔI)	−1.5	−1.5	− 1.5	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUT					
RI DAC Input Range	2.85/3.15	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	1	1	1	μA max	
LOGIC INPUTS					
(LDAC, TFS, TCLK, DT)					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	10	pF max	
ANALOG OUTPUT					
Output Voltage Range	±3	±3	±3	V nom	
dc Output Impedance	0.3	0.3	0.3	Ω typ	
Short-Circuit Current	20	20	20	mA typ	
AC CHARACTERISTICS[7]					
Voltage Output Settling-Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	3	3	3	μs max	Typically 2 μs
Negative Full-Scale Change	3	3	3	μs max	Typically 2.5 μs
Digital-to-Analog Glitch Impulse	10	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough	2	2	2	nV secs typ	
V_{IN} to V_{OUT} Isolation	100	100	100	dB typ	V_{IN} = ±3 V, 41.5 kHz Sine Wave
POWER REQUIREMENTS	As per ADC Section				

NOTES
[1]Temperature ranges are as follows: A/B Versions, −40°C to +85°C; T Version, −55°C to +125°C.
[2]V_{OUT} (pk-pk) = ±3 V.
[3]SNR calculation includes distortion and noise components.
[4]Using external sample and hold.
[5]Measured with respect to RI DAC and includes bipolar offset error.
[6]For capacitive loads greater than 50 pF a series resistor is required (see INTERNAL REFERENCE section).
[7]Sample tested @ +25°C to ensure compliance.
Specifications subject to notice without notice.

ORDERING GUIDE

Model	Temperature Range	Signal-to-Noise Ratio	Relative Accuracy	Package Option*
AD7868AN	−40°C to +85°C	70 dB	±1/2 LSB typ	N-24
AD7868AQ	−40°C to +85°C	70 dB	±1/2 LSB typ	Q-24
AD7868BN	−40°C to +85°C	72 dB	±1 LSB max	N-24
AD7868BQ	−40°C to +85°C	72 dB	±1 LSB max	Q-24
AD7868AR	−40°C to +85°C	70 dB	±1/2 LSB typ	R-28
AD7868BR	−40°C to +85°C	72 dB	±1 LSB max	R-28

*N = Plastic DIP; Q = Cerdip; R = SOIC (Small Outline IC). For outline information see Package Information section.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V)

Parameter	Limit at T_{min}, T_{max} (A, B Versions)	Limit at T_{min}, T_{max} (T Version)	Units	Conditions/Comments
ADC TIMING				
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2[3]	440	440	ns min	RCLK Cycle Time, Internal Clock
t_3	100	100	ns min	$\overline{RFS}$ to RCLK Falling Edge Setup Time
t_4	20	20	ns min	RCLK Rising Edge to $\overline{RFS}$
	100	100	ns max	
t_5[4]	155	155	ns max	RCLK to Valid Data Delay, C_L = 35 pF
t_6	4	4	ns min	Bus Relinquish Time after RCLK
	100	100	ns max	
t_{13}[5]	2 RCLK +200 to 3 RCLK + 200	2 RCLK +200 to 3 RCLK + 200	ns typ	$\overline{CONVST}$ to $\overline{RFS}$ Delay
DAC TIMING				
t_7	50	50	ns min	$\overline{TFS}$ to TCLK Falling Edge
t_8	75	100	ns min	TCLK Falling Edge to $\overline{TFS}$
t_9[6]	150	200	ns min	TCLK Cycle Time
t_{10}	30	40	ns min	Data Valid to TCLK Setup Time
t_{11}	75	100	ns min	Data Valid to TCLK Hold Time
t_{12}	40	40	ns min	$\overline{LDAC}$ Pulse Width

NOTES

[1]Timing specifications are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]Serial timing is measured with a 4.7 kΩ pull-up resistor on DR and $\overline{RFS}$ and a 2 kΩ pull-up resistor on RCLK. The capacitance on all three outputs is 35 pF.

[3]When using internal clock, RCLK mark/space ratio (measured form a voltage level of 1.6 V) range is 40/60 to 60/40. For external clock, RCLK mark/space ratio = external clock mark/space ratio.

[4]DR will drive higher capacitance loads but this will add to t_5 since it increases the external RC time constant (4.7 kΩ//C_L) and hence the time to reach 2.4 V.

[5]Time 2 RCLK to 3 RCLK depends on conversion start to ADC clock synchronization.

[6]TCLK mark/space ratio is 40/60 to 60/40.

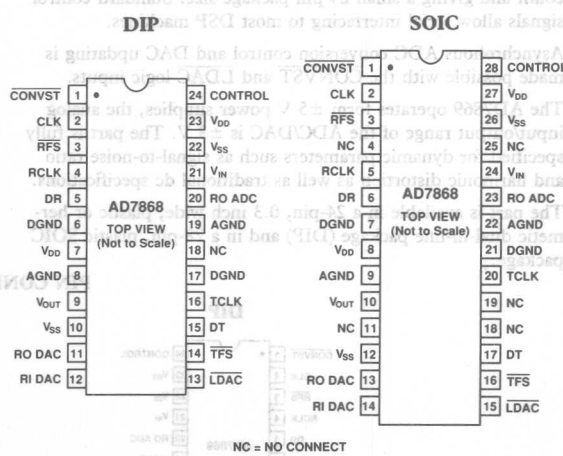
ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	−0.3 V to +7 V
V_{SS} to AGND	+0.3 V to −7 V
AGND to DGND	−0.3 V to V_{DD}+0.3 V
V_{OUT} to AGND	V_{SS} to V_{DD}
V_{IN} to AGND	V_{SS} −0.3 V to V_{DD}+0.3 V
RO ADC to AGND	−0.3 V to V_{DD}+0.3 V
RO DAC to AGND	−0.3 V to V_{DD}+0.3 V
RI DAC to AGND	−0.3 V to V_{DD}+0.3 V
Digital Inputs to DGND	−0.3 V to V_{DD}+0.3 V
Digital Outputs to DGND	−0.3 V to V_{DD}+0.3 V
Operating Temperature Range	
A, B Versions	−40°C to +85°C
T Version	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Any Package) to +75°C	450 mW
Derates above +75°C by	10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS



CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

Complete, 14-Bit Analog I/O System

AD7869

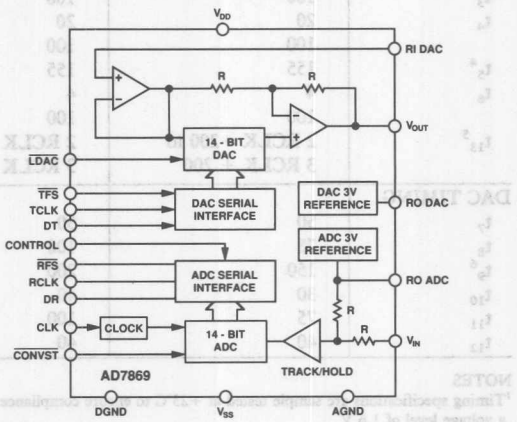
FEATURES

Complete 14-Bit I/O System, Comprising
14-Bit ADC with Track/Hold Amplifier
83 kHz Throughput Rate
14-Bit DAC with Output Amplifier
3.5 μs Settling Time
On-Chip Voltage Reference
Operates from ±5 V Supplies
Low Power – 130 mW typ
Small 0.3″ Wide DIP

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7869 is a complete 14-bit I/O system containing a DAC and an ADC. The ADC is a successive approximation type with a track-and-hold amplifier having a combined throughput rate of 83 kHz. The DAC has an output buffer amplifier with a settling time of 4 μs to 14 bits. Temperature compensated 3 V buried Zener references provide precision references for the DAC and ADC.

Interfacing to both the DAC and ADC is serial, minimizing pin count and giving a small 24-pin package size. Standard control signals allow serial interfacing to most DSP machines.

Asynchronous ADC conversion control and DAC updating is made possible with the $\overline{\text{CONVST}}$ and $\overline{\text{LDAC}}$ logic inputs.

The AD7869 operates form ±5 V power supplies, the analog input/output range of the ADC/DAC is ±3 V. The part is fully specified for dynamic parameters such as signal-to-noise ratio and harmonic distortion as well as traditional dc specifications.

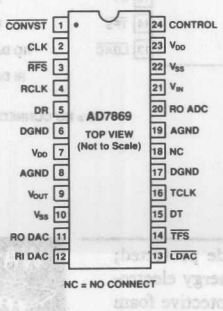
The part is available in a 24-pin, 0.3 inch wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin, plastic SOIC package.

PRODUCT HIGHLIGHTS

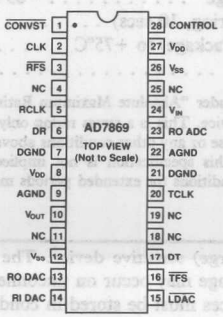
1. Complete 14-Bit I/O System.
   The AD7869 contains a 14-bit ADC with a track-and-hold amplifier and a 14-bit DAC with output amplifier. Also included are separate on-chip voltage references for the DAC and the ADC.
2. Dynamic Specifications for DSP Users.
   In addition to traditional dc specifications, the AD7869 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
3. Small Package.
   The AD7869 is available in a 24-pin DIP and a 28-pin SOIC package.

PIN CONFIGURATIONS

DIP



SOIC



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

ADC SECTION (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ±5%, AGND = DGND = 0 V, f_{CLK} = 2.0 MHz external. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J Version[1]	A Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio[3, 4] (SNR) @ +25°C	78	78	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{min} to T_{max}	78	77	dB min	
Total Harmonic Distortion (THD)	−86	−86	dB typ	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
Peak Harmonic or Spurious Noise	−86	−86	dB typ	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
Intermodulation Distortion (IMD)				
Second Order Terms	−86	−86	dB typ	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−88	−88	dB typ	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	µs max	
DC ACCURACY				
Resolution	14	14	Bits	
Minimum Resolution for Which				
No Missing Codes Are Guaranteed	14	14	Bits	
Integral Nonlinearity	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	
Bipolar Zero Error	±20	±20	LSB max	
Positive Gain Error[5]	±20	±20	LSB max	
Negative Gain Error[5]	±20	±20	LSB max	
ANALOG INPUT				
Input Voltage Range	±3	±3	Volts	
Input Current	±1	±1	mA max	
REFERENCE OUTPUT[6]				
RO ADC @ +25°C	2.99/3.01	2.99/3.01	V min/ V max	
RO ADC TC	±25	±25	ppm/°C typ	
		±40	±ppm/°C max	
Reference Load Sensitivity (ΔRO ADC vs. ΔI)	−1.5	−1.5	mV max	Reference Load Current Change (0–500 µA), Reference Load Should Not Be Changed During Conversion
LOGIC INPUTS (CONVST, CLK, CONTROL)				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current[7] (CONTROL & CLK)	±10	±10	µA max	V_{IN} = V_{SS} to DGND
Input Capacitance, C_{IN}[8]	10	10	pF max	
LOGIC OUTPUTS				
DR, RFS Outputs				
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA, Pull-Up Resistor = 4.7 kΩ
RCLK Output				
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 2.6 mA, Pull-Up Resistor = 2 kΩ
DR, RFS, RCLK Outputs				
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[8]	15	15	pF max	
CONVERSION TIME				
External Clock	10	10	µs max	
Internal Clock	10	10	µs max	The Internal Clock Has a Nominal Value of 2.0 MHz
POWER REQUIREMENTS				For Both DAC and ADC
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	22	22	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	12	12	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	170	170	mW max	Typically 130 mW

NOTES
[1]Temperature ranges are as follows: J Version, 0°C to +70°C; A Version, −40°C to +85°C.
[2]V_{IN} = ±3 V.
[3]SNR calculation includes distortion and noise components.
[4]SNR degradation due to asynchronous DAC updating during conversion is 0.1 dB typ.
[5]Measured with respect to internal reference.
[6]For capacitive loads greater than 50 pF a series resistor is required (see Internal Reference section).
[7]Tying the CONTROL input to V_{DD} places the device in a factory test mode where normal operation is not exhibited.
[8]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

DAC SECTION (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, RI DAC = +3 V and decoupled as shown in Figure 2, V_{OUT} Load to AGND; = 2 kΩ, C_L = 100 pF. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J Version[1]	A Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio[3] (SNR) @ +25°C	78	78	dB min	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{min} to T_{max}	78	77	dB min	Typically 82 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
Total Harmonic Distortion (THD)	−86	−86	dB typ	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 83 kHz
				Typically −84 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
Peak Harmonic or Spurious Noise	−86	−86	dB typ	V_{OUT} = 1 kHz, f_{SAMPLE} = 83 kHz
				Typically −84 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
DC ACCURACY				
Resolution	14	14	Bits	
Integral Nonlinearity	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±10	±10	LSB max	
Positive Full-Scale Error[5]	±10	±10	LSB max	
Negative Full-Scale Error[5]	±10	±10	LSB max	
REFERENCE OUTPUT[6]				
RO DAC @ +25°C	2.99/3.01	2.99/3.01	V min/V max	
RO DAC TC	±25	±25	ppm/°C typ	
		±40	ppm/°C max	
Reference Load Change (ΔRO DAC vs. ΔI)	−1.5	−1.5	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUT				
RI DAC Input Range	2.85/3.15	2.85/3.15	V min/V max	3 V ±5%
Input Current	1	1	μA max	
LOGIC INPUTS (LDAC, TFS, TCLK, DT)				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ±5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ±5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	pF max	
ANALOG OUTPUT				
Output Voltage Range	±3	±3	V nom	
DC Output Impedance	0.3	0.3	Ω typ	
Short-Circuit Current	20	20	mA typ	
AC CHARACTERISTICS[7]				
Voltage Output Settling-Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	4	4	μs max	Typically 3 μs
Negative Full-Scale Change	4	4	μs max	Typically 3.5 μs
Digital-to-Analog Glitch Impulse	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough	2	2	nV secs typ	
V_{IN} to V_{OUT} Isolation	100	100	dB typ	V_{IN} = ±3 V, 41.5 kHz Sine Wave
POWER REQUIREMENTS	As per ADC Section			

NOTES
[1]Temperature ranges are as follows: J Version, 0°C to +70°C; A Version, −40°C to +85°C.
[2]V_{OUT} (p–p) = ±3 V.
[3]SNR calculation includes distortion and noise components.
[4]Using external sample and hold, see Figures 13 to 15.
[5]Measured with respect to REF IN and includes bipolar offset error.
[6]For capacitive loads greater than 50 pF a series resistor is required (see Internal Reference section).
[7]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ±5%, AGND = DGND = 0 V)

Parameter	Limit at T_{min}, T_{max} (All Versions)	Units	Conditions/Comments
ADC TIMING			
t_1	50	ns min	$\overline{CONVST}$ Pulse Width
t_2[3]	440	ns min	RCLK Cycle Time, Internal Clock
t_3	100	ns min	$\overline{RFS}$ to RCLK Falling Edge Setup Time
t_4	20	ns min	RCLK Rising Edge to $\overline{RFS}$
	100	ns max	
t_5[4]	155	ns max	RCLK to Valid Data Delay, C_L = 35 pF
t_6	4	ns min	Bus Relinquish Time after RCLK
	100	ns max	
t_{13}[5]	2 RCLK +200 to 3 RCLK + 200	ns typ	$\overline{CONVST}$ to $\overline{RFS}$ Delay
DAC TIMING			
t_7	50	ns min	$\overline{TFS}$ to TCLK Falling Edge
t_8	75	ns min	TCLK Falling Edge to $\overline{TFS}$
t_9[6]	150	ns min	TCLK Cycle Time
t_{10}	30	ns min	Data Valid to TCLK Setup Time
t_{11}	75	ns min	Data Valid to TCLK Hold Time
t_{12}	40	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Timing specifications are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Serial timing is measured with a 4.7 kΩ pull-up resistor on DR and $\overline{RFS}$ and a 2 kΩ pull-up resistor on RCLK. The capacitance on all three outputs is 35 pF.
[3]When using internal clock, RCLK mark/space ratio (measured form a voltage level of 1.6 V) range is 40/60 to 60/40. For external clock, RCLK mark/space ratio = external clock mark/space ratio.
[4]DR will drive higher capacitance loads but this will add to t_5 since it increases the external RC time constant (4.7 kΩ//C_L) and hence the time to reach 2.4 V.
[5]Time 2 RCLK to 3 RCLK depends on conversion start to ADC clock synchronization.
[6]TCLK mark/space ratio is 40/60 to 60/40.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	−0.3 V to +7 V
V_{SS} to AGND	+0.3 V to −7 V
AGND to DGND	−0.3 V to V_{DD}+0.3 V
V_{OUT} to AGND	V_{SS} to V_{DD}
V_{IN} to AGND	V_{SS} −0.3 V to V_{DD}+0.3 V
RO ADC to AGND	−0.3 V to V_{DD}+0.3 V
RO DAC to AGND	−0.3 V to V_{DD}+0.3 V
RI DAC to AGND	−0.3 V to V_{DD}+0.3 V
Digital Inputs to DGND	−0.3 V to V_{DD}+0.3 V
Digital Outputs to DGND	−0.3 V to V_{DD}+0.3 V

Operating Temperature Range	
J Version	0°C to +70°C
A Version	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Any Package) to +75°C	1000 mW
Derates above +75°C by	10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

Model	Temperature Range	Signal-to-Noise Ratio (SNR)	Relative Accuracy	Package Option*
AD7869JN	0°C to +70°C	78 dB	±2 LSB max	N-24
AD7869JR	0°C to +70°C	78 dB	±2 LSB max	R-28
AD7869AQ	−40°C to +85°C	77 dB	±2 LSB max	Q-24

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

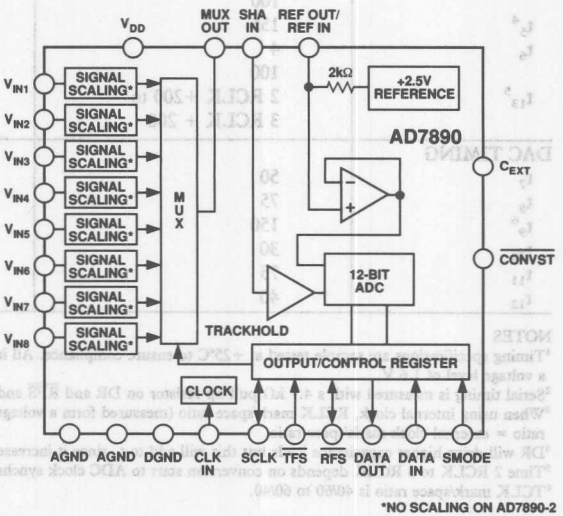
AD7890

FEATURES

Fast 12-Bit ADC with 5.9 μs Conversion Time
Eight Single-Ended Analog Input Channels
Selection of Input Ranges
- **±10 V for AD7890-10**
- **0 V to +4.096 V for AD7890-4**
- **0 V to +2.5 V for AD7890-2**

Allows Separate Access to Multiplexer and ADC
On-Chip Track/Hold Amplifier
On-Chip Reference
High Speed, Flexible, Serial Interface
Single Supply, Low Power Operation (50 mW max)
Power-Down Mode (75 μW typ)

FUNCTIONAL BLOCK DIAGRAM



*NO SCALING ON AD7890-2

GENERAL DESCRIPTION

The AD7890 is an eight-channel 12-bit data acquisition system. The part contains an input multiplexer, an on-chip track/hold amplifier, a high-speed 12-bit ADC, a +2.5 V reference and a high speed, serial interface. The part operates from a single +5 V supply and accepts an analog input range of ±10 V (AD7890-10), 0 to +4.096 V (AD7890-4) and 0 to +2.5 V (AD7890-2).

The multiplexer on the part is independently accessible. This allows the user to insert an antialiasing filter or signal conditioning, if required, between the multiplexer and the ADC. This means that one antialiasing filter can be used for all eight channels. Connection of an external capacitor allows the user to adjust the time given to the multiplexer settling to include any external delays in the filter or signal conditioning circuitry.

Output data from the AD7890 is provided via a high speed bidirectional serial interface port. The part contains an on-chip control register, allowing control of channel selection, conversion start and power-down via the serial port. Versatile, high speed logic ensures easy interfacing to serial ports on microcontrollers and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7890 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

Power dissipation in normal mode is low at 30 mW typ and the part can be placed in a standby (power-down) mode if it is not required to perform conversions. The AD7890 is fabricated in Analog Devices' Linear Compatible CMOS (LC^2MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3" wide, plastic or hermetic dual-in-line package or in a 24-pin small outline package (SOIC).

PRODUCT HIGHLIGHTS

1. Complete 12-Bit Data Acquisition System on a Chip
   The AD7890 is a complete monolithic ADC combining an eight-channel multiplexer, 12-bit ADC, +2.5 V reference and a track/hold amplifier on a single chip.
2. Separate Access to Multiplexer and ADC
   The AD7890 provides access to the output of the multiplexer allowing one antialiasing filter for eight channels—a considerable saving over the eight antialiasing filters required if the multiplexer was internally connected to the ADC.
3. High Speed Serial Interface
   The part provides a high speed serial interface for easy connection to serial ports of microcontrollers and DSP processors.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (V_{DD} = +5 V, AGND = DGND = 0 V, REF IN = +2.5 V, $f_{CLK\ IN}$ = 2.5 MHz external, MUX OUT connect to SHA IN. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	B Versions	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					Using External $\overline{CONVST}$. Any Channel
Signal to (Noise + Distortion) Ratio[2]	70	70	70	dB min	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz[3]
Total Harmonic Distortion (THD)[2]	−78	−78	−78	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz[3]
Peak Harmonic or Spurious Noise[2]	−79	−79	−79	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz[3]
Intermodulation Distortion					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 100 kHz[3]
2nd Order Terms	−80	−80	−80	dB typ	
3rd Order Terms	−80	−80	−80	dB typ	
Channel-to-Channel Isolation[2]	−80	−80	−80	dB max	f_{IN} = 1 kHz Sine Wave
DC ACCURACY					Any Channel
Resolution	12	12	12	Bits	
Minimum Resolution for Which					
No Missing Codes are Guaranteed	12	12	12	Bits	
Relative Accuracy[2]	±1	±0.5	±1	LSB max	
Differential Nonlinearity[2]	±1	±1	±1	LSB max	
Positive Full-Scale Error[2]	±2.5	±2.5	±2.5	LSB max	
Full-Scale Error Match[4]	2	2	2	LSB max	
AD7890-2, AD7890-4					
Unipolar Offset Error[2]	±2	±2	±2	LSB max	
Unipolar Offset Error Match	2	2	2	LSB max	
AD7890-10 Only					
Negative Full-Scale Error[2]	±2	±2	±2	LSB max	
Bipolar Zero Error[2]	±4	±4	±4	LSB max	
Bipolar Zero Error Match	2	2	2	LSB max	
ANALOG INPUTS					
AD7890-10					
Input Voltage Range	±10	±10	±10	Volts	
Input Resistance	20	20	20	kΩ min	
AD7890-4					
Input Voltage Range	0 to +4.096	0 to +4.096	0 to +4.096	Volts	
Input Resistance	11	11	11	kΩ min	
AD7890-2					
Input Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Input Current	50	50	200	nA max	
MUX OUT OUTPUT					
Output Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Output Resistance					
(AD7890-10, AD7890-4)	3/5	3/5	3/5	kΩ min/kΩ max	
(AD7890-2)	2	2	2	kΩ max	Assuming V_{IN} Is Driven from Low Impedance
SHA IN INPUT					
Input Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Input Current	±50	±50	±50	nA max	
REFERENCE OUTPUT/INPUT					
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Impedance	1.6	1.6	1.6	kΩ min	Resistor Connected to Internal Reference Node
Input Capacitance[5]	10	10	10	pF max	
REF OUT Output Voltage	2.5	2.5	2.5	V nom	
REF OUT Error @ +25°C	±10	±10	±10	mV max	
T_{MIN} to T_{MAX}	±20	±20	±25	mV max	
REF OUT Temperature Coefficient	25	25	25	ppm/°C typ	
REF OUT Output Impedance	2	2	2	kΩ nom	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	pF max	

5

AD7890—SPECIFICATIONS

Parameter	A Versions[1]	B Versions	S Version	Units	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
Serial Data Output Coding					
AD7890-10	2s Complement				
AD7890-4	Straight (Natural) Binary				
AD7890-2	Straight (Natural) Binary				
CONVERSION RATE					
Conversion Time	5.9	5.9	5.9	μs max	$f_{CLK\ IN}$ = 2.5 MHz, MUX OUT Connected to SHA IN
Track/Hold Acquisition Time[2, 5]	2	2	2	μs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD} (Normal Mode)	10	10	10	mA max	Logic Inputs = 0 V or V_{DD}
I_{DD} (Standby Mode)[6] @ +25°C	15	15	15	μA typ	Logic Inputs = 0 V or V_{DD}
Power Dissipation					
Normal Mode	50	50	50	mW max	Typically 30 mW
Standby Mode @ +25°C	75	75	75	μW typ	

NOTES
[1]Temperature ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.
[2]See Terminology.
[3]This sample rate is only achievable when using the part in external clocking mode.
[4]Full-scale error match applies to positive full scale for the AD7890-2 and AD7890-4. It applies to both positive and negative full scale for the AD7890-10.
[5]Sample tested @ +25°C to ensure compliance.
[6]Analog inputs on AD7890-10 must be at 0 V to achieve correct power-down current.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{DD} to DGND . . . . . −0.3 V to +7 V
Analog Input Voltage to AGND
AD7890-10, AD7890-4 . . . . . ±17 V
AD7890-2 . . . . . −5 V, +10 V
Reference Input Voltage to AGND . . −0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . −0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Commercial (A, B Versions) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +150°C
Plastic DIP Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 105°C/W
Lead Temperature (Soldering, 10 sec) . . . . . +260°C
Cerdip Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 70°C/W
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
SOIC Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)	Package Option*
AD7890AN-2	−40°C to +85°C	±1 LSB	N-24
AD7890BN-2	−40°C to +85°C	±1/2 LSB	N-24
AD7890AR-2	−40°C to +85°C	±1 LSB	R-24
AD7890BR-2	−40°C to +85°C	±1/2 LSB	R-24
AD7890SQ-2	−55°C to +125°C	±1 LSB	Q-24
AD7890AN-4	−40°C to +85°C	±1 LSB	N-24
AD7890BN-4	−40°C to +85°C	±1/2 LSB	N-24
AD7890AR-4	−40°C to +85°C	±1 LSB	R-24
AD7890BR-4	−40°C to +85°C	±1/2 LSB	R-24
AD7890SQ-4	−55°C to +125°C	±1 LSB	Q-24
AD7890AN-10	−40°C to +85°C	±1 LSB	N-24
AD7890BN-10	−40°C to +85°C	±1/2 LSB	N-24
AD7890AR-10	−40°C to +85°C	±1 LSB	R-24
AD7890BR-10	−40°C to +85°C	±1/2 LSB	R-24
AD7890SQ-10	−55°C to +125°C	±1 LSB	Q-24

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7890 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, AGND = DGND = 0 V, REF IN = +2.5 V, $f_{CLK\ IN}$ = 2.5 MHz external, MUX OUT connected to SHA IN.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, B, S Versions)	Units	Conditions/Comments
f_{CLKIN}[3]	100	kHz min	Master Clock Frequency. For Specified Performance
	2.5	MHz max	
$t_{CLK\ IN\ LO}$	0.3 × $t_{CLK\ IN}$	ns min	Master Clock Input Low Time
$t_{CLK\ IN\ HI}$	0.3 × $t_{CLK\ IN}$	ns min	Master Clock Input High Time
tr[4]	25	ns max	Digital Output Rise Time. Typically 10 ns
tf[4]	25	ns max	Digital Output Fall Time. Typically 10 ns
$t_{CONVERT}$	5.9	µs max	Conversion Time
t_{CST}	100	ns min	$\overline{CONVST}$ Pulse Width
Self-Clocking Mode			
t_1	$t_{CLK\ IN\ HI}$ +50	ns max	$\overline{RFS}$ Low to SCLK Falling Edge
t_2[5]	25	ns max	$\overline{RFS}$ Low to Data Valid Delay
t_3	$t_{CLK\ IN\ HI}$	ns nom	SCLK High Pulse Width
t_4	$t_{CLK\ IN\ LO}$	ns nom	SCLK Low Pulse Width
t_5[5]	20	ns max	SCLK Rising Edge to Data Valid Delay
t_6	40	ns max	SCLK Rising Edge to $\overline{RFS}$ Delay
t_7[6]	50	ns max	Bus Relinquish Time after Rising Edge of SCLK
t_8	0	ns min	$\overline{TFS}$ Low to SCLK Falling Edge
	$t_{CLK\ IN}$ + 50	ns max	
t_9	0	ns min	Data Valid to $\overline{TFS}$ Falling Edge Setup Time (A2 Address Bit)
t_{10}	20	ns min	Data Valid to SCLK Falling Edge Setup Time
t_{11}	10	ns min	Data Valid to SCLK Falling Edge Hold Time
t_{12}	20	ns min	$\overline{TFS}$ to SCLK Falling Edge Hold Time
External-Clocking Mode			
t_{13}	20	ns min	$\overline{RFS}$ Low to SCLK Falling Edge Setup Time
t_{14}[5]	40	ns max	$\overline{RFS}$ Low to Data Valid Delay
t_{15}	50	ns min	SCLK High Pulse Width
t_{16}	50	ns min	SCLK Low Pulse Width
t_{17}[5]	35	ns max	SCLK Rising Edge to Data Valid Delay
t_{18}	20	ns min	$\overline{RFS}$ to SCLK Falling Edge Hold Time
t_{19}[6]	50	ns max	Bus Relinquish Time after Rising Edge of $\overline{RFS}$
t_{19A}[6]	90	ns max	Bus Relinquish Time after Rising Edge of SCLK
t_{20}	20	ns min	$\overline{TFS}$ Low to SCLK Falling Edge Setup Time
t_{21}	10	ns min	Data Valid to SCLK Falling Edge Setup Time
t_{22}	15	ns min	Data Valid to SCLK Falling Edge Hold Time
t_{23}	40	ns min	$\overline{TFS}$ to SCLK Falling Edge Hold Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 8 to 11.

[3]The AD7890 is production tested with f_{CLKIN} at 2.5 MHz. It is guaranteed by characterization to operate at 100 kHz.

[4]Specified using 10% and 90% points on waveform of interest.

[5]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

[6]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

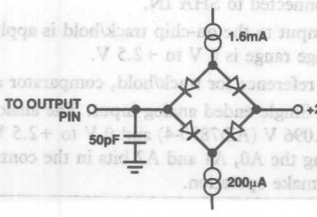


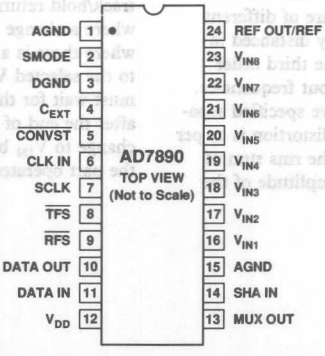
Figure 1. Load Circuit for Access Time and Bus Relinquish Time

Pin	Mnemonic	Description
1	AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
2	SMODE	Control Input. Determines whether the part operates in its External Clocking (slave) or Self-Clocking (master) serial mode. With SMODE at a logic low, the part is in its Self-Clocking serial mode with $\overline{RFS}$ and SCLK as outputs. This Self-Clocking mode is useful for connection to shift registers or to serial ports of DSP processors. With SMODE at a logic high, the part is in its External Clocking serial mode with SCLK and $\overline{RFS}$ as inputs. This External Clocking mode is useful for connection to the serial port of microcontrollers such as the 8XC51 and the 68HCXX and for connection to the serial ports of DSP processors.
3	DGND	Digital Ground. Ground reference for digital circuitry.
4	C_{EXT}	External Capacitor. An external capacitor is connected to this pin to determine the length of the internal pulse (see $\overline{CONVST}$ input and Control Register section). Larger capacitances on this pin extend the pulse to allow for settling time delays through an external antialiasing filter or signal conditioning circuitry.
5	$\overline{CONVST}$	Convert Start. Edge-triggered logic input. A low to high transition on this input puts the track/hold into hold and initiates conversion provided that the internal pulse has timed out (see Control Register section). If the internal pulse is active when the $\overline{CONVST}$ goes high, the track/hold will not go into hold until the pulse times out. If the internal pulse has timed out when $\overline{CONVST}$ goes high, the rising edge of $\overline{CONVST}$ drives the track/hold into hold and initiates conversion.
6	CLK IN	Clock Input. An external TTL-compatible clock is applied to this input pin to provide the clock source for the conversion sequence. In the Self-Clocking serial mode, the SCLK output is derived from this CLK IN pin.
7	SCLK	Serial Clock Input. In the External Clocking (slave) mode (see Serial Interface section) this is an externally applied serial clock which is used to load serial data to the control register and to access data from the output register. In the Self-Clocking (master) mode, the internal serial clock, which is derived from the clock input (CLK IN), appears on this pin. Once again, it is used to load serial data to the control register and to access data from the output register.
8	$\overline{TFS}$	Transmit Frame Synchronization Pulse. Active low logic input with serial data expected after the falling edge of this signal.
9	$\overline{RFS}$	Receive Frame Synchronization Pulse. In the External Clocking mode, this pin is an active low logic input with $\overline{RFS}$ provided externally as a strobe or framing pulse to access serial data from the output register. In the Self-Clocking mode, it is an active low output which is internally generated and provides a strobe or framing pulse for serial data from the output register. For applications which require that data be transmitted and received at the same time, $\overline{RFS}$ and $\overline{TFS}$ should be connected together.
10	DATA OUT	Serial Data Output. Sixteen bits of serial data are provided with one leading zero, preceding the three address bits of the Control register and the 12 bits of conversion data. Serial data is valid on the falling edge of SCLK for sixteen edges after $\overline{RFS}$ goes low. Output coding from the ADC is 2s complement for the AD7890-10 and straight binary for the AD7890-4 and AD7890-2.
11	DATA IN	Serial Data Input. Serial data to be loaded to the control register is provided at this input. The first five bits of serial data are loaded to the control register on the first five falling edges of SCLK after $\overline{TFS}$ goes low. Serial data on subsequent SCLK edges is ignored while $\overline{TFS}$ remains low.
12	V_{DD}	Positive supply voltage, +5 V ± 5%.
13	MUX OUT	Multiplexer Output. The output of the multiplexer appears at this pin. The output voltage range from this output is 0 V to +2.5 V for the nominal analog input range to the selected channel. The output impedance of this output is nominally 3.5 kΩ. If no external antialiasing filter is required, MUX OUT should be connected to SHA IN.
14	SHA IN	Track/Hold Input. The input to the on-chip track/hold is applied to this pin. It is a high impedance input and the input voltage range is 0 V to +2.5 V.
15	AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
16	V_{IN1}	Analog Input Channel 1. Single-ended analog input. The analog input range on is ±10 V (AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.

Pin	Mnemonic	Description
17	V_{IN2}	Analog Input Channel 2. Single-ended analog input. The analog input range on is ±10 V (AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
18	V_{IN3}	Analog Input Channel 3. Single-ended analog input. The analog input range on is ±10 V(AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
19	V_{IN4}	Analog Input Channel 4. Single-ended analog input. The analog input range on is ±10 V(AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
20	V_{IN5}	Analog Input Channel 5. Single-ended analog input. The analog input range on is ±10 V(AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
21	V_{IN6}	Analog Input Channel 6. Single-ended analog input. The analog input range on is ±10 V(AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
22	V_{IN7}	Analog Input Channel 7. Single-ended analog input. The analog input range on is ±10 V(AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
23	V_{IN8}	Analog Input Channel 8. Single-ended analog input. The analog input range on is ±10 V(AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
24	REF OUT/REF IN	Voltage Reference Output/Input. The part can be used with either its own internal reference or with an external reference source. The on-chip +2.5 V reference voltage is provided at this pin. When using this internal reference as the reference source for the part, REF OUT should decoupled to AGND with a 0.1 μF disc ceramic capacitor. The output impedance of this reference source is typically 2 kΩ. When using an external reference source as the reference voltage for the part, the reference source should be connected to this pin. This overdrives the internal reference and provides the reference source for the part. The REF IN input is buffered on-chip. The nominal reference voltage for correct operation of the AD7890 is +2.5 V.

PIN CONFIGURATION

DIP and SOIC



TERMINOLOGY

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7890, it is defined as:

$$THD\ (dB) = 20\ log\ \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

The AD7890 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Channel-to-Channel Isolation

Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 1 kHz signal to any one of the other seven inputs and determining how much that signal is attenuated in the channel of interest. The figure given is the worst case across all eight channels.

Relative Accuracy

Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Positive Full-Scale Error (AD7890-10)

This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal (4 × REF IN − 1 LSB) after the Bipolar Zero Error has been adjusted out.

Positive Full-Scale Error (AD7890-4)

This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111) from the ideal (1.638 × REF IN − 1 LSB) after the Unipolar Offset Error has been adjusted out.

Positive Full-Scale Error (AD7890-2)

This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111) from the ideal (REF IN − 1 LSB) after the Unipolar Offset Error has been adjusted out.

Bipolar Zero Error (AD7890-10)

This is the deviation of the midscale transition (all 0s to all 1s) from the ideal 0 V (AGND).

Unipolar Offset Error (AD7890-2, AD7890-4)

This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal 0 V (AGND).

Negative Full-Scale Error (AD7890-10)

This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal (−4 × REF IN + 1 LSB) after Bipolar Zero Error has been adjusted out.

Track/Hold Acquisition Time

Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where a change in the selected input channel takes place or where there is a step input change on the input voltage applied to the selected V_{IN} input of the AD7890. It means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a channel change/step input change to V_{IN} before starting another conversion, to ensure that the part operates to specification.

CONTROL REGISTER

The Control Register for the AD7890 contains 5 bits of information as described below. Six serial clock pulses must be provided to the part in order to write data to the Control Register (seven if the write is required to put the part in Standby Mode). If $\overline{TFS}$ returns high before six serial clock cycles then no data transfer takes place to the Control Register and the write cycle will have to be restarted to write the data to the Control Register. If, however, the CONV bit of the register (see below) is set to a Logic 1, then a conversion will be initiated whenever a Control Register write takes place regardless of how many serial clock cycles the $\overline{TFS}$ remains low for. The default (power-on) condition of all bits in the Control Register is 0.

MSB

A2	A1	A0	CONV	STBY

A2	Address Input. This input is the most significant address input for multiplexer channel selection.
A1	Address Input. This is the 2nd most significant address input for multiplexer channel selection.
A0	Address Input. Least significant address input for multiplexer channel selection. When the address is written to the control register, an internal pulse is initiated, the pulse width of which is determined by the value of capacitance on the C_{EXT} pin. When this pulse is active, it ensures the conversion process cannot be activated. This allows for the multiplexer settling time and track/hold acquisition time before the track/hold goes into hold and conversion is initiated. In applications where there is an antialiasing filter between MUX OUT and SHA IN, the filter settling time can be taken into account before the input at SHA IN is sampled. When the internal pulse times out, the track/hold goes into hold and conversion is initiated.
CONV	Conversion Start. Writing a 1 to this bit initiates a conversion in a similar manner to the $\overline{CONVST}$ input. Continuous conversion starts do not take place when there is a 1 in this location. The internal pulse and the conversion process are initiated after the sixth serial clock cycle of the write operation if a 1 is written to this bit. With a 1 in this bit, the hardware conversion start i.e., the $\overline{CONVST}$ input, is disabled. Writing a 0 to this bit enables the hardware $\overline{CONVST}$ input.
STBY	Standby Mode Input. Writing a 1 to this bit places the device in its standby or power-down mode. Writing a 0 to this bit places the device in its normal operating mode. The part does not enter its standby mode until the seventh falling edge of SCLK in a write operation. Therefore, the part requires seven serial clock pulses in its serial write operation if it is required to put the part into standby

CONVERTER DETAILS

The AD7890 is an eight-channel, 12-bit, single supply, serial data acquisition system. It provides the user with signal scaling, multiplexer, track/hold, reference, A/D converter and versatile serial logic functions on a single chip. The signal scaling allows the part to handle ±10 V input signals (AD7890-10) and 0 V to +4.096 V input signals (AD7890-4) while operating from a single +5 V supply. The AD7890-2 contains no signal scaling and accepts an analog input range of 0 V to +2.5 V. The part operates from a +2.5 V reference which can be provided from the part's own internal reference or from an external reference source.

Unlike other single chip data acquisition solutions, the AD7890 provides the user with separate access to the multiplexer and the A/D converter. This means that the flexibility of separate multiplexer and ADC solutions is not sacrificed with the one-chip solution. With access to the multiplexer output, the user can implement external signal conditioning between the multiplexer and the track/hold. It means that one antialiasing filter can be used on the output of the multiplexer to provide the antialiasing function for all eight channels.

Conversion is initiated on the AD7890 either by pulsing the $\overline{CONVST}$ input or by writing a Logic 1 to the CONV bit of the Control Register. When using the hardware $\overline{CONVST}$ input, on the rising edge of the $\overline{CONVST}$ signal, the on-chip track/hold goes from track to hold mode and the conversion sequence is started provided the internal pulse has timed out. This internal pulse (which appears at the C_{EXT} pin) is initiated whenever the multiplexer address is loaded to the AD7890 Control Register. This pulse goes from high to low when a serial write to the part is initiated. It starts to discharge on the sixth falling clock edge of SCLK in a serial write operation to the part. The track/hold cannot go into hold and conversion cannot be initiated until the C_{EXT} pin has crossed its trigger point of 2.5 V. The discharge time of the voltage on C_{EXT} depends upon the value of capacitor connected to the C_{EXT} pin (see C_{EXT} Functioning section). The fact that the pulse is initiated every time a write to the control register takes place means that the software conversion start and track/hold signal is always delayed by the internal pulse.

The conversion clock for the part is generated from the clock signal applied to the CLK IN pin of the part. Conversion time for the AD7890 is 5.9 μs from the rising edge of the hardware $\overline{CONVST}$ signal and the track/hold acquisition time is 2 μs. To obtain optimum performance from the part, the data read operation or Control Register write operation should not occur during the conversion or during 500 ns prior to the next conversion. This allows the part to operate at throughput rates up to 117 kHz in the external clocking mode and achieve data sheet specifications. The part can operate at slightly higher throughput rates (up to 127 kHz), again in external clocking mode with degraded performance (see Timing and Control section). The throughput rate for self clocking mode is limited by the serial clock rate to 78 kHz.

All unused inputs should be connected to a voltage within the nominal analog input range to avoid noise pickup. On the AD7890-10, if any one of the input channels which are not being converted goes more negative than −12 V, it can interfere with the conversion on the selected channel.

CIRCUIT DESCRIPTION

Analog Input Section

The AD7890 is offered as three part types, the AD7890-10 which handles a ±10 V input voltage range, the AD7890-4 which handles a 0 to +4.096 V input range and the AD7890-2 which handles a 0 to +2.5 V input voltage range.

AD7890-10

Figure 2 shows the analog input section for the AD7890-10. The analog input range for each of the analog inputs is ±10 V into an input resistance of typically 33 kΩ. This input is benign with no dynamic charging currents with the resistor attenuator stage followed by the multiplexer and in cases where MUX OUT is connected to SHA IN this is followed by the high input impedance stage of the track/hold amplifier. The designed code transitions occur on successive integer LSB values (i.e., 1 LSB, 2 LSBs, 3 LSBs . . .). Output coding is 2s complement binary with 1 LSB = FS/4096 = 20 V/4096 = 4.88 mV. The ideal input/output transfer function is shown in Table I.

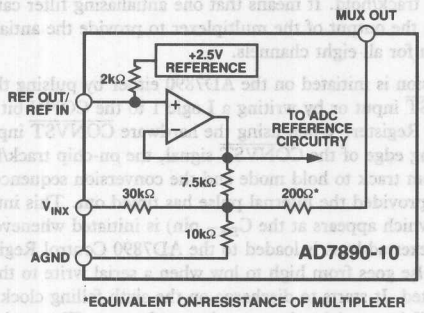


Figure 2. AD7890-10 Analog Input Structure

Table I. Ideal Input/Output Code Table for the AD7890-10

Analog Input[1]	Digital Output Code Transition
+FSR/2 − 1 LSB[2] (9.995117 V)	011 . . . 110 to 011 . . . 111
+FSR/2 − 2 LSBs (9.990234 V)	011 . . . 101 to 011 . . . 110
+FSR/2 − 3 LSBs (9.985352 V)	011 . . . 100 to 011 . . . 101
AGND + 1 LSB (0.004883 V)	000 . . . 000 to 000 . . . 001
AGND (0.000000 V)	111 . . . 111 to 000 . . . 000
AGND − 1 LSB (−0.004883 V)	111 . . . 110 to 111 . . . 111
−FSR/2 + 3 LSBs (−9.985352 V)	100 . . . 010 to 100 . . . 011
−FSR/2 + 2 LSBs (−9.990234 V)	100 . . . 001 to 100 . . . 010
−FSR/2 + 1 LSB (−9.995117 V)	100 . . . 000 to 100 . . . 001

NOTES
[1]FSR is full-scale range and is 20 V with REF IN = +2.5 V.
[2]1 LSB = FSR/4096 = 4.883 mV with REF IN = +2.5 V.

AD7890-4

Figure 3 shows the analog input section for the AD7890-4. The analog input range for each of the analog inputs is ±10 V into an input resistance of typically 15 kΩ. This input is benign with no dynamic charging currents with the resistor attenuator stage followed by the multiplexer and in cases where MUX OUT is connected to SHA IN this is followed by the high input impedance stage of the track/hold amplifier. The designed code transitions occur on successive integer LSB values (i.e., 1 LSB, 2 LSBs, 3 LSBs . . .). Output coding is straight (natural) binary with 1 LSB = FS/4096 = 4.096 V/4096 = 1 mV. The ideal input/output transfer function is shown in Table II.

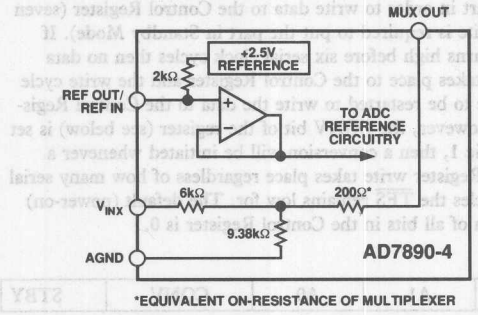


Figure 3. AD7890-4 Analog Input Structure

Table II. Ideal Input/Output Code Table for the AD7890-4

Analog Input[1]	Digital Output Code Transition
+FSR − 1 LSB[2] (4.095 V)	111 . . . 110 to 111 . . . 111
+FSR − 2 LSBs (4.094 V)	111 . . . 101 to 111 . . . 110
+FSR − 3 LSBs (4.093 V)	111 . . . 100 to 111 . . . 101
AGND + 3 LSBs (0.003 V)	000 . . . 010 to 000 . . . 011
AGND + 2 LSBs (0.002 V)	000 . . . 001 to 000 . . . 010
AGND + 1 LSB (0.001 V)	000 . . . 000 to 000 . . . 001

NOTES
[1]FSR is full-scale range and is 4.096 V with REF IN = +2.5 V.
[2]1 LSB = FSR/4096 = 1 mV with REF IN = +2.5 V.

AD7890-2

The analog input section for the AD7890-2 contains no biasing resistors and the selected analog input connects to the multiplexer and in cases where MUX OUT is connected to SHA IN this is followed by the high input impedance stage of the track/hold amplifier. The analog input range is, therefore, 0 V to +2.5 V into a high impedance stage with an input current of less than 50 nA. The designed code transitions occur on successive integer LSB values (i.e., 1 LSB, 2 LSBs, 3 LSBs . . . FS-1 LSBs). Output coding is straight (natural) binary with 1 LSB = FS/4096 = 2.5 V/4096 = 0.61 mV. The ideal input/output transfer function is shown in Table III.

Table III. Ideal Input/Output Code Table for the AD7890-2

Analog Input[1]	Digital Output Code Transition
+FSR − 1 LSB[2] (2.499390 V)	111 . . . 110 to 111 . . . 111
+FSR − 2 LSBs (2.498779 V)	111 . . . 101 to 111 . . . 110
+FSR − 3 LSBs (2.498169 V)	111 . . . 100 to 111 . . . 101
AGND + 3 LSBs (0.001831 V)	000 . . . 010 to 010 . . . 011
AGND + 2 LSBs (0.001221 V)	000 . . . 001 to 001 . . . 010
AGND + 1 LSB (0.000610 V)	000 . . . 000 to 000 . . . 001

NOTES
[1]FSR is full-scale range and is 2.5 V with REF IN = +2.5 V.
[2]1 LSB = FSR/4096 = 0.61 mV with REF IN = +2.5 V.

Track/Hold Section

The SHA IN input on the AD7890 connects directly to the input stage of the track/hold amplifier. This is a high impedance input with input leakage currents of less than 50 nA. Connecting the MUX OUT pin directly to the SHA IN pin connects the multiplexer output directly to the track/hold amplifier. The input voltage range for this input is 0 to +2.5 V. If external circuitry is connected between MUX OUT and SHA IN, then the user must ensure that the input voltage range to the SHA IN input is 0 to +2.5 V to ensure that the full dynamic range of the converter is utilized.

The track/hold amplifier on the AD7890 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the track/hold is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate of 117 kHz (i.e., the track/hold can handle input frequencies in excess of 58 kHz).

The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 2 μs. The operation of the track/hold is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion. The start of conversion is the rising edge of $\overline{\text{CONVST}}$ (assuming the internal pulse has timed out) for hardware conversion starts and for software conversion starts is the point where the internal pulse is timed out. The aperture time for the track/hold (i.e., the delay time between the external $\overline{\text{CONVST}}$ signal and the track/hold actually going into hold) is typically 15 ns. For software conversion starts, the time depends on the internal pulse widths. Therefore, for software conversion starts, the sampling instant is not very well defined. For sampling systems which require well defined, equidistant sampling, it may not be possible to achieve optimum performance from the part using the software conversion start. At the end of conversion, the part returns to its tracking mode. The acquisition time of the track/hold amplifier begins at this point.

Reference Section

The AD7890 contains a single reference pin, labelled REF OUT/REF IN, which either provides access to the part's own +2.5 V reference or to which an external +2.5 V reference can be connected to provide the reference source for the part. The part is specified with a +2.5 V reference voltage. Errors in the reference source will result in gain errors in the AD7890's transfer function and will add to the specified full-scale errors on the part. On the AD7893-10, it will also result in an offset error injected in the attenuator stage.

The AD7890 contains an on-chip +2.5 V reference. To use this reference as the reference source for the AD7890, simply connect a 0.1 μF disc ceramic capacitor from the REF OUT/REF IN pin to AGND. The voltage which appears at this pin is internally buffered before being applied to the ADC. If this reference is required for use external to the AD7890, it should be buffered as the source impedance of this output is 2 kΩ nominal. The tolerance on the internal reference is ±10 mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error over temperature of ±25 mV.

If the application requires a reference with a tighter tolerance or the AD7890 needs to be used with a system reference, then the user has the option of connecting an external reference to this REF OUT/REF IN pin. The external reference will effectively overdrive the internal reference and thus provide the reference source for the ADC. The reference input is buffered but has a nominal 2 kΩ resistor connected to the AD7890's internal reference. Suitable reference sources for the AD7890 include the AD680, AD780 and REF-43 precision +2.5 V references.

Timing and Control Section

The AD7890 is capable of two interface modes, selected by the SMODE input. The first of these is a self-clocking mode where the part provides the frame sync, serial clock and serial data at the end of conversion. In this mode the serial clock rate is determined by the master clock rate of the part (at CLK IN input). The second mode is an external clocking mode where the user provides the frame sync and serial clock signals to obtain the serial data from the part. In this second mode, the user has control of the serial clock rate up to a maximum of 10 MHz. The two modes are discussed in more detail in the Serial Interface section.

The part also provides hardware and software conversion start features. The former provides a well-defined sampling instant with the track/hold going into hold on the rising edge of the $\overline{\text{CONVST}}$ signal. For the software conversion start, a write to the CONV bit to the Control Register initiates the conversion sequence. However, for the software conversion start an internal pulse has to time out before the input signal is sampled. This pulse, plus the difficult in maintaining exactly equal delays between each software conversion start command, means that the dynamic performance of the AD7890 may have difficulty meeting spec when used in software conversion start mode.

The AD7890 provides separate channel select and conversion start control. This allows the user to optimize the throughput rate of the system. Once the track/hold has gone into hold mode, the input channel can be updated and the input voltage can settle to the new value while the present conversion is in progress.

Assuming the internal pulse has timed out before the $\overline{\text{CONVST}}$ pulse is exercised, the conversion will consist of 14.5 master clock cycles. In the self-clocking mode, the conversion time is defined as the time from the rising edge of $\overline{\text{CONVST}}$ to the falling edge of $\overline{\text{RFS}}$ (i.e., when the device starts to transmit its conversion result). This time includes the 14.5 master clock cycles plus the updating of the output register and delay time in outputting the $\overline{\text{RFS}}$ signal, resulting in a total conversion time of 5.9 μs maximum. Figure 4 shows the conversion timing for the AD7890 when used in the Self-Clocking (Master) Mode with hardware $\overline{\text{CONVST}}$. The timing diagram assumes that the internal pulse is not active when the $\overline{\text{CONVST}}$ signal goes high. To ensure this, the channel address to be converted should be selected by writing to the Control Register prior to the $\overline{\text{CONVST}}$ pulse. Sufficient setup time should be allowed between the Control Register write and the $\overline{\text{CONVST}}$ to ensure that the internal pulse has timed out. The duration of the internal pulse (and hence the duration of setup time) depends on the value of C_{EXT}.

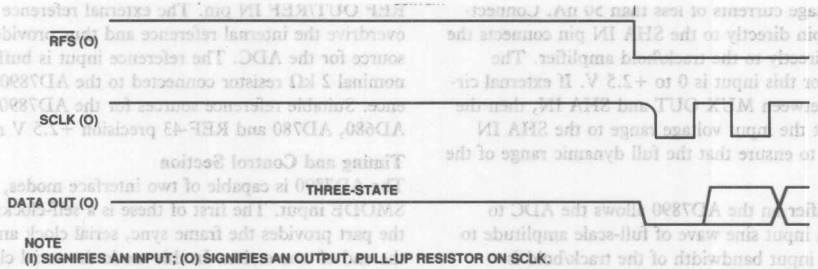


Figure 4. Self-Clocking (Master) Mode Conversion Sequence

When using the device in the External-Clocking Mode, the output register can be read at any time and the most up-to-date conversion result will be obtained. However, reading data from the output register or writing data to the Control Register during conversion or during the 500 ns prior to the next $\overline{\text{CONVST}}$ will result in reduced performance from the part. A read operation to the output register has most effect on performance with the signal-to-noise ratio likely to degrade especially when higher serial clock rates are used while the code flicker from the part will also increase (see AD7890 Performance section).

Figure 5 shows the timing and control sequence required to obtain optimum performance from the part in the external clocking mode. In the sequence shown, conversion is initiated on the rising edge of $\overline{\text{CONVST}}$ and new data is available in the output register of the AD7890 5.9 μs later. Once the read operation has taken place, a further 500 ns should be allowed before the next rising edge of $\overline{\text{CONVST}}$ to optimize the settling of the track/hold before the next conversion is initiated. The diagram shows the read operation and the write operation taking place in parallel. On the sixth falling edge of SCLK in the write sequence the internal pulse will be initiated. Assuming MUX OUT is connected to SHA IN, 2 μs are required between this sixth falling edge of SCLK and the rising edge of $\overline{\text{CONVST}}$ to allow for the full acquisition time of the track/hold amplifier. With the serial clock rate at its maximum of 10 MHz, the achievable throughput rate for the part is 5.9 μs (conversion time) plus 0.6 μs (six serial clock pulses before internal pulse is initiated) plus 2 μs (acquisition time). This results in a minimum throughput time of 8.5 μs (equivalent to a throughput rate of 117 kHz). If the part is operated with a slower serial clock, it will impact the achievable throughput rate for optimum performance.

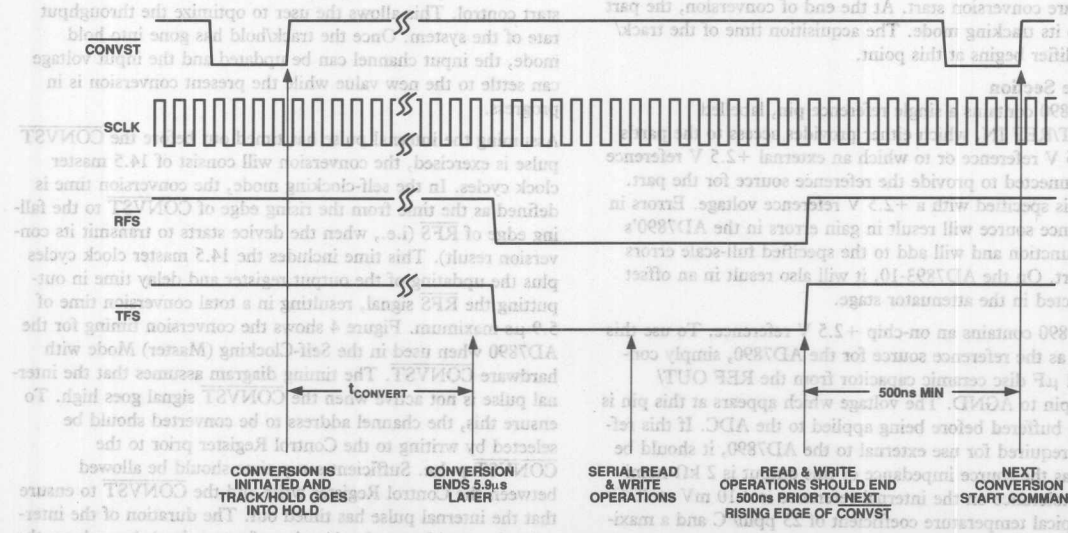


Figure 5. External Clocking (Slave) Mode Timing Sequence for Optimum Performance

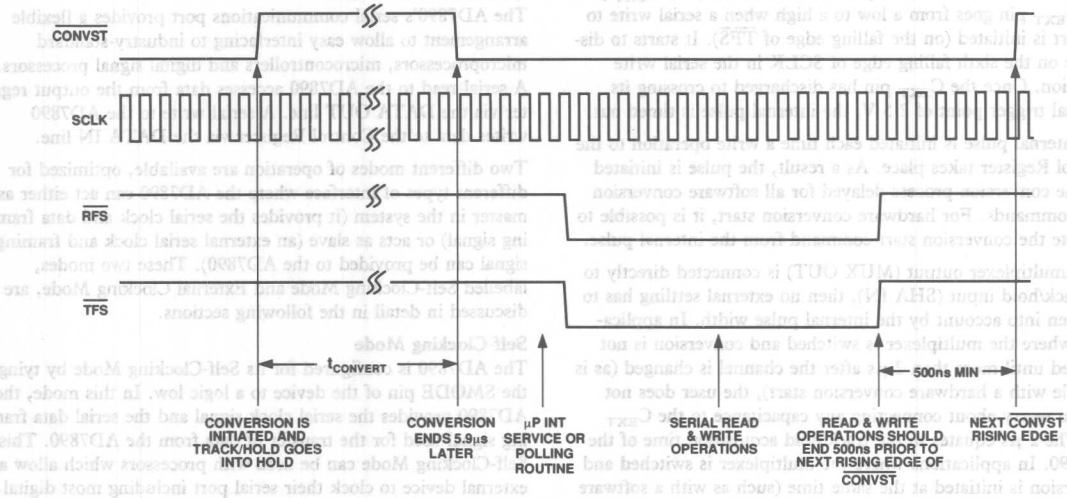


Figure 6. CONVST Used as Status Signal in External Clocking Mode

In the Self-Clocking Mode, the AD7890 indicates when conversion is complete by bringing the RFS line low and initiating a serial data transfer. In the external clocking mode, there is no indication of when conversion is complete. In many applications, this will not be a problem as the data can be read from the part during conversion or after conversion. However, applications which want to achieve optimum performance from the AD7890 will have to ensure that the data read does not occur during conversion or during 500 ns prior to the rising edge of CONVST. This can be achieved in either of two ways. The first is to ensure in software that the read operation is not initiated until 5.9 µs after the rising edge of CONVST. This will only be possible if the software knows when the CONVST command is issued. The second scheme would be to use the CONVST signal as both the conversion start signal and an interrupt signal. The simplest way to do this would be to generate a square wave signal for CONVST with high and low times of 5.9 µs (see Figure 6). Conversion is initiated on the rising edge of CONVST. The falling edge of CONVST occurs 5.9 µs later and can be used as either an active low or falling edge-triggered interrupt signal to tell the processor to read the data from the AD7890. Provided the read operation is completed 500 ns before the rising edge of CONVST, the AD7890 will operate to specification.

This scheme limits the throughput rate to 11.8 µs minimum. However, depending upon the response time of the microprocessor to the interrupt signal and the time taken by the processor to read the data, this may the fastest which the system could have operated. In any case, the CONVST signal does not have to have a 50:50 duty cycle. This can be tailored to optimize the throughput rate of the part for a given system.

Alternatively, the CONVST signal can be used as a normal narrow pulse width. The rising edge of CONVST can be used as an active high or rising edge-triggered interrupt. A software delay of 5.9 µs can then be implemented before data is read from the part.

C_{EXT} FUNCTIONING

The C_{EXT} input on the AD7890 provides a means of determining how long after a new channel address is written to the part that a conversion can take place. The reason behind this is two-fold. Firstly, when the input channel to the AD7890 is changed, the input voltage on this new channel is likely to be very different from the previous channel voltage. Therefore, the part's track/hold has to acquire the new voltage before an accurate conversion can take place. An internal pulse delays any conversion start command (as well as the signal to send the track/hold into hold) until after this pulse has timed out. The second reason is to allow the user to connect external anti-aliasing or signal conditioning circuitry between MUX OUT and SHA IN. This external circuitry will introduce extra settling time into the system. The C_{EXT} pin provides a means for the user to extend the internal pulse to take this extra settling time into account. Basically, varying the value of the capacitor on the C_{EXT} pin varies the duration of the internal pulse. Figure 7 shows the relationship between the value of the C_{EXT} capacitor and the internal delay.

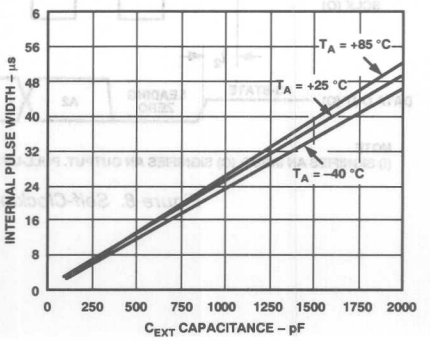


Figure 7. Internal Pulse Width vs. C_{EXT}

The duration of the internal pulse can be seen on the C_{EXT} pin. The C_{EXT} pin goes from a low to a high when a serial write to the part is initiated (on the falling edge of $\overline{TFS}$). It starts to discharge on the sixth falling edge of SCLK in the serial write operation. Once the C_{EXT} pin has discharged to crossing its nominal trigger point of 2.5 V, the internal pulse is timed out.

The internal pulse is initiated each time a write operation to the Control Register takes place. As a result, the pulse is initiated and the conversion process delayed for all software conversion start commands. For hardware conversion start, it is possible to separate the conversion start command from the internal pulse.

If the multiplexer output (MUX OUT) is connected directly to the track/hold input (SHA IN), then no external settling has to be taken into account by the internal pulse width. In applications where the multiplexer is switched and conversion is not initiated until more than 2 μs after the channel is changed (as is possible with a hardware conversion start), the user does not have to worry about connecting any capacitance to the C_{EXT} pin. The 2 μs equates to the track/hold acquisition time of the AD7890. In applications where the multiplexer is switched and conversion is initiated at the same time (such as with a software conversion start), a 120 pF capacitor should be connected to C_{EXT} to allow for the acquisition time of the track/hold before conversion is initiated.

If external circuitry is connected between MUX OUT and SHA IN, then the extra settling time introduced by this circuitry will have to be taken into account. In the case where the multiplexer change command and the conversion start command are separated, they need to be separated by greater than the acquisition time of the AD7890 plus the settling time of the external circuitry if the user does not have to worry about the C_{EXT} capacitance. In applications where the multiplexer is switched and conversion is initiated at the same time (such as with a software conversion start), the capacitor on C_{EXT} needs to allow for the acquisition time of the track/hold plus the settling-time of the external circuitry before conversion is initiated.

SERIAL INTERFACE

The AD7890's serial communications port provides a flexible arrangement to allow easy interfacing to industry-standard microprocessors, microcontrollers and digital signal processors. A serial read to the AD7890 accesses data from the output register via the DATA OUT line. A serial write to the AD7890 writes data to the Control Register via the DATA IN line.

Two different modes of operation are available, optimized for different types of interface where the AD7890 can act either as master in the system (it provides the serial clock and data framing signal) or acts as slave (an external serial clock and framing signal can be provided to the AD7890). These two modes, labelled Self-Clocking Mode and External Clocking Mode, are discussed in detail in the following sections.

Self-Clocking Mode

The AD7890 is configured for its Self-Clocking Mode by tying the SMODE pin of the device to a logic low. In this mode, the AD7890 provides the serial clock signal and the serial data framing signal used for the transfer of data from the AD7890. This Self-Clocking Mode can be used with processors which allow an external device to clock their serial port including most digital signal processors.

Read Operation

Figure 8 shows a timing diagram for reading from the AD7890 in the Self-Clocking mode. At the end of conversion, $\overline{RFS}$ goes low and the serial clock (SCLK) and serial data (DATA OUT) outputs become active. Sixteen bits of data are transmitted with one leading zero, followed by the three address bits of the Control Register, followed by the 12-bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. The $\overline{RFS}$ output remains low for the duration of the sixteen clock cycles. On the sixteenth rising edge of SCLK, the $\overline{RFS}$ output is driven high and DATA OUT is disabled.

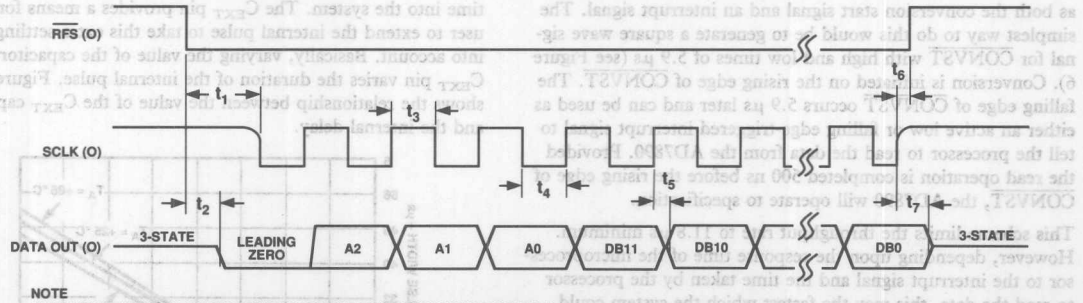


Figure 8. Self-Clocking (Master) Mode Output Register Read

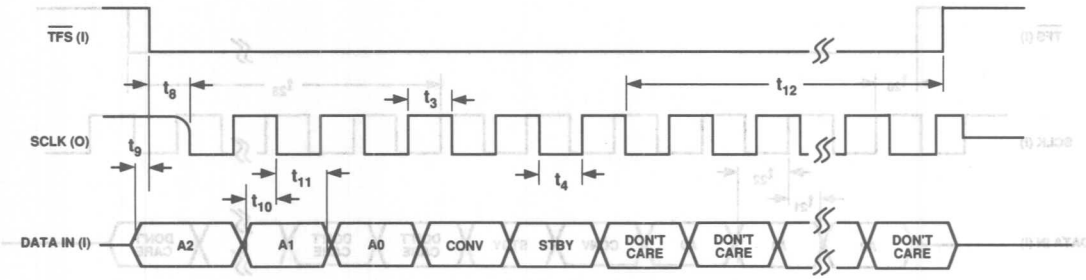


Figure 9. Self-Clocking (Master) Mode Control Register Write

5

Write Operation

Figure 9 shows a write operation to the Control Register of the AD7890. The $\overline{TFS}$ input is taken low to indicate to the part that a serial write is about to occur. $\overline{TFS}$ going low initiates the SCLK output and this is used to clock data out of the processors serial port and into the Control Register of the AD7890. The AD7890 Control Register requires only five bits of data. These are loaded on the first five clock cycles of the serial clock with data on all subsequent clock cycles being ignored. However, the part requires six serial clock cycles to load data to the Control Register. Serial data to be written to the AD7890 must be valid on the falling edge of SCLK.

External-Clocking Mode

The AD7890 is configured for its external-clocking mode by tying the SMODE pin of the device to a logic high. In this mode, SCLK and $\overline{RFS}$ of the AD7890 are configured as inputs. This external-clocking mode is designed for direct interface to systems which provide a serial clock output which is synchronized to the serial data output including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

Read Operation

Figure 10 shows the timing diagram for reading from the AD7890 in the external-clocking mode. $\overline{RFS}$ goes low to access data from the AD7890. The serial clock input does not have to be continuous. The serial data can be accessed in a number of bytes. However, $\overline{RFS}$ must remain low for the duration of the data transfer operation. Once again, sixteen bits of data are transmitted with one leading zero, followed by the three address bits in the Control Register, followed by the 12-bit conversion result starting with the MSB. If $\overline{RFS}$ goes low during the high time of SCLK, the leading zero is clocked out from the falling edge of $\overline{RFS}$ (as per Figure 10). If $\overline{RFS}$ goes low during the low time of SCLK, the leading zero is clocked out on the next rising edge of SCLK. This ensures that, regardless of whether $\overline{RFS}$ goes low during a high time or low time of SCLK, the leading zero is valid on the first falling edge of SCLK after $\overline{RFS}$ goes low, provided t_{14} and t_{17} are adhered to. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. At the end of the read operation, the DATA OUT line is three-stated by a rising edge on either the SCLK or $\overline{RFS}$ inputs, whichever occurs first. If a serial read from the output register is in progress when conversion is complete, the updating of the output register is deferred until the serial data read is complete and $\overline{RFS}$ returns high.

Write Operation

Figure 11 shows a write operation to the Control Register of the AD7890. As with the Self-Clocking mode, the $\overline{TFS}$ input goes low to indicate to the part that a serial write is about to occur. As before, the AD7890 Control Register requires only five bits of data. These are loaded on the first five clock cycles of the serial clock with data on all subsequent clock cycles being ignored. However, the part requires six serial clocks to load data to the Control Register. Serial data to be written to the AD7890 must be valid on the falling edge of SCLK.

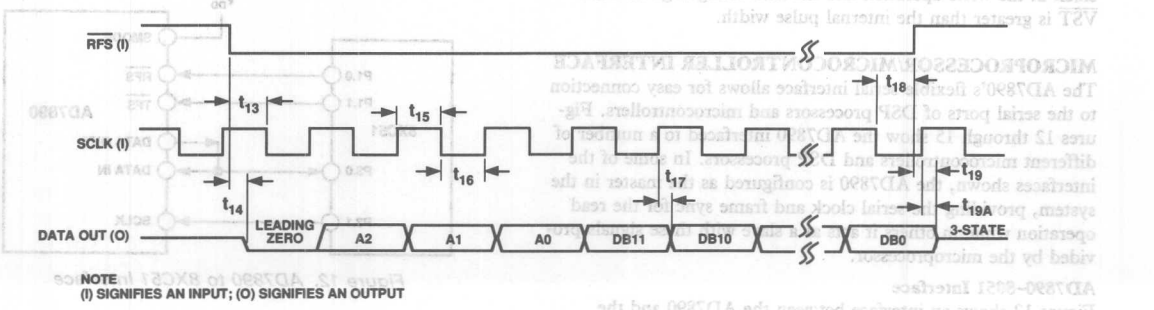


Figure 10. External Clocking (Slave) Mode Output Register Read

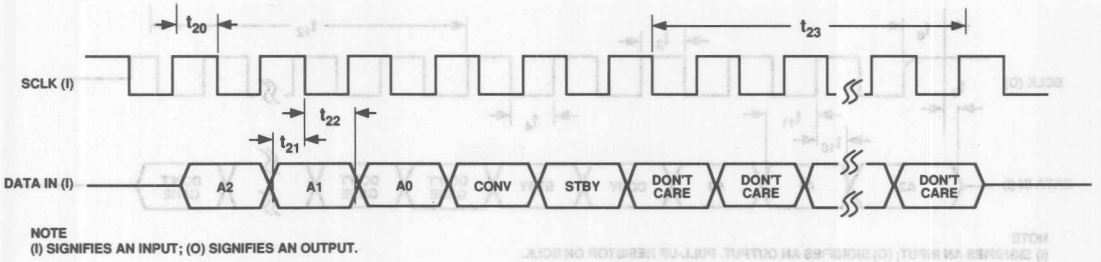


Figure 11. External Clocking (Slave) Mode Control Register Write

SIMPLIFYING THE INTERFACE

To minimize the number of interconnect lines to the AD7890, the user can connect the $\overline{RFS}$ and $\overline{TFS}$ lines of the AD7890 together and read and write from the part simultaneously. In this case, new control register data should be provided on the DATA IN line selecting the input channel and possibly providing a conversion start command while the part provides the result from the conversion just completed on the DATA OUT line.

In the self-clocking mode, this means that the part provides all the signals for the serial interface. It does require that the microprocessor has the data to be written to the Control Register available in its output register when the part brings the $\overline{TFS}$ line low. In the external clocking mode, it means that the user only has to supply a single frame synchronization signal to control both the read and write operations.

Care must be taken with this scheme that the read operation is completed before the next conversion starts if the user wants to obtain optimum performance from the part. In the case of the software conversion start, the conversion command is written to the Control Register on the sixth serial clock edge. However, the read operation continues for another 10 serial clock cycles. To avoid reading during the sampling instant or during conversion, the user should ensure that the internal pulse width is sufficiently long (by choosing C_{EXT}) so that the read operation is completed before the next conversion sequence begins. Failure to do this will result in significantly degraded performance from the part, both in terms of signal-to-noise ratio and dc parameters. In the case of a hardware conversion start, the user should ensure that the delay between the sixth falling edge of the serial clock in the write operation and the next rising edge of $\overline{CONVST}$ is greater than the internal pulse width.

MICROPROCESSOR/MICROCONTROLLER INTERFACE

The AD7890's flexible serial interface allows for easy connection to the serial ports of DSP processors and microcontrollers. Figures 12 through 15 show the AD7890 interfaced to a number of different microcontrollers and DSP processors. In some of the interfaces shown, the AD7890 is configured as the master in the system, providing the serial clock and frame sync for the read operation while in others it acts as a slave with these signals provided by the microprocessor.

AD7890–8051 Interface

Figure 12 shows an interface between the AD7890 and the 8XC51 microcontroller. The AD7890 is configured for its external clocking mode while the 8XC51 is configured for its Mode 0 serial interface mode. The diagram shown in Figure 12 makes no provisions for monitoring when conversion is complete on the AD7890 (assuming hardware conversion start is used). To monitor the conversion time on the AD7890 a scheme such as outlined previously with $\overline{CONVST}$ can be used. This can be implemented in two ways. One is to connect the $\overline{CONVST}$ line to another parallel port bit which is configured as an input. This port bit can then be polled to determine when conversion is complete. An alternative is to use an interrupt driven system in which case the $\overline{CONVST}$ line should be connected to the $\overline{INT1}$ input of the 8XC51.

Since the 8XC51 contains only one serial data line, the DATA OUT and DATA IN lines of the AD7890 must be connected together. This means that the 8XC51 cannot communicate with the output register and Control Register of the AD7890 at the same time. The 8XC51 outputs the LSB first in a write operation so care should be taken in arranging the data which is to be transmitted to the AD7890. Similarly, the AD7890 outputs the MSB first during a read operation while the 8XC51 expects the LSB first. Therefore, the data that is to be read into the serial port needs to be rearranged before the correct data word from the AD7890 is available in the microcontroller.

The serial clock rate from the 8XC51 is limited to significantly less than the allowable input serial clock frequency with which the AD7890 can operate. As a result, the time to read data from the part will actually be longer than the conversion time of the part. This means that the AD7890 cannot run at its maximum throughput rate when used with the 8XC51.

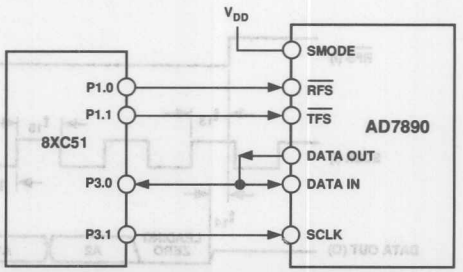


Figure 12. AD7890 to 8XC51 Interface

AD7890–68HC11 Interface

An interface circuit between the AD7890 and the 68HC11 microcontroller is shown in Figure 13. For the interface shown, the AD7890 is configured for its external clocking mode while the 68HC11's SPI port is used and the 68HC11 is configured in its single-chip mode. The 68HC11 is configured in the master mode with its CPOL bit set to a logic zero and its CPHA bit set to a logic one.

As with the previous interface, there are no provisions for monitoring when conversion is complete on the AD7890. To monitor the conversion time on the AD7890 a scheme, such as outlined in the previous interface with $\overline{\text{CONVST}}$, can be used. This can be implemented in two ways. One is to connect the $\overline{\text{CONVST}}$ line to another parallel port bit which is configured as an input. This port bit can then be polled to determine when conversion is complete. An alternative is to use an interrupt driven system in which case the $\overline{\text{CONVST}}$ line should be connected to the $\overline{\text{IRQ}}$ input of the 68HC11.

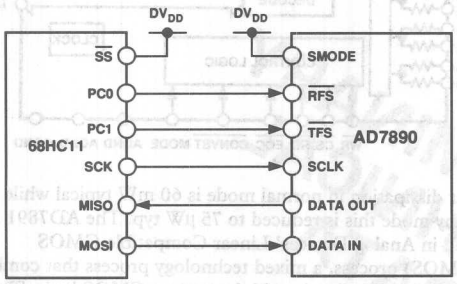


Figure 13. AD7890 to 68HC11 Interface

The serial clock rate from the 68HC11 is limited to significantly less than the allowable input serial clock frequency with which the AD7890 can operate. As a result, the time to read data from the part will actually be longer than the conversion time of the part. This means that the AD7890 cannot run at its maximum throughput rate when used with the 68HC11.

AD7890–ADSP-2101 Interface

An interface circuit between the AD7890 and the ADSP-2101 DSP processor is shown in Figure 14. The AD7890 is configured for its external clocking mode with the ADSP-2101 providing the serial clock and frame synchronization signals. The RFS1 and TFS1 inputs are outputs are configured for active low operation.

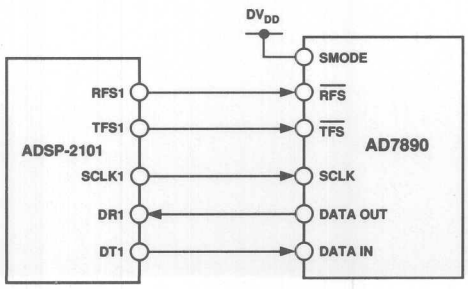


Figure 14. AD7890 to ADSP-2101 Interface

In the scheme shown, the maximum serial clock frequency which the ADSP-2101 can provide is 6.25 MHz. This allows the AD7890 to be operated at a sample rate of 111 kHz. If it is desirable to operate the AD7890 at its maximum throughput rate of 117 kHz, an external serial clock of 10 MHz can be provided to drive the serial clock input of both the AD7890 and the ADSP-2101.

To monitor the conversion time on the AD7890 a scheme, such as outlined in previous interfaces with $\overline{\text{CONVST}}$, can be used. This can be implemented by connecting the $\overline{\text{CONVST}}$ line directly to the $\overline{\text{IRQ2}}$ input of the ADSP-2101. An alternative to this, where the user does not have to worry about monitoring the conversion status, is to operate the AD7890 in its Self-Clocking Mode. In this scheme, the actual interface connections would remain the same as in Figure 14 but now the AD7890 provides the serial clock and receive frame synchronization signals. Using the AD7890 in its Self-Clocking Mode, limits the throughput rate of the system as the serial clock rate is limited to 2.5 MHz.

5

AD7890–DSP56000 Interface

Figure 15 shows an interface circuit between the AD7890 and the DSP56000 DSP processor. The AD7890 is configured for its external clocking mode. The DSP56000 is configured for normal mode, synchronous operation with continuous clock. It is also set up for a 16-bit word with SCK and SC2 as outputs. The FSL bit of the DSP56000 should be set to 0.

The $\overline{\text{RFS}}$ and $\overline{\text{TFS}}$ inputs of the AD7890 are connected together so data is transmitted to and from the AD7890 at the same time. With the DSP56000 in synchronous mode, it provides a common frame synchronization pulse for read and write operations on its SC2 output. This is inverted before being applied to the $\overline{\text{RFS}}$ and $\overline{\text{TFS}}$ inputs of the AD7890.

To monitor the conversion time on the AD7890 a scheme, such as outlined in previous interface examples with $\overline{\text{CONVST}}$, can be used. This can be implemented by connecting the $\overline{\text{CONVST}}$ line directly to the $\overline{\text{IRQA}}$ input of the DSP56000.

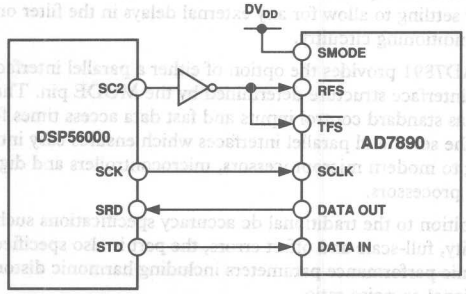


Figure 15. AD7890 to DSP56000 Interface

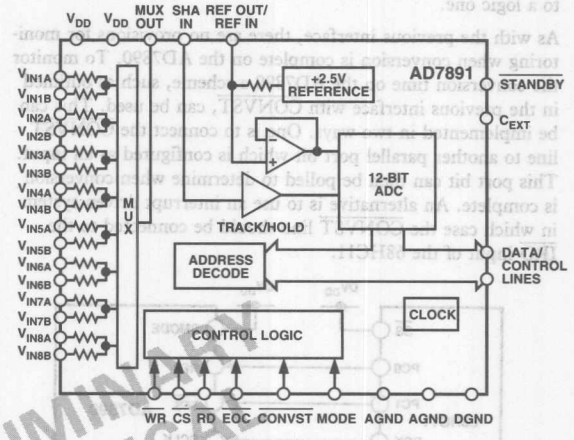
LC²MOS 8-Channel, 12-Bit High Speed Data Acquisition System

AD7891

FEATURES

Fast 12-Bit ADC with 1.6 μs Conversion Time
Eight Single-Ended Analog Input Channels
Selection of Input Ranges:
±5 V, ±10 V for AD7891-1
0 V to +2.5 V, 0 to +5 V ±2.5 V for AD7891-2
Parallel and Serial Interface
Allows Separate Access to Mux and ADC
On-Chip Track/Hold Amplifier
On-Chip Reference
Single Supply, Low Power Operation (75 mW max)
Power-Down Mode (75 μW typ)
Overvoltage Protection on Analog Inputs

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7891 is an eight-channel 12-bit data acquisition system with a choice of either parallel or serial interface structure. The part contains an input multiplexer, an on-chip track/hold amplifier, a high speed 12-bit ADC, a +2.5 V reference and a high speed interface. The part operates from a single +5 V supply and accepts a variety of analog input ranges across two models, the AD7891-1 (±5 V and ±10 V) and the AD7891-2 (0 V to +2.5 V, 0 V to +5 V and ±2.5 V).

The multiplexer on the part is independently accessible. As a result, an antialiasing filter or signal conditioning can be inserted, if required, between the multiplexer and the ADC. This allows one antialiasing filter to be used for all eight channels. The value of an external capacitor determines the time given to the multiplexer settling to allow for any external delays in the filter or signal conditioning circuitry.

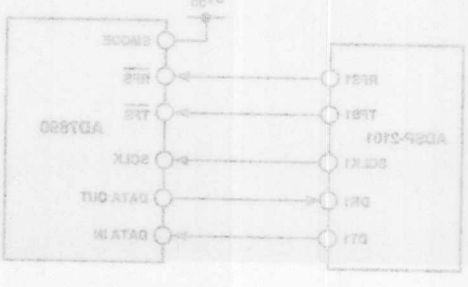
The AD7891 provides the option of either a parallel interface or serial interface structure determined by the MODE pin. The part has standard control inputs and fast data access times for both the serial and parallel interfaces which ensures easy interfacing to modern microprocessors, microcontrollers and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the part is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

Power dissipation in normal mode is 60 mW typical while in the standby mode this is reduced to 75 μW typ. The AD7891 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 44-pin plastic quad flatpack (PQFP) and a 44-lead plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. The AD7891 is a complete monolithic 12-bit data acquisition system combining an eight-channel multiplexer, 12-bit ADC, +2.5 V reference and track/hold amplifier on a single chip.
2. The part provides separate access to the multiplexer and the ADC, thus retaining all the flexibility of separate multiplexer and ADC solutions.
3. The part offers high speed parallel or serial interface options for easy connection to microprocessors, microcontrollers and digital signal processors.



PRELIMINARY TECHNICAL DATA

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SPECIFICATIONS

(V_{DD} = +5 V, AGND = DGND = 0 V, REF IN = +2.5 V, MUX OUT connected to SHA IN. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	B Versions	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					Any Channel
Signal to (Noise+Distortion) Ratio[3]					
@ 25°C	70	72	70	dB min	f_{SAMPLE} = 500 kHz[4]
T_{MIN} to T_{MAX}	70	70	70	dB min	
Total Harmonic Distortion[3]	–78	–78	–78	dB max	f_{SAMPLE} = 500 kHz[4]
Peak Harmonic or Spurious Noise[3]	–79	–79	–79	dB max	f_{SAMPLE} = 500 kHz[4]
Intermodulation Distortion[3]					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 500 kHz[4]
2nd Order Terms	–80	–80	–80	dB typ	
3rd Order Terms	–80	–80	–80	dB typ	
Channel-to-Channel Isolation[3]	–80	–80	–80	dB max	f_{IN} = 1 kHz Sine Wave
DC ACCURACY					Any Channel
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes are Guaranteed	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[3]	±1	±1	±1	LSB max	
Positive Full-Scale Error[3]	±1	±1	±1	LSB max	
Full-Scale Error Match[3]	1	1	1	LSB max	
Unipolar Offset Error	±1	±1	±1	LSB max	Input Ranges of 0 V to +2.5 V, 0 V to +5 V
Unipolar Offset Error Match	1	1	1	LSB max	Input Ranges of 0 V to +2.5 V, 0 V to +5 V
Negative Full-Scale Error[3]	±1	±1	±1	LSB max	Input Ranges of ±2.5 V, ±5 V, ±10 V
Bipolar Zero Error	±1	±1	±1	LSB max	Input Ranges of ±2.5 V, ±5 V, ±10 V
Bipolar Zero Error Match	1	1	1	LSB max	Input Ranges of ±2.5 V, ±5 V, ±10 V
ANALOG INPUTS					
AD7891-1 Input Voltage Range	±5	±5	±5	Volts	Input Applied to Both V_{INXA} and V_{INXB}
	±10	±10	±10	Volts	Input Applied to V_{INXA}, V_{INXB} = AGND
AD7891-1 V_{INXA} Input Resistance	10	10	10	kΩ min	Input Range of ±5 V
AD7891-1 V_{INXA} Input Resistance	20	20	20	kΩ min	Input Range of ±10 V
AD7891-2 Input Voltage Range					
	0 to +2.5	0 to +2.5	0 to +2.5	Volts	Input Applied to Both V_{INXA} and V_{INXB}
	0 to +5	0 to +5	0 to +5	Volts	Input Applied to V_{INXA}, V_{INXB} = AGND
	±2.5	±2.5	±2.5	Volts	Input Applied to V_{INXA}, V_{INXB} = REF IN[6]
AD7891-2 V_{INXA} Input Resistance	1	1	1	kΩ min	Input Ranges of ±2.5 V and 0 V to +5 V
AD7891-2 V_{INXA} Input Current	±50	±50	±50	nA max	Input Range of 0 V to +2.5 V
MUX OUT OUTPUT					
Output Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Output Resistance					
AD7891-1	3/7	3/7	3/7	kΩ min/kΩ max	
AD7891-2	0.5/2.5	0.5/2.5	0.5/2.5	kΩ min/kΩ max	
SHA IN INPUT					
Input Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Input Current	±50	±50	±50	nA max	
REFERENCE INPUT/OUTPUT					
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Impedance	1.6	1.6	1.6	kΩ min	Resistor Connected to Internal Reference Node
Input Capacitance[5]	10	10	10	pF max	
REF OUT Output Voltage	2.5	2.5	2.5	V nom	
REF OUT Error @ +25°C	±10	±10	±10	mV max	
T_{MIN} to T_{MAX}	±20	±20	±25	mV max	
REF OUT Temperature Coefficient	25	25	25	ppm/°C typ	
REF OUT Output Impedance	2	2	2	kΩ nom	See REF IN Input Impedance
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.0	2.0	2.0	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	10	pF max	

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7891–SPECIFICATIONS

Parameter	A Versions[1]	B Versions	S Version	Units	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	±10	±10	±10	μA max	
Floating-State Capacitance[5]	15	15	15	pF max	
Output Coding					
	Straight (Natural) Binary				Data Format Bit of Control Register = 0
	2s Complement				Data Format Bit of Control Register = 1
CONVERSION RATE					
Conversion Time	1.6	1.6	1.6	μs max	MUX OUT Connected to SHA IN
Track/Hold Acquisition Time	0.4	0.4	0.4	μs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD} (Normal Mode)	15	15	15	mA max	
I_{DD} (Standby Mode)	25	25	25	μA max	Logic Inputs = 0 V or V_{DD}
Power Dissipation (Normal Mode)	75	75	75	mW max	Typically 60 mW
Power Dissipation (Standby Mode)	125	125	125	μW max	Typically 75 μW

NOTES

[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S Version: –55°C to +125°C.

[2]AD7891-1's dynamic performance is measured with an input frequency of 10 kHz while the AD7891-2's dynamic performance is measured with an input frequency of 100 kHz.

[3]See Terminology.

[4]This sample rate can only be achieved when the part is operated in the parallel interface mode. Maximum achievable throughput rate in the serial interface mode is 385 kHz.

[5]Sample tested @ +25°C to ensure compliance.

[6]REF IN must be buffered before being applied to V_{INXB}.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND ..... –0.3 V to +7 V
V_{DD} to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND
AD7891-1 ..... ±17 V
AD7891-2 ..... ±5 V
Reference Input Voltage to AGND .... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Commercial (A, B Versions) ..... –40°C to +85°C
Extended (S Version). ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
PQFP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 95°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infared (15 sec) ..... +220°C
PLCC Package, Power Dissipation ..... 500 mW
θ_{JA} Thermal Impedance ..... 55°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infared (15 sec) ..... +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7891 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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TIMING CHARACTERISTICS[1, 2] (V_{DD}= +5 V, AGND = DGND = 0 V, REF IN = +2.5 V, MUX OUT connected to SHA IN)

Parameter	A, B Versions	S Version	Units	Test Conditions/Comments
t_r[3]	20	20	ns max	Digital Output Rise Time, Typically 10 ns
t_f[3]	50	50	ns max	Digital Output Fall Time, Typically 10 ns
t_{CONV}	2	2	µs max	Conversion Time
Parallel Interface				
t_1	0	0	ns min	$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Setup Time
t_2	35	45	ns min	Write Pulse Width
t_3	25	30	ns min	Data Valid to Write Setup Time
t_4	5	5	ns min	Data Valid to Write Hold Time
t_5	0	0	ns min	$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Setup Time
t_6	35	45	ns min	$\overline{CONVST}$ Pulse Width
t_7	100	100	ns min	$\overline{EOC}$ Pulse Width
t_8	35	45	ns min	Read Pulse Width
t_9[4]	25	35	ns min	Data Access Time After Falling Edge of $\overline{RD}$
t_{10}[5]	5	5	ns max	Bus Relinquish Time After Rising Edge of $\overline{RD}$
	30	40	ns max	
Serial Interface				
t_{11}	30	30	ns min	$\overline{RFS}$ Low to SCLK Falling Edge Setup Time
t_{12}[4]	20	25	ns max	$\overline{RFS}$ Low to Data Valid Delay
t_{13}	25	25	ns min	SCLK High Pulse Width
t_{14}	25	25	ns min	SCLK Low Pulse Width
t_{15}[4]	5	5	ns min	SCLK Rising Edge to Data Valid Hold Time
t_{16}[4]	15	20	ns max	SCLK Rising Edge to Data Valid Delay
t_{17}[5]	20	20	ns min	$\overline{RFS}$ to SCLK Falling Edge Hold Time
t_{18}[5]	0	0	ns min	Bus Relinquish Time after Rising Edge of $\overline{RFS}$
	30	30	ns max	
t_{18A}[5]	0	0	ns min	Bus Relinquish Time After Rising Edge of SCLK
	30	30	ns max	
t_{19}	20	25	ns min	$\overline{TFS}$ Low to SCLK Falling Edge Setup Time
	t_{13}	t_{13}	ns max	
t_{20}	15	20	ns min	Data Valid to SCLK Falling Edge Setup Time
t_{21}	10	10	ns min	Data Valid to SCLK Falling Edge Hold Time
t_{22}	25	30	ns min	$\overline{TFS}$ Low to SCLK Falling Edge Setup Time

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are measured with tr = tf = 1 ns (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.
[2]See Figures 2 and 3.
[3]Specified using 10% and 90% points on the waveform of interest.
[4]Measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.0 V.
[5]These times are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.
Specifications subject to change without notice.

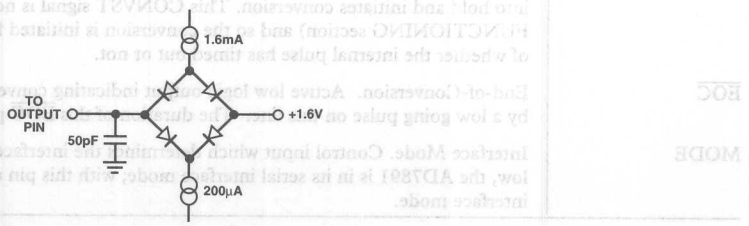

Figure 1. Load Circuit for Access Time and Bus Relinquish Time

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PIN DESCRIPTION

Mnemonic	Description
V_{INXA}, V_{INXB}	Analog Input Channels. The AD7891 contains eight pairs of analog input channels. Each channel contains two input pins to allow a number of different input ranges to be used with the AD7891. There are two possible input voltage ranges on the AD7891-1. The ±5 V input range is selected by connecting the input voltage to both V_{INXA} and V_{INXB}, while the ±10 V input range is selected by applying the input voltage to V_{INXA} and connecting V_{INXB} to AGND. The AD7891-2 has three possible input ranges. The 0 V to +2.5 V input range is selected by connecting the analog input voltage to both V_{INXA} and V_{INXB}; the 0 V to +5 V input range is selected by applying the input voltage to V_{INXA} and connecting V_{INXB} to AGND; while the ±2.5 V input range is selected by connecting the analog input voltage to V_{INXA} and connecting V_{INXB} to REF IN (provided this REF IN voltage comes from a low impedance source). The channel to be converted is selected by the A2, A1 and A0 bits of the Control Register. In the parallel interface mode, these bits are available as three data input lines (DB3 to DB5) in a parallel write operation, while in the serial interface mode, these three bits are accessed via the DATA IN line in a serial write operation. The multiplexer has guaranteed break-before-make operation.
V_{DD}	Positive supply voltage, +5 V ± 5%.
AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
DGND	Digital Ground. Ground reference for digital circuitry.
$\overline{\text{STANDBY}}$	Standby Mode Input. TTL-compatible input which is used to put the device into the power save or standby mode. The $\overline{\text{STANDBY}}$ input is high for normal operation and low for standby operation.
MUX OUT	Multiplexer Output. The output of the multiplexer appears at this pin. The output voltage range from this output is 0 V to +2.5 V for the nominal analog input range to the selected channel. The output impedance of this output is nominally 7.5 kΩ for the AD7891-1 and 1 kΩ for the AD7891-2. If no external antialiasing filter or signal conditioning is required, MUX OUT should be connected to SHA IN.
SHA IN	Track/Hold Input. The input to the on-chip track/hold is applied to this pin. It is a high impedance input and the input voltage range is 0 V to +2.5 V.
C_{EXT}	External capacitor. An external capacitor is connected to this pin to determine the length of the internal pulse (see C_{EXT} FUNCTIONING section). Larger capacitances on this pin extend the pulse to allow for settling-time delays through an external antialiasing filter.
REF OUT/REF IN	Voltage Reference Output/Input. The part can either be used with its own internal reference or with an external reference source. The on-chip +2.5 V reference voltage is provided at this pin. When using this internal reference as the reference source for the part, REF OUT should be decoupled to AGND with a 0.1 µF disc ceramic capacitor. The output impedance of the reference source is typically 2 kΩ. When using an external reference source as the reference voltage for the part, the reference source should be connected to this pin. This overdrives the internal reference and provides the reference source for the part. The reference pin is buffered on-chip but must be able to sink or source current through this 2 kΩ resistor to the output of the on-chip reference. The nominal reference voltage for correct operation of the AD7891 is +2.5 V.
$\overline{\text{CONVST}}$	Convert Start. Edge-triggered logic input. A low to high transition on this input puts the track/hold into hold and initiates conversion. This CONVST signal is not gated with the internal pulse (see C_{EXT} FUNCTIONING section) and so the conversion is initiated from the rising edge of CONVST regardless of whether the internal pulse has timed out or not.
$\overline{\text{EOC}}$	End-of-Conversion. Active low logic output indicating converter status. The end of conversion is signified by a low going pulse on this line. The duration of this $\overline{\text{EOC}}$ pulse is nominally 120 ns.
MODE	Interface Mode. Control input which determines the interface mode for the part. With this pin at a logic low, the AD7891 is in its serial interface mode; with this pin at a logic high, the device is in its parallel interface mode.

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PARALLEL INTERFACE MODE FUNCTIONS

Mnemonic	Description
$\overline{CS}$	Chip Select. Active low logic input which is used in conjunction with $\overline{RD}$ to enable the data outputs and with $\overline{WR}$ to allow input data to be written to the part.
$\overline{RD}$	Read. Active low logic input which is used in conjunction with $\overline{CS}$ low to enable the data outputs.
$\overline{WR}$	Write Input. Active low, logic input used in conjunction with $\overline{CS}$ to latch the multiplexer address. The rising edge of this input also initiates an internal pulse, the width of which is determined by the value of capacitance on the C_{EXT} pin. When this pulse is active, it gates off the software conversion start until the pulse has timed out. This allows an external antialiasing filter (the output of which is applied to SHA IN) to settle when a channel address is changed before the track/hold goes into hold and conversion is initiated. If the SWCON bit of the Control Register is set to 1, when this pulse times out, the track/hold then goes into hold and conversion is initiated. If the SWCON bit of the Control Register is set to 0, the track/hold and conversion sequence are unaffected by the $\overline{WR}$ operation.

5

Data I/O Lines

There are twelve data input/output lines on the AD7891. When the part is configured for parallel mode (MODE = 1), the output data from the part is provided at these 12 pins during a read operation. For a write operation in parallel mode, these lines provide access to the part's Control Register.

Parallel Read Operation

During a parallel read operation the 12 lines become the 12 data bit containing the conversion result from the AD7891. These data bits are labelled Data Bit 0 (LSB) to Data Bit 11 (MSB). They are three-state TTL-compatible outputs. Output data coding is 2s complement when the DATA FORMAT Bit of the Control Register is 1 and straight binary when the DATA FORMAT Bit of the Control Register is 0.

Mnemonic	Description
DB0–DB11	Data Bit 0 (LSB) to Data Bit 11 (MSB). Three state TTL-compatible outputs which are controlled by the $\overline{CS}$ and $\overline{RD}$ inputs.

PRELIMINARY TECHNICAL DATA

Parallel Write Operation

During a parallel write operation the following functions can be written to the Control Register via the 12 data input/output pins.

Mnemonic	Description
A0	Address Input. The status of this input during a parallel write operation is latched to the A0 bit of the Control Register (see Control Register section).
A1	Address Input. The status of this input during a parallel write operation is latched to the A1 bit of the Control Register (see Control Register section).
A2	Address Input. The status of this input during a parallel write operation is latched to the A2 bit of the Control Register (see Control Register section).
SWCON	Software Conversion Start. The status of this input during a parallel write operation is latched to the SWCONV bit of the Control Register (see Control Register section).
SWSTBY	Software Standby Control. The status of this input during a parallel write operation is latched to the SWSTBY bit of the Control Register (see Control Register section).
FORMAT	Data Format Selection. The status of this input during a parallel write operation is latched to the FORMAT bit of the Control Register (see Control Register section).

SERIAL INTERFACE MODE FUNCTIONS

When the part is configured for serial mode (MODE = 0), five of the twelve data input/output lines provide serial interface functions. These functions are outlined below.

Mnemonic	Description
SCLK	Serial Clock Input. This is an externally applied serial clock which is used to load serial data to the Control Register and to access data from the output register.
$\overline{TFS}$	Transmit Frame Synchronization Pulse. Active low logic input with serial data expected after the falling edge of this signal.

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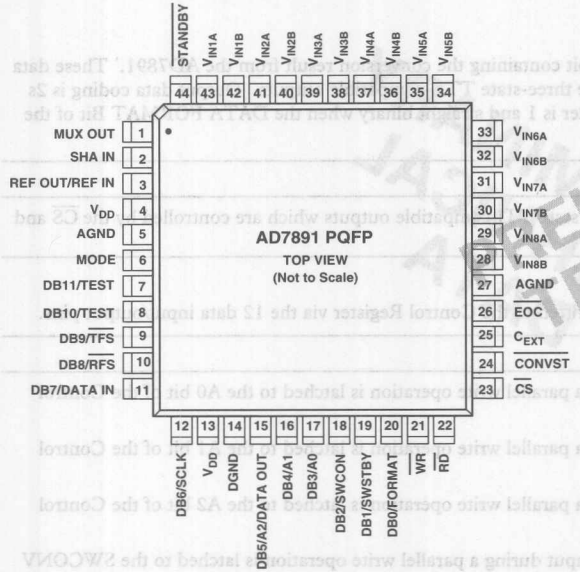
mitted and received at the same time, $\overline{RFS}$ and $\overline{TFS}$ should be connected together.

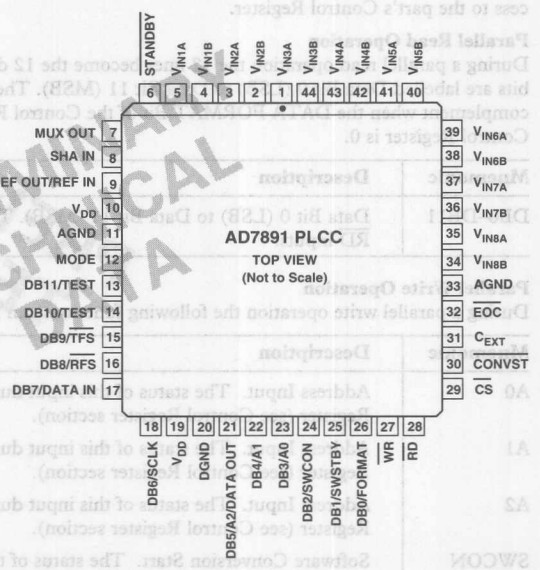
DATA OUT	Serial Data Output. Sixteen bits of serial data are provided with the DATA FORMAT bit and the three address bits of the Control Register preceding the 12 bits of conversion data. Serial data is valid on the falling edge of SCLK for sixteen edges after $\overline{RFS}$ goes low. Output conversion data coding is 2s complement when the DATA FORMAT Bit of the Control Register is 1 and straight binary when the DATA FORMAT Bit of the Control Register is 0.
DATA IN	Serial Data Input. Serial data to be loaded to the Control Register is provided at this input. The first six bits of serial data are loaded to the Control Register on the first six falling edges of SCLK after $\overline{TFS}$ goes low. Serial data on subsequent SCLK edges is ignored while $\overline{TFS}$ remains low.

PIN CONFIGURATIONS

PQFP



PLCC



PRELIMINARY TECHNICAL DATA

ORDERING GUIDE

Model	Input Ranges	Relative Accuracy	Temperature Range	Package Option*
AD7891AS-1	±5 V or ±10 V	±1 LSB	–40°C to +85°C	S-44
AD7891BS-1	±5 V or ±10 V	±1/2 LSB	–40°C to +85°C	S-44
AD7891AP-1	±5 V or ±10 V	±1 LSB	–40°C to +85°C	P-44A
AD7891BP-1	±5 V or ±10 V	±1/2 LSB	–40°C to +85°C	P-44A
AD7891AS-2	0 V to +2.5 V, 0 V to +5 V or ±2.5 V	±1 LSB	–40°C to +85°C	S-44
AD7891BS-2	0 V to +2.5 V, 0 V to +5 V or ±2.5 V	±1/2 LSB	–40°C to +85°C	S-44
AD7891AP-2	0 V to +2.5 V, 0 V to +5 V or ±2.5 V	±1 LSB	–40°C to +85°C	P-44A
AD7891BP-2	0 V to +2.5 V, 0 V to +5 V or ±2.5 V	±1/2 LSB	–40°C to +85°C	P-44A

*S = Plastic Quad Flatpack (PQFP); P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

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The Control Register for the AD7891 contains 6 bits of information as described below. These 6 bits can be written to the Control Register either in a parallel mode write operation or via a serial mode write operation. The default (power-on) condition of all bits in the Control Register is 0.

MSB

A2	A1	A0	SWCONV	SWSTBY	FORMAT

A2	Address Input. This input is the most significant address input for multiplexer channel selection.
A1	Address Input. This is the 2nd most significant address input for multiplexer channel selection.
A0	Address Input. Least significant address input for multiplexer channel selection. When the address is written to the control register, an internal pulse is initiated, the pulse width of which is determined by the value of capacitance on the C_{EXT} pin. SWCON will not sample the input signal or initiate a conversion until this pulse has timed out. This allows for the multiplexer settling time and track/hold acquisition time before the track/hold goes into hold and conversion is initiated. In applications where there is an antialiasing filter between MUX OUT and SHA IN, the filter settling time can be taken into account before the input at SHA IN is sampled. When the internal pulse times out, the track/hold goes into hold and conversion is initiated.
SWCONV	Conversion Start. Writing a 1 to this bit initiates a conversion in a similar manner to the $\overline{\text{CONVST}}$ input. Continuous conversion starts do not take place when there is a 1 in this location. The internal pulse and the conversion process are initiated when a 1 is written to this bit. With a 1 in this bit, the hardware conversion start, i.e., the $\overline{\text{CONVST}}$ input, is disabled. Writing a 0 to this bit enables the hardware $\overline{\text{CONVST}}$ input.
SWSTBY	Standby Mode Input. Writing a 1 to this bit places the device in its standby or power-down mode. Writing a 0 to this bit places the device in its normal operating mode.
FORMAT	Data Format. Writing a 0 to this bit determines that the conversion data output format is straight (natural) binary. This data format is generally be used for unipolar input ranges. Writing a 1 to this bit determines that the conversion data output format is 2s complement. This output data format is generally used for bipolar input ranges.

PRELIMINARY TECHNICAL DATA

CIRCUIT DESCRIPTION

The AD7891 is an eight-channel, high speed, 12-bit data acquisition system. It provides the user with signal scaling, multiplexer, track/hold, reference, A/D converter and high speed parallel and serial interface logic functions on a single chip. The signal conditioning on the AD7891-1 allows the part to accept analog input ranges of ±5 V or ±10 V when operating from a single supply. The input circuitry on the AD7891-2 allows the part to handle input signal ranges of 0 V to +2.5 V, 0 V to +5 V and ±2.5 V again while operating from a single +5 V supply. The part requires a +2.5 V reference which can be provided from the part's own internal reference or from an external reference source.

Unlike other single chip solutions, the AD7891 provides the user with separate access to the multiplexer and the A/D converter. This means that the flexibility of separate multiplexer and ADC solutions is not sacrificed with the one-chip solution. With access to the multiplexer output, the user can implement external signal conditioning between the multiplexer and the track/hold. It means that one antialiasing filter can be used on the output of the multiplexer to provide the antialiasing function for all eight channels. The extra settling time introduced into the circuit by the external circuitry can be allowed for by the AD7891 by connecting a single capacitor to the C_{EXT} pin. If no external signal conditioning is required, the multiplexer output (MUX OUT) can simply be connected directly to the track/hold input (SHA IN).

Conversion is initiated on the AD7891 either by pulsing the $\overline{\text{CONVST}}$ input or by writing a logic 1 to the SWCONV bit of the Control Register. When using the hardware $\overline{\text{CONVST}}$ input, the on-chip track/hold goes from track to hold mode and the conversion sequence is started on the rising edge of the $\overline{\text{CONVST}}$ signal. When a software conversion start is initiated, an internal pulse is generated which delays the track/hold acquisition point and the conversion start sequence until the pulse is timed out. This internal pulse is initiated (goes from low to high) whenever a write to the AD7891 Control Register takes place with a 1 in the SWCONV bit. It then starts to discharge and the track/hold cannot go into hold and conversion cannot be initiated until the C_{EXT} pin has crossed its trigger point of 2.5 V. The discharge time of the voltage on C_{EXT} depends upon the value of capacitor connected to the C_{EXT} pin.

The conversion clock for the part is internally generated and conversion time for the AD7891 is 1.6 µs from the rising edge of the hardware $\overline{\text{CONVST}}$ signal, and the track/hold acquisition time for the part is 400 ns. To obtain optimum performance from the part, the data read operation should not occur during the conversion or during 200 ns prior to the next conversion. This allows the part to operate at throughput rates up to 500 ksps in the parallel mode and achieve data sheet specifications. In the serial mode, the maximum achievable throughput rate for the part is 385 ksps (assuming a 20 MHz serial clock).

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INTERFACE INFORMATION

The AD7891 provides two interface options, a 12-bit parallel interface and a high speed serial interface. The required interface mode is selected via the MODE pin. The two interface modes are discussed in the following sections.

Parallel Interface Mode

The parallel interface mode is selected by tying the MODE input to a logic high. Figure 2 shows a timing diagram illustrating the operational sequence of the AD7891 in parallel mode for a hardware conversion start. The multiplexer address is written to the AD7891 on the rising edge of the $\overline{WR}$ input. The on-chip track/hold goes into hold mode on the rising edge of $\overline{CONVST}$, and conversion is also initiated at this point. When conversion is complete, the end of conversion line ($\overline{EOC}$) pulses low to indicate that new data is available in the AD7891's output register. This $\overline{EOC}$ line can be used to drive an edge-triggered interrupt of a microprocessor. $\overline{CS}$ and $\overline{RD}$ going low accesses the 12-bit conversion result. In systems where the part is interfaced to a gate array or ASIC, this $\overline{EOC}$ pulse can be applied to the $\overline{CS}$ and $\overline{RD}$ inputs to latch data out of the AD7891 and into the gate array or ASIC. This means that the gate array or ASIC does not need any conversion status recognition logic, and it also eliminates the logic required in the gate array or ASIC to generate the read signal for the AD7891.

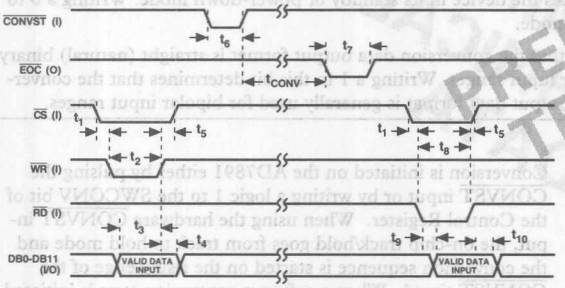

Figure 2. Parallel Mode Timing Diagram

Serial Interface Mode

The serial interface mode is selected by tying the MODE input to a logic low. In this case, five of the data/control inputs of the parallel mode assume serial interface functions. The serial interface on the AD7891 is a five-wire interface with read and write capabilities, with data being read from the output register via the DATA OUT line and data being written to the Control Register via the DATA IN line. The part operates in a slave or external clocking mode and requires an externally applied serial clock to the SCLK input to access data from the data register or write data to the control register. There are separate framing signals for the read ($\overline{RFS}$) and write ($\overline{TFS}$) operations.

Read Operation

Figure 3 shows the timing diagram for reading from the AD7891 in serial mode. $\overline{RFS}$ goes low to access data from the AD7891. The serial clock input does not have to be continuous. The serial data can be accessed in a number of bytes. However, $\overline{RFS}$ must remain low for the duration of the data transfer operation. Sixteen bits of data are transmitted in serial mode with the data FORMAT bit, followed by the three address bits in the Control Register, followed by the 12-bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. At the end of the read operation, the DATA OUT line is three-stated by a rising edge on either the SCLK or $\overline{RFS}$ inputs, whichever occurs first.

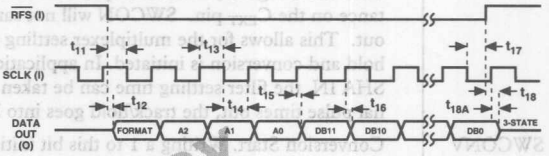

Figure 3. Serial Mode Read Operation

Write Operation

Figure 4 shows a write operation to the Control Register of the AD7891. The $\overline{TFS}$ input goes low to indicate to the part that a serial write is about to occur. The AD7891 Control Register requires only six bits of data. These are loaded on the first six clock cycles of the serial clock with data on all subsequent clock cycles being ignored. Serial data to be written to the AD7891 must be valid on the falling edge of SCLK.

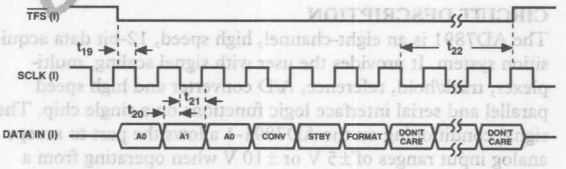

Figure 4. Serial Mode Write Operation

Simplifying the Serial Interface

To minimize the number of interconnect lines to the AD7891 in serial mode, the user can connect the $\overline{RFS}$ and $\overline{TFS}$ lines of the AD7891 together and read and write from the part simultaneously. In this case, new Control Register data line selecting the input channel and providing a conversion start command should be provided on the DATA IN while the part provides the result from the conversion just completed on the DATA OUT line.

PRELIMINARY TECHNICAL DATA

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C_{EXT} FUNCTIONING

The C_{EXT} input on the AD7891 provides a means of determining how long after a new channel address is written to the part that a conversion can take place. The reason behind this is twofold. First, when the input channel to the AD7891 is changed, the input voltage on this new channel is likely to be very different from the previous channel voltage. Therefore, the part's track/hold has to acquire the new voltage before an accurate conversion can take place. An internal pulse delays any software conversion start command (as well as the signal to send the track/hold into hold) until after this pulse has timed out.

The second reason is to allow the user to connect external antialiasing or signal conditioning circuitry between MUX OUT and SHA IN. This external circuitry will introduce extra settling time into the system. The C_{EXT} pin provides a means for the user to extend the internal pulse to take this extra settling time into account. Basically, varying the value of the capacitor on the C_{EXT} pin varies the duration of the internal pulse.

The duration of the internal pulse can be seen on the C_{EXT} pin. The C_{EXT} pin goes from a low to a high when a software conversion start is written to the part. Once the C_{EXT} pin has discharged to crossing its nominal trigger point of 2.5 V, the internal pulse is timed out. With no capacitor on the C_{EXT} pin, the internal pulse duration is 600 ns.

If the multiplexer output (MUX OUT) is connected directly to the track/hold input (SHA IN), then external settling need not be taken into account by the internal pulse width. In this case, the 600 ns internal pulse duration with no C_{EXT} is sufficient to cater for the 400 ns acquisition time. If external circuitry is connected between MUX OUT and SHA IN, then the extra settling time introduced by this circuitry will have to be taken into account by placing a larger value of capacitance on the C_{EXT} pin.

5

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

FEATURES
2 μs ADC with T/H
4-Channel MUX
AD899 Compatible
+5 Volt Operation
On-Chip Reference
4 μs Voltage Output DAC
Fast Bus Access Time—75 ns

APPLICATIONS
Servo Controls
Digitally Controlled Calibration
Process Control Equipment

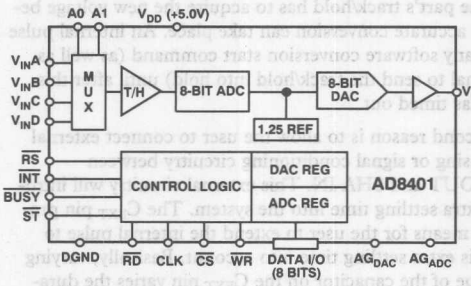
GENERAL DESCRIPTION

The AD8401 is a complete data acquisition and control system containing ADC, DAC, 4-channel MUX, and internal voltage reference. Built using CBCMOS, this monolithic circuit offers the user a complete system with very high package density and reliability.

The converter is a successive approximation ADC with T/H, and is capable of operating with conversion times as short as 2 μs. Analog input bandwidth is 200 kHz, and DAC output voltage settling time is less than 4 μs, making the AD8401 capable of controlling servo loops with speed and precision.

The 8-bit data interface provides both read and write operation for parallel bus interfaces to microcontrollers and DSP processors. An external 5 MHz clock sets the 2 μs conversion rate. Slower clocks reduce the conversion time and the internal power dissipation. The standard control lines: Reset, Busy, Interrupt, Read and Write complete the handshaking signals for microprocessor communication. A start trigger $\overline{ST}$ input allows precise sampling intervals in synchronous sampling applications.

FUNCTIONAL BLOCK DIAGRAM



The input multiplexer addressing is designed for direct interface to the AD899 hard-disk drive, read-channel device with no extra hardware or special software. Analog input range levels are likewise compatible with the AD899.

The AD8401 is designed to operate from a single +5 volt supply, which will give an ADC input range of 0 V to 3.0 V, and DAC output range of 0 V to 2.5 V.

The AD8401 is offered in the SOIC-28 surface mount package, and is guaranteed to operate over the extended industrial temperature range of −40°C to +85°C.

ADC ELECTRICAL CHARACTERISTICS

(@ V_{DD} = +5.0 V ± 5%, AG_{DAC} = AG_{ADC} = 0.0 V; f_{CLK} = 5 MHz; −40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N		8			Bits
Total Unadjusted Error	TUE			±3		LSB
Relative Accuracy	INL		−1		+1	LSB
Differential Nonlinearity	DNL		−1		+1	LSB
Offset Error	V_{OSE}	T_A = +25°C	−4		+4	LSB
		T_A = Full Temp Range	−6		+6	LSB
Full-Scale Error	A_E	T_A = +25°C	−4		+4	LSB
		T_A = Full Temp Range	−6		+6	LSB
ΔFull-Scale/ΔV_{DD}		T_A = +25°C			1	LSB
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio	SNR			44		dB
Total Harmonic Distortion	THD			48		dB
Intermodulation Distortion	IMD			60		dB
Frequency Response		0 to 200 kHz		0.1		dB
Track/Hold Acquisition Time	t_{AQ}			200		ns
ANALOG INPUTS (Applies to Inputs A, B, C, D)						
Unipolar Input Range	V_{IN}		0		3	V
Input Current	I_{IN}		−500		+500	µA
Input Capacitance	C_{IN}			10		pF
LOGIC INPUTS						
Clock Input Current Low	I_{CKL}	V_{IN} = 0 V	1.6			mA
Clock Input Current High	I_{CKH}	V_{IN} = V_{DD}			40	µA
Input Leakage Current	I_L	$\overline{CS}$, $\overline{RD}$, $\overline{RS}$, $\overline{ST}$			10	µA
LOGIC OUTPUTS (Applies to Outputs DB0–DB7, $\overline{INT}$, $\overline{BUSY}$)						
Logic Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Logic Output High Voltage	V_{OH}	I_{OH} = 200 µA	4.0			V
Output Leakage Current	I_{OZ}	$\overline{CS}$ = 1 (Except $\overline{INT}$ & $\overline{BUSY}$)			10	µA
Output Capacitance	C_{OZ}	$\overline{CS}$ = 1 (Except $\overline{INT}$ & $\overline{BUSY}$)			10	pF
CONVERSION TIME						
	t_C	External Clock			2	µs

Specifications subject to change without notice.

Table I. Multiplexer Address Input Decode

A1	A0	Input Selected
0	0	V_{IN}A
0	1	V_{IN}B
1	0	V_{IN}C
1	1	V_{IN}D

DAC ELECTRICAL CHARACTERISTICS

(@ V_{DD} = +5.0 V ± 5%, AG_{DAC} = AG_{ADC} = 0.0 V; R_L = 2 kΩ, C_L = 100 pF to AG_{DAC}; −40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N		8			Bits
Total Unadjusted Error	TUE			±2		LSB
Relative Accuracy	INL		−1		+1	LSB
Differential Nonlinearity	DNL		−1		+1	LSB
Offset Error	V_{OSE}	T_A = +25°C	−2		+2	LSB
		T_A = Full Temp Range	−2.5		+2.5	LSB
Full-Scale Error	A_E	T_A = +25°C	−3		+3	LSB
		T_A = Full Temp Range	−4		+4	LSB
ΔFull-Scale/ΔV_{DD}		T_A = +25°C	−0.5		+0.5	LSB
Load Regulation at Full-Scale			−0.2		+0.2	LSB
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio	SNR			44		dB
Total Harmonic Distortion	THD			48		dB
ANALOG OUTPUT						
Output Voltage Range	OVR		0		+2.5	V
LOGIC INPUTS (Applies to DB0 – DB7, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{RS}$)						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_L		−10		10	μA
Input Capacitance	C_{IL}				10	pF
AC CHARACTERISTICS						
Voltage Output Settling Time	t_S	To ±1/2 LSB of Final Value		2	4	μs
Positive Full-Scale Change	t_{POS}	10% to 90%		1	2	μs
Negative Full-Scale Change	t_{NEG}	90% to 10%		2	4	μs
DAC Glitch Impulse				15		nV s
Digital Feedthrough				1		nV s
V_{IN} to V_{OUT} Isolation		f = 50 kHz		60		dB
POWER REQUIREMENTS						
Positive Supply Current	I_{DD}	No Load			13	mA

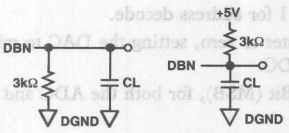
Specifications subject to change without notice.

TIMING ELECTRICAL SPECIFICATIONS

(@ V_{DD} = +5.0 V ± 5%, AG_{DAC} = AG_{ADC} = 0.0 V; f_{CLK} = 5 MHz; −40°C ≤ T_A ≤ +85°C, unless otherwise noted)

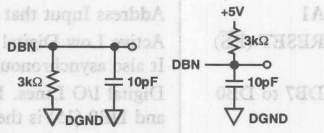
Parameter[1, 2, 3]	Symbol	Condition	Min	Typ	Max	Units
DAC TIMING (See Figure 8 Timing Diagram)						
$\overline{WR}$ Pulse Width	t_1		50			ns
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_2		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_3		0			ns
Data Setup Time	t_4		60			ns
Data Hold Time	t_5		0			ns
ADC TIMING (See Figures 6 and 7 Timing Diagrams)						
$\overline{ST}$ Pulse Width	t_6		40			ns
$\overline{ST}$ to $\overline{BUSY}$ Delay	t_7				110	ns
$\overline{BUSY}$ to $\overline{INT}$ Delay	t_8				30	ns
$\overline{BUSY}$ to $\overline{CS}$ Delay	t_9		0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{10}		0			ns
$\overline{RD}$ Pulse Width[4]	t_{11}		75			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{12}		0			ns
Data Access after $\overline{RD}$	t_{13}	C_L = 20 pF	10		75	ns
Data Access after $\overline{RD}$	t_{13}	C_L = 100 pF	10		135	ns
Bus Relinquish after $\overline{RD}$	t_{14}		10		70	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{15}				85	ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_{16}				110	ns
Data Valid after $\overline{BUSY}$	t_{17}	C_L = 20 pF			90	ns
Data Valid after $\overline{BUSY}$	t_{17}	C_L = 100 pF			135	ns

NOTES
[1]All input control signals are specified with t_R = t_F = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[2]t_{13} and t_{17} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross either 0.8 V or 2.4 V.
[3]t_{14} is defined as the time required for the data line to change 0.5 V when loaded with the circuit of Figure 2.
[4]t_{11} is determined by t_{13}.



a. High Z to V_{OH} *b. High Z to V_{OL}*

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High Z *b. V_{OL} to High Z*

Figure 2. Load Circuits for Bus Relinquish Time Test

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{DD}) . . . . . +8 V
Input Voltages . . . . . −0.3 V to V_{DD} + 0.3 V
Output Short-Circuit Duration . . . . . Indefinite
Package Power Dissipation . . . . . (T_J max–T_A)/θ_{JA}
Thermal Resistance θ_{JA}
28-Lead SOIC (R) . . . . . 53°C/W
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . −40°C to +85°C
Junction Temperature Range (T_J max) . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

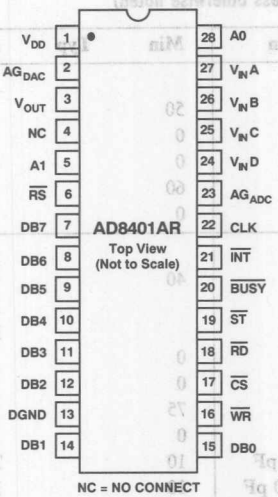
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD8401AR	−40°C to +85°C	28-Lead SOIC	SOL-28
AD8401Chips	+25°C	Die	

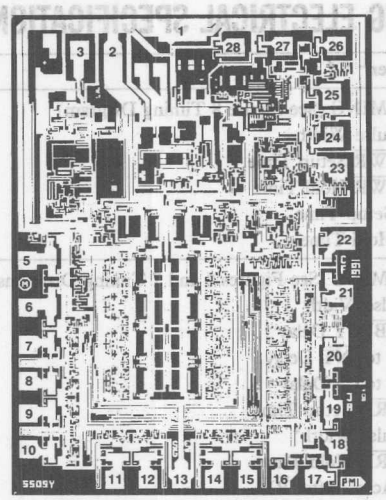
NOTES
[1]The AD8401 contains 1257 transistors.
[2]For outline information see Package Information section.

PIN CONFIGURATION



NC = NO CONNECT

DICE CHARACTERISTICS



Die Size 91 X 121 mil = 11,011 sq mil

PIN DESCRIPTIONS

Pin#	Name	Description
1	V_{DD}	Positive Supply. Nominal value +5 volts. This pad requires 2 bonds for die assembly. The substrate is common with V_{DD}.
2	AG_{DAC}	Analog Ground for the DAC. There is a separate analog ground for the ADC.
3	V_{OUT}	Voltage Output from the DAC.
4	NC	No Connect.
5	A1	Address Input that controls multiplexer. See Table I for address decode.
6	RESET ($\overline{RS}$)	Active Low Digital Input that clears the DAC register to zero, setting the DAC to minimum scale. It also asynchronously clears the $\overline{INT}$ line of the ADC.
7–12, 14, 15	DB7 to DB0	Digital I/O Lines. DB7 (7) is the Most Significant Bit (MSB), for both the ADC and the DAC, and DB0 (15) is the Least Significant Bit (LSB).
13	DGND	Digital Ground.
16	$\overline{WR}$	Rising Edge Triggered Write Input. Used to load data into the DAC register.
17	$\overline{CS}$	Chip Select. Active Low Input
18	$\overline{RD}$	Active Low Read Input. When this input is active, ADC data can be read from the part. $\overline{RD}$ going low starts the ADC conversion.
19	$\overline{ST}$	Falling Edge Triggered Start Input. Used for applications requiring precise sample timing. The falling edge of $\overline{ST}$ starts the conversion and sets the $\overline{BUSY}$ low. The $\overline{ST}$ is not gated by $\overline{CS}$.
20	$\overline{BUSY}$	ADC Active Low, Status Output. When the ADC is performing a conversion, the $\overline{BUSY}$ output is low.
21	$\overline{INT}$	Active Low Output. The Interrupt output notifies the system that the ADC has completed its conversion. $\overline{INT}$ goes high on the rising edge of $\overline{CS}$ or $\overline{RD}$. It will also be forced high when RESET is asserted.
22	CLK	External Clock Input Pin. Accepts a TTL or 5 V CMOS input logic levels.
23	AG_{ADC}	Analog ADC Ground
27–24	V_{IN}A, B, C, D	Four Analog Inputs
28	A0	Address input that controls multiplexer. See Table I for address decode.

OPERATION

The AD8401 is a complete data acquisition and control system. It contains the DAC, a four channel input multiplexer, a track/hold, an ADC, as well as an internal bandgap reference. It interfaces to the microcontroller via an 8-bit digital I/O port.

D/A CONVERTER SECTION

The DAC is an 8-bit voltage mode DAC with an output that swings from AG_{DAC} to the 1.25 volt bandgap voltage. It uses an R-2R ladder fed by PNP current sources which allow the output to swing to ground so that the DAC operates in a unipolar mode.

AMPLIFIER SECTION

The DAC's output is buffered by an internal high speed op amp. The op amps output range is set at 0 V to 2.5 V. The op amp has a 500 ns typical settling time to 0.2% for positive slewing signals. There are differences in settling time for negative slewing signals. Signals going to zero volts will settle slightly slower to ground than is seen in the positive direction.

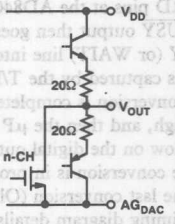


Figure 3. Equivalent Amplifier Output Stage

Current sinking capability is also limited near zero volts in single supply operation. Figure 3 provides an equivalent amplifier output stage schematic.

INTERNAL REFERENCE

An on-chip bandgap is provided as a voltage reference to both the DAC and the ADC. This reference is internal to the AD8401 and is not accessible to the user. It is laser trimmed for both absolute accuracy and temperature coefficients. The reference is internally buffered by a separate control amplifier for both the DAC and ADC to improve isolation between the converters.

DIGITAL I/O

The 8-bit parallel data I/O port on the AD8401 provides access to both the DAC and the ADC. This port is TTL/CMOS compatible with three-state outputs that are ESD protected.

The data format is binary. This data coding applies to both the DAC and the ADC. See the applications information section.

ADC SECTION

A fast successive approximation ADC is used to attain a conversion time of 2 microseconds. Start of conversion is initiated by $\overline{CS}$ and $\overline{RD}$. Following a Start command the $\overline{BUSY}$ signal will become active and another Start command should not be given until the conversion is complete.

The RESET ($\overline{RS}$) input does not affect A/D conversion, but the $\overline{INT}$ (Interrupt or conversion complete) which normally goes active low at the end of a conversion will be forced high by RESET asynchronously.

Figure 4 shows the wave forms for a conversion cycle. The track and hold begins holding the input voltage V_{IN} approximately 50 ns after the falling edge of the Start command. The MSB decision is made approximately 50 ns after the second falling edge of the CLK. If t_X is greater than 50 ns, then the falling edge of the CLK will be seen as the first falling clock edge. If t_X is less than 50 ns, the first MSB conversion will not occur until one clock cycle later. The following bits will each be converted in a similar manner 50 ns after each CLK edge until all eight bits have been converted. After the end of conversion the contents of the ADC SAR register are transferred to the output data latch, the track and hold is returned to the track mode, $\overline{INT}$ goes low and the SAR is reset.

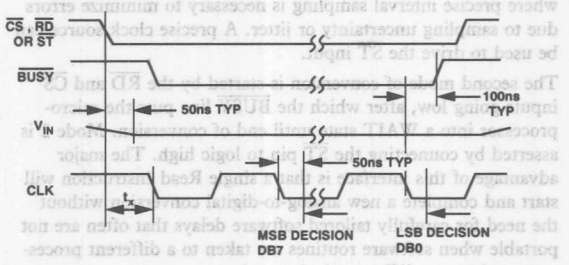


Figure 4. Operating Waveforms Using the External Clock

ANALOG INPUT

The analog inputs of the AD8401 are fed into resistor voltage-divider networks with a typical value of 8.5 kΩ. The amplifiers driving these inputs must have an output resistance low enough to drive these nodes without losing accuracy. Taps from the voltage dividers are connected to the track and hold amplifier by the multiplexer switches.

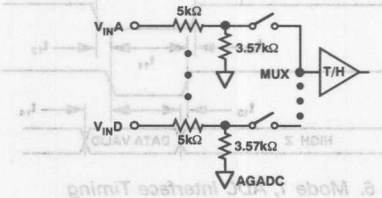


Figure 5. Equivalent Analog Input Circuit

TRACK-AND-HOLD AMPLIFIER

Following the resistive divider at the input of the AD8401 is a track-and-hold amplifier that captures input signals accurately up to the 200 kHz Nyquist frequency of the ADC. To attain this performance the T/H amplifier must have a much greater bandwidth than the signal of interest. Because of this the user must be careful to band limit the input signal to avoid aliasing high frequency components and noise into the passband.

The track-and-hold amplifier is internally controlled by the Start command and is not directly available to the user. After the Start command signal the track-and-hold is placed into the hold mode; it returns to the track mode after the conversion is complete.

compatible. The external clock speed is 5 MHz and the duty cycle may vary from 30% to 70%. The external clock can be continuously operated between conversions.

DIGITAL INTERFACE: ADC TIMING AND CONTROL

Two basic ADC operating modes are available with the AD8401. The first mode uses the Start ($\overline{ST}$) pin to trigger a synchronized A/D conversion. As soon as the $\overline{ST}$ pin is asserted, the T/H switches from tracking to the hold mode capturing the present analog input-voltage sample. With the T/H holding the analog sample the successive-approximation analog-to-digital conversion is completed on that sample value. At the end of conversion the T/H returns to the tracking mode. This mode of conversion is ideal for digital signal processing applications where precise interval sampling is necessary to minimize errors due to sampling uncertainty or jitter. A precise clock source can be used to drive the $\overline{ST}$ input.

The second mode of conversion is started by the $\overline{RD}$ and $\overline{CS}$ inputs going low, after which the $\overline{BUSY}$ line puts the microprocessor into a WAIT state until end of conversion. Mode 2 is asserted by connecting the $\overline{ST}$ pin to logic high. The major advantage of this interface is that a single Read Instruction will start and complete a new analog-to-digital conversion without the need for carefully tailored software delays that often are not portable when software routines are taken to a different processor running at a different clock speed.

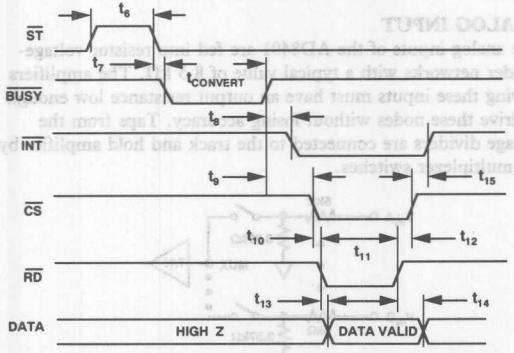


Figure 6. Mode 1, ADC Interface Timing

Mode 1 Interface

As shown in Figure 6, the falling edge of the $\overline{ST}$ pulse initiates a conversion and puts the T/H amplifier into the hold mode. The $\overline{BUSY}$ signal goes low during the whole A/D conversion time and returns high signaling end of conversion. The $\overline{INT}$ line can be used to interrupt the microprocessor. When the microprocessor performs a READ to access the AD8401 data, the rising edges of $\overline{CS}$ or $\overline{RD}$ will reset the $\overline{INT}$ output to high after the t_{15} timing specification. $\overline{INT}$ can also be used to externally trigger a pulse that activates the $\overline{CS}$ and $\overline{RD}$ and places the new data into a buffer or First In First Out FIFO memory. The microprocessor can then load a series of readings from this buffer memory at a convenient time. Care must be taken not to have the $\overline{ST}$ input high when $\overline{RD}$ is brought low; otherwise, the AD8401 will not operate properly. Also triggering the $\overline{ST}$ line a second time before conversion is complete will cause erroneous readings.

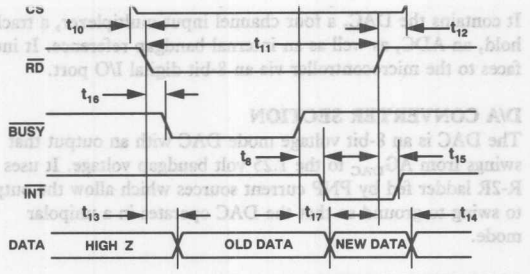


Figure 7. Mode 2, ADC Interface Timing

Mode 2 Interface

This interface mode can be used with microprocessors that can be put into a WAIT state for at least 2 microseconds. The $\overline{ST}$ pin must be tied to logic high for proper operation. The microprocessor begins a conversion by executing a READ instruction that asserts the $\overline{CS}$ and $\overline{RD}$ pins at the AD8401's decoded address. The AD8401 $\overline{BUSY}$ output then goes low, forcing the microprocessor's READY (or WAIT) line into a WAIT state. The analog input signal is captured by the T/H on the falling edge of $\overline{RD}$. When the conversion is complete (8 clocks later), the $\overline{BUSY}$ line returns high, and then the µP completes its READ of the new data now on the digital output port of the AD8401. Note that while conversion is in progress the ADC places the results from the last conversion (Old Data) on the data bus. The Figure 7 timing diagram details the applicable timing specification requirements.

DIGITAL INTERFACE: DAC TIMING AND CONTROL

Table II shows the truth table for DAC operation. The internal 8-bit DAC register contents are loaded from the data bus when both $\overline{WR}$ and $\overline{CS}$ are asserted. The DAC register determines the D/A converter analog-output voltage. The $\overline{WR}$ input is a positive edge triggered input that loads the bus data into the DAC register subject to the data setup and data hold timing requirements. When $\overline{CS}$ and $\overline{WR}$ are low, the DAC register contents will not change with changing data bus values. Figure 8 provides the detail timing diagram for write cycle operation.

Table II. DAC Register Logic

$\overline{CS}$	$\overline{WR}$	$\overline{RS}$	DAC Function
H	H	H	No Effect
L	L	H	No Effect
L	∧	H	DAC Register Updated
∧	L	H	DAC Register Updated
X	X	L	DAC Register Loaded with all Zeros

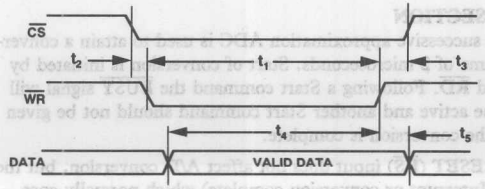


Figure 8. Write Cycle Timing

An active low pulse, at any time, on the RESET pin asynchronously forces all DAC register bits to zero. The DAC output voltage becomes zero volts and stays at that value until a new data word is loaded into the DAC register with a new $\overline{WR}$ command. The equivalent input logic for the DAC register loading is shown in Figure 9.

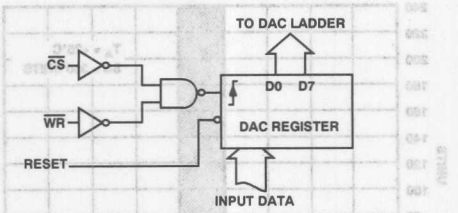


Figure 9. Equivalent DAC Register Control Logic

TYPICAL PERFORMANCE CHARACTERISTICS

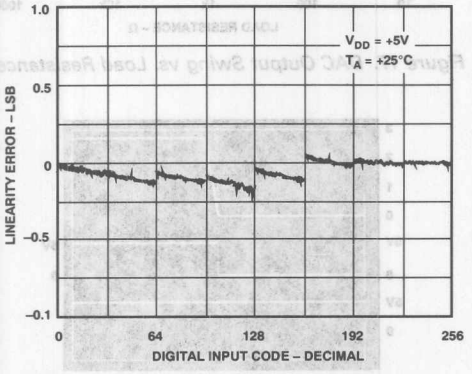


Figure 10. ADC Linearity Error vs. Digital Code

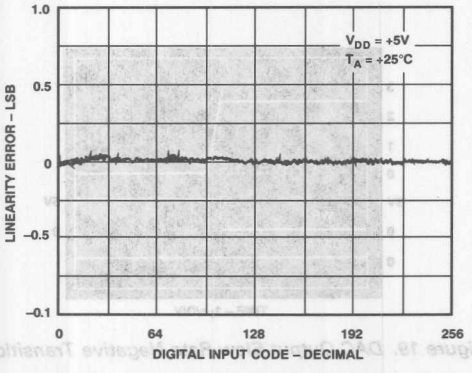


Figure 11. DAC Linearity Error vs. Digital Code

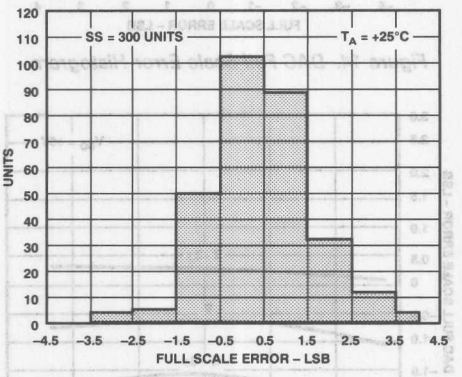


Figure 12. ADC Full-Scale Error Histogram

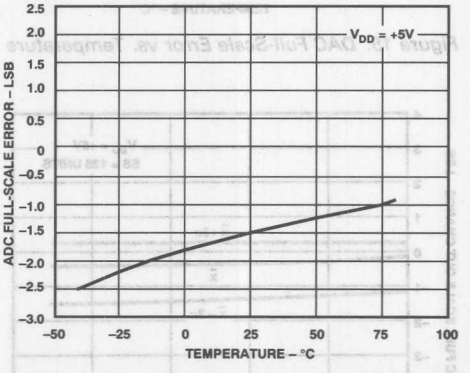


Figure 13. ADC Full-Scale Error vs. Temperature

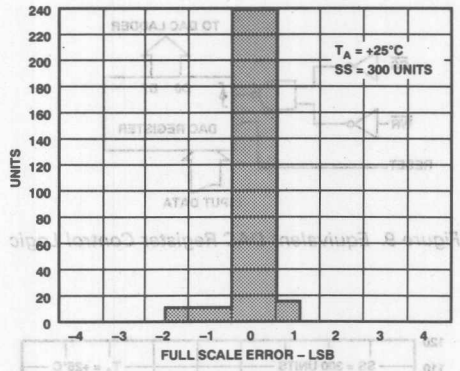


Figure 14. DAC Full-Scale Error Histogram

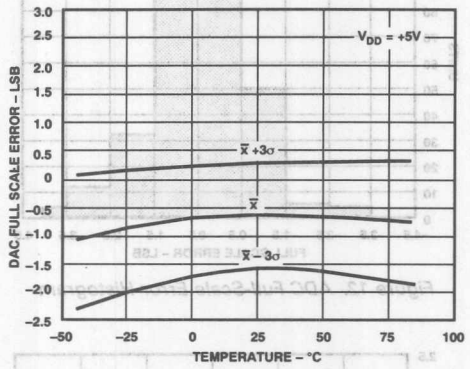


Figure 15. DAC Full-Scale Error vs. Temperature

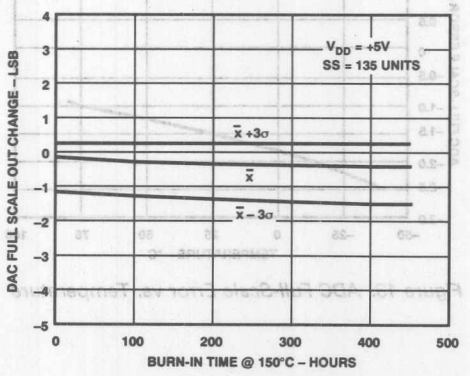


Figure 16. DAC Full-Scale Out Change vs. Time Accelerated by Burn-In

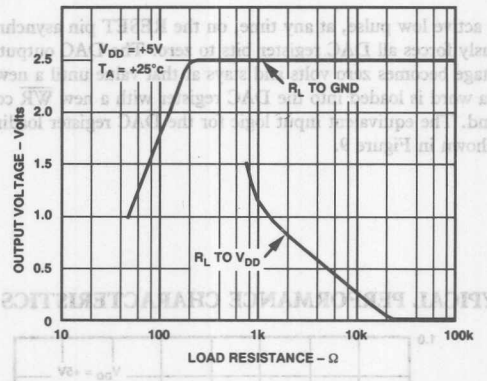


Figure 17. DAC Output Swing vs. Load Resistance

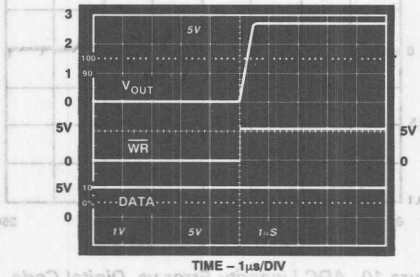


Figure 18. DAC Output Slew Rate Positive Transition

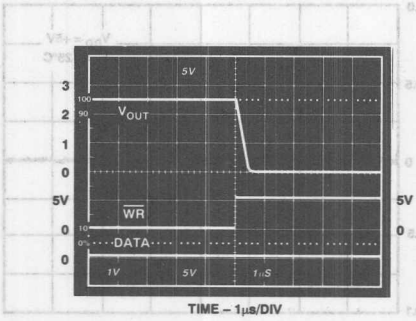


Figure 19. DAC Output Slew Rate Negative Transition

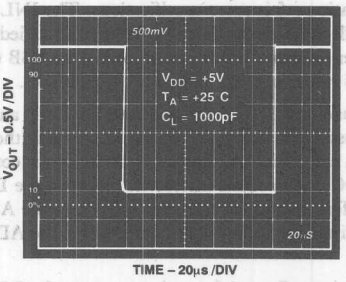


Figure 20. DAC Output Swing with Capacitive Load

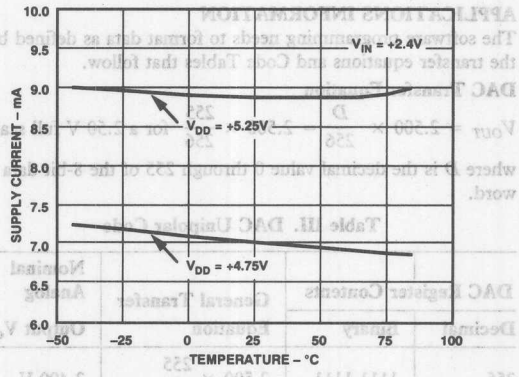


Figure 21. Supply Current vs. Temperature

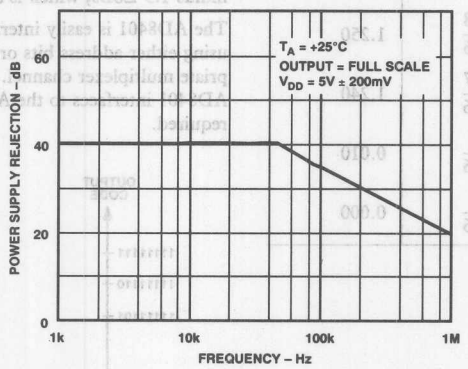


Figure 22. Power Supply Rejection Ratio vs. Frequency

The software programming needs to format data as defined by the transfer equations and Code Tables that follow.

DAC Transfer Equation

$$V_{OUT} = 2.500 \times \frac{D}{256} = 2.500 \times \frac{255}{256} \text{ for a 2.50 V full scale}$$

where D is the decimal value 0 through 255 of the 8-bit data word.

Table III. DAC Unipolar Code

DAC Register Contents		General Transfer Equation	Nominal Analog Output V_{OUT}
Decimal	Binary		
255	1111 1111	$2.500 \times \frac{255}{256}$	2.490 V
129	1000 0001	$2.500 \times \frac{129}{256}$	1.260
128	1000 0000	$2.500 \times \frac{128}{256}$	1.250
127	0111 1111	$2.500 \times \frac{127}{256}$	1.240
1	0000 0001	$2.500 \times \frac{1}{256}$	0.010
0	0000 0000	$2.500 \times \frac{0}{256}$	0.000

ject to the static performance specifications. The INL, Zero-Scale and Full-Scale errors describe the total specified variation that will be encountered from part to part. One LSB of error for the 2.5 V FS range is 9.766 millivolts (= 2.50/256).

Although separate AGNDs exist for both the DAC and ADC to minimize crosstalk, writing data to the DAC while the ADC is performing a conversion may result in an incorrect conversion from the ADC due to signal interaction between the DAC and ADC. Therefore, to ensure correct operation of the ADC, the DAC register should not be updated while the ADC is converting.

The AD8401 is configured for an input range of +3.0 volts Full Scale. The nominal transfer characteristic for this range is plotted in Figure 23. The output coding is natural binary with one LSB equal to 11.72 millivolts. Note that the first code transition between 0 and 1 LSB occurs at 5.8 mV, one half of the 11.72 mV LSB step size. The last code transition occurs at Full Scale minus 1.5 LSBs, which is a 2.982 V input.

The AD8401 is easily interfaced to most microprocessors by using either address bits or address decode to select the appropriate multiplexer channel. Figure 24 shows how easily the AD8401 interfaces to the AD899. No additional hardware is required.

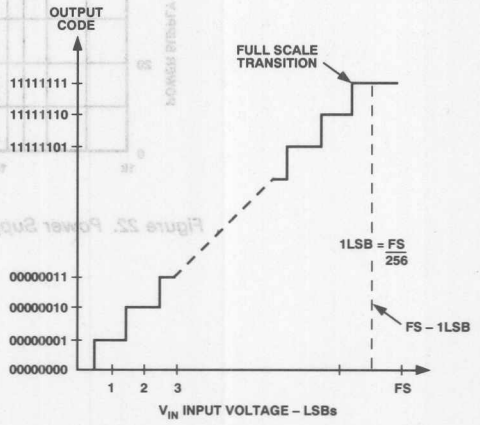


Figure 23. ADC 0 V to +3 V Input Transfer Characteristic

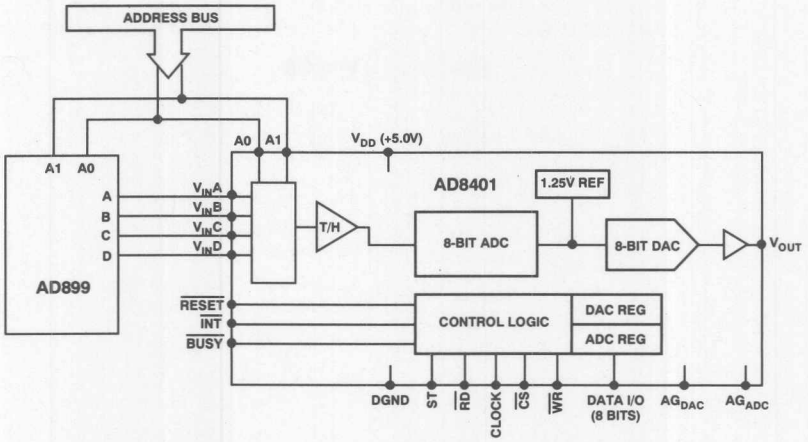
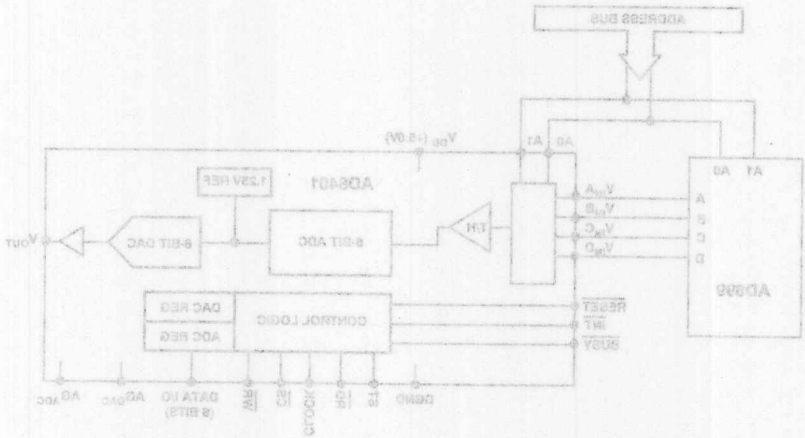


Figure 24. AD8401 Interface to the AD899 Read-Channel Hard Disk Drive Circuit

5



Sample/Track-Hold Amplifiers
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AD783 – Complete Very High Speed Sample-and-Hold Amplifier	6–14
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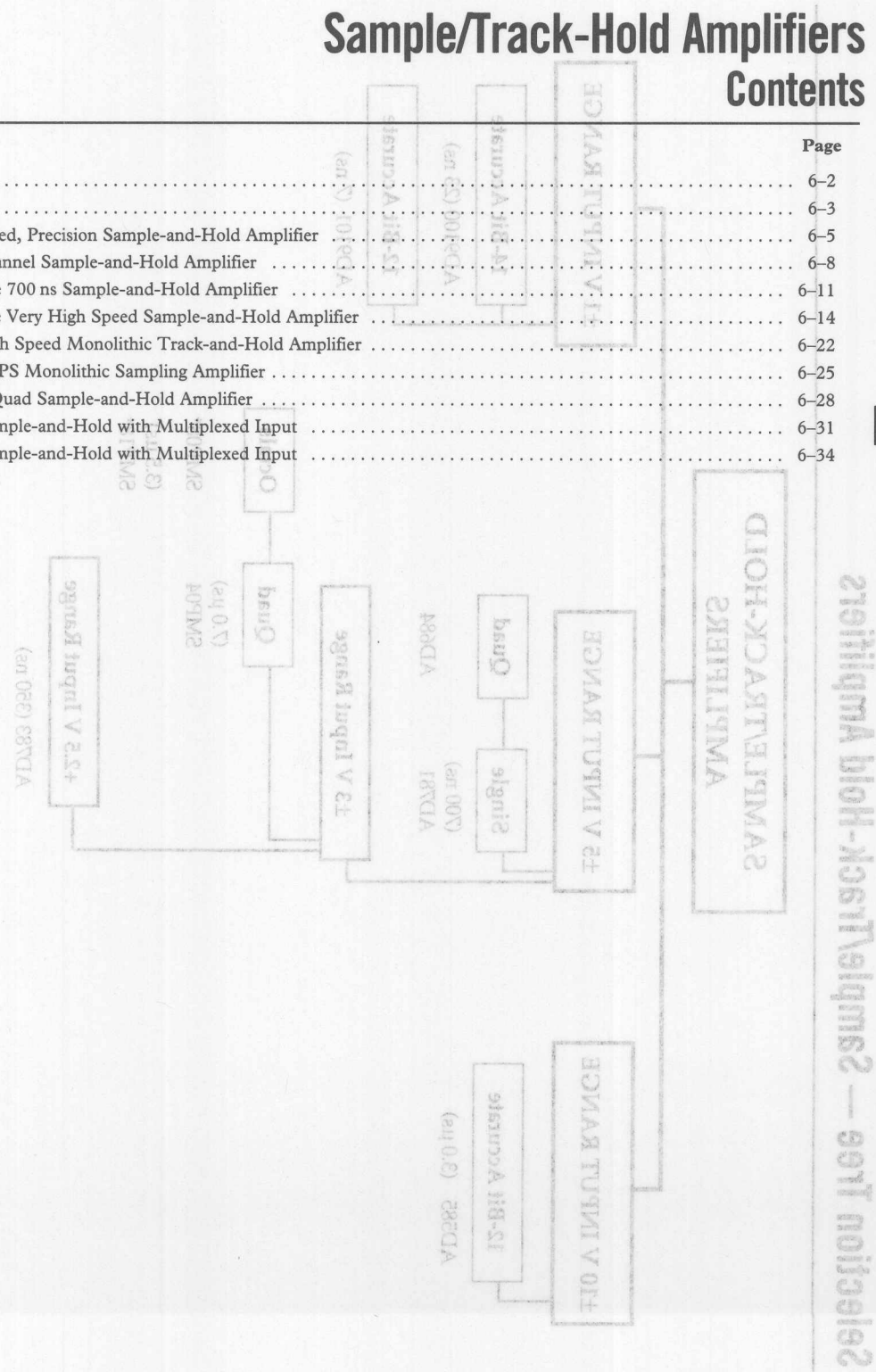
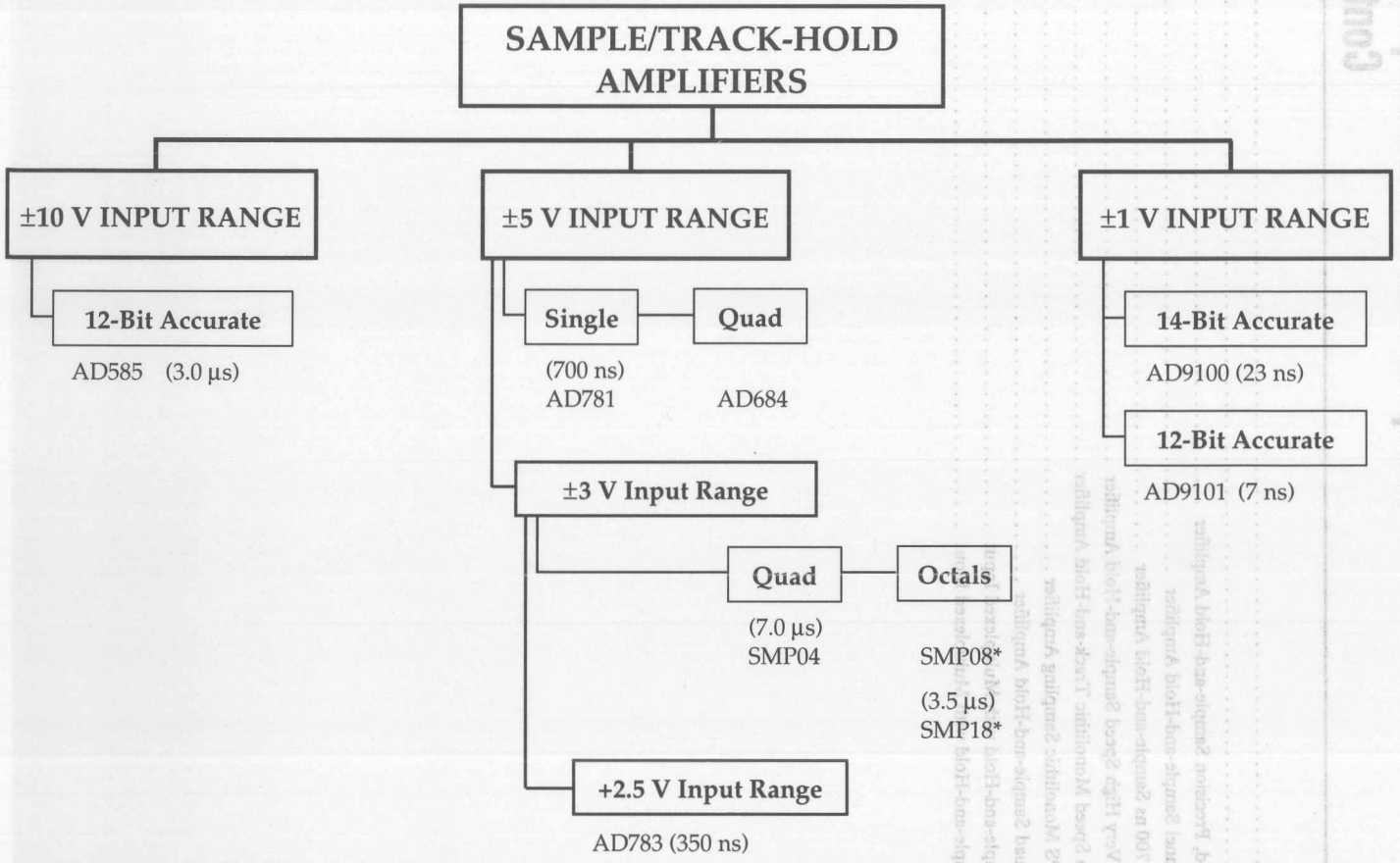
SMP04 – CMOS Quad Sample-and-Hold Amplifier	6–28
SMP08 – Octal Sample-and-Hold with Multiplexed Input	6–31
SMP18 – Octal Sample-and-Hold with Multiplexed Input	6–34



Selection Tree — Sample/Track-Hold Amplifiers



* One Input, Eight Outputs

Selection Guide—Sample/Track-Hold Amplifiers

Model	Specified Accuracy %	Acquisition Time µs max	Aperture Time ns typ	Aperture Jitter ns typ	Droop Rate µV/µs max	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
AD1154	0.00076	5.0	80	0.15	0.1	D	C, I	Low Cost 16-Bit Accurate, High Speed Amplifier	CII 4–69
AD9100	**0.01**	**0.023**	**0.8**	**<0.001**	**6000**	**D, J**	**C, I, M**	**Ultrahigh Speed Monolithic T/H, Low Distortion**	**6–22**
AD783	**0.01**	**0.375**	**15**	**0.01**	**1**	**Q, R**	**C, I, M/**	**Complete 375 ns Sample-and-Hold Amplifier**	**6–14**
AD781	**0.01**	**0.7**	**25**	**0.05**	**1**	**N, Q**	**C, I, M**	**Complete 700 ns Sample-and-Hold Amplifier**	**6–11**
AD684	**0.01**	**1.0**	**20**	**0.1**	**1**	**Q**	**C, I, M/**	**Quad, Monolithic 1 µs SHA**	**6–8**
AD585	**0.01**	**3.0**	**35**	**0.5**	**1**	**E, P, Q**	**C, I, $M/_D$**	**High Speed, Precision, On-Board Hold Cap**	**6–5**
SMP10	0.01	3.5	50	1	0.02	Q	C, $M/_D$	Low Droop Rate, High Sample/Hold Current Ratio	CII 4–109
SMP11	0.01	3.5	50	1	0.2	N, Q	C, I, $M/_{DJ}$	Low Droop Rate, Fast Hold Mode Settling Time	CII 4–109
SMP18	**0.01**	**3.5**	**—**	**—**	**0.04**	**N, Q, R**	**I**	**Fast SMP08**	**6–34**
SMP04	**0.01**	**7.0**	**—**	**—**	**0.025**	**N, Q, R**	**I, M**	**CMOS, Quad Sample-and-Hold Amplifier, Low Cost**	**6–28**
SMP81	0.045	3.5	50	1	2.0	Q	I	High Accuracy, Fast Acquisition for PCM Encodes	D
AD582	0.1	6.0	200	15		D, M	C, M/	Low Cost, 15 µs	CII 4–29
SMP08	**0.1**	**7.0**	**—**	**—**	**0.02**	**M, Q, R**	**I, M**	**Octal, Sample-and-Hold with Multiplexed Input**	**6–31**
AD9101	**0.1**	**0.007**	**0.5**	**<0.001**	**9000**	**E, R**	**C, I, M**	**100 MSPS Track-and-Hold Samplifier™**	**6–25**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]CII = *Data Converter Reference Manual, Volume II*; D = Data Sheet. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.
Samplifier is a trademark of Analog Devices, Inc.

Selection Guide—Sample/Track-Hold Amplifiers

Model	Specified Accuracy %	Acquisition Time µs max	Aperture Time ns typ	Aperture Jitter ns typ	Droop Rate µV/µs max	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
ADI154	0.000076	5.0	80	0.15	0.1	D	C, I	Low Cost 16-Bit Accurate, High Speed Amplifier	CII 4–69
ADI9100	0.01	0.025	0.8	<0.001	4000	D, J	C, I, M	Ultrahigh Speed Monolithic T/H, Low Distortion	6–22
ADI783	0.01	0.375	15	0.01	1	Q, R	C, I, M/	Complete 375 ns Sample-and-Hold Amplifier	6–14
ADI781	0.01	0.7	25	0.05	1	N, Q	C, I, M	Complete 700 ns Sample-and-Hold Amplifier	6–11
ADI684	0.01	1.0	20	0.1	1	Q	C, I, M/	Quad, Monolithic 1 µs S/HA	6–8
ADI585	0.01	3.0	35	0.5	1	E, P, Q	C, I, M/Q	High Speed, Precision, On-Board Hold Cap	6–5
SMP10	0.01	3.5	50	1	0.02	Q	C, M/Q	Low Droop Rate, High Sample/Hold Current Ratio	CII 4–109
SMP11	0.01	3.5	50	1	0.2	N, Q	C, I, M/Q	Low Droop Rate, Fast Hold Mode Settling Time	CII 4–109
SMP15	0.01	3.5	—	—	0.04	N, Q, R	I	Fast SMP68	6–24
SMP04	0.01	7.0	—	—	0.025	N, Q, R	I, M	CMOS, Quad Sample-and-Hold Amplifier, Low Cost	6–28
SMP81	0.04	3.5	50	1	2.0	Q	I	High Accuracy, Fast Acquisition for PCM Encodes	D
ADI582	0.1	6.0	200	15		D, M	C, M/	Low Cost, 15 µs	CII 4–29
SMP08	0.1	7.0	—	—	0.02	M, Q, R	I, M	Octal, Sample-and-Hold with Multiplexed Input	6–31
ADI910	0.1	0.007	0.5	<0.001	9000	E, R	C, I, M	100 MSPS Track-and-Hold Amplifier™	6–25

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP–Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP–Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.

[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, –40°C to +85°C (Some older products –25°C to +85°C); M = Military, –55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by /, to indicate 883B, $_{1}$ for JAN, $_{Q}$ for SMD, and $_{E}$ for space level.

[3]CII = Data Conversion Reference Manual, Volume II; D = Data Sheet. All other entries refer to this volume.

Boldface Type: Data sheet information in this volume.

Sampl/Hold is a trademark of Analog Devices, Inc.

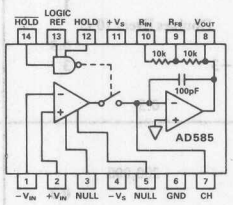
High Speed, Precision Sample-and-Hold Amplifier

AD585

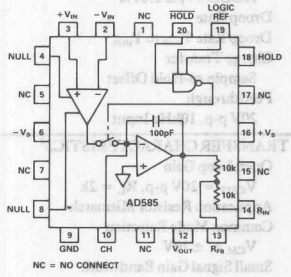
FEATURES
3.0μs Acquisition Time to ±0.01% max
Low Droop Rate: 1.0mV/ms max
Sample/Hold Offset Step: 3mV max
Aperture Jitter: 0.5ns
Extended Temperature Range: −55°C to +125°C
Internal Hold Capacitor
Internal Application Resistors
±12V or ±15V Operation
Available in Surface Mount

APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Analog Delay & Storage
Peak Amplitude Measurements
MIL-STD-883 Compliant Versions Available

DIP



LCC/PLCC PACKAGE



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD585 is a complete monolithic sample-and-hold circuit consisting of a high performance operational amplifier in series with an ultralow leakage analog switch and a FET input integrating amplifier. An internal holding capacitor and matched applications resistors have been provided for high precision and applications flexibility.

The performance of the AD585 makes it ideal for high speed 10- and 12-bit data acquisition systems, where fast acquisition time, low sample-to-hold offset, and low droop are critical. The AD585 can acquire a signal to ±0.01% in 3μs maximum, and then hold that signal with a maximum sample-to-hold offset of 3mV and less than 1mV/ms droop, using the on-chip hold capacitor. If lower droop is required, it is possible to add a larger external hold capacitor.

The high-speed analog switch used in the AD585 exhibits aperture jitter of 0.5ns, enabling the device to sample full-scale (20V peak-to-peak) signals at frequencies up to 78kHz with 12-bit precision.

The AD585 can be used with any user-defined feedback network to provide any desired gain in the sample mode. On-chip precision thin-film resistors can be used to provide gains of +1, −1, or +2. Output impedance in the hold mode is sufficiently low to maintain an accurate output signal even when driving the dynamic load presented by a successive-approximation A/D converter. However, the output is protected against damage from accidental short circuits.

The control signal for the HOLD command can be either active high or active low. The differential HOLD signal is compatible with all logic families, if a suitable reference level is provided. An on-chip TTL reference level is provided for TTL compatibility.

The AD585 is available in three performance grades. The JP grade is specified for the 0 to +70°C commercial temperature range and packaged in a 20-pin PLCC. The AQ grade is specified for the −25°C to +85°C industrial temperature range and is packaged in a 14-pin cerdip. The SQ and SE grades are specified for the −55°C to +125°C military temperature range and are packaged in a 14-pin cerdip and 20-pin LCC.

PRODUCT HIGHLIGHTS

1. The fast acquisition time (3μs) and low aperture jitter (0.5ns) make it the first choice for very high speed data acquisition systems.
2. The droop rate is only 1.0mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
3. The low charge transfer of the analog switch keeps sample-to-hold offset below 3mV with the on-chip 100pF hold capacitor, eliminating the trade-off between acquisition time and S/H offset required with other SHAs.
4. The AD585 has internal pretrimmed application resistors for applications versatility.
5. The AD585 is complete with an internal hold capacitor for ease of use. Capacitance can be added externally to reduce the droop rate when long hold times and high accuracy are required.
6. The AD585 is recommended for use with 10- and 12-bit successive-approximation A/D converters such as AD573, AD574A, AD674A, AD7572 and AD7672.
7. The AD585 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD585/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD585—SPECIFICATIONS (typical @ +25°C and V_S = ±12V or ±15V, and C_H = Internal, A = +1, $\overline{HOLD}$ active unless otherwise specified)

Model	AD585J Min	AD585J Typ	AD585J Max	AD585A Min	AD585A Typ	AD585A Max	AD585S Min	AD585S Typ	AD585S Max	Units
SAMPLE/HOLD CHARACTERISTICS										
Acquisition Time, 10V Step to 0.01%			3			3			3	µs
20V Step to 0.01%			5			5			5	µs
Aperture Time, 20V p-p Input, $\overline{HOLD}$ 0V		35			35			35		ns
Aperture Jitter, 20V p-p Input, $\overline{HOLD}$ 0V		0.5			0.5			0.5		ns
Settling Time, 20V p-p Input, $\overline{HOLD}$ 0V, to 0.01%		0.5			0.5			0.5		µs
Droop Rate			1			1			1	mV/ms
Droop Rate T_{min} to T_{max}		Doubles Every 10°C			Doubles Every 10°C			Doubles Every 10°C		
Charge Transfer			0.3			0.3			0.3	pC
Sample-to-Hold Offset	−3		3	−3		3	−3		3	mV
Feedthrough 20V p-p, 10kHz Input		0.5			0.5			0.5		mV
TRANSFER CHARACTERISTICS[1]										
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k		200,000			200,000			200,000		V/V
Application Resistor Mismatch			0.3			0.3			0.3	%
Common Mode Rejection V_{CM} = ±10V	80			80			80			dB
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p		2.0			2.0			2.0		MHz
Full Power Bandwidth V_{OUT} = 20V p-p		160			160			160		kHz
Slew Rate V_{OUT} = 20V p-p		10			10			10		V/µs
Output Resistance (Sample Mode) I_{OUT} = ±10mA			0.05			0.05			0.05	Ω
Output Short Circuit Current		50			50			50		mA
Output Short Circuit Duration		Indefinite			Indefinite			Indefinite		
ANALOG INPUT CHARACTERISTICS										
Offset Voltage			5			2			2	mV
Offset Voltage, T_{min} to T_{max}			6			3			3	mV
Bias Current			2			2			2	nA
Bias Current T_{min} to T_{max}			5			5		20	50[2]	nA
Input Capacitance, f = 1MHz		10			10			10		pF
Input Resistance, Sample or Hold 20V p-p Input, A = +1		10^{12}			10^{12}			10^{12}		Ω
DIGITAL INPUT CHARACTERISTICS										
TTL Reference Output	1.2	1.4	1.6	1.2	1.4	1.6	1.2	1.4	1.6	V
Logic Input High Voltage T_{min} to T_{max}	2.0			2.0			2.0			V
Logic Input Low Voltage T_{min} to T_{max}			0.8			0.8			0.7	V
Logic Input Current (Either Input)			50			50			50	µA
POWER SUPPLY CHARACTERISTICS										
Operating Voltage Range	+5, −10.8		±18	+5, −10.8		±18	+5, −10.8		±18	V
Supply Current, R_L = ∞	6		10	6		10	6		10	mA
Power Supply Rejection, Sample Mode	70			70			70			dB
TEMPERATURE RANGE										
Specified Performance	0		+70	−25		+85	−55		+125	°C
PACKAGE OPTIONS[3,4]										
Cerdip (Q-14)					AD585AQ			AD585SQ		
LCC (E-20A)								AD585SE		
PLCC (P-20A)		AD585JP								

NOTES

[1]Maximum input signal is the minimum supply minus a headroom voltage of 2.5V.

[2]Not tested at −55°C.

[3]E = Leadless Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

[4]For AD585/883B specifications, refer to Analog Devices Military Products Databook.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supplies ($+V_S$, $-V_S$)	±18V
Logic Inputs	$\pm V_S$
Analog Inputs	$\pm V_S$
R_{IN}, R_{FB} Pins	$\pm V_S$
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering)	300°C
Output Short Circuit to Ground	Indefinite
TTL Logic Reference Short Circuit to Ground	Indefinite

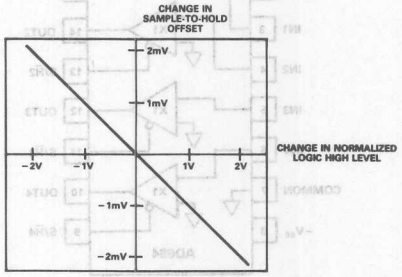


Figure 1. Sample-to-Hold Offset vs. Logic Level (HOLD Active)

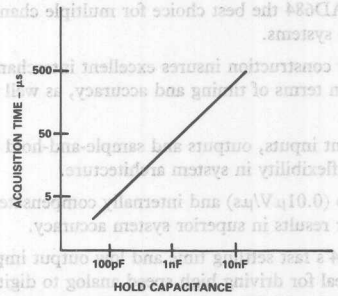


Figure 2. Acquisition Time vs. Hold Capacitance (10V Step to 0.01%)

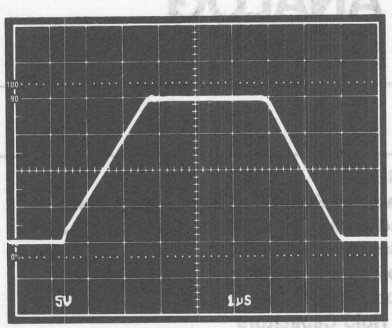


Figure 3. Large Signal Response, Sample Mode

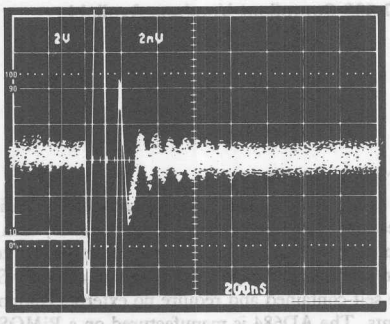


Figure 4. Sample-to-Hold Settling Time (HOLD Active)

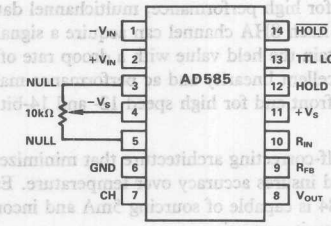


Figure 5. DIP Pin Configuration

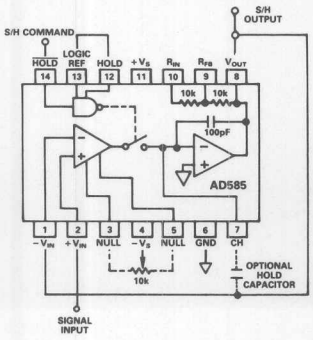


Figure 6. Connection Diagram, Gain = +1, HOLD Active

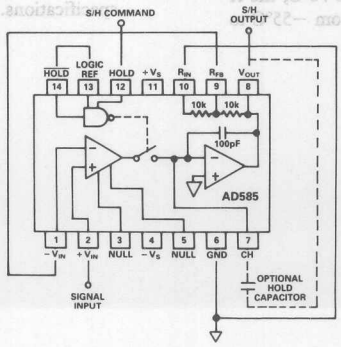


Figure 7. Connection Diagram, Gain = +2, HOLD Active

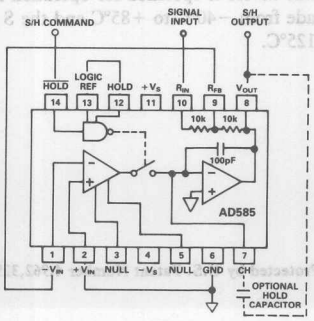


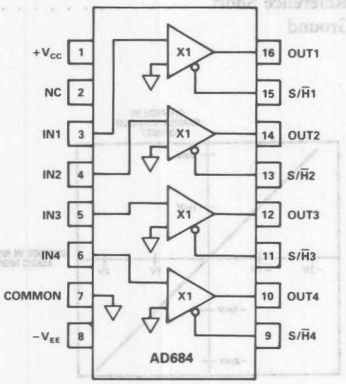
Figure 8. Connection Diagram, Gain = −1, HOLD Active

AD684*

FEATURES

Four Matched Sample-and-Hold Amplifiers
Independent Inputs, Outputs and Control Pins
500ns Hold Mode Settling
1μs Maximum Acquisition Time to 0.01%
Low Droop Rate: 0.01μV/μs
Internal Hold Capacitors
75ps Maximum Aperture Jitter
Low Power Dissipation: 430mW
0.3" Skinny DIP Package
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD684 is a monolithic quad sample-and-hold amplifier (SHA). It features four complete sampling channels, each controlled by an independent hold command. Each SHA is complete with an internal hold capacitor. The high accuracy SHA channels are self-contained and require no external components or adjustments. The AD684 is manufactured on a BiMOS process which provides a merger of high performance bipolar circuitry and low power CMOS logic.

The AD684 is ideal for high performance, multichannel data acquisition systems. Each SHA channel can acquire a signal in less than 1μs and retain the held value with a droop rate of less than 0.01μV/μs. Excellent linearity and ac performance make the AD684 an ideal front end for high speed 12- and 14-bit ADCs.

The AD684 has a self-correcting architecture that minimizes hold mode errors and insures accuracy over temperature. Each channel of the AD684 is capable of sourcing 5mA and incorporates output short circuit protection.

The AD684 is specified for three temperature ranges. The J grade device is specified for operation from 0 to 70°C, the A grade from −40°C to +85°C and the S grade from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Fast acquisition time (1μs) and low aperture jitter (75ps) make the AD684 the best choice for multiple channel data acquisition systems.
2. Monolithic construction insures excellent interchannel matching in terms of timing and accuracy, as well as high reliability.
3. Independent inputs, outputs and sample-and-hold controls allow user flexibility in system architecture.
4. Low droop (0.01μV/μs) and internally compensated hold mode error results in superior system accuracy.
5. The AD684's fast settling time and low output impedance make it ideal for driving high speed analog to digital converters such as the AD578, AD674, AD7572 and the AD7672.
6. The AD684 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD684/883B data sheet for detailed specifications.

***Protected by U.S. Patent Number 4,962,325.**

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Acquisition Time										
10V Step to 0.01%		0.75	1.0		0.75	1.0		0.75	1.0	µs
10V Step to 0.1%		0.5	0.6		0.5	0.6		0.5	0.6	µs
Small Signal Bandwidth		4			4			4		MHz
Full Power Bandwidth		1			1			1		MHz
HOLD CHARACTERISTICS										
Effective Aperture Delay	−35	−25	−15	−35	−25	−15	−35	−25	−15	ns
Aperture Jitter		50	75		50	75		50	75	ps
Hold Settling Time (to 1mV)		250	500		250	500		250	500	ns
Droop Rate[1]		0.01	**1**		0.01	**1**		0.01	**1**	µV/µs
Feedthrough										
(V_{IN} = ±5V, 100kHz)		−90			−90			−90		dB
ACCURACY CHARACTERISTICS[1]										
Hold Mode Offset	**−4**	−1	**+3**	**−4**	−1	**+3**	**−4**	−1	**+3**	mV
Hold Mode Offset Drift		10			10			10		µV/°C
Sample Mode Offset		50	**200**		50	**200**		50	**200**	mV
Nonlinearity		±0.002	±0.003		±0.002	±0.003		±0.003	±0.005	% FS
Gain Error		±0.03	**±0.05**		±0.03	**±0.05**		±0.03	**±0.05**	% FS
INTERCHANNEL CHARACTERISTICS										
Interchannel Isolation										
(V_{IN} = ±5V, 100kHz)	80	86		80	86		80	86		dB
Interchannel Aperture Offset		150	300		150	300		150	300	ps
Interchannel Offset		0.4	**1.5**		0.4	**2.0**		0.4	**2.0**	mV
OUTPUT CHARACTERISTICS										
Output Drive Current[2]	**−5**		**+5**	**−5**		**+5**	**−5**		**+5**	mA
Output Resistance, dc		0.3	0.5		0.3	0.5		0.3	0.5	Ω
Total Output Noise										
(dc to 5MHz)		150			150			150		µV rms
Sampled dc Uncertainty		85			85			85		µV rms
Hold Mode Noise										
(dc to 5MHz)		125			125			125		µV rms
Short Circuit Current[3]										
Source		20			20			20		mA
Sink		10			10			10		mA
INPUT CHARACTERISTICS										
Input Voltage Range	−5		+5	−5		+5	−5		+5	V
Bias Current[4]		100	**250**		100	**250**		100	**250**	nA
			400			500			500	nA
Input Impedance		50			50			50		MΩ
Input Capacitance		2			2			2		pF
DIGITAL CHARACTERISTICS										
Input Voltage Low			**0.8**			**0.8**			**0.8**	V
Input Voltage High	**2.0**			**2.0**			**2.0**			V
Input Current (V_{IN} = 5V)		2	**10**		2	**10**		2	**10**	µA
POWER SUPPLY CHARACTERISTICS										
Operating Voltage Range (V_{CC}, V_{EE})	±10.8	±12	±13.2	±10.8	±12	±13.2	±10.8	±12	±13.2	V
Supply Current		18	**25**		18	**25**		18	**26**	mA
+ PSRR	**65**	70		**65**	70		**65**	70		dB
−PSRR	**60**	65		**60**	65		**60**	65		dB
Power Consumption		430	600		430	600		430	625	mW
TEMPERATURE RANGE										
Specified Performance	0		+70	−40		+85	−55		+125	°C
PACKAGE OPTIONS										
16-Pin Cerdip (Q)		AD684JQ			AD684AQ			AD684SQ		

NOTES

[1]Specified and tested over an input range of ±5V.

[2]Maximum current the AD684 can source (or sink). Testing guarantees that the accuracy of the held signal remains within 2.5mV of its initial value.

[3]The output is protected for a short circuit to common, V_{CC} and V_{EE}.

[4]V_{CC} and V_{EE} at nominal voltage levels.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

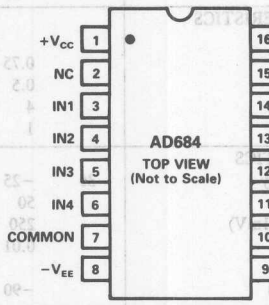
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Spec	With Respect to	Min	Max	Unit
V_{CC}	Common	−0.3	+15	V
V_{EE}	Common	−15	+0.3	V
Control Inputs	Common	−0.5	+7	V
Analog Inputs	Common	−12	+12	V
Output Short Circuit to Ground, V_{CC}, or V_{EE}		Indefinite		
Max Junction Temperature			+175	°C
Storage		−65	+150	°C
Lead Temperature (10sec max)			+300	°C
Power Dissipation			640	mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

PIN CONFIGURATION



NC = NO CONNECT

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD684JQ	0 to +70°C	Q-16
AD684AQ	−40°C to +85°C	Q-16
AD684SQ	−55°C to +125°C	Q-16

NOTES

[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD684/883B data sheet.

[2]Q = Cerdip. For outline information see Package Information section.

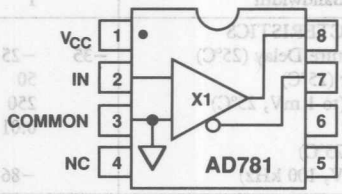
Complete 700 ns Sample-and-Hold Amplifier

AD781*

FEATURES

Acquisition Time to 0.01%: 700 ns Maximum
Low Power Dissipation: 95 mW
Low Droop Rate: 0.01 μV/μs
Fully Specified and Tested Hold Mode Distortion
Total Harmonic Distortion: −80 dB Maximum
Aperture Jitter: 75 ps Maximum
Internal Hold Capacitor
Self-Correcting Architecture
8-Pin Mini Cerdip and Plastic Package
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD781 is a high speed monolithic sample-and-hold amplifier (SHA). The AD781 guarantees a maximum acquisition time of 700 ns to 0.01% over temperature. The AD781 is specified and tested for hold mode total harmonic distortion and hold mode signal-to-noise and distortion. The AD781 is configured as a unity gain amplifier and uses a self-correcting architecture that minimizes hold mode errors and insures accuracy over temperature. The AD781 is self-contained and requires no external components or adjustments.

The low power dissipation, 8-pin mini-DIP package and completeness make the AD781 ideal for highly compact board layouts. The AD781 will acquire a full-scale input in less than 700 ns and retain the held value with a droop rate of 0.01 μV/μs. Excellent linearity and hold mode dc and dynamic performance make the AD781 ideal for 12- and 14-bit high speed analog-to-digital converters.

The AD781 is manufactured on Analog Devices' BiMOS process which merges high performance, low noise bipolar circuitry with low power CMOS to provide an accurate, high speed, low power SHA.

The AD781 is specified for three temperature ranges. The J grade device is specified for operation from 0°C to 70°C, the A grade from −40°C to +85°C and the S grade from −55°C to +125°C. The J and A grades are available in 8-pin plastic DIP packages. The S grade is available in an 8-pin cerdip package.

***Protected by U.S. Patent No. 4,962,325.**

PRODUCT HIGHLIGHTS

1. Fast acquisition time (700 ns), low aperture jitter (75 ps) and fully specified hold mode distortion make the AD781 an ideal SHA for sampling systems.
2. Low droop (0.01 μV/μs) and internally compensated hold mode error results in superior system accuracy.
3. Low power (95 mW typical), complete functionality and small size make the AD781 an ideal choice for a variety of high performance, low power applications.
4. The AD781 requires no external components or adjustments.
5. Excellent choice as a front-end SHA for high speed analog-to-digital converters such as the AD671, AD7586, AD674B, AD774B, AD7572 and AD7672.
6. Fully specified and tested hold mode distortion guarantees the performance of the SHA in sampled data systems.
7. The AD781 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD781/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD781—SPECIFICATIONS

DC SPECIFICATIONS (T_{min} to T_{max} with V_{CC} = +12 V ± 10%, V_{EE} = −12 V ± 10%, C_L = 20 pF, unless otherwise specified)

Parameter	AD781J Min	AD781J Typ	AD781J Max	AD781A Min	AD781A Typ	AD781A Max	AD781S Min	AD781S Typ	AD781S Max	Units
SAMPLING CHARACTERISTICS										
Acquisition Time										
10 V Step to 0.01%		600	700		600	700		600	700	ns
10 V Step to 0.1%		500	600		500	600		500	600	ns
Small Signal Bandwidth		4			4			4		MHz
Full Power Bandwidth		1			1			1		MHz
HOLD CHARACTERISTICS										
Effective Aperture Delay (25°C)	**−35**	−25	**−15**	**−35**	−25	**−15**	**−35**	−25	**−15**	ns
Aperture Jitter (25°C)		50	75		50	75		50	75	ps
Hold Settling (to 1 mV, 25°C)		250	**500**		250	**500**		250	**500**	ns
Droop Rate		0.01	**1**		0.01	**1**		0.01	**1**	μV/μs
Feedthrough (25°C)										
(V_{IN} = ±5 V, 100 kHz)		−86			−86			−86		dB
ACCURACY CHARACTERISTICS[1]										
Hold Mode Offset	**−4**	−1	**+3**	**−4**	−1	**+3**	**−4**	−1	**+3**	mV
Hold Mode Offset Drift		10			10			10		μV/°C
Sample Mode Offset		50	**200**		50	**200**		50	**200**	mV
Nonlinearity		±0.002	±0.003		±0.002	±0.003		±0.003	±0.005	% FS
Gain Error		±0.01	**±0.025**		±0.01	**±0.025**		±0.01	**±0.025**	% FS
OUTPUT CHARACTERISTICS										
Output Drive Current	**−5**		**+5**	**−5**		**+5**	**−5**		**+5**	mA
Output Resistance, DC		0.3	**0.5**		0.3	**0.5**		0.3	**0.5**	Ω
Total Output Noise (DC to 5 MHz)		150			150			150		μV rms
Sampled DC Uncertainty		85			85			85		μV rms
Hold Mode Noise (DC to 5 MHz)		125			125			125		μV rms
Short Circuit Current										
Source		20			20			20		mA
Sink		10			10			10		mA
INPUT CHARACTERISTICS										
Input Voltage Range	−5		+5	−5		+5	−5		+5	V
Bias Current		50	**250**		50	**250**		50	**250**	nA
Input Impedance		50			50			50		MΩ
Input Capacitance		2			2			2		pF
DIGITAL CHARACTERISTICS										
Input Voltage Low			**0.8**			**0.8**			**0.8**	V
Input Voltage High	**2.0**			**2.0**			**2.0**			V
Input Current High (V_{IN} = 5 V)		2	**10**		2	**10**		2	**10**	μA
POWER SUPPLY CHARACTERISTICS										
Operating Voltage Range	±10.8	±12	±13.2	±10.8	±12	±13.2	±10.8	±12	±13.2	V
Supply Current		4	**6.5**		4	**6.5**		4	7	mA
+PSRR (+12 V ± 10%)	**70**	80		**70**	80		**70**	80		dB
−PSRR (−12 V ± 10%)	**65**	75		**65**	75		**65**	75		dB
Power Consumption		95	175		95	175		95	185	mW
TEMPERATURE RANGE										
Specified Performance	0		+70	−40		+85	−55		+125	°C

NOTE

[1]Specified and tested over an input range of ±5 V.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested.

HOLD MODE AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±10%, V_{EE} = −12 V ±10%, C_L = 20 pF, unless otherwise specified)[1]

Parameter	AD781J Min	AD781J Typ	AD781J Max	AD781A Min	AD781A Typ	AD781A Max	AD781S Min	AD781S Typ	AD781S Max	Units
TOTAL HARMONIC DISTORTION										
F_{IN} = 10 kHz		−90	**−80**		−90	**−80**		−90	**−80**	dB
F_{IN} = 50 kHz		−73			−73			−73		dB
F_{IN} = 100 kHz		−68			−68			−68		dB
SIGNAL-TO-NOISE AND DISTORTION										
F_{IN} = 10 kHz	**72**	78		**72**	78		72	78		dB
F_{IN} = 50 kHz		73			73			73		dB
F_{IN} = 100 kHz		67			67			67		dB
INTERMODULATION DISTORTION										
F_{IN1} = 49 kHz, F_{IN2} = 50 kHz										
2nd Order Products		−77			−77			−77		dB
3rd Order Products		−78			−78			−78		dB

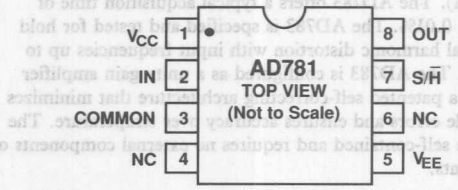
NOTE
[1]F_{IN} amplitude = 0 dB and F_{SAMPLE} = 500 kHz unless otherwise indicated.
Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested.

ABSOLUTE MAXIMUM RATINGS*

Spec	With Respect to	Min	Max	Unit
V_{CC}	Common	−0.3	+15	V
V_{EE}	Common	−15	+0.3	V
Control Input	Common	−0.5	+7	V
Analog Input	Common	−12	+12	V
Output Short Circuit to Ground, V_{CC}, or V_{EE}		Indefinite		
Maximum Junction Temperature			+175	°C
Storage		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C
Power Dissipation			195	mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

PIN CONFIGURATION



ORDERING GUIDE

Model[1]	Temperature Range	Description	Package Options[2]
AD781JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD781AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD781SQ	−55°C to +125°C	8-Pin Cerdip	Q-8

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD781/883B data sheet.
[2]N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.

CAUTION

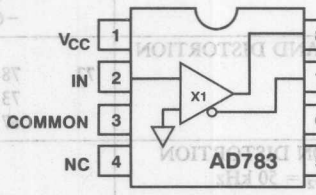
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.

Complete Very High Speed Sample-and-Hold Amplifier

AD783*

FEATURES
- Acquisition Time to 0.01%: 250 ns Typical
- Low Power Dissipation: 95 mW
- Low Droop Rate: 0.02 μV/μs
- Fully Specified and Tested Hold Mode Distortion
- Total Harmonic Distortion: −85 dB
- Aperture Jitter: 50 ps Maximum
- Internal Hold Capacitor
- Self-Correcting Architecture
- 8-Pin Mini Cerdip and SOIC Packages

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD783 is a high speed, monolithic sample-and-hold amplifier (SHA). The AD783 offers a typical acquisition time of 250 ns to 0.01%. The AD783 is specified and tested for hold mode total harmonic distortion with input frequencies up to 100 kHz. The AD783 is configured as a unity gain amplifier and uses a patented self-correcting architecture that minimizes hold mode errors and ensures accuracy over temperature. The AD783 is self-contained and requires no external components or adjustments.

The AD783 retains the held value with a droop rate of 0.02 μV/μs. Excellent linearity and hold mode dc and dynamic performance make the AD783 ideal for high speed 12- and 14-bit analog-to-digital converters.

The AD783 is manufactured on Analog Devices' ABCMOS process which merges high performance, low noise bipolar circuitry with low power CMOS to provide an accurate, high speed, low power SHA.

The J grade device is specified for operation from 0°C to +70°C and the A grade from −40°C to +85°C. The J and A grades are available in 8-pin cerdip and SOIC packages. The military temperature range version is specified for operation from −55°C to +125°C and is available in an 8-pin cerdip package. For details refer to the *Analog Devices Military Products Databook* or AD783/883B data sheet.

PRODUCT HIGHLIGHTS

1. Fast acquisition time (250 ns), low aperture jitter (20 ps) and fully specified hold mode distortion make the AD783 an ideal SHA for sampling systems.
2. Low droop (0.02 μV/μs) and internally compensated hold mode error result in superior system accuracy.
3. Low power (95 mW typical), complete functionality and small size make the AD783 an ideal choice for a variety of high performance applications.
4. The AD783 requires no external components or adjustments.
5. The AD783 is an excellent choice as a front-end SHA for high speed analog-to-digital converters such as the AD671, AD7586, AD674B, AD774B, AD7572 and AD7672.
6. Fully specified and tested hold mode distortion guarantees the performance of the SHA in sampled data systems.

*Protected by U.S. Patent Number 4,962,325.

SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{EE} = −5 V ± 5%, C_L = 50 pF, unless otherwise noted)

Parameter	AD783J/A Min	Typ	Max	Units
SAMPLING CHARACTERISTICS				
Acquisition Time				
5 V Step to 0.01%		250	375	ns
5 V Step to 0.1%		200	350	ns
Small Signal Bandwidth		15		MHz
Full Power Bandwidth		2		MHz
HOLD CHARACTERISTICS				
Effective Aperture Delay (+25°C)	−30	15	30	ns
Aperture Jitter (+25°C)		20	50	ps
Hold Settling (to 1 mV, +25°C)		150	200	ns
Droop Rate		0.02	1	μV/μs
Feedthrough (+25°C)				
(V_{IN} = ±2.5 V, 500 kHz)		−80		dB
ACCURACY CHARACTERISTICS[1]				
Hold Mode Offset	−5	0	+5	mV
Hold Mode Offset Drift		10		μV/°C
Sample Mode Offset		50	200	mV
Nonlinearity		±0.005		% FS
Gain Error		±0.03	±0.1	% FS
OUTPUT CHARACTERISTICS				
Output Drive Current	−5		+5	mA
Output Resistance, DC		0.3	0.6	Ω
Total Output Noise (DC to 5 MHz)		150		μV rms
Sampled DC Uncertainty		85		μV rms
Hold Mode Noise (DC to 5 MHz)		125		μV rms
Short Circuit Current				
Source			20	mA
Sink			13	mA
INPUT CHARACTERISTICS				
Input Voltage Range	−2.5		+2.5	V
Bias Current		100	250	nA
Input Impedance		10		MΩ
Input Capacitance		2		pF
DIGITAL CHARACTERISTICS				
Input Voltage Low			0.8	V
Input Voltage High	2.0			V
Input Current High (V_{IN} = 5 V)		2	10	μA
POWER SUPPLY CHARACTERISTICS				
Operating Voltage Range	±4.75	±5	±5.25	V
Supply Current		9.5	17	mA
+PSRR (+5 V ± 5%)	45	65		dB
−PSRR (−5 V ± 5%)	45	65		dB
Power Consumption		95	175	mW
TEMPERATURE RANGE				
Specified Performance (J)	0		+70	°C
(A)	−40		+85	°C

NOTE
[1]Specified and tested over an input range of ±2.5 V.
Specifications subject to change without notice.

Parameter	AD783J/A Min	Typ	Max	Units
TOTAL HARMONIC DISTORTION				
f_{IN} = 100 kHz		−85	−80	dB
f_{IN} = 500 kHz		−72		dB
SIGNAL-TO-NOISE AND DISTORTION				
f_{IN} = 100 kHz		77		dB
f_{IN} = 500 kHz		70		dB
INTERMODULATION DISTORTION				
(F1 = 99 kHz, F2 = 100 kHz)				
Second Order Products		−80		dB
Third Order Products		−85		dB

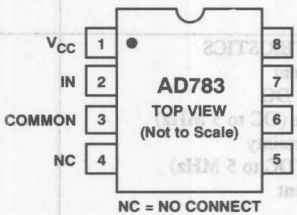
NOTE
[1]f_{IN} amplitude = 0 dB and f_{SAMPLE} = 300 kHz unless otherwise indicated.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Spec	With Respect to	Min	Max	Units
V_{CC}	COM	−0.5	+6.5	V
V_{EE}	COM	−6.5	+0.5	V
Analog Input	COM	−6.5	+6.5	V
Digital Input	COM	−0.5	+6.5	V
Output Short Circuit to Ground, V_{CC}, or V_{EE}		Indefinite		
Maximum Junction Temperature			+175	°C
Storage		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

PIN CONFIGURATION



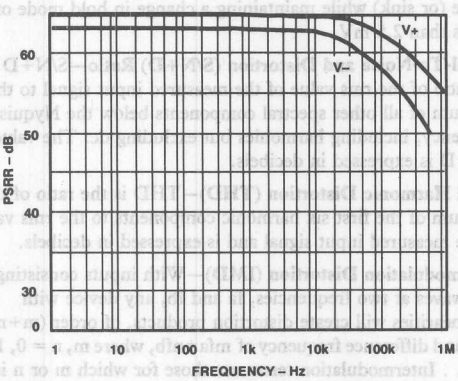
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.

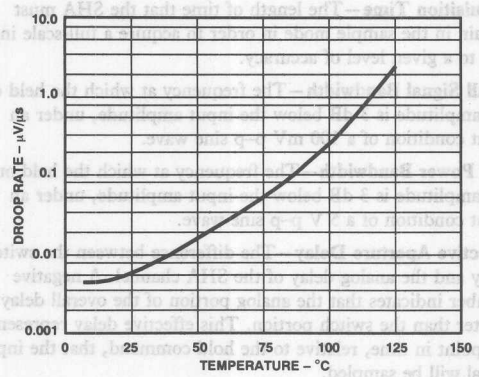
ORDERING GUIDE

Model[1]	Temperature Range	Description	Package Options[2]
AD783JQ	0°C to +70°C	8-Pin Cerdip	Q-8
AD783AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD783JR	0°C to +70°C	8-Pin SOIC	R-8
AD783AR	−40°C to +85°C	8-Pin SOIC	R-8

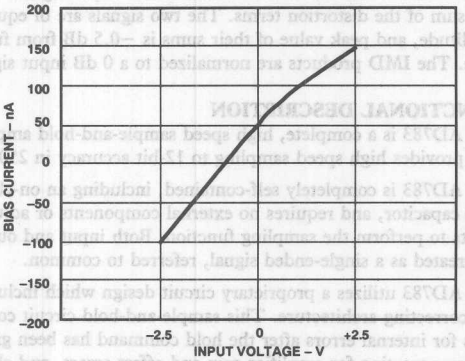
NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD783/883B data sheet.
[2]Q = Cerdip, R = SOIC. For outline information see Package Information section.



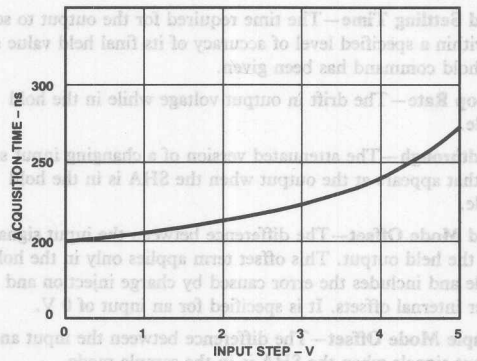
Power Supply Rejection Ratio vs. Frequency



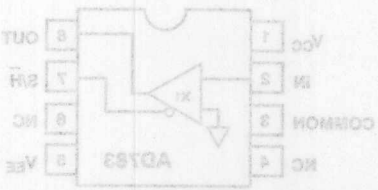
Droop Rate vs. Temperature, V_{IN} = 0 V



Bias Current vs. Input Voltage



Acquisition Time (to 0.01%) vs. Input Step Size



6

DEFINITIONS OF SPECIFICATIONS

Acquisition Time—The length of time that the SHA must remain in the sample mode in order to acquire a full-scale input step to a given level of accuracy.

Small Signal Bandwidth—The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 100 mV p–p sine wave.

Full Power Bandwidth—The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 5 V p–p sine wave.

Effective Aperture Delay—The difference between the switch delay and the analog delay of the SHA channel. A negative number indicates that the analog portion of the overall delay is greater than the switch portion. This effective delay represents the point in time, relative to the hold command, that the input signal will be sampled.

Aperture Jitter—The variations in aperture delay for successive samples. Aperture jitter puts an upper limit on the maximum frequency that can be accurately sampled.

Hold Settling Time—The time required for the output to settle to within a specified level of accuracy of its final held value after the hold command has been given.

Droop Rate—The drift in output voltage while in the hold mode.

Feedthrough—The attenuated version of a changing input signal that appears at the output when the SHA is in the hold mode.

Hold Mode Offset—The difference between the input signal and the held output. This offset term applies only in the hold mode and includes the error caused by charge injection and all other internal offsets. It is specified for an input of 0 V.

Sample Mode Offset—The difference between the input and output signals when the SHA is in the sample mode.

Nonlinearity—The deviation from a straight line on a plot of input vs. (held) output as referenced to a straight line drawn between endpoints, over an input range of −2.5 V and +2.5 V.

Gain Error—Deviation from a gain of +1 on the transfer function of input vs. held output.

Power Supply Rejection Ratio—A measure of change in the held output voltage for a specified change in the positive or negative supply.

Sampled DC Uncertainty—The internal rms SHA noise that is sampled onto the hold capacitor.

Hold Mode Noise—The rms noise at the output of the SHA while in the hold mode, specified over a given bandwidth.

Total Output Noise—The total rms noise that is seen at the output of the SHA while in the hold mode. It is the rms summation of the sampled dc uncertainty and the hold mode noise.

Output Drive Current—The maximum current the SHA can source (or sink) while maintaining a change in hold mode offset of less than 2.5 mV.

Signal-To-Noise and Distortion (S/N+D) Ratio—S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Total Harmonic Distortion (THD)—THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed in decibels.

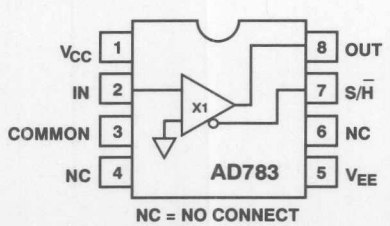
Intermodulation Distortion (IMD)—With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequency of mfa±nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa+fb) and (fa−fb), and the third order terms are (2fa+fb), (2fa−fb), (fa+2fb) and (fa−2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude, and peak value of their sums is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

FUNCTIONAL DESCRIPTION

The AD783 is a complete, high speed sample-and-hold amplifier that provides high speed sampling to 12-bit accuracy in 250 ns.

The AD783 is completely self-contained, including an on-chip hold capacitor, and requires no external components or adjustments to perform the sampling function. Both input and output are treated as a single-ended signal, referred to common.

The AD783 utilizes a proprietary circuit design which includes a self-correcting architecture. This sample-and-hold circuit corrects for internal errors after the hold command has been given, by compensating for amplifier gain and offset errors, and charge injection errors. Due to the nature of the design, the SHA output in the sample mode is not intended to provide an accurate representation of the input. However, in hold mode, the internal circuitry is reconfigured to produce an accurately held version of the input signal. Below is a block diagram of the AD783.



Functional Block Diagram

DYNAMIC PERFORMANCE

The AD783 is compatible with 12-bit A-to-D converters in terms of both accuracy and speed. The fast acquisition time, fast hold settling time and good output drive capability allow the AD783 to be used with high speed, high resolution A-to-D converters like the AD671 and AD7586. The AD783's fast acquisition time provides high throughput rates for multichannel data acquisition systems. Typically, the AD783 can acquire a 5 V step in less than 250 ns. Figure 1 shows the settling accuracy as a function of acquisition time.

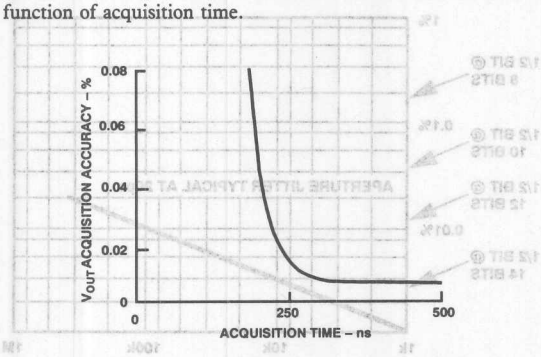


Figure 1. V_{OUT} Settling vs. Acquisition Time

The hold settling determines the required time, after the hold command is given, for the output to settle to its final specified accuracy. The typical settling behavior of the AD783 is 150 ns. The settling time of the AD783 is sufficiently fast to allow the SHA, in most cases, to directly drive an A-to-D converter without the need for an added "start convert" delay.

HOLD MODE OFFSET

The dc accuracy of the AD783 is determined primarily by the hold mode offset. The hold mode offset refers to the difference between the final held output voltage and the input signal at the time the hold command is given. The hold mode offset arises from a voltage error introduced onto the hold capacitor by charge injection of the internal switches. The nominal hold mode offset is specified for a 0 V input condition. Over the input range of −2.5 V to +2.5 V, the AD783 is also characterized for an effective gain error and nonlinearity of the held value, as shown in Figure 2. As indicated by the AD783 specifications, the hold mode offset is very stable over temperature.

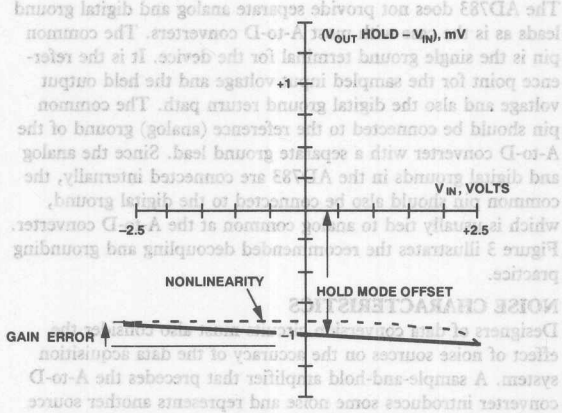


Figure 2. Hold Mode Offset, Gain Error and Nonlinearity

For applications where it is important to obtain zero offset, the hold mode offset may be nulled externally at the input to the A-to-D converter. Adjustment of the offset may be accomplished through the A-to-D itself or by an external amplifier with offset nulling capability (e.g., AD711). The offset will change less than 0.5 mV over the specified temperature range.

SUPPLY DECOUPLING AND GROUNDING CONSIDERATIONS

As with any high speed, high resolution data acquisition system, the power supplies should be well regulated and free from excessive high frequency noise (ripple). The supply connection to the AD783 should also be capable of delivering transient currents to the device. To achieve the specified accuracy and dynamic performance, decoupling capacitors must be placed directly at both the positive and negative supply pins to common. Ceramic type 0.1 μF capacitors should be connected from V_{CC} and V_{EE} to common.

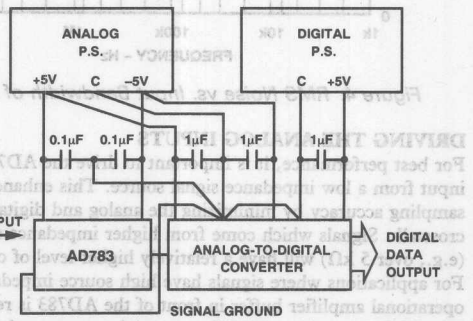


Figure 3. Basic Grounding and Decoupling Diagram

The AD783 does not provide separate analog and digital ground leads as is the case with most A-to-D converters. The common pin is the single ground terminal for the device. It is the reference point for the sampled input voltage and the held output voltage and also the digital ground return path. The common pin should be connected to the reference (analog) ground of the A-to-D converter with a separate ground lead. Since the analog and digital grounds in the AD783 are connected internally, the common pin should also be connected to the digital ground, which is usually tied to analog common at the A-to-D converter. Figure 3 illustrates the recommended decoupling and grounding practice.

NOISE CHARACTERISTICS

Designers of data conversion circuits must also consider the effect of noise sources on the accuracy of the data acquisition system. A sample-and-hold amplifier that precedes the A-to-D converter introduces some noise and represents another source of uncertainty in the conversion process. The noise from the AD783 is specified as the total output noise, which includes both the sampled wideband noise of the SHA in addition to the band limited output noise. The total output noise is the rms sum of the sampled dc uncertainty and the hold mode noise. A plot of the total output noise vs. the equivalent input bandwidth of the converter being used is given in Figure 4.

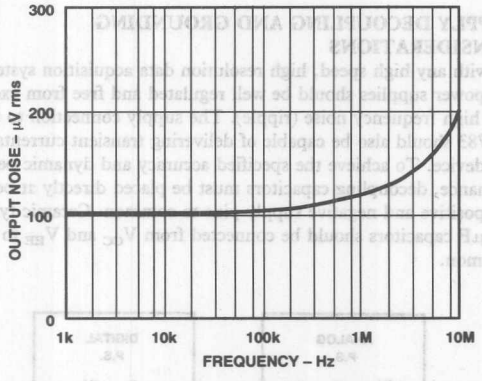


Figure 4. RMS Noise vs. Input Bandwidth of ADC

DRIVING THE ANALOG INPUTS

For best performance, it is important to drive the AD783 analog input from a low impedance signal source. This enhances the sampling accuracy by minimizing the analog and digital crosstalk. Signals which come from higher impedance sources (e.g., over 5 kΩ) will have a relatively higher level of crosstalk. For applications where signals have high source impedance, an operational amplifier buffer in front of the AD783 is required. The AD711 (precision BiFET op amp) is recommended for these applications.

HIGH FREQUENCY SAMPLING

Aperture jitter and distortion are the primary factors which limit frequency domain performance of a sample-and-hold amplifier. Aperture jitter modulates the phase of the hold command and produces an effective noise on the sampled analog input. The magnitude of the jitter induced noise is directly related to the frequency of the input signal.

A graph showing the magnitude of the jitter induced error vs. frequency of the input signal is given in Figure 5.

The accuracy in sampling high frequency signals is also constrained by the distortion and noise created by the sample-and-hold. The level of distortion increases with frequency and reduces the "effective number of bits" of the conversion.

Measurements of Figures 6 and 7 were made using a 14-bit A/D converter with V_{IN} = 5 V p–p and a sample frequency of 100 ksps.

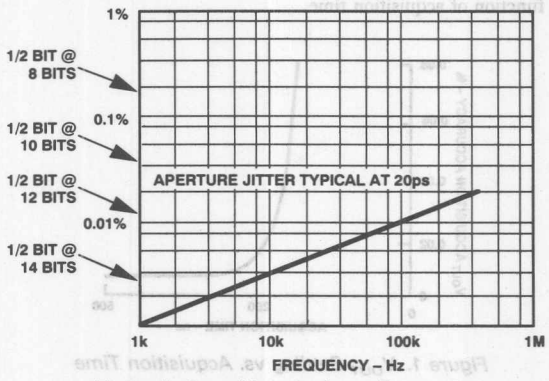


Figure 5. Error Magnitude vs. Frequency

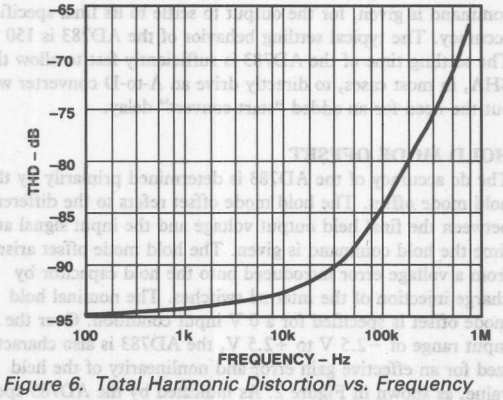


Figure 6. Total Harmonic Distortion vs. Frequency

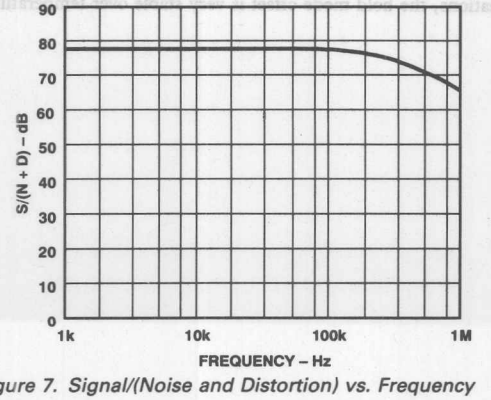


Figure 7. Signal/(Noise and Distortion) vs. Frequency

AD783 TO AD670 INTERFACE

The 15 MHz small signal bandwidth of the AD783 makes it a good choice for undersampling applications. Figure 8 shows the interface between the AD783 and the AD670 ADC, where the AD783 samples the incoming IF signal. For this particular application, the IF carrier was 10.7 MHz and the information signal was a 5 kHz FSK-modulated tone. The sample-and-hold signal is applied to the 8-bit AD670 ADC and then digitally processed for analysis.

The CLKIN signal is connected directly to the S/H pin of the AD783 and must comply with the acquisition and settling requirements of the SHA. A delayed version of CLKIN is applied to the R/$\overline{W}$ input of the AD670 in order to accommodate the hold-mode settling requirements of the AD783. The 10 µs conversion speed of the AD670 combined with the 150 ns hold-mode settling time of the AD783 result in a total system throughput of 10.15 µs.

By keeping the 10.7 MHz IF input to the AD783 at a low amplitude, 255 mV p-p, the resultant distortion and jitter-induced noise result in approximately 45 dB of dynamic range. The AD670 can be conveniently configured such that its full-scale input range is 255 mV in order to retain the full 8-bit dynamic range of the converter. The maximum sample rate of the AD670 is 10 µs; therefore, to comply with the Nyquist criteria the maximum information bandwidth is 50 kHz.

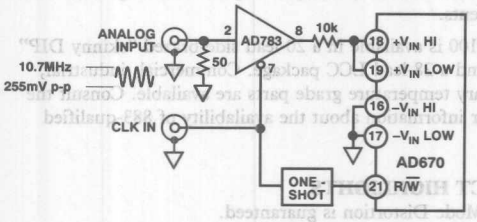


Figure 8. AD783 to AD670 Interface

AD783 to AD671 (12-Bit, 500 ns ADC) Interface

The AD783 to AD671 interface requires an op amp, a dual flip-flop, and a monostable multivibrator or "one-shot." The op amp amplifies the ±2.5 V output of the AD783 to the full-scale input of the AD671. Appropriate op amps include the AD841 and AD845 (see the AD671 data sheet for additional information). The flip-flops and one-shot are used to generate the AD671 ENCODE pulse and the appropriately timed AD783 S/H pulse.

A master sampling clock is tied to the clock input of flip-flop1 and the input of the one-shot. The D1 input of flip-flop1 should be tied high and the one-shot should be configured to generate a pulse on a rising edge of the sampling clock. The rising edge of the sampling clock causes the $\overline{Q1}$ output of the flip-flop to go low placing the AD783 into hold mode. Simultaneously, a low going pulse is generated at the one-shot output. The length of this pulse would usually be made long enough to allow the output of the AD783 to settle (hold-mode settling time), but because of the error-correcting ability of the AD671, the length of this pulse may be reduced to approximately 200 ns.

The low-going one-shot output is connected to the clock input of flip-flop2. The D2 input of flip-flop2 is tied high. The rising edge of the low-going pulse toggles the Q2 output of flip-flop2 to a high state. This output, which is tied to the ENCODE input of the AD671, initiates a conversion of the buffered output signal of the AD783. The AD671 issues the signal DAV when the conversion is complete. The DAV signal is tied to the asynchronous $\overline{CLR1}$ and $\overline{CLR2}$ inputs of both flip-flops. When DAV goes low, the $\overline{Q1}$ output goes high returning the AD783 to the sample or acquisition mode. The Q2 output (ENCODE) returns low until it is again triggered by the rising edge of the one-shot output.

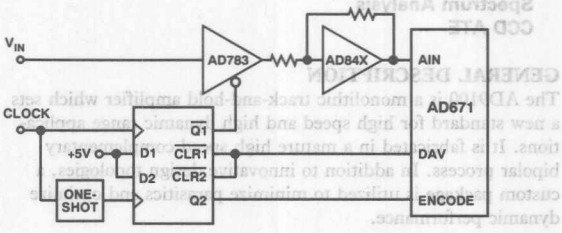


Figure 9. AD783 to AD671 Interface

AD9100*

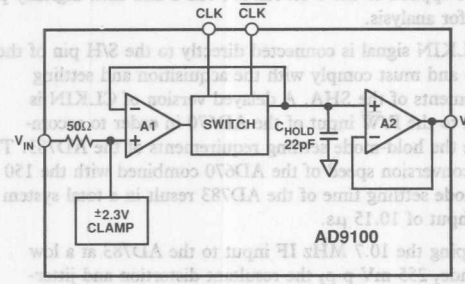
FEATURES

Excellent Hold Mode Distortion into 250 Ω
−88 dB @ 30 MSPS (2.3 MHz V_{IN})
−83 dB @ 30 MSPS (12.1 MHz V_{IN})
−74 dB @ 30 MSPS (19.7 MHz V_{IN})
16 ns Acquisition Time to 0.01%
<1 ps Aperture Jitter
250 MHz Tracking Bandwidth
83 dB Feedthrough Rejection @ 20 MHz
3.3 nV/√Hz Spectral Noise Density
MIL-STD-Compliant Versions Available

APPLICATIONS

A/D Conversion
Direct IF Sampling
Imaging/FLIR Systems
Peak Detectors
Radar/EW/ECM
Spectrum Analysis
CCD ATE

BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9100 is a monolithic track-and-hold amplifier which sets a new standard for high speed and high dynamic range applications. It is fabricated in a mature high speed complementary bipolar process. In addition to innovative design topologies, a custom package is utilized to minimize parasitics and optimize dynamic performance.

Acquisition time (hold to track) is 13 ns to 0.1% accuracy, and 16 ns to 0.01%. The AD9100 boasts superlative hold-mode frequency domain performance; when sampling at 30 MSPS hold mode distortion is less than −83 dBfs for analog frequencies up to 12 MHz; and −74 dBfs at 20 MHz. The AD9100 can also drive capacitive loads up to 100 pF with little degradation in acquisition time; it is therefore well suited to drive 8- and 10-bit flash converters at clock speeds to 50 MSPS. With a spectral noise density of 3.3 nV/√Hz and feedthrough rejection of 83 dB at 20 MHz, the AD9100 is well suited to enhance the dynamic range of many 8- to 16-bit systems.

The AD9100 is "user friendly" and easy to apply: (1) it requires +5 V/−5.2 V power supplies; (2) the hold capacitor and switch power supply decoupling capacitors are built into the DIP package; (3) the encode clock is differential ECL to minimize clock jitter; (4) the input resistance is typically 800 kΩ; (5) the analog input is internally clamped to prevent damage from voltage transients.

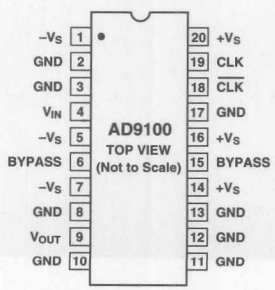
The AD9100 is available in a 20-lead side-brazed "skinny DIP" package and a 28-lead LCC package. Commercial, industrial, and military temperature grade parts are available. Consult the factory for information about the availability of 883-qualified devices.

PRODUCT HIGHLIGHTS

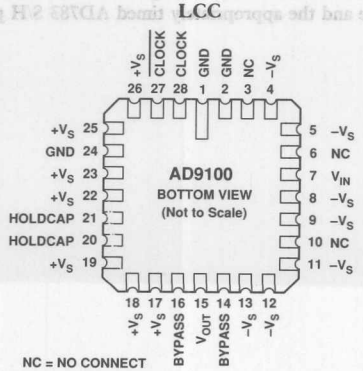
1. Hold Mode Distortion is guaranteed.
2. Monolithic construction.
3. Analog input is internally clamped to protect against overvoltage transients and ensure fast recovery.
4. Output is short circuit protected.
5. Drives capacitive loads to 100 pF.
6. Differential ECL clock inputs.

PIN DESIGNATIONS

DIP



LCC



NC = NO CONNECT

*Patent pending.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±6 V
Continuous Output Current . . . . . 70 mA
Analog Input Voltage[2] . . . . . ±5 V
Operating Temperature Range (Case)
AD9100JD . . . . . 0°C to +70°C
AD9100AD/AE . . . . . −25°C to +85°C
AD9100SD/SE . . . . . −55°C to +125°C
Junction Temperature . . . . . +175°C
Storage Temperature . . . . . −65°C to +150°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $+V_S = +5$ V; $-V_S = -5.2$ V; $R_{LOAD} = 100\ \Omega$; $R_{IN} = 50\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9100AE/SE/JD/AD/SD[3] Min	Typ	Max	Units
DC ACCURACY							
Gain	$\Delta V_{IN} = 2$ V	Full	VI	0.989	0.994		V/V
Offset	$V_{IN} = 0$ V	Full	VI	−5	±1	+5	mV
Output Resistance		25°C	V		0.4		Ω
Output Drive Capability		Full	VI	±40	±60		mA
PSRR	$\Delta V_S = 0.5$ V p–p	Full	VI	48	55		dB
Pedestal Sensitivity to Supply	$\Delta V_S = 0.5$ V p–p	Full	VI		0.9	3	mV/V
ANALOG INPUT/OUTPUT							
Output Voltage Range		Full	VI	+2	±2.2	−2	V
Input Bias Current		25°C	VI	−8	±3	+8	μA
		Full	VI	−16		+16	μA
Input Overdrive Current[4]	$V_{IN} = \pm 4$ V; $R_{IN} = 50\ \Omega$	25°C	V		±22		mA
Input Capacitance		25°C	V		1.2		pF
Input Resistance		25°C, T_{MAX}	VI	350	800		kΩ
		T_{MIN}	VI	200			kΩ
CLOCK/$\overline{\text{CLOCK}}$ INPUTS							
Input Bias Current	CL/$\overline{\text{CL}}$ = −1.0 V	Full	VI		4	5	mA
Input Low Voltage (V_{IL})		Full	VI	−1.8		−1.5	V
Input High Voltage (V_{IH})		Full	VI	−1.0		−0.8	V
TRACK MODE DYNAMICS							
Bandwidth (−3 dB)	$V_{OUT} \leq 0.4$ V p–p	Full	IV	150	250		MHz
Slew Rate	4 V Step	25°C	IV	550	850		V/μs
	4 V Step	Full	IV	500			V/μs
Overdrive Recovery Time[4] (to 0.1%)	$V_{IN} = \pm 4$ V to 0 V	25°C	V		21		ns
2nd Harm. Dist. (20 MHz, 2 V p–p)		Full	V		−65		dBc
3rd Harm. Dist. (20 MHz, 2 V p–p)		Full	V		−75		dBc
Integrated Output Noise (1–200 MHz)		25°C	V		45		μV
RMS Spectral Noise @ 10 MHz		25°C	V		3.3		nV/$\sqrt{\text{Hz}}$
HOLD MODE DYNAMICS							
Worst Harmonic (2.3 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	25°C	V		−83		dBfs
Worst Harmonic (12.1 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	25°C	IV		−80	−72	dBfs
Worst Harmonic (12.1 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	T_{MAX}	IV			−70	dBfs
Worst Harmonic (12.1 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	T_{MIN}	IV		−77	−68	dBfs
Worst Harmonic (19.7 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	25°C	V		−74		dBfs
Hold Noise[5]		25°C	V		300 × t_H		V/s rms
Droop Rate[6]	$V_{IN} = 0$ V	25°C	VI		1	6	±mV/μs
		T_{MIN}	VI		7	40	±mV/μs
		T_{MAX}	VI		5	30	±mV/μs
Feedthrough Rejection (20 MHz)	$V_{IN} = 2$ V p–p	Full	V		83		dB
TRACK-TO-HOLD SWITCHING							
Aperture Delay		25°C	V		+800		ps
Aperture Jitter		25°C	V		<1		ps
Pedestal Offset	$V_{IN} = 0$ V	25°C	VI	−5	±1	+5	mV
		Full	VI	−10		+10	mV
Transient Amplitude	$V_{IN} = 0$ V	Full	V		±6		mV
Settling Time to 1 mV		Full	IV		7	10	ns
Glitch Product	$V_{IN} = 0$ V	25°C	V		15		pV-s

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AD9100—SPECIFICATIONS

Parameter	Conditions	Temp	Test Level	AD9100AE/SE/JD/AD/SD[3] Min	Typ	Max	Units
HOLD-TO-TRACK SWITCHING							
Acquisition Time to 0.1%	2 V Step	25°C	V		13		ns
Acquisition Time to 0.01%	2 V Step	Full	IV		16	23	ns
Acquisition Time to 0.01%	4 V Step	25°C	V		20		ns
POWER SUPPLY							
Power Dissipation		Full	VI		1.05	1.25	W
$+V_S$ Current		Full	VI		96	118	mA
$-V_S$ Current		Full	VI		116	132	mA

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Analog input voltage should not exceed $\pm V_S$.

[3]AD9100JD: 0°C to +70°C. AD9100AD: −40°C to +85°C. AD9100SD: −55°C to +125°C. DIP θ_{JA} = 38°C/W; this is valid with the device mounted flush to a grounded 2 oz copper clad board with 16 sq inches of surface area and no air flow. LCC θ_{JA} = 48°C/W.

[4]The input to the AD9100 is internally clamped at ±2.3 V. The internal input series resistance is nominally 50 Ω.

[5]Hold mode noise is proportional to the length of time a signal is held. For example, if the hold time (t_H) is 20 ns, the accumulated noise is typically 6 μV (300 V/s × 20 ns). This value must be combined with the track mode noise to obtain total noise.

[6]Min and max droop rates are based on the military temperature range (−55°C to +125°C). Refer to the "Droop Rate vs Temperature" chart for min/max limits over the commercial and industrial ranges.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Periodically sample tested.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

DIP PIN DESCRIPTIONS/CONNECTIONS

Pin No.	Description	Connection
1	$-V_S$	−5.2 V Power Supply
2	GND	Common Ground Plane
3	GND	Common Ground Plane
4	V_{IN}	Analog Input Signal
5	$-V_S$	−5.2 V Power Supply
6	BYPASS	0.1 μF to Ground
7	$-V_S$	−5.2 V Power Supply
8	GND	Common Ground Plane
9	V_{OUT}	Track-and-Hold Output
10	GND	Common Ground Plane
11	GND	Common Ground Plane
12	GND	Common Ground Plane
13	GND	Common Ground Plane
14	$+V_S$	+5 V, Power Supply
15	BYPASS	0.1 μF to Ground
16	$+V_S$	+5 V, Power Supply
17	GND	Common Ground Plane
18	$\overline{CLK}$	Complement ECL Clock
19	CLK	"True" ECL Clock
20	$+V_S$	+5 V Power Supply

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD9100JD	0°C to +70°C	Ceramic DIP	D-28
AD9100AD	−40°C to +85°C	Ceramic DIP	D-28
AD9100AE	−40°C to +85°C	Ceramic LCC	E-28A
AD9100SD	−55°C to +125°C	Ceramic DIP	D-28
AD9100SE	−55°C to +125°C	Ceramic LCC	E-28A

NOTES

[1]Consult factory about availability of parts screened to MIL-STD-883.

[2]For outline information see Package Information section.

LCC PIN DESCRIPTIONS/CONNECTIONS

Pin No.	Description	Connection
1	GND	Common Ground Plane
2	GND	Common Ground Plane
3	NC	None
4	$-V_S$	−5.2 V Power Supply
5	$-V_S$	−5.2 V Power Supply
6	NC	None
7	V_{IN}	Analog Input Signal
8	$-V_S$	−5.2 V Power Supply
9	$-V_S$	−5.2 V Power Supply
10	NC	None
11	$-V_S$	−5.2 V Power Supply
12	$-V_S$	−5.2 V Power Supply
13	$-V_S$	−5.2 V Power Supply
14	BYPASS	0.1 μF to Pin 16
15	V_{OUT}	Track-and-Hold Output
16	BYPASS	0.1 μF to Pin 14
17	$+V_S$	+5 V Power Supply
18	$+V_S$	+5 V Power Supply
19	$+V_S$	+5 V Power Supply
20	HOLDCAP	External Hold Capacitor
21	HOLDCAP	External Hold Capacitor
22	$+V_S$	+5 V Power Supply
23	$+V_S$	+5 V Power Supply
24	GND	Common Ground Plane
25	$+V_S$	+5 V Power Supply
26	$+V_S$	+5 V Power Supply
27	CLOCK	Complement ECL Clock
28	$\overline{CLOCK}$	"True" ECL Clock

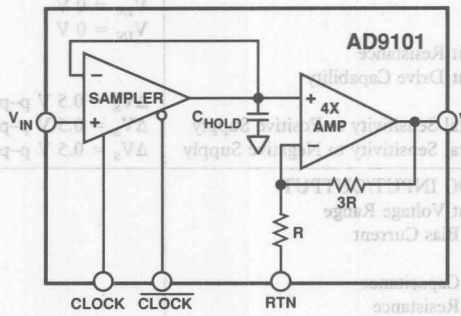
125 MSPS Monolithic Sampling Amplifier

AD9101

FEATURES
350 MHz Sampling Bandwidth
125 MHz Sampling Rate
Excellent Hold Mode Distortion
−75 dB @ 50 MSPS (25 MHz V_{IN})
−57 dB @ 125 MSPS (50 MHz V_{IN})
7 ns Acquisition Time to 0.1%
<1 ps Aperture Jitter
66 dB Feedthrough Rejection @ 50 MHz
3.3 nV/$\sqrt{Hz}$ Spectral Noise Density

APPLICATIONS
Direct IF Sampling
Digital Sampling Oscilloscopes
HDTV Cameras
Peak Detectors
Radar/EW/ECM
Spectrum Analysis
Test Equipment/CCD Testers
DDS DAC Deglitcher

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9101 is an extremely accurate, general purpose, high speed sampling amplifier. Its fast and accurate acquisition speed allows for a wide range of frequency vs. resolution performance. The AD9101 is capable of 8 to 12 bits of accuracy at clock rates of 125 MSPS or 50 MSPS, respectively. This level of performance makes it an ideal driver for almost all 8- to 12-bit A/D encoders on the market today.

In effect, the AD9101 is a track-and-hold with a post amplifier. This configuration allows the front end sampler to operate at relatively low signal amplitudes. This results in dramatic improvement in both track and hold mode distortion while keeping power low.

The gain-of-four output amplifier has been optimized for fast and accurate large signal step settling characteristics even when heavily loaded. This amplifier's fast Settling Time Linearity (STL) characteristic causes the amplifier to be transparent to the low signal level distortion of the sampler. When sampled, output distortion levels reflect only the distortion performance of the sampler.

Dramatic SNR and distortion improvements can be realized when using the AD9101 with high speed flash converters. Flash converters generally have excellent linearity at dc and low frequencies. However, as signal slew rate increases, their performance degrades due to the internal comparators' aperture delay variations and finite gain bandwidth product.

The benefits of using a track-and-hold ahead of a flash converter have been well known for many years. However, before the AD9101, there was no track-and-hold amplifier with sufficient bandwidth and linearity to markedly increase the dynamic performance of such flashes as the AD9002, AD9012, AD9020, and AD9060.

A new application made possible by the AD9101 is direct IF-to-digital conversion. Utilizing the Nyquist principle, the IF frequency can be rejected, and the baseband signal can be recovered. As an example, a 40 MHz IF is modulated by a 10 MHz bandwidth signal. By sampling at 25 MSPS, the signal of interest is detected.

The AD9101 is offered in commercial and military temperature ranges. Commercial versions include the AD9101AR in plastic SOIC and AD9101AE in ceramic LCC. Military devices are available in ceramic LCC. Contact the factory for availability of versions in DIP and/or military versions.

PRODUCT HIGHLIGHTS

1. Guaranteed Hold-Mode Distortion
2. 125 MHz Sampling Rate to 8 Bits; 50 MHz to 12 Bits
3. 350 MHz Sampling Bandwidth
4. Super-Nyquist Sampling Capability
5. Output Offset Adjustable

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9101—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $+V_S = +5$ V, $-V_S = -5.2$ V, $R_{LOAD} = 100\ \Omega$, $R_{IN} = 50\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9101 Min	AD9101 Typ	AD9101 Max	Units
DC ACCURACY							
Gain	$\Delta V_{IN} = 0.5$ V	25°C	I	3.93	4	4.07	V/V
	$\Delta V_{IN} = 0.5$ V	Full	VI	3.9		4.1	V/V
Offset	$V_{IN} = 0$ V	25°C	I		±3	±10	mV
	$V_{IN} = 0$ V	Full	VI			±15	mV
Output Resistance		25°C	V		0.4		Ω
Output Drive Capability		Full	VI	±60	±70		mA
PSRR	$\Delta V_S = 0.5$ V p–p	25°C	VI	37	43		dB
Pedestal Sensitivity to Positive Supply	$\Delta V_S = 0.5$ V p–p	Full	V		4		mV/V
Pedestal Sensitivity to Negative Supply	$\Delta V_S = 0.5$ V p–p	Full	V		8		mV/V
ANALOG INPUT/OUTPUT							
Output Voltage Range		Full	VI	±2.4	±2.7		V
Input Bias Current		25°C	I		±5	±15	μA
		Full	VI			±20	μA
Input Capacitance		25°C	V		2		pF
Input Resistance		25°C – T_{MAX}	VI	30	125		kΩ
		T_{MIN}	VI	25			kΩ
CLOCK/$\overline{\text{CLOCK}}$ INPUTS							
Input Bias Current	CL/$\overline{\text{CL}}$ = −1.0 V	Full	VI		3	3.6	mA
Input Low Voltage (V_{IL})[1]	$V_{IN} = 0.5$ V p–p	Full	VI	−1.8		−1.5	V
Input High Voltage (V_{IH})[1]	$V_{IN} = 0.5$ V p–p	Full	VI	−1.0		−0.8	V
TRACK MODE DYNAMICS							
Bandwidth (−3 dB)	$V_{OUT} = 1$ V p–p	Full	IV	160	250		MHz
Slew Rate	4 Volt Output Step	Full	IV	1300	1800		V/μs
Overdrive Recovery Time[2] (to 0.1%)	$V_{IN} = \pm 1$ V to 0 V	25°C	V		55		ns
Integrated Output Noise	(5 MHz–200 MHz)	25°C	V		210		μV
Input RMS Spectral Noise @ 10 MHz		25°C	V		3.3		nV/√Hz
HOLD MODE DYNAMICS							
Worst Harmonic (23 MHz, 50 MSPS)	$V_{OUT} = 2$ V p–p	25°C	V		−75		dBFS
Worst Harmonic (48 MHz, 100 MSPS)	$V_{OUT} = 2$ V p–p	25°C	IV		−62	−57	dBFS
Worst Harmonic (48 MHz, 100 MSPS)	$V_{OUT} = 2$ V p–p	Full (Ind.)	IV			−53	dBFS
Worst Harmonic (48 MHz, 100 MSPS)	$V_{OUT} = 2$ V p–p	Full (Mil.)	IV			−51	dBFS
Worst Harmonic (48 MHz, 125 MSPS)	$V_{OUT} = 2$ V p–p	25°C	V		−57		dBFS
Sampling Bandwidth (−3 dB)[3]	$V_{IN} = 0.5$ V p–p	25°C	V		350		MHz
Hold Noise[4] (RMS)		Full	V		150 × t_H		mV/s
Droop Rate		25°C	I		±5	±18	mV/μs
		Full	VI			±40	mV/μs
Feedthrough Rejection (50 MHz)	$V_{OUT} = 2$ V p–p	Full	V		−66		dB
TRACK-TO-HOLD SWITCHING							
Aperture Delay		25°C	V		−250		ps
Aperture Jitter		25°C	V		<1		ps rms
Pedestal Offset	$V_{IN} = 0$ V	25°C	I		±5	±20	mV
	$V_{IN} = 0$ V	Full	VI			±35	mV
Transient Amplitude	$V_{IN} = 0$ V	Full	V		8		mV
Settling Time to 4 mV	$V_{IN} = 0$ V	Full	V		4		ns
Glitch Product[5]	$V_{IN} = 0$ V	25°C	V		20		pV-s
HOLD-TO-TRACK SWITCHING							
Acquisition Time to 0.1%	2 V Output Step	25°C	V		7		ns
Acquisition Time to 0.01%	2 V Output Step	25°C	IV		11	14	ns
	2 V Output Step	Full	IV			16	ns
POWER SUPPLY							
$+V_S$ Current		Full	VI		55	70	mA
$-V_S$ Current		Full	VI		59	73	mA
Power Dissipation		Full	VI		570	715	mW

NOTES
[1]If the analog input exceeds ±300 mV, the clock levels should be shifted as shown in the Theory of Operation section entitled "Driving the Encode Clock."
[2]Time to recover within rated error band from 160% overdrive.
[3]Sampling bandwidth is defined as the −3 dB frequency response of the input sampler to the hold capacitor when operating in the sampling mode. It is greater than tracking bandwidth because it does not include the bandwidth of the output amplifier.
[4]Hold mode noise is proportional to the length of time a signal is held. For example, if the hold time (t_H) is 20 ns, the accumulated noise is typically 3 μV (150 mV/s × 20 ns). This value must be combined with the track mode noise to obtain total noise.
[5]Total energy of worst case track-to-hold or hold-to-track glitch.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S$) . . . . . −0.5 V to +6 V
Supply Voltage ($-V_S$) . . . . . −6 V to +0.5 V
Analog Input Voltage . . . . . ±5 V
CLOCK/CLOCK Input . . . . . −5 V to +0.5 V
Continuous Output Current[4] . . . . . 70 mA
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature Range
AE, AR . . . . . −40°C to +85°C
SE . . . . . −55°C to +125°C
Junction Temperature (Ceramic)[2] . . . . . +175°C
Junction Temperature (Plastic)[2] . . . . . +150°C
Soldering Temperature (1 minute)[3] . . . . . +220°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances (no air flow, soldered to PC board) are as follows: Ceramic LCC: θ_{JA} = 48°C/W; θ_{JC} = 9.9°C/W; Plastic SOIC: θ_{JA} = 54°C/W; θ_{JC} = 7.3°C/W.
[3]For surface mount devices, mounted by vapor phase soldering. Prior to vapor phase soldering, plastic units should receive a minimum eight hour bakeout at 110°C to drive off any moisture absorbed in plastic during shipping or storage. Through-hole devices can be soldered at +300°C for 10 seconds.
[4]Output is short circuit protected to ground. Continuous short circuit may affect device reliability.

Pin Description

Pin	Description	Connection
1	RTN	Gain Set Resistor Return*
2	RTN	Gain Set Resistor Return*
3	C_{B+}	Bootstrap Capacitor (Positive Bias)
4	$+V_S$	+5 V Power Supply (Analog)
5	$+V_S$	+5 V Power Supply (Analog)
6	GND	Hold Capacitor Ground
7	GND	Hold Capacitor Ground
8	$+V_S$	+5 V Power Supply (Digital)
9	$+V_S$	+5 V Power Supply (Digital)
10	CLK	True ECL T/H Clock
11	$\overline{CLK}$	Complement ECL T/H Clock
12	$-V_S$	−5.2 V Power Supply (Digital)
13	$-V_S$	−5.2 V Power Supply (Digital)
14	N/C	No Connection
15	V_{IN}	Analog Signal Input
16	GND	Ground (Signal Return)
17	$-V_S$	−5.2 V Power Supply (Analog)
18	$-V_S$	−5.2 V Power Supply (Analog)
19	C_{B-}	Bootstrap Capacitor (Negative Bias)
20	V_{OUT}	Analog Signal Output

*See "Matching the AD9101 to A/D Encoders" in complete data sheet. Both pins should either be grounded or connected to voltage source for offset.

EXPLANATION OF TEST LEVELS

Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Periodically sample tested.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

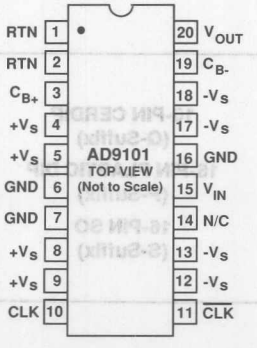
ORDERING INFORMATION

Model	Temperature Range	Package Description	Package Option*
AD9101AR	−40°C to +85°C	Plastic SOIC	R-20
AD9101AE	−40°C to +85°C	LCC	E-20A
AD9101SE	−55°C to +125°C	LCC	E-20A

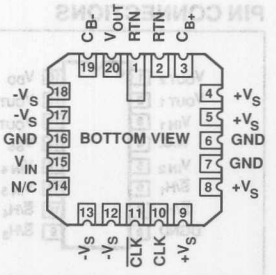
*For outline information see Package Information section.

PIN CONFIGURATIONS

20-Pin SOIC



20-PIN LCC PACKAGE (E-20A)



ANALOG DEVICES

CMOS Quad Sample-and-Hold Amplifier

SMP04

FEATURES

- Four Independent Sample-and-Holds
- Internal Hold Capacitors
- High Accuracy – 12-Bit
- Very Low Droop Rate (2mV/s Typ)
- Output Buffers Stable for $C_L \leq 500pF$
- TTL/CMOS Compatible Logic Inputs
- Single or Dual Supply Applications
- Monolithic Low Power CMOS Design

APPLICATIONS

- Signal Processing Systems
- Multichannel Data Acquisition Systems
- Automatic Test Equipment
- Medical and Analytical Instrumentation
- Event Analysis
- DAC Deglitching

ORDERING INFORMATION †

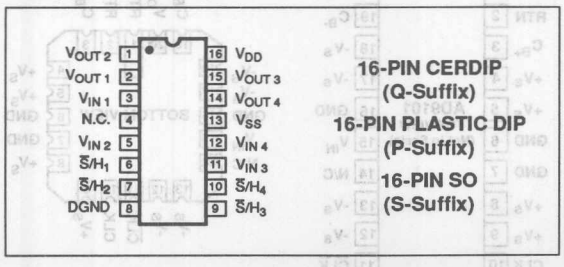
PACKAGE			OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN		CERDIP 16-PIN	
—		SMP04AQ/883*	MIL
SMP04EP		SMP04EQ	XIND
SMP04ES††		—	XIND

* Consult factory for 883 data sheet.

† Burn-in is available on extended industrial temperature range parts in CerDIP and plastic DIP packages.

†† For availability and burn-in information on SO packages, contact your local sales office.

PIN CONNECTIONS



16-PIN CERDIP (Q-Suffix)

16-PIN PLASTIC DIP (P-Suffix)

16-PIN SO (S-Suffix)

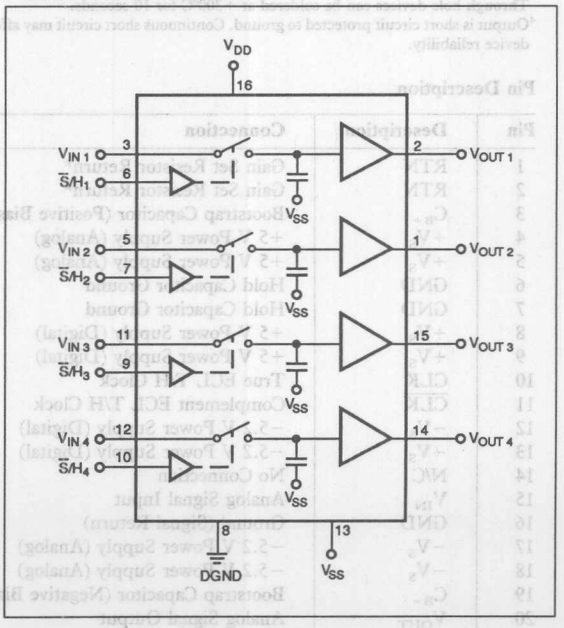
GENERAL DESCRIPTION

The SMP-04 is a monolithic quad sample-and-hold; it has four internal precision buffer amplifiers and internal hold capacitors. It is manufactured in PMI's advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate and fast acquisition time required by data acquisition and signal processing systems. The device can acquire an 8-bit input signal to ±1/2 LSB in less than seven microseconds. The SMP-04 can operate from single or dual power supplies with TTL/CMOS logic compatibility. Its output swing includes the negative supply.

The SMP-04 is ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more can be used with a single or multiple DACs to provide multiple set points within a system.

The SMP-04 offers significant cost and size reduction over equivalent module or discrete designs. It is available in a 16-pin hermetic or plastic DIP and surface mount SOIC packages. It is specified over the extended industrial temperature range of –40°C to +85°C. See SMP-04/883 data sheet for –55°C to +125°C specifications.

FUNCTIONAL DIAGRAM



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DD} to DGND ..... –0.3V, 17V
V_{DD} to V_{SS} ..... –0.7V, 17V
V_{LOGIC} to DGND ..... –0.3V, V_{DD}
V_{IN} to DGND ..... V_{SS}, V_{DD}
V_{OUT} to DGND ..... V_{SS}, V_{DD}
Analog Output Current ..... ±20mA
(Not short-circuit protected)
Digital Input Voltage to DGND ..... –0.3V, V_{DD} +0.3V
Operating Temperature Range
EQ, EP, ES ..... –40°C to +85°C
AQ ..... –55°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin CerDIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SO (S)	92	27	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

CAUTION:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and function operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper anti-static handling procedures.
3. Remove power before inserting or removing units from their sockets.

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ELECTRICAL CHARACTERISTICS at V_{DD} = +12.0V, V_{SS} = DGND = 0V, R_L = No Load, T_A = Operating Temperature Range specified in Absolute Maximum Ratings, unless otherwise specified.

			SMP-04			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Linearity Error			–	0.01	–	%
Buffer Offset Voltage	V_{OS}	V_{IN} = 6V	–10	±2.5	+10	mV
Hold Step	V_{HS}	V_{IN} = 6V	–	1	±4	mV
Droop Rate	$\Delta V/\Delta t$	V_{IN} = 6V, T_A = +25°C	–	2	25	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 6V (Note 1)	1.2	–	–	mA
Output Sink Current	I_{SINK}	V_{IN} = 6V (Note 1)	0.5	–	–	mA
Output Voltage Range	OVR	R_L = 20kΩ R_L = 10kΩ	0.06 0.06	– –	10.0 9.5	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4	–	–	V
Logic Input Low Voltage	V_{INL}		–	–	0.8	V
Logic Input Current	I_{IN}		–	0.5	1	µA
DYNAMIC PERFORMANCE (Note 2)						
Acquisition Time	t_A	T_A = +25°C, 0 to 10V step to 0.1%	–	7	–	µs
Acquisition Time	t_A	T_A = +25°C, 0 to 10V step to 0.01%	–	9	–	µs
Hold Mode Settling Time	t_H	To 1mV	–	1	–	µs
Slew Rate	SR	R_L = 20kΩ (Note 3)	3	4	–	V/µs
Capacitive Load Stability	C_L	<30% Overshoot	–	500	–	pF
Analog Crosstalk		0 to 10V step	–	–80	–	dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	$10.8 \le V_{DD} \le 13.2V$	60	75	–	dB
Supply Current	I_{DD}		–	4	7	mA
Power Dissipation	P_{DIS}		–	–	84	mW

NOTES:
1. Outputs are capable of sinking and sourcing over 20mA but linearity and offset are guaranteed at specified load levels.
2. All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
3. Slew rate is measured in the sample mode with a 0 to 10 volt step from 20 to 80%.

PARAMETER	SYMBOL	CONDITIONS	SMP-04 MIN	SMP-04 TYP	SMP-04 MAX	UNITS
Linearity Error			–	.01	–	%
Buffer Offset Voltage	V_{OS}	V_{IN} = 0V	–10	±2.5	+10	mV
Hold Step	V_{HS}	V_{IN} = 0V	–	–1	±4	mV
Droop Rate	$\Delta V/\Delta t$	V_{IN} = 0V, T_A = +25°C	–	2	25	mV/s
Output Resistance	R_{OUT}		–	1	–	Ω
Output Source Current	I_{SOURCE}	V_{IN} = 0V (Note 1)	1.2	–	–	mA
Output Sink Current	I_{SINK}	V_{IN} = 0V (Note 1)	0.5	–	–	mA
Output Voltage Range	OVR	R_L = 20kΩ	–3.0	–	+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4	–	–	V
Logic Input Low Voltage	V_{INL}		–	–	0.8	V
Logic Input Current	I_{IN}		–	0.5	1	µA
DYNAMIC PERFORMANCE (Note 2)						
Acquisition Time	t_A	–3 to +3V step to 0.1%	–	7	–	µs
Acquisition Time	t_A	–3 to +3V step to 0.01%	–	9	–	µs
Hold Mode Settling Time	t_H	To 1mV	–	1	–	µs
Slew Rate	SR	R_L = 20kΩ (Note 3)	–	3	–	V/µs
Capacitive Load Stability	C_L	<30% Overshoot	500	–	–	pF
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	$\pm5 \le V_{DD} \le \pm6V$	60	75	–	dB
Supply Current	I_{DD}		–	3.5	5.5	mA
Power Dissipation	P_{DIS}		–	–	55	mW

NOTES:

1. Outputs are capable of sinking and sourcing over 20mA but linearity and offset are guaranteed at specified load levels.
2. All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of +5V) and timed from a voltage level of 1.6V.
3. Slew rate is measured in the sample mode with a –3 to +3 volt step from 20 to 80%.

Octal Sample-and-Hold with Multiplexed Input

SMP08

FEATURES

- Internal Hold Capacitors
- Low Droop Rate
- TTL/CMOS Compatible Logic Inputs
- Single or Dual Supply Operation
- Break-Before-Make Channel Addressing
- Compatible With CD4051 Pinout
- Low Cost

APPLICATIONS

- Multiple Path Timing Deskew for A.T.E.
- Memory Programmers
- Mass Flow/Process Control Systems
- Multichannel Data Acquisition Systems
- Robotics and Control Systems
- Medical and Analytical Instrumentation
- Event Analysis
- Stage Lighting Control

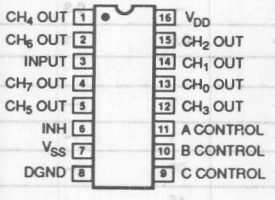
ORDERING INFORMATION †

PACKAGE: 16-PIN DIP/SO		
CERDIP 16-PIN	PLASTIC 16-PIN	OPERATING TEMPERATURE RANGE
TBA*	–	MIL
SMP08FQ	SMP08FP	XIND
–	SMP08FS	XIND

* Consult factory for 883 data sheet.

† Burn-in is available on industrial temperature range parts in CerDIP and plastic DIP packages.

PIN CONNECTIONS



16-PIN CERDIP (Q-Suffix)

16-PIN EPOXY DIP (P-Suffix)

16-PIN SO (S-Suffix)

GENERAL DESCRIPTION

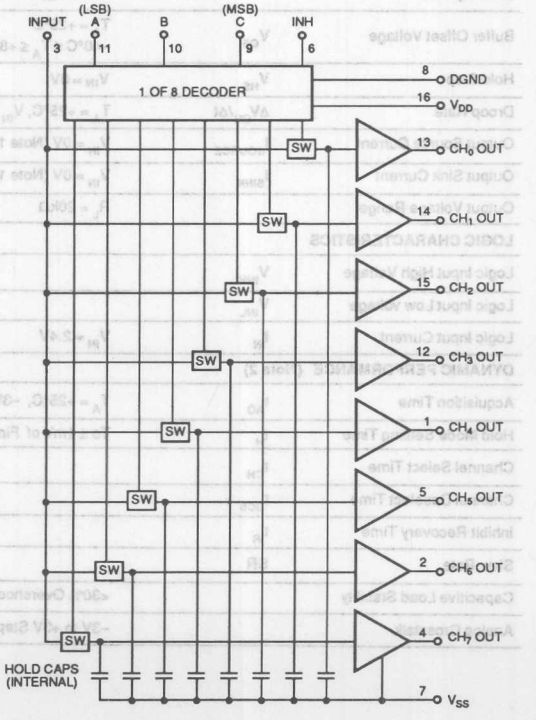
The SMP-08 is a monolithic octal sample-and-hold; it has eight internal buffer amplifiers, input multiplexer, and internal hold capacitors. It is manufactured in an advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate, and fast acquisition time. The SMP-08 has a typical linearity error of only 0.01% and can accurately acquire a 10-bit input signal to ±1/2 LSB in less than seven microseconds. The SMP-08's output swing includes the negative supply in both single and dual supply operation.

The SMP-08 was specifically designed for systems that use a calibration cycle to adjust a multiple of system parameters. The low cost and high level of integration makes the SMP-08 ideal for calibration requirements that have previously required an ASIC, or high cost multiple D/A converters.

The SMP-08 is also ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more SMP-08s can be used with single or multiple DACs to provide multiple set points within a system.

The SMP-08 offers significant cost and size reduction over discrete designs. It is available in a 16-pin hermetic or plastic DIP, or surface mount SOIC package.

FUNCTIONAL DIAGRAM



Manufactured under the following U.S. patent: 4,739,281

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ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{DD} to DGND ..... –0.3V, 17V
V_{DD} to V_{SS} ..... –0.3V, 17V
V_{LOGIC} to DGND ..... –0.3V, V_{DD}
V_{IN} to DGND ..... V_{SS}, V_{DD}
V_{OUT} to DGND ..... V_{SS}, V_{DD}
Analog Output Current ..... ±20mA
(Not short-circuit protected)
Operating Temperature Range
FP, FS ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SO (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

CAUTION:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper anti-static handling procedures.
3. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{SS} = –5V, DGND = 0V, R_L = No Load, T_A = –40°C to +85°C for SMP-08F, unless otherwise noted.

			SMP-08F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Linearity Error		–3V ≤ V_{IN} ≤ +3V	—	0.01	—	%
Buffer Offset Voltage	V_{OS}	T_A = +25°C	—	2.5	10	mV
		–40°C ≤ T_A ≤ +85°C	—	3.5	20	
Hold Step	V_{HS}	V_{IN} = 0V	—	1	4	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 0V	—	2	20	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 0V (Note 1)	1.2	—	—	mA
Output Sink Current	I_{SINK}	V_{IN} = 0V (Note 1)	0.5	—	—	mA
Output Voltage Range		R_L = 20kΩ	–3.0	—	+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4	—	—	V
Logic Input Low voltage	V_{INL}		—	—	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4V	—	0.5	1	µA
DYNAMIC PERFORMANCE (Note 2)						
Acquisition Time	t_{AQ}	T_A = +25°C, –3V to +3V to 0.1%	—	7	—	µs
Hold Mode Settling Time	t_H	To ± 1mV of Final Value	—	1	—	µs
Channel Select Time	t_{CH}		—	90	—	ns
Channel Deselect Time	t_{DCS}		—	45	—	ns
Inhibit Recovery Time	t_{IR}		—	90	—	ns
Slew Rate	SR		—	3	—	V/µs
Capacitive Load Stability		<30% Overshoot	—	500	—	pF
Analog Crosstalk		–3V to +3V Step	—	–72	—	dB

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{SS} = –5V, DGND = 0V, R_L = No Load, T_A = –40°C to +85°C for SMP-08F, unless otherwise noted. *Continued*

			SMP-08F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±6V	60	75	—	dB
Supply Current	I_{DD}	T_A = +25°C –40°C ≤ T_A ≤ +85°C	— —	5.5 7.5	7.5 9.5	mA

NOTES:
1. Outputs are capable of sinking and sourcing over 20mA but offset is guaranteed at specified load levels.
2. All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

ELECTRICAL CHARACTERISTICS at V_{DD} = +12V, V_{SS} = 0V, DGND = 0V, R_L = No Load, T_A = –40°C to +85°C for SMP-08F, unless otherwise noted.

			SMP-08F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Linearity Error		60mV ≤ V_{IN} ≤ 10V	—	0.01	—	%
Buffer Offset Voltage	V_{OS}	T_A = +25°C –40°C ≤ T_A ≤ +85°C	— —	2.5 3.5	10 20	mV
Hold Step	V_{HS}	V_{IN} = 6V	—	1	4	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 6V	—	2	20	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 6V (Note 1)	1.2	—	—	mA
Output Sink Current	I_{SINK}	V_{IN} = 6V (Note 1)	0.5	—	—	mA
Output Voltage Range		R_L = 20kΩ R_L = 10kΩ	0.06 0.06	— —	10.0 9.5	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4	—	—	V
Logic Input Low voltage	V_{INL}		—	—	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4V	—	0.5	1	µA
DYNAMIC PERFORMANCE (Note 2)						
Acquisition Time	t_{AQ}	T_A = +25°C, 0 to 10V to 0.1%	—	9	—	µs
Hold Mode Settling Time	t_H	To ± 1mV of Final Value	—	1	—	µs
Channel Select Time	t_{CH}		—	90	—	ns
Channel Deselect Time	t_{DCS}		—	45	—	ns
Inhibit Recovery Time	t_{IR}		—	90	—	ns
Slew Rate	SR	R_L = 20kΩ (Note 3)	3	4	—	V/µs
Capacitive Load Stability		<30% Overshoot	—	500	—	pF
Analog Crosstalk		0 to 10V Step	—	–72	—	dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	10.8V ≤ V_{DD} ≤ 13.2V	60	75	—	dB
Supply Current	I_{DD}	T_A = +25°C –40°C ≤ T_A ≤ +85°C	— —	6.0 8.0	8.0 10.0	mA

NOTES:
1. Outputs are capable of sinking and sourcing over 20mA but offset is guaranteed at specified load levels.
2. All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
3. Slew rate is measured in the sample mode with a 0 to 10V step from 20% to 80%.

Octal Sample-and-Hold with Multiplexed Input

SMP18

FEATURES

- High Speed Version of SMP-08
- Internal Hold Capacitors
- Low Droop Rate
- TTL/CMOS Compatible Logic Inputs
- Single or Dual Supply Operation
- Break-Before-Make Channel Addressing
- Compatible With CD4051 Pinout
- Low Cost

APPLICATIONS

- Multiple Path Timing Deskew for A.T.E.
- Memory Programmers
- Mass Flow/Process Control Systems
- Multichannel Data Acquisition Systems
- Robotics and Control Systems
- Medical and Analytical Instrumentation
- Event Analysis
- Stage Lighting Control

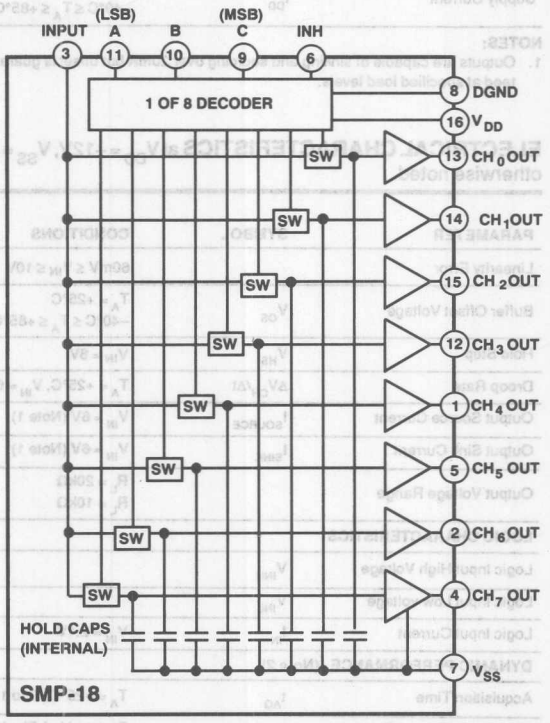
GENERAL DESCRIPTION

The SMP-18 is a monolithic octal sample-and-hold; it has eight internal buffer amplifiers, input multiplexer, and internal hold capacitors. It is manufactured in an advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate, and fast acquisition time. The SMP-18 has a typical linearity error of only 0.01% and can accurately acquire a 10-bit input signal to ±1/2 LSB in less than 2.5 microseconds. The SMP-18's output swing includes the negative supply in both single and dual supply operation.

The SMP-18 was specifically designed for systems that use a calibration cycle to adjust a multiple of system parameters. The low cost and high level of integration make the SMP-18 ideal for calibration requirements that have previously required an ASIC, or high cost multiple D/A converters.

The SMP-18 is also ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more SMP-18s can be used with single or multiple DACs to provide multiple set points within a system.

FUNCTIONAL BLOCK DIAGRAM



The SMP-18 offers significant cost and size reduction over discrete designs. It is available in a 16-pin hermetic, plastic DIP or narrow body SO-16 surface-mount SOIC package. The SMP-18 is a higher speed direct replacement for the SMP-08.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5 V, V_{SS} = −5 V, DGND = 0 V, R_L = No Load, T_A = −40°C to +85°C for SMP-18F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error		−3 V ≤ V_{IN} ≤ +3 V		0.01		%
Buffer Offset Voltage	V_{OS}	T_A = +25°C, V_{IN} = 0 V		2.5	10	mV
		−40°C ≤ T_A ≤ +85°C, V_{IN} = 0 V		3.5	20	mV
Hold Step	V_{HS}	V_{IN} = 0 V		4	6	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 0 V		2	40	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 0 V[1]	1.2			mA
Output Sink Current	I_{SINK}	V_{IN} = 0 V[1]	0.5			mA
Output Voltage Range		R_L = 20 kΩ	−3.0		+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4 V		0.5	1	µA
DYNAMIC PERFORMANCE[2]						
Acquisition Time	t_{AQ}	T_A = +25°C, −3 V to +3 V to 0.1%		3.5		µs
Hold Mode Settling Time	t_H	To ±1 mV of Final Value		1		µs
Channel Select Time	t_{CH}			90		ns
Channel Deselect Time	t_{DCS}			45		ns
Inhibit Recovery Time	t_{IR}			90		ns
Slew Rate	SR			6		V/µs
Capacitive Load Stability		<30% Overshoot		500		pF
Analog Crosstalk		−3 V to +3 V Step		−72		dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	V_{SS} = ±5 V to ±6 V	60	75		dB
Supply Current	I_{DD}	T_A = +25°C		5.5	7.5	mA
		−40°C ≤ T_A ≤ +85°C		7.5	9.5	mA

NOTES
[1]Outputs are capable of sinking and sourcing over 10 mA but offset is guaranteed at specified load levels.
[2]All input control signals are specified with t_r = t_f = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +12 V, V_{SS} = 0 V, DGND = 0 V, R_L = No Load, T_A = −40°C to +85°C for SMP-18F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error		60 mV ≤ V_{IN} ≤ 10 V		0.01		%
Buffer Offset Voltage	V_{OS}	T_A = +25°C, V_{IN} = 6 V		2.5	10	mV
		−40°C ≤ T_A ≤ +85°C, V_{IN} = 6 V		3.5	20	mV
Hold Step	V_{HS}	V_{IN} = 6 V		4	6	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 6 V		2	40	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 6 V[1]	1.2			mA
Output Sink Current	I_{SINK}	V_{IN} = 6 V[1]	0.5			mA
Output Voltage Range		R_L = 20 kΩ	0.06		10.0	V
		R_L = 10 kΩ	0.06		9.5	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4 V		0.5	1	µA
DYNAMIC PERFORMANCE[2]						
Acquisition Time	t_{AQ}	T_A = +25°C, 0 to 10 V to 0.1%		2.5		µs
Hold Mode Settling Time	t_H	To ±1 mV of Final Value		1		µs
Channel Select Time	t_{CH}			90		ns
Channel Deselect Time	t_{DCS}			45		ns
Inhibit Recovery Time	t_{IR}			90		ns
Slew Rate[3]	SR			7		V/µs
Capacitive Load Stability		<30% Overshoot		500		pF
Analog Crosstalk		0 to 10 V Step		−72		dB

Supply Current	I_{DD}	T_A = +25°C	6.0	8.0	mA
		−40°C ≤ T_A ≤ +85°C	8.0	10.0	mA

NOTES
[1]Outputs are capable of sinking and sourcing over 10 mA but offset is guaranteed at specified load levels.
[2]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[3]Slew rate is measured in the sample mode with a 0 to 10 V step from 20% to 80%.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to DGND ..... −0.3 V, 17 V
V_{DD} to V_{SS} ..... −0.3 V, 17 V
V_{LOGIC} to DGND ..... −0.3 V, V_{DD}
V_{IN} to DGND ..... V_{SS}, V_{DD}
V_{OUT} to DGND ..... V_{SS}, V_{DD}
Analog Output Current ..... ±20 mA
(Not short-circuit protected)
Operating Temperature Range
FQ, FP, FS ..... −40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

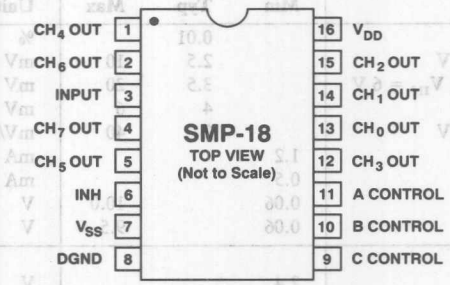
Package Type	θ_{JA}[2]	θ_{JC}	Units
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOIC (S)	92	27	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

CAUTION

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures.
3. Remove power before inserting or removing units from their sockets.

PIN CONNECTIONS



ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
SMP18FQ	−40°C to +85°C	Cerdip	Q-16
SMP18FP	−40°C to +85°C	Plastic DIP	N-16
SMP18FS	−40°C to +85°C	SO-16	R-16A

NOTES
[1]Consult factory for 883 data sheet.
[2]For outline information see Package Information section.

Switches and Multiplexers
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ADG406/ADG407/ADG426 – LC²MOS 8-/16-Channel High Performance Analog Multiplexers	7–22
ADG408/ADG409 – LC²MOS 4/8 Channel High Performance Analog Multiplexers	7–28
ADG411/ADG412/ADG413 – DI LC²MOS Precision Quad SPST Switches	7–36
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ADG428/ADG429 – LC²MOS Latchable 4/8 Channel High Performance Analog Multiplexers	7–48
ADG431/ADG432/ADG433 – DI LC²MOS Precision Quad SPST Switches	7–56
ADG441/ADG442/ADG444 – LC²MOS Quad SPST Switches	7–64
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ADG508F/ADG509F/ADG528F/ADG529F – LC²MOS 4/8 Channel Fault-Protected Analog Multiplexers	7–74
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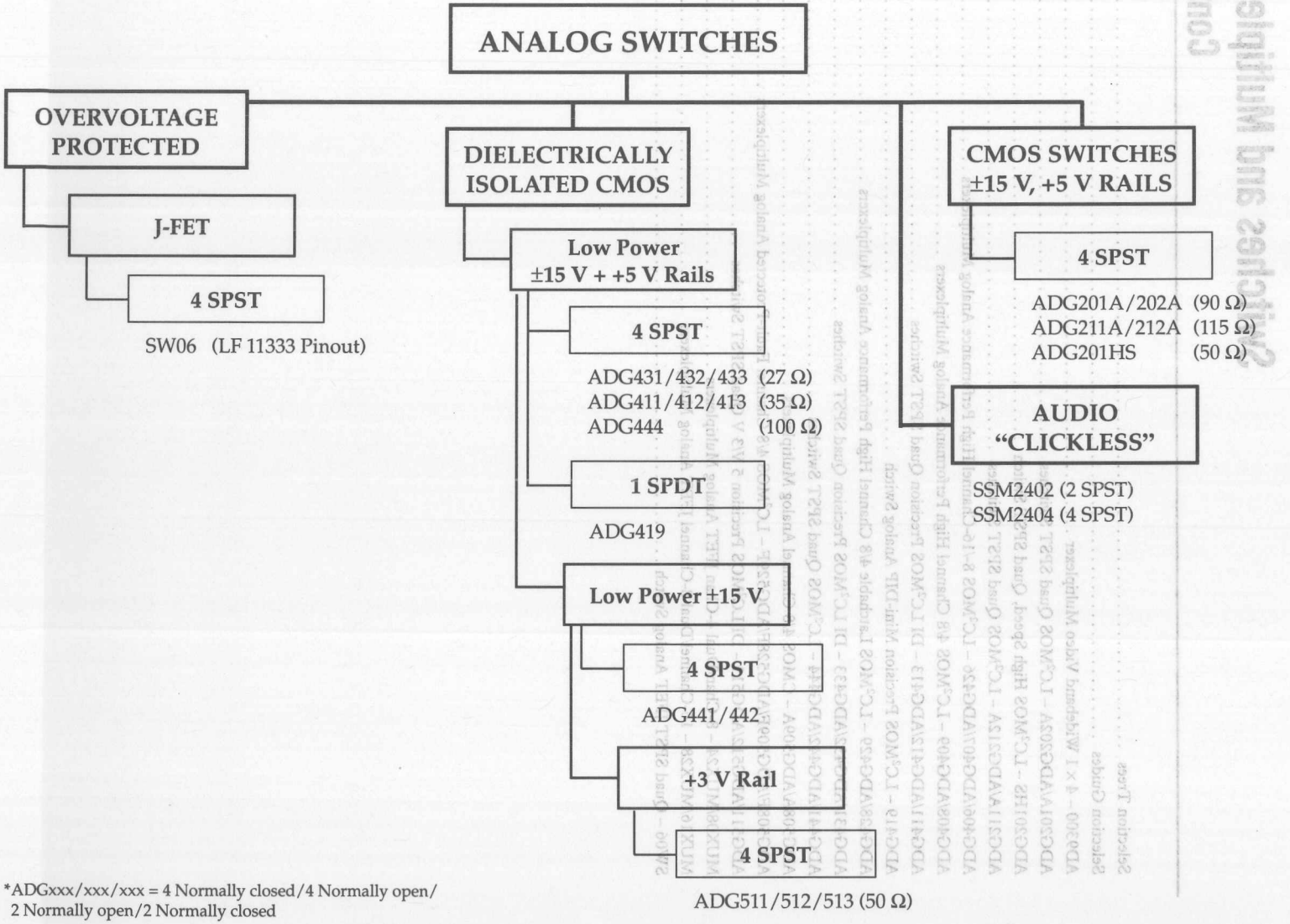
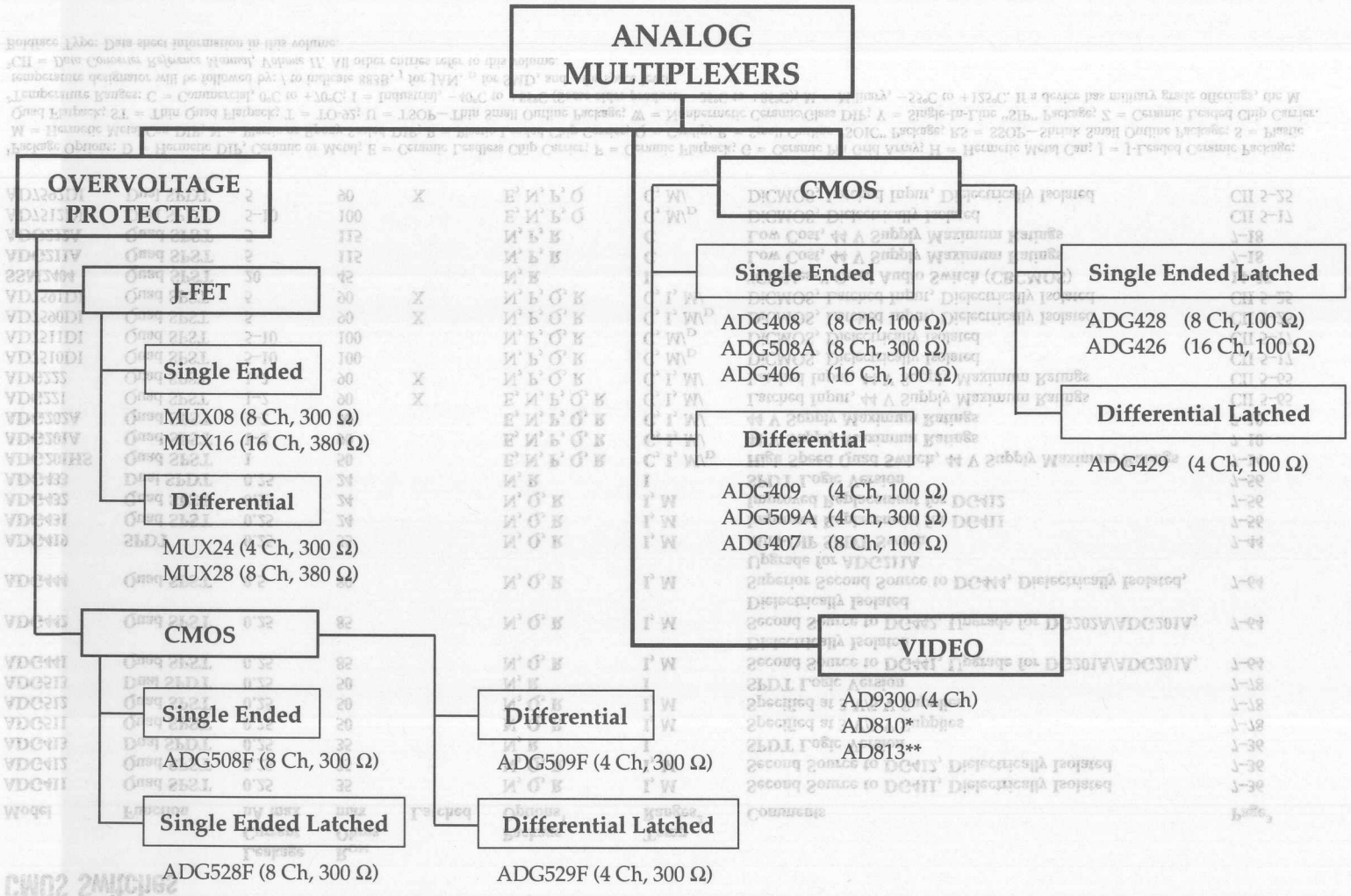
MUX08/MUX24 – 8-Chan/Dual 4-Chan JFET Analog Multiplexers	7–87
MUX16/MUX28 – 16-Channel/Dual 8-Channel JFET Analog Multiplexers	7–90
SW06 – Quad SPST JFET Analog Switch	7–93

Selection Tree — Switches



*ADGxxx/xxx/xxx = 4 Normally closed/4 Normally open/ 2 Normally open/2 Normally closed

Selection Tree — Multiplexers



* Single Op Amp with Disable Function
** Triple Op Amp with Disable Function

Selection Guides—Switches and Multiplexers

CMOS Switches

Model	Function	Leakage Current nA max	R_{ON} Ohms max	Latched	Package Options[1]	Temp Ranges[2]	Comments
ADG411	**Quad SPST**	**0.25**	**35**		**N, Q, R**	**I, M**	**Second Source to DG411, Dielectrically Isolated**
ADG412	**Quad SPST**	**0.25**	**35**		**N, Q, R**	**I, M**	**Second Source to DG412, Dielectrically Isolated**
ADG413	**Dual SPDT**	**0.25**	**35**		**N, R**	**I**	**SPDT Logic Version**
ADG511	**Quad SPST**	**0.25**	**50**		**N, Q, R**	**I, M**	**Specified at 3 V/5 V Supplies**
ADG512	**Quad SPST**	**0.25**	**50**		**N, Q, R**	**I, M**	**Specified at 3 V/5 V Supplies**
ADG513	**Dual SPDT**	**0.25**	**50**		**N, R**	**I**	**SPDT Logic Version**
ADG441	**Quad SPST**	**0.25**	**85**		**N, Q, R**	**I, M**	**Second Source to DG441, Upgrade for DG201A/ADG201A, Dielectrically Isolated**
ADG442	**Quad SPST**	**0.25**	**85**		**N, Q, R**	**I, M**	**Second Source to DG442, Upgrade for DG202A/ADG201A, Dielectrically Isolated**
ADG444	**Quad SPST**	**0.5**	**80**		**N, Q, R**	**I, M**	**Superior Second Source to DG444, Dielectrically Isolated, Upgrade for ADG211A**
ADG419	**SPDT**	**0.25**	**35**		**N, Q, R**	**I, M**	**Mini-DIP SPDT Switch**
ADG431	**Quad SPST**	**0.25**	**24**		**N, Q, R**	**I, M**	**Improved Replacement for DG411**
ADG432	**Quad SPST**	**0.25**	**24**		**N, Q, R**	**I, M**	**Improved Replacement for DG412**
ADG433	**Dual SPDT**	**0.25**	**24**		**N, R**	**I**	**SPDT Logic Version**
ADG201HS	**Quad SPST**	**1**	**50**		**E, N, P, Q, R**	**C, I, $M/_D$**	**High Speed Quad Switch, 44 V Supply Maximum Ratings**
ADG201A	**Quad SPST**	**1–2**	**90**		**E, N, P, Q, R**	**C, I, M/**	**44 V Supply Maximum Ratings**
ADG202A	**Quad SPST**	**1–2**	**90**		**E, N, P, Q, R**	**C, I, M/**	**44 V Supply Maximum Ratings**
ADG221	Quad SPST	1–2	90	X	E, N, P, Q, R	C, I, M/	Latched Input, 44 V Supply Maximum Ratings
ADG222	Quad SPST	1–2	90	X	N, P, Q, R	C, I, M/	Latched Input, 44 V Supply Maximum Ratings
AD7510DI	Quad SPST	5–10	100		N, P, Q, R	C, $M/_D$	DiCMOS, Dielectrically Isolated
AD7511DI	Quad SPST	5–10	100		N, P, Q, R	C, $M/_D$	DiCMOS, Dielectrically Isolated
AD7590DI	Quad SPST	5	90	X	N, P, Q, R	C, I, $M/_D$	DiCMOS, Latched Input, Dielectrically Isolated
AD7591DI	Quad SPST	5	90	X	N, P, Q, R	C, I, M/	DiCMOS, Latched Input, Dielectrically Isolated
SSM2404	**Quad SPST**	**20**	**45**		**N, R**	**I**	**"Clickless" Quad Audio Switch (CBCMOS)**
ADG211A	**Quad SPST**	**5**	**115**		**N, P, R**	**C**	**Low Cost, 44 V Supply Maximum Ratings**
ADG212A	**Quad SPST**	**5**	**115**		**N, P, R**	**C**	**Low Cost, 44 V Supply Maximum Ratings**
AD7512DI	Dual SPDT	5–10	100		E, N, P, Q	C, $M/_D$	DiCMOS, Dielectrically Isolated
AD7592DI	Dual SPDT	5	90	X	E, N, P, Q	C, M/	DiCMOS, Latched Input, Dielectrically Isolated

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceran
M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package
Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Lead
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offe
temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]CII = *Data Converter Reference Manual, Volume II*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Bipolar JFET Switches

Model	Function	Leakage Current nA max	R_{ON} Ohms max	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
SW06	**Quad SPST**	**2.0**	**80**	**E, N, P, Q**	**I, M/$_D$**	**Improved LF11333/13333, Configures to 2X SPDT & DPDT**	**7–93**
SW201	Quad SPST	10.0	150	N, R	I, M/	Improved Low Cost DG201	CII 5–161
SW202	Quad SPST	10.0	150	N, R	I	Improved Low Cost DG202	CII 5–161
SSM2402	**Dual SPST**	**10.0**	**85**	**N, R**	**I**	**"Clickless" Bilateral Audio Switch**	**14–37**
SSM2412	**Dual SPST**	**10.0**	**85**	**N, R**	**I**	**Fast, Dual Audio Switch**	**14–34**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]CII = *Data Converter Reference Manual, Volume II*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Selection Guides—Switches and Multiplexers

CMOS Multiplexers

Model	Function	Leakage Current nA max	R_{ON} Ohms max	Latched	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
AD75019	16:16	10	300	X	P	C	16 × 16 Analog Crosspoint, Serial Interface	CII 5–39
ADG406	**16:1**	**0.5**	**80**		**N, P**	**I**	**Superior Second Source to DG406**	**7–22**
ADG426	**16:1**	**0.5**	**80**	**X**	**N, RS**	**I**	**Plug-In Upgrade for DG526**	**7–22**
ADG428	**16:1**	**0.5**	**100**	**X**	**N, P, Q**	**I, M**	**Superior Second Source to DG428**	**7–48**
ADG506A	16:1	1	280		E, N, P, Q, R	C, I, $M/_D$	Superior Second Source to DG506A	CII 5–79
ADG526A	16:1	1	280	X	E, N, P, Q, R	C, I, $M/_D$	Superior Second Source to DG526A	CII 5–95
ADG407	**Diff. 8:1**	**0.5**	**80**		**N, P**	**I**	**Superior Second Source to DG407**	**7–22**
ADG429	**Diff. 8:1**	**0.5**	**100**	**X**	**N, P, Q**	**I, M**	**Superior Second Source to DG429**	**7–48**
ADG507A	Diff. 8:1	1	280		E, N, P, Q, R	C, I, $M/_D$	Superior Second Source to DG507A	CII 5–79
ADG527A	Diff. 8:1	1	280	X	E, N, P, Q, R	C, I, $M/_D$	Superior Second Source to DG527A	CII 5–95
ADG408	**8:1**	**0.5**	**100**		**E, N, Q**	**C, I, M**	**Superior Second Source to DG408**	**7–28**
ADG508A	**8:1**	**1**	**300**		**E, N, P, Q, R**	**C, I, $M/_D$**	**Superior Second Source to DG508A**	**7–70**
ADG508F	**8:1**	**0.5**	**300**		**N, P, Q, R**	**I, M**	**Fault Protected**	**7–74**
ADG528F	**8:1**	**0.5**	**300**	**X**	**N, P, Q**	**I, M**	**Fault Protected**	**7–74**
ADG528A	8:1	1	300	X	E, N, P, Q,	C, I, $M/_D$	Superior Second Source to DG528A	CII 5–103
ADG409	**Diff. 4:1**	**0.5**	**100**		**N, Q, R**	**C, I, M**	**Superior Second Source to DG409**	**7–28**
ADG509A	**Diff. 4:1**	**1**	**300**		**E, N, P, Q, R**	**C, I, $M/_D$**	**Superior Second Source to DG509A**	**7–70**
ADG509F	**Diff. 4:1**	**0.5**	**300**	**X**	**N, P, Q, R**	**I, M**	**Fault Protected**	**7–74**
ADG529F	**Diff. 4:1**	**0.5**	**300**	**X**	**N, P, Q**	**I, M**	**Fault Protected**	**7–74**
ADG529A	Diff. 4:1	1	300	X	E, N, P, Q	C, I, $M/_D$	Superior Second Source to DG529A	CII 5–103

Bipolar JFET Multiplexers

Model	Function	Leakage Current nA max	R_{ON} Ohms max	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
MUX08	**8:1**	**1.0**	**300**	**E, N, Q, R**	**C, I, $M/_D$**	**Improved DG508**	**7–87**
MUX16	**16:1**	**1.0**	**380**	**E, N, P, Q**	**I, $M/_D$**	**Improved DG506**	**7–90**
MUX24	**Diff. 4:1**	**1.0**	**300**	**E, N, Q, R**	**C, I, $M/_D$**	**Improved DG509**	**7–87**
MUX28	**Diff. 8:1**	**1.0**	**380**	**E, N, P, Q**	**I, M/**	**Improved DG507**	**7–90**

Video Multiplexer

Model	Function	Full Power BW MHz min	Crosstalk Rejection F = 10 MHz dB	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
AD9300	**4:1**	**30**	**75**	**E, Q**	**C, M/**	**Wideband Video Mux**	**7–7**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]CII = *Data Converter Reference Manual, Volume II*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

4 × 1 Wideband Video Multiplexer

AD9300

FEATURES

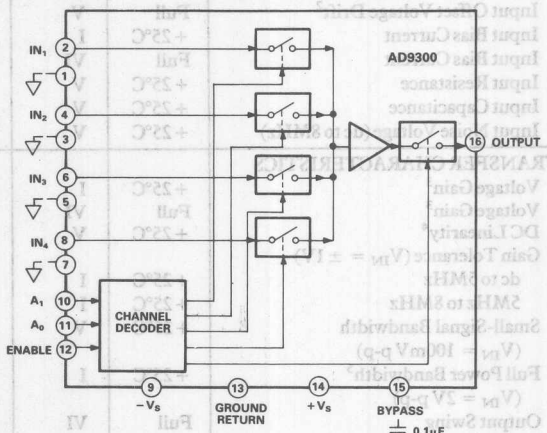
34MHz Full Power Bandwidth
±0.1dB Gain Flatness to 8MHz
72dB Crosstalk Rejection @ 10MHz
0.03°/0.01% Differential Phase/Gain
Cascadable for Switch Matrices
MIL-STD-883 Compliant Versions Available

APPLICATIONS

Video Routing
Medical Imaging
Electro-Optics
ECM Systems
Radar Systems
Data Acquisition

FUNCTIONAL BLOCK DIAGRAM

(Based on Cerdip)



GENERAL DESCRIPTION

The AD9300 is a monolithic high-speed video signal multiplexer useable in a wide variety of applications.

Its four channels of video input signals can be randomly switched at megahertz rates to the single output. In addition, multiple devices can be configured in either parallel or cascade arrangements to form switch matrices. This flexibility in using the AD9300 is possible because the output of the device is in a high-impedance state when the chip is not enabled; when the chip is enabled, the unit acts as a buffer with a high input impedance and low output impedance.

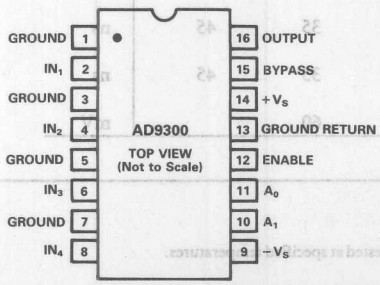
An advanced bipolar process provides fast, wideband switching capabilities while maintaining crosstalk rejection of 72dB at 10MHz. Full power bandwidth is a minimum 27MHz. The device can be operated from ±10V to ±15V power supplies.

The AD9300K is available in a 16-pin ceramic DIP and a 20-pin PLCC and is designed to operate over the commercial temperature range of 0 to +70°C. The AD9300TQ is a hermetic 16-pin ceramic DIP for military temperature range (−55°C to +125°C) applications. This part is also available processed to MIL-STD-883. The AD9300 is available in a 20-pin LCC as the model AD9300TE, which operates over a temperature range of −55°C to +125°C.

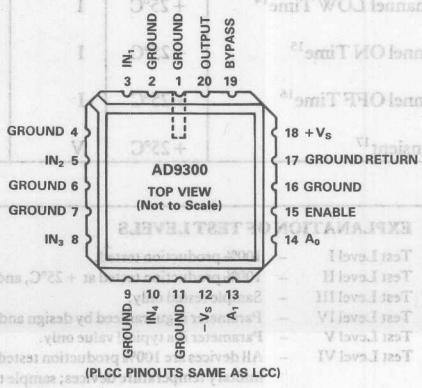
The AD9300 Video Multiplexer is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9300/883B data sheet for detailed specifications.

PIN DESIGNATIONS

DIP



LCC and PLCC



(PLCC PINOUTS SAME AS LCC)

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9300—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 12V \pm 5\%$; $C_L = 10pF$; $R_L = 2k\Omega$, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	COMMERCIAL 0°C to +70°C AD9300KQ/KP Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Input Offset Voltage	+25°C	I		3	10	mV
Input Offset Voltage	Full	VI			14	mV
Input Offset Voltage Drift[2]	Full	V		75		µV/°C
Input Bias Current	+25°C	I		15	37	µA
Input Bias Current	Full	VI			55	µA
Input Resistance	+25°C	V		3.0		MΩ
Input Capacitance	+25°C	V		2		pF
Input Noise Voltage (dc to 8MHz)	+25°C	V		16		µV rms
TRANSFER CHARACTERISTICS						
Voltage Gain[3]	+25°C	I	0.990	0.994		V/V
Voltage Gain[3]	Full	VI	0.985			V/V
DC Linearity[4]	+25°C	V		0.01		%
Gain Tolerance ($V_{IN} = \pm 1V$)						
dc to 5MHz	+25°C	I		0.05	0.1	dB
5MHz to 8MHz	+25°C	I		0.1	0.3	dB
Small-Signal Bandwidth (V_{IN} = 100mV p-p)	+25°C	V		350		MHz
Full Power Bandwidth[5] (V_{IN} = 2V p-p)	+25°C	I	27	34		MHz
Output Swing	Full	VI	±2			V
Output Current (Sinking @ = 25°C)	+25°C	V		5		mA
Output Resistance	+25°C	IV, V		9	15	Ω
DYNAMIC CHARACTERISTICS						
Slew Rate[6]	+25°C	I	170	215		V/µs
Settling Time (to 0.1% on ±2V Output)	+25°C	IV		70	100	ns
Overshoot						
To T-Step[7]	+25°C	V		<0.1		%
To Pulse[8]	+25°C	V		<10		%
Differential Phase[9]	+25°C	IV		0.03	0.1	°
Differential Gain[9]	+25°C	IV		0.01	0.1	%
Crosstalk Rejection						
Three Channels[10]	+25°C	IV	68	72		dB
One Channel[11]	+25°C	IV	70	76		dB
SWITCHING CHARACTERISTICS[12]						
A_X Input to Channel HIGH Time[13] (t_{HIGH})	+25°C	I		40	50	ns
A_X Input to Channel LOW Time[14] (t_{LOW})	+25°C	I		35	45	ns
Enable to Channel ON Time[15] (t_{ON})	+25°C	I		35	45	ns
Enable to Channel OFF Time[16] (t_{OFF})	+25°C	I		35	45	ns
Switching Transient[17]	+25°C	V		60		mV

EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.
Test Level II – 100% production tested at + 25°C, and sample tested at specified temperatures.
Test Level III – Sample tested only.
Test Level IV – Parameter is guaranteed by design and characterization testing.
Test Level V – Parameter is a typical value only.
Test Level VI – All devices are 100% production tested at + 25°C. 100% production tested at temperature extremes for military temperature devices; sample tested at temperature extremes for commercial/industrial devices.

Parameter (Conditions)	Temp	Test Level	COMMERCIAL 0°C to +70°C AD9300KQ/KP Min	Typ	Max	Units
DIGITAL INPUTS						
Logic "1" Voltage	Full	VI	2			V
Logic "0" Voltage	Full	VI			0.8	V
Logic "1" Current	Full	VI			5	μA
Logic "0" Current	Full	VI			1	μA
POWER SUPPLY						
Positive Supply Current (+12V)	+25°C	I		13	16	mA
Positive Supply Current (+12V)	Full	VI		13	16	mA
Negative Supply Current (−12V)	+25°C	I		12.5	15	mA
Negative Supply Current (−12V)	Full	VI		12.5	16	mA
Power Supply Rejection Ratio ($\pm V_S = \pm 12V \pm 5\%$)	Full	VI	67	75		dB
Power Dissipation (±12V)[18]	+25°C	V		306		mW

NOTES
[1]Permanent damage may occur if any one absolute maximum rating is exceeded. Functional operation is not implied, and device reliability may be impaired by exposure to higher-than-recommended voltages for extended periods of time.
[2]Measured at extremes of temperature range.
[3]Measured as slope of V_{OUT} versus V_{IN} with $V_{IN} = \pm 1V$.
[4]Measured as worst deviation from end-point fit with $V_{IN} = \pm 1V$.
[5]Full Power Bandwith (FPBW) based on Slew Rate (SR). FPBW = $SR/2\pi V_{PEAK}$
[6]Measured between 20% and 80% transition points of ±1V output.
[7]T-Step = Sin^2X Step, when Step between 0V and +700mV points has 10%-to-90% risetime = 125ns.
[8]Measured with a pulse input having slew rate >250V/μs.
[9]Measured at output between 0.28Vdc and 1.0Vdc with V_{IN} = 284mV p–p at 3.58MHz and 4.43MHz.
[10]This specification is critically dependent on circuit layout. Value shown is measured with selected channel grounded and 10MHz 2V p–p signal applied to remaining three channels. If selected channel is grounded through 75Ω, value is approximately 6dB higher.
[11]This specification is critically dependent on circuit layout. Value shown is measured with selected channel grounded and 10MHz 2V p–p signal applied to one other channel. If selected channel is grounded through 75Ω, value is approximately 6dB higher. Minimum specification in ( ) applies to DIPs.
[12]Consult system timing diagram.
[13]Measured from address change to 90% point of −2V to +2V output LOW-to-HIGH transition.
[14]Measured from address change to 90% point of +2V to −2V output HIGH-to-LOW transition.
[15]Measured from 50% transition point of ENABLE input to 90% transition of 0V to −2V and 0V to +2V output.
[16]Measured from 50% transition point of ENABLE input to 10% transition of +2V to 0V and −2V to 0V output.
[17]Measured while switching between two grounded channels.
[18]Maximum power dissipation is a package-dependent parameter related to the following typical thermal impedances:
16-Pin Ceramic θ_{JA} = 87°C/W; θ_{JC} = 25°C/W
20-Pin LCC θ_{JA} = 74°C/W; θ_{JC} = 10°C/W
20-Pin PLCC θ_{JA} = 71°C/W; θ_{JC} = 26°C/W

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±16V
Analog Input Voltage Each Input (IN_1 thru IN_4) . . . . . ±3.5V
Differential Voltage Between Any Two Inputs (IN_1 thru IN_4) 5V
Digital Input Voltages (A_0, A_1, ENABLE) . −0.5V to +5.5V
Output Current
Sinking 6.0mA
Sourcing 6.0mA
Operating Temperature Range
AD9300KQ/KP . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering (10sec) . . . . . +300°C

ORDERING GUIDE

Device	Temperature Range	Description	Package Option[1]
AD9300KQ	0 to +70°C	16-Pin Cerdip, Commercial	Q-16
AD9300TE/883B[2]	−55°C to +125°C	20-Pin LCC, Military Temperature	E-20A
AD9300TQ/883B[2]	−55°C to +125°C	16-Pin Cerdip, Military Temperature	Q-16
AD9300KP	0 to +70°C	20-Pin PLCC, Commercial	P-20A

NOTES
[1]E = Ceramic Leadless Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.

ANALOG DEVICES

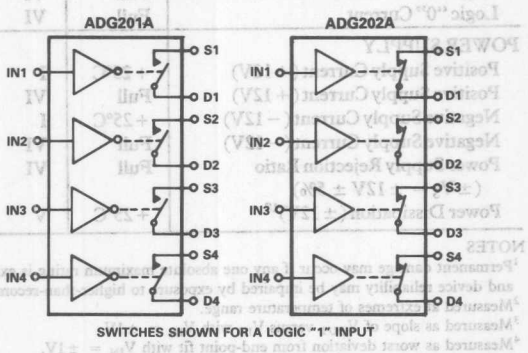
LC²MOS Quad SPST Switches

ADG201A/ADG202A

FEATURES

- 44V Supply Maximum Rating
- ±15V Analog Signal Range
- Low R_{ON} (60Ω)
- Low Leakage (0.5nA)
- Break Before Make Switching
- Extended Plastic Temperature Range (−40°C to +85°C)
- Low Power Dissipation (33mW)
- Available in 16-Lead DIP/ SOIC and 20-Lead PLCC/LCCC Packages
- Superior Second Source:
  - ADG201A Replaces DG201A, HI-201
  - ADG202A Replaces DG202

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG201A and ADG202A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG201A and ADG202A consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range:
   These switches are fabricated on an enhanced LC²MOS process, resulting in high breakdown and an increased analog signal range of ±15V.
2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

(V_{DD} = +15V, V_{SS} = −15V, unless otherwise specified)

Parameter	K Version 25°C	K Version −40°C to +85°C	B Version 25°C	B Version −40°C to +85°C	T Version 25°C	T Version −55°C to +125°C	Units	Test Conditions
ANALOG SWITCH								
Analog Signal Range	±15	±15	±15	±15	±15	±15	Volts	
R_{ON}	60		60		60		Ω typ	−10V≤V_S≤+10V
	90	145	90	145	90	145	Ω max	I_{DS} = 1.0mA
								Test Circuit 1
R_{ON} vs. V_D (V_S)	20		20		20		% typ	
R_{ON} Drift	0.5		0.5		0.5		%/°C typ	
R_{ON} Match	5		5		5		% typ	V_S = 0V, I_{DS} = 1mA
I_S (OFF)	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S ∓14V; Test Circuit 2
OFF Input Leakage	2	100	2	100	1	100	nA max	
I_D (OFF)	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
OFF Output Leakage	2	100	2	100	1	100	nA max	
I_D (ON)	0.5		0.5		0.5		nA typ	V_D = ±14V; Test Circuit 3
ON Channel Leakage	2	200	2	200	1	200	nA max	
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	
DYNAMIC CHARACTERISTICS								
t_{OPEN}	30		30		30		ns typ	
t_{ON}[1]	300		300		300		ns max	Test Circuit 4
t_{OFF}[1]	250		250		250		ns max	Test Circuit 4
OFF Isolation	80		80		80		dB typ	V_S = 10V(p-p); f = 100kHz
								R_L = 75Ω; Test Circuit 6
Channel-to-Channel Crosstalk	80		80		80		dB typ	Test Circuit 7
C_S (OFF)	5		5		5		pF typ	
C_D (OFF)	5		5		5		pF typ	
C_D, C_S (ON)	16		16		16		pF typ	
C_{IN} Digital Input Capacitance	5		5		5		pF typ	
Q_{INJ} Charge Injection	20		20		20		pC typ	R_S = 0Ω; C_L = 1000pF; V_S = 0V
								Test Circuit 5
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}		2		2		2	mA max	
I_{SS}	0.1		0.1		0.1		mA typ	
I_{SS}		0.2		0.2		0.2	mA max	
Power Dissipation		33		33		33	mW max	

NOTES
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to V_{SS} 44V
V_{DD} to GND 25V
V_{SS} to GND . . . . . −25V
Analog Inputs[1]
Voltage at S, D . . . . . V_{SS} −0.3V to V_{DD} +0.3V
Continuous Current, S or D 30mA
Pulsed Current S or D
1ms Duration, 10% Duty Cycle 70mA
Digital Inputs[1]
Voltage at IN . . . . . V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First

Power Dissipation (Any Package)
Up to +75°C 470mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
Commercial (K Version) . . . . . −40°C to +85°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C

NOTE
[1]Overvoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

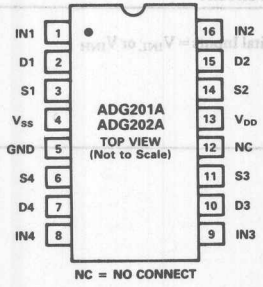
ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG201AKN	−40°C to +85°C	N-16
ADG201AKR	−40°C to +85°C	R-16A
ADG201AKP	−40°C to +85°C	P-20A
ADG201ABQ	−40°C to +85°C	Q-16
ADG201ATQ	−55°C to +125°C	Q-16
ADG201ATE	−55°C to +125°C	E-20A
ADG202AKN	−40°C to +85°C	N-16
ADG202AKR	−40°C to +85°C	R-16A
ADG202AKP	−40°C to +85°C	P-20A
ADG202ABQ	−40°C to +85°C	Q-16
ADG202ATQ	−55°C to +125°C	Q-16
ADG202ATE	−55°C to +125°C	E-20A

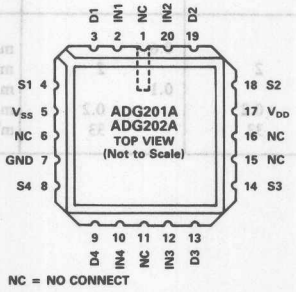
NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers. See Analog Devices Military Products Databook (1990) for military data sheet.
[2]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; E = Leadless Ceramic Chip Carrier (LCCC). For outline information see Package Information section.

PIN CONFIGURATIONS

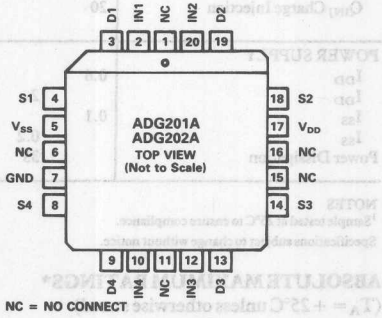
DIP, SOIC



LCCC



PLCC



ADG201A/ADG202A FUNCTIONAL DIAGRAM

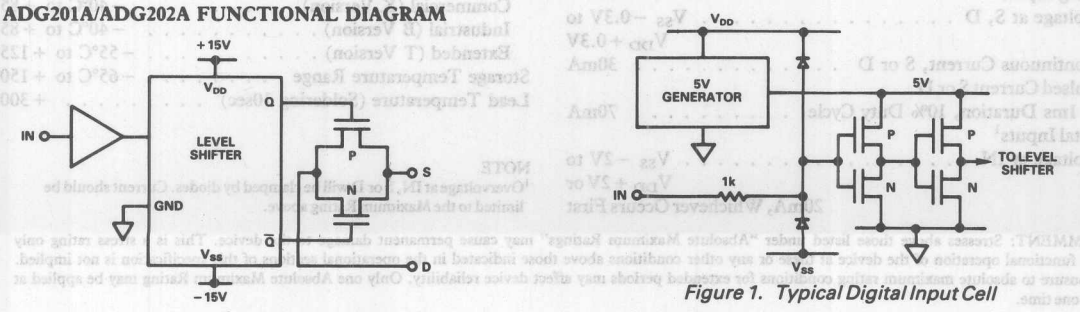
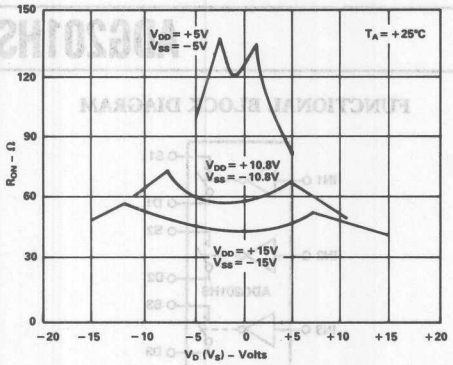


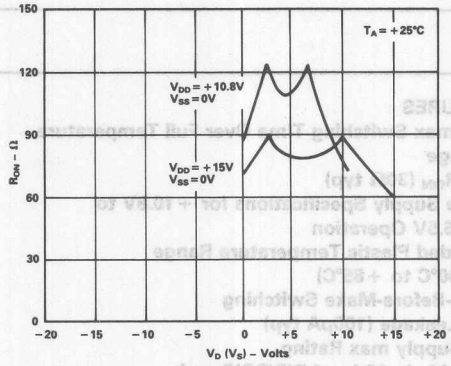
Figure 1. Typical Digital Input Cell

Typical Performance Characteristics

The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.

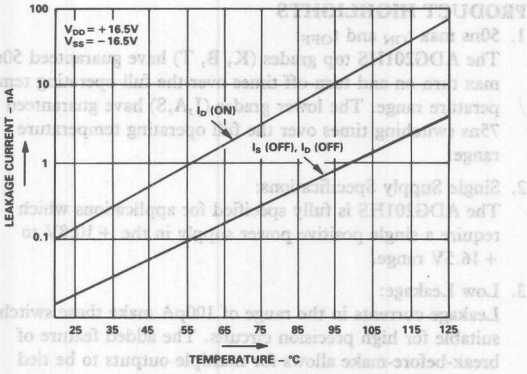


R_{ON} as a Function of V_D (V_S): Dual Supply Voltage

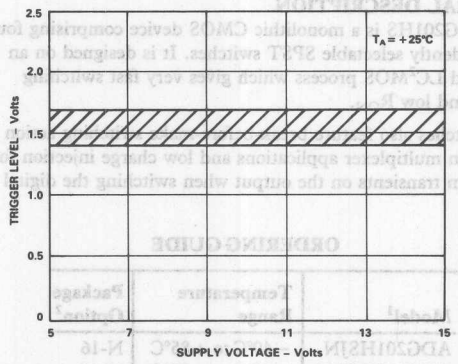


R_{ON} as a Function of V_D (V_S): Single Supply Voltage

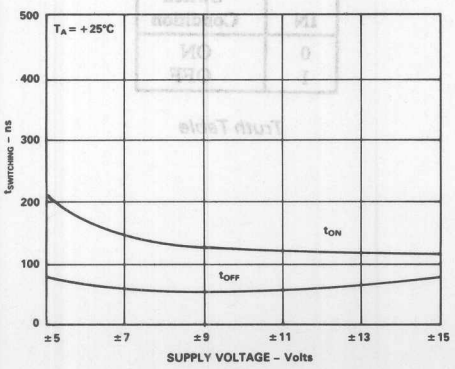
7



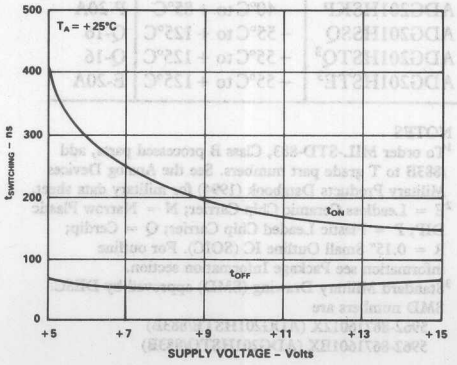
Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



Trigger Level vs. Power Supply Voltage: Dual or Single Supply Voltage



Switching Time vs. Supply Voltage (Dual Supply)



Switching Time vs. Supply Voltage (Single Supply)

ANALOG DEVICES

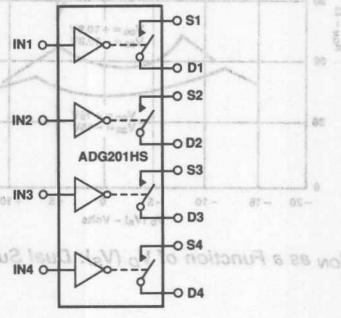
LC²MOS High Speed, Quad SPST Switch

ADG201HS

FEATURES

- 50ns max Switching Time Over Full Temperature Range
- Low R_{ON} (30Ω typ)
- Single Supply Specifications for +10.8V to +16.5V Operation
- Extended Plastic Temperature Range (−40°C to +85°C)
- Break-Before-Make Switching
- Low Leakage (100pA typ)
- 44V Supply max Rating
- Available in 16-Lead DIP/SOIC and 20-Lead LCCC/PLCC Packages
- ADG201HS (K, B, T) Replaces HI-201HS
- ADG201HS (J, A, S) Replaces DG271

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG201HS is a monolithic CMOS device comprising four independently selectable SPST switches. It is designed on an enhanced LC²MOS process which gives very fast switching speeds and low R_{ON}.

The switches also feature break-before-make switching action for use in multiplexer applications and low charge injection for minimum transients on the output when switching the digital inputs.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG201HSJN	−40°C to +85°C	N-16
ADG201HSKN	−40°C to +85°C	N-16
ADG201HSKR	−40°C to +85°C	R-16
ADG201HSAQ	−40°C to +85°C	Q-16
ADG201HSBQ	−40°C to +85°C	Q-16
ADG201HSJP	−40°C to +85°C	P-20A
ADG201HSKP	−40°C to +85°C	P-20A
ADG201HSSQ	−55°C to +125°C	Q-16
ADG201HSTQ[3]	−55°C to +125°C	Q-16
ADG201HSTE[3]	−55°C to +125°C	E-20A

NOTES

[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers. See the Analog Devices Military Products Databook (1994) for military data sheet.

[2]E = Leadless Ceramic Chip Carrier; N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.

[3]Standard Military Drawing (SMD) approved by DESC. SMD numbers are
5962-86716012X (ADG201HSTE/883B)
5962-8671601EX (ADG201HSTQ/883B)

PRODUCT HIGHLIGHTS

1. 50ns max t_{ON} and t_{OFF}:
   The ADG201HS top grades (K, B, T) have guaranteed 50ns max turn-on and turn-off times over the full operating temperature range. The lower grades (J,A,S) have guaranteed 75ns switching times over the full operating temperature range.
2. Single Supply Specifications:
   The ADG201HS is fully specified for applications which require a single positive power supply in the +10.8V to +16.5V range.
3. Low Leakage:
   Leakage currents in the range of 100pA make these switches suitable for high precision circuits. The added feature of break-before-make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

IN	Switch Condition
0	ON
1	OFF

Truth Table

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

DUAL SUPPLY (V_{DD} = +13.5V to +16.5V, = −13.5V to −16.5V, GND = 0V, V_{IN} 3V [Logic High Level] or 0.8 V [Logic Low Level] unless otherwise noted)

Parameter	Version	+25°C	$T_{min}-T_{max}$[1]	Units	Comments
ANALOG SWITCH					
Analog Signal Range	All	V_{SS}	V_{SS}	Vmin	
	All	V_{DD}	V_{DD}	V max	
R_{ON}	All	30	–	Ω typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA; Test Circuit 1
	All	50	75	Ω max	
R_{ON} Drift	All	0.5	–	%/°C typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA
R_{ON} Match	All	3	–	% typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA
I_S (OFF), Off Input Leakage[2]	All	0.1		nA typ	$V_D = \pm 14V$; $V_S = \mp 14V$; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (OFF), Off Output Leakage[2]	All	0.1		nA typ	$V_D = \pm 14V$; $V_S = \mp 14V$; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S,T	1	60	nA max	
I_D (ON), On Channel Leakage[2]	All	0.1		nA typ	$V_D = V_S = \pm 14V$; Test Circuit 3
	J, K, A, B	1	20	nA max	
	S,T	1	60	nA max	
DIGITAL CONTROL					
V_{INH}, Input High Voltage	All	2.4	2.4	V min	
V_{INL}, Input Low Voltage	All	0.8	0.8	V max	
I_{INL} or I_{INH}	All	1	1	μA max	
C_{IN}	All	8	8	pF max	
DYNAMIC CHARACTERISTICS					
t_{ON}	K, B, T	50	50	ns max	Test Circuit 4
	J, A, S	75	75	ns max	
t_{OFF1}	K, B, T	50	50	ns max	Test Circuit 4
	J, A, S	75	75	ns max	
t_{OFF2}	All	150	–	ns typ	Test Circuit 4
t_{OPEN}	All	5	5	ns typ	t_{ON}–t_{OFF1}; Test Circuit 4
Output Settling Time to 0.1%	All	180	–	ns typ	V_{IN} = 3V to 0V; Test Circuit 4
OFF Isolation	All	72	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 5
Channel-to-Channel Crosstalk	All	86	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 6
Q_{INJ}, Charge Injection	All	10	–	pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 7
C_S (OFF)	All	10	–	pF typ	
C_D (OFF)	All	10	–	pF typ	
C_D, C_S (ON)	All	30	–	pF typ	
C_{DS} (OFF)	All	0.5	–	pF typ	
POWER SUPPLY					
I_{DD}	All	10	10	mA max	
I_{SS}	All	6	6	mA max	
Power Dissipation	All	240	240	mW max	V_{DD} = +15V, V_{SS} = −15V

NOTES

[1]Temperature ranges are as follows: ADG201HSJ, K; −40°C to +85°C
ADG201HSA, B; −40°C to +85°C
ADG201HSS, T; −55°C to +125°C

[2]Leakage specifications apply with a V_D (V_S) of ± 14V or with a V_D (V_S) of 0.5V within the supply voltages (V_{DD}, V_{SS}), whichever is the minimum.

Specifications subject to change without notice.

Parameter	Version	+25°C	$T_{min}-T_{max}$	Units	Comments
ANALOG SWITCH					
Analog Signal Range	All	V_{SS}	V_{SS}	V min	
	All	V_{DD}	V_{DD}	V max	
R_{ON}	All	65	–	Ω typ	$0V \leq V_S \leq +10V$, $I_{DS} = 1mA$; Test Circuit 1
	All	90	120	Ω max	
R_{ON} Drift	All	0.5	–	%/°C typ	$0V \leq V_S \leq +10V$, $I_{DS} = 1mA$
R_{ON} Match	All	3	–	% typ	$0V \leq V_S \leq +10V$, $I_{DS} = 1mA$
I_S (OFF), Off Input Leakage[1]	All	0.1		nA typ	$V_D = +10V/+0.5V$; $V_S = +0.5V/+10V$; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (OFF), Off Output Leakage[1]	All	0.1		nA typ	$V_D = +10V/+0.5V$; $V_S = +0.5V/+10V$; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (ON), On Channel Leakage[1]	All	0.1		nA typ	$V_D = V_S = +10V/+0.5V$; Test Circuit 3
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
DIGITAL CONTROL					
V_{INH}, Input High Voltage	All	2.4	2.4	V min	
V_{INL}, Input Low Voltage	All	0.8	0.8	V max	
I_{INL} or I_{INH}	All	1	1	μA max	
C_{IN}	All	8	8	pF max	
DYNAMIC CHARACTERISTICS					
t_{ON}	K, B, T	50	70	ns max	Test Circuit 4
	J, A, S	75	90	ns max	
t_{OFF1}	K, B, T	50	70	ns max	Test Circuit 4
	J, A, S	75	90	ns max	
t_{OFF2}	All	150	–	ns typ	Test Circuit 4
t_{OPEN}	All	5	5	ns typ	$t_{ON}-t_{OFF1}$; Test Circuit 4
Output Settling Time to 0.1%	All	180	–	ns typ	V_{IN} = 3V to 0V; Test Circuit 4
OFF Isolation	All	72	–	dB typ	$V_S = 3V$ rms, f = 100kHz, $R_L = 1k\Omega$; $C_L = 10pF$; Test Circuit 5
Channel-to-Channel Crosstalk	All	86	–	dB typ	$V_S = 3V$ rms, f = 100kHz, $R_L = 1k\Omega$; $C_L = 10pF$; Test Circuit 6
Q_{INJ}, Charge Injection	All	10	–	pC typ	$R_S = 0\Omega$, $V_S = 0V$; Test Circuit 7
C_S (OFF)	All	10	–	pF typ	
C_D (OFF)	All	10	–	pF typ	
C_D, C_S (ON)	All	30	–	pF typ	
C_{DS} (OFF)	All	0.5	–	pF typ	
POWER SUPPLY					
I_{DD}	All	10	10	mA max	
Power Dissipation	All	150	150	mW max	$V_{DD} = +15V$

NOTE
[1]The leakage specifications degrade marginally (typically 1nA at 25°C) with V_D (V_S) = V_{SS}.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS}	44V
V_{DD} to GND	−0.3V, 25V
V_{SS} to GND[1]	+0.3V, −25V
Analog Inputs[2]	
Voltage at S, D	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D	20mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA
Digital Inputs[2]	
Voltage at IN	V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commerical (J, K Version)	−40°C to +85°C
Industrial (A, B Version)	−40°C to +85°C
Extended (S, T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

NOTES

[1]If V_{SS} is open circuited with V_{DD} and GND applied, the V_{SS} pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V_{SS} to GND (cathode end to GND) ensures that the Absolute Maximum Ratings will be observed.

[2]Overvoltage at IN, S or D, will be clamped by diodes. Current should be limited to the maximum rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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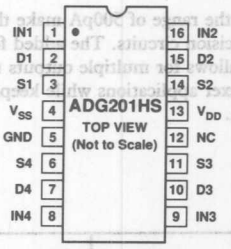
CAUTION:

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

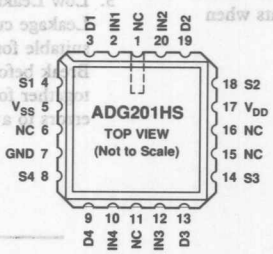
PIN CONFIGURATIONS

DIP, SOIC



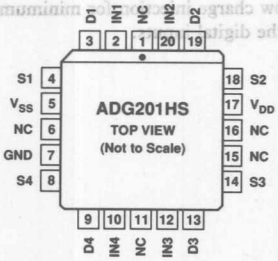
NC = NO CONNECT

LCCC



NC = NO CONNECT

PLCC



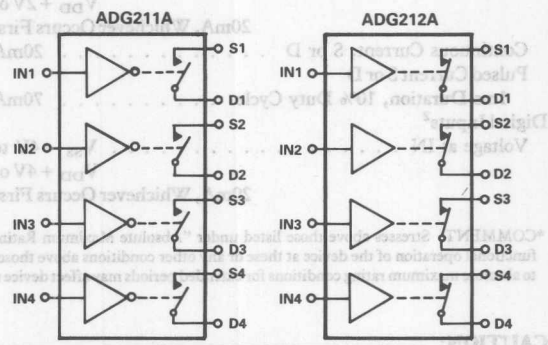
NC = NO CONNECT

ANALOG DEVICES

LC²MOS Quad SPST Switches

ADG211A/ADG212A

FEATURES
44V Supply Maximum Rating
±15V Analog Signal Range
Low R_{ON} (115Ω max)
Low Leakage (0.5nA typ)
Break Before Make Switching
Single Supply Operation Possible
Extended Plastic Temperature Range (−40°C to +85°C)
TTL/CMOS Compatible
Available in 16-Lead DIP/SOIC and 20-Lead PLCC Packages
Superior Second Source:
ADG211A Replaces DG211
ADG212A Replaces DG212



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG211A and ADG212A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG211A and ADG212A consist of four SPST switches. They differ only in that the digital control logic is inverted. In multiplexer applications, all switches exhibit break-before-make switching action when driven simultaneously. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range:
   These switches are fabricated on an enhanced LC²MOS process, resulting in high breakdown and an increased analog signal range of ±15V.
2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

ADG211A IN	ADG212A IN	SWITCH CONDITION
0	1	ON
1	0	OFF

Table I. Truth Table

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

(V_{DD} = +15 V, V_{SS} = −15 V, V_L = 5 V, unless otherwise noted.)

Parameter	ADG211AKN ADG212AKN 25°C	−40°C to +85°C	Units	Test Conditions
ANALOG SWITCH				
Analog Signal Range	±15	±15	Volts	
R_{ON}	115	175	Ωmax	−10V≤V_S≤+10V, I_{DS} = 1mA, Test Circuit 1
R_{ON} vs. V_D (V_S)	20		% typ	
R_{ON} Drift	0.5		%/°C typ	
R_{ON} Match	5		% typ	V_S = 0V, I_{DS} = 1mA
I_S (OFF)	0.5		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
OFF Input Leakage	5	100	nA max	
I_D (OFF)	0.5		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
OFF Output Leakage	5	100	nA max	
I_D (ON)	0.5		nA typ	V_D = V_S = ±14V; Test Circuit 3
ON Channel Leakage	5	200	nA max	
DIGITAL CONTROL				
V_{INH}, Input High Voltage		2.4	V min	TTL Compatibility is Independent of V_L
V_{INL}, Input Low Voltage		0.8	V max	
I_{INL} or I_{INH}		1	μA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS				
t_{OPEN}[1]	30		ns typ	Test Circuit 4
t_{ON}[1]	600		ns max	Test Circuit 5
t_{OFF}[1]	450		ns max	Test Circuit 5
OFF Isolation	80		dB typ	V_S = 10V(p-p); f = 100kHz R_L = 75Ω; Test Circuit 6
Channel-to-Channel Crosstalk	80		dB typ	Test Circuit 7
C_S (OFF)	5		pF typ	
C_D (OFF)	5		pF typ	
C_S, C_D (ON)	16		pF typ	
Q_{INJ}, Charge Injection	20		pC typ	R_S = 0Ω; C_L = 1000pF; V_S = 0V Test Circuit 8
POWER SUPPLY				
I_{DD}	0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}	1		mA max	
I_{SS}	0.1		mA typ	
I_{SS}	0.2		mA max	
I_L	0.9		mA max	

NOTE

[1]Sample tested at 25°C to ensure compliance.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise stated)

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	−25V
V_L to GND	−0.3V, 25V
Analog Inputs[1]	
Voltage at S, D	V_{SS} −0.3V to V_{DD} +0.3V
Continuous Current, S or D	30mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA
Digital Inputs[1]	
Voltage at IN	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

NOTE

[1]Overvoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

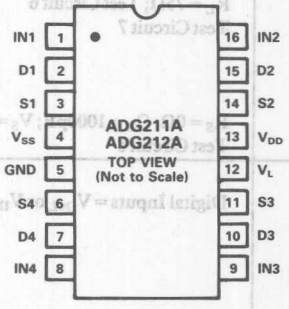
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

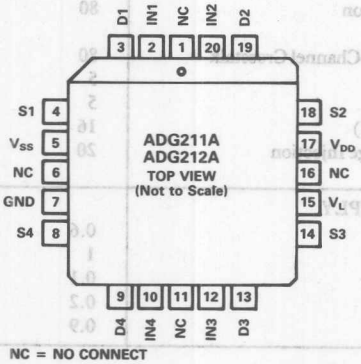
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

DIP, SOIC



PLCC



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG211AKN	−40°C to +85°C	N-16
ADG211AKR	−40°C to +85°C	R-16A
ADG211AKP	−40°C to +85°C	P-20A
ADG212AKN	−40°C to +85°C	N-16
ADG212AKR	−40°C to +85°C	R-16A
ADG212AKP	−40°C to +85°C	P-20A

*N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

Typical Performance Characteristics

The switches can comfortably operate anywhere in the 10V to 15V single or dual supply range, with only a slight degradation in performance. The following graphs show the relevant performance curves. The test circuits and test conditions are given in a following section, "Test Circuits."

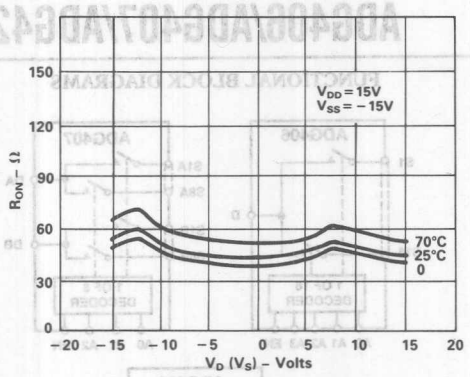


Figure 1. R_{ON} as a Function of V_D (V_S): Dual ± 15 Supplies

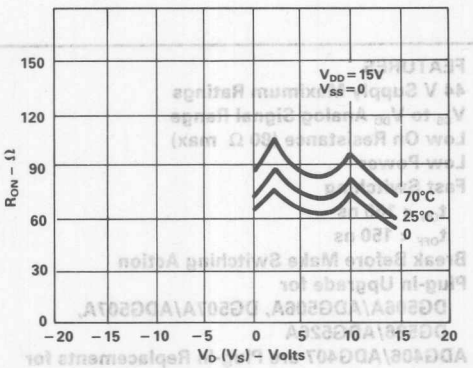


Figure 2. R_{ON} as a Function of V_D (V_S): Single + 15V Supply

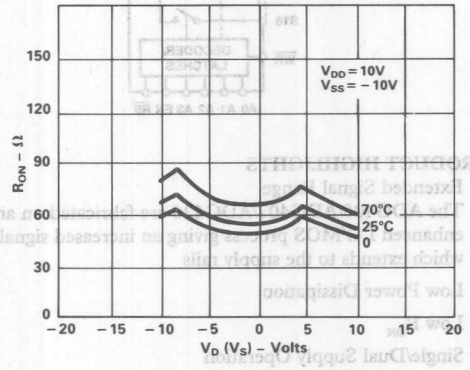


Figure 3. R_{ON} as a Function of V_D (V_S): Dual ± 10V Supplies

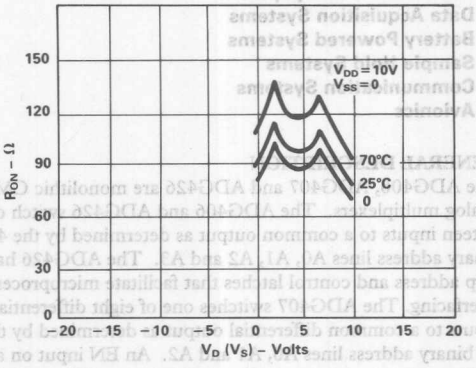


Figure 4. R_{ON} as a Function of V_D (V_S): Single + 10V Supply

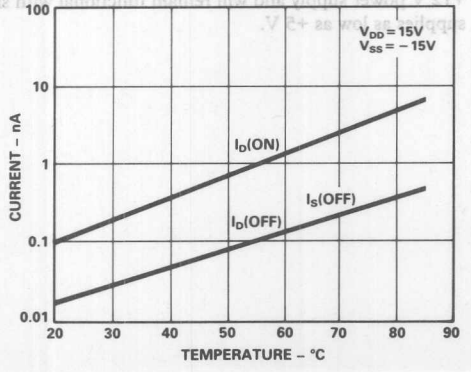


Figure 5. Leakage Current as a Function of Temperature (Note: Leakage Current Reduces as the Supply Voltages Reduce)

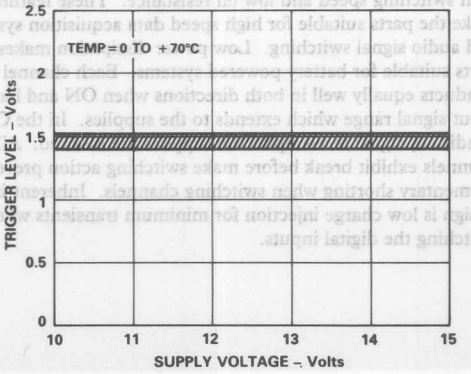


Figure 6. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply Voltage

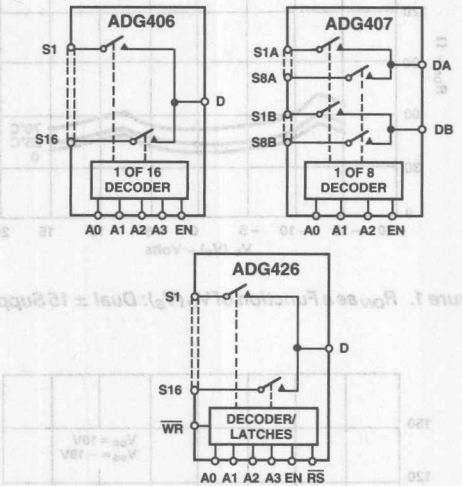
FEATURES

- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (80 Ω max)
- Low Power
- Fast Switching
  - t_{ON} < 160 ns
  - t_{OFF} < 150 ns
- Break Before Make Switching Action
- Plug-In Upgrade for DG506A/ADG506A, DG507A/ADG507A, DG526/ADG526A
- ADG406/ADG407 are Plug-In Replacements for DG406/DG407

APPLICATIONS

- Audio and Video Routing
- Automatic Test Equipment
- Data Acquisition Systems
- Battery Powered Systems
- Sample Hold Systems
- Communication Systems
- Avionics

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG406, ADG407 and ADG426 are monolithic CMOS analog multiplexers. The ADG406 and ADG426 switch one of sixteen inputs to a common output as determined by the 4-bit binary address lines A0, A1, A2 and A3. The ADG426 has on-chip address and control latches that facilitate microprocessor interfacing. The ADG407 switches one of eight differential inputs to a common differential output as determined by the 3-bit binary address lines A0, A1 and A2. An EN input on all devices is used to enable or disable the device. When disabled, all channels are switched OFF.

The ADG406/ADG407/ADG426 are designed on an enhanced LC^2MOS process that provides low power dissipation yet gives high switching speed and low on resistance. These features make the parts suitable for high speed data acquisition systems and audio signal switching. Low power dissipation makes the parts suitable for battery powered systems. Each channel conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break before make switching action preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG406/ADG407/ADG426 are fabricated on an enhanced LC^2MOS process giving an increased signal range which extends to the supply rails
2. Low Power Dissipation
3. Low R_{ON}
4. Single/Dual Supply Operation
5. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG406/ADG407/ADG426 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter	+25°C	−40°C to +85°C	+25°C	−55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	50		50		Ω typ	V_D = ±10 V, I_S = −1 mA
	80	125	80	125	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
R_{ON} Match	4		4		Ω typ	V_D = 0 V, I_S = −1 mA
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source OFF Leakage I_S (OFF)	±0.5	±20	±0.5	±50	nA max	V_D = ±10 V, V_S = ∓10 V, Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = ±10 V, V_S = ∓10 V;
ADG406, ADG426	±1	±20	±1	±200	nA max	Test Circuit 3
ADG407	±1	±20	±1	±100	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = ±10 V;
ADG406, ADG426	±1	±20	±1	±200	nA max	Test Circuit 4
ADG407	±1	±20	±1	±100	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±1		±1	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	120		120		ns typ	R_L = 300 Ω, C_L = 35 pF;
	150	250	150	250	ns max	V_1 = ±10 V, V_2 = ∓10 V;
						Test Circuit 5
Break Before Make Delay, t_{OPEN}	10	10	10	10	ns min	R_L = 300 Ω, C_L = 35 pF;
						V_S = +5 V, Test Circuit 6
t_{ON} (EN, $\overline{WR}$)	120	175	120	175	ns typ	R_L = 300 Ω, C_L = 35 pF;
	160	225	160	225	ns max	V_S = +5 V, Test Circuit 7
t_{OFF} (EN, $\overline{RS}$)	110	130	110	130	ns typ	R_L = 300 Ω, C_L = 35 pF;
	150	180	150	180	ns max	V_S = +5 V, Test Circuit 7
ADG426 Only						
t_W, Write Pulse Width		100		100	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulse Width		100		100	ns min	V_S = +5 V
Charge Injection	8		8		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF;
						Test Circuit 10
OFF Isolation	−75		−75		dB typ	R_L = 1 kΩ, f = 100 kHz;
						V_{EN} = 0 V, Test Circuit 11
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, f = 100 kHz, Test Circuit 12
C_S (OFF)	5		5		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG406, ADG426	50		50		pF typ	
ADG407	25		25		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG406, ADG426	60		60		pF typ	
ADG407	40		40		pF typ	
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}		1		1	μA typ	V_{IN} = 0 V, V_{EN} = 0 V
		5		5	μA max	
I_{SS}		1		1	μA typ	
		5		5	μA max	
I_{DD}	100		100		μA typ	V_{IN} = 0 V, V_{EN} = 2.4 V
	200	500	200	500	μA max	
I_{SS}		1		1	μA typ	
		5		5	μA max	

NOTES

[1] Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.

[2] Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY (V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version −40°C to +85°C	T Version +25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	90		90		Ω typ	V_D = +3 V, +8.5 V, I_S = −1 mA;
	125	200	125	200	Ω max	V_{DD} = +10.8 V
LEAKAGE CURRENTS						V_{DD} = +13.2 V
Source OFF Leakage I_S (OFF)	±0.5	±20	±0.5	±50	nA max	V_D = 8 V/0.1 V, V_S = 0.1 V/8 V; Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = 8 V/0.1 V, V_S = 0.1 V/8 V;
ADG406, ADG426	±1	±20	±1	±200	nA max	Test Circuit 3
ADG407	±1	±20	±1	±100	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = 8 V/0.1 V, Test Circuit 4
ADG406, ADG426	±1	±20	±1	±200	nA max	
ADG407	±1	±20	±1	±100	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±1		±1	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	180		180		ns typ	R_L = 300 Ω, C_L = 35 pF;
	220	350	220	350	ns max	V_1 = 8 V/0 V, V_2 = 0 V/8 V; Test Circuit 5
Break Before Make Delay, t_{OPEN}	10		10		ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = +5 V, Test Circuit 6
t_{ON} (EN, $\overline{WR}$)	180		180		ns typ	R_L = 300 Ω, C_L = 35 pF;
	240	350	240	350	ns max	V_S = +5 V, Test Circuit 7
t_{OFF} (EN, $\overline{RS}$)	135		135		ns typ	R_L = 300 Ω, C_L = 35 pF;
	180	220	180	220	ns max	V_S = +5 V, Test Circuit 7
ADG426 Only						
t_W, Write Pulse Width		100		100	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulse Width		100		100	ns min	V_S = +5 V
Charge Injection	5		5		pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 10
OFF Isolation	−75		−75		dB typ	R_L = 1 kΩ, f = 100 kHz; Test Circuit 11
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, f = 100 kHz; Test Circuit 12
C_S (OFF)	8		8		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG406, ADG426	80		80		pF typ	
ADG407	40		40		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG406, ADG426	100		100		pF typ	
ADG407	50		50		pF typ	
POWER REQUIREMENTS						V_{DD} = +13.2 V
I_{DD}		1		1	μA typ	V_{IN} = 0 V, V_{EN} = 0 V
		5		5	μA max	
I_{DD}	100		100		μA typ	V_{IN} = 0 V, V_{EN} = 2.4 V
	200	500	200	500	μA max	

NOTES

[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} ..... +44 V
V_{DD} to GND ..... –0.3 V to +25 V
V_{SS} to GND ..... +0.3 V to –25 V
Analog, Digital Inputs[2] ..... V_{SS} – 2 V to V_{DD} + 2 V
or 20 mA, Whichever Occurs First
Continuous Current, S or D ..... 20 mA
Peak Current, S or D ..... 40 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Extended (T Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic Package
θ_{JA}, Thermal Impedance ..... 75°C/W
Lead Temperature, Soldering (10 sec) ..... +260°C
PLCC Package
θ_{JA}, Thermal Impedance ..... 80°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
SSOP Package
θ_{JA}, Thermal Impedance ..... 122°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at A, S, D, $\overline{WR}$ or $\overline{RS}$ will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG406BN	–40°C to +85°C	N-28
ADG406BP	–40°C to +85°C	P-28A
ADG407BN	–40°C to +85°C	N-28
ADG407BP	–40°C to +85°C	P-28A
ADG426BN	–40°C to +85°C	N-28
ADG426BRS	–40°C to +85°C	RS-28

*N = Plastic DIP, P = Plastic Leaded Chip Carrier (PLCC), RS = Shrink Small Outline Package (SSOP). For outline information see Package Information section.

7

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

A3	A2	A1	A0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

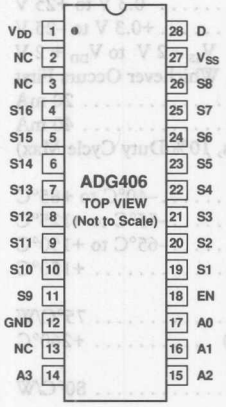
Table II. Truth Table (ADG407)

A2	A1	A0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

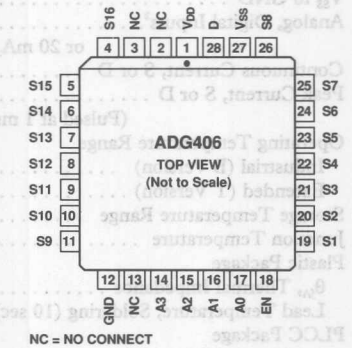
Table III. Truth Table (ADG426)

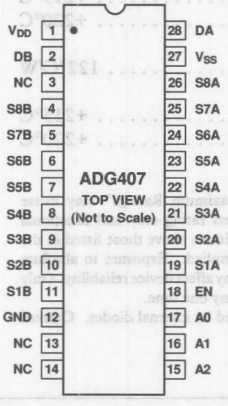
A3	A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X	X	↓	1	Retains Previous Switch Condition
X	X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	X	0	0	1	NONE
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

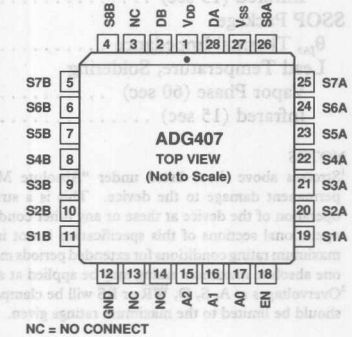
DIP



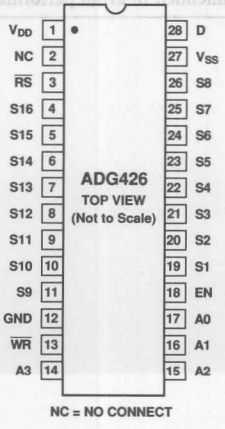
PLCC







PIN CONFIGURATION
DIP/SSOP



TIMING DIAGRAMS (ADG426)

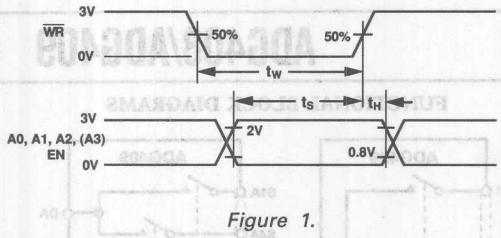


Figure 1.

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

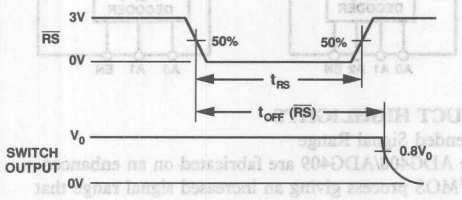


Figure 2.

Figure 2 shows the Reset Pulse Width, t_{RS}, and the Reset Turn Off Time, t_{OFF} ($\overline{RS}$).

Note: All digital input signals rise and fall times are measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to ground.
GND	Ground (0 V) reference.
R_{ON}	Ohmic resistance between D and S.
R_{ON} Match	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current when the switch is off.
I_D (OFF)	Drain leakage current when the switch is off.
I_D, I_S (ON)	Channel leakage current when the switch is on.
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	Channel input capacitance for "OFF" condition.
C_D (OFF)	Channel output capacitance for "OFF" condition.
C_D, C_S (ON)	"ON" switch capacitance.
C_{IN}	Digital input capacitance.
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition.
t_{OFF} (EN)	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
t_{OPEN}	"OFF" time measured between 80% points of both switches when switching from one address state to another.
V_{INL}	Maximum input voltage for logic "0."
V_{INH}	Minimum input voltage for logic "1."
I_{INL} (I_{INH})	Input current of the digital input.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

7

LC²MOS 4/8 Channel High Performance Analog Multiplexers

ADG408/ADG409

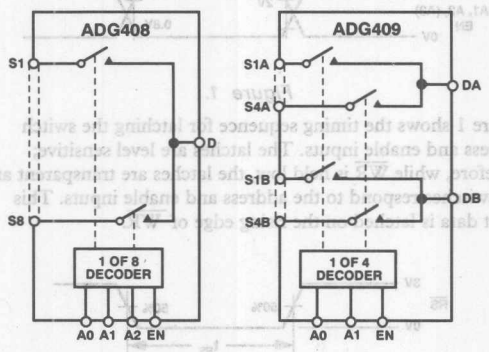
FEATURES

- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (100 Ω max)
- Low Power ($I_{SUPPLY} < 75$ μA)
- Fast Switching
- Break-Before-Make Switching Action
- Plug-in Replacement for DG408/DG409

APPLICATIONS

- Audio and Video Routing
- Automatic Test Equipment
- Data Acquisition Systems
- Battery Powered Systems
- Sample and Hold Systems
- Communication Systems

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG408 and ADG409 are monolithic CMOS analog multiplexers comprising 8 single channels and four differential channels respectively. The ADG408 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG409 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF.

The ADG408/ADG409 are designed on an enhanced LC²MOS process which provides low power dissipation yet gives high switching speed and low on resistance. Each channel conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break before make switching action preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

The ADG408/ADG409 are improved replacements for the DG408/DG409 Analog Multiplexers.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG408/ADG409 are fabricated on an enhanced LC²MOS process giving an increased signal range that extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG408/ADG409 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

DUAL SUPPLY[1] (V_{DD} = +15 V, V_{SS} = −15 V, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version −40°C to +85°C	T Version +25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	40		40		Ω typ	V_D = ±10 V, I_S = −10 mA
	100	125	100	125	Ω max	
ΔR_{ON}	15		15		Ω max	V_D = +10 V, −10 V
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	±0.5	±50	±0.5	±50	nA max	V_D = ±10 V, V_S = ∓10 V; Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = ±10 V; V_S = ∓10 V;
ADG408	±1	±100	±1	±100	nA max	Test Circuit 3
ADG409	±1	±50	±1	±50	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = ±10 V;
ADG408	±1	±100	±1	±100	nA max	Test Circuit 4
ADG409	±1	±50	±1	±50	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±10		±10	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$		120		120	ns typ	R_L = 300 Ω, C_L = 35 pF;
		250		250	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V; Test Circuit 5
t_{OPEN}	10	10	10	10	ns min	R_L = 300 Ω, C_L = 35 pF; V_S = +5 V; Test Circuit 6
t_{ON} (EN)	85	125	85	125	ns typ	R_L = 300 Ω, C_L = 35 pF;
	150	225	150	225	ns max	V_S = +5 V; Test Circuit 7
t_{OFF} (EN)		65		65	ns typ	R_L = 300 Ω, C_L = 35 pF;
		150		150	ns max	V_S = +5 V; Test Circuit 7
Charge Injection	20		20		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 8
OFF Isolation	−75		−75		dB typ	R_L = 1 kΩ, f = 100 kHz; V_{EN} = 0 V; Test Circuit 9
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, f = 100 kHz; Test Circuit 10
C_S (OFF)	11		11		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG408	40		40		pF typ	
ADG409	20		20		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG408	54		54		pF typ	
ADG409	34		34		pF typ	
POWER REQUIREMENTS						
I_{DD}		1		1	μA typ	V_{IN} = 0 V, V_{EN} = 0 V
		5		5	μA max	
I_{SS}		1		1	μA typ	
		5		5	μA max	
I_{DD}	100		100		μA typ	V_{IN} = 0 V, V_{EN} = 2.4 V
	200	500	200	500	μA max	

NOTES

[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY[1] (V_{DD} = +12 V, V_{SS} = 0 V, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version −40°C to +85°C	T Version +25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	90		90		Ω typ	V_D = +3 V, +10 V, I_S = −1 mA
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	±0.5	±50	±0.5	±50	nA max	V_D = 8 V/0 V, V_S = 0 V/8 V; Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = 8 V/0 V, V_S = 0 V/8 V;
ADG408	±1	±100	±1	±100	nA max	Test Circuit 3
ADG409	±1	±50	±1	±50	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = 8 V/0 V;
ADG408	±1	±100	±1	±100	nA max	Test Circuit 4
ADG409	±1	±50	±1	±50	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±10		±10	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	130		130		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = 8 V/0 V, V_{S8} = 0 V/8 V; Test Circuit 5
t_{OPEN}	10		10		ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = +5 V; Test Circuit 6
t_{ON} (EN)	140		140		ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = +5 V; Test Circuit 7
t_{OFF} (EN)	60		60		ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = +5 V; Test Circuit 7
Charge Injection	5		5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 8
OFF Isolation	−75		−75		dB typ	R_L = 1 kΩ, f = 100 kHz; V_{EN} = 0 V; Test Circuit 9
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, f = 100 kHz; Test Circuit 10
C_S (OFF)	11		11		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG408	40		40		pF typ	
ADG409	20		20		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG408	54		54		pF typ	
ADG409	34		34		pF typ	
POWER REQUIREMENTS						
I_{DD}		1		1	μA typ	V_{IN} = 0 V, V_{EN} = 0 V
		5		5	μA max	
I_{DD}	100		100		μA typ	V_{IN} = 0 V, V_{EN} = 2.4 V
	200	500	200	500	μA max	

NOTES
[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . . +44 V
V_{DD} to GND . . . . . −0.3 V to +25 V
V_{SS} to GND . . . . . +0.3 V to −25 V
Analog, Digital Inputs[2] . . . V_{SS} −2 V to V_{DD} +2 V or 20 mA, Whichever Occurs First
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle max) . . . . . 40 mA
Operating Temperature Range
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +150°C
Cerdip Package, Power Dissipation . . . . . 900 mW
θ_{JA}, Thermal Impedance . . . . . 76°C/W
Lead Temperature, Soldering (10 sec) . . . . . +300°C
Plastic Package, Power Dissipation . . . . . 470 mW
θ_{JA}, Thermal Impedance . . . . . 117°C/W
Lead Temperature, Soldering (10 sec) . . . . . +260°C
SOIC Package, Power Dissipation . . . . . 600 mW
θ_{JA}, Thermal Impedance . . . . . 77°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at A, EN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING INFORMATION

Model[1]	Temperature Range	Package Option[2]
ADG408BN	−40°C to +85°C	N-16
ADG408BR	−40°C to +85°C	R-16A
ADG408TQ	−55°C to +125°C	Q-16
ADG409BN	−40°C to +85°C	N-16
ADG409BR	−40°C to +85°C	R-16A
ADG409TQ	−55°C to +125°C	Q-16

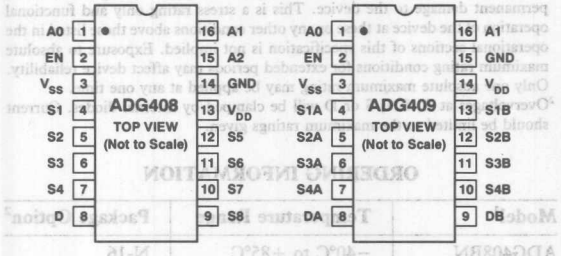
NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); Q = Cerdip. For outline information see Package Information section.

7

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS (DIP/SOIC)



ADG408 Truth Table

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

ADG409 Truth Table

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to ground.
GND	Ground (0 V) reference.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current when the switch is off.
I_D (OFF)	Drain leakage current when the switch is off.
I_D, I_S (ON)	Channel leakage current when the switch is on.
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	Channel input capacitance for "OFF" condition.
C_D (OFF)	Channel output capacitance for "OFF" condition.
C_D, C_S (ON)	"ON" switch capacitance.
C_{IN}	Digital input capacitance.
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition.
t_{OFF} (EN)	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
t_{OPEN}	"OFF" time measured between the 80% points of both switches when switching from one address state to another.
V_{INL}	Maximum input voltage for logic "0."
V_{INH}	Minimum input voltage for logic "1."
I_{INL} (I_{INH})	Input current of the digital input.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

Typical Performance Characteristics

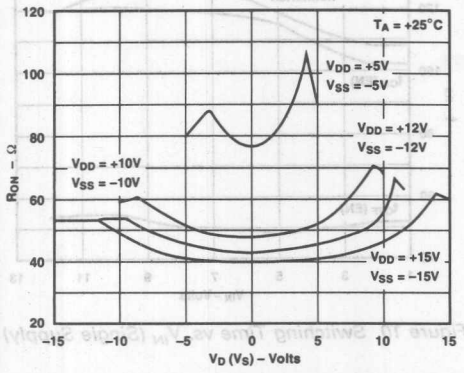


Figure 1. R_{ON} as a Function of V_D (V_S): Dual Supply Voltage

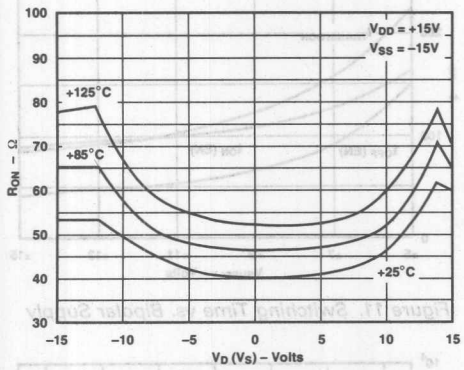


Figure 2. R_{ON} as a Function of V_D (V_S) for Different Temperatures

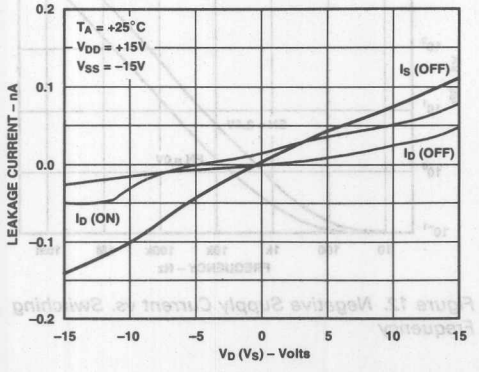


Figure 3. Leakage Currents as a Function of V_D (V_S)

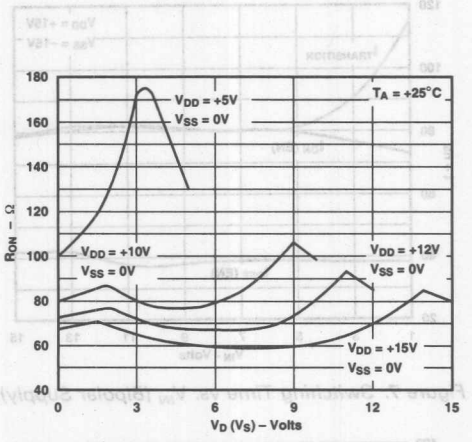


Figure 4. R_{ON} as a Function of V_D (V_S): Single Supply Voltage

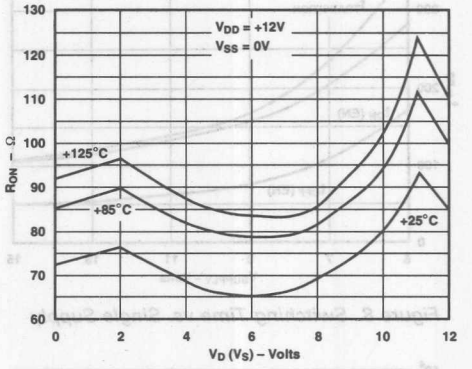


Figure 5. R_{ON} as a Function of V_D (V_S) for Different Temperatures

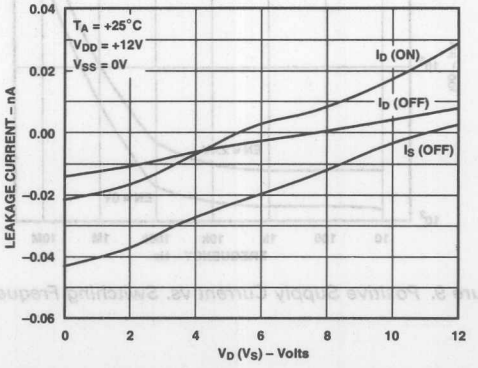


Figure 6. Leakage Currents as a Function of V_D (V_S)

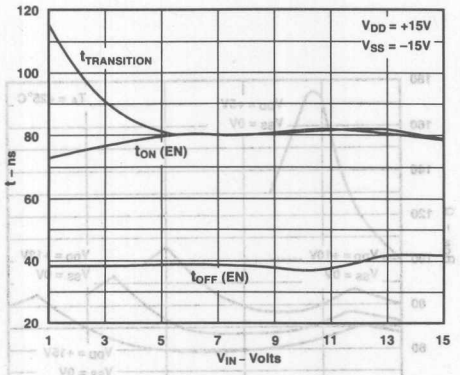


Figure 7. Switching Time vs. V_{IN} (Bipolar Supply)

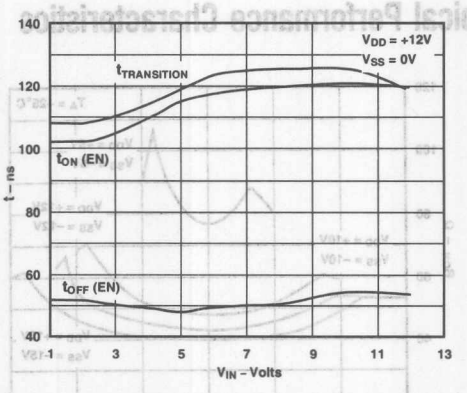


Figure 10. Switching Time vs. V_{IN} (Single Supply)

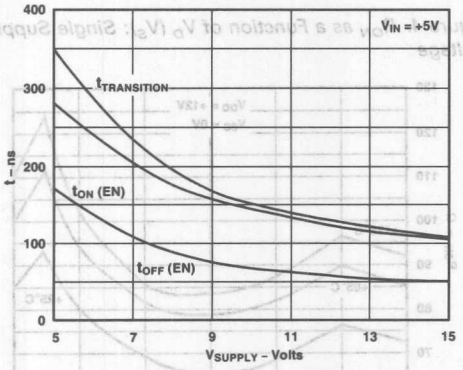


Figure 8. Switching Time vs. Single Supply

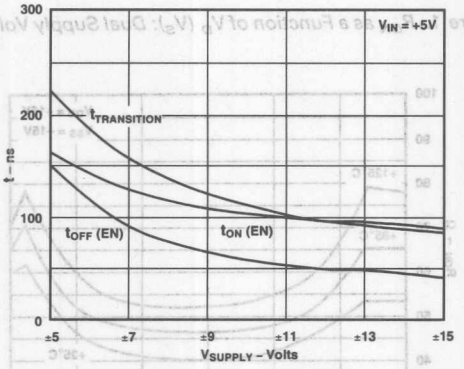


Figure 11. Switching Time vs. Bipolar Supply

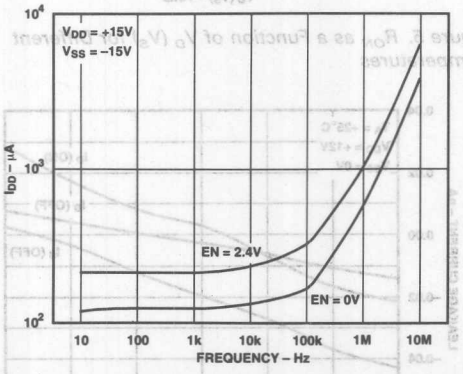


Figure 9. Positive Supply Current vs. Switching Frequency

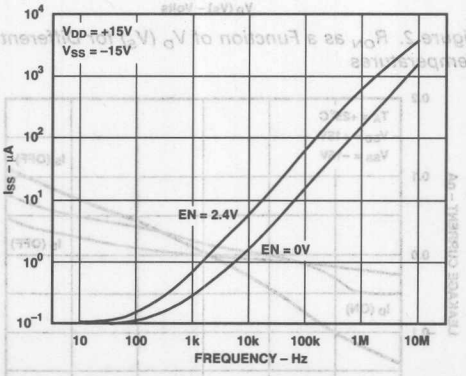


Figure 12. Negative Supply Current vs. Switching Frequency

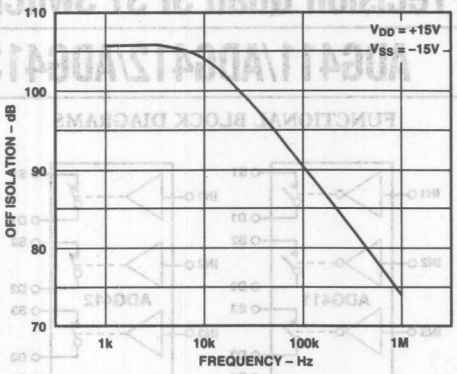


Figure 13. Off Isolation vs. Frequency

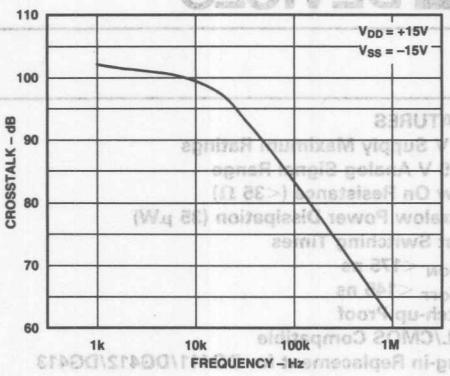
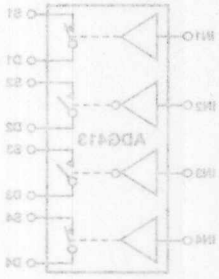


Figure 14. Crosstalk vs. Frequency



FEATURES
44 V Supply Maximum Ratings
±15 V Analog Signal Range
Low On Resistance (<35 Ω)
Ultralow Power Dissipation (35 μW)
Fast Switching Times
t_{ON} <175 ns
t_{OFF} <145 ns
Latch-up Proof
TTL/CMOS Compatible
Plug-in Replacement for DG411/DG412/DG413

APPLICATIONS
Audio and Video Switching
Automatic Test Equipment
Precision Data Acquisition
Battery Powered Systems
Sample Hold Systems
Communication Systems

GENERAL DESCRIPTION

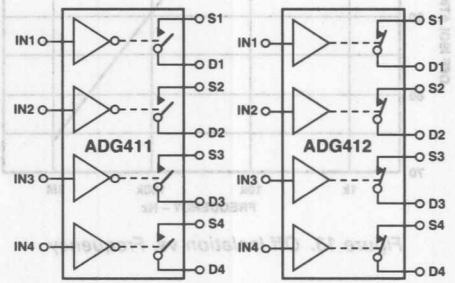
The ADG411, ADG412 and ADG413 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS, trench isolated process which provides low power dissipation yet gives high switching speed and low on resistance. Trench isolation gives all the benefits of dielectric isolation and ensures no latch up even under extreme overvoltage conditions.

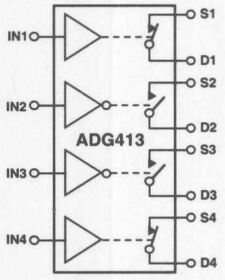
The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG411, ADG412 and ADG413 contain four independent SPST switches. The ADG411 and ADG412 differ only in that the digital control logic is inverted. The ADG411 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG412. The ADG413 has two switches with digital control logic similar to that of the ADG411 while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break before make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

FUNCTIONAL BLOCK DIAGRAMS





SWITCHES SHOWN FOR A LOGIC "1" INPUT

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG411, ADG412 and ADG413 are fabricated on an enhanced LC²MOS, trench isolated process giving an increased signal range which extends fully to the supply rails.
2. Ultralow Power Dissipation
3. Low R_{ON}
4. Trench Isolation Guards Against Latch-up
   A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
5. Break Before Make Switching
   This prevents channel shorting when the switches are configured as a multiplexer.
6. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG411, ADG412 and ADG413 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version −40°C to +85°C	T Version +25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{DD} to V_{SS}		V_{DD} to V_{SS}	V	
R_{ON}	25		25		Ω typ	V_D = ±8.5 V, I_S = −10 mA;
	35	45	35	45	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±20	±0.25	±20	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±20	±0.25	±20	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		±0.1		nA typ	V_D = V_S = ±15.5 V;
	±0.4	±40	±0.4	±40	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	μA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	110		110		ns typ	R_L = 300 Ω, C_L = 35 pF;
		175		175	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	100		100		ns typ	R_L = 300 Ω, C_L = 35 pF;
		145		145	ns max	V_S = ±10 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG413 Only)	25		25		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +10 V; Test Circuit 5
Charge Injection	5		5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		0.0001		μA typ	
	1	5	1	5	μA max	
I_{SS}	0.0001		0.0001		μA typ	
	1	5	1	5	μA max	
I_L	0.0001		0.0001		μA typ	
	1	5	1	5	μA max	

NOTES
[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

Single Supply (V_{DD} = +12 V ± 10%, V_{SS} = 0 V, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version −40°C to +85°C	T Version +25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
Analog Signal Range		0 V to V_{DD}		0 V to V_{DD}	V	
R_{ON}	40		40		Ω typ	0 < V_D < 8.5 V, I_S = −10 mA;
	80	100	80	100	Ω max	V_{DD} = +10.8 V
LEAKAGE CURRENTS						V_{DD} = +13.2 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = 12.2/1 V, V_S = 1/12.2 V;
	±0.25	±20	±0.25	±20	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = 12.2/1 V, V_S = 1/12.2 V;
	±0.25	±20	±0.25	±20	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		±0.1		nA typ	V_D = V_S = +12.2 V/+1 V;
	±0.4	±40	±0.4	±40	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	μA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	175		175		ns typ	R_L = 300 Ω, C_L = 35 pF;
		250		250	ns max	V_S = +8 V; Test Circuit 4
t_{OFF}	95		95		ns typ	R_L = 300 Ω, C_L = 35 pF;
		125		125	ns max	V_S = +8 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG413 Only)	25		25		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +10 V; Test Circuit 5
Charge Injection	25		25		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +13.2 V
						Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		0.0001		μA typ	
	1	5	1	5	μA max	
I_L	0.0001		0.0001		μA typ	
	1	5	1	5	μA max	V_L = +5.25 V

NOTES
[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Truth Table (ADG411/ADG412)

ADG411 In	ADG412 In	Switch Condition
0	1	ON
1	0	OFF

Truth Table (ADG413)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . . +44 V
V_{DD} to GND . . . . . −0.3 V to +25 V
V_{SS} to GND . . . . . +0.3 V to −25 V
V_L to GND . . . . . −0.3 V to V_{DD} + 0.3 V
Analog, Digital Inputs[2] . . . . . V_{SS} −2 V to V_{DD} +2 V or 30 mA, whichever occurs first
Continuous Current, S or D . . . . . 30 mA
Peak Current, S or D . . . . . 100 mA
(Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +150°C
Cerdip Package, Power Dissipation . . . . . 900 mW
θ_{JA} Thermal Impedance . . . . . 76°C/W
Lead Temperature, Soldering (10 sec) . . . . . +300°C
Plastic Package, Power Dissipation . . . . . 470 mW
θ_{JA} Thermal Impedance . . . . . 117°C/W
Lead Temperature, Soldering (10 sec) . . . . . +260°C
SOIC Package, Power Dissipation . . . . . 600 mW
θ_{JA} Thermal Impedance . . . . . 77°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

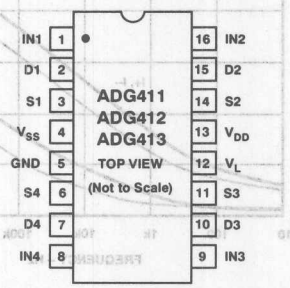
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

7

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper precautions are recommended to avoid any performance degradation or loss of functionality.

PIN CONFIGURATION (DIP/SOIC)



ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2, 3]
ADG411BN	−40°C to +85°C	N-16
ADG411BR	−40°C to +85°C	R-16A
ADG411TQ	−55°C to +125°C	Q-16
ADG412BN	−40°C to +85°C	N-16
ADG412BR	−40°C to +85°C	R-16A
ADG412TQ	−55°C to +125°C	Q-16
ADG413BN	−40°C to +85°C	N-16
ADG413BR	−40°C to +85°C	R-16A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); Q = Cerdip.
[3]For outline information see Package Information section.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
V_L	Logic power supply (+5 V).
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
R_{ON}	Ohmic resistance between D and S.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" switch source capacitance.
C_D (OFF)	"OFF" switch drain capacitance.
C_D, C_S (ON)	"ON" switch capacitance.

t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_D	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.

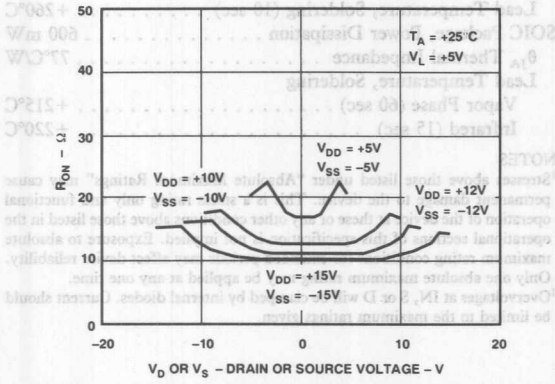


Figure 1. On Resistance as a Function of V_D (V_S) Dual Supplies

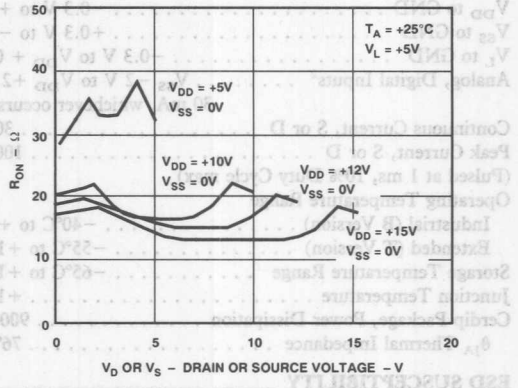


Figure 4. On Resistance as a Function of V_D (V_S) Single Supply

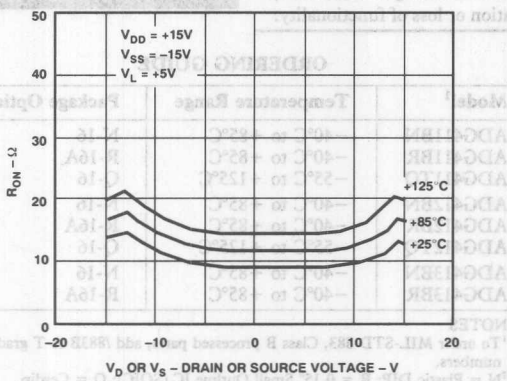


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures

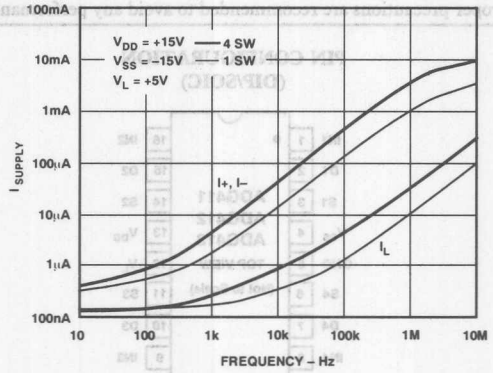


Figure 5. Supply Current vs. Input Switching Frequency

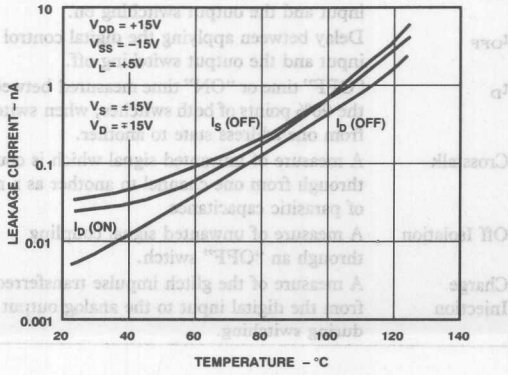


Figure 3. Leakage Currents as a Function of Temperature

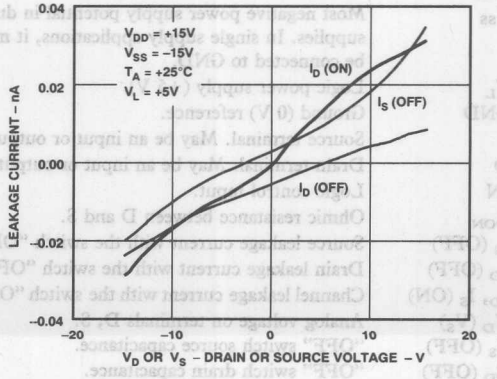


Figure 6. Leakage Currents as a Function of V_D (V_S)

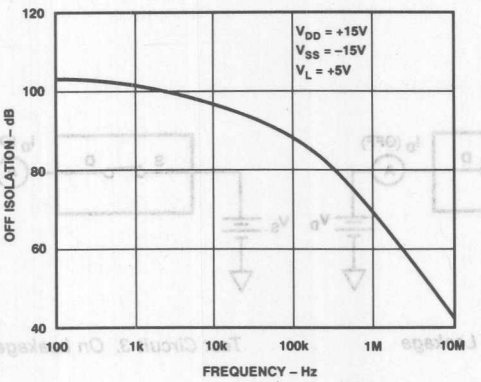


Figure 7. Off Isolation vs. Frequency

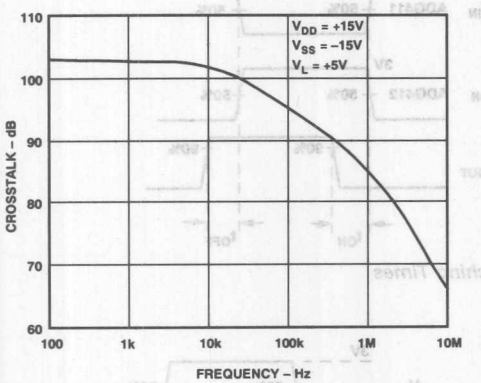


Figure 8. Crosstalk vs. Frequency

TRENCH ISOLATION

In the ADG411, ADG412 and ADG413, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in Junction Isolated switches, are eliminated, the result being a completely latch-up proof switch.

In Junction Isolation, the N and P wells of the PMOS and NMOS transistors form a diode which is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A Silicon-Controlled Rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch-up. With Trench Isolation, this diode is removed, the result being a latch-up proof switch.

Trench Isolation also leads to lower leakage currents. The ADG411, ADG412 and ADG413 have a leakage current of 0.25 nA as compared with a leakage current of several nanoamps in non-Trench Isolated switches. Leakage current is an important parameter in sample-and-hold circuits, this current being responsible for the discharge of the holding capacitor with time causing droop. The ADG411/ADG412/ADG413's low leakage current, along with its fast switching speeds, make it suitable for fast and accurate sample-and-hold circuits.

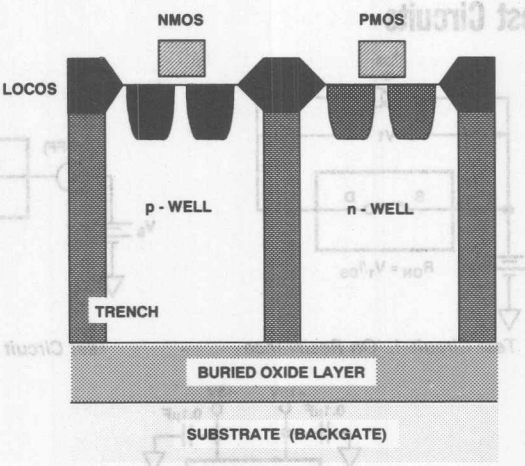


Figure 9. Trench Isolation

APPLICATION

Figure 10 illustrates a precise, fast sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an AD711. During the track mode, SW1 is closed and the output V_{OUT} follows the input signal V_{IN}. In the hold mode, SW1 is opened and the signal is held by the hold capacitor C_H.

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG411/ADG412/ADG413 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically 30 μV/μs.

A second switch SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp AD711 which will minimize charge injection effects. Pedestal error is also reduced by the compensation network R_C and C_C. This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ±10 V input range. Both the acquisition and settling times are 850 ns.

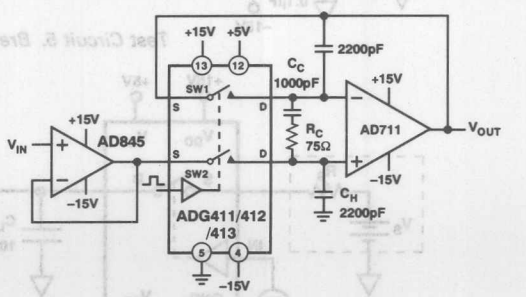
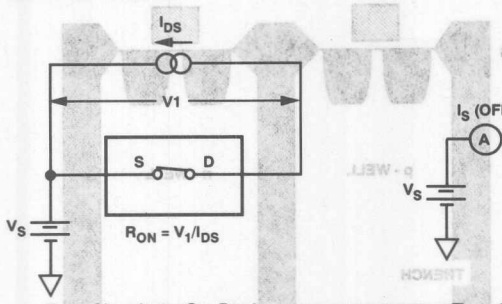
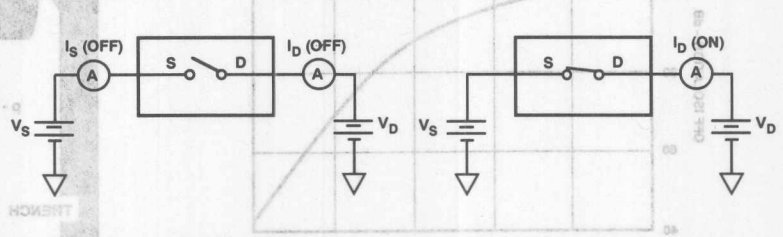


Figure 10. Fast, Accurate Sample-and-Hold

Test Circuits

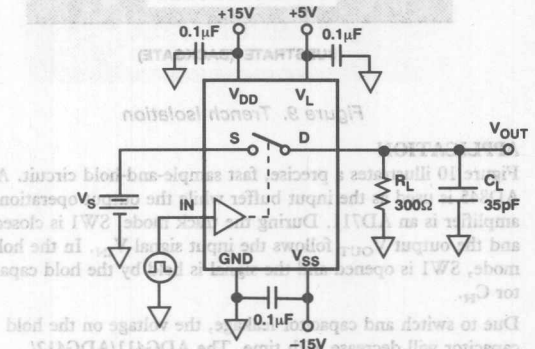


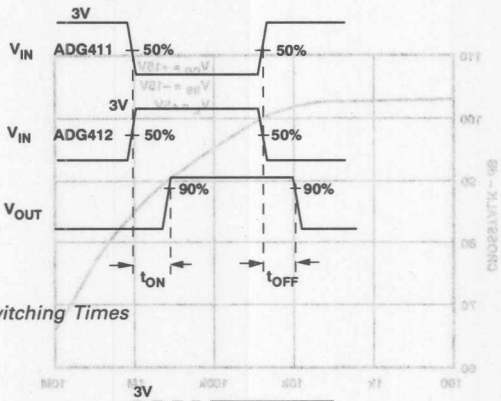
Test Circuit 1. On Resistance



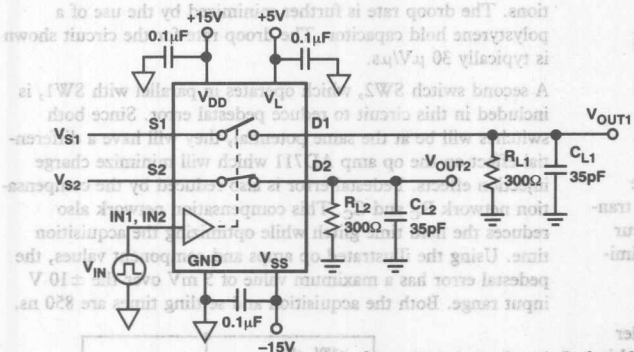
Test Circuit 2. Off Leakage

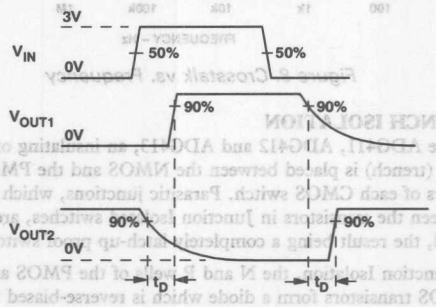
Test Circuit 3. On Leakage



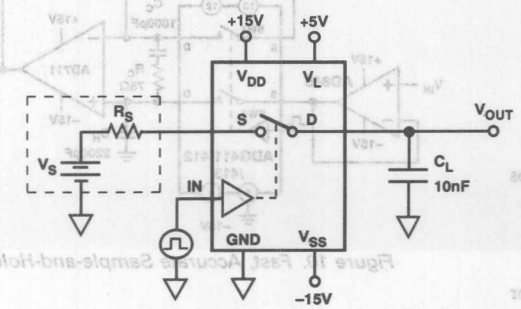


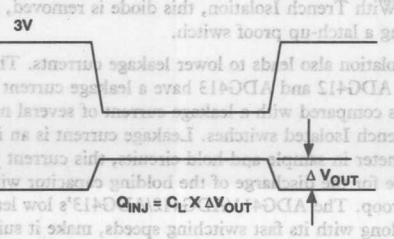
Test Circuit 4. Switching Times



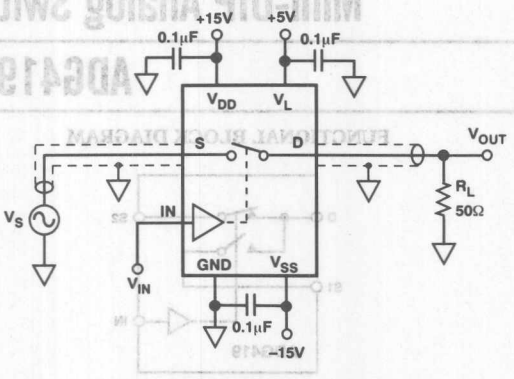


Test Circuit 5. Break-Before-Make Time Delay

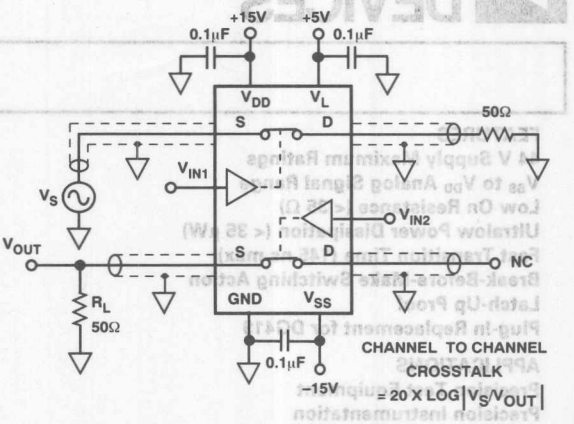




Test Circuit 6. Charge Injection



Test Circuit 7. Off Isolation



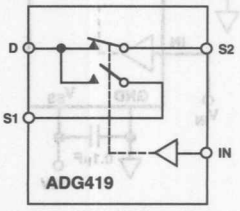
Test Circuit 8. Channel-to-Channel Crosstalk

7

FEATURES
44 V Supply Maximum Ratings
V_{SS} to V_{DD} Analog Signal Range
Low On Resistance (< 35 Ω)
Ultralow Power Dissipation (< 35 μW)
Fast Transition Time (145 ns max)
Break-Before-Make Switching Action
Latch-Up Proof
Plug-In Replacement for DG419

APPLICATIONS
Precision Test Equipment
Precision Instrumentation
Battery Powered Systems
Sample Hold Systems

FUNCTIONAL BLOCK DIAGRAM



SWITCH SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG419 is a monolithic CMOS SPDT switch. This switch is designed on an enhanced LC^2MOS process which provides low power dissipation yet gives high switching speed, low on resistance and low leakage currents.

The on resistance profile of the ADG419 is very flat over the full analog input range ensuring excellent linearity and low distortion. The part also exhibits high switching speed and high signal bandwidth. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

Each switch of the ADG419 conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. The ADG419 exhibits break-before-make switching action.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG419 is fabricated on an enhanced LC^2MOS, trench isolated process giving an increased signal range that extends to the supply rails.
2. Ultralow Power Dissipation
3. Low R_{ON}
4. Trench Isolation Guards Against Latch Up
   A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions
5. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG419 can be operated from a single rail power supply. The part is fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	25		25		Ω typ	V_D = ±12.5 V, I_S = –10 mA
	35	45	35	45	Ω max	V_{DD} = +13.5 V, V_{SS} = –13.5 V
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±5	±0.25	±15	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.75	±5	±0.75	±30	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.4		±0.4		nA typ	V_S = V_D = ±15.5 V;
	±0.75	±5	±0.75	±30	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±0.005		±0.005	μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	μA max	
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	145	200	145	200	ns max	R_L = 300 Ω, C_L = 35 pF; V_{S1} = ±10 V, V_{S2} = ∓10 V; Test Circuit 4
Break-Before-Make Time Delay, t_D	30		30		ns typ	R_L = 300 Ω, C_L = 35 pF;
	5		5		ns min	V_{S1} = V_{S2} = ±10 V; Test Circuit 5
OFF Isolation	80		80		dB typ	R_L = 50 Ω, f = 1 MHz; Test Circuit 6
Channel-to-Channel Crosstalk	70		70		dB typ	R_L = 50 Ω, f = 1 MHz; Test Circuit 7
C_S (OFF)	6		6		pF typ	f = 1 MHz
C_D, C_S (ON)	55		55		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
I_{DD}	0.0001		0.0001		μA typ	V_{IN} = 0 V or 5 V
	1	2.5	1	2.5	μA max	
I_{SS}	0.0001		0.0001		μA typ	
	1	2.5	1	2.5	μA max	
I_L	0.0001		0.0001		μA typ	V_L = +5.5 V
	1	2.5	1	2.5	μA max	

NOTES

[1]Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply (V_{DD} = +12 V ± 10%, V_{SS} = 0 V, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	40		40		Ω typ	V_D = +3 V, +8.5 V, I_S = –10 mA
		60		70	Ω max	V_{DD} = +10.8 V
LEAKAGE CURRENT						V_{DD} = +13.2 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V;
	±0.25	±5	±0.25	±15	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V;
	±0.75	±5	±0.75	±30	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.4		±0.4		nA typ	V_S = V_D = 12.2 V/1 V;
	±0.75	±5	±0.75	±30	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±0.005		±0.005	μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	μA max	
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	170	250	170	250	ns max	R_L = 300 Ω, C_L = 35 pF; V_{S1} = 0 V/8 V, V_{S2} = 8 V/0 V; Test Circuit 4
Break-Before-Make Time Delay, t_D	60		60		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +8 V; Test Circuit 5
OFF Isolation	80		80		dB typ	R_L = 50 Ω, f = 1 MHz; Test Circuit 6
Channel-to-Channel Crosstalk	70		70		dB typ	R_L = 50 Ω, f = 1 MHz; Test Circuit 7
C_S (OFF)	13		13		pF typ	f = 1 MHz
C_D, C_S (ON)	65		65		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +13.2 V
I_{DD}	0.0001		0.0001		μA typ	V_{IN} = 0 V or 5 V
	1	2.5	1	2.5	μA max	
I_L	0.0001		0.0001		μA typ	V_L = +5.5 V
	1	2.5	1	2.5	μA max	

NOTES
[1]Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

Table I. Truth Table

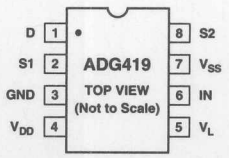
Logic	Switch 1	Switch 2
0	ON	OFF
1	OFF	ON

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG419BN	–40°C to +85°C	N-8
ADG419BR	–40°C to +85°C	SO-8
ADG419TQ	–55°C to +125°C	Q-8

*N = Plastic DIP, Q = Cerdip, SO = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.

PIN CONFIGURATION DIP/SOIC



ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} ..... +44 V
V_{DD} to GND ..... –0.3 V to +25 V
V_{SS} to GND ..... +0.3 V to –25 V
V_L to GND ..... –0.3 V to V_{DD} + 0.3 V
Analog, Digital Inputs[2] ..... V_{SS} – 2 V to V_{DD} + 2 V
or 30 mA, Whichever Occurs First
Continuous Current, S or D ..... 30 mA
Peak Current, S or D ..... 100 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Extended (T Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
Cerdip Package, Power Dissipation ..... 600 mW
θ_{JA}, Thermal Impedance ..... 110°C/W
Lead Temperature, Soldering (10 sec) ..... +300°C
Plastic Package, Power Dissipation ..... 400 mW
θ_{JA}, Thermal Impedance ..... 100°C/W
Lead Temperature, Soldering (10 sec) ..... +260°C
SOIC Package, Power Dissipation ..... 400 mW
θ_{JA}, Thermal Impedance ..... 155°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

NOTE

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

7

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
V_L	Logic power supply (+5 V).
GND	Ground (0 V) reference.
S	Source terminal. May be an input or an output.
D	Drain terminal. May be an input or an output.
IN	Logic control input.
R_{ON}	Ohmic resistance between D and S.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" switch source capacitance.
C_D, C_S (ON)	"ON" switch capacitance.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
t_D	"OFF" time or "ON" time measured between the 90% points of both switches when switching from one address state to the other.
V_{INL}	Maximum input voltage for logic "0."
V_{INH}	Minimum input voltage for logic "1."
I_{INL} (I_{INH})	Input current of the digital input.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

LC²MOS Latchable 4/8 Channel High Performance Analog Multiplexers

ADG428/ADG429

FEATURES

- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (60 Ω typ)
- Low Power Consumption (1.6 mW max)
- Low Charge Injection (<4 pC typ)
- Fast Switching
- Break Before make Switching Action
- Plug-In Replacement for DG428/DG429

APPLICATIONS

- Automatic Test Equipment
- Data Acquisition Systems
- Communication Systems
- Avionics and Military Systems
- Microprocessor Controlled Analog Systems
- Medical Instrumentation

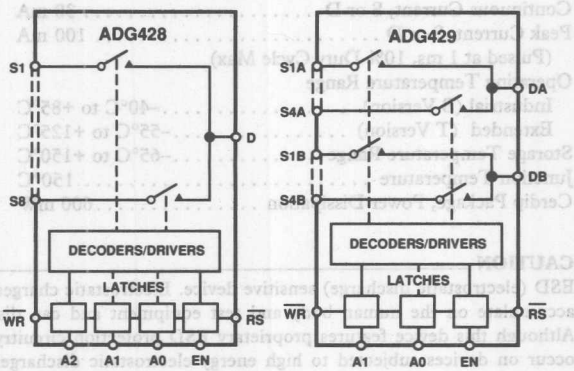
GENERAL DESCRIPTION

The ADG428 and ADG429 are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels respectively. On-chip address and control latches facilitate microprocessor interfacing. The ADG428 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG429 switches one of four differential inputs to a common differential output as determined by the 2 bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF. All the control inputs, address and enable inputs are TTL compatible over the full specified operating temperature range. This makes the part suitable for bus-controlled systems such as data acquisition systems, process controls, avionics and ATEs because the TTL compatible address latches simplify the digital interface design and reduce the board space required.

The ADG428/ADG429 are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance. Each channel conducts equally well in both directions when ON and has an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break before make switching action preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

The ADG428/ADG429 are improved replacements for the DG428/DG429 Analog Multiplexers.

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG428/ADG429 are fabricated on an enhanced LC²MOS process giving an increased signal range that extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Single/Dual Supply Operation
5. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG428/ADG429 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS[1]

DUAL SUPPLY (V_{DD} = +15 V, V_{SS} = −15 V, GND = 0 V, $\overline{WR}$ = 0 V, $\overline{RS}$ = 2.4 V unless otherwise noted)

Parameter	B Version 25°C	B Version −40°C to +85°C	T Version 25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	60		60		Ω typ	V_D = ±10 V, I_S = −1 mA
	100	125	100	125	Ω max	
ΔR_{ON}	10		10		% max	−10 V < V_S < 10 V, I_S = −1 mA
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	±0.03	±0.3	±0.03	±0.3	nA typ	V_D = ±10 V, V_S = ∓10 V;
	±0.5	±50	±0.5	±50	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = ±10 V, V_S = ∓10 V;
ADG428	±0.07	±0.7	±0.07	±0.7	nA typ	Test Circuit 3
	±1	±100	±1	±100	nA max	
ADG429	±0.05	±0.5	±0.05	±0.5	nA typ	
	±1	±50	±1	±50	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = ±10 V;
ADG428	±1	±100	±1	±100	nA max	Test Circuit 4
ADG429	±1	±50	±1	±50	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	±0.1	±1	±0.1	±1	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	110		110		ns typ	R_L = 1 MΩ, C_L = 35 pF;
	250	300	250	300	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V;
						Test Circuit 5
t_{OPEN}	10		10		ns min	R_L = 1 kΩ, C_L = 35 pF;
						V_S = +5 V; Test Circuit 6
t_{ON} (EN, $\overline{WR}$)	115		115		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	150	225	150	225	ns max	V_S = +5 V; Test Circuit 7
t_{OFF} (EN, $\overline{RS}$)	105		105		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	150	300	150	300	ns max	V_S = +5 V; Test Circuit 7
t_W, Write Pulse Width		100		100	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulse Width		100		100	ns min	V_S = +5 V
Charge Injection	4		4		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF;
						Test Circuit 10
OFF Isolation	−75		−75		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
	−60		−60		dB min	V_S = 7 V_{RMS}, V_{EN} = 0 V; Test Circuit 11
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
						Test Circuit 12
C_S (OFF)	11		11		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG428	40		40		pF typ	
ADG429	20		20		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG428	54		54		pF typ	
ADG429	34		34		pF typ	
POWER REQUIREMENTS						V_{IN} = 0 V, V_{EN} = 0 V
I_{DD}	20		20		μA typ	
	100		100		μA max	
I_{SS}	0.001		0.001		μA typ	
	5		5		μA max	

NOTES
[1]Temperature Ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

Parameter	B Version 25°C	B Version −40°C to +85°C	T Version 25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	90		90		Ω typ	V_D = +10 V, I_S = −500 μA
		200		200	Ω max	
ΔR_{ON}	10		10		% max	0 V < V_S < 10 V, I_S = −1 mA
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	±0.005		±0.005		nA typ	V_D = 10 V/0 V, V_S = 0 V/10 V;
	±0.5	±50	±0.5	±50	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = 10 V/0 V, V_S = 0 V/10 V;
ADG428	±0.015		±0.015		nA typ	Test Circuit 3
	±1	±100	±1	±100	nA max	
ADG429	±0.008		±0.008		nA typ	
	±1	±50	±1	±50	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = 10 V/0 V;
ADG428	±0.02		±0.02		nA typ	Test Circuit 4
	±1	±100	±1	±100	nA max	
ADG429	±0.01		±0.01		nA typ	
	±1	±50	±1	±50	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±1		±1	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	250		250		ns typ	R_L = 1 MΩ, C_L = 35 pF;
	350	450	350	450	ns max	V_{S1} = 10 V/0 V, V_{S8} = 0 V/10 V;
						Test Circuit 5
t_{OPEN}	25	10	25	10	ns min	R_L = 1 kΩ, C_L = 35 pF;
						V_S = +5 V; Test Circuit 6
t_{ON} (EN, $\overline{WR}$)	200		200		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	300	400	300	400	ns max	V_S = +5 V; Test Circuit 7
t_{OFF} (EN, $\overline{RS}$)	80		80		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	300	400	300	400	ns max	V_S = +5 V; Test Circuit 7
t_W, Write Pulse Width		100		100	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulse Width		100		100	ns min	V_S = 5 V
Charge Injection	4		4		pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 10 nF;
						Test Circuit 10
OFF Isolation	−75		−75		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
	−60		−60		dB min	V_S = 7 V_{RMS}, V_{EN} = 0 V; Test Circuit 11
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
						Test Circuit 12
C_S (OFF)	11		11		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG428	40		40		pF typ	
ADG429	20		20		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG428	54		54		pF typ	
ADG429	34		34		pF typ	
POWER REQUIREMENTS						V_{IN} = 0 V, V_{EN} = 0 V
I_{DD}	20		20		μA typ	
	100		100		μA max	

NOTES
[1]Temperature Ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted.)

V_{DD} to V_{SS}	+44 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog, Digital Inputs[2]	V_{SS} − 2 V to V_{DD} + 2 V or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)	
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Cerdip Package, Power Dissipation	900 mW
θ_{JA}, Thermal Impedance	73°C/W
Lead Temperature, Soldering (10 sec)	+300°C
Plastic Package, Power Dissipation	470 mW
θ_{JA}, Thermal Impedance	115°C/W
Lead Temperature, Soldering (10 sec)	+260°C
PLCC Package, Power Dissipation	800 mW
θ_{JA}, Thermal Impedance	90°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at A, EN, $\overline{WR}$, $\overline{RS}$, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

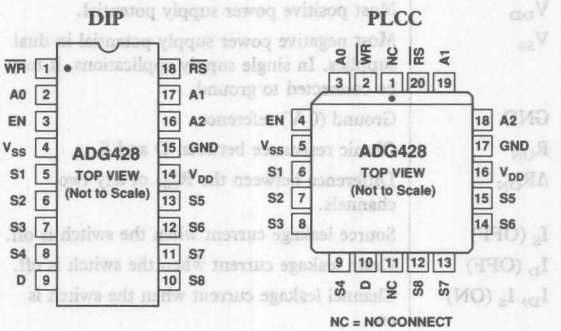
Model[1]	Temperature Range	Package Option[2]
ADG428BN	−40°C to +85°C	N-18
ADG428BP	−40°C to +85°C	P-20A
ADG428TQ	−55°C to +125°C	Q-18
ADG429BN	−40°C to +85°C	N-18
ADG429BP	−40°C to +85°C	P-20A
ADG429TQ	−55°C to +125°C	Q-18

NOTES

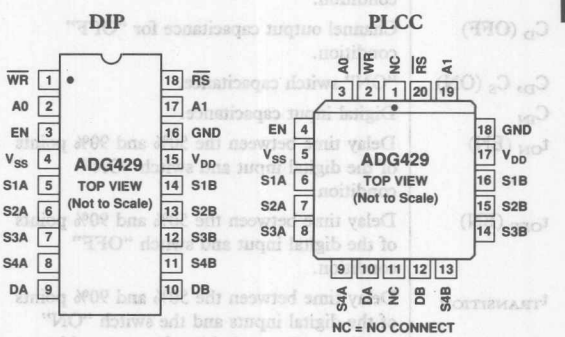
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.

[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.

ADG428 PIN CONFIGURATIONS



ADG429 PIN CONFIGURATIONS



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to ground.
GND	Ground (0 V) reference.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current when the switch is off.
I_D (OFF)	Drain leakage current when the switch is off.
I_D, I_S (ON)	Channel leakage current when the switch is on.
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	Channel input capacitance for "OFF" condition.
C_D (OFF)	Channel output capacitance for "OFF" condition.
C_D, C_S (ON)	"ON" switch capacitance.
C_{IN}	Digital input capacitance.
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition.
t_{OFF} (EN)	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
t_{OPEN}	"OFF" time measured between 80% points of both switches when switching from one address state to another.
V_{INL}	Maximum input voltage for logic "0".
V_{INH}	Minimum input voltage for logic "1".
I_{INL} (I_{INH})	Input current of the digital input.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

ADG428 Truth Table

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching						
X	X	X	X	↓	1	Maintains Previous Switch Condition
Reset						
X	X	X	X	X	0	NONE (Latches Cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

ADG429 Truth Table

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
Latching					
X	X	X	↓	1	Maintains Previous Switch Condition
Reset					
X	X	X	X	0	NONE (Latches Cleared)
Transparent Operation					
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

TIMING DIAGRAMS

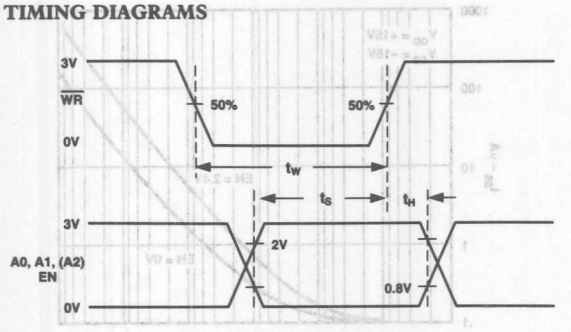


Figure 1.

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

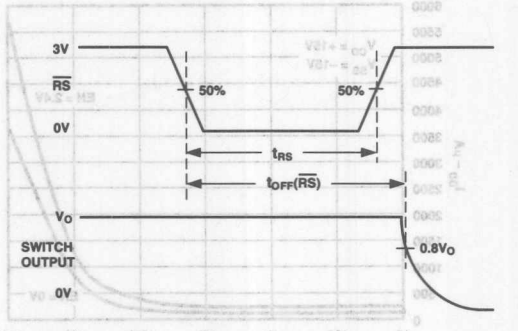


Figure 2.

Figure 2 shows the Reset Pulse Width, t_{RS}, and the Reset Turn-off Time, $t_{OFF(\overline{RS})}$.

Note: All digital input signals rise and fall times are measured from 10% to 90% of 3 V. tr = tf = 20 ns.

7

Typical Characteristics

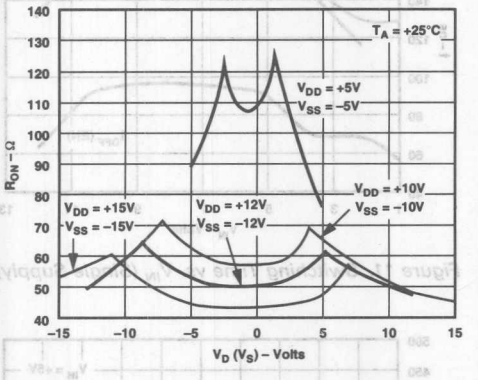


Figure 3. R_{ON} as a Function of V_D (V_S): Dual Supply Voltage

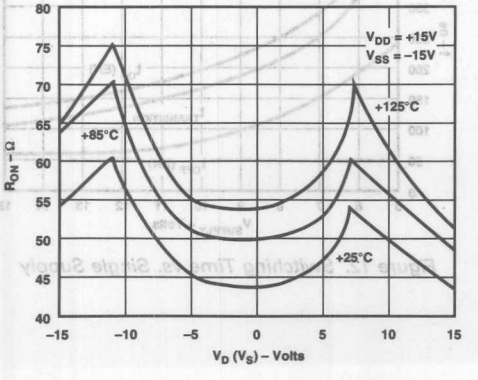


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures

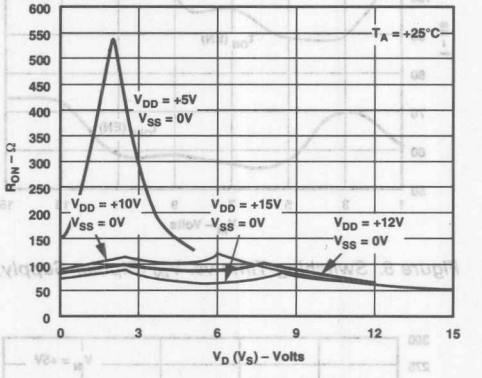


Figure 5. R_{ON} as a Function of V_D (V_S): Single Supply Voltage

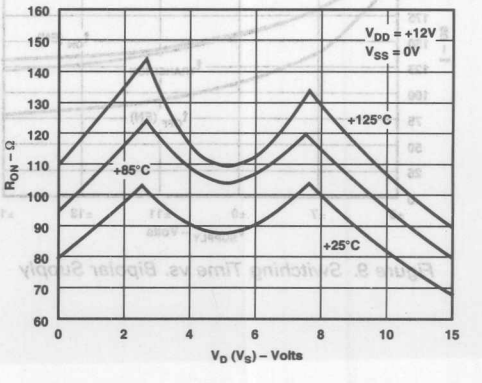


Figure 6. R_{ON} as a Function of V_D (V_S) for Different Temperatures

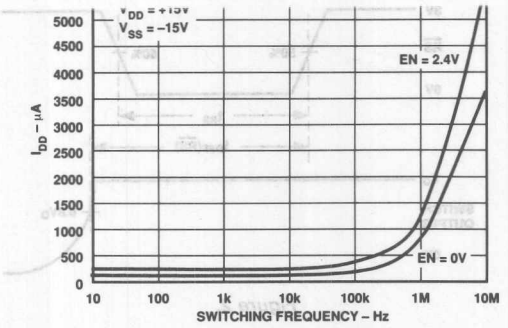


Figure 7. Positive Supply Current vs. Switching Frequency

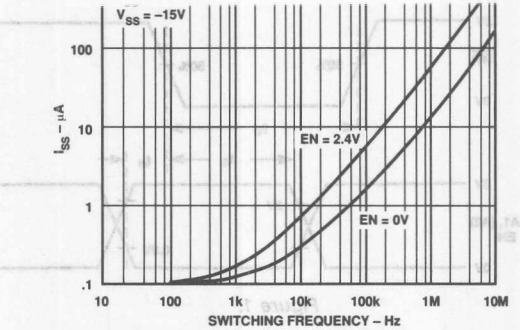


Figure 10. Negative Supply Current vs. Switching Frequency

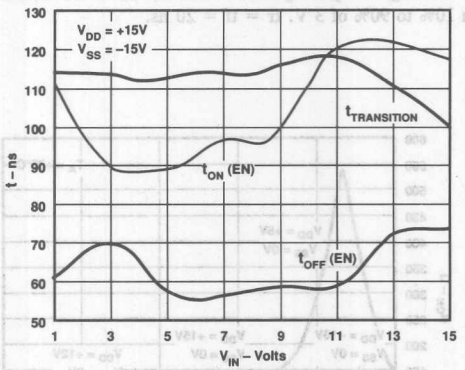


Figure 8. Switching Time vs. V_{IN} (Bipolar Supply)

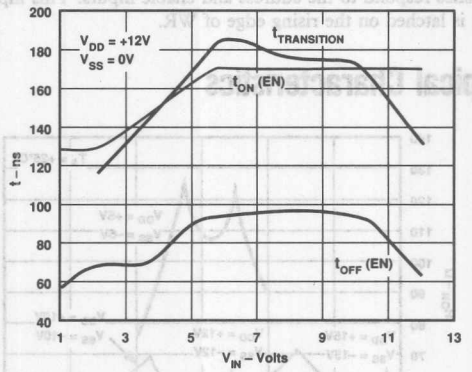


Figure 11. Switching Time vs. V_{IN} (Single Supply)

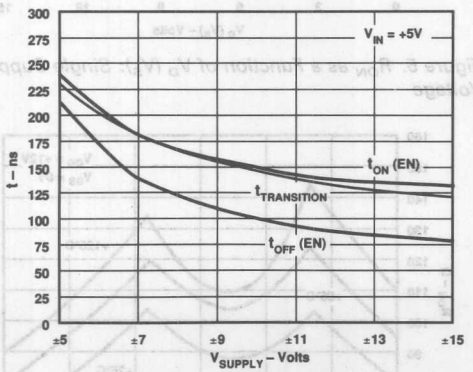


Figure 9. Switching Time vs. Bipolar Supply

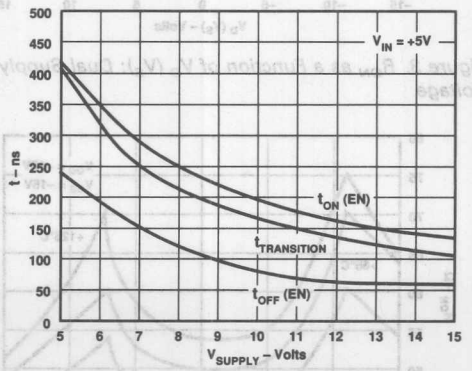


Figure 12. Switching Time vs. Single Supply

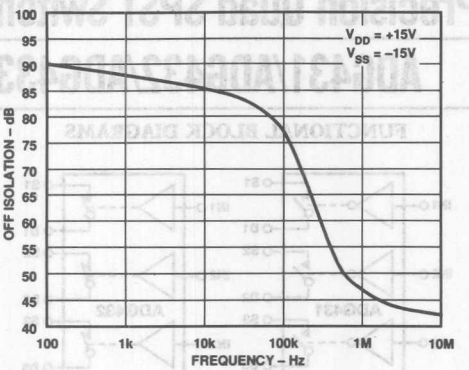


Figure 13. OFF Isolation vs. Frequency

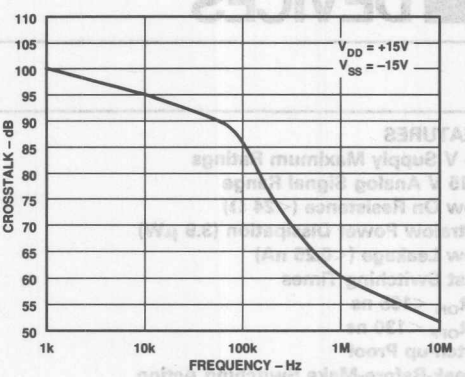


Figure 15. Crosstalk vs. Frequency

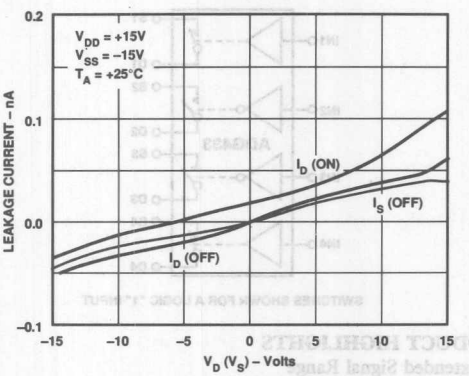


Figure 14. Leakage Currents as a Function of V_D (V_S)

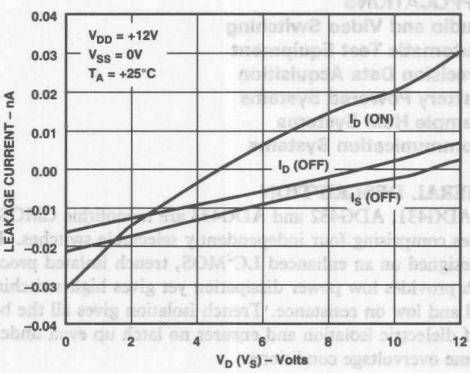


Figure 16. Leakage Currents as a Function of V_D (V_S)

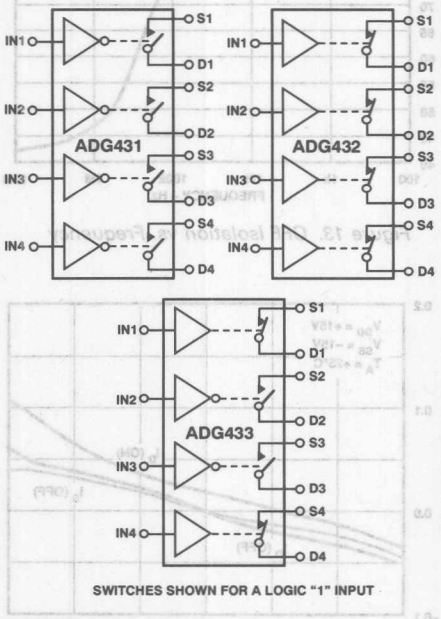
ANALOG DEVICES

DI LC²MOS
Precision Quad SPST Switches
ADG431/ADG432/ADG433

FEATURES
- 44 V Supply Maximum Ratings
- ±15 V Analog Signal Range
- Low On Resistance (<24 Ω)
- Ultralow Power Dissipation (3.9 μW)
- Low Leakage (<0.25 nA)
- Fast Switching Times
  - t_{ON} <165 ns
  - t_{OFF} <130 ns
- Latch-up Proof
- Break-Before-Make Switching Action
- TTL/CMOS Compatible
- Plug-in Replacement for DG411/DG412/DG413

APPLICATIONS
- Audio and Video Switching
- Automatic Test Equipment
- Precision Data Acquisition
- Battery Powered Systems
- Sample Hold Systems
- Communication Systems

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG431, ADG432 and ADG433 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS, trench isolated process which provides low power dissipation yet gives high switching speed and low on resistance. Trench isolation gives all the benefits of dielectric isolation and ensures no latch up even under extreme overvoltage conditions.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG431, ADG432 and ADG433 contain four independent SPST switches. The ADG431 and ADG432 differ only in that the digital control logic is inverted. The ADG431 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG432. The ADG433 has two switches with digital control logic similar to that of the ADG431 while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break before make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG431, ADG432 and ADG433 are fabricated on an enhanced LC²MOS, trench isolated process giving an increased signal range which extends fully to the supply rails.
2. Ultralow Power Dissipation
3. Low R_{ON}
4. Trench Isolation Guards Against Latch-up
   A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
5. Break Before Make Switching
   This prevents channel shorting when the switches are configured as a multiplexer.
6. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG431, ADG432 and ADG433 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version −40°C to +25°C	B Version −40°C to +85°C	T Version −55°C to +25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{DD} to V_{SS}		V_{DD} to V_{SS}	V	
R_{ON}	17		17		Ω typ	V_D = ±8.5 V, I_S = −10 mA;
	24	26	24	27	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
R_{ON} vs. V_D (V_S)	15		15		% typ	
R_{ON} Drift	0.5		0.5		%/°C typ	
R_{ON} Match	5		5		% typ	V_D = 0 V, I_S = −10 mA
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source OFF Leakage I_S (OFF)	±0.05		±0.05		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±2	±0.25	±15	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		±0.05		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±2	±0.25	±15	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		±0.1		nA typ	V_D = V_S = ±15.5 V;
	±0.35	±2	±0.35	±17	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.02		±0.02	μA max	
C_{IN} Digital Input Capacitance	9		9		pF typ	
DYNAMIC CHARACTERISTICS[2]						V_{DD} = +15 V, V_{SS} = −15 V
t_{ON}	90		90		ns typ	R_L = 300 Ω, C_L = 35 pF;
		165		175	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	60		60		ns typ	R_L = 300 Ω, C_L = 35 pF;
		130		145	ns max	V_S = ±10 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG433 Only)	25		25		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +10 V; Test Circuit 5
Charge Injection	5		5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		0.0001		μA typ	
	0.1	0.2	0.1	0.2	μA max	
I_{SS}	0.0001		0.0001		μA typ	
	0.1	0.2	0.1	0.2	μA max	
I_L	0.0001		0.0001		μA typ	
	0.1	0.2	0.1	0.2	μA max	
Power Dissipation		7.7		7.7	μW max	

NOTES
[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

Single Supply (V_{DD} = +12 V ± 10%, V_{SS} = 0 V, V_L = [illegible])

Parameter	B Version −40°C to +25°C	B Version −40°C to +85°C	T Version −55°C to +25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
Analog Signal Range		0 V to V_{DD}		0 V to V_{DD}	V	
R_{ON}	28		28		Ω typ	0 < V_D < 8.5 V, I_S = −10 mA;
	42	45	42	45	Ω max	V_{DD} = +10.8 V
R_{ON} vs. V_D (V_S)	20		20		% typ	
R_{ON} Drift	0.5		0.5		%/°C typ	
R_{ON} Match	5		5		% typ	V_D = 0 V, I_S = −10 mA
LEAKAGE CURRENTS						V_{DD} = +13.2 V
Source OFF Leakage I_S (OFF)	±0.04		±0.04		nA typ	V_D = 12.2/1 V, V_S = 1/12.2 V;
	±0.25	±1	±0.25	±15	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.04		±0.04		nA typ	V_D = 12.2/1 V, V_S = 1/12.2 V;
	±0.25	±1	±0.25	±15	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		±0.01		nA typ	V_D = V_S = +12.2 V/+1 V;
	±0.3	±5	±0.3	±17	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.01		±0.01	μA max	
C_{IN} Digital Input Capacitance	9		9		pF typ	
DYNAMIC CHARACTERISTICS[2]						V_{DD} = +12 V, V_{SS} = 0 V
t_{ON}	165		165		ns typ	R_L = 300 Ω, C_L = 35 pF;
		240		240	ns max	V_S = +8 V; Test Circuit 4
t_{OFF}	60		60		ns typ	R_L = 300 Ω, C_L = 35 pF;
		115		115	ns max	V_S = +8 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG433 Only)	25		25		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +10 V; Test Circuit 5
Charge Injection	25		25		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +13.2 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		0.0001		μA typ	
	0.03	0.1	0.03	0.1	μA max	
I_L	0.0001		0.0001		μA typ	
	0.03	0.1	0.03	0.1	μA max	V_L = +5.25 V
Power Dissipation		1.9		1.9	μW max	

NOTES
[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

Truth Table (ADG431/ADG432)

ADG431 In	ADG432 In	Switch Condition
0	1	ON
1	0	OFF

Truth Table (ADG433)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS}	+44 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
V_L to GND	−0.3 V to V_{DD} + 0.3 V
Analog, Digital Inputs[2]	V_{SS} −2 V to V_{DD} +2 V or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA
(Pulsed at 1 ms, 10% Duty Cycle max)	
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Cerdip Package, Power Dissipation	900 mW
θ_{JA}, Thermal Impedance	76°C/W
Lead Temperature, Soldering (10 sec)	+300°C
Plastic Package, Power Dissipation	470 mW
θ_{JA}, Thermal Impedance	117°C/W
Lead Temperature, Soldering (10 sec)	+260°C
SOIC Package, Power Dissipation	600 mW
θ_{JA}, Thermal Impedance	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

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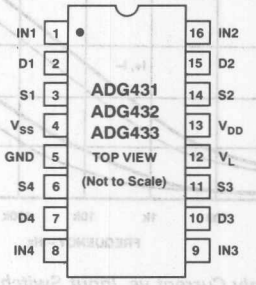
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION (DIP/SOIC)



ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG431BN	−40°C to +85°C	N-16
ADG431BR	−40°C to +85°C	R-16A
ADG431TQ	−55°C to +125°C	Q-16
ADG432BN	−40°C to +85°C	N-16
ADG432BR	−40°C to +85°C	R-16A
ADG432TQ	−55°C to +125°C	Q-16
ADG433BN	−40°C to +85°C	N-16
ADG433BR	−40°C to +85°C	R-16A

NOTES

[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.

[2]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); Q = Cerdip. For outline information see Package Information section.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
V_L	Logic power supply (+5 V).
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
R_{ON}	Ohmic resistance between D and S.
R_{ON} vs. V_D (V_S)	The variation in R_{ON} due to a change in the analog input voltage with a constant load current.
R_{ON} Drift	Change in R_{ON} vs. temperature.
R_{ON} Match	Difference between the R_{ON} of any two switches.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" switch source capacitance.
C_D (OFF)	"OFF" switch drain capacitance.
C_D, C_S (ON)	"ON" switch capacitance.
C_{IN}	Input Capacitance to ground of a digital input.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_D	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Typical Performance Graphs

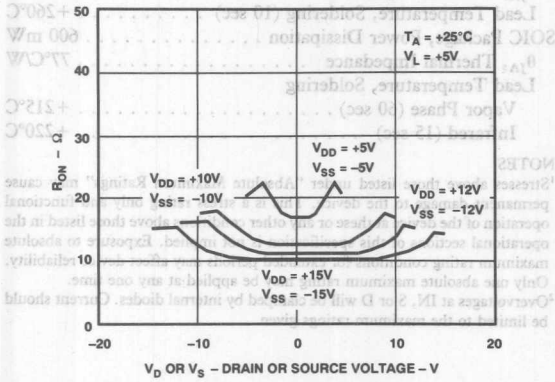


Figure 1. On Resistance as a Function of V_D (V_S) Dual Supplies

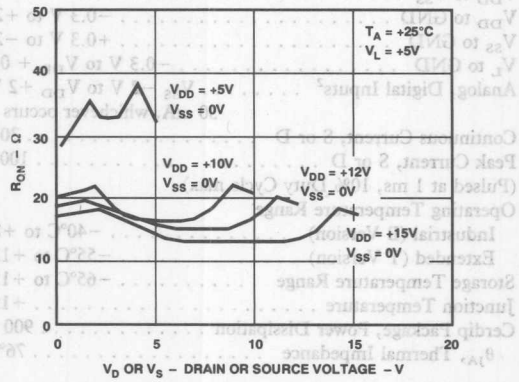


Figure 4. On Resistance as a Function of V_D (V_S) Single Supply

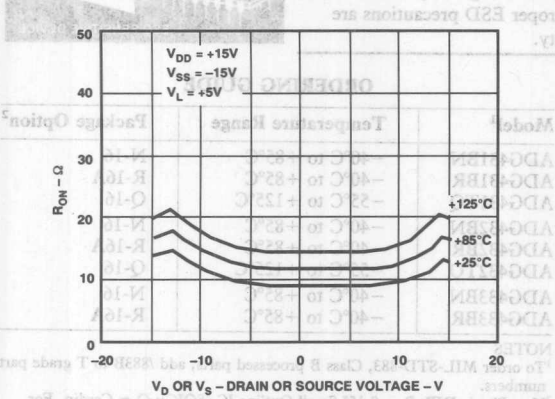


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures

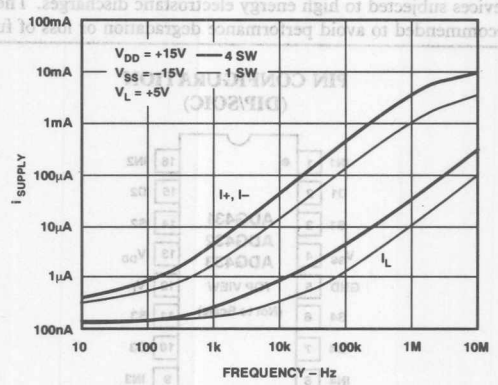


Figure 5. Supply Current vs. Input Switching Frequency

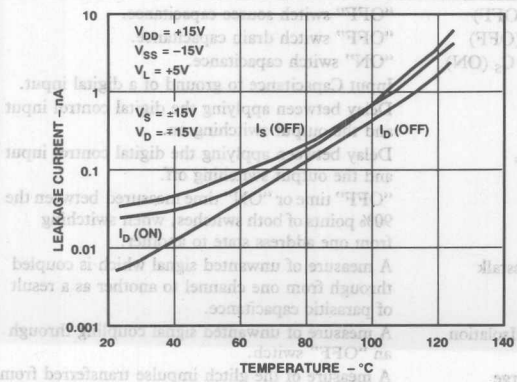


Figure 3. Leakage Currents as a Function of Temperature

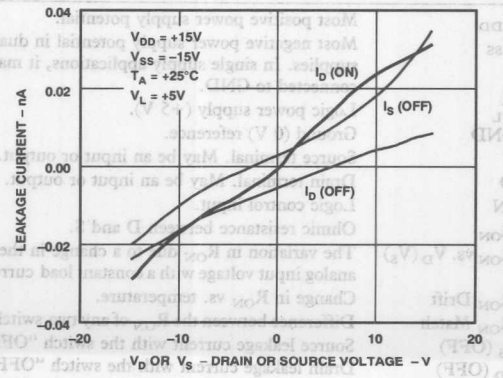


Figure 6. Leakage Currents as a Function of V_D (V_S)

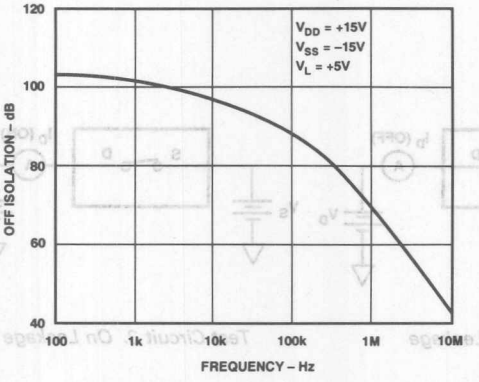


Figure 7. Off Isolation vs. Frequency

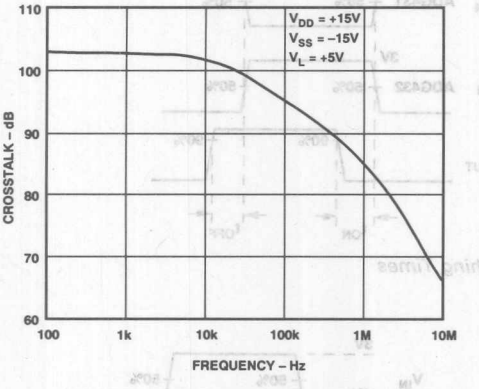


Figure 8. Crosstalk vs. Frequency

TRENCH ISOLATION

In the ADG431, ADG432 and ADG433, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in Junction Isolated switches, are eliminated, the result being a completely latch-up proof switch.

In Junction Isolation, the N and P wells of the PMOS and NMOS transistors form a diode which is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A Silicon-Controlled Rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch-up. With Trench Isolation, this diode is removed, the result being a latch-up proof switch.

Trench Isolation also leads to lower leakage currents. The ADG431, ADG432 and ADG433 have a leakage current of 0.25 nA as compared with a leakage current of several nanoamps in non-Trench Isolated switches. Leakage current is an important parameter in sample-and-hold circuits, this current being responsible for the discharge of the holding capacitor with time causing droop. The ADG431/ADG432/ADG433's low leakage current, along with its fast switching speeds, make it suitable for fast and accurate sample-and-hold circuits.

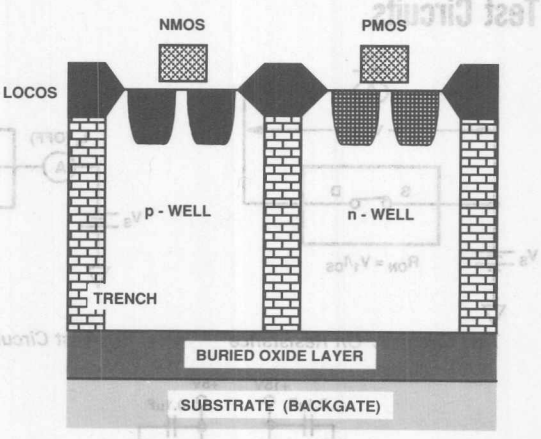


Figure 9. Trench Isolation

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APPLICATION

Figure 10 illustrates a precise, fast sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an AD711. During the track mode, SW1 is closed and the output V_{OUT} follows the input signal V_{IN}. In the hold mode, SW1 is opened and the signal is held by the hold capacitor C_H.

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG431/ADG432/ADG433 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically 30 μV/μs.

A second switch SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp AD711 which will minimize charge injection effects. Pedestal error is also reduced by the compensation network R_C and C_C. This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ±10 V input range. Both the acquisition and settling times are 850 ns.

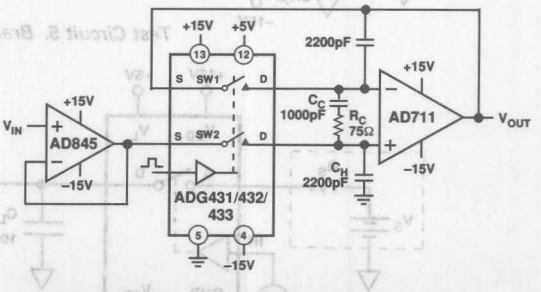
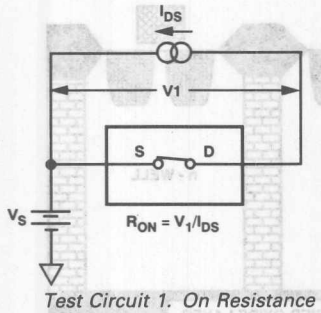
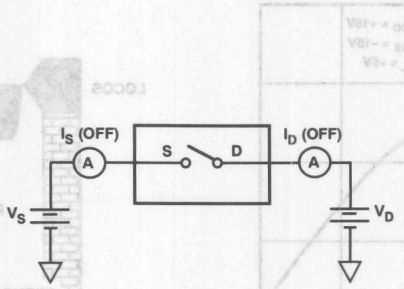


Figure 10. Fast, Accurate Sample-and-Hold

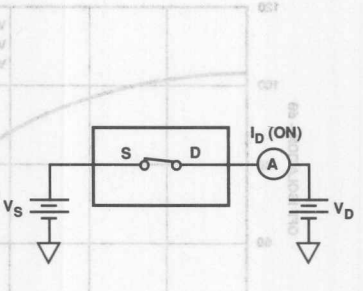
Test Circuits



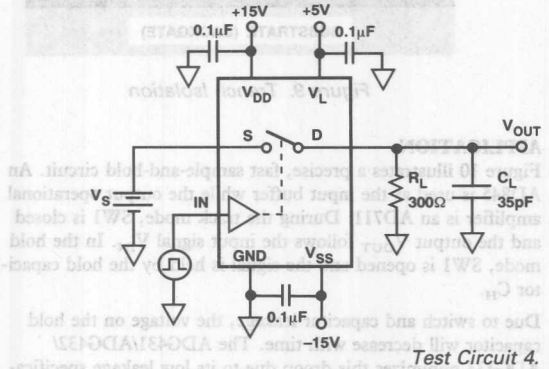
Test Circuit 1. On Resistance

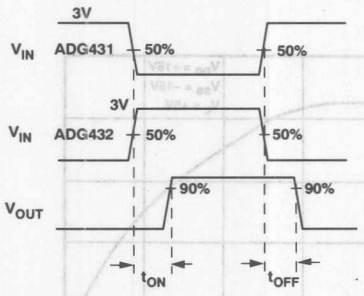


Test Circuit 2. Off Leakage

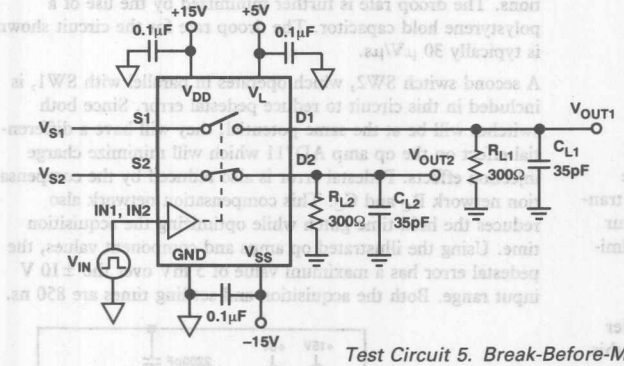


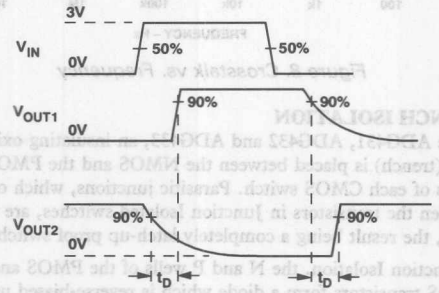
Test Circuit 3. On Leakage



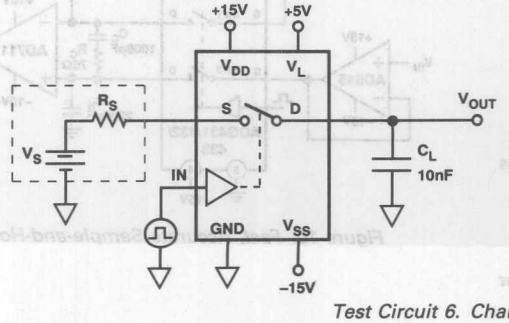


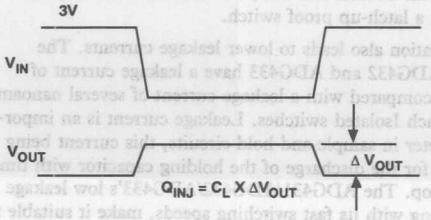
Test Circuit 4. Switching Times



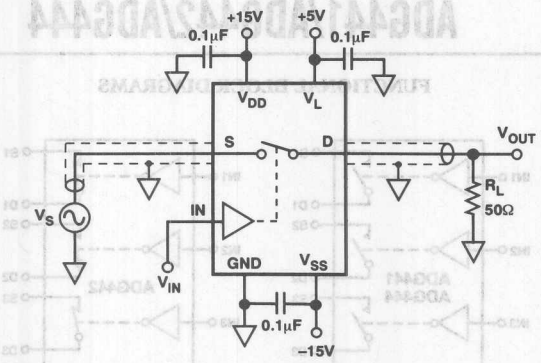


Test Circuit 5. Break-Before-Make Time Delay

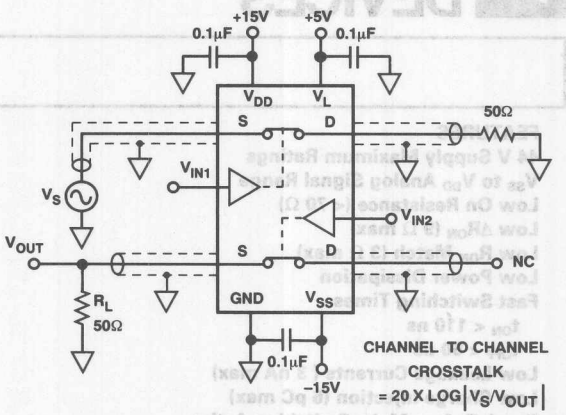




Test Circuit 6. Charge Injection



Test Circuit 7. Off Isolation



Test Circuit 8. Channel-to-Channel Crosstalk

7

LC²MOS Quad SPST Switches

ADG441/ADG442/ADG444

FEATURES

- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (< 70 Ω)
- Low ΔR_{ON} (9 Ω max)
- Low R_{ON} Match (3 Ω max)
- Low Power Dissipation
- Fast Switching Times
  - t_{ON} < 110 ns
  - t_{OFF} < 60 ns
- Low Leakage Currents (3 nA max)
- Low Charge Injection (6 pC max)
- Break-Before-Make Switching Action
- Latch-Up Proof
- Plug-In Upgrade for
  DG201A/ADG201A, DG202A/ADG202A,
  DG211/ADG211A
- Plug in Replacement for DG441/DG442/DG444

APPLICATIONS

- Audio and Video Switching
- Automatic Test Equipment
- Precision Data Acquisition
- Battery Powered Systems
- Sample Hold Systems
- Communication Systems

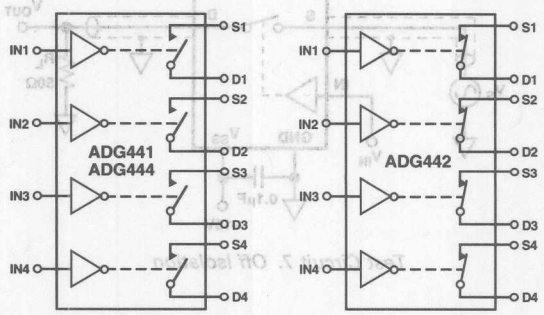
GENERAL DESCRIPTION

The ADG441, ADG442 and ADG444 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG441, ADG442 and ADG444 contain four independent SPST switches. Each switch of the ADG441 and ADG444 turns on when a logic low is applied to the appropriate control input. The ADG442 switches are turned on with a logic high on the appropriate control input. The ADG441 and ADG444 switches differ in that the ADG444 requires a 5 V logic power supply which is applied to the V_L pin. The ADG441 and ADG442 do not have a V_L pin, the logic power supply being generated internally by an on-chip voltage generator.

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

Each switch conducts equally well in both directions when ON and has an input signal range that extends to the power supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG441/ADG442/ADG444 are fabricated on an enhanced LC²MOS, trench-isolated process, giving an increased signal range that extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Trench Isolation Guards Against Latch Up
   A dielectric trench separates the P and N channel transistors thereby preventing latch up even under severe overvoltage conditions.
5. Break-Before-Make Switching
   This prevents channel shorting when the switches are configured as a multiplexer.
6. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG441/ADG442/ADG444 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, V_L = +5 V ± 10% (ADG444), GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	40		40		Ω typ	V_D = ±8.5 V, I_S = –10 mA
	70	85	70	85	Ω max	V_{DD} = +13.5 V, V_{SS} = –13.5 V
ΔR_{ON}		4		4	Ω typ	–8.5 V ≤ V_D ≤ +8.5 V
		9		9	Ω max	
R_{ON} Match		1		1	Ω typ	V_D = 0 V, I_S = –10 mA
		3		3	Ω max	
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.01		±0.01		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.5	±3	±0.5	±20	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01		±0.01		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.5	±3	±0.5	±20	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.08		±0.08		nA typ	V_S = V_D = ±15.5 V;
	±0.5	±3	±0.5	±40	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±0.00001		±0.00001	µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	85		85		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	110	170	110	170	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	45		45		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	60	80	60	80	ns max	V_S = ±10 V; Test Circuit 4
t_{OPEN}	30		30		ns typ	R_L = 1 kΩ, C_L = 35 pF;
Charge Injection	1		1		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF;
	6		6		pC max	V_{DD} = +15 V, V_{SS} = –15 V; Test Circuit 5
OFF Isolation	60		60		dB typ	R_L = 50 Ω, C_L = 5 pF; f = 1 MHz; Test Circuit 6
Channel-to-Channel Crosstalk	100		100		dB typ	R_L = 50 Ω, C_L = 5 pF; f = 1 MHz; Test Circuit 7
C_S (OFF)	4		4		pF typ	f = 1 MHz
C_D (OFF)	4		4		pF typ	f = 1 MHz
C_D, C_S (ON)	16		16		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
I_{DD}						Digital Inputs = 0 V or 5 V
ADG441/ADG442		80		80	µA max	
ADG444	0.001		0.001		µA typ	
	1	2.5	1	2.5	µA max	
I_{SS}	0.0001		0.0001		µA typ	
	1	2.5	1	2.5	µA max	
I_L (ADG444 Only)	0.001		0.001		µA typ	V_L = +5.5 V
	1	2.5	1	2.5	µA max	

NOTES

[1]Temperature ranges are as follows: B Versions: –40°C to +85°C; T Versions: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply (V_{DD} = +12 V ± 10%, V_{SS} = 0 V, V_L = +5 V ± 10% (ADG444), GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version −40°C to +85°C	T Version +25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	70		70		Ω typ	V_D = +3 V, +8 V, I_S = −10 mA;
	110	130	110	130	Ω max	V_{DD} = +10.8 V
ΔR_{ON}		4		4	Ω typ	+3 V ≤ V_D ≤ +8 V
		9		9	Ω max	
R_{ON} Match		1		1	Ω typ	V_D = 6 V, I_S = −10 mA
		3		3	Ω max	
LEAKAGE CURRENT						V_{DD} = +13.2 V
Source OFF Leakage I_S (OFF)	±0.01		±0.01		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V;
	±0.5	±3	±0.5	±20	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01		±0.01		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V;
	±0.5	±3	±0.5	±20	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.08		±0.08		nA typ	V_S = V_D = 12.2 V/1 V;
	±0.5	±3	±0.5	±40	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±0.00001		±0.00001	µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	105		105		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	150	220	150	220	ns max	V_S = +8 V; Test Circuit 4
t_{OFF}	40		40		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	60	100	60	100	ns max	V_S = +8 V; Test Circuit 4
t_{OPEN}	50		50		ns typ	R_L = 1 kΩ, C_L = 35 pF;
Charge Injection	2		2		pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF;
	6		6		pC max	V_{DD} = +12 V, V_{SS} = 0 V; Test Circuit 5
OFF Isolation	60		60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 6
Channel-to-Channel Crosstalk	100		100		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
C_S (OFF)	7		7		pF typ	f = 1 MHz
C_D (OFF)	10		10		pF typ	f = 1 MHz
C_D, C_S (ON)	16		16		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +13.2 V
I_{DD}						Digital Inputs = 0 V or 5 V
ADG441/ADG442		80		80	µA max	
ADG444	0.001		0.001		µA typ	
	1	2.5	1	2.5	µA max	
I_L (ADG444 Only)	0.001		0.001		µA typ	V_L = +5.5 V
	1	2.5	1	2.5	µA max	

NOTES
[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

Table I. Truth Table

ADG441/ADG444 IN	ADG442 IN	Switch Condition
0	1	ON
1	0	OFF

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG441BN	−40°C to +85°C	N-16
ADG441BR	−40°C to +85°C	R-16A
ADG441TQ	−55°C to +125°C	Q-16
ADG442BN	−40°C to +85°C	N-16
ADG442BR	−40°C to +85°C	R-16A
ADG444BN	−40°C to +85°C	N-16
ADG444BR	−40°C to +85°C	R-16A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]N = Plastic DIP, R = 0.15" Small Outline IC (SOIC), Q = Cerdip. For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS}	+44 V
V_{DD} to GND	–0.3 V to +25 V
V_{SS} to GND	+0.3 V to –25 V
V_L to GND	–0.3 V to V_{DD} + 0.3 V
Analog, Digital Inputs[2]	V_{SS} – 2 V to V_{DD} + 2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	100 mA
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Extended (T Version)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
Cerdip Package, Power Dissipation	900 mW
θ_{JA}, Thermal Impedance	76°C/W
Lead Temperature, Soldering (10 sec)	+300°C
Plastic Package, Power Dissipation	470 mW
θ_{JA}, Thermal Impedance	177°C/W
Lead Temperature, Soldering (10 sec)	+260°C
SOIC Package, Power Dissipation	600 mW
θ_{JA}, Thermal Impedance	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

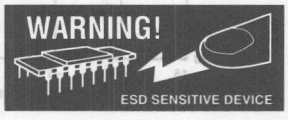
TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
V_{SS}	Most Negative Power Supply Potential in dual supplies. In single supply applications, it may be connected to ground.
V_L	Logic Power Supply (+5 V).
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R_{ON}	Ohmic resistance between D and S.
R_{ON} Match	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" Switch Source Capacitance.
C_D (OFF)	"OFF" Switch Drain Capacitance.
C_D, C_S (ON)	"ON" Switch Capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_{OPEN}	Break-Before-Make Delay when switches are configured as a multiplexer.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.

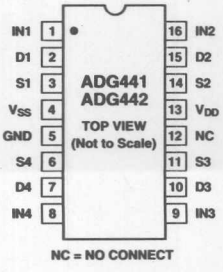
7

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

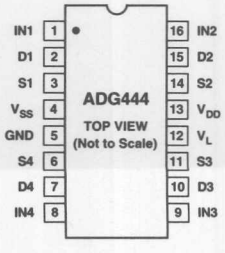


ADG441/ADG442 PIN CONFIGURATION (DIP/SOIC)



NC = NO CONNECT

ADG444 PIN CONFIGURATION (DIP/SOIC)



transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, the result being a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch up. With trench isolation, this diode is removed, the result being a latch-up proof switch.

Trench isolation also leads to lower leakage currents. The ADG441, ADG442 and ADG444 have a leakage current of 0.5 nA as compared with a leakage current of several nanoamperes in non-trench isolated switches. Leakage current is an important parameter in sample-and-hold circuits, this current being responsible for the discharge of the holding capacitor with time causing droop. The ADG441/ADG442/ADG444's low leakage current, along with its fast switching speeds, make it suitable for fast and accurate sample-and-hold circuits.

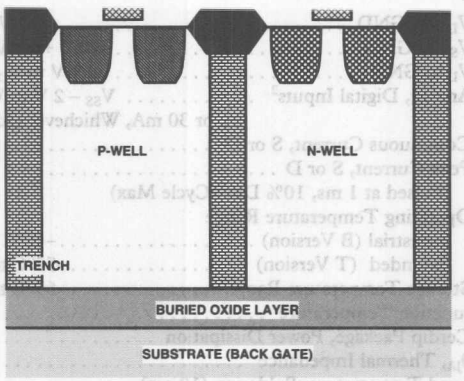


Figure 1. Trench Isolation

Typical Performance Characteristics

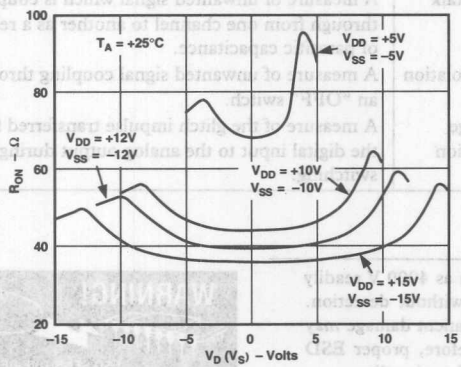


Figure 2. R_{ON} as a Function of V_D (V_S): Dual Supply

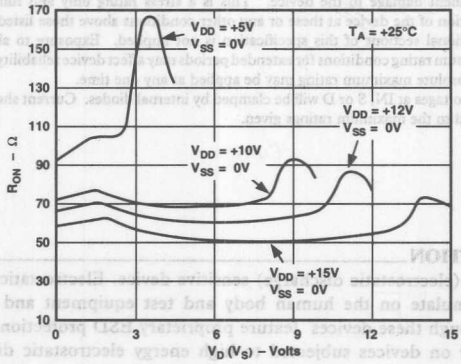


Figure 3. R_{ON} as a Function of V_D (V_S): Single Supply

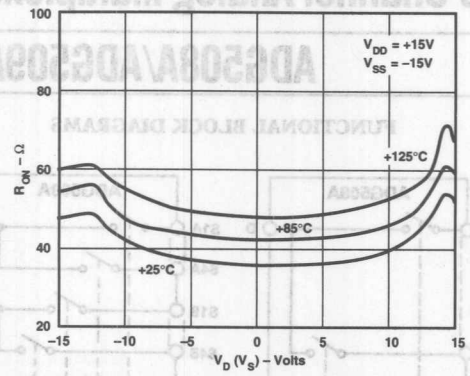


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures

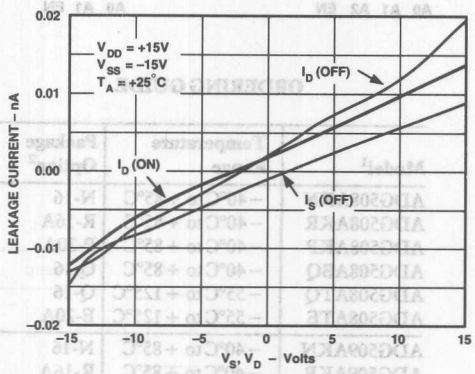


Figure 5. Leakage Currents as a Function of V_S (V_D)

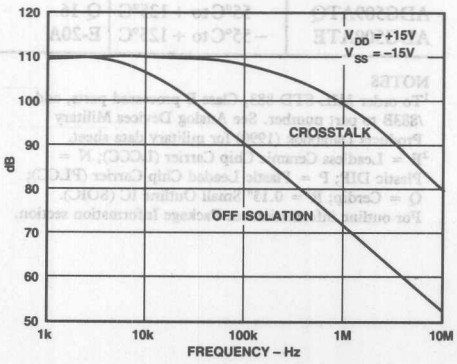


Figure 6. Crosstalk and Off Isolation vs. Frequency

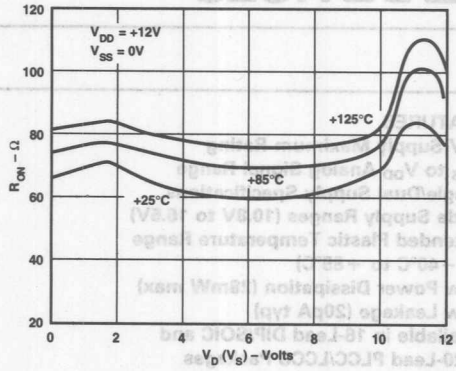


Figure 7. R_{ON} as a Function of V_D (V_S) for Different Temperatures

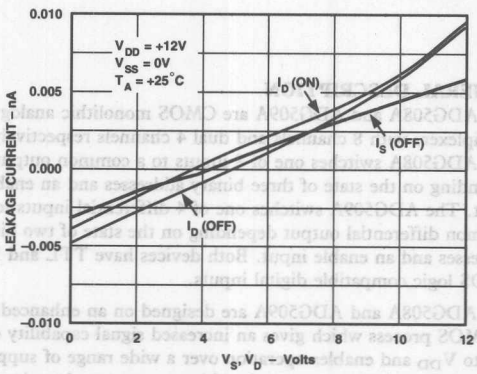


Figure 8. Leakage Currents as a Function of V_S (V_D)

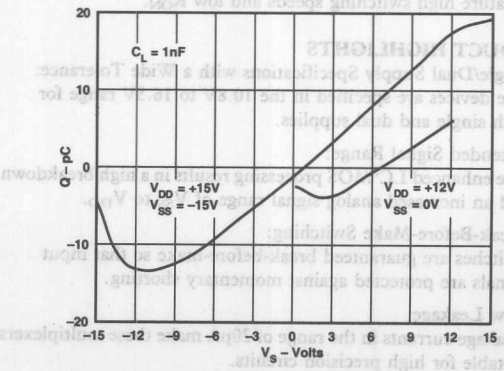


Figure 9. Charge Injection vs. Source Voltage

ANALOG DEVICES

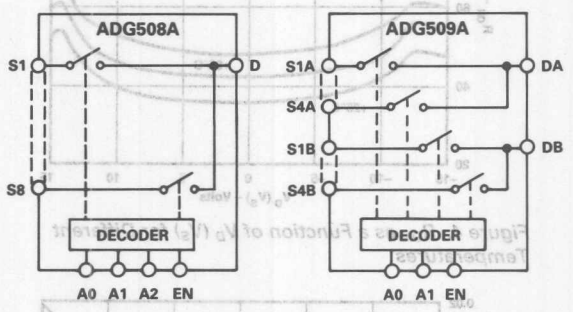
CMOS 4/8 Channel Analog Multiplexers

ADG508A/ADG509A

FEATURES

- 44V Supply Maximum Rating
- V_{SS} to V_{DD} Analog Signal Range
- Single/Dual Supply Specifications
- Wide Supply Ranges (10.8V to 16.5V)
- Extended Plastic Temperature Range (−40°C to +85°C)
- Low Power Dissipation (28mW max)
- Low Leakage (20pA typ)
- Available in 16-Lead DIP/SOIC and 20-Lead PLCC/LCCC Packages
- Superior Alternative to:
  - DG508A, HI-508
  - DG509A, HI-509

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG508A and ADG509A are CMOS monolithic analog multiplexers with 8 channels and dual 4 channels respectively. The ADG508A switches one of 8 inputs to a common output depending on the state of three binary addresses and an enable input. The ADG509A switches one of 4 differential inputs to a common differential output depending on the state of two binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG508A and ADG509A are designed on an enhanced LC²MOS process which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low R_{ON}.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:
   The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. Extended Signal Range:
   The enhanced LC²MOS processing results in a high breakdown and an increased analog signal range of V_{SS} to V_{DD}.
3. Break-Before-Make Switching:
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
4. Low Leakage:
   Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG508AKN	−40°C to +85°C	N-16
ADG508AKR	−40°C to +85°C	R-16A
ADG508AKP	−40°C to +85°C	P-20A
ADG508ABQ	−40°C to +85°C	Q-16
ADG508ATQ	−55°C to +125°C	Q-16
ADG508ATE	−55°C to +125°C	E-20A
ADG509AKN	−40°C to +85°C	N-16
ADG509AKR	−40°C to +85°C	R-16A
ADG509AKP	−40°C to +85°C	P-20A
ADG509ABQ	−40°C to +85°C	Q-16
ADG509ATQ	−55°C to +125°C	Q-16
ADG509ATE	−55°C to +125°C	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. See Analog Devices Military Products Databook (1990) for military data sheet.
[2]E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

DUAL SUPPLY (V_{DD} = +10.8V to +16.5V, V_{SS} = −10.8V to −16.5V unless otherwise noted.)

Parameter	ADG508A ADG509A K Version +25°C	ADG508A ADG509A K Version −40°C to +85°C	ADG508A ADG509A B Version +25°C	ADG508A ADG509A B Version −40°C to +85°C	ADG508A ADG509A T Version +25°C	ADG508A ADG509A T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	280		280		280		Ω typ	$-10V \le V_S \le +10V$, I_{DS} = 1mA; Test Circuit 1
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15V(±10%), V_{SS} = −15V(±10%)
					300	400	Ω max	V_{DD} = 15V(±5%), V_{SS} = −15V(±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	V_S = 0, I_{DS = 1mA
R_{ON} Match	5		5		5		% typ	$-10V \le V_S \le +10V$, I_{DS} = 1mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 3
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = V2 = ±10V; Test Circuit 4
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG509A only)		25		25		25	nA max	V1 = ±10V, V2 = ∓10V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	200		200		200		ns typ	V1 = ±10V, V2 = ∓10V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
t_{OFF} (EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 7V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG508A	22		22		22		pF typ	V_{EN} = 0.8V
ADG509A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		μA typ	V_{IN} = V_{INL} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

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ADG508A/ADG509A

SINGLE SUPPLY (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V unless otherwise noted.)

Parameter	ADG508A ADG509A K Version +25°C	ADG508A ADG509A K Version −40°C to +85°C	ADG508A ADG509A B Version +25°C	ADG508A ADG509A B Version −40°C to +85°C	ADG508A ADG509A T Version +25°C	ADG508A ADG509A T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	GND	GND	GND	GND	GND	GND	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	500		500		500		Ω typ	GND≤V_S≤+10V, I_{DS} = 0.5mA; Test Circuit 1
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	V_S = 0, I_{DS} = 0.5mA
R_{ON} Match	5		5		5		% typ	GND≤V_S≤+10V, I_{DS} = 0.5mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = +10V/GND, V2 = GND/+10V,
	1	50	1	50	1	50	nA max	Test Circuit 2
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/GND, V2 = GND/+10V;
ADG508A	1	100	1	100	1	100	nA max	Test Circuit 3
ADG509A	1	50	1	50	1	50	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = V2 = +10V/GND;
ADG508A	1	100	1	100	1	100	nA max	Test Circuit 4
ADG509A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG509A only)		25		25		25	nA max	V1 = +10V/GND, V2 = GND/+10V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	300		300		300		ns typ	V1 = +10V/GND, V2 = GND/+10V; Test Circuit 6
	450	600	450	600	450	600	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN)[1]	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
t_{OFF} (EN)[1]	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 3.5V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG508A	22		22		22		pF typ	V_{EN} = 0.8V
ADG509A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	10		10		10		mW typ	
		25		25		25	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

TERMINOLOGY

R_{ON}	Ohmic resistance between terminals D and S
R_{ON} Match	Difference between the R_{ON} of any two channels
R_{ON} Drift	Change in R_{ON} versus temperature
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_S (V_D)	Analog voltage on terminal S or D
C_S (OFF)	Channel input capacitance for "OFF" condition
C_D (OFF)	Channel output capacitance for "OFF" condition
C_{IN}	Digital input capacitance
t_{OFF} (EN)	Delay time between the 50% and 10% points of the digital input and switch "OFF" condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another
t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Maximum input voltage for Logic "0"
V_{INH}	Minimum input voltage for Logic "1"
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	−25V
Analog Inputs[2]	
Voltage at S, D	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D	20mA
Pulsed Current S or D 1ms Duration, 10% Duty Cycle	40mA
Digital Inputs[2]	
Voltage at A, EN	V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commercial (K Version)	−40°C to +85°C
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Overvoltage at A, EN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

TRUTH TABLES

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

ADG508A

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care

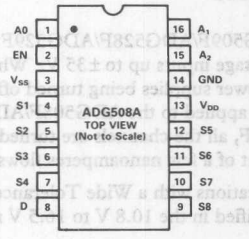
ADG509A

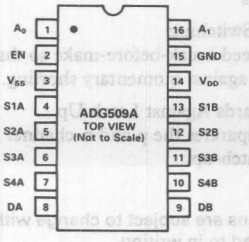
CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

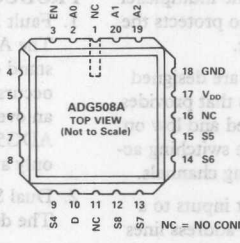
PIN CONFIGURATIONS

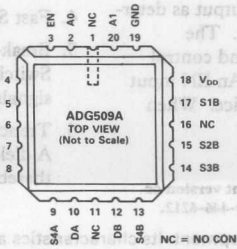
DIP, SOIC



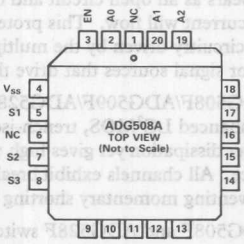


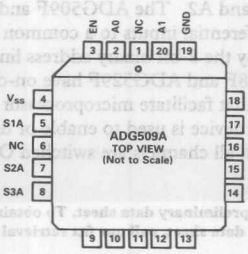
LCCC





PLCC





LC²MOS 4/8 Channel Fault-Protected Analog Multiplexers

ADG508F/ADG509F/ADG528F/ADG529F

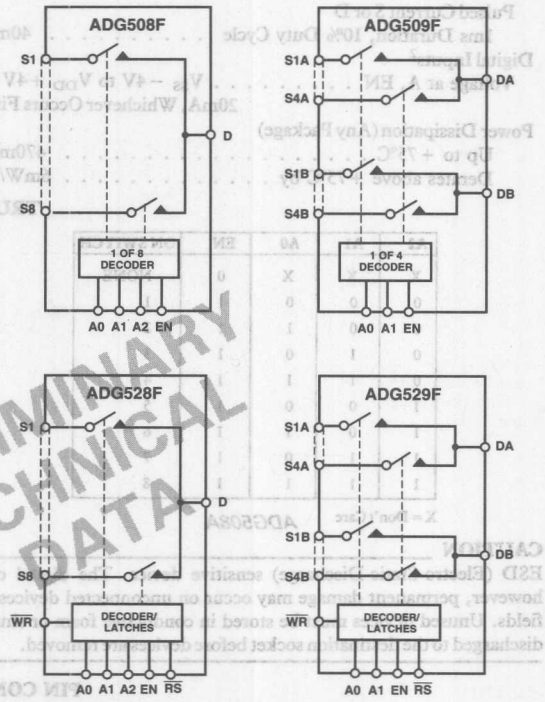
FEATURES

- Wide Supply Ranges (10.8 V to 16.5 V)
- Low On Resistance (300 Ω max)
- Fast Switching Times
  - t_{ON} 300 ns max
  - t_{OFF} 300 ns max
- Low Power Dissipation (3.3 mW max)
- Fault and Overvoltage Protection
- All Switches OFF with Power Supply OFF
- ON Channel Turns OFF if Overvoltage Occurs
- Latch-Up Proof Construction
- Break-Before-Make Construction
- TTL and CMOS Compatible Inputs
- Superior Alternative to
  - MAX358/MAX359
  - DG458/DG459

APPLICATIONS

- Data Acquisition Systems
- Industrial and Process Control Systems
- Avionics Test Equipment
- Signal Routing Between Systems
- High Reliability Control Systems

FUNCTIONAL BLOCK DIAGRAMS



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADG508F, ADG509F, ADG528F and ADG529F are CMOS analog multiplexers comprising eight single channels and four differential channels respectively which have fault protection. Using a series n-channel, p-channel, n-channel MOSFET structure, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs up to ±35 V. During fault conditions, the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources that drive the multiplexer.

The ADG508F/ADG509F/ADG528F/ADG529F are designed on an enhanced LC²MOS, trench-isolated process that provides low power dissipation yet gives high switching speed and low on resistance. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels.

The ADG508F and ADG528F switch one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG509F and ADG529F switch one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. The ADG528F and ADG529F have on-chip address and control latches that facilitate microprocessor interfacing. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched OFF.

PRODUCT HIGHLIGHTS

1. Fault Protection
   The ADG508F/ADG509F/ADG528F/ADG529F can withstand continuous voltage inputs up to ±35 V. When a fault occurs, due to the power supplies being turned off or due to an overvoltage being applied to the ADG508F/ADG509F/ADG528F/ADG529F, all the channels are turned off and only a leakage current of a few nanoamperes flows.
2. Dual Supply Specifications with a Wide Tolerance
   The devices are specified in the 10.8 V to 16.5 V range.
3. Low R_{ON}
4. Fast Switching Times
5. Break-Before-Make Switching
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
6. Trench Isolation Guards Against Latch Up
   A dielectric trench separates the p and n-channel MOSFETs thereby preventing latch-up.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SPECIFICATIONS[1]

Dual Supply (V_{DD} = +10.8 V to +16.5 V, V_{SS} = −10.8 V to −16.5 V, GND = 0 V, unless otherwise noted)

Parameter	B Version		T Version			
	+25°C	−40°C to +85°C	+25°C	−55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} + 3		V_{SS} + 3	V min	
		V_{DD} − 0.7		V_{DD} − 0.7	V max	
R_{ON}	300	400	300	400	Ω max	−10 V ≤ V_S ≤ +10 V, I_S = 1 mA; V_{DD} = +15 V ± 5%, V_{SS} = −15 V ± 5%
	200	250	200	250	Ω typ	−5 V ≤ V_S ≤ +5 V, I_S = 1 mA; V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%
R_{ON} Drift	0.6		0.6		%/°C typ	V_S = 0 V, I_{DS} = 1 mA
R_{ON} Match	5		5		% typ	−10 V ≤ V_S ≤ +10 V, I_S = 1 mA; V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	±0.02		±0.02		nA typ	V_D = ±10 V, V_S = ∓10 V;
	±0.5	±50	±0.5	±50	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.04		±0.04		nA typ	V_D = ±10 V, V_S = ∓10 V;
ADG508F/ADG528F	±1	±100	±1	±100	nA max	Test Circuit 3
ADG509F/ADG529F	±1	±50	±1	±50	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.04		±0.04		nA typ	V_S = V_D = ±10 V;
ADG508F/ADG528F	±1	±100	±1	±100	nA max	Test Circuit 4
ADG509F/ADG529F	±1	±50	±1	±50	nA max	
FAULT						
Output Leakage Current	±0.02		±0.02		nA typ	V_S = ±33 V, V_D = 0 V
(With Overvoltage)		±2		±2	µA max	
Input Leakage Current	±0.005		±0.005		µA typ	V_S = ±25 V, V_D = ±25 V
(With Overvoltage)	±5		±10		µA max	
Input Leakage Current	±0.001		±0.001		µA typ	V_S = ±25 V, V_D = V_{EN} = 0 V,
(With Power Supplies Off)	±2		±5		µA max	V_{IN} = 0 V or 5 V
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±1		±1	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	5		5		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	200		200		ns typ	R_L = 1 MΩ, C_L = 35 pF;
	300	400	300	400	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V; Test Circuit 5
t_{OPEN}	50		50		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	25	10	25	10	ns max	V_S = +5 V; Test Circuit 6
t_{ON} (EN)	200		200		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	300	400	300	400	ns max	V_S = +5 V; Test Circuit 7
t_{OFF} (EN)	200		200		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	300	400	300	400	ns max	V_S = +5 V; Test Circuit 7
t_{SETT}, Settling Time						
0.1%		0.6		0.6	µs typ	
0.01%		1.7		1.7	µs typ	
t_W, Write Pulse Width	100	120	100	130	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulse Width		100		100	ns min	
Charge Injection	15		15		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 8
OFF Isolation	68		68		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
	50		50		dB min	V_S = 7 V rms; Test Circuit 9
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz; Test Circuit 11
C_S (OFF)	5		5		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG508F/ADG528F	15		15		pF typ	
ADG509F/ADG529F	10		10		pF typ	
POWER REQUIREMENTS						
I_{DD}	0.05		0.05		mA typ	V_{IN} = V_{INL} or V_{INH}
	0.1	0.2	0.1	0.2	mA max	
I_{SS}	0.01		0.01		mA typ	
	0.1	0.2	0.1	0.2	mA max	

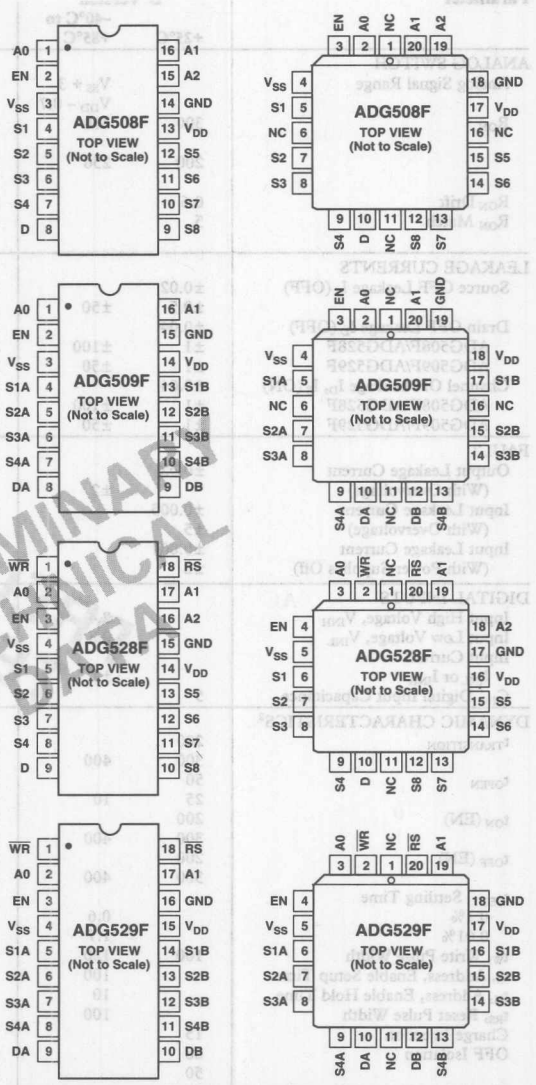
NOTES
[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

V_{DD} to GND ..... –0.3 V to +25 V
V_{SS} to GND ..... +0.3 V to –25 V
V_{EN}, V_A Digital Input ..... V_{SS} – 4 V to V_{DD} + 4 V
V_S, Analog Input Overvoltage with Power ON. .... V_{SS} – 20 V to V_{DD} + 20 V
V_S, Analog Input Overvoltage with Power OFF ..... –35 V to +35 V
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle max) ..... 40 mA
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Extended (T Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Cerdip Package, Power Dissipation ..... 900 mW
θ_{JA}, Thermal Impedance ..... 76°C/W
Lead Temperature, Soldering (10 sec) ..... +300°C
Plastic Package, Power Dissipation ..... 470 mW
θ_{JA}, Thermal Impedance ..... 117°C/W
Lead Temperature, Soldering (10 sec) ..... +260°C
SOIC Package, Power Dissipation ..... 600 mW
θ_{JA}, Thermal Impedance. ..... 77°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
PLCC Package, Power Dissipation ..... 800 mW
θ_{JA}, Thermal Impedance ..... 90°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.



PRELIMINARY TECHNICAL DATA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG508FBN	–40°C to +85°C	N-16
ADG508FBR	–40°C to +85°C	R-16A
ADG508FBP	–40°C to +85°C	P-20A
ADG508FTQ	–55°C to +125°C	Q-16
ADG509FBN	–40°C to +85°C	N-16
ADG509FBR	–40°C to +85°C	R-16A
ADG509FBP	–40°C to +85°C	P-20A
ADG509FTQ	–55°C to +125°C	Q-16
ADG528FBN	–40°C to +85°C	N-18
ADG528FBP	–40°C to +85°C	P-20A
ADG528FTQ	–55°C to +125°C	Q-18
ADG529FBN	–40°C to +85°C	N-18
ADG529FBP	–40°C to +85°C	P-20A
ADG529FTQ	–55°C to +125°C	Q-18

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.

Table I. ADG508F Truth Table

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

Table II. ADG509F Truth Table

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care.

PRELIMINARY TECHNICAL DATA

Table III. ADG528F Truth Table

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X	↑	1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care

Table IV. ADG529F Truth Table

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	↑	1	Retains Previous Switch Condition
X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

X = Don't Care

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

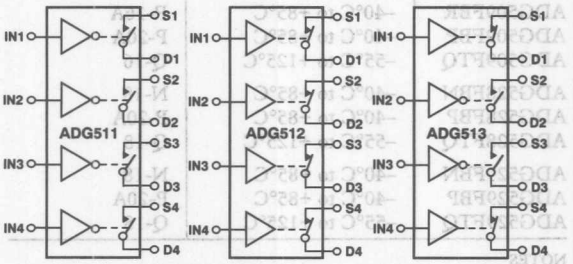
DI LC²MOS
Precision 5 V/3 V Quad SPST Switches

ADG511/ADG512/ADG513

FEATURES
- +3 V, +5 V or ±5 V Power Supplies
- Ultralow Power Dissipation (<0.5 μW)
- Low Leakage (<100 pA)
- Low On Resistance (<50 Ω)
- Fast Switching Times
- Low Charge Injection
- Latch-Up Proof
- TTL/CMOS Compatible
- 16-Pin DIP or SOIC Package

APPLICATIONS
- Battery Powered Instruments
- Single Supply Systems
- Remote Powered Equipment
- +5 V Supply Systems
- Computer Peripherals such as Disk Drives
- Precision Instrumentation
- Audio and Video Switching
- Automatic Test Equipment
- Precision Data Acquisition
- Sample Hold Systems
- Communication Systems
- Compatible with ±5 V Supply DACs and ADCs such as AD7840/8, AD7870/1/2/4/5/6/8

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "1" INPUT

The ADG511, ADG512 and ADG513 contain four independent SPST switches. The ADG511 and ADG512 differ only in that the digital control logic is inverted. The ADG511 switch is turned on with a logic low on the appropriate control input, while a logic high is required for the ADG512. The ADG513 contains two switches whose digital control logic is similar to that of the ADG511 while the logic is inverted in the remaining two switches.

GENERAL DESCRIPTION

The ADG511, ADG512 and ADG513 are monolithic CMOS ICs containing four independently selectable analog switches. These switches feature low, well-controlled on resistance and wide analog signal range, making them ideal for precision analog signal switching.

These switch arrays are fabricated using Analog Devices' advanced linear compatible CMOS (LC²MOS) process which offers the additional benefits of low leakage currents, ultralow power dissipation and low capacitance for fast switching speeds with minimum charge injection. These features make the ADG511, ADG512 and ADG513 the optimum choice for a wide variety of signal switching tasks in precision analog signal processing and data acquisition systems.

The ability to operate from single +3 V, +5 V or ±5 V bipolar supplies make the ADG511, ADG512 and ADG513 perfect for use in battery-operated instruments, 4–20 mA loop systems and with the new generation of DACs and ADCs from Analog Devices. The use of 5 V supplies and reduced operating currents give much lower power dissipation than devices operating from ±15 V supplies.

PRODUCT HIGHLIGHTS

1. +5 Volt Single Supply Operation
   The ADG511/ADG512/ADG513 offers high performance, including low on resistance and wide signal range, fully specified and guaranteed with +3 V, ±5 V as well as +5 V supply rails.
2. Ultralow Power Dissipation
   CMOS construction ensures ultralow power dissipation.
3. Low R_{ON}
4. Trench Isolation Guards Against Latch-up
   A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
5. Break Before Make Switching
   Switches are guaranteed to have break-before-make operation. This allows multiple outputs to be tied together for multiplexer applications without the possibility of momentary shorting between channels.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS[1]

Dual Supply (V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version −40°C to +25°C	B Version −40°C to +85°C	T Version −55°C to +25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{DD} to V_{SS}		V_{DD} to V_{SS}	V	
R_{ON}	30		30		Ω typ	V_D = ±3.5 V, I_S = −10 mA;
		50		50	Ω max	V_{DD} = +4.5 V, V_{SS} = −4.5 V
LEAKAGE CURRENTS						V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source OFF Leakage I_S (OFF)	±0.025		±0.025		nA typ	V_D = ±4.5 V, V_S = ∓4.5 V;
	±0.1	±2.5	±0.1	±2.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.025		±0.025		nA typ	V_D = ±4.5 V, V_S = ∓4.5 V;
	±0.1	±2.5	±0.1	±2.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.05		±0.05		nA typ	V_D = V_S = ±4.5 V;
	±0.2	±5	±0.2	±5	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1		±0.1	μA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	200		200		ns typ	R_L = 300 Ω, C_L = 35 pF;
		375		375	ns max	V_S = ±3 V; Test Circuit 4
t_{OFF}	120		120		ns typ	R_L = 300 Ω, C_L = 35 pF;
		150		150	ns max	V_S = ±3 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG513 Only)	100		100		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +3 V; Test Circuit 5
Charge Injection	11		11		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						
V_{DD}		+4.5/5.5		+4.5/5.5	V min/max	
V_{SS}		−4.5/−5.5		−4.5/−5.5	V min/max	
I_{DD}	0.0001		0.0001		μA typ	V_{DD} = +5.5 V, V_{SS} = −5.5 V
		1		1	μA max	Digital Inputs = 0 V or 5 V
I_{SS}	0.0001		0.0001		μA typ	
		1		1	μA max	

NOTES

[1]Temperature ranges are as follows: B Versions −40°C to +85°C; T Versions −55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Parameter	B Version −40°C to +25°C	B Version −40°C to +85°C	T Version −55°C to +25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		0 V to V_{DD}		0 V to V_{DD}	V	
R_{ON}	45		45		Ω typ	V_D = 3.5 V, I_S = −10 mA;
		75		75	Ω max	V_{DD} = +4.5 V
LEAKAGE CURRENTS						V_{DD} = +5.5 V
Source OFF Leakage I_S (OFF)	±0.025		±0.025		nA typ	V_D = 4.5/1 V, V_S = 1/4.5 V;
	±0.1	±2.5	±0.1	±2.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.025		±0.025		nA typ	V_D = 4.5/1 V, V_S = 1/4.5 V;
	±0.1	±2.5	±0.1	±2.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.05		±0.05		nA typ	V_D = V_S = +4.5 V/+1 V;
	±0.2	±5	±0.2	±5	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1		±0.1	μA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	250		250		ns typ	R_L = 300 Ω, C_L = 35 pF;
		500		500	ns max	V_S = +2 V; Test Circuit 4
t_{OFF}	50		50		ns typ	R_L = 300 Ω, C_L = 35 pF;
		100		100	ns max	V_S = +2 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG513 only)	200		200		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +2 V; Test Circuit 5
Charge Injection	16		16		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						
V_{DD}		4.5/5.5		4.5/5.5	V min/max	
I_{DD}	0.0001		0.0001		μA typ	V_{DD} = +5.5 V
		1		1	μA max	Digital Inputs = 0 V or 5 V

NOTES
[1]Temperature ranges are as follows: B Versions −40°C to +85°C; T Versions −55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

Single Supply (V_{DD} = +3.3 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version 0°C to +70°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
R_{ON}	200		Ω typ	V_D = 1.5 V, I_S = −1 mA;
		500	Ω max	V_{DD} = +3 V
LEAKAGE CURRENTS				V_{DD} = +3.6 V
Source OFF Leakage I_S (OFF)	±0.025		nA typ	V_D = 2.6/1 V, V_S = 1/2.6 V;
	±0.1	±2.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.025		nA typ	V_D = 2.6/1 V, V_S = 1/2.6 V;
	±0.1	±2.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.05		nA typ	V_D = V_S = +2.6 V/+1 V;
	±0.2	±5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	600		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1200	ns max	V_S = +1 V; Test Circuit 4
t_{OFF}	100		ns typ	R_L = 300 Ω, C_L = 35 pF;
		160	ns max	V_S = +1 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG513 only)	500		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +1 V; Test Circuit 5
Charge Injection	11		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		pF typ	f = 1 MHz
C_D (OFF)	9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		pF typ	f = 1 MHz
POWER REQUIREMENTS				
V_{DD}		3/3.6	V min/max	
I_{DD}	0.0001		µA typ	V_{DD} = +3.6 V
		1	µA max	Digital Inputs = 0 V or 3 V

NOTES
[1]Temperature range is as follows: B Version 0°C to +70°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . . +44 V
V_{DD} to GND . . . . . −0.3 V to +25 V
V_{SS} to GND . . . . . +0.3 V to −25 V
Analog, Digital Inputs[1] . . . . . V_{SS} −2 V to V_{DD} +2 V or 30 mA, whichever occurs first
Continuous Current, S or D . . . . . 30 mA
Peak Current, S or D . . . . . 100 mA
(Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +150°C
Cerdip Package, Power Dissipation . . . . . 900 mW
θ_{JA} Thermal Impedance . . . . . 76°C/W
Lead Temperature, Soldering (10 sec) . . . . . +300°C
Plastic Package, Power Dissipation . . . . . 470 mW
θ_{JA} Thermal Impedance . . . . . 117°C/W
Lead Temperature, Soldering (10 sec) . . . . . +260°C
SOIC Package, Power Dissipation . . . . . 600 mW
θ_{JA} Thermal Impedance . . . . . 77°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[1]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the ADG511/ADG512/ADG513 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Option[3]
ADG511BN	−40°C to +85°C	N-16
ADG511BR	−40°C to +85°C	R-16A
ADG511TQ	−55°C to +125°C	Q-16
ADG512BN	−40°C to +85°C	N-16
ADG512BR	−40°C to +85°C	R-16A
ADG512TQ	−55°C to +125°C	Q-16
ADG513BN	−40°C to +85°C	N-16
ADG513BR	−40°C to +85°C	R-16A

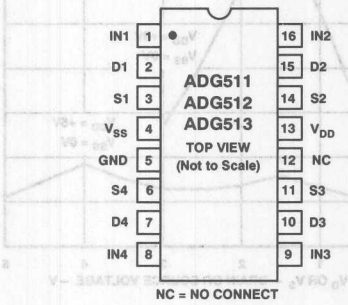
NOTES

[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.

[2]3.3 V specifications apply over 0°C to +70°C temperature range.

[3]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); Q = Cerdip. For outline information see Package Information section.

PIN CONFIGURATION (DIP/SOIC)



NC = NO CONNECT

Truth Table (ADG511/ADG512)

ADG511 In	ADG512 In	Switch Condition
0	1	ON
1	0	OFF

Truth Table (ADG513)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
R_{ON}	Ohmic resistance between D and S.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" switch source capacitance.
C_D (OFF)	"OFF" switch drain capacitance.
C_D, C_S (ON)	"ON" switch capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_D	"OFF" or "ON" time measured between the 90% points of both switches when switching from one address state to another.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.

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ADG511/ADG512/ADG513—Typical Performance Graphs

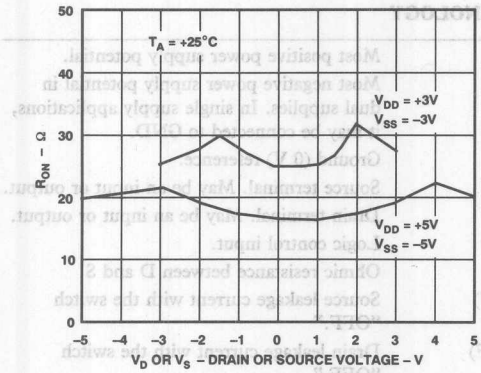

Figure 1. On Resistance as a Function of V_D (V_S) Dual Supplies

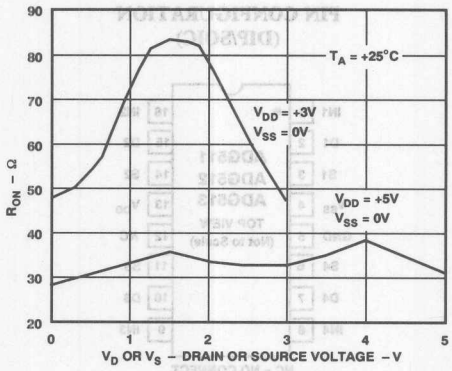

Figure 3. On Resistance as a Function of V_D (V_S) Single Supply

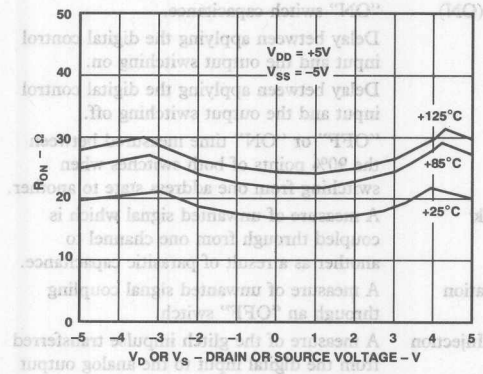

Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures

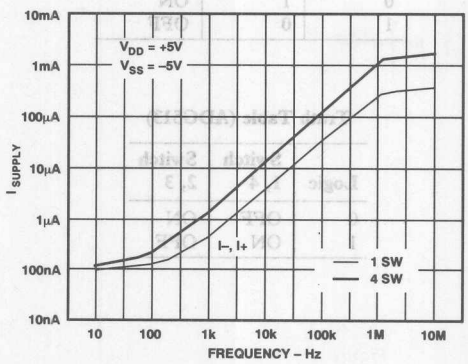

Figure 4. Supply Current vs. Input Switching Frequency

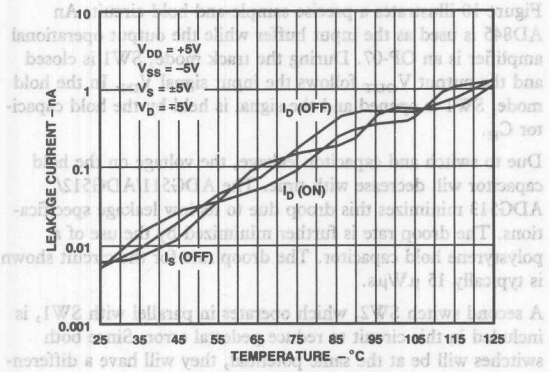

Figure 5. Leakage Currents as a Function of Temperature

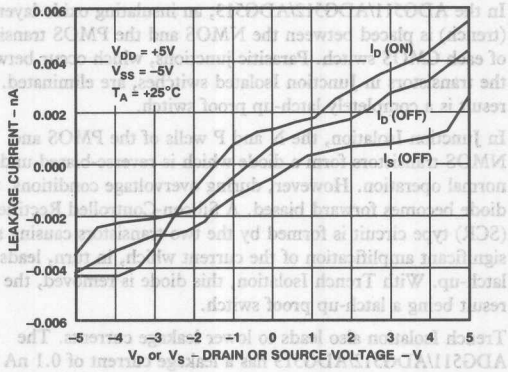

Figure 7. Leakage Currents as a Function of V_D (V_S)

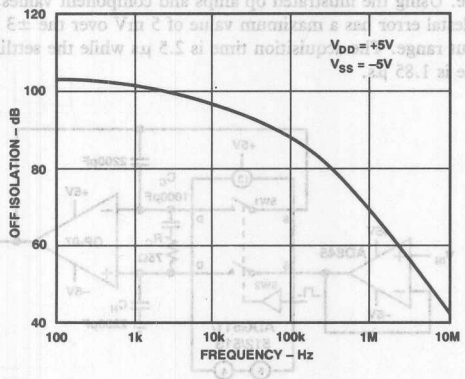

Figure 6. Off Isolation vs. Frequency

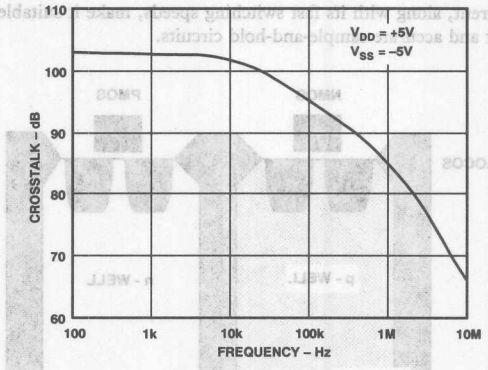

Figure 8. Crosstalk vs. Frequency

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(trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in Junction Isolated switches, are eliminated. The result is a completely latch-up proof switch.

In Junction Isolation, the N and P wells of the PMOS and NMOS transistors form a diode which is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A Silicon-Controlled Rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch-up. With Trench Isolation, this diode is removed, the result being a latch-up proof switch.

Trench Isolation also leads to lower leakage currents. The ADG511/ADG512/ADG513 has a leakage current of 0.1 nA as compared with a leakage current of several nanoamps in non-Trench Isolated switches. Leakage current is an important parameter in sample-and-hold circuits, this current being responsible for the discharge of the holding capacitor with time causing droop. The ADG511/ADG512/ADG513's low leakage current, along with its fast switching speeds, make it suitable for fast and accurate sample-and-hold circuits.

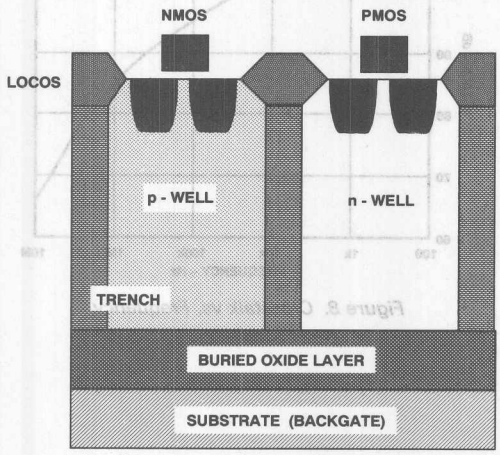

Figure 9. Trench Isolation

AD845 is used as the input buffer while the output operational amplifier is an OP-07. During the track mode, SW1 is closed and the output V_{OUT} follows the input signal V_{IN}. In the hold mode, SW1 is opened and the signal is held by the hold capacitor C_H.

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG511/ADG512/ADG513 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically 15 μV/μs.

A second switch SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp OP-07 which will minimize charge injection effects. Pedestal error is also reduced by the compensation network R_C and C_C. This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ±3 V input range. The acquisition time is 2.5 μs while the settling time is 1.85 μs.

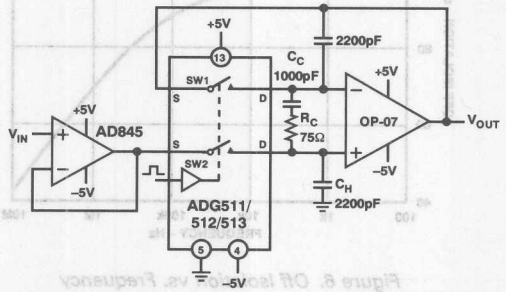

Figure 10. Accurate Sample-and-Hold

ANALOG DEVICES

8-Chan/Dual 4-Chan JFET Analog Multiplexers (Overvoltage & Power Supply Loss Protected)

MUX08/MUX24

FEATURES

- **JFET Switches Rather Than CMOS**
- **Low "ON" Resistance ..... 220Ω Typ**
- **Highly Resistant to Static Discharge Damage**
- **No SCR Latch-Up Problems**
- **Digital Inputs Compatible With TTL and CMOS**
- **125° C Temperature Tested Dice Available**
- **MUX-08 Pin Compatible With DG508, HI-508A, IH5108, IH6108, LF11508/12508/13508, AD7506**
- **MUX-24 Pin Compatible With DG509, HI-509A, IH5208, IH6208, LF11509/12509/13509, AD7507**
- **Available in Surface Mount Packages**
- **Available in Die Form**

ORDERING INFORMATION †

25°C ON RESISTANCE	PACKAGE CERDIP 16-PIN	PACKAGE PLASTIC 16-PIN	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
220Ω	MUX08AQ*	–	–	MIL
	MUX08EQ	–	–	IND
	–	MUX08EP	–	COM
300Ω	MUXO8BQ*	–	MUX08BRC/883	MIL
	MUX08FQ	–	–	IND
	–	MUX08FP	–	XIND
	–	MUX08FS††	–	XIND
220Ω	MUX24AQ*	–	–	MIL
	MUX24EQ	–	–	IND
	–	MUX24EP	–	COM
300Ω	MUX24BQ*	–	–	MIL
	MUX24FQ	–	–	IND
	–	MUX24FP	–	XIND
	–	MUX24FS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The MUX-08 is a monolithic eight-channel analog multiplexer which connects a single output to one of the eight analog inputs depending upon the state of a 3-bit binary address.

The MUX-24 is a monolithic four-channel differential analog multiplexer configured in a double pole, four-position (plus OFF) electronic switch array. A two-bit binary input address connects a pair of independent analog inputs from each four-channel input section to the corresponding pair of independent analog outputs.

All switches in the MUX-08/MUX-24 are turned OFF by applying logic "0" to the ENABLE pin, thereby providing a package select function.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance, low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors over the full operating temperature range.

For single sixteen-channel and dual eight-channel models, refer to the MUX-16/MUX-28 data sheet.

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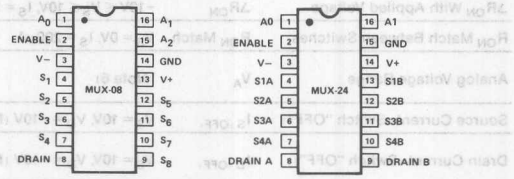
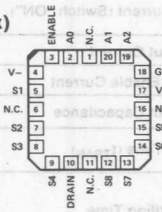
PIN CONNECTIONS



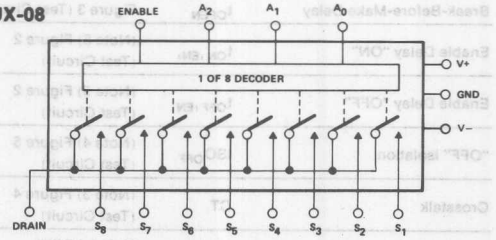
16-PIN CERDIP (Q-Suffix)
16-PIN PLASTIC DIP (P-Suffix)
16-PIN SO (S-Suffix)



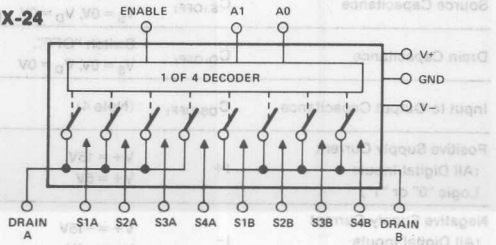
20-CONTACT LCC (RC-Suffix)

FUNCTIONAL DIAGRAMS

MUX-08



MUX-24



ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range
- MUX-08/24-AQ, BQ, BRC ..... –55°C to +125°C
- MUX-02/24-EQ, FQ ..... –25°C to +85°C
- MUX-08/24-EP ..... 0°C to +70°C
- MUX-08/24-FP, FS ..... –40°C to +85°C

Junction Temperature (T_j) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
P-Suffix ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply to V– Supply 36V
Logic Input Voltage ..... (–4V or V–) to V+ Supply
Analog Input Voltage ..... V– Supply –20V to V+ Supply +20V
Maximum Current Through Any Pin 25mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	98	38	°C/W
16-Pin SO (S)	111	35	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V+ = +15V, V– = –15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-08A/E MUX-24A/E MIN	TYP	MAX	MUX-08B/F MUX-24B/F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_S \le 10V$, $I_S \le 200\mu A$		—	220	300	—	300	400	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_S \le 10V$, $I_S = 200\mu A$		—	1	5	—	3	7	%
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, $I_S = 200\mu A$		—	7	15	—	9	20	%
Analog Voltage Range	V_A	(Note 6)		+10 –10	+10.4 –15	— —	+10 –10	+10.4 –15	— —	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	V_S = 10V, V_D = –10V (Note 1)		—	0.01	1.0	—	0.01	2.0	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	V_S = 10V, V_D = –10V (Note 1)	MUX-08 MUX-24	— —	0.1 0.05	1.0 1.0	— —	0.1 0.05	2.0 2.0	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+I_{S(ON)}$	V_D = 10V (Note 1)	MUX-08 MUX-24	— —	0.1 0.05	1.0 1.0	— —	0.1 0.05	2.0 2.0	nA
Digital Input Current	I_{IN}	V_{IN} = 0.4V to 15V		—	1	10	—	1	10	μA
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.4V		—	4	10	—	4	10	μA
Digital Input Capacitance	C_{DIG}			—	3	—	—	3	—	pF
Switching Time (t_{TRAN})	t_{PHL} t_{PLH}	(Notes 2, 5) Figure 1 (Test Circuit)		— —	1.5 1.0	2.1 1.3	— —	1.5 1.0	2.1 1.3	μs
Output Settling Time	t_S	10V Step to 0.10% 10V Step to 0.05% 10V Step to 0.02%		— — —	2.2 2.7 3.4	— — —	— — —	2.2 2.7 3.4	— — —	μs
Break-Before-Make Delay	t_{OPEN}	Figure 3 (Test Circuit)		—	0.8	—	—	1.0	—	μs
Enable Delay "ON"	$t_{ON(EN)}$	(Note 5) Figure 2 (Test Circuit)		—	1	2	—	1	2	μs
Enable Delay "OFF"	$t_{OFF(EN)}$	(Note 5) Figure 2 (Test Circuit)	MUX-08 MUX-24	— —	0.1 0.2	0.4 0.5	— —	0.2 0.3	0.4 0.6	μs
"OFF" Isolation	ISO_{OFF}	(Note 4) Figure 5 (Test Circuit)	MUX-08 MUX-24	— —	60 66	— —	— —	60 66	— —	dB
Crosstalk	CT	(Note 3) Figure 4 (Test Circuit)	MUX-08 MUX-24	— —	70 76	— —	— —	70 76	— —	dB
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	MUX-08 MUX-24	— —	2.5 2	— —	— —	2.5 2	— —	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	MUX-08 MUX-24	— —	7 4	— —	— —	7 4	— —	pF
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 4)	MUX-08 MUX-24	— —	0.3 0.15	— —	— —	0.3 0.15	— —	pF
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I+	V+ = 15V V+ = 5V		— —	10 8	12 —	— —	6 5	12 —	mA
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I–	V+ = –15V V+ = –5V		— —	3.0 2.5	3.8 —	— —	2.0 1.8	3.8 —	mA

ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-08A/ MUX-24A MIN	TYP	MAX	MUX-08B/ MUX-24B MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_S \le 10V$, $I_S \le 200\mu A$		—	—	400	—	—	500	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_S \le 10V$, $I_S = 200\mu A$		—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$		—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)		+10 −10	+10.4 −15	— —	+10 −10	+10.4 −15	— —	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)		—	—	25	—	—	50	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)	MUX-08 MUX-24	— —	— —	100 50	— —	— —	500 500	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ + $I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24	— —	— —	100 50	— —	— —	500 500	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)		2	—	—	2	—	—	V
Digital "0" Input Voltage	V_{INL}	(Note 6)		—	—	0.7	—	—	0.7	V
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$		—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"		—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0" or "1"		—	—	5	—	—	5	mA

ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and −25°C ≤ T_A +85°C for MUX-08EQ/FQ and MUX-24EQ/FQ; 0°C ≤ T_A ≤ +70°C for MUX-08EP and MUX-24EP; −40°C ≤ T_A ≤ +85°C for MUX-08FP/FS and MUX-24FP/FS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-08E/ MUX-24E MIN	TYP	MAX	MUX-08F/ MUX-24F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_S \le 10V$, $I_S \le 200\mu A$		—	—	400	—	—	500	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_S \le 10V$, $I_S = 200\mu A$		—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$		—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)		+10 −10	+10.4 −15	— —	+10 −10	+10.4 −15	— —	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)		—	—	10	—	—	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)	MUX-08 MUX-24	— —	— —	100 50	— —	— —	100 50	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ + $I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24	— —	— —	100 50	— —	— —	100 50	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)		2	—	—	2	—	—	V
Digital "0" Input Voltage	V_{INL}	(Note 6)		—	—	0.8	—	—	0.8	V
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$		—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"		—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0" or "1"		—	—	5	—	—	5	mA

NOTES:

1. Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".
2. $R_L = 10M\Omega$, $C_L = 10pF$.
3. Crosstalk is measured by driving channel 8 with channel 4 "ON". $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz.
4. "OFF" isolation is measured by driving channel 8 with ALL channels "OFF". $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz. C_{DS} is computed from the OFF isolation measurement.
5. Sample tested.
6. Guaranteed by leakage current and R_{ON} tests.
7. Leakage tests are performed only on military temperature grades at 125°C.

FEATURES

- **JFET Switches Rather Than CMOS**
- **Highly Resistant To Static Discharge Damage**
- **No SCR Latch-up Problems**
- **Low "ON" Resistance — 290Ω Typical**
- **Low Leakage Current**
- **Digital Inputs Compatible With TTL and CMOS**
- **Break-Before-Make Action**
- **125° C Temperature-Tested Dice Available**
- **Overvoltage Protected**
- **Supply Loss Protection**
- **MUX-16 Pin Compatible With DG506, HI-506A, AD7506**
- **MUX-28 Pin Compatible With DG507, HI-507A, AD7507**
- **Available In Die Form**

ORDERING INFORMATION †

25°C RESISTANCE	PACKAGE CERDIP 28-PIN	PACKAGE LCC 28-CONTACT	PACKAGE PLASTIC 28-PIN	OPERATING TEMPERATURE RANGE
290Ω	MUX16AT*	–	–	MIL
290Ω	MUX16ET	–	–	IND
400Ω	MUX16BT*	MUX16BTC/883	–	MIL
400Ω	MUX16FT	–	MUX16FP	XIND
400Ω	–	–	MUX16FPC	XIND
290Ω	MUX28AT*	–	–	MIL
290Ω	MUX28ET	–	–	IND
400Ω	MUX28BT*	MUX28BTC/883	–	MIL
400Ω	MUX28FT	–	MUX28FP	XIND
400Ω	–	–	MUX28FPC	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

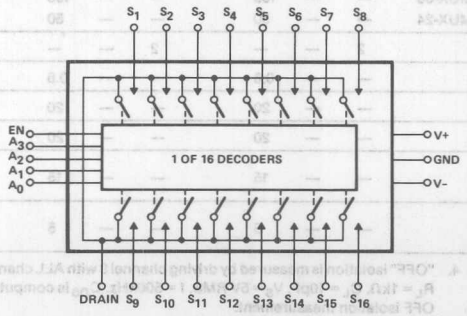
The MUX-16 is a monolithic 16-channel analog multiplexer which connects a single output to 1 of the 16 analog inputs depending upon the state of a 4-bit binary address. Disconnection of the output is provided by a logical "0" at the ENABLE input, thereby providing a package selection function.

The MUX-28 is a monolithic 8-channel differential analog multiplexer configured in a double pole, 8-position (plus OFF) electronic switch array. A 3-bit binary input address connects a pair of independent analog inputs from each 8-channel input section to the corresponding pair of independent analog outputs. Disconnection of both inputs is provided by a logical "0" at the ENABLE input, thereby offering a package select function.

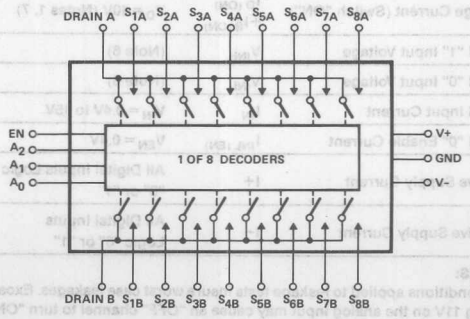
Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static discharge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors. For single 8-channel and dual 4-channel models, refer to the MUX-08/MUX-24 data sheet.

FUNCTIONAL DIAGRAMS

MUX-16

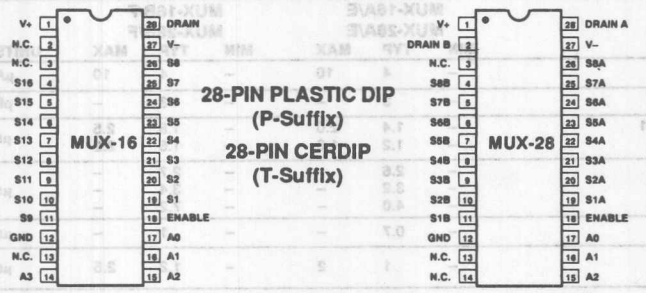


MUX-28



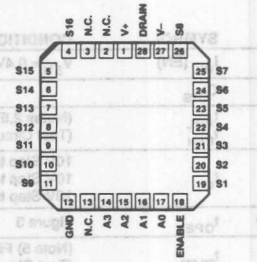
This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PIN CONNECTIONS & TRUTH TABLES



28-PIN PLASTIC DIP (P-Suffix)

28-PIN CERDIP (T-Suffix)



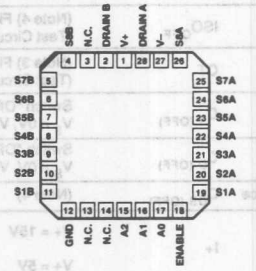
MUX-16BTC/883
LCC
(TC-Suffix)
PLCC
(PC-Suffix)

MUX-16

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

MUX-28

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8



MUX-28BTC/883
LCC
(TC-Suffix)
PLCC
(PC-Suffix)

7

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range,
MUX-16/28-AT, BT, BTC ..... –55°C to +125°C
MUX-16/28-ET ..... –25°C to +85°C
MUX-16/28-FP, FPC, FT ..... –40°C to +85°C
Junction Temperature (T_j) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply to V– Supply 36V
Logic Input Voltage ..... (V– or –4V) to V+ Supply
Analog Input Voltage ..... V– Supply –20V to V+ Supply +20V

Maximum Current Through Any Pin 25mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
28-Pin Hermetic DIP (T)	55	15	°C/W
28-Pin Plastic DIP (P)	56	30	°C/W
28-Contact LCC (TC)	86	35	°C/W
28-Contact PLCC (PC)	70	33	°C/W

NOTES:
1. Ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for PLCC package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-16A/E MUX-28A/E MIN	TYP	MAX	MUX-16B/F MUX-28B/F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_S \le 10V$, $I_S \le 200\mu A$		—	290	380	—	400	580	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_S \le 10V$, $I_S = 200\mu A$		—	1.5	5	—	1.5	5	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$		—	7	15	—	9	20	%
Analog Voltage Range	V_A	(Note 6)		+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	V
Source Current (Switch "OFF")	I_S (OFF)	$V_S = 10V$, $V_D = -10V$ (Note 1)		—	0.01	1	—	0.01	2	nA
Drain Current (Switch "OFF")	I_D (OFF)	$V_S = 10V$, $V_D = -10V$ (Note 1)	MUX-16 MUX-28	— —	0.2 0.1	1 1	— —	0.2 0.1	2 2	nA
Leakage Current (Switch "ON")	I_D (ON) $+I_S$ (ON)	$V_D = 10V$ (Note 1)	MUX-16 MUX-28	— —	0.2 0.1	1 1	— —	0.2 0.1	2 2	nA
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	1	10	—	1	10	μA

ELECTRICAL CHARACTERISTICS at V_S = ±15V and T_A = +25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS		MUX-16A/E MUX-28A/E MIN	TYP	MAX	MUX-16B/F MUX-28B/F MIN	TYP	MAX	UNITS
Digital "0" Enable Current	I_{INL} (EN)	V_{EN} = 0.4V		–	4	10	–	4	10	µA
Digital Input Capacitance	C_{DIG}			–	3	–	–	3	–	pF
Switching Time (t_{TRAN})	t_{PHL} t_{PLH}	(Notes 2,5) Figure 1 (Test Circuits)		– –	1.4 1.2	2.0 1.8	– –	1.8 1.6	2.5 2.2	µs
Output Settling Time	t_s	10V Step to 0.10% 10V Step to 0.05% 10V Step to 0.02%		– – –	2.6 3.2 4.0	– – –	– – –	2.7 3.4 7.2	– – –	µs
Break-Before-Make Delay	t_{OPEN}	Figure 3		–	0.7	–	–	1	–	µs
Enable Delay "ON"	$t_{ON (EN)}$	(Note 5) Figure 2 (Test Circuits)		–	1	2	–	1.2	2.5	µs
Enable Delay "OFF"	$t_{OFF (EN)}$	(Note 5) Figure 2 (Test Circuits)	MUX-16 MUX-28	– –	0.25 0.25	0.5 0.5	– –	0.25 0.25	0.5 0.6	µs
"OFF" Isolation	ISO_{OFF}	(Note 4) Figure 4 (Test Circuits)		–	66	–	–	66	–	dB
Crosstalk	CT	(Note 3) Figure 5 (Test Circuits)		–	75	–	–	75	–	dB
Source Capacitance	$C_{S (OFF)}$	Switch "OFF," V_S = 0V, V_D = 0V		–	2.5	–	–	2.5	–	pF
Drain Capacitance	$C_{D (OFF)}$	Switch "OFF," V_S = 0V, V_D = 0V	MUX-16 MUX-28	– –	13 8	– –	– –	13 8	– –	pF
Input to Output Capacitance	$C_{DS (OFF)}$	(Note 4)		–	0.15	–	–	0.15	–	pF
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I+	V+ = 15V V+ = 5V	MUX-16 MUX-28 MUX-16 MUX-28	– – – –	15 15 12 12	19 19 – –	– – – –	9 8 8 7	19 19 – –	mA
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I–	V– = –15V V– = –5V	MUX-16 MUX-28 MUX-16 MUX-28	– – – –	5 5 4 4	7 7 – –	– – – –	3.5 3 3 2.5	7 7 – –	mA

NOTES:
1. Conditions applied to leakage tests insure worst case leakages.
2. R_L = 10MΩ, C_L = 10pF.
3. Crosstalk is measured by driving channel 8 (8B*) with channel 7 (7B*) ON. R_L = 1MΩ, C_L = 10pF, V_S = 5V RMS, f = 500kHz.
4. "OFF" isolation is measured by driving channel 8 (8B) with ALL channels OFF. R_L = 1kΩ, C_L = 10pF, V_S = 5V RMS, f = 500kHz. C_{DS} is computed from the OFF isolation measurement.
5. Sample tested.
6. Guaranteed by leakage current and R_{ON} tests.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A ≤ +125°C for MUX-16AT/BT/BTC and MUX-28AT/BT/BTC; –25°C ≤ T_A ≤ +85°C for MUX-16ET and MUX-28ET; –40°C ≤ T_A ≤ +85°C for MUX-16 FT/FP/FPC and MUX-28FT/FP/FPC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16A/E MUX-28A/E MIN	TYP	MAX	MUX-16B/F MUX-28B/F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	V_S ≤ 10, I_S ≤ 200µA	–	–	500	–	–	800	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	–10V ≤ V_S ≤ 10V, I_S = 200µA	–	2	–	–	5.5	–	%
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 200µA	–	10	–	–	15	–	%
Analog Voltage Range	V_A	(Note 6)	+10 –10	+11 –15	– –	+10 –10	+11 –15	– –	V
Source Current (Switch"OFF")	$I_{S (OFF)}$	V_S = 10V, V_D = –10V (Note 1)	–	–	25	–	–	50	nA
Drain Current (Switch "OFF")	$I_{D (OFF)}$	V_S = 10V, V_D = –10V (Note 1)	–	–	75	–	–	250	nA
Leakage Current (Switch "ON")	$I_{D (ON)}$ $+I_{S (ON)}$	V_D = 10V (Note 1)	–	–	75	–	–	250	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	2	–	–	2	–	–	V
Digital "0" Input Voltage	V_{INL}	(Note 6)	–	–	0.7	–	–	0.7	V
Digital Input Current	I_{IN}	V_{IN} = 0.4V to 15V	–	–	20	–	–	20	µA
Digital "0" Enable Current	I_{INL} (EN)	V_{EN} = 0.4V	–	–	20	–	–	20	µA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"	–	–	24	–	–	24	mA
Negative Supply Current	I–	All Digital Inputs Logic "0" or "1"	–	–	8.2	–	–	8.2	mA

Quad SPST JFET Analog Switch

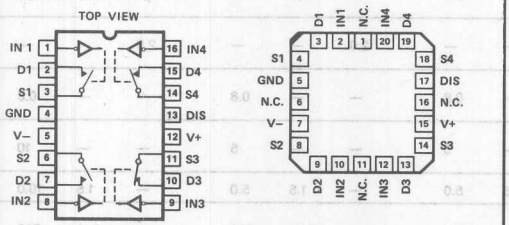
SW06

FEATURES

- **Two Normally Open and Two Normally Closed SPST Switches with Disable**
- **Switches can be Easily Configured as a Dual SPDT or a DPDT**
- **Highly Resistant to Static Discharge Destruction**
- **Higher Resistance to Radiation Than Analog Switches Designed with MOS Devices**
- **Guaranteed R_{ON} Matching ..... 10% Max**
- **Guaranteed Switching Speeds ..... T_{ON} = 500ns Max**
  T_{OFF} = 400ns Max
- **Guaranteed Break-Before-Make Switching**
- **Low "ON" Resistance ..... 80Ω Max**
- **Low R_{ON} Variation from Analog Input Voltage 5%**
- **Low Total Harmonic Distortion 0.01%**
- **Low Leakage Currents at High Temperature:**
  T_A = 125° C ..... 100nA Max
  T_A = 85° C ..... 30nA Max
- **Digital Inputs TTL/CMOS Compatible and Independent of V+**
- **Improved Specifications and Pin Compatible to LF-11333/13333**
- **Dual or Single Power Supply Operation**
- **Available in Die Form**

PIN CONNECTIONS

Switches are shown in the logic "0" input state and DIS = "1"



16-PIN DIP
(Q or P-Suffix)
16-PIN SOL
(S-Suffix)

SW-06BRC/883
LCC PACKAGE
(RC-Suffix)

TRUTH TABLE

DISABLE INPUT	LOGIC INPUT	SWITCH STATE CHANNELS 1 & 2	SWITCH STATE CHANNELS 3 & 4
0	X	OFF	OFF
1 or NC	0	OFF	ON
1 or NC	1	ON	OFF

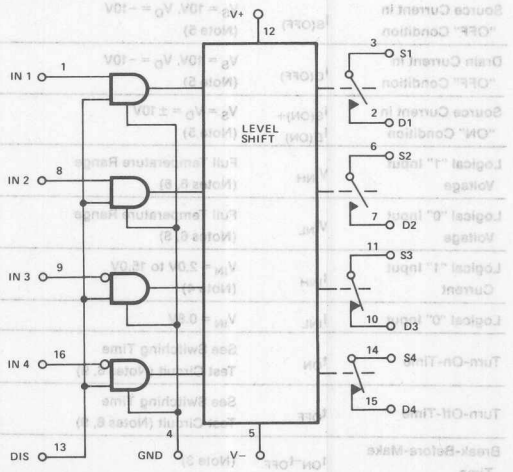
GENERAL DESCRIPTION

The SW-06 is a four channel single-pole, single-throw analog switch that employs both bipolar and ion-implanted FET devices. The SW-06 FET switches use bipolar digital logic inputs which are more resistant to static electricity than CMOS devices. Ruggedness and reliability are inherent in the SW-06 design and construction technology.

Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal R_{ON} variation over a 20V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With V+ = 36V, V– = 0V, the analog signal range will extend from ground to +32V.

PNP logic inputs are TTL and CMOS compatible to allow the SW-06 to upgrade existing designs. The logic "0" and logic "1" input currents are at micro-ampere levels reducing loading on CMOS and TTL logic.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION †

PLASTIC 16-PIN	CERDIP 16-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
–	SW06BQ*	SW06BRC/883	MIL
SW06GP	SW06FQ	–	XIND
SW06GS	–	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Operating Temperature Range
- SW-06BQ, BRC ..... –55°C to +125°C
- SW-06FQ ..... –40°C to +85°C
- SW-06GP, GS ..... –40°C to +85°C

Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply To V– Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage ..... (–4V or V–) to V+ Supply
Analog Input Voltage Range
- Continuous ..... V– Supply to V+ Supply +20V

Any Pin Including Switch 30mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	98	38	°C/W
16-Pin SOL (S)	98	30	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V and T_A = 25°C, unless otherwise noted.

			SW-06B			SW-06F			SW-06G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 1mA V_S = ±10V, I_S = 1mA	—	60 65	80 80	—	60 65	100 100	—	100 100	150 150	Ω
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 100μA (Note 1)	—	5	10	—	5	20	—	—	20	%
Analog Voltage Range	V_A	I_S = 1mA I_S = 1mA (Note 8)	+10 –10	+11 –15	—	+10 –10	+11 –15	—	+10 –10	+11 –15	—	V
Analog Current Range	I_A	V_S = ±10V	10	15	—	7	12	—	5	10	—	mA
ΔR_{ON} vs Applied Voltage	ΔR_{ON}	–10V ≤ V_S ≤ 10V, I_S = 1.0mA	—	5	15	—	10	20	—	10	20	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = –10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = –10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Source Current in "ON" Condition	$I_{S(ON)+}$ $I_{D(ON)}$	V_S = V_D = ±10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Logical "1" Input Voltage	V_{INH}	Full Temperature Range (Notes 6, 8)	2.0	—	—	2.0	—	—	2.0	—	—	V
Logical "0" Input Voltage	V_{INL}	Full Temperature Range (Notes 6, 8)	—	—	0.8	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I_{INH}	V_{IN} = 2.0V to 15.0V (Note 4)	—	—	5	—	—	5	—	—	10	μA
Logical "0" Input	I_{INL}	V_{IN} = 0.8V	—	1.5	5.0	—	1.5	5.0	—	1.5	10.0	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit (Notes 6, 9)	—	340	500	—	340	600	—	340	700	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit (Notes 6, 9)	—	200	400	—	200	400	—	200	500	ns
Break-Before-Make Time	t_{ON}–t_{OFF}	(Note 3)	50	140	—	50	140	—	50	140	—	ns
Source Capacitance	$C_{S(OFF)}$	V_S = 0V (Note 5)	—	7.0	—	—	7.0	—	—	7.0	—	pF
Drain Capacitance	$C_{D(OFF)}$	V_S = 0V (Note 5)	—	5.5	—	—	5.5	—	—	5.5	—	pF
Channel "ON" Capacitance	$C_{D(ON)+}$ $C_{S(ON)}$	V_S = V_D = 0V (Note 5)	—	15	—	—	15	—	—	15	—	pF
"OFF" Isolation	$I_{SO(OFF)}$	V_S = $5V_{RMS}$, R_L = 680Ω, C_L = 7pF, f = 500kHz (Note 5)	—	58	—	—	58	—	—	58	—	dB
Crosstalk	C_T	V_S = $5V_{RMS}$, R_L = 680Ω, C_L = 7pF, f = 500kHz (Note 5)	—	70	—	—	70	—	—	70	—	dB

ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V and T_A = 25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SW-06B MIN	SW-06B TYP	SW-06B MAX	SW-06F MIN	SW-06F TYP	SW-06F MAX	SW-06G MIN	SW-06G TYP	SW-06G MAX	UNITS
Positive Supply Current	I+	All Channels "OFF", DIS = "0" (Note 5)	–	5.0	6.0		5.0	9.0	–	6.0	9.0	mA
Negative Supply Current	I–	All Channels "OFF", DIS = "0" (Note 5)	–	3.0	5.0	–	4.0	7.0	–	4.0	7.0	mA
Ground Current	I_G	All Channels "ON" or "OFF" (Note 5)	–	3.0	4.0	–	3.0	4.0	–	3.0	5.0	mA

ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V, –55°C ≤ T_A ≤ +125°C for SW-06BQ, –40°C ≤ T_A ≤ +85°C for SW-06FQ and –40°C ≤ T_A ≤ +85°C for SW-06GP/GS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06B MIN	SW-06B TYP	SW-06B MAX	SW-06F MIN	SW-06F TYP	SW-06F MAX	SW-06G MIN	SW-06G TYP	SW-06G MAX	UNITS
Temperature Range	T_A	Operating	–55	—	125	–25	—	85	0	—	70	°C
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 1.0mA V_S = ±10V, I_S = 1.0mA	— —	75 80	110 110	— —	75 80	125 125	— —	75 80	175 175	Ω
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 100μA (Note 1)	—	6	20	—	6	25	—	10	—	%
Analog Voltage Range	V_A	I_S = 1.0mA (Note 8) I_S = 1.0mA	+10 –10	+11 –15	— —	+10 –10	+11 –15	— —	+10 –10	+11 –15	— —	V
Analog Current Range	I_A	V_S = ±10.0V	7	12	—	5	11	—	—	11	—	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	–10V ≤ V_S ≤ +10V, I_S = 1.0mA	—	10	—	—	12	—	—	15	—	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = –10V, T_A = Max. Operating Temp. (Notes 5, 7)	—	—	60	—	—	30	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = –10V, T_A = Max. Operating Temp. (Notes 5, 7)	—	—	60	—	—	30	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)}$+ $I_{D(ON)}$	V_S = V_D = ±10V, T_A = Max. Operating Temp. (Notes 5, 7)	—	—	100	—	—	30	—	—	60	nA
Logical "1" Input Current	I_{INH}	V_{IN} = 2.0V to 15.0V (Note 4)	—	—	10	—	—	10	—	—	15	μA
Logical "0" Input Current	I_{INL}	V_{IN} = 0.8V	—	4	10	—	4	10	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit (Notes 2, 6)	—	440	900	—	500	900	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit (Notes 2, 6)	—	300	500	—	330	500	—	—	500	ns
Break-Before-Make Time	t_{ON}–t_{OFF}	(Note 3)	—	70	—	—	70	—	—	50	—	ns
Positive Supply Current	I+	All Channels "OFF" DIS = "0" (Note 5)	—	—	9.0	—	—	13.5	—	—	13.5	mA
Negative Supply Current	I–	All Channels "OFF" DIS = "0" (Note 5)	—	—	7.5	—	—	10.5	—	—	10.5	mA
Ground Current	I_G	All Channels "ON" or "OFF" (Note 5)	—	—	6.0	—	—	7.5	—	—	7.5	mA

NOTES:

1. V_S = 0V, I_S = 100μA. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

2. Guaranteed by design.
3. Switch is guaranteed by design to provide break-before-make operation.
4. Current tested at V_{IN} = 2.0V. This is worst case condition.
5. Switch being tested ON or OFF as indicated, V_{INH} = 2.0V or V_{INL} = 0.8V, per logic truth table.
6. Also applies to disable pin.
7. Parameter tested only at T_A = +125°C for military grade device.
8. Guaranteed by R_{ON} and leakage tests. For normal operation maximum analog signal voltages should be restricted to less than (V+) –4V.
9. Sample tested.

ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V and T_A = 25°C, unless otherwise noted. Continued

PARAMETER	SYMBOL	CONDITIONS	SW-08B			SW-08F			SW-08G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Positive Supply Current	I_+	All Channels "OFF", DIS = "0" (Note 5)	–	5.0	6.0		5.0	6.0	–	6.0	8.0	mA
Negative Supply Current	I_-	All Channels "OFF", DIS = "0" (Note 5)	–	3.0	5.0	–	4.0	7.0	–	4.0	7.0	mA
Ground Current	I_G	All Channels "ON" or "OFF" (Note 5)	–	3.0	4.0	–	3.0	4.0	–	3.0	5.0	mA

ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V, –55°C ≤ T_A ≤ +125°C for SW-08BD, –40°C ≤ T_A ≤ +85°C for SW-08FD and –40°C ≤ T_A ≤ +85°C for SW-08GP/GS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-08B			SW-08F			SW-08G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Temperature Range	T_A	Operating	–55	—	125	–25	—	85	0	—	70	°C
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 1.0mA	—	75	110	—	75	125	—	75	175	Ω
		V_S = ± 10V, I_S = 1.0mA	—	80	110	—	80	125	—	80	175	
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 100µA (Note 1)	—	6	20	—	6	25	—	10	—	%
Analog Voltage Range	V_A	I_S = 1.0mA (Note 8)	+ 10	+ 11	—	+ 10	+ 11	—	+ 10	+ 11	—	V
		I_S = 1.0mA	–10	–15	—	–10	–15	—	–10	–15	—	
Analog Current Range	I_A	V_S = ± 10.0V	7	12	—	5	11	—	—	11	—	mA
ΔR_{ON} With Applied voltage	ΔR_{ON}	–10V ≤ V_S ≤ + 10V, I_S = 1.0mA	—	10	—	—	12	—	—	15	—	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = – 10V, T_A = Max. Operating Temp. (Notes 6, 7)	—	—	60	—	—	20	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = – 10V, T_A = Max. Operating Temp. (Notes 6, 7)	—	—	60	—	—	20	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)+}$ $I_{D(ON)}$	V_S = V_D = ± 10V, T_A = Max. Operating Temp. (Notes 6, 7)	—	—	100	—	—	30	—	—	60	nA
Logical "1" Input Current	I_{INH}	V_{IH} = 2.0V to 15.0V (Note 4)	—	—	10	—	—	10	—	—	15	µA
Logical "0" Input Current	I_{INL}	V_{IL} = 0.8V	—	<	10	—	4	10	—	8	15	µA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit (Notes 2, 6)	—	440	800	—	500	900	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit (Notes 2, 6)	—	300	500	—	350	500	—	—	500	ns
Break-Before-Make Time	t_{ON}–t_{OFF}	(Note 3)	—	70	—	—	70	—	—	80	—	ns
Positive Supply Current	I_+	All Channels "OFF" DIS = "0" (Note 5)	—	—	9.0	—	—	10.5	—	—	10.5	mA
Negative Supply Current	I_-	All Channels "OFF" DIS = "0" (Note 5)	—	—	7.5	—	—	10.5	—	—	10.5	mA
Ground Current	I_G	All Channels "ON" or "OFF" (Note 5)	—	—	8.0	—	—	7.5	—	—	7.5	mA

NOTES:

1. V_S = 0V, I_S = 100µA. Specified as a percentage of $R_{AVERAGE}$ where:
$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$
2. Guaranteed by design.
3. Switch is guaranteed by design to provide break-before-make operation.
4. Current tested at V_{IH} = 2.0V. This is worst case condition.
5. Switch being tested ON or OFF as indicated, V_{INH} = 2.0V or V_{INL} = 0.8V, per logic truth table.
6. Also applies to disable pin.
7. Parameter tested only at T_A = + 125°C for military grade device.
8. Guaranteed by R_{ON} and leakage tests. For normal operation maximum analog signal voltage should be restricted to less than (V+) –4V.
9. Sample tested.

Voltage References and Regulators
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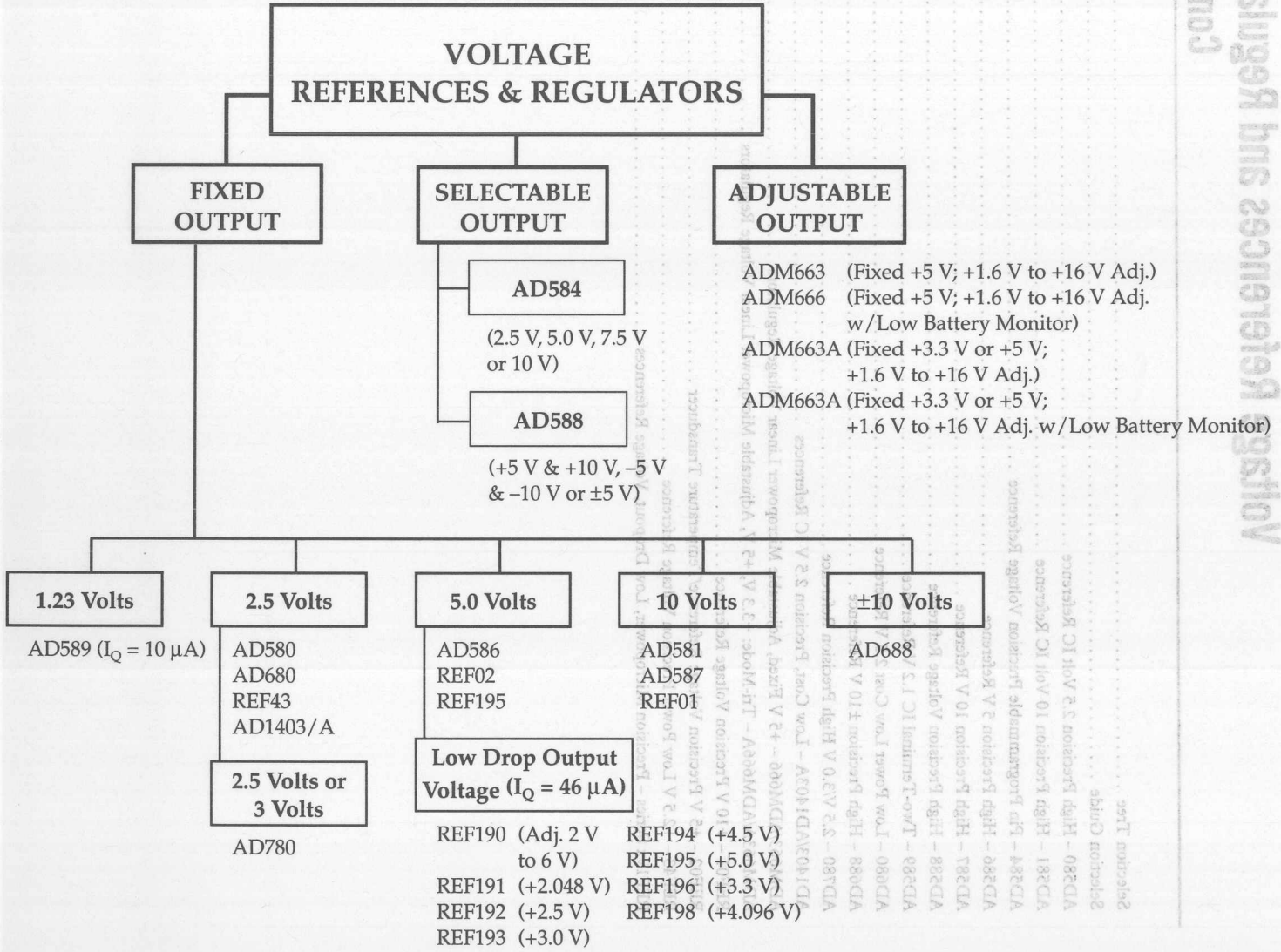
Selection Tree — Voltage References and Regulators



Selection Guides—Voltage References and Regulators

Voltage References

Model	Output Voltage V	Initial Accuracy % FS max	Temp Stability ppm/°C max	Package Options[1]	Temp Ranges[2]	Page[3]	Comments
AD589	**+1.235**	**1.2–2.8**	**10–100**	**H**	**C, M/**	**8–22**	**Two Terminal, 1.2 V Reference**
REF191	**+2.048**	**2–10 mV**	**5–25**	**N, R**	**I**	**8–61**	**45 µA Supply Current, 0.6 V Dropout @ 10 mA Out**
REF192	**+2.5**	**2–10 mV**	**5–25**	**N, R**	**I**	**8–61**	**45 µA Supply Current, 0.6 V Dropout @ 10 mA Out**
AD780	**+2.5/+3.0**	**0.03–0.04**	**3**	**N, Q, R**	**I, M**	**8–30**	**Ultrahigh Precision +2.5 V/+3.0 V Bandgap Reference**
AD680	**+2.5**	**0.2–0.4**	**20–30**	**N, R, T**	**C, I**	**8–24**	**Low Cost, Low Power 2.5 V Reference**
AD580	**+2.5**	**0.4–3**	**10–85**	**H**	**C, M/$_D$**	**8–5**	**Precision, Three Terminal, 2.5 V Reference**
AD1403/AD1403A	**+2.5**	**0.4–1**	**25–40**	**N**	**I**	**8–38**	**Second Source, 2.5 V Reference**
REF43	**+2.5**	**0.6–1**	**10–25**	**H, N, Q, R**	**I, M/$_D$**	**8–58**	**Precision Bandgap Reference**
REF03	+2.5	0.6	50	N, R	I	CII 6–99	Low Cost Bandgap Reference
REF193	**+3.0**	**10 mV**	**25**	**N, R**	**I**	**8–61**	**45 µA Supply Current, 0.6 V Dropout @ 10 mA Out**
REF196	**+3.3**	**10 mV**	**25**	**N, R**	**I**	**8–61**	**45 µA Supply Current, 0.6 V Dropout @ 10 mA Out**
REF198	**+4.096**	**2–10 mV**	**5–25**	**N, R**	**I**	**8–61**	**45 µA Supply Current, 0.6 V Dropout @ 10 mA Out**
REF194	**+4.5**	**2–10 mV**	**5–25**	**N, R**	**I**	**8–61**	**45 µA Supply Current, 0.6 V Dropout @ 10 mA Out**
AD586	**+5**	**0.04–0.4**	**5–25**	**Q, R**	**C, M/$_D$**	**8–13**	**Precision, Buried Zener 5 V Reference**
REF195	**+5.0**	**2–10 mV**	**5–25**	**N, R**	**I**	**8–61**	**45 µA Supply Current, 0.6 V Dropout @ 10 mA Out**
REF02	**+5**	**0.3–2.0**	**8.5–250**	**E, H, N, Q, R**	**C, I, M/$_D$**	**8–55**	**Precision Bandgap Reference, Adjustable**
AD2710	+10	0.01	1–5	N	C	CII 6–79	Ultrahigh Precision 10 V Reference
AD2700	+10	0.025–0.05	3–10	D	C, M/$_D$	CII 6–75	Very High Precision 10 V Reference
AD587	**+10**	**0.05–0.1**	**5–20**	**Q, R**	**C, M/$_D$**	**8–16**	**Precision 10 V Buried Zener Reference**
AD581	**+10**	**0.05–0.3**	**5–30**	**H**	**C, M/$_D$**	**8–7**	**Three Terminal 10 V Bandgap Reference**
REF01	**+10**	**0.3–1.0**	**8.5–65**	**E, H, N, Q, R**	**C, I, M/$_D$**	**8–52**	**Precision Bandgap Reference**
AD2712	±10	0.01	1–5	N	C	CII 6–79	Ultrahigh Precision ±10 V Reference
AD688	**±10**	**0.02–0.05**	**1.5–6**	**Q**	**I, M/**	**8–27**	**High Precision Monolithic ±10 V Reference**
AD2702	±10	0.025–0.05	3–10	D	C, M/$_D$	CII 6–75	Very High Precision ±10 V Reference
AD2701	−10	0.025–0.05	3–10	D	C, M/$_D$	CII 6–75	Very High Precision −10 V Reference
AD588	**Selectable**	**0.01**	**1.5–6**	**E, N, Q**	**C, I, M/$_D$**	**8–19**	**Ultrahigh Precision, Monolithic Programmable Reference**
AD584	**Selectable**	**0.05–0.3**	**5–30**	**E, H**	**C, M/$_D$**	**8–9**	**Precision, Programmable Bandgap Reference**
REF190	**Adjustable**	**10 mV**	**5–25**	**N, R**	**I**	**8–61**	**45 µA Supply Current, 0.6 V Dropout @ 10 mA Out**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]CII = *Data Converter Reference Manual, Volume II*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Selection Guides—Voltage References and Regulators

Voltage Regulators

Model	Output Voltage	Output Current	Functions	Package Options[1]	Temp Ranges[2]	Page	Comments
ADM663	**+5 V Fixed, 1.3 to +16 V Adjustable**	**40**	**Output Boost Temperature Output Shutdown**	**N, R**	**I**	**8–40**	**MAX663 Replacement**
ADM666	**+5 V Fixed, 1.3 to +16 V Adjustable**	**40**	**Low Battery Detect Shutdown**	**N, R**	**I**	**8–40**	**MAX666 Replacement**
ADM663A	**+3.3 V or +5 V Fixed, 1.3 to +16 V Adjustable**	**100**	**Output Boost Temperature Output Shutdown**	**N, R, RS**	**I**	**8–46**	**Higher Output Replacement**
ADM666A	**+3.3 V or 5 V Fixed, 1.3 to +16 V Adjustable**	**100**	**Low Battery Detect Shutdown**	**N, R, RS**	**I**	**8–46**	**Higher Output Replacement**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
Boldface Type: Data sheet information in this volume.

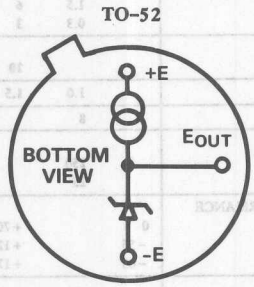
High Precision 2.5V IC Reference

AD580*

FEATURES

Laser Trimmed to High Accuracy: 2.500V ±0.4%
3-Terminal Device: Voltage In/Voltage Out
Excellent Temperature Stability: 10ppm/°C (AD580M, U)
Excellent Long Term Stability: 250μV (25μV/Month)
Low Quiescent Current: 1.5mA max
Small, Hermetic IC Package: TO-52 Can
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM[1]



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PRODUCT DESCRIPTION

The AD580 is a three-terminal, low cost, temperature compensated, bandgap voltage reference which provides a fixed 2.5V output for inputs between 4.5V and 30V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provide the AD580 with an initial tolerance of ±0.4%, a temperature stability of better than 10ppm/°C and long-term stability of better than 250μV. In addition, the low quiescent current drain of 1.5mA max offers a clear advantage over classical zener techniques.

The AD580 is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD580 allows operation with 5 volt logic supplies making the AD580 ideal for digital panel meter applications or whenever only a single logic power supply is available.

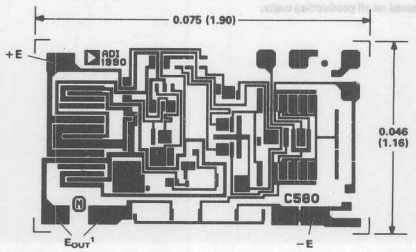
The AD580J, K, L and M are specified for operation over the 0 to +70°C temperature range; the AD580S, T and U are specified for operation over the extended temperature range of −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Laser-trimming of the thin-film resistors minimizes the AD580 output error. For example, the AD580L output tolerance is ±10mV.
2. The three-terminal voltage in/voltage out operation of the AD580 provides regulated output voltage without any external components.
3. The AD580 provides a stable 2.5V output voltage for input voltages between 4.5V and 30V. The capability to provide a stable output voltage using a 5-volt input makes the AD580 an ideal choice for systems that contain a single logic power supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD580 with temperature stabilities to 10ppm/°C and long term stability better than 250μV.
5. The low quiescent current drain of the AD580 makes it ideal for CMOS and other low power applications.
6. The AD580 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD580/883B data sheet for detailed specifications.

AD580 CHIP DIMENSIONS AND PAD LAYOUT

Dimensions shown in inches and (mm).



NOTE
[1]BOTH E_{OUT} PADS MUST BE CONNECTED TO THE OUTPUT.

The AD580 is also available in chip form. Consult the factory for specifications and applications information.

*Protected by Patent Nos. 3,887,863; RE30, 586.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

REV. A

AD580 SPECIFICATIONS

(Error from Nominal 2.500 Volt Output)			±25			±25			±10			±10	mV
OUTPUT VOLTAGE CHANGE													
T_{min} to T_{max}			15			7			4.3			1.75	mV
			85			40			25			10	ppm/°C
LINE REGULATION													
$7V \le V_{IN} \le 30V$		1.5	6		1.5	4			2			2	mV
$4.5V \le V_{IN} \le 7V$		0.3	3		0.3	2			1			1	mV
LOAD REGULATION													
ΔI = 10mA			10			10			10			10	mV
QUIESCENT CURRENT		1.0	1.5		1.0	1.5		1.0	1.5		1.0	1.5	mA
NOISE (0.1Hz to 10Hz)		8			8			8			8		µV (p-p)
STABILITY													
Long Term		250			250			250			250		µV
Per Month		25			25			25			25		µV
TEMPERATURE PERFORMANCE													
Specified	0		+70	0		+70	0		+70	0		+70	°C
Operating	−55		+125	−55		+125	−55		+125	−55		+125	°C
Storage	−65		+175	−65		+175	−65		+175	−65		+175	°C
PACKAGE OPTION *													
TO-52 (H-03A)		AD580JH			AD580KH			AD580LH			AD580MH		

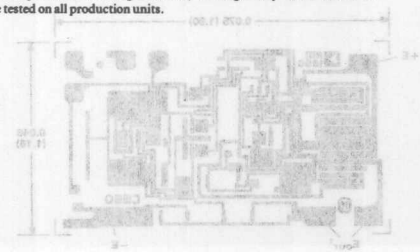
Model	AD580S			AD580T			AD580U			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE										
(Error from Nominal 2.500 Volt Output)			±25			±10			±10	mV
OUTPUT VOLTAGE CHANGE										
T_{min} to T_{max}			25			11			4.5	mV
			55			25			10	ppm/°C
LINE REGULATION										
$7V \le V_{IN} \le 30V$		1.5	6			2			2	mV
$4.5V \le V_{IN} \le 7V$		0.3	3			1			1	mV
LOAD REGULATION										
ΔI = 10mA			10			10			10	mV
QUIESCENT CURRENT		1.0	1.5		1.0	1.5		1.0	1.5	mA
NOISE (0.1Hz to 10Hz)		8			8			8		µV (p-p)
STABILITY										
Long Term		250			250			250		µV
Per Month		25			25			25		µV
TEMPERATURE PERFORMANCE										
Specified	−55		+125	−55		+125	−55		+125	°C
Operating	−55		+150	−55		+150	−55		+150	°C
Storage	−65		+175	−65		+175	−65		+175	°C
PACKAGE OPTION *										
TO-52 (H-03A)		AD580SH			AD580TH			AD580UH		

NOTE

*** H = Metal Can. For outline information see Package Information section.**

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Power Dissipation @ +25°C
  Ambient Temperature 350mW
Derate above +25°C . . . . . 2.8mW/°C
Lead Temperature (Soldering, 10sec) . . . . . 300°C
Thermal Resistance
  Junction-to-Case . . . . . 100°C/W
  Junction-to-Ambient . . . . . 360°C/W

ANALOG DEVICES

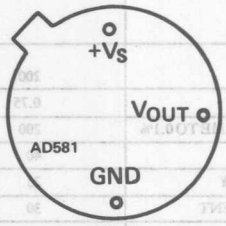
High Precision 10V IC Reference

AD581*

FEATURES

- **Laser-Trimmed to High Accuracy:**
  - **10.000 Volts ±5mV (L and U)**
- **Trimmed Temperature Coefficient:**
  - **5ppm/°C max, 0 to +70°C (L)**
  - **10ppm/°C max, −55°C to +125°C (U)**
- **Excellent Long-Term Stability:**
  - **25ppm/1000 hrs. (Noncumulative)**
- **Negative 10 Volt Reference Capability**
- **Low Quiescent Current: 1.0mA max**
- **10mA Current Output Capability**
- **3-Terminal TO-5 Package**
- **MIL-STD-883 Compliant Versions Available**

FUNCTIONAL BLOCK DIAGRAM



TO-5

BOTTOM VIEW

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PRODUCT DESCRIPTION

The AD581 is a three-terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 30 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/°C guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical Zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically 750μA. The long-term stability of the band-gap design is equivalent or superior to selected Zener reference diodes.

The AD581 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to +70°C; the AD581S, T, and U are specified for the −55°C to +125°C range. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.

***Covered by Patent Nos. 3,887,863; RE 30,586**

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C, while the AD581U guarantees ±15mV maximum total error without external trims from −55°C to +125°C.
2. Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
3. The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
4. Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 13 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.
5. The AD581 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD581/883B data sheet for detailed specifications.

AD581—SPECIFICATIONS (@ V_{IN} = +15V and 25°C)

Model	AD581J Min	AD581J Typ	AD581J Max	AD581K Min	AD581K Typ	AD581K Max	AD581L Min	AD581L Typ	AD581L Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			±30			±10			±5	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C			±13.5			±6.75			±2.25	mV
Value, T_{min} to T_{max} (Temperature Coefficient)			30			15			5	ppm/°C
LINE REGULATION										
15V≤V_{IN}≤30V			3.0			3.0			3.0	mV
			(0.002)			(0.002)			(0.002)	%/V
13V≤V_{IN}≤15V			1.0			1.0			1.0	mV
			(0.005)			(0.005)			(0.005)	%/V
LOAD REGULATION										
0≤I_{OUT}≤5mA		200	500		200	500		200	500	µV/mA
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.0	mA
TURN-ON SETTLING TIME TO 0.1%		200			200			200		µs
NOISE (0.1 to 10Hz)		40			40			40		µV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			µA
Sink −55°C to +85°C	–			–			–			mA
TEMPERATURE RANGE										
Specified	0		+70	0		+70	0		+70	°C
Operating	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[1]										
TO-5 (H-03B)		AD581JH			AD581KH			AD581LH		

Model	AD581S Min	AD581S Typ	AD581S Max	AD581T Min	AD581T Typ	AD581T Max	AD581U Min	AD581U Typ	AD581U Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			±30			±10			±5	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C			±30			±15			±10	mV
Value, T_{min} to T_{max} (Temperature Coefficient)			30			15			10	ppm/°C
LINE REGULATION										
15V≤V_{IN}≤30V			3.0			3.0			3.0	mV
			(0.002)			(0.002)			(0.002)	%/V
13V≤V_{IN}≤15V			1.0			1.0			1.0	mV
			(0.005)			(0.005)			(0.005)	%/V
LOAD REGULATION										
0≤I_{OUT}≤5mA		200	500		200	500		200	500	µV/mA
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.0	mA
TURN-ON SETTLING TIME TO 0.1%		200			200			200		µs
NOISE (0.1 to 10Hz)		40			40			40		µV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	200			200			200			µA
Sink −55°C to +85°C	5			5			5			mA
TEMPERATURE RANGE										
Specified	−55		+125	−55		+125	−55		+125	°C
Operating	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[1]										
TO-5 (H-03B)		AD581SH			AD581TH			AD581UH		

NOTES
[1]H = Hermetic Metal Can. For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Input Voltage V_{IN} to Ground 40V
Power Dissipation @ +25°C 600mW
Operating Junction Temperature Range . . −55°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Thermal Resistance
Junction-to-Ambient . . . . . 150°C/W

Pin Programmable Precision Voltage Reference

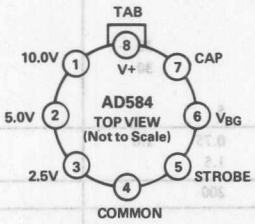
AD584*

FEATURES

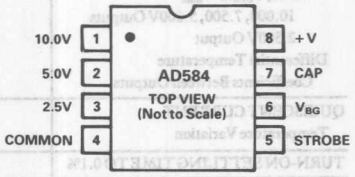
- Four Programmable Output Voltages: 10.000V, 7.500V, 5.000V, 2.500V
- Laser-Trimmed to High Accuracies
- No External Components Required
- Trimmed Temperature Coefficient: 5ppm/°C max, 0 to +70°C (AD584L) 15ppm/°C max, −55°C to +125°C (AD584T)
- Zero Output Strobe Terminal Provided
- Two Terminal Negative Reference Capability (5V & Above)
- Output Sources or Sinks Current
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability
- MIL-STD-883 Compliant Versions Available

PIN CONFIGURATIONS

8-Pin TO-99



8-Pin DIP



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PRODUCT DESCRIPTION

The AD584 is an eight-terminal precision voltage reference offering pin-programmable selection of four popular output voltages: 10.000V, 7.500V, 5.000V and 2.500V. Other output voltages, above, below or between the four standard outputs, are available by the addition of external resistors. Input voltage may vary between 4.5 and 30 volts.

Laser Wafer Trimming (LWT) is used to adjust the pin-programmable output levels and temperature coefficients, resulting in the most flexible high precision voltage reference available in monolithic form.

In addition to the programmable output voltages, the AD584 offers a unique strobe terminal which permits the device to be turned on or off. When the AD584 is used as a power supply reference, the supply can be switched off with a single, low-power signal. In the "off" state the current drain by the AD584 is reduced to about 100μA. In the "on" state the total supply current is typically 750μA including the output buffer amplifier.

The AD584 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters of up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD584J, K and L are specified for operation from 0 to +70°C; the AD584S and T are specified for the -55°C to +125°C range. All grades are packaged in a hermetically sealed eight-terminal TO-99 metal can; the AD584J and K are also available in an 8-pin plastic DIP.

***Protected by U.S. Patent No. 3,887,863; RE 30, 586**

PRODUCT HIGHLIGHTS

1. The flexibility of the AD584 eliminates the need to design-in and inventory several different voltage references. Furthermore one AD584 can serve as several references simultaneously when buffered properly.
2. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD584LH has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C.
3. The AD584 can be operated in a two-terminal "Zener" mode at 5 volts output and above. By connecting the input and the output, the AD584 can be used in this "Zener" configuration as a negative reference.
4. The output of the AD584 is configured to sink or source currents. This means that small reverse currents can be tolerated in circuits using the AD584 without damage to the reference and without disturbing the output voltage (10V, 7.5V and 5V outputs).
5. The AD584 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD584/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD584—SPECIFICATIONS (@ V_{IN} = 15V and 25°C)

Model	AD584J			AD584K			AD584L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE										
Maximum Error[1] for Nominal Outputs of:										
10.000V			±30			±10			±5	mV
7.500V			±20			±8			±4	mV
5.000V			±15			±6			±3	mV
2.500V			±7.5			±3.5			±2.5	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C Value, T_{min} to T_{max}[2]										
10.000, 7.500, 5.000V Outputs			30			15			5	ppm/°C
2.500V Output			30			15			10	ppm/°C
Differential Temperature Coefficients Between Outputs		5			3			3		ppm/°C
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.0	mA
Temperature Variation		1.5			1.5			1.5		µA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200			200		µs
NOISE (0.1 to 10Hz)		50			50			50		µV p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 Hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
LINE REGULATION (No Load)										
$15V \le V_{IN} \le 30V$		0.002				0.002			0.002	%/V
$(V_{OUT} + 2.5V) \le V_{IN} \le 15V$		0.005				0.005			0.005	%/V
LOAD REGULATION $0 \le I_{OUT} \le 5mA$, All Outputs		20	50		20	50		20	50	ppm/mA
OUTPUT CURRENT $V_{IN} \ge V_{OUT} + 2.5V$										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			mA
TEMPERATURE RANGE										
Operating	0		+70	0		+70	0		+70	°C
Storage	−65		+175	−65		+175	−65		+175	°C
PACKAGE OPTION[3]										
TO-99 (H-08A)		AD584JH			AD584KH			AD584LH		
Plastic (N-8)		AD584JN			AD584KN					

NOTES
[1]At Pin 1.
[2]Calculated as average over the operating temperature range.
[3]H = Hermetic Metal Can; N = Plastic DIP. For package outline information see Package Information section.

Specifications subject to change without notice.

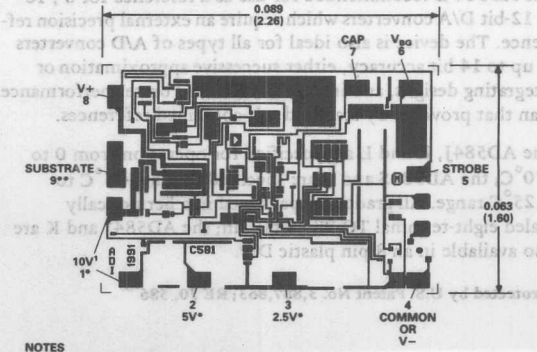
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAX RATINGS

Input Voltage V_{IN} to Ground 40V
Power Dissipation @ +25°C 600mW
Operating Junction Temperature Range . . −55°C to +125°C
Lead Temperature (Soldering 10sec) . . . . . +300°C
Thermal Resistance
Junction-to-Ambient (H-08A) . . . . . 150°C/W

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



NOTES
*BOTH 10V PADS MUST BE CONNECTED TO THE OUTPUT.
*INTERCONNECTIONS REQUIRED; SEE PIN DESIGNATIONS FOR INFORMATION.
**NOT BROUGHT OUT IN PACKAGE DEVICE.
PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99, 8-PIN METAL PACKAGE.

Model	AD584S			AD584T			Units
	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE							
Maximum Error[1] for Nominal Outputs of:							
10.000V			±30			±10	mV
7.500V			±20			±8	mV
5.000V			±15			±6	mV
2.500V			±7.5			±3.5	mV
OUTPUT VOLTAGE CHANGE							
Maximum Deviation from +25°C Value, T_{min} to T_{max}[2]							
10.000, 7.500, 5.000V Outputs			30			15	ppm/°C
2.500V Output			30			20	ppm/°C
Differential Temperature Coefficients Between Outputs		5			3		ppm/°C
QUIESCENT CURRENT		0.75	1.0		0.75	1.0	mA
Temperature Variation		1.5			1.5		µA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200		µs
NOISE (0.1 to 10Hz)		50			50		µV p-p
LONG-TERM STABILITY		25			25		ppm/1000 Hrs.
SHORT-CIRCUIT CURRENT		30			30		mA
LINE REGULATION (No Load)							
$15V \le V_{IN} \le 30V$			0.002			0.002	%/V
$(V_{OUT} + 2.5V) \le V_{IN} \le 15V$			0.005			0.005	%/V
LOAD REGULATION $0 \le I_{OUT} \le 5mA$, All Outputs		20	50		20	50	ppm/mA
OUTPUT CURRENT $V_{IN} \ge V_{OUT} + 2.5V$							
Source @ +25°C	10			10			mA
Source T_{min} to T_{max}	5			5			mA
Sink T_{min} to T_{max}	5			5			mA
TEMPERATURE RANGE							
Operating	−55		+125	−55		+125	°C
Storage	−65		+175	−65		+175	°C
PACKAGE OPTION[3]							
TO-99 (H-08A)		AD584SH			AD584TH		

NOTES
[1]At Pin 1.
[2]Calculated as average over the operating temperature range.
[3]H = Hermetic Metal Can. For package outline information see Package Information section.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

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pins 1 and 4 (see Figure 1). The stabilized output voltage may be reduced to 7.5V, 5.0V or 2.5V by connecting the programming pins as follows:

OUTPUT VOLTAGE	PIN PROGRAMMING
7.5V	Join the 2.5V and 5.0V pins (2) and (3).
5.0V	Connect the 5.0V pin (2) to the output pin (1).
2.5V	Connect the 2.5V pin (3) to the output pin (1).

The options shown above are available without the use of any additional components. Multiple outputs using only one AD584, are also possible by simply buffering each voltage programming pin with a unity-gain noninverting op amp.

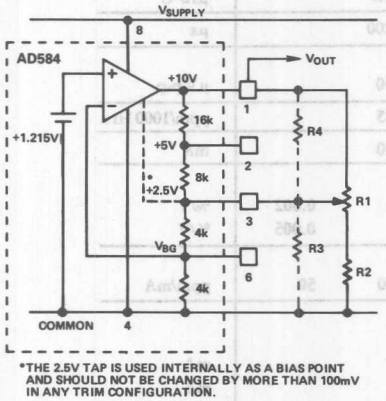


Figure 1. Variable Output Options

The AD584 can also be programmed over a wide range of output voltages, including voltages greater than 10V, by the addition of one or more external resistors. Figure 1 illustrates the general adjustment procedure, with approximate values given for the internal resistors of the AD584. The AD584 may be modeled as an op amp with a noninverting feedback connection, driven by a high stability 1.215 volt bandgap reference (see Figure 3 for schematic).

When the feedback ratio is adjusted with external resistors, the output amplifier can be made to multiply the reference voltage by almost any convenient amount, making popular outputs of 10.24V, 5.12V, 2.56V or 6.3V easy to obtain. The most general adjustment (which gives the greatest range and poorest resolution) uses R1 and R2 alone (see Figure 1). As R1 is adjusted to its upper limit the 2.5V pin 3 will be connected to the output, which will reduce to 2.5V. As R1 is adjusted to its lower limit, the output voltage will rise to a value limited by R2. For example, if R2 is about 6kΩ, the upper limit of the output range will be about 20V even for large values of R1. R2 should

quired to be set at levels other than the standard outputs, the 20% absolute tolerance in the internal resistor ladder must be accounted for.

Alternatively, the output voltage can be raised by loading the 2.5V tap with R3 alone. The output voltage can be lowered by connecting R4 alone. Either of these resistors can be a fixed resistor selected by test or an adjustable resistor. In all cases the resistors should have a low temperature coefficient to match the AD584 internal resistors, which have a negative T.C. less than 60ppm/°C. If both R3 and R4 are used, these resistors should have matched temperature coefficients.

When only small adjustments or trims are required, the circuit of Figure 2 offers better resolution over a limited trim range. The circuit can be programmed to 5.0V, 7.5V or 10V and adjusted by means of R1 over a range of about ±200mV. To trim the 2.5V output option, R2 (Figure 2) can be reconnected to the bandgap reference (pin 6). In this configuration, the adjustment should be limited to ±100mV in order to avoid affecting the performance of the AD584.

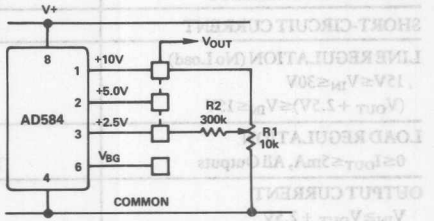


Figure 2. Output Trimming

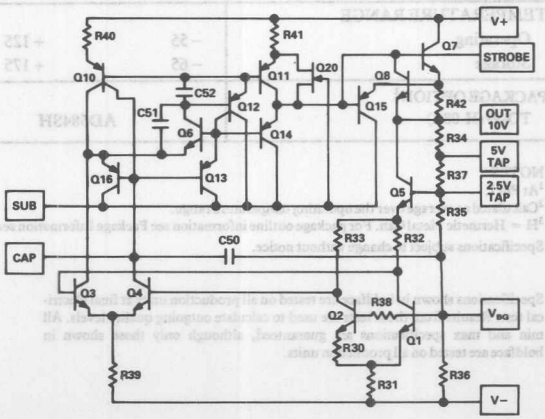


Figure 3. Schematic Diagram

ANALOG DEVICES

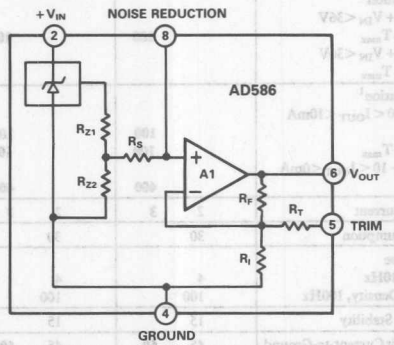
High Precision 5V Reference

AD586

FEATURES

Laser Trimmed to High Accuracy:
5.000V ±2.0mV (M Grade)
Trimmed Temperature Coefficient:
2ppm/°C max, 0 to +70°C (M Grade)
5ppm/°C max, −40°C to +85°C (B Grade)
10ppm/°C max, −55°C to +125°C (T Grade)
Low Noise, 100nV/√Hz
Noise Reduction Capability
Output Trim Capability
MIL-STD-883 Compliant Versions Available
Industrial Temperature Range SOICs Available
Output Capable of Sourcing or Sinking 10mA

FUNCTIONAL BLOCK DIAGRAM



NOTE: PINS 1, 3 & 7 ARE INTERNAL TEST POINTS.
MAKE NO CONNECTIONS TO THESE POINTS.

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PRODUCT DESCRIPTION

The AD586 represents a major advance in the state-of-the-art in monolithic voltage references. Using a proprietary ion-implanted buried Zener diode and laser wafer trimming of high stability thin-film resistors, the AD586 provides outstanding performance at low cost.

The AD586 offers much higher performance than most other 5V references. Because the AD586 uses an industry standard pinout, many systems can be upgraded instantly with the AD586. The buried Zener approach to reference design provides lower noise and drift than bandgap voltage references. The AD586 offers a noise reduction pin which can be used to further reduce the noise level generated by the buried Zener.

The AD586 is recommended for use as a reference for 8-, 10-, 12-, 14- or 16-bit D/A converters which require an external precision reference. The device is also ideal for successive approximation or integrating A/D converters with up to 14 bits of accuracy and, in general, can offer better performance than the standard on-chip references.

The AD586J, K, L and M are specified for operation from 0 to +70°C, the AD586A and B are specified for −40°C to +85°C operation, and the AD586S and T are specified for −55°C to +125°C operation. The AD586J, K, L and M are available in an 8-pin plastic DIP. The AD586J, K, L, A and B are available in an 8-pin plastic surface mount small outline (SO) package. The AD586J, K, L, S and T are available in an 8-pin cerdip package.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficients results in very low errors over temperature without the use of external components. The AD586M has a maximum deviation from 5.000V of ±2.45mV between 0 and +70°C, and the AD586T guarantees ±7.5mV maximum total error between −55°C and +125°C.
2. For applications requiring higher precision, an optional fine-trim connection is provided.
3. Any system using an industry standard pinout reference can be upgraded instantly with the AD586.
4. Output noise of the AD586 is very low, typically 4μV p-p. A noise reduction pin is provided for additional noise filtering using an external capacitor.
5. The AD586 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD586/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD586—SPECIFICATIONS (T_A = +25°C, V_{IN} = +15V unless otherwise noted)

Model	AD586J			AD586K/A			AD586L/B			AD586M			AD586S			AD586T			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage	4.980		5.020	4.995		5.005	4.9975		5.0025	4.998		5.002	4.990		5.010	4.9975		5.0025	V
Output Voltage Drift[1]																			
0 to +70°C			25			15			5			2							ppm/°C
−55°C to +125°C															20			10	
Gain Adjustment	+6			+6			+6			+6			+6			+6			%
	−2			−2			−2			−2			−2			−2			
Line Regulation[1]																			
10.8V < +V_{IN} <36V																			
T_{min} to T_{max}			100			100			100			100							±μV/V
11.4V < +V_{IN} <36V																			
T_{min} to T_{max}															150			150	
Load Regulation[1]																			
Sourcing 0 < I_{OUT} <10mA																			
25°C			100			100			100			100			150			150	μV/mA
T_{min} to T_{max}			100			100			100			100			150			150	
Sinking −10 < I_{OUT} <0mA																			
25°C			400			400			400			400			400			400	
Quiescent Current		2	3		2	3		2	3		2	3		2	3		2	3	mA
Power Consumption		30			30			30			30			30			30		mW
Output Noise																			
0.1Hz to 10Hz		4			4			4			4			4			4		μV p-p
Spectral Density, 100Hz		100			100			100			100			100			100		nV/√Hz
Long-Term Stability		15			15			15			15			15			15		ppm/1000Hr
Short-Circuit Current-to-Ground		45	60		45	60		45	60		45	60		45	60		45	60	mA
Temperature Range																			
Specified Performance[2]	0		+70	0		+70	0		+70	0		+70	−55		+125	−55		+125	°C
				−40		+85	−40		+85										
Operating Performance[3]	−40		+85	−40		+85	−40		+85	−40		+85	−55		+125	−55		+125	

NOTES

[1]Maximum output voltage drift is guaranteed for all packages and grades. Cerdip packaged parts are also 100% production tested.

[2]Lower row shows specified performance for A and B grades.

[3]The operating temperature ranged is defined as the temperatures extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

Specifications subject to change without notice.

Specifications in boldface are tested on all production units at final electrical test. Result from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units unless otherwise specified.

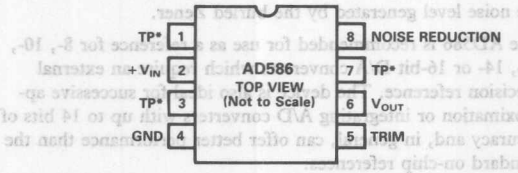
ABSOLUTE MAXIMUM RATINGS*

V_{IN} to Ground 36V
Power Dissipation (25°C) 500mW
Storage Temperature . . . . . −65°C to +150°C
Lead Temp (Soldering, 10sec) . . . . . 300°C
Package Thermal Resistance
θ_{JC} . . . . . 22°C/W
θ_{JA} . . . . . 110°C/W
Output Protection: Output safe for indefinite short to ground or V_{IN}.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM

(Top View)



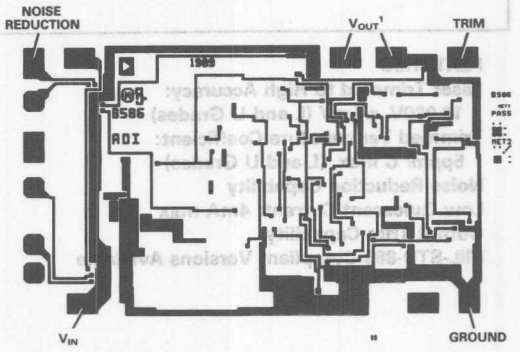
*TP DENOTES FACTORY TEST POINT. NO CONNECTIONS SHOULD BE MADE TO THESE PINS.

DIE SPECIFICATIONS

The following specifications are tested at the die level for AD586JCHIPS. These die are probed at 25°C only. (T_A = +25°C, V_{IN} = +15V unless otherwise specified)

Parameter	AD586JCHIPS Min	Typ	Max	Units
Output Voltage	4.980		5.020	V
Gain Adjustment	+6			%
	−2			%
Line Regulation				
10.8V < + V_{IN} < 36V			100	± µV/V
Load Regulation				
Sourcing 0 < I_{OUT} < 10mA			100	µV/mA
Sinking −10 < I_{OUT} < 0mA			400	µV/mA
Quiescent Current			3	mA
Short-Circuit Current-to-Ground			60	mA

DIE LAYOUT



Die Size: 0.096 × 0.061 Inches

NOTES

[1]Both V_{OUT} pads should be connected to the output.

Die Thickness: The standard thickness of Analog Devices Bipolar dice is 24 mils ± 2 mils.

Die Dimensions: The dimensions given have a tolerance of ± 2 mils.

Backing: The standard backside surface is silicon (not plated). Analog Devices does not recommend gold-backed dice for most applications.

Edges: A diamond saw is used to separate wafers into dice thus providing perpendicular edges half-way through the die. In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pick-up) while the uniform shape and size simplifies substrate design and die attach.

Top Surface: The standard top surface of the die is covered by a layer of glassivation. All areas are covered except bonding pads and scribe lines.

Surface Metalization: The metalization to Analog Devices bipolar dice is aluminum. Minimum thickness is 10,000Å.

Bonding Pads: All bonding pads have a minimum size of 4 mils by 4 mils. The passivation windows have 3.5 mils by 3.5 mils minimum.

ORDERING GUIDE

Model[1]	Initial Error mV	Temp. Coefficient ppm/°C	Temp. Range °C	Package Option[2]
AD586JN	20	25	0 to +70	N-8
AD586JQ	20	25	0 to +70	Q-8
AD586JR	20	25	0 to +70	R-8
AD586KN	5	15	0 to +70	N-8
AD586KQ	5	15	0 to +70	Q-8
AD586KR	5	15	0 to +70	R-8
AD586LN	2.5	5	0 to +70	N-8
AD586LR	2.5	5	0 to +70	R-8
AD586MN	2	2	0 to +70	N-8
AD586AR	5	15	−40 to +85	N-8
AD586BR	2.5	5	−40 to +85	N-8
AD586LQ	2.5	5	0 to +70	Q-8
AD586SQ	10	20	−55 to +125	Q-8
AD586TQ	2.5	10	−55 to +125	Q-8
AD586JCHIPS	20	25	0 to +70	–

NOTES

[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD586/883B data sheet.

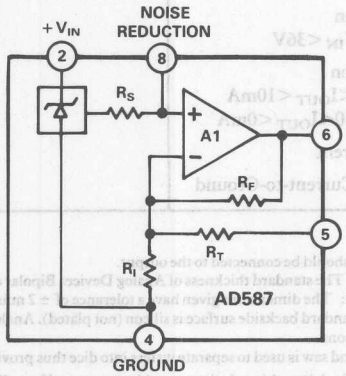
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

High Precision 10V Reference

AD587

FEATURES
Laser Trimmed to High Accuracy:
10.000V ±5mV (L and U Grades)
Trimmed Temperature Coefficient:
5ppm/°C max, (L and U Grades)
Noise Reduction Capability
Low Quiescent Current: 4mA max
Output Trim Capability
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



NOTE: PINS 1, 3 & 7 ARE INTERNAL TEST POINTS. NO CONNECTIONS TO THESE POINTS.

PRODUCT DESCRIPTION

The AD587 represents a major advance in the state-of-the-art in monolithic voltage references. Using a proprietary ion-implanted buried Zener diode and laser wafer trimming of high stability thin-film resistors, the AD587 provides outstanding performance at low cost.

The AD587 offers much higher performance than most other 10V references. Because the AD587 uses an industry standard pinout, many systems can be upgraded instantly with the AD587. The buried Zener approach to reference design provides lower noise and drift than band-gap voltage references. The AD587 offers a noise reduction pin which can be used to further reduce the noise level generated by the buried Zener.

The AD587 is recommended for use as a reference for 8-, 10-, 12-, 14- or 16-bit D/A converters which require an external precision reference. The device is also ideal for successive approximation or integrating A/D converters with up to 14 bits of accuracy and, in general, can offer better performance than the standard on-chip references.

The AD587J, K and L are specified for operation from 0 to +70°C, and the AD587S, T and U are specified for −55°C to +125°C operation. All grades are available in 8-pin cerdip. The J and K versions are also available in an 8-pin Small Outline IC (SOIC) package for surface mount applications, while the J, K and L grades also come in an 8-pin plastic package.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficients results in very low errors over temperature without the use of external components. The AD587L has a maximum deviation from 10.000V of ±8.5mV between 0 and +70°C, and the AD587U guarantees ±14mV maximum total error between −55°C and +125°C.
2. For applications requiring higher precision, an optional fine-trim connection is provided.
3. Any system using an industry standard pinout 10 volt reference can be upgraded instantly with the AD587.
4. Output noise of the AD587 is very low, typically 4μV p-p. A noise reduction pin is provided for additional noise filtering using an external capacitor.
5. The AD587 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD587/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (T_A = +25°C, V_{IN} = +15 V unless otherwise noted)

Model	AD587J/S Min	AD587J/S Typ	AD587J/S Max	AD587K/T Min	AD587K/T Typ	AD587K/T Max	AD587L/U Min	AD587L/U Typ	AD587L/U Max	Units
Output Voltage	9.990		10.010	9.995		10.005	9.995		10.005	V
Output Voltage Drift[1]										
0 to +70°C			20			10			5	ppm/°C
−55°C to +125°C			20			10			5	
Gain Adjustment	+3			+3			+3			%
	−1			−1			−1			
Line Regulation[1]										
13.5V ≤ +V_{IN} ≤36V										
T_{min} to T_{max}			100			100			100	± µV/V
Load Regulation[1]										
Sourcing 0 < I_{OUT} <10mA										
T_{min} to T_{max}			100			100			100	± µV/mA
Sinking −10 < I_{OUT} <0mA[2]										
T_{min} to T_{max}			100			100			100	
Quiescent Current		2	4		2	4		2	4	mA
Power Dissipation		30			30			30		mW
Output Noise										
0.1Hz to 10Hz		4			4			4		µV p-p
Spectral Density, 100Hz		100			100			100		nV/√Hz
Long-Term Stability		15			15			15		± ppm/1000Hr
Short-Circuit Current-to-Ground		30	50		30	50		30	50	mA
Short-Circuit Current-to-V_{IN}		30	50		30	50		30	50	mA
Temperature Range										
Specified Performance (J, K, L)	0		+70	0		+70	0		+70	°C
Operating Performance (J, K, L)[3]	−40		+85	−40		+85	−40		+85	
Specified Performance (S, T, U)	−55		+125	−55		+125	−55		+125	
Operating Performance (S, T, U)[3]	−55		+125	−55		+125	−55		+125	

NOTES
[1]Spec is guaranteed for all packages and grades. Cerdip packaged parts are 100% production tested.
[2]Load Regulation (Sinking) specification for SOIC (R) package is ± 200µV/mA.
[3]The operating temperature ranged is defined as the temperatures extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

Specifications subject to change without notice.

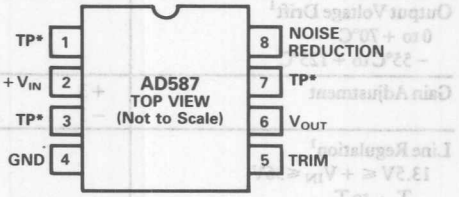
ORDERING GUIDE

Model[1]	Initial Error mV	Temp. Coefficient ppm/°C	Temp. Range °C	Package Options[2]
AD587JQ	10	20	0 to +70	Q-8
AD587JR	10	20	0 to +70	R-8
AD587JN	10	20	0 to +70	N-8
AD587KQ	5	10	0 to +70	Q-8
AD587KR	5	10	0 to +70	R-8
AD587KN	5	10	0 to +70	N-8
AD587LQ	5	5	0 to +70	Q-8
AD587LN	5	5	0 to +70	N-8
AD587SQ	10	20	−55 to +125	Q-8
AD587TQ	10	10	−55 to +125	Q-8
AD587UQ	5	5	−55 to +125	Q-8
AD587JCHIPS	10	20	0 to +70	–

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD587/883B data sheet.
[2]N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

Storage Temperature . . . . . −65°C to +150°C
Lead Temp (Soldering, 10sec) . . . . . 300°C
Package Thermal Resistance
θ_{JC} . . . . . 22°C/W
θ_{JA} . . . . . 110°C/W
Output Protection: Output safe for indefinite short to ground and momentary short to V_{IN}.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



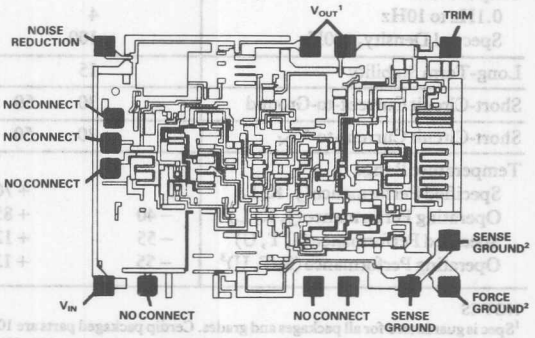
*TP DENOTES FACTORY TEST POINT. NO CONNECTIONS SHOULD BE MADE TO THESE PINS.

DIE SPECIFICATIONS

The following specifications are tested at the die level for AD587JCHIPS. These die are probed at 25°C only. (T_A = +25°C, V_{IN} = +15V unless otherwise noted)

Parameter	AD587JCHIPS Min	Typ	Max	Units
Output Voltage	9.990		10.010	V
Gain Adjustment	−1		3	%
Line Regulation 13.5V < +V_{IN} <36V			100	±μV/V
Load Regulation Sourcing 0<I_{OUT} <10mA Sinking −10<I_{OUT} <0mA			100 100	μV/mA μV/mA
Quiescent Current		2	4	mA
Short-Circuit Current-to-Ground			50	mA
Short-Circuit Current-to-V_{OUT}			50	mA

DIE LAYOUT



Die Size: 0.081 × 0.060 inches

NOTES
[1]Both V_{OUT} pads should be connected to the output.
[2]Sense and force grounds must be tied together.

Die Thickness: The standard thickness of Analog Devices Bipolar dice is 24 mils ± 2 mils.
Die Dimensions: The dimensions given have a tolerance of ± 2 mils.
Backing: The standard backside surface is silicon (not plated). Analog Devices does not recommend gold-backed dice for most applications.
Edges: A diamond saw is used to separate wafers into dice thus providing perpendicular edges half-way through the die. In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pick-up) while the uniform shape and size simplifies substrate design and die attach.
Top Surface: The standard top surface of the die is covered by a layer of glassivation. All areas are covered except bonding pads and scribe lines.
Surface Metalization: The metalization to Analog Devices bipolar dice is aluminum. Minimum thickness is 10,000Å.
Bonding Pads: All bonding pads have a minimum size of 4 mils by 4 mils. The passivation windows have 3.5 mils by 3.5 mils minimum.

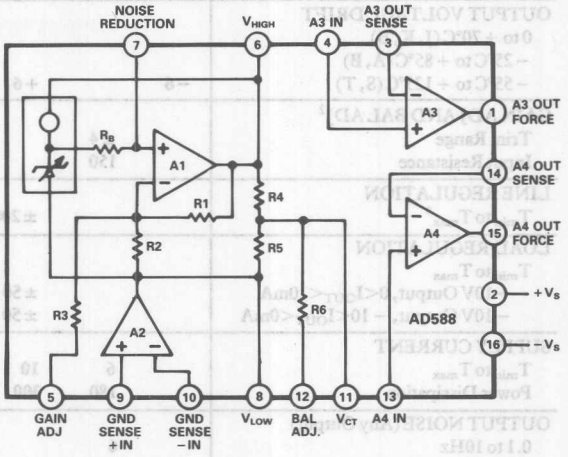
ANALOG DEVICES

High Precision Voltage Reference

AD588*

FEATURES
Low Drift – 1.5ppm/°C
Low Initial Error – 1mV
Pin-Programmable Output
+10V, +5V, ±5V Tracking, −5V, −10V
Flexible Output Force and Sense Terminals
High Impedance Ground Sense
Machine-Insertable DIP Packaging
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD588 represents a major advance in the state-of-the-art in monolithic voltage references. Low initial error and low temperature drift give the AD588 absolute accuracy performance previously not available in monolithic form. The AD588 uses a proprietary ion-implanted buried Zener diode, and laser-wafer-drift-trimming of high stability thin-film resistors to provide outstanding performance at low cost.

The AD588 includes the basic reference cell and three additional amplifiers which provide pin-programmable output ranges. The amplifiers are laser-trimmed for low offset and low drift to maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high-current loads, delivering the full accuracy of the AD588 where it is required in the application circuit.

The low initial error allows the AD588 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD588 can provide a known voltage for system calibration in software and the low drift allows compensation for the drift of other components in a system. Manual system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD588 in conjunction autocalibration software.

The AD588 is available in seven versions. The AD588 JQ and KQ grades are packaged in a 16-pin cerdip and are specified for 0 to +70°C operation. AD588AD and BD grades are packaged in a 16-pin side-brazed ceramic DIP and are specified for the −25°C to +85°C industrial temperature range. The ceramic AD588SD and TD grades are specified for the full military/aerospace temperature range. For military surface mount applications, the AD588SE and TE grades will also be available in 20-pin LCC packages.

***Covered by Patent Number 4,644,253**

PRODUCT HIGHLIGHTS

1. The AD588 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the Zener or the buffer amplifiers and thus does not increase the temperature drift.
2. Output noise of the AD588 is very low – typically 6μV p-p. A pin is provided for additional noise filtering using an external capacitor.
3. A precision ±5V tracking mode with Kelvin output connections is available with no external components. Tracking error is less than one millivolt and a fine-trim is available for applications requiring exact symmetry between the +5V and −5V outputs.
4. Pin strapping capability allows configuration of a wide variety of outputs: ±5V, +5V & +10V, −5V & −10V dual outputs or +5V, −5V, +10V, −10V single outputs.
5. Extensive temperature testing at −55°C, −25°C, 0, +25°C, +50°C, +70°C, +85°C and +125°C ensures that the specified temperature coefficient is truly representative of device performance.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD588—SPECIFICATIONS (typical @ +25°C, +10V output, V_S = ±15V unless otherwise noted[1])

	AD588SD			AD588JQ/AD/TD			AD588KQ/BD			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
OUTPUT VOLTAGE ERROR										
+10V, −10V Outputs	−5		+5	−3		+3	−1		+1	mV
+5V, −5V Outputs	−5		+5	−3		+3	−1		+1	mV
±5V TRACKING MODE										
Symmetry Error	−1.5		+1.5	−1.5		+1.5	−0.75		+0.75	mV
OUTPUT VOLTAGE DRIFT										
0 to +70°C (J, K, B)				−3	±2	+3	−1.5		+1.5	ppm/°C
−25°C to +85°C (A, B)				−3		+3	−3		+3	ppm/°C
−55°C to +125°C (S, T)	−6		+6	−4		+4				ppm/°C
GAIN ADJ AND BAL ADJ[2]										
Trim Range		±4			±4			±4		mV
Input Resistance		150			150			150		kΩ
LINE REGULATION										
T_{min} to T_{max}[3]			±200			±200			±200	μV/V
LOAD REGULATION										
T_{min} to T_{max}										
+10V Output, $0<I_{OUT}<10mA$			±50			±50			±50	μV/mA
−10V Output, $-10<I_{OUT}<0mA$			±50			±50			±50	μV/mA
SUPPLY CURRENT										
T_{min} to T_{max}		6	10		6	10		6	10	mA
Power Dissipation		180	300		180	300		180	300	mW
OUTPUT NOISE (Any Output)										
0.1 to 10Hz		6			6			6		μV p-p
Spectral Density, 100Hz		100			100			100		$nV/\sqrt{Hz}$
LONG-TERM STABILITY (@ +25°C)		15			15			15		ppm/1000hr
BUFFER AMPLIFIERS										
Offset Voltage		100			100			100		μV
Offset Voltage Drift		1			1			1		μV/°C
Bias Current		20			20			20		nA
Open Loop Gain		110			110			110		dB
Output Current A3, A4	−10		+10	−10		+10	−10		+10	mA
Common Mode Rejection (A3, A4)										
V_{CM} = 1V p-p		100			100			100		dB
Short-Circuit Current		50			50			50		mA
TEMPERATURE RANGE										
Specified Performance										
J, K Grades				0		+70	0		+70	°C
A, B Grades				−25		+85	−25		+85	°C
S, T Grades	−55		+125	−55		+125				°C

NOTES

[1]Output Configuration
+10V Figure 2a
−10V Figure 2c
+5V, −5V, ±5V Figure 2b
Specifications tested using +10V configuration unless otherwise indicated.

[2]Gain and balance adjustments guaranteed capable of trimming output voltage error and symmetry error to zero.

[3]Test Conditions:
+10V Output $-V_S = -15V, 13.5V \le +V_S \le 18V$
−10V Output $-18V \le -V_S \le -13.5V, +V_S = 15V$
±5V Output $+V_S = +18V, -V_S = -18V$
$+V_S = +10.8V, -V_S = -10.8V$

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Part Number[1]	Initial Error	Temperature Coefficient	Temperature Range °C	Package Option[2]
AD588AD	3mV	3ppm/°C	−25 to +85	Ceramic (D-16)
AD588BD	1mV	1.5ppm/°C	−25 to +85[3]	Ceramic (D-16)
AD588SD	5mV	6ppm/°C	−55 to +125	Ceramic (D-16)
AD588TD	3mV	4ppm/°C	−55 to +125	Ceramic (D-16)
AD588JQ	3mV	3ppm/°C	0 to +70	Cerdip (Q-16)
AD588KQ	1mV	1.5ppm/°C	0 to +70	Cerdip (Q-16)

NOTES

[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD588/883B data sheet.

[2]For outline information see Package Information section.

[3]Temperature coefficient specified from 0 to +70°C.

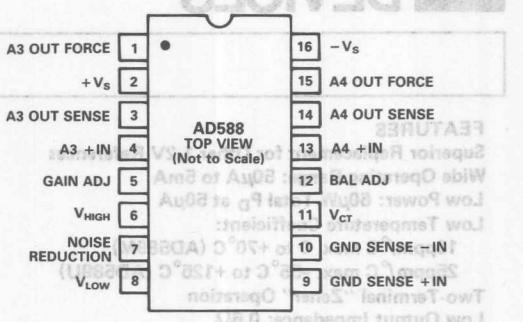
ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to $-V_S$	36V
Power Dissipation (+25°C)	
D Package	600mW
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C
Package Thermal Resistance	
D (θ_{JA}/θ_{JC})	90/25°C/W
Output Protection: All outputs safe if shorted to ground	

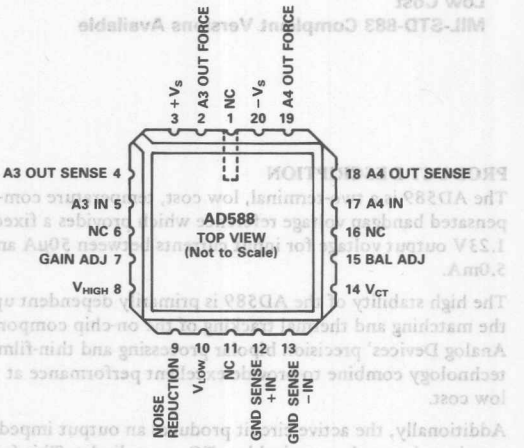
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

DIP



LCC



APPLYING THE AD588

The AD588 can be configured to provide +10V and −10V reference outputs as shown in Figures 2a and 2c respectively. It can also be used to provide +5V, −5V or a ±5V tracking reference as shown in Figure 2b. Table I details the appropriate pin connections for each output range. In each case, pin 9 is connected to system ground and power is applied to pins 2 and 16.

The architecture of the AD588 provides ground sense and uncommitted output buffer amplifiers which offer the user a great deal of functional flexibility. The AD588 is specified and tested in the configurations shown in Figure 2. The user may choose to take advantage of the many other configuration options available with the AD588. However, performance in these configurations is not guaranteed to meet the extremely stringent data sheet specifications.

As indicated in Table I, a +5V buffered output can be provided using amplifier A4 in the +10V configuration (Figure 2a). A −5V buffered output can be provided using amplifier A3 in the −10V configuration (Figure 2c). Specifications are not guaranteed for the +5V or −5V outputs in these configurations. Performance will be similar to that specified for the +10V or −10V outputs.

As indicated in Table I, unbuffered outputs are available at pins 6, 8 and 11. Loading of these unbuffered outputs will impair circuit performance.

Amplifiers A3 and A4 can be used interchangeably. However, the AD588 is tested (and the specifications are guaranteed) with the amplifiers connected as indicated in Figure 2 and Table I.

When either A3 or A4 is unused, its output force and sense pins should be connected and the input tied to ground.

Two outputs of the same voltage may be obtained by connecting both A3 and A4 to the appropriate unbuffered output on pin 6, 8 or 11. Performance in these dual output configurations will typically meet data sheet specifications.

Range	Connect Pin 10 to Pin:	Unbuffered[1] Output on Pins −10V	−5V	0V	+5V	+10V	Buffered Output Connections	Buffered Output on Pins −10V	−5V	0V	+5V	+10V
+10V	8	–	–	8	11	6	11-13 & 14-15	–	–	–	15	–
							6-4 & 3-1	–	–	–	–	1
−5V or +5V	11	–	8	11	6	–	8-13 & 14-15	–	15	–	–	–
							6-4 & 3-1	–	–	–	1	–
−10V	6	8	11	6	–	–	8-13 & 14-15	15	–	–	–	–
							11-4 & 3-1	–	1	–	–	–
+5V	11	–	–	–	6	–	6-4 & 3-1	–	–	–	1	–
−5V		–	8	–	–	–	8-13 & 14-15	–	15	–	–	–

[1]"Unbuffered" outputs should not be loaded.

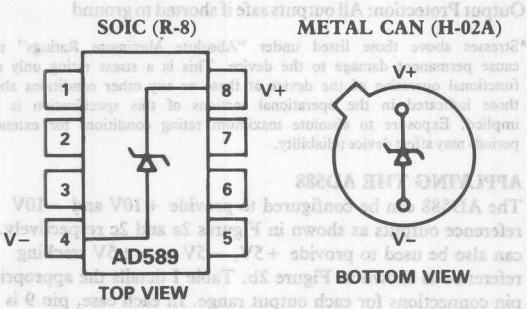
Table I. AD588 Connections

AD589

FEATURES

- Superior Replacement for Other 1.2V References
- Wide Operating Range: 50μA to 5mA
- Low Power: 60μW Total P_D at 50μA
- Low Temperature Coefficient:
  - 10ppm/°C max, 0 to +70°C (AD589M)
  - 25ppm/°C max, –55°C to +125°C (AD589U)
- Two-Terminal "Zener" Operation
- Low Output Impedance: 0.6Ω
- No Frequency Compensation Required
- Low Cost
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD589 is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23V output voltage for input currents between 50μA and 5.0mA.

The high stability of the AD589 is primarily dependent upon the matching and thermal tracking of the on-chip components. Analog Devices' precision bipolar processing and thin-film technology combine to provide excellent performance at low cost.

Additionally, the active circuit produces an output impedance ten times lower than typical low-TC zener diodes. This feature allows operation with no external components required to maintain full accuracy under changing load conditions.

The AD589 is available in seven versions. The AD589J, K, L and M grades are specified for 0 to +70°C operation, while the S, T and U grades are rated for the full –55°C to +125°C temperature range. All grades are available in a metal can (H-02A) package. The AD589J is also available in an 8-pin SOIC package.

PRODUCT HIGHLIGHTS

1. The AD589 is a two-terminal device which delivers a a constant reference voltage for a wide range of input current.
2. Output impedance of 0.6Ω and temperature coefficients as low as 10ppm/°C insure stable output voltage over a wide range of operating conditions.
3. The AD589 can be operated as a positive or negative reference. "Floating" operation is also possible.
4. The AD589 will operate with total current as low as 50μA (60μW total power dissipation), ideal for battery powered instrument applications.
5. The AD589 is an exact replacement for other 1.2V references, offering superior temperature performance and reduced sensitivity to capacitive loading.
6. The AD589 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD589/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

OUTPUT VOLTAGE CHANGE vs. CURRENT (50μA – 5mA)			5			5			5			5	mV
DYNAMIC OUTPUT IMPEDANCE		0.6	2		0.6	2		0.6	2		0.6	2	Ω
RMS NOISE VOLTAGE 10Hz<f<10kHz		5			5			5			5		μV
TEMPERATURE COEFFICIENT[1]			100			50			25			10	ppm/°C
TURN-ON SETTLING TIME TO 0.1%		25			25			25			25		μs
OPERATING CURRENT[2]	0.05		5	0.05		5	0.05		5	0.05		5	mA
OPERATING TEMPERATURE	0		+70	0		+70	0		+70	0		+70	°C
PACKAGE OPTION[3] Metal Can (H-02A) SOIC (R-8)	AD589JH AD589JR			AD589KH			AD589LH			AD589MH			

Model	AD589SH			AD589TH			AD589UH			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE, T_A = +25°C	1.200	1.235	1.250	1.200	1.235	1.250	1.200	1.235	1.250	V
OUTPUT VOLTAGE CHANGE vs. CURRENT (50μA – 5mA)			5			5			5	mV
DYNAMIC OUTPUT IMPEDANCE		0.6	2		0.6	2		0.6	2	Ω
RMS NOISE VOLTAGE 10Hz<f<10kHz		5			5			5		μV
TEMPERATURE COEFFICIENT[1]			100			50			25	ppm/°C
TURN-ON SETTLING TIME TO 0.1%		25			25			25		μs
OPERATING CURRENT[2]	0.05		5	0.05		5	0.05		5	mA
OPERATING TEMPERATURE	−55		+125	−55		+125	−55		+125	°C
PACKAGE OPTION[3] Metal Can (H-02A)	AD589SH			AD589TH			AD589UH			

NOTES

[1]See following page for explanation of temperature coefficient measurement method.

[2]Optimum performance is obtained at currents below 500μA. For current operation below 200μA, stray shunt capacitances should be limited to 20pF or increased to 1μF. If strays can not be avoided, operation at 500μA and a shunt capacitor of at least 1000pF are recommended.

[3]H = Hermetic Metal Can; R = SOIC. For outline information see Package Information section.

Specifications shown in boldface are tested on all production units at final electrical test.

Specifications subject to change without notice.

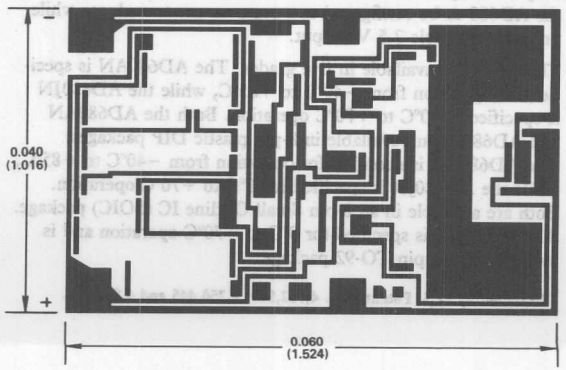
ABSOLUTE MAXIMUM RATINGS

Current	10mA
Reverse Current	10mA
Power Dissipation[1]	125mW
Storage Temperature Range	−65°C to +175°C
Operating Junction Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

NOTE

[1]Absolute maximum power dissipation is limited by maximum current through the device. Maximum rating at elevated temperatures must be computed assuming $T_J \leq 150°C$, and $\theta_{JA} = 400 = C/W$.

AD589 CHIP DIMENSIONS AND PAD LAYOUT



THE AD589 IS AVAILABLE IN CHIP FORM WITH FULLY TESTED AND GUARANTEED SPECIFICATIONS. CONSULT FACTORY FOR AVAILABLE GRADES AND PRICING.

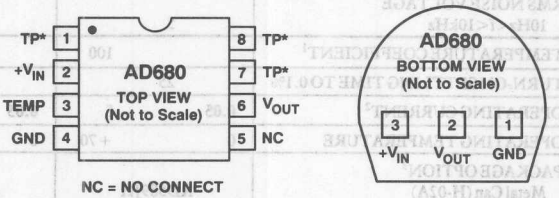
Low Power, Low Cost 2.5 V Reference

AD680*

FEATURES

- Low Quiescent Current: 250 μA max
- Laser Trimmed to High Accuracy:
  - 2.5 V ±5 mV max (AN, AR Grade)
- Trimmed Temperature Coefficient:
  - 20 ppm/°C max (AN, AR Grade)
- Low Noise: 8 μV p–p from 0.1 to 10 Hz
  - 250 nV/$\sqrt{\text{Hz}}$ Wideband
- Temperature Output Pin (N, R Packages)
- Available in Three Package Styles:
  - 8-Pin Plastic DIP, 8-Pin SOIC and 3-Pin TO-92

CONNECTION DIAGRAMS



NC = NO CONNECT

*TP DENOTES FACTORY TEST POINT. NO CONNECTIONS SHOULD BE MADE TO THESE PINS.

PRODUCT DESCRIPTION

The AD680 is a bandgap voltage reference which provides a fixed 2.5 V output from inputs between 4.5 V and 36 V. The architecture of the AD680 enables the reference to be operated at a very low quiescent current while still realizing excellent dc characteristics and noise performance. Trimming of the high stability thin-film resistors is performed for initial accuracy and temperature coefficient, resulting in low errors over temperature.

The precision dc characteristics of the AD680 make it ideal for use as a reference for D/A converters which require an external precision reference. The device is also ideal for A/D converters and, in general, can offer better performance than the standard on-chip references.

Based upon the low quiescent current of the AD680, which rivals that of many incomplete two-terminal references, the AD680 is recommended for low power applications such as hand-held battery equipment.

A temperature output pin is provided on the 8-pin package versions of the AD680. The temperature output pin provides an output voltage that varies linearly with temperature and allows the AD680 to be configured as a temperature transducer while providing a stable 2.5 V output.

The AD680 is available in five grades. The AD680AN is specified for operation from −40°C to +85°C, while the AD680JN is specified for 0°C to +70°C operation. Both the AD680AN and AD680JN are available in 8-pin plastic DIP packages. The AD680AR is specified for operation from −40°C to +85°C, while the AD680JR is specified for 0°C to +70°C operation. Both are available in an 8-pin Small Outline IC (SOIC) package. The AD680JT is specified for 0°C to +70°C operation and is available in a 3-pin TO-92 package.

*Protected by U.S. Patent Nos. 4,902,959; 4,250,445 and 4,857,862.

PRODUCT HIGHLIGHTS

1. The AD680 bandgap reference operates on a very low quiescent current which rivals that of many two-terminal references. This makes the complete, higher accuracy AD680 ideal for use in power sensitive applications.
2. Laser trimming of both initial accuracy and temperature coefficients results in low errors over temperature without the use of external components. The AD680AN and AD680AR have a maximum variation of 6.25 mV between −40°C and +85°C.
3. The AD680 noise is low, typically 8 μV p–p from 0.1 to 10 Hz. Spectral density is also low, typically 250 nV/$\sqrt{\text{Hz}}$.
4. The temperature output pin on the 8-pin package versions enables the AD680 to be configured as a temperature transducer.
5. Plastic DIP packaging provides machine insertability, while SOIC packaging provides surface mount capability. TO-92 packaging offers a cost effective alternative to two-terminal references, offering a complete solution in the same package in which two-terminal references are usually found.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (T_A = +25°C, V_{IN} = +5 V unless otherwise specified)

Model	AD680AN/AR Min	AD680AN/AR Typ	AD680AN/AR Max	AD680JN/JR Min	AD680JN/JR Typ	AD680JN/JR Max	AD680JT Min	AD680JT Typ	AD680JT Max	Units
OUTPUT VOLTAGE	2.495		2.505	2.490		2.510	2.490		2.510	V
OUTPUT VOLTAGE DRIFT[1]										
0°C to +70°C		10			10	25		10	30	ppm/°C
−40°C to +85°C			20		25			25		
LINE REGULATION										
4.5 V ≤ +V_{IN} ≤ 15 V			40			*			*	µV/V
(@ T_{min} to T_{max})			40			*			*	
15 V ≤ +V_{IN} ≤ 36 V			40			*			*	
(@ T_{min} to T_{max})			40			*			*	
LOAD REGULATION										
0 < I_{OUT} < 10 mA		80	100		*	*		*	*	µV/mA
(@ T_{min} to T_{max})		80	100		*	*		*	*	
QUIESCENT CURRENT		195	250		*	*		*	*	µA
(@ T_{min} to T_{max})			280			*			*	
POWER DISSIPATION		1	1.25		*	*		*	*	mW
OUTPUT NOISE										
0.1 to 10 Hz		8	10		*	*		*	*	µV p–p
Spectral Density, 100 Hz		250			*			*		nV/√Hz
CAPACITIVE LOAD			50			*			*	nF
LONG TERM STABILITY		25			*			*		ppm/1000 hr
SHORT CIRCUIT CURRENT TO GROUND		25	50		*	*		*	*	mA
TEMPERATURE PIN										
Voltage Output @ 25°C	540	596	660	*	*	*				mV
Temperature Sensitivity		2			*					mV/°C
Output Current	−5		+5	*		*				µA
Output Resistance		12			*					kΩ
TEMPERATURE RANGE										
Specified Performance	−40		+85	0		+70	0		+70	°C
Operating Performance[2]	−40		+85	−40		+85	−40		+85	

NOTES

[1]Maximum output voltage drift is guaranteed for all packages.

[2]The operating temperature range is defined as the temperature extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

*Same as AD680AN/AR specification.

Specifications subject to change without notice.

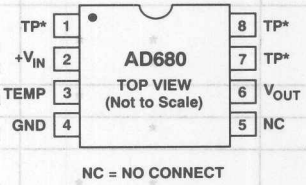
Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed.

8

V_{IN} to Ground . . . . . 36 V
Power Dissipation (25°C) . . . . . 500 mW
Storage Temperature . . . . . −65°C to +125°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Package Thermal Resistance
θ_{JA} (All Packages) . . . . . 120°C/W
Output Protection: Output safe for indefinite short to ground and momentary short to V_{IN}.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8-Pin Plastic DIP and 8-Pin SOIC Packages



NC = NO CONNECT

*TP DENOTES FACTORY TEST POINT. NO CONNECTIONS SHOULD BE MADE TO THESE PINS.

TO-92 Package

Figure 1. Connection Diagrams

Bandgap references are the high performance solution for low supply voltage operation. A typical precision bandgap will consist of a reference core and buffer amplifier. Based on a new, patented bandgap reference design (Figure 2), the AD680 merges the amplifier and the core bandgap function to produce a compact, complete precision reference. Central to the device is a high gain amplifier with an intentionally large Proportional To Absolute Temperature (PTAT) input offset. This offset is controlled by the area ratio of the amplifier input pair, Q1 and Q2, and is developed across resistor R1. Transistor Q12's base emitter voltage has a Complementary To Absolute Temperature (CTAT) characteristic. Resistor R2 and the parallel combination of R3 and R4 "multiply" the PTAT voltage across R1. Trimming resistors R3 and R4 to the proper ratio produces a temperature invariant 2.5 V at the output. The result is an accurate, stable output voltage accomplished with a minimum number of components.

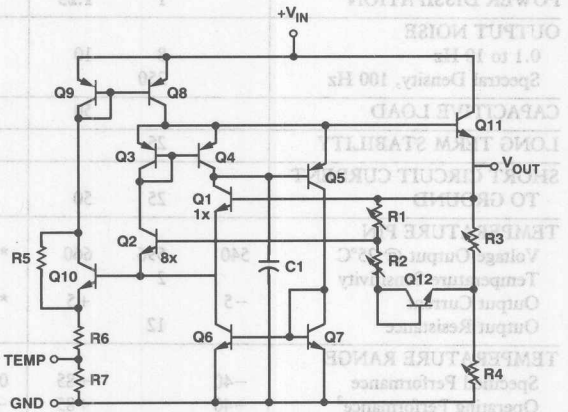


Figure 2. AD680 Schematic Diagram

An additional feature with this approach is the ability to minimize the noise while maintaining very low overall power dissipation for the entire circuit. Frequently it is difficult to independently control the dominant noise sources for bandgap references: bandgap transistor noise and resistor thermal noise. By properly choosing the operating currents of Q1 and Q2 and separately sizing R1, low wideband noise is realized while maintaining 1 mW typical power dissipation.

ORDERING GUIDE

Model	Initial Error mV	Temperature Coeff. ppm/°C	Temperature Range	Package Description	Package Option*
AD680JN	10	25	0°C to +70°C	Plastic	N-8
AD680JR	10	25	0°C to +70°C	SOIC	R-8
AD680JT	10	30	0°C to +70°C	TO-92	TO-92
AD680AN	5	20	−40°C to +85°C	Plastic	N-8
AD680AR	5	20	−40°C to +85°C	SOIC	R-8

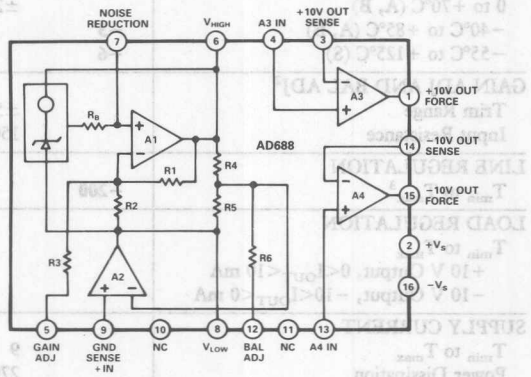
*N = Plastic DIP Package; R = SOIC Package; T = TO-92 Package. For outline information see Package Information section.

AD688*

FEATURES

±10 V Tracking Outputs
Kelvin Connections
Low Tracking Error – 1.5 mV
Low Initial Error – 2.0 mV
Low Drift – 1.5 ppm/°C
Low Noise – 6 μV p–p
Flexible Output Force and Sense Terminals
High Impedance Ground Sense
Machine Insertable DIP Packaging
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD688 is a high precision ±10 V tracking reference. Low tracking error, low initial error and low temperature drift give the AD688 reference absolute ±10 V accuracy performance previously unavailable in monolithic form. The AD688 uses a proprietary ion-implanted buried Zener diode, and laser-wafer-drift-trimming of high stability thin-film resistors to provide outstanding performance at low cost.

The AD688 includes the basic reference cell and three additional amplifiers. The amplifiers are laser-trimmed for low offset and low drift and maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high current loads, delivering the full accuracy of the AD688 where it is required in the application circuit.

The low initial error allows the AD688 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD688 can provide a known voltage for system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD688 and calibration software.

The AD688 is available in three versions. The AD688AQ and BQ grades are packaged in 16-pin cerdip (0.3″) packages and are specified for operation from −40°C to +85°C. The AD688SQ grade is specified for operation from −55°C to +125°C.

***Protected by Patent Number 4,644,253.**

PRODUCT HIGHLIGHTS

1. The AD688 offers precision tracking ±10 V Kelvin output connections with no external components. Tracking error is less than 1.5 mV and a fine-trim is available for applications requiring exact symmetry between the +10 V and −10 V outputs.
2. The AD688 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the Zener or the buffer amplifiers and thus does not increase the temperature drift.
3. Output noise of the AD688 is low – typically 6 μV p–p. A pin is provided for broadband noise filtering using an external capacitor.
4. The AD688 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD688/883B data sheet for detailed specifications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD688—SPECIFICATIONS (typical @ +25°C, +10 V output, V_S = ±15 V unless otherwise noted[1])

	AD688AQ/SQ			AD688BQ			
	Min	Typ	Max	Min	Typ	Max	Units
OUTPUT VOLTAGE ERROR							
+10V, −10V Outputs	−5		+5	−2		+2	mV
±10V TRACKING ERROR	−3		+3	−1.5		+1.5	mV
OUTPUT VOLTAGE DRIFT							
+10V, −10V Outputs							
0 to +70°C (A, B)		±2		−1.5		+1.5	ppm/°C
−40°C to +85°C (A, B)	−3		+3	−3		+3	ppm/°C
−55°C to +125°C (S)	−6		+6				ppm/°C
GAIN ADJ AND BAL ADJ[2]							
Trim Range		±5			±5		mV
Input Resistance		150			150		kΩ
LINE REGULATION							
T_{min} to T_{max}[3]	−200		+200	−200		+200	μV/V
LOAD REGULATION							
T_{min} to T_{max}							
+10 V Output, $0<I_{OUT}<10$ mA			±50			±50	μV/mA
−10 V Output, $-10<I_{OUT}<0$ mA			±50			±50	μV/mA
SUPPLY CURRENT							
T_{min} to T_{max}		9	12		9	12	mA
Power Dissipation		270	360		270	360	mW
OUTPUT NOISE (ANY OUTPUT)							
0.1 Hz to 10 Hz		6			6		μV p–p
Spectral Density, 100 Hz		140			140		nV/√Hz
LONG TERM STABILITY (@ +25°C)		15			15		ppm/1000 hours
BUFFER AMPLIFIERS							
Offset Voltage		100			100		μV
Offset Voltage Drift		1			1		μV/°C
Bias Current		20			20		nA
Open Loop Gain		110			110		dB
Output Current A3, A4	−10		+10	−10		+10	mA
Common Mode Rejection (A3, A4)							
V_{CM} = 1 V p–p		100			100		dB
Short-Circuit Current		50			50		mA
TEMPERATURE RANGE							
Specified Performance							
A, B Grades	−40		+85	−40		+85	°C
S Grade	−55		+125				°C

NOTES

[1]See Figure 2a for output configuration. Specifications tested using +10 V output unless otherwise indicated.

[2]Gain and balance adjustments guaranteed capable of trimming output voltage error and symmetry error to zero.

[3]Test Condition: $+V_S$ = +18 V, $-V_S$ = −18 V; $+V_S$ = +13.5 V, $-V_S$ = −13.5 V.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to $-V_S$ . . . . . 36 V

Power Dissipation (+25°C)

Q Package . . . . . 600 mW

Storage Temperature . . . . . −65°C to +150°C

Lead Temperature (Soldering, 10 Seconds) . . . . . +300°C

Package Thermal Resistance

Q (θ_{JA}/θ_{JC}) . . . . . 120/35°C/W

Output Protection: All outputs safe if shorted to ground

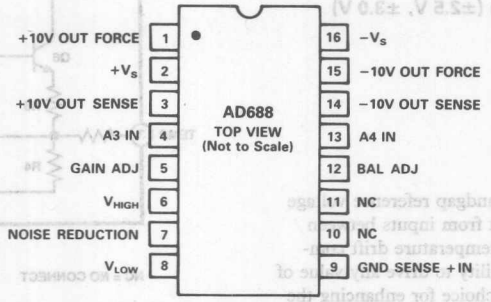
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ORDERING GUIDE

Part Number[1]	Initial Error	Temperature Coefficient	Temperature Range – °C	Package Option[2]
AD688AQ	5 mV	3 ppm/°C	−40 to +85	Q-16
AD688BQ	2 mV	3 ppm/°C	−40 to +85[3]	Q-16
AD688SQ	5 mV	6 ppm/°C	−55 to +125	Q-16
AD688/883B	*	*	−55 to +125	*

NOTE
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD688/883B data sheet.
[2]Q = Cerdip. For outline information see Package Information section.
[3]Temperature coefficient specified from 0 to +70°C.
*Refer to AD688/883B military data sheet.

PIN CONFIGURATION



NC = NO CONNECT

NC PINS ARE USED AS TEST POINTS BY THE FACTORY. TO ENSURE PROPER OPERATION, DO NOT CONNECT ANYTHING TO THESE PINS.

THEORY OF OPERATION

The AD688 consists of a buried Zener diode reference, amplifiers and associated thin-film resistors as shown in the block diagram of Figure 1. The temperature compensation circuitry provides the device with a temperature coefficient of 1.5 ppm/°C or less.

Amplifier A1 performs several functions. A1 primarily acts to amplify the Zener voltage to the required 20 volts. In addition, A1 also provides for external adjustment of the 20 V output through Pin 5, the GAIN ADJUST. Using the bias compensation resistor between the Zener output and the noninverting input to A1, a capacitor can be added at the NOISE REDUCTION pin (Pin 7) to form a low pass filter and reduce the noise contribution of the Zener to the circuit. Two matched 12 kΩ nominal thin-film resistors (R4 and R5) divide the 20 V output in half.

Ground sensing for the circuit is provided by Amplifier A2. The noninverting input (Pin 9) senses the system ground and forces the midpoint of resistors R4 and R5 to be a virtual ground. Pin 12 (BALANCE ADJUST) can be used for fine adjustment of this midpoint transfer.

Amplifiers A3 and A4 are internally compensated and are used to buffer the voltages at Pins 6 and 8 as well as to provide a full Kelvin output. Thus, the AD688 has a full Kelvin capability by providing the means to sense a system ground and provide forced and sensed outputs referenced to that ground.

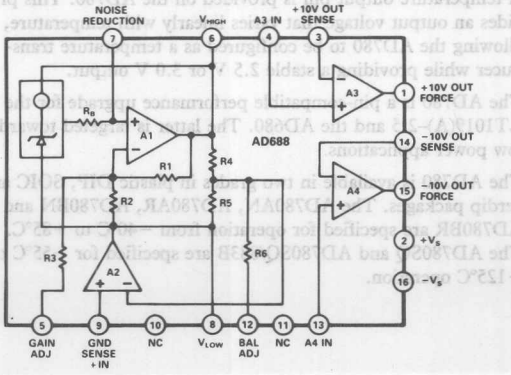


Figure 1. AD688 Functional Block Diagram

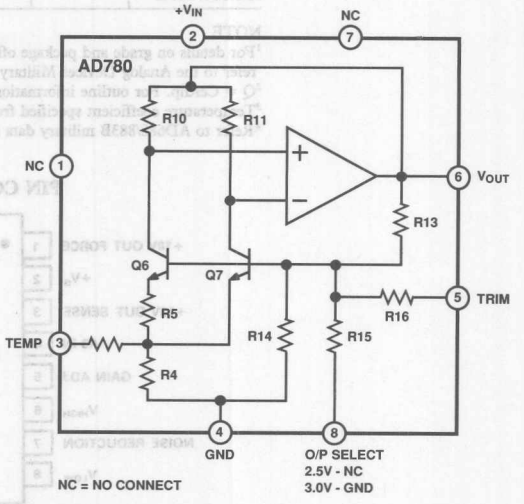
2.5 V/3.0 V High Precision Reference

AD780

FEATURES

Pin-Programmable 2.5 V or 3.0 V Output
Ultralow Drift: 3 ppm/°C max
High Accuracy: 2.5 V or 3.0 V ± 1 mV max
Low Noise: 100 nV/$\sqrt{Hz}$
Noise Reduction Capability
Low Quiescent Current: 1 mA max
Output Trim Capability
Plug-In Upgrade for Present References
Temperature Output Pin
Series or Shunt Mode Operation (±2.5 V, ±3.0 V)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD780 is an ultrahigh precision bandgap reference voltage which provides a 2.5 V or 3.0 V output from inputs between 4.0 V and 36 V. Low initial error and temperature drift combined with low output noise and the ability to drive any value of capacitance make the AD780 the ideal choice for enhancing the performance of high resolution ADCs and DACs and for any general purpose precision reference application. A unique low headroom design facilitates a 3.0 V output from a 5.0 V ± 10% input, providing a 20% boost to the dynamic range of an ADC, over performance with existing 2.5 V references.

The AD780 can be used to source or sink up to 10 mA and can be used in series or shunt mode, thus allowing positive or negative output voltages without external components. This makes it suitable for virtually any high performance reference application. Unlike some competing references, the AD780 has no "region of possible instability." The part is stable under all load conditions when a 1 μF bypass capacitor is used on the supply.

A temperature output pin is provided on the AD780. This provides an output voltage that varies linearly with temperature, allowing the AD780 to be configured as a temperature transducer while providing a stable 2.5 V or 3.0 V output.

The AD780 is a pin-compatible performance upgrade for the LT1019(A)–2.5 and the AD680. The latter is targeted toward low power applications.

The AD780 is available in two grades in plastic DIP, SOIC and cerdip packages. The AD780AN, AD780AR, AD780BN and AD780BR are specified for operation from −40°C to +85°C. The AD780SQ and AD780SQ/883B are specified for −55°C to +125°C operation.

PRODUCT HIGHLIGHTS

1. The AD780 provides a pin-programmable 2.5 V or 3.0 V output from a 4 V to 36 V input.
2. Laser trimming of both initial accuracy and temperature coefficients results in low errors over temperature without the use of external components. The AD780BN has a maximum variation of 0.8 mV from −40°C to +85°C.
3. For applications requiring even higher accuracy, an optional fine-trim connection is provided.
4. The AD780 noise is extremely low, typically 4 μV p-p from 0.1 Hz to 10 Hz and a wideband spectral noise density of typically 100 nV/$\sqrt{Hz}$. This can be further reduced if desired, by simply using two external capacitors.
5. The temperature output pin enables the AD780 to be configured as a temperature transducer while providing a stable output reference voltage.

SPECIFICATIONS (T_A = +25°C, V_{IN} = +5 V unless otherwise noted)

Parameter	AD780AN/AR/SQ Min	Typ	Max	AD780BN/BR Min	Typ	Max	Units
OUTPUT VOLTAGE							
2.5 V Out	2.495		2.505	2.499		2.501	Volts
3.0 V Out	2.995		3.005	2.999		3.001	Volts
OUTPUT VOLTAGE DRIFT[1]							
−40°C to +85°C			7			3	ppm/°C
−55°C to +125°C			20				ppm/°C
LINE REGULATION							
2.5 V Output, 4 V ≤ $+V_{IN}$ ≤ 36 V							
T_{MIN} to T_{MAX}			10		*		μV/V
3.0 V Output, 4.5 V ≤ $+V_{IN}$ ≤ 36 V							
T_{MIN} to T_{MAX}			10			*	μV/V
LOAD REGULATION, SERIES MODE							
Sourcing 0 < I_{OUT} < 10 mA			50			*	μV/mA
T_{MIN} to T_{MAX}			75			*	μV/mA
Sinking −10 < I_{OUT} < 0 mA			75			*	μV/mA
−40°C to +85°C			75			*	μV/mA
−55°C to +125°C			150			*	μV/mA
LOAD REGULATION, SHUNT MODE							
1 < I_{SHUNT} < 10 mA			75			*	μV/mA
QUIESCENT CURRENT, 2.5 V SERIES MODE[2]							
−40°C to +85°C		0.75	1.0		*	*	mA
−55°C to +125°C		0.8	1.3		*	*	mA
MINIMUM SHUNT CURRENT		0.7	1.0		*	*	mA
OUTPUT NOISE							
0.1 Hz to 10 Hz		4			*	*	μV p-p
Spectral Density, 100 Hz		100			*	*	nV/√Hz
LONG TERM STABILITY[3]		20			*		±ppm/1000 Hr
TRIM RANGE	4.0			*			±%
TEMPERATURE PIN							
Voltage Output @ 25°C	500	560	620	*	*	*	mV
Temperature Sensitivity		1.9			*		mV/°C
Output Resistance		3			*		kΩ
SHORT CIRCUIT CURRENT TO GROUND		30			*		mA
TEMPERATURE RANGE							
Specified Performance (A, B)	−40		+85	*		*	°C
Operating Performance (A, B)[4]	−55		+125	*		*	°C
Specified Performance (S)	−55		+125	*		*	°C
Operating Performance (S)	−55		+125	*		*	°C

NOTES

[1]Maximum output voltage drift is guaranteed for all packages.

[2]3.0 V mode typically adds 100 μA to the quiescent current. Also, Iq increases by 2 μA/V above an input voltage of 5 V.

[3]The long term stability specification is noncumulative. The drift in subsequent 1000 hr. periods is significantly lower than in the first 1000 hr. period.

[4]The operating temperature range is defined as the temperature extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

*Same as AD780AN/AR/SQ specification.

Specifications subject to change without notice.

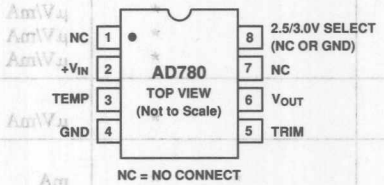
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD780 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

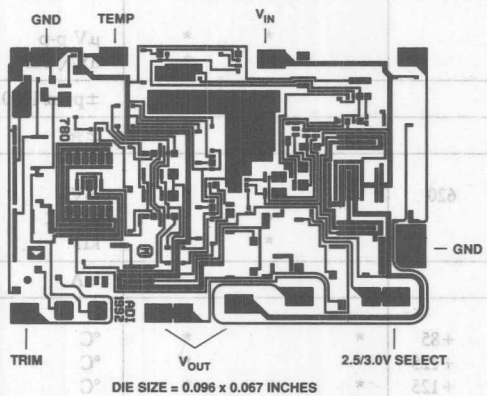
V_{IN} to Ground . . . . . 36 V
Trim Pin to Ground . . . . . 36 V
Temp Pin to Ground . . . . . 36 V
Power Dissipation (25°C) . . . . . 500 mW
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Output Protection: Output safe for indefinite short to ground and momentary short to V_{IN}.
ESD Classification . . . . . Class 1 (1000 V)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational specification is not implied. Exposure to absolute maximum specifications for extended periods may affect device reliability.

PIN CONFIGURATION
8-Pin Plastic DIP, SOIC and Cerdip Packages



DIE LAYOUT



NOTES
Both V_{OUT} pads should be connected to the output.
Die Thickness: The standard thickness of Analog Devices Bipolar dice is 24 mils ±2 mils.
Die Dimensions: The dimensions given have a tolerance of ±2 mils.
Backing: The standard backside surface is silicon (not plated). Analog Devices does not recommend gold-backed dice for most applications.
Edges: A diamond saw is used to separate wafers into dice thus providing perpendicular edges half-way through the die.

In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pick-up) while the uniform shape and size simplifies substrate design and die attach.
Top Surface: The standard top surface of the die is covered by a layer of glassivation. All areas are covered except bonding pads and scribe lines.
Surface Metalization: The metalization to Analog Devices bipolar dice is aluminum. Minimum thickness is 10,000Å.
Bonding Pads: All bonding pads have a minimum size of 4.0 mils by 6.0 mils. The passivation windows have a 3.6 mils by 5.6 mils minimum size.

Model	Initial Error	Temperature Coefficient	Temperature Range	Package Option*
AD780AN	5 mV	7 ppm/°C	−40°C to +85°C	N-8
AD780AR	5 mV	7 ppm/°C	−40°C to +85°C	R-8
AD780BN	1 mV	3 ppm/°C	−40°C to +85°C	N-8
AD780BR	1 mV	3 ppm/°C	−40°C to +85°C	R-8
AD780SQ	5 mV	20 ppm/°C	−55°C to +125°C	Q-8
AD780SQ/883B	5 mV	20 ppm/°C	−55°C to +125°C	Q-8

*For outline information see Package Information section.

THEORY OF OPERATION

Bandgap references are the high performance solution for low supply voltage and low power voltage reference applications. In this technique a voltage with a positive temperature coefficient is combined with the negative coefficient of a transistor's Vbe to produce a constant *bandgap* voltage.

In the AD780, the bandgap cell contains two npn transistors (Q6 and Q7) which differ in emitter area by 12×. The difference in their Vbe's produces a PTAT current in R5. This in turn produces a PTAT voltage across R4, which when combined with the Vbe of Q7, produces a voltage Vbg that does not vary with temperature. Precision laser trimming of the resistors and other patented circuit techniques are used to further enhance the drift performance.

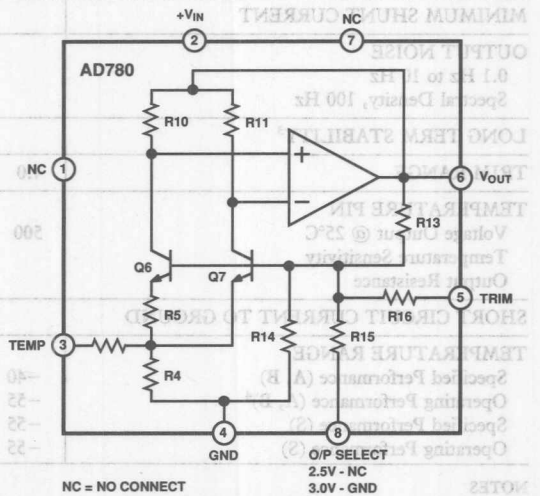


Figure 1. Schematic Diagram

The output voltage of the AD780 is determined by the configuration of resistors R13, R14 and R15 in the amplifier's feedback loop. This sets the output to either 2.5 V or 3.0 V depending on whether R15 (Pin 8) is grounded or not connected.

A unique feature of the AD780 is the low headroom design of the high gain amplifier which produces a precision 3 V output from an input voltage as low as 4.5 V (or 2.5 V from a 4.0 V input). The amplifier design also allows the part to work with $V_{IN} = V_{OUT}$ when current is forced into the output terminal. This allows the AD780 to work as a two terminal shunt regulator providing a −2.5 V or −3.0 V reference voltage output without external components.

The PTAT voltage is also used to provide the user with a thermometer output voltage (at Pin 3) which increases at a rate of approximately 2 mV/°C.

The AD780's NC Pin 7 is a 20 kΩ resistor to V+ which is used solely for production test purposes. Users who are currently using the LT1019 self-heater pin (Pin 7) must take into account the different load on the heater supply.

APPLYING THE AD780

The AD780 can be used without any external components to achieve specified performance. If power is supplied to Pin 2 and Pin 4 is grounded, Pin 6 provides a 2.5 V or 3.0 V output depending on whether Pin 8 is left unconnected or grounded.

A bypass capacitor of 1 μF (V_{IN} to GND) should be used if the load capacitance in the application is expected to be greater than 1 nF. The AD780 in 2.5 V mode typically draws 700 μA of Iq at 5 V. This increases by ~2 μA/V up to 36 V.

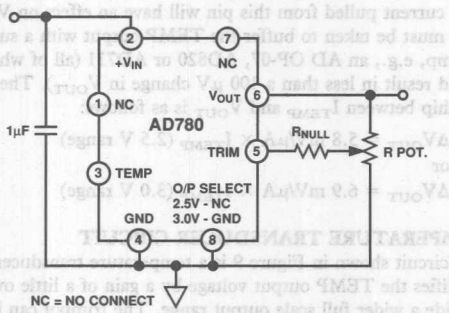


Figure 2. Optional Fine Trim Circuit

Initial error can be nulled using a single 25 kΩ potentiometer connected between V_{OUT}, Trim and GND. This is a coarse trim with an adjustment range of ±4% and is only included here for compatibility purposes with other references. A fine trim can be implemented by inserting a large value resistor (e.g. 1–5 MΩ) in series with the wiper of the potentiometer. See Figure 2 above. The trim range, expressed as a fraction of the output, is simply greater than or equal to 2.1 kΩ/R_{NULL} for either the 2.5 V or 3.0 V mode.

The external null resistor affects the overall temperature coefficient by a factor equal to the percentage of V_{OUT} nulled.

For example a 1 mV (.03%) shift in the output caused by the trim circuit, with a 100 ppm/°C null resistor will add less than 0.06 ppm/°C to the output drift (0.03% × 200 ppm/°C, since the resistors internal to the AD780 also have temperature coefficients of less than 100 ppm/°C).

NOISE PERFORMANCE

The impressive noise performance of the AD780 can be further improved if desired by the addition of two capacitors: a load capacitor C1 between the output and ground, and a compensation capacitor C2 between the TEMP pin and ground. Suitable values are shown in Figure 3.

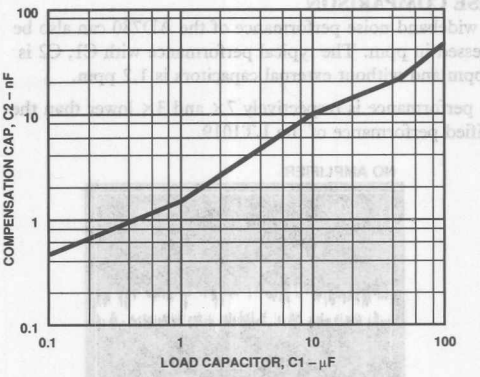


Figure 3. Compensation and Load Capacitor Combinations

C1 and C2 also improve the settling performance of the AD780 when subjected to load transients. The improvement in noise performance is shown in Figures 4, 5 and 6 following.

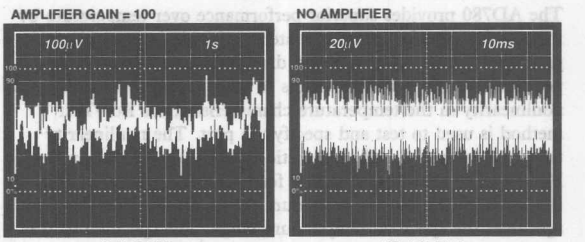


Figure 4. Stand-Alone Noise Performance

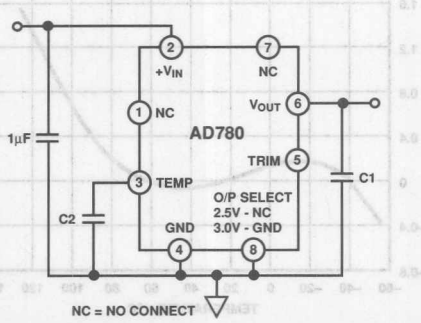


Figure 5. Noise Reduction Circuit

NOISE COMPARISON

The wideband noise performance of the AD780 can also be expressed in ppm. The typical performance with C1, C2 is 0.6 ppm and without external capacitors is 1.2 ppm.

This performance is respectively 7× and 3× lower than the specified performance of the LT1019.

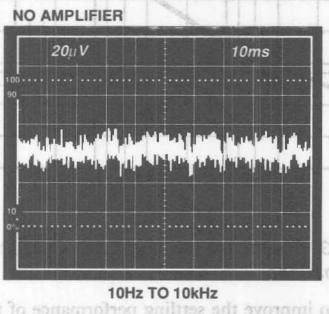


Figure 6. Reduced Noise Performance with C1 = 100 μF, C2 = 100 nF

TEMPERATURE PERFORMANCE

The AD780 provides superior performance over temperature by means of a combination of patented circuit design techniques, precision thin film resistors and drift trimming. Temperature performance is specified in terms of ppm/°C, but because of nonlinearity in the temperature characteristic, the Box-Test method is used to test and specify the part. The nonlinearity takes the form of the characteristic S-shaped curve shown in Figure 7. The Box-Test method forms a rectangular box around this curve, enclosing the maximum and minimum output voltages over the specified temperature range. The specified drift is equal to the slope of the diagonal of this box.

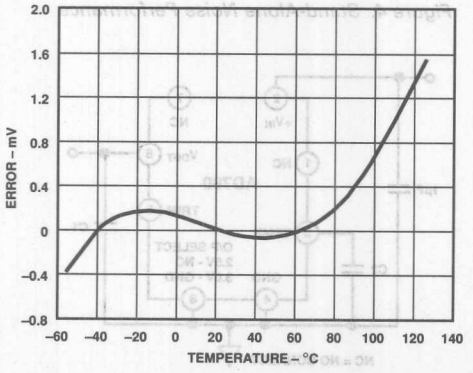


Figure 7. Typical AD780BN Temperature Drift

TEMPERATURE OUTPUT PIN

The AD780 provides a "TEMP" output (Pin 3) that varies linearly with temperature. This output can be used to monitor changes in system ambient temperature and to initiate calibration of the system if desired.

The voltage V_{TEMP} is 560 mV at 25°C, and the temperature coefficient is approximately 2 mV/°C. Figure 8 following shows the typical V_{TEMP} characteristic curve over temperature.

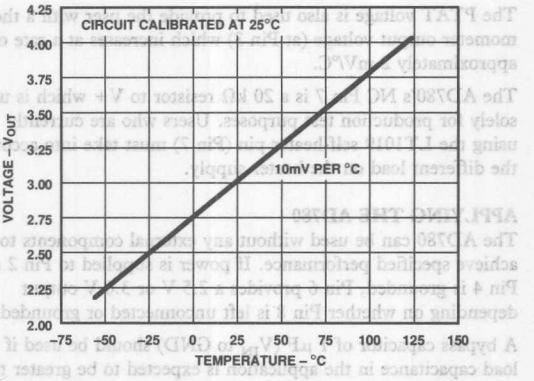


Figure 8. Temperature Pin Transfer Characteristic

Since the TEMP voltage is acquired from the bandgap core circuit, current pulled from this pin will have an effect on V_{OUT}. Care must be taken to buffer the TEMP output with a suitable op amp, e.g., an AD OP-07, AD820 or AD711 (all of which would result in less than a 100 μV change in V_{OUT}). The relationship between I_{TEMP} and V_{OUT} is as follows:

$$\Delta V_{OUT} = 5.8\ mV/\mu A \times I_{TEMP}\ (2.5\ V\ range)$$

or

$$\Delta V_{OUT} = 6.9\ mV/\mu A \times I_{TEMP}\ (3.0\ V\ range)$$

TEMPERATURE TRANSDUCER CIRCUIT

The circuit shown in Figure 9 is a temperature transducer which amplifies the TEMP output voltage by a gain of a little over 5 to provide a wider full scale output range. The trimpot can be used to adjust the output so it varies exactly by 10 mV/°C.

To minimize resistance changes with temperature, resistors with low temperature coefficients, such as metal film resistors should be used.

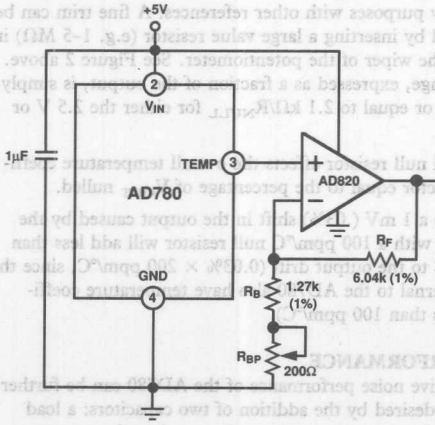


Figure 9. Differential Temperature Transducer

SUPPLY CURRENT OVER TEMPERATURE

The AD780's quiescent current will vary slightly over temperature and input supply range. The test limit is 1 mA over the industrial and 1.3 mA over the military temperature range. Typical performance with input voltage and temperature variation is shown in Figure 10 following.

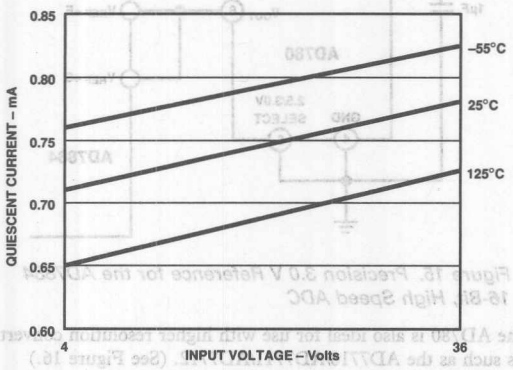


Figure 10. Typical Supply Current over Temperature

TURN-ON TIME

The time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. The two major factors that affect this are the active circuit settling time and the time for the thermal gradients on the chip to stabilize. Typical settling performance is shown in Figure 11 following. The AD780 settles to within 0.1% of its final value within 10 μs.

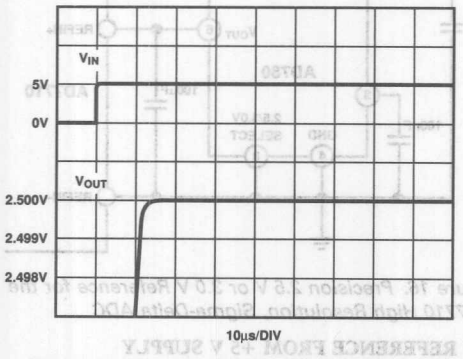


Figure 11. Turn-On Settling Time Performance

DYNAMIC PERFORMANCE

The output stage of the AD780 has been designed to provide superior static and dynamic load regulation.

Figure 12 shows the performance of the AD780 while driving a 0 mA to 10 mA load.

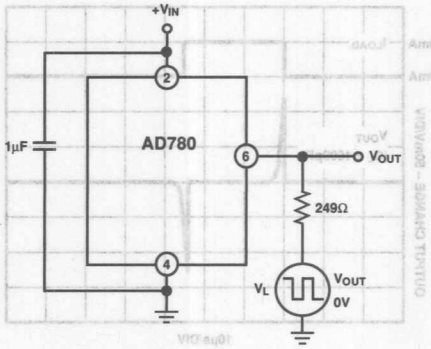


Figure 12a. Transient Resistive Load Test Circuit

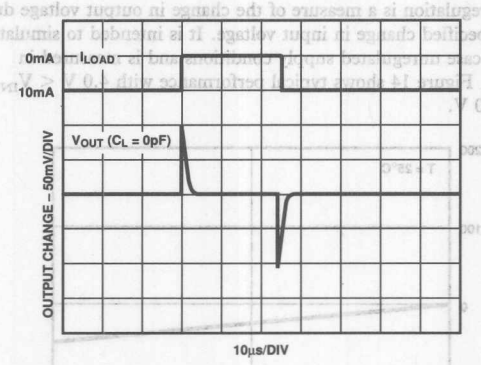


Figure 12b. Settling Under Transient Resistive Load

The dynamic load may be resistive and capacitive. For example the load may be connected via a long capacitive cable. Figure 13 following shows the performance of the AD780 driving a 1000 pF, 0 mA to 10 mA load.

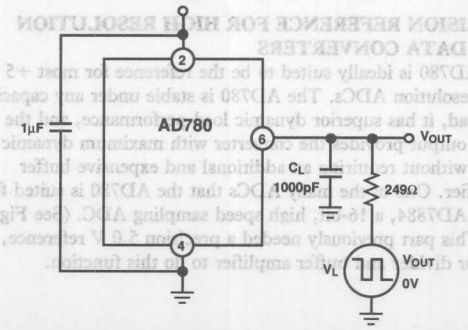


Figure 13a. Capacitive Load Transient Response Test Circuit

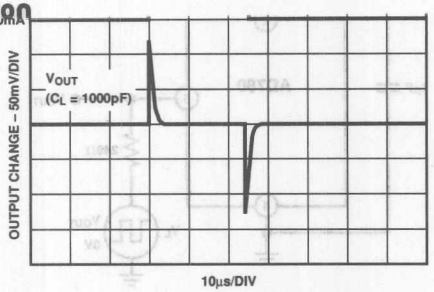


Figure 13b. Settling Under Dynamic Capacitive Load

LINE REGULATION

Line regulation is a measure of the change in output voltage due to a specified change in input voltage. It is intended to simulate worst case unregulated supply conditions and is measured in µV/V. Figure 14 shows typical performance with 4.0 V < V_{IN} < 15.0 V.

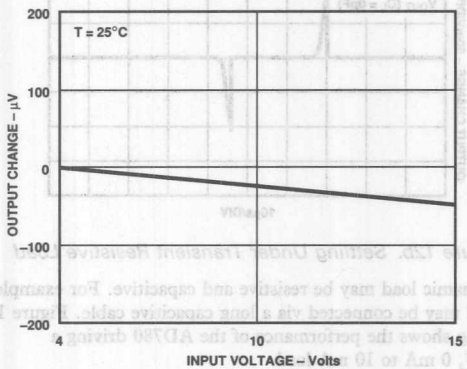


Figure 14. Output Voltage Change vs. Input Voltage

PRECISION REFERENCE FOR HIGH RESOLUTION +5 V DATA CONVERTERS

The AD780 is ideally suited to be the reference for most +5 V high resolution ADCs. The AD780 is stable under any capacitive load, it has superior dynamic load performance, and the 3.0 V output provides the converter with maximum dynamic range without requiring an additional and expensive buffer amplifier. One of the many ADCs that the AD780 is suited for is the AD7884, a 16-bit, high speed sampling ADC. (See Figure 15.) This part previously needed a precision 5.0 V reference, resistor divider and buffer amplifier to do this function.

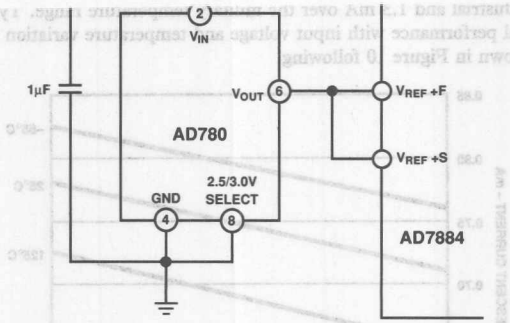


Figure 15. Precision 3.0 V Reference for the AD7884 16-Bit, High Speed ADC

The AD780 is also ideal for use with higher resolution converters such as the AD7710/AD7711/AD7712. (See Figure 16.) While these parts are specified with a 2.5 V internal reference, the AD780 in 3 V mode can be used to improve the absolute accuracy, temperature stability and dynamic range. It is shown following with the two optional noise reduction capacitors.

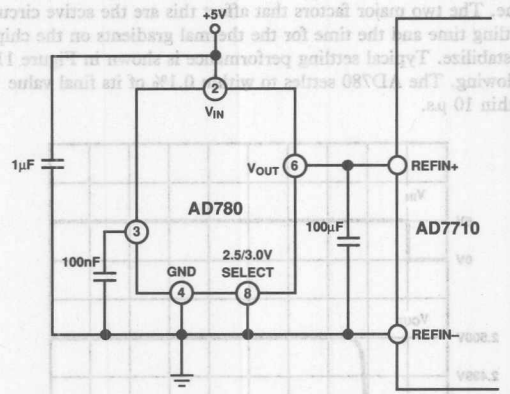


Figure 16. Precision 2.5 V or 3.0 V Reference for the AD7710 High Resolution, Sigma-Delta ADC

+4.5 V REFERENCE FROM +5 V SUPPLY

Some +5 V high resolution ADCs can accommodate reference voltages up to +4.5 V. The AD780 can be used to provide a precision +4.5 V reference voltage from a +5 V supply using the circuit shown following in Figure 17. This circuit will provide a regulated +4.5 V output from a supply voltage as low as +4.7 V. The high quality tantalum 10 µF capacitor in parallel with the ceramic 0.1 µF capacitor and the 3.9 Ω resistor ensure a low output impedance up to around 50 MHz.

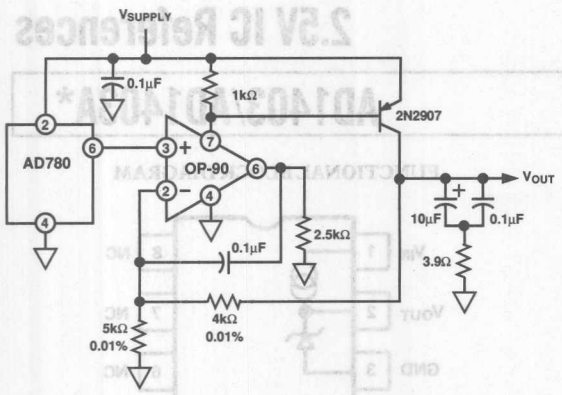


Figure 17. +4.5 V Reference from a Single +5 V Supply

NEGATIVE (−2.5 V OR −3.0 V) REFERENCE

The AD780 can produce a negative output voltage in shunt mode, simply by connecting the input and output to ground and connecting the AD780's GND pin to a negative supply via a bias resistor as shown in Figure 18.

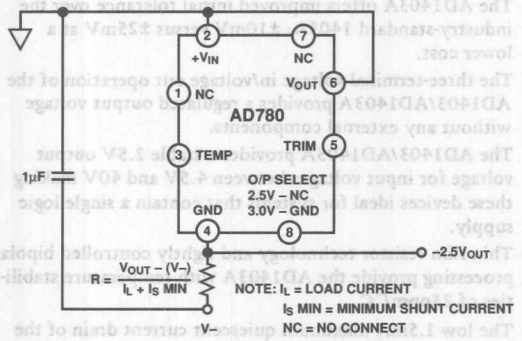


Figure 18. Negative (−2.5 V) Shunt Mode Reference

A precise −2.5 V (or −3.0 V) reference capable of supplying up to 100 mA to a load can be implemented with the AD780 in series mode using the bootstrap circuit following.

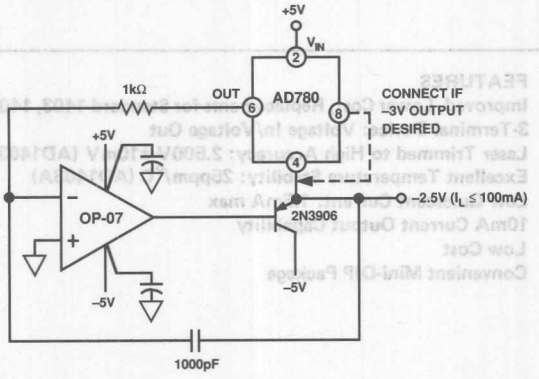


Figure 19. −2.5 V High Load Current Reference

8

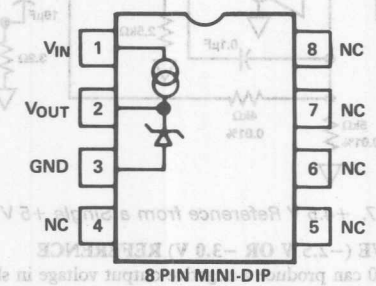
Low Cost, Precision 2.5V IC References

AD1403/AD1403A*

FEATURES

Improved, Lower Cost, Replacements for Standard 1403, 1403A
3-Terminal Device: Voltage In/Voltage Out
Laser Trimmed to High Accuracy: 2.500V ±10mV (AD1403A)
Excellent Temperature Stability: 25ppm/°C (AD1403A)
Low Quiescent Current: 1.5mA max
10mA Current Output Capability
Low Cost
Convenient Mini-DIP Package

FUNCTIONAL BLOCK DIAGRAM



8 PIN MINI-DIP

PRODUCT DESCRIPTION

The AD1403 and AD1403A are improved three-terminal, low cost, temperature compensated, bandgap voltage references that provide a fixed 2.5V output voltage for inputs between 4.5V and 40V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provides the AD1403/AD1403A with an initial tolerance of ±10mV and a temperature stability of better than 25ppm/°C. In addition, the low quiescent current drain of 1.5mA (max) offers a clear advantage over classical Zener techniques.

The AD1403 or AD1403A is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD1403/AD1403A allows operation with 5 volt logic supplies, making these devices ideal for digital panel meter applications and when only a single logic supply is available.

The AD1403 and AD1403A are specified for operation over the 0 to +70°C temperature range. The AD580 series of 2.5 volt precision IC references is recommended for applications where operation over the −55°C to +125°C range is required.

PRODUCT HIGHLIGHTS

1. The AD1403A offers improved initial tolerance over the industry-standard 1403A: ±10mV versus ±25mV at a lower cost.
2. The three-terminal voltage in/voltage out operation of the AD1403/AD1403A provides a regulated output voltage without any external components.
3. The AD1403/AD1403A provides a stable 2.5V output voltage for input voltages between 4.5V and 40V making these devices ideal for systems that contain a single logic supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD1403A with temperature stabilities of 25ppm/°C.
5. The low 1.5mA maximum quiescent current drain of the AD1403 and AD1403A makes them ideal for CMOS and other low power applications.

*Protected by U.S. Patent Numbers: 3,887,863, RE30,586.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (V_{IN} = 15V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0mA)	V_O				
AD1403		2.475	2.500	2.525	V
AD1403A		2.490	2.500	2.510	
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
AD1403		–	10	40	
AD1403A		–	10	25	
Output Voltage Change, 0 to +70°C	ΔV_O				mV
AD1403		–	–	7.0	
AD1403A		–	–	4.4	
Line Regulation	Reg_{in}				mV
(15V≤V_{IN}≤40V)		–	1.2	4.5	
(4.5≤V_{IN}≤15V)		–	0.6	3.0	
Load Regulation (0mA<I_O<10mA)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0mA)	I_I	–	1.2	1.5	mA

Specifications subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	40	V
Storage Temperature	T_{STG}	–25 to 100	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C

ORDERING GUIDE

Model	Initial Tolerance	Package Option*
AD1403	±25mV	N-8
AD1403A	±10mV	N-8

*N = Plastic DIP. For outline information see Package Information section.

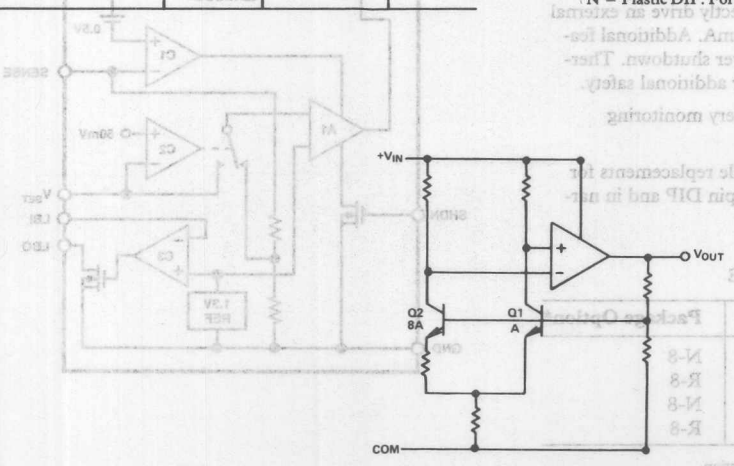


Figure 1. Simplified AD1403 Schematic

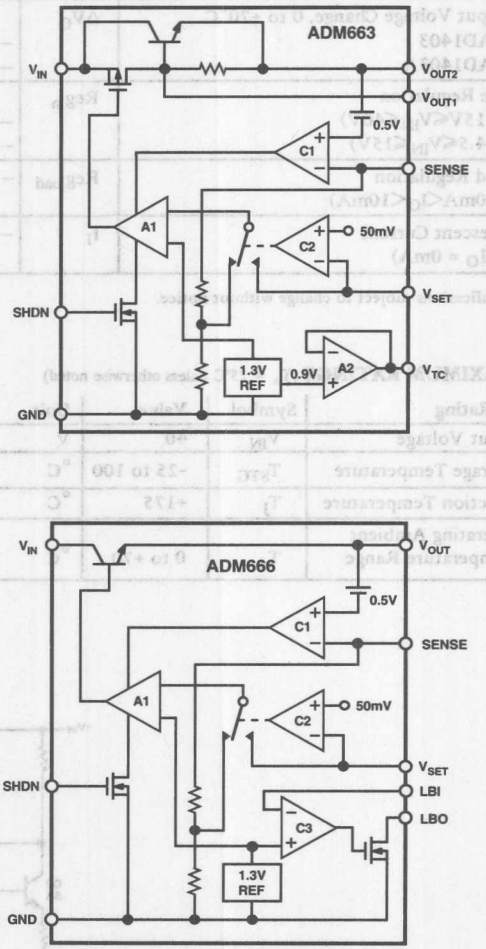
FEATURES

5 V Fixed or +1.3 V to +16 V Adjustable
Low Power CMOS: 12 μA max Quiescent Current
40 mA Output Current
Current Limiting
Pin Compatible with MAX663/666
+2 V to +16.5 V Operating Range
Low Battery Detector ADM666
No Overshoot on Power-Up

APPLICATIONS

Handheld Instruments
LCD Display Systems
Pagers
Remote Data Acquisition

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADM663/ADM666 are precision voltage regulators featuring a maximum quiescent current of 12 μA. They can be used to give a fixed +5 V output with no additional external components or can be adjusted from 1.3 V to 16 V using two external resistors. Fixed or adjustable operation is automatically selected via the V_{SET} input. The low quiescent current makes these devices especially suitable for battery powered systems. The input voltage range is 2 V to 16.5 V and an output current up to 40 mA is provided. The ADM663 can directly drive an external pass transistor for currents in excess of 40 mA. Additional features include current limiting and low power shutdown. Thermal shutdown circuitry is also included for additional safety.

The ADM666 features additional low battery monitoring circuitry to detect for low battery voltages.

The ADM663/ADM666 are pin-compatible replacements for the MAX663/666. Both are available in 8-pin DIP and in narrow surface mount (SOIC) packages.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM663AN	–40°C to +85°C	N-8
ADM663AR	–40°C to +85°C	R-8
ADM666AN	–40°C to +85°C	N-8
ADM666AR	–40°C to +85°C	R-8

*For outline information see Package Information section.

SPECIFICATIONS (V_{IN} = +9 V, V_{OUT} = + 5 V, T_A = + 25°C unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Input Voltage, V_{IN}	2.0		16.5	V	$T_A = T_{MIN}$ to T_{MAX}
Quiescent Current, I_Q					No Load, V_{IN} = +16.5 V
		6	12	µA	T_A = +25°C
			15	µA	$T_A = T_{MIN}$ to T_{MAX}
Output Voltage, V_{OUT}	4.75	5.0	5.25	V	$T_A = T_{MIN}$ to T_{MAX}, V_{SET} = GND
Line Regulation, $\Delta V_{OUT}/\Delta V_{IN}$		0.03	0.35	%/V	+2 V ≤ V_{IN} ≤ +15 V, $V_{OUT} = V_{REF}$
Load Regulation, $\Delta V_{OUT}/\Delta I_{OUT}$		3.0	7.0	Ω	ADM663, 1 mA ≤ I_{OUT2} ≤ 20 mA
		1.0	5.0	Ω	ADM663, 50 µA ≤ I_{OUT1} ≤ 5 mA
		3.0	7.0	Ω	ADM666, 1 mA ≤ I_{OUT} ≤ 20 mA
Reference Voltage, V_{SET}	1.27		1.33	V	$V_{OUT} = V_{SET}$
Reference Tempco, $\Delta V_{SET}/\Delta T$		±100		ppm/°C	$T_A = T_{MIN}$ to T_{MAX}
V_{SET} Internal Threshold, $V_{F/A}$		50		mV	$V_{SET} < V_{F/A}$ for +5 V Out;
					$V_{SET} > V_{F/A}$ for Adj. Out
V_{SET} Input Current, I_{SET}		±0.01	±10	nA	$T_A = T_{MIN}$ to T_{MAX}
Shutdown Input Voltage, V_{SHDN}	1.4			V	V_{SHDN} High = Output Off
			0.3	V	V_{SHDN} Low = Output On
Shutdown Input Current, I_{SHDN}		±0.01	±10	nA	
SENSE Input Threshold, V_{OUT}–V_{SENSE}		0.5		V	Current Limit Threshold
SENSE Input Resistance, R_{SENSE}		3		MΩ	
Input-Output Saturation Resistance, R_{SAT}					
ADM663 V_{OUT1}		200	500	Ω	V_{IN} = +2 V, I_{OUT} = 1 mA
		70	150	Ω	V_{IN} = +9 V, I_{OUT} = 2 mA
		50	150	Ω	V_{IN} = +15 V, I_{OUT} = 5 mA
Output Current from $V_{OUT(2)}$, I_{OUT}	40			mA	+3 V ≤ V_{IN} ≤ +16.5 V, V_{IN}–V_{OUT} = +1.5 V
Minimum Load Current, $I_{L(MIN)}$			1.0	µA	T_A = +25°C
			5.0	µA	$T_A = T_{MIN}$ to T_{MAX}
LBI Input Threshold, V_{LBI}	1.21	1.28	1.37	V	ADM666
LBI Input Current, I_{LBI}		±0.01	±10	nA	ADM666
LBO Output Saturation Resistance, R_{SAT}		35	100	Ω	ADM666, I_{SAT} = 2 mA
LBO Output Leakage Current		10		nA	ADM666, LBI = 1.4 V
V_{TC} Open Circuit Voltage, V_{TC}		0.9		V	ADM663
V_{TC} Sink Current, I_{TC}	2.0	8.0		mA	ADM663
V_{TC} Temperature Coefficient		+2.5		mV/°C	ADM663

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A= +25°C unless otherwise noted)

Input Voltage, V_{IN} ..... +18 V

Terminal Voltage

(ADM663) Pins 1, 3, 5, 6, 7 ..... (GND – 0.3 V) to (V_{IN} + 0.3 V)

(ADM666) Pins 1, 2, 3, 5, 6 ..... (GND – 0.3 V) to (V_{IN} + 0.3 V)

(ADM663) Pin 2 ..... (GND – 0.3 V) to (V_{OUT1} + 0.3 V)

(ADM666) Pin 7 ..... (GND – 0.3 V) to +16.5 V

Output Source Current

(ADM663, ADM666) Pin 2 ..... 50 mA

(ADM663) Pin 3 ..... 25 mA

Output Sink Current,

(ADM663, ADM666) Pin 7 ..... –20 mA

Power Dissipation, N-8 ..... 625 mW

(Derate 8.3 mW/°C above +50°C)

θ_{JA}, Thermal Impedance ..... 120°C/W

Power Dissipation R-8 ..... 450 mW

(Derate 6 mW/°C above +50°C)

θ_{JA}, Thermal Impedance ..... 170°C/W

Operating Temperature Range

Industrial (A Version) ..... –40°C to +85°C

Storage Temperature Range ..... –65°C to +150°C

Lead Temperature (Soldering, 10 sec) ..... +300°C

Vapor Phase (60 sec) ..... +215°C

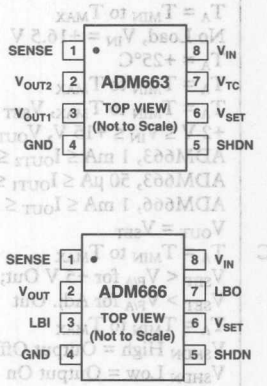
Infrared (15 sec) ..... +220°C

ESD Rating ..... >5000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

8

DIP & SOIC PIN CONFIGURATIONS



PIN FUNCTION DESCRIPTION

Mnemonic	Function
$V_{OUT(1)\ (2)}$	Voltage Regulator Output(s)
V_{IN}	Voltage Regulator Input
SENSE	Current Limit Sense Input. (Referenced to $V_{OUT(2)}$.) If not used it should be connected to $V_{OUT(2)}$
GND	Ground Pin. Must be connected to 0 V
LBI	Low Battery Detect Input. Compared with 1.3 V
LBO	Low Battery Detect Output. Open Drain Output
SHDN	Digital Input. May be used to disable the device so that the power consumption is minimized
V_{SET}	Voltage Setting Input. Connect to GND for +5 V output or connect to resistive divider for adjust able output
V_{TC}	Temperature-Proportional Voltage for negative TC Output

GENERAL INFORMATION

The ADM663/ADM666 contains a micropower bandgap reference voltage source, an error amplifier A1, two comparators C1, C2 and a series pass output transistor. A P-channel FET and an NPN transistor are used on the ADM663 while the ADM666 uses an NPN output transistor.

CIRCUIT DESCRIPTION

The internal bandgap reference is trimmed to 1.3 V ± 30 mV. This is used as a reference input to the error amplifier A1. The feedback signal from the regulator output is supplied to the other input by an on-chip voltage divider or by two external resistors. When V_{SET} is at ground, the internal divider provides the error amplifier's feedback signal giving a +5 V output. When V_{SET} is at more than 50 mV above ground, the error amplifier's input is switched directly to the V_{SET} pin, and external resistors are used to set the output voltage. The external resistors are selected so that the desired output voltage gives 1.3 V at V_{SET}.

Comparator C1 monitors the output current via the SENSE input. This input, referenced to $V_{OUT(2)}$, monitors the voltage drop across a load sense resistor. If the voltage drop exceeds 0.5 V, then the error amplifier A_1 is disabled and the output current is limited.

The ADM663 has an additional amplifier, A2, which provides a temperature-proportional output, V_{TC}. If this is summed into the inverting input of the error amplifier, a negative temperature coefficient results at the output. This is useful when powering liquid crystal displays over wide temperature ranges.

The ADM666 has an additional comparator, C3 which compares the voltage on the Low Battery Input, LBI, pin to the internal +1.3 V reference. The output from the comparator drives an open drain FET connected to the Low Battery Output pin, LBO. The Low Battery Threshold may be set using a suitable voltage divider connected to LBI. When the voltage on LBI falls below 1.3 V, the open drain output LBO is pulled low.

Both the ADM663 and the ADM666 contain a shutdown (SHDN) input which can be used to disable the error amplifier and hence the voltage output. The quiescent current in shutdown is less than 12 µA.

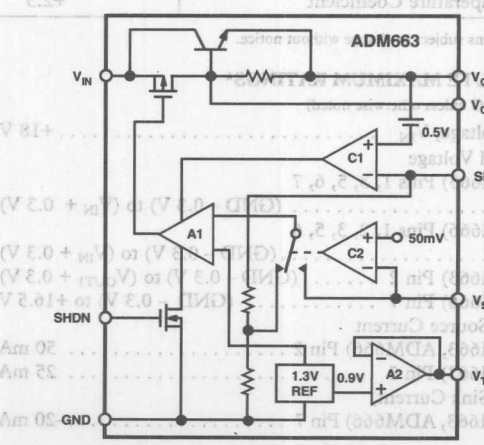


Figure 1. ADM663 Functional Block Diagram

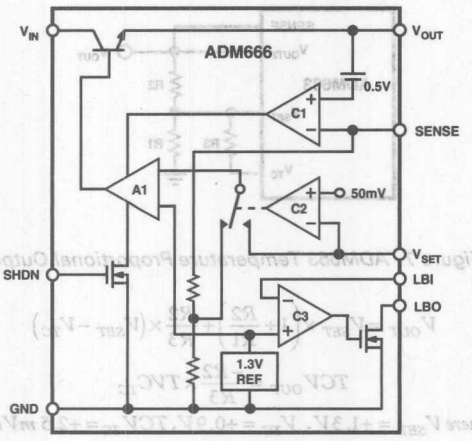


Figure 2. ADM666 Functional Block Diagram

Circuit Configurations

For a fixed +5 V output the V_{SET} input is grounded and no external resistors are necessary. This basic configuration is shown in Figure 3. Current limiting is not being utilized so the SENSE input is connected to $V_{OUT(2)}$. The input voltage can range from +6 V to +16 V and output currents up to 40 mA are available provided that the maximum package power dissipation is not exceeded.

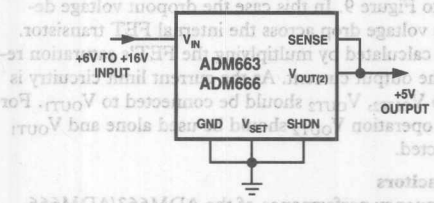


Figure 3. ADM663/ADM666 Fixed +5 V Output

Output Voltage Setting

If V_{SET} is not connected to GND, the output voltage is set according to the following equation.

$$V_{OUT} = V_{SET} \times \frac{R1 + R2}{R1} \text{ where } V_{SET} = 1.30\,V$$

The resistor values may be selected by firstly choosing a value for R1 and then selecting R2 according to the following equation.

$$R2 = R1 \times \left(\frac{V_{OUT}}{1.30} - 1 \right)$$

The input leakage current on V_{SET} is 10 nA maximum. This allows large resistor values to be chosen for R1 and R2 with little degradation in accuracy. For example, a 1 MΩ resistor may be selected for R1 and then R2 may be calculated accordingly. The tolerance on V_{SET} is guaranteed at less than ±30 mV so in most applications, fixed resistors will be suitable.

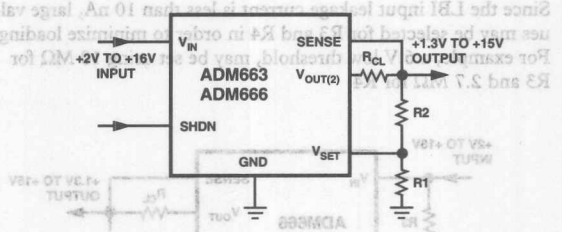


Figure 4. ADM663/ADM666 Adjustable Output

Current Limiting

Current limiting may be achieved by using an external current sense resistor in series with $V_{OUT(2)}$. When the voltage across the sense resistor exceeds the internal 0.5 V threshold, current limiting is activated. The sense resistor is therefore chosen such that the voltage across it will be 0.5 V when the desired current limit is reached.

$$R_{CL} = \frac{0.5}{I_{CL}}$$

where R_{CL} is the current sense resistor, I_{CL} is the maximum current limit.

The value chosen for R_{CL} should also ensure that the current is limited to less than the 50 mA absolute maximum rating and also that the power dissipation will also be within the package maximum ratings.

If current limiting is employed, there will be an additional voltage drop across the sense resistor which must be considered when determining the regulators dropout voltage.

If current limiting is not used, the SENSE input should be connected to $V_{OUT(2)}$.

Shutdown Input (SHDN)

The SHDN input allows the regulator to be switched off with a logic level signal. This will disable the output and reduce the current drain to a low quiescent (12 µA maximum) current. This is very useful for low power applications. The SHDN input should be driven with a CMOS logic level signal since the input threshold is 0.3 V. In TTL systems, an open collector driver with a pull-up resistor may be used.

If the shutdown function is not being used, then SHDN should be connected to GND.

Low Supply or Low Battery Detection

The ADM666 contains on-chip circuitry for low power supply or battery detection. If the voltage on the LBI pin falls below the internal 1.3 V reference, then the open drain output LBO will go low. The low threshold voltage may be set to any voltage above 1.3 V by appropriate resistor divider selection.

$$R3 = R4 \times \left(\frac{V_{BATT}}{1.30} - 1 \right)$$

where R3 and R4 are the resistive divider resistors and V_{BATT} is the desired low voltage threshold.

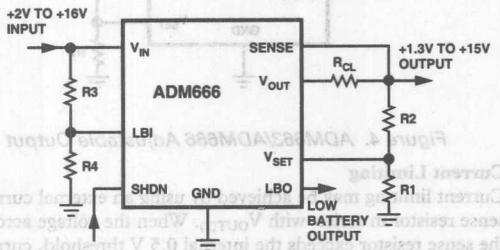


Figure 5. ADM666 Adjustable Output with Low Battery Detection

High Current Operation

The ADM663 contains an additional output, V_{OUT1}, suitable for directly driving the base of an external NPN transistor. Figure 6 shows a configuration which can be used to provide +5 V with boosted current drive. A 1 Ω current sensing resistor limits the current at 0.5 A.

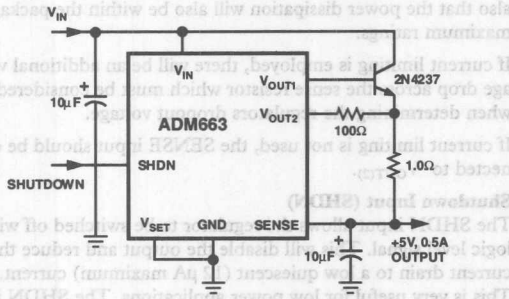


Figure 6. ADM663 Boosted Output Current (0.5 A)

Temperature Proportional Output

The ADM663 contains a V_{TC} output with a positive temperature coefficient of +2.5 mV/°C. This may be connected to the summing junction of the error amplifier (V_{SET}) through a resistor resulting in a negative temperature coefficient at the output of the regulator.

This is especially useful in multiplexed LCD displays to compensate for the inherent negative temperature coefficient of the LCD threshold. At 25°C the voltage at the VTC output is typically 0.9 V. The equations for setting both the output voltage and the tempco are given below. If this function is not being used, then V_{TC} should be left unconnected.

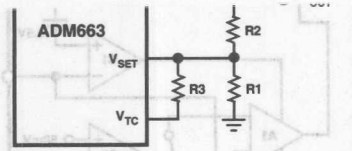


Figure 7. ADM663 Temperature Proportional Output

$$V_{OUT} = V_{SET} \times \left(1 + \frac{R2}{R1}\right) + \frac{R2}{R3} \times \left(V_{SET} - V_{TC}\right)$$

$$TCV_{OUT} = \frac{-R2}{R3} \times TVC_{TC}$$

where $V_{SET} = +1.3\,V$, $V_{TC} = +0.9\,V$, $TCV_{TC} = +2.5\,mV/°C$

APPLICATION HINTS

Input-Output (Dropout Voltage)

A regulator's minimum input-output differential or dropout voltage determines the lowest input voltage for a particular output voltage. The ADM663/ADM666 dropout voltage is 0.8 V at its rated output current. For example when used as a fixed +5 V regulator the minimum input voltage is +5.8 V. At lower output currents, (I_{OUT} < 5 mA), on the ADM663, V_{OUT1} may be used as the output driver in order to achieve lower dropout voltages. Please refer to Figure 9. In this case the dropout voltage depends on the voltage drop across the internal FET transistor. This may be calculated by multiplying the FET's saturation resistance by the output current. As the current limit circuitry is referenced to V_{OUT2}, V_{OUT2} should be connected to V_{OUT1}. For high current operation V_{OUT2} should be used alone and V_{OUT1} left unconnected.

Bypass Capacitors

The high frequency performance of the ADM663/ADM666 may be improved by decoupling the output using a filter capacitor. A capacitor value of 10 µF is suitable.

An input capacitor helps reduce noise and improves dynamic performance. A suitable input capacitor of 0.1 µF or greater may be used.

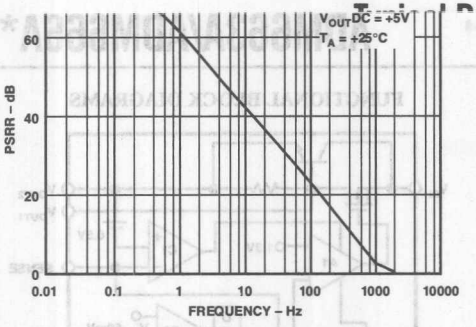


Figure 8. Power Supply Rejection Ratio vs. Frequency

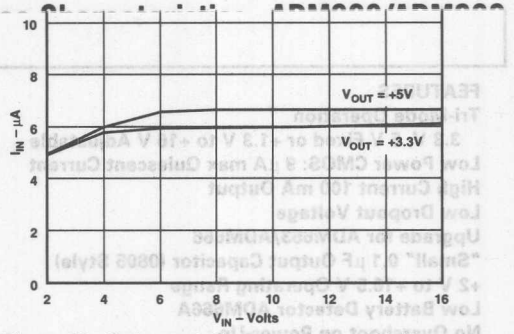


Figure 10. Quiescent Current vs. Input Voltage

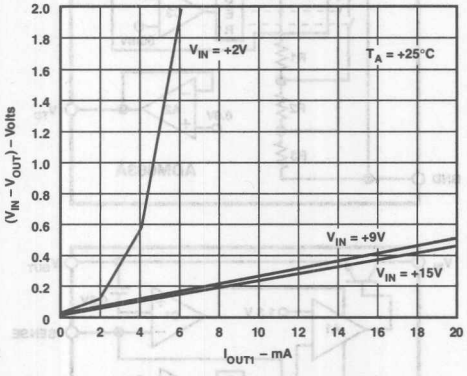


Figure 9. V_{OUT1} Input-Output Differential vs. Output Current

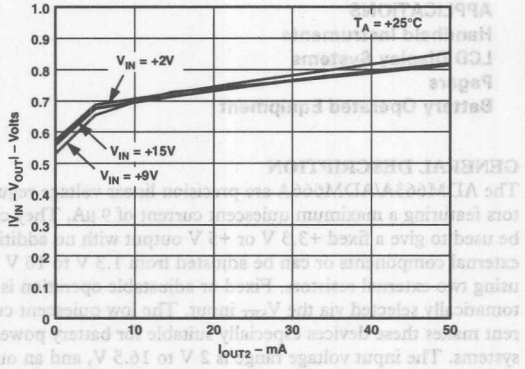


Figure 11. $V_{OUT(2)}$ Input-Output Differential vs. Output Current

8

Tri-Mode: +3.3 V, +5 V, Adjustable Micropower Linear Voltage Regulators

ADM663A/ADM666A*

FEATURES

Tri-Mode Operation
3.3 V, 5 V Fixed or +1.3 V to +16 V Adjustable
Low Power CMOS: 9 µA max Quiescent Current
High Current 100 mA Output
Low Dropout Voltage
Upgrade for ADM663/ADM666
"Small" 0.1 µF Output Capacitor (0805 Style)
+2 V to +16.5 V Operating Range
Low Battery Detector ADM666A
No Overshoot on Power-Up
Thermal Shutdown

APPLICATIONS

Handheld Instruments
LCD Display Systems
Pagers
Battery Operated Equipment

GENERAL DESCRIPTION

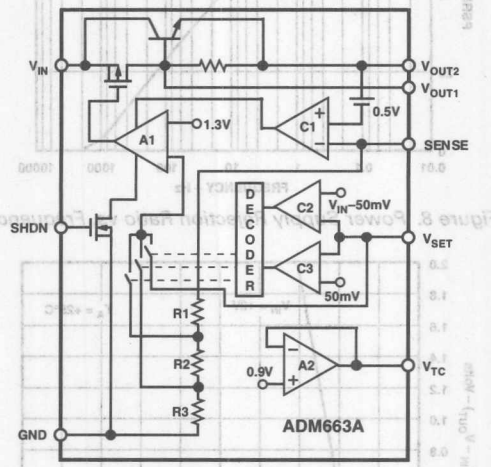
The ADM663A/ADM666A are precision linear voltage regulators featuring a maximum quiescent current of 9 µA. They can be used to give a fixed +3.3 V or +5 V output with no additional external components or can be adjusted from 1.3 V to 16 V using two external resistors. Fixed or adjustable operation is automatically selected via the V_{SET} input. The low quiescent current makes these devices especially suitable for battery powered systems. The input voltage range is 2 V to 16.5 V, and an output current up to 100 mA is provided. Current limiting may be set using a single external resistor. For additional safety, an internal thermal shutdown circuit monitors the internal die temperature.

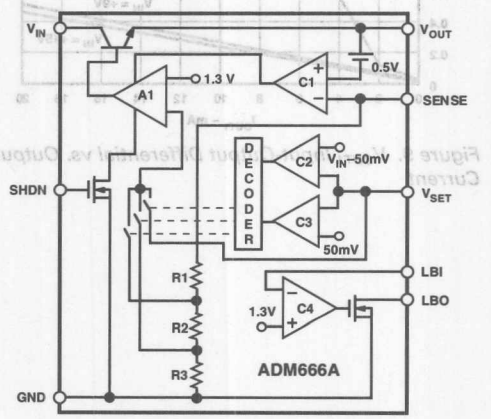
The ADM666A features additional low battery monitoring circuitry to detect for low battery voltages.

The ADM663A/ADM666A are pin compatible enhancements for the ADM663/ADM666. Improvements include an additional 3.3 V output range, higher output current, and operation with a small output capacitor.

The ADM663A/ADM666A are available in an 8-pin DIP and narrow surface mount (SOIC) packages.

FUNCTIONAL BLOCK DIAGRAMS





*Patent pending.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (V_{IN} = +9 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Input Voltage, V_{IN}	2.0		16.5	V	
Quiescent Current, I_Q		6	9	µA	No Load, V_{IN} = +16.5 V
Output Voltage, $V_{OUT(2)}$ (+5 V Mode)	4.75	5.0	5.25	V	V_{SET} = GND
Output Voltage, $V_{OUT(2)}$ (+3.3 V Mode)	3.135	3.3	3.465	V	V_{SET} = V_{IN}
Dropout Voltage, V_{DO}		0.75	0.9	V	I_{OUT} = 40 mA, V_{OUT} = +14.5 V
Dropout Voltage, V_{DO}		1.0	1.2	V	I_{OUT} = 100 mA, V_{OUT} = +14.5 V
Line Regulation ($\Delta V_{OUT(2)}/\Delta V_{IN}$)		0.03	0.35	%/V	+2 V ≤ V_{IN} ≤ +15 V, V_{OUT} = V_{REF}
Load Regulation					V_{IN} = (V_{OUT} +3 V), 1 mA ≤ $I_{OUT(2)}$ ≤ 100 mA
$\Delta V_{OUT(2)}$;($\Delta V_{OUT(2)}/\Delta I_{OUT(2)}$)		0.3	1.0	Ω	V_{SET} = GND (Fixed +5 V Output)
		0.15	0.35	Ω	V_{SET} = V_{IN} (Fixed +3.3 V Output)
		0.15	0.30	Ω	V_{SET} = Resistive Divider (Adjustable Output)
ΔV_{OUT1};($\Delta V_{OUT1}/\Delta I_{OUT1}$)		0.25	1.2	Ω	ADM663A, 50 µA ≤ I_{OUT1} ≤ 10 mA
Reference Voltage, V_{SET}	1.27		1.33	V	T_A = +25°C, V_{OUT} = V_{SET}
Reference Tempco ($\Delta V_{SET}/\Delta T$)		±100		ppm/°C	
V_{SET} Internal Threshold					
$V_{F/A}$ Low		50		mV	V_{SET} < $V_{F/A}$ Low for +5 V Output
$V_{F/A}$ High		V_{IN} – 50		mV	V_{SET} > $V_{F/A}$ High for +3.3 V Output
V_{SET} Input Current, I_{SET}		±0.01	±10	nA	
Shutdown Input Voltage, V_{SHDN}	1.4			V	V_{SHDN} High = Output Off
			0.3	V	V_{SHDN} Low = Output On
Shutdown Input Current, I_{SHDN}		±0.01	±10	nA	
SENSE Input Threshold, V_{OUT} – V_{SENSE}		0.5		V	Current Limit Threshold
SENSE Input Resistance, R_{SENSE}		3		MΩ	
Input-Output Saturation Resistance, R_{SAT}					
ADM663A, V_{OUT1}		200	400	Ω	V_{IN} = +2 V, I_{OUT} = 1 mA
		20	40	Ω	V_{IN} = +9 V, I_{OUT} = 10 mA
		20	30	Ω	V_{IN} = +15 V, I_{OUT} = 10 mA
Output Current, $I_{OUT(2)}$	100			mA	+3 V ≤ V_{IN} ≤ +16.5 V, V_{IN} – V_{OUT} = +1.5 V
Minimum Load Current, $I_{L\ (MIN)}$			1.0	µA	
LBI Input Threshold					
Low Going	1.1	1.26		V	ADM666A
High Going		1.29	1.42	V	ADM666A
Hysteresis		30		mV	ADM666A
LBI Input Current, I_{LBI}		±0.01	±10	nA	ADM666A
LBO Output Saturation Resistance, R_{SAT}		20	30	Ω	ADM666A, I_{SAT} = 2 mA
LBO Output Leakage Current		0.2		nA	ADM666A, LBI = 1.4 V
V_{TC} Open Circuit Voltage, V_{TC}		0.9		V	ADM663A
V_{TC} Sink Current, I_{TC}		8.0	2.0	mA	ADM663A
V_{TC} Temperature Coefficient		+2.5		mV/°C	ADM663A

Specifications subject to change without notice.

8

ABSOLUTE MAXIMUM RATINGS*

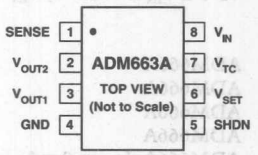
(T_A = +25°C unless otherwise noted)

Input Voltage, V_{IN} ..... +18 V
Terminal Voltage
(ADM663A) Pins 1, 3, 5, 6, 7
..... (GND – 0.3 V) to (V_{IN} + 0.3 V)
(ADM666A) Pins 1, 2, 3, 5, 6
..... (GND – 0.3 V) to (V_{IN} + 0.3 V)
(ADM663A) Pin 2 ..... (GND – 0.3 V) to (V_{OUT1} + 0.3 V)
(ADM666A) Pin 7 ..... (GND – 0.3 V) to +16.5 V
Output Source Current
(ADM663A, ADM666A) Pin 2 ..... 100 mA
(ADM663A) Pin 3 ..... 25 mA
Output Sink Current, Pin 7 .....–20 mA
Power Dissipation, N-8 ..... 800 mW
(Derate 8.3 mW/°C above +30°C)
θ_{JA}, Thermal Impedance ..... 120°C/W
Power Dissipation, R-8 ..... 570 mW
(Derate 6 mW/°C above +30°C)
θ_{JA}, Thermal Impedance ..... 170°C/W
Operating Temperature Range
Industrial (A Version) .....–40°C to +85°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
ESD Rating ..... >5000 V

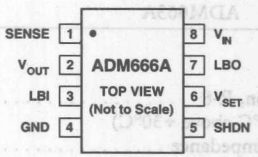
*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

$V_{OUT(1)\ (2)}$	Voltage Regulator Output(s).
V_{IN}	Voltage Regulator Input.
SENSE	Current Limit Sense Input. (Referenced to $V_{OUT(2)}$.) If not used, it should be connected to $V_{OUT(2)}$.
GND	Ground Pin. Must be connected to 0 V.
LBI	Low Battery Detect Input. Compared with 1.3 V.
LBO	Low Battery Detect Output. Open Drain Output.
SHDN	Digital Input. May be used to disable the device so that the power consumption is minimized.
V_{SET}	Voltage Setting Input. Connect to GND for +5 V output, to V_{IN} for +3.3 V output or connect to external resistive divider for adjustable output.
V_{TC}	Temperature-Proportional Voltage for negative TC Output.

PIN CONFIGURATIONS
DIP & SOIC



DIP & SOIC



ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM663AAN	–40°C to +85°C	N-8
ADM663AAR	–40°C to +85°C	R-8
ADM666AAN	–40°C to +85°C	N-8
ADM666AAR	–40°C to +85°C	R-8

*For outline information see Package Information section.

ther reductions in input voltage. It is measured when the output decreases 100 mV from its nominal value. The nominal value is the measured value with $V_{IN} = V_{OUT} + 2$ V.

Line Regulation: The change in output voltage as a result of a change in the input voltage. It is specified as a percentage change in output voltage for an input voltage change.

$$Line\ Reg = \frac{\frac{\Delta V_{OUT}}{V_{OUT}}(100)}{\Delta V_{IN}}$$

Load Regulation: The change in output voltage for a change in output current.

$$Load\ Reg\ (\Omega) = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

Quiescent Current: The input bias current which flows when the regulator output is unloaded or when the regulator is in shutdown.

Sense Input Threshold: Current limit sense voltage. This is the voltage (referenced to $V_{OUT(2)}$) at which current limiting occurs.

Input-Output Saturation Resistance (ADM663A): This is a measure of the internal MOS transistor effective resistance in series with V_{OUT1}. The minimum input-output voltage differential at low currents may be calculated by multiplying the load current by the saturation resistance.

Thermal Limiting: This feature monitors the internal die temperature and disables the output when an internal temperature of 125°C is reached.

Maximum Power Dissipation: The maximum total device dissipation for which the regulator will continue to operate within specifications.

GENERAL INFORMATION

The ADM663A/ADM666A contains a micropower bandgap reference voltage source; an error amplifier, A1; three comparators, C1, C2, C3, and a series pass output transistor. A P-channel FET and an NPN transistor are used on the ADM663A while the ADM666A uses an NPN output transistor.

CIRCUIT DESCRIPTION

The internal bandgap reference is trimmed to 1.3 V ± 30 mV. This is used as a reference input to the error amplifier A1. The feedback signal from the regulator output is supplied to the other input by an on-chip voltage divider or by two external resistors. When V_{SET} is at ground, the internal divider tap between R1 and R2, provides the error amplifier's feedback signal giving a +5 V output. When V_{SET} is at V_{IN}, the internal divider tap between R2 and R3 provides the error amplifier's feedback signal giving a +3.3 V output. When V_{SET} is at more than 50 mV above ground and less than 50 mV below V_{IN}, the error amplifier's input is switched directly to the V_{SET} pin, and external resistors are used to set the output voltage. The external resistors are selected so that the desired output voltage gives 1.3 V at V_{SET}.

Comparator C1 monitors the output current via the SENSE input. This input, referenced to $V_{OUT(2)}$, monitors the voltage drop across a load sense resistor. If the voltage drop exceeds 0.5 V, then the error amplifier A1 is disabled and the output current is limited.

The ADM663A has an additional amplifier, A2, which provides a temperature proportional output, V_{TC}. If this is summed into the inverting input of the error amplifier, a negative temperature coefficient results at the output. This is useful when powering liquid crystal displays over wide temperature ranges.

The ADM666A has an additional comparator, C4, that compares the voltage on the low battery input, LBI, pin to the internal +1.3 V reference. The output from the comparator drives an open drain FET connected to the low battery output pin, LBO. The low battery threshold may be set using a suitable voltage divider connected to LBI. When the voltage on LBI falls below 1.3 V, the open drain output LBO is pulled low.

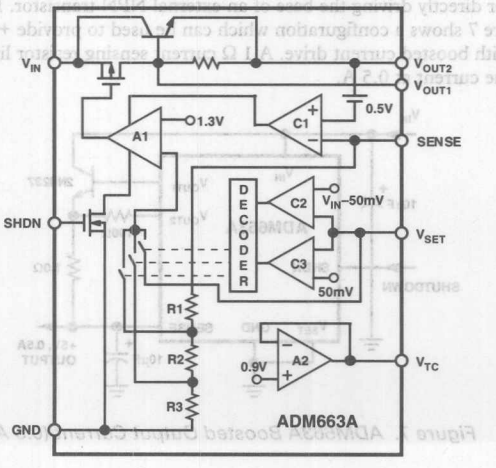


Figure 1. ADM663A Functional Block Diagram

Both the ADM663A and the ADM666A contain a shutdown (SHDN) input that can be used to disable the error amplifier and hence the voltage output. The power consumption in shutdown reduces to less than 9 µA.

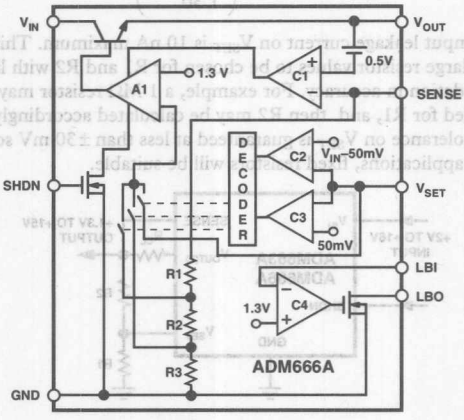


Figure 2. ADM666A Functional Block Diagram

Circuit Configurations

For a fixed +5 V output the V_{SET} input is grounded and no external resistors are necessary. This basic configuration is shown in Figure 3. For a fixed +3.3 V output, the V_{SET} input is connected to V_{IN} as shown in Figure 4. Current limiting is not being utilized so the SENSE input is connected to $V_{OUT(2)}$.

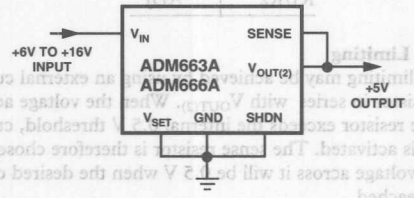


Figure 3. A Fixed +5 V Output

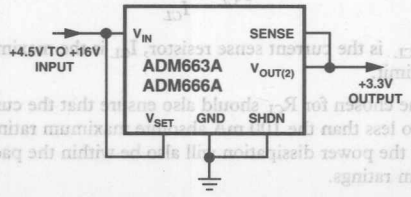


Figure 4. A Fixed +3.3 V Output

Output Voltage Setting

If V_{SET} is not connected to GND or to V_{IN}, the output voltage is set according to the following equation:

$$V_{OUT} = V_{SET} \times \frac{(R1 + R2)}{R1}$$

where V_{SET} = 1.30 V.

The resistor values may be selected by first choosing a value for R1 and then selecting R2 according to the following equation:

$$R2 = R1 \times \left(\frac{V_{OUT}}{1.30} - 1 \right)$$

The input leakage current on V_{SET} is 10 nA maximum. This allows large resistor values to be chosen for R1 and R2 with little degradation in accuracy. For example, a 1 MΩ resistor may be selected for R1, and then R2 may be calculated accordingly. The tolerance on V_{SET} is guaranteed at less than ±30 mV so in most applications, fixed resistors will be suitable.

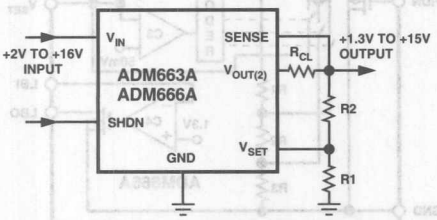


Figure 5. Adjustable Output

Table I. Output Voltage Selection

V_{SET}	V_{OUT}
GND	+5 V
V_{IN}	+3 V
R1/R2	ADJ

Current Limiting

Current limiting may be achieved by using an external current sense resistor in series with $V_{OUT(2)}$. When the voltage across the sense resistor exceeds the internal 0.5 V threshold, current limiting is activated. The sense resistor is therefore chosen such that the voltage across it will be 0.5 V when the desired current limit is reached.

$$R_{CL} = \frac{0.5}{I_{CL}}$$

where R_{CL} is the current sense resistor, I_{CL} is the maximum current limit.

The value chosen for R_{CL} should also ensure that the current is limited to less than the 100 mA absolute maximum rating and also that the power dissipation will also be within the package maximum ratings.

If current limiting is employed, there will be an additional voltage drop across the sense resistor that must be considered when determining the regulators dropout voltage.

If current limiting is not used, the SENSE input should be connected to $V_{OUT(2)}$.

Shutdown Input (SHDN)

The SHDN input allows the regulator to be turned off with a logic level signal. This will disable the output and reduce the current drain to a low quiescent (9 µA maximum) current. This is very useful for low power applications. The SHDN input should be driven with a CMOS logic level signal since the input threshold is 0.3 V. In TTL systems, an open collector driver with a pull-up resistor may be used.

If the shutdown function is not being used, then it should be connected to GND.

Low Supply or Low Battery Detection

The ADM666A contains on-chip circuitry for low power supply or battery detection. If the voltage on the LBI pin falls below the internal 1.3 V reference, then the open drain output LBO will go low. The low threshold voltage may be set to any voltage above 1.3 V by appropriate resistor divider selection.

$$R3 = R4 \left(\frac{V_{BATT}}{1.3\,V} - 1 \right)$$

where R3 and R4 are the resistive divider resistors and V_{BATT} is the desired low voltage threshold.

Since the LBI input leakage current is less than 10 nA, large values may be selected for R3 and R4 in order to minimize loading. For example, a 6 V low threshold may be set using 10 MΩ for R3 and 2.7 M Ω for R4.

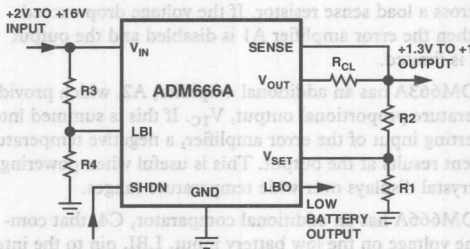


Figure 6. ADM666A Adjustable Output with Low Battery Detection

High Current Operation

The ADM663A contains an additional output, V_{OUT1}, suitable for directly driving the base of an external NPN transistor. Figure 7 shows a configuration which can be used to provide +5 V with boosted current drive. A 1 Ω current sensing resistor limits the current at 0.5 A.

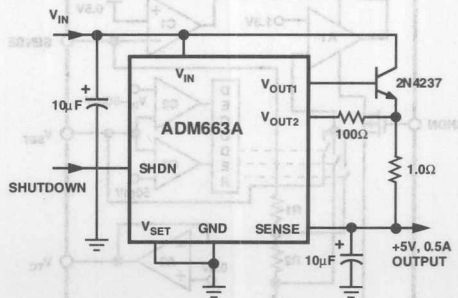


Figure 7. ADM663A Boosted Output Current (0.5 A)

Temperature Proportional Output

The ADM663A contains a V_{TC} output with a positive temperature coefficient of +2.5 mV/°C. This may be connected to the summing junction of the error amplifier (V_{SET}) through a resistor resulting in a negative temperature coefficient at the output of the regulator. This is especially useful in multiplexed LCD displays to compensate for the inherent negative temperature coefficient of the LCD threshold. At +25°C the voltage at the VTC output is typically 0.9 V. The equations for setting both the output voltage and the tempco are given below. If this function is not being used, then V_{TC} should be left unconnected.

$$V_{OUT} = V_{SET}\left(1+\frac{R2}{R1}\right)+\frac{R2}{R3}\left(V_{SET}-V_{TC}\right)$$

$$TCV_{OUT} = \frac{-R2}{R3}\left(TCV_{TC}\right)$$

where V_{SET} = +1.3 V, V_{TC} = +0.9 V, TCV_{TC} = +2.5 mV/°C

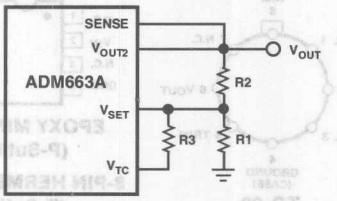


Figure 8. ADM663A Temperature Proportional Output

APPLICATION HINTS

Input-Output (Dropout Voltage)

A regulator's minimum input-output differential or dropout voltage determines the lowest input voltage for a particular output voltage. The ADM663A/ADM666A dropout voltage is 1 V at its rated output current. For example when used as a fixed +5 V regulator, the minimum input voltage is +6 V. At lower output currents (I_{OUT} < 10 mA) on the ADM663A, V_{OUT1} may be used as the output driver in order to achieve lower dropout voltages. In this case the dropout voltage depends on the voltage drop across the internal FET transistor. This may be calculated by multiplying the FET's saturation resistance by the output current, for example with V_{IN} = 9 V, R_{SAT} = 20 Ω. Therefore, the dropout voltage for 5 mA is 100 mV. As the current limit circuitry is referenced to V_{OUT2}, V_{OUT2} should be connected to V_{OUT1}. For high current operation V_{OUT2} should be used alone and V_{OUT1} left unconnected.

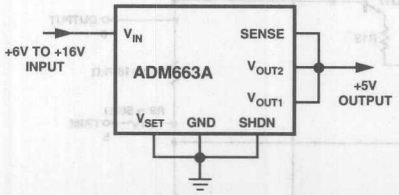


Figure 9. Low Current, Low Dropout Configuration

Thermal Considerations

The ADM663A/ADM666A can supply up to 100 mA load current and can operate with input voltages up to 16.5 V, but the package power dissipation and hence the die temperature must be kept within the maximum limits. The package power dissipation is calculated from the product of the voltage differential across the regulator times the current being supplied to the load. The power dissipation must be kept within the maximum limits given in the Absolute Maximum Ratings section.

$$P_D = (V_{IN}-V_{OUT})(I_L)$$

The die temperature is dependent on both the ambient temperature and on the power being dissipated by the device. The ADM663A/ADM666A contains an internal thermal limiting circuit which will shut down the regulator if the internal die temperature exceeds 125°C. Therefore, care must be taken to ensure that, under normal operating conditions, the die temperature is kept below the thermal limit.

$$T_J = T_A + P_D\,(\theta_{JA})$$

This may be expressed in terms of power dissipation as follows:

$$P_D = (T_J - T_A)/(\theta_{JA})$$

where:

T_J = Die Junction Temperature (°C)

T_A = Ambient Temperature (°C)

P_D = Power Dissipation (W)

θ_{JA} = Junction to Ambient Thermal Resistance (°C/W)

If the device is being operated at the maximum permitted ambient temperature of 85°C the maximum power dissipation permitted is:

$$P_D\,(max) = (T_J\,(max) - T_A)/(\theta_{JA})$$

$$P_D\,(max) = (125 - 85)/(\theta_{JA})$$

$$= 40/\theta_{JA}$$

θ_{JA} = 120°C/W for the 8-pin DIP (N-8) package

θ_{JA} = 170°C/W for the 8-pin SOIC (R-8) package

Therefore, for a maximum ambient temperature of 85°C

$$P_D\,(max) = 333\ mW\ for\ N\text{-}8$$

$$P_D\,(max) = 235\ mW\ for\ R\text{-}8$$

At lower ambient temperatures the maximum permitted power dissipation increases accordingly up to the maximum limits specified in the absolute maximum specifications.

The thermal impedance (θ_{JA}) figures given are measured in still air conditions and are reduced considerably where fan assisted cooling is employed. Other techniques for reducing the thermal impedance include large contact pads on the printed circuit board and wide traces. The copper will act as a heat exchanger thereby reducing the effective thermal impedance.

Bypass Capacitors

The high frequency performance of the ADM663A/ADM666A may be improved by decoupling the ouput using a filter capacitor. A capacitor of 0.1 µF is suitable.

An input capacitor helps reduce noise, improves dynamic performance and reduces the input dV/dt at the regulator input. A suitable input capacitor is 0.1 µF or greater.

+10V Precision Voltage Reference

REF01

FEATURES

- **10 Volt Output** ..... ±0.3% Max
- **Adjustment Range** ..... ±3% Min
- **Excellent Temperature Stability** ..... 8.5ppm/°C Max
- **Low Noise** ..... $30\mu V_{p-p}$ Max
- **Low Supply Current** ..... 1.4mA Max
- **Wide Input Voltage Range** ..... 12V to 40V
- **High Load-Driving Capability** 20mA
- **No External Components**
- **Short-Circuit Proof**
- **MIL-STD-883 Screening Available**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = 25°C ΔV_{OS} MAX (mV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
±30	REF01AJ*	REF01AZ*	—	—	MIL
±30	REF01EJ	REF01EZ	—	—	COM
±50	REF01J*	REF01Z*	—	REF01RC/883	MIL
±50	REF01HJ	REF01HZ	REF01HP	—	COM
±100	REF01CJ	REF01CZ	—	—	COM
±100	—	—	REF01CP	—	XIND
±100	—	—	REF01CS††	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

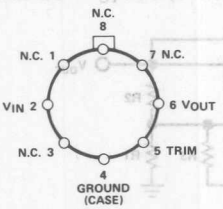
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

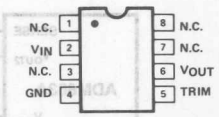
GENERAL DESCRIPTION

The REF-01 precision voltage reference provides a stable +10V output which can be adjusted over a ±3% range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 12V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-01 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. Full military temperature range devices with screening to MIL-STD-883 are available. For guaranteed long-term drift see the REF-10 data sheet.

PIN CONNECTIONS



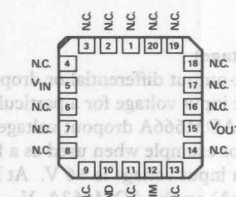
TO-99
(J-Suffix)



EPOXY MINI-DIP
(P-Suffix)

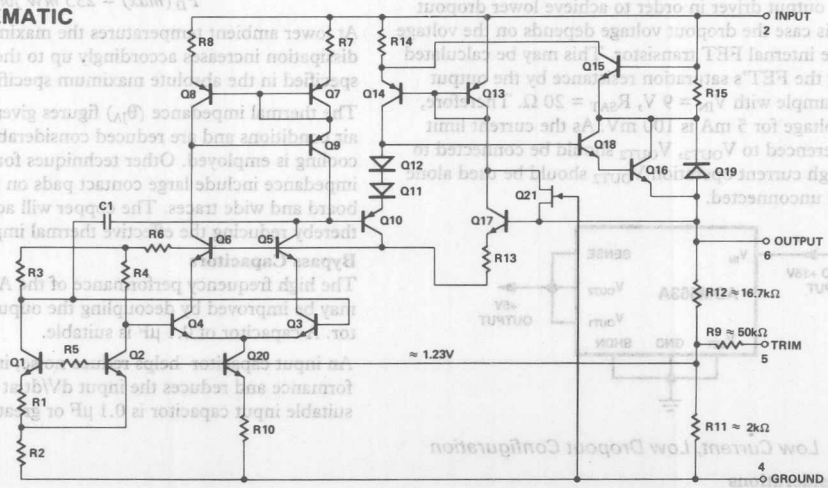
8-PIN HERMETIC DIP
(Z-Suffix)

8-PIN SO
(S-Suffix)



REF-01RC/883
LCC
(RC-Suffix)

SIMPLIFIED SCHEMATIC



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage
- REF-01, A, E, H, RC, All DICE 40V
- REF-01C 30V

Output Short-Circuit Duration
- (to Ground or V_{IN}) ..... Indefinite

Storage Temperature Range
- J, RC, and Z Packages ..... –65° C to +150°C
- P Package ..... –65°C to +125°C

Operating Temperature Range
- REF-01A, REF-01, REF-01RC ..... –55°C to +125°C
- REF-01E, REF-01H,
- REF-01CJ, REF-01CZ ..... 0°C to +70°C
- REF-01CP, REF-01CS ..... –40°C to +85°C

Junction Temperature (T_J) ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	170	24	°C/W
8-Pin Hermetic DIP (Z)	162	26	°C/W
8-Pin Plastic DIP (P)	110	50	°C/W
20-Contact LCC (RC)	120	40	°C/W
8-Pin SO (S)	160	44	°C/W
20-Contact PLCC (PC)	80	39	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, T_A = 25° C, unless otherwise noted.

			REF-01A/E			REF-01/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage	V_O	I_L = 0	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±3.3	—	±3.0	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	20	30	—	20	30	μV_{p-p}
Line Regulation (Note 4)		V_{IN} = 13V to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10mA	—	0.005	0.008	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S	(Note 7)	−0.3	−0.5	—	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, –55°C ≤ T_A ≤ +125°C for REF-01 A/E, and 0°C ≤ T_A ≤ +70°C for REF-01 H and I_L = 0mA, unless otherwise noted.

			REF-01A/E			REF-01/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Ouput Voltage Change with Temperature (Notes 1, 2)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C −55°C ≤ T_A ≤ +125°C	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3.0	8.5	—	10.0	25.0	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 13V to 33V) (Note 4)		0°C ≤ T_A ≤ +70°C −55°C ≤ T_A ≤ +125°C	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 4)		0°C ≤ T_A ≤ +70°C −55°C ≤ T_A ≤ +125°C	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA

NOTES:
1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O\,(0° \text{ to } +70°C) = \frac{\Delta V_{OT}\,(0° \text{ to } +70°C)}{70°C}$$

$$\text{and } TCV_O\,(-55° \text{ to } +125°C) = \frac{\Delta V_{OT}\,(-55° \text{ to } +125°C)}{180°C}$$

4. Line and Load Regulation specifications include the effect of self heating.
5. Guaranteed by design.
6. Sample tested.
7. During sink current test the device meets the output voltage specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_O	I_L = 0mA	9.90	10.00	10.10	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	25	35	μV_{p-p}
Line Regulation (Note 4)		V_{IN} = 13V to 30V	—	0.009	0.015	%/V
Load Regulation (Note 4)		I_L = 0 to 8mA	—	0.006	0.015	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	mA
Load Current	I_L		8	21	—	mA
Sink Current	I_S	(Note 7)	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	mA

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V°C ≤ T_A ≤ +70°C for REF-01CJ, CZ, −40°C ≤ T_A ≤ +85°C for REF-01CP,CS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01C MIN	TYP	MAX	UNITS
Ouput Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	—	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	ppm/%
Line Regulation (Note 4)		V_{IN} = 13V to 30V	—	0.011	0.018	%/V
Load Regulation (Note 4)		I_L = 0 to 5mA	—	0.008	0.018	%/mA

NOTES:

1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

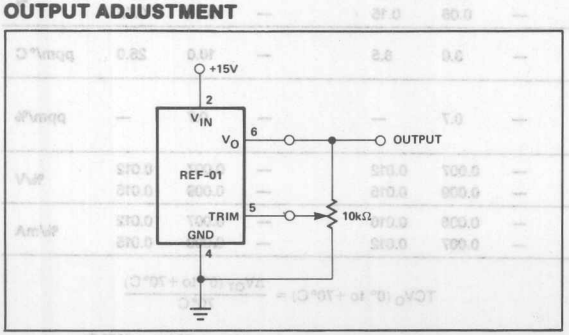
$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

4. Line and Load Regulation specifications include the effect of self heating.
5. Guaranteed by design.
6. Sample tested.
7. During sink current test the device meets the output voltage specified.

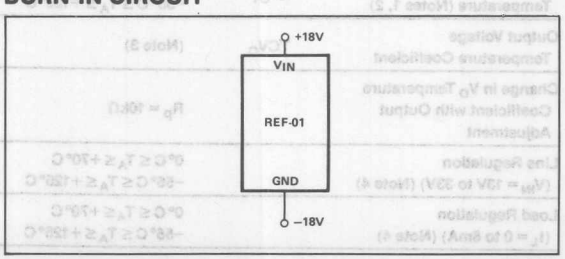
OUTPUT ADJUSTMENT



The REF-01 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V, or to 10.240V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7 ppm/° C for 100mV of output adjustment.

BURN-IN CIRCUIT



+5V Precision Voltage Reference/Temperature Transducer

REF02

FEATURES

- 5 Volt Output ..... ±0.3% Max
- Temperature Voltage Output ..... 2.1mV/°C
- Adjustment Range ..... ±3% Min
- Excellent Temperature Stability ..... 8.5ppm/°C Max
- Low Noise ..... $15\mu V_{p-p}$ Max
- Low Supply Current ..... 1.4mA Max
- Wide Input Voltage Range ..... 7V to 40V
- High Load-Driving Capability 20mA
- No External Components
- Short-Circuit Proof
- MIL-STD-883 Screening Available
- Available in Die Form

GENERAL DESCRIPTION

The REF-02 precision voltage reference provides a stable +5V output which can be adjusted over a ±6% range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 7V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-02 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. The versatility of the REF-02 is enhanced by its use as a monolithic temperature transducer. For +10V references, see the REF-01 and REF-10 data sheets.

ORDERING INFORMATION †

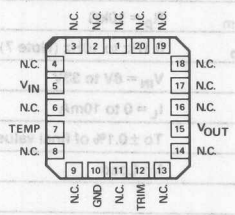
T_A = 25°C	PACKAGE				OPERATING
V_{OS} MAX (mV)	TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	TEMPERATURE RANGE
±15	REF02AJ*	REF02AZ*	–	–	MIL
±15	REF02EJ	REF02EZ	–	–	COM
±25	REF02J*	REF02Z*	–	REF02RC/883	MIL
±25	REF02HJ	REF02HZ	REF02HP	–	COM
±50	REF02CJ	REF02CZ	–	–	COM
±50	–	–	REF02CP	–	XIND
±50	–	–	REF02CS††	–	XIND
±100	REF02DJ	REF02DZ	REF02DP	–	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

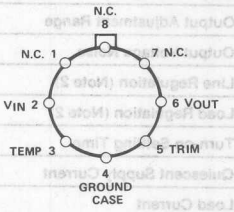
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

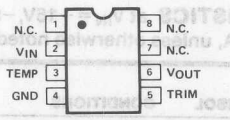
PIN CONNECTIONS



REF-02RC/883
LCC (RC-Suffix)

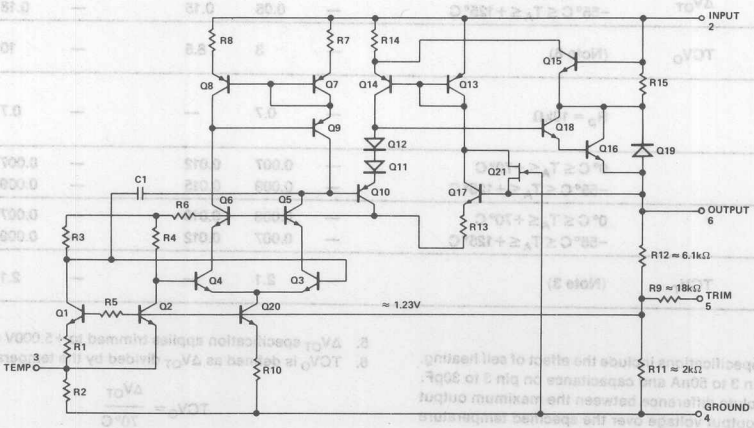


TO-99 (J-Suffix)



8-PIN HERMETIC DIP
(Z-Suffix)
EPOXY MINI-DIP
(P-Suffix)
8-PIN SO
(S-Suffix)

SIMPLIFIED SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage
- REF-02A, E, H, RC, All DICE 40V
- REF-02C, D 30V

Output Short-Circuit Duration
- (to Ground or V_{IN}) ..... Indefinite

Storage Temperature Range
- J, RC, and Z Packages ..... –65°C to +150°C
- P Packages ..... –65°C to +125°C

Operating Temperature Range
- REF-02A, REF-02, REF-02RC ..... –55°C to +125°C
- REF-02E, REF-02H ..... 0°C to +70°C
- REF-02CJ,CZ, REF-02D ..... 0°C to +70°C
- REF-02CP, CS ..... –40°C to +85°C

Lead Temperature (Soldering, 60 sec) ..... 300°C

Junction Temperature (T_J) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	170	24	°C/W
8-Pin Hermetic DIP (Z)	162	26	°C/W
8-Pin Plastic DIP (P)	110	50	°C/W
20-Contact LCC (RC, TC)	120	40	°C/W
8-Pin SO (S)	160	44	°C/W
20-Contact PLCC (PC)	80	39	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02A/E MIN	REF-02A/E TYP	REF-02A/E MAX	REF-02/H MIN	REF-02/H TYP	REF-02/H MAX	UNITS
Output Voltage	V_O	$I_L = 0$	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±3	±6	—	±3	±6	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 7)	—	10	15	—	10	15	μV_{p-p}
Line Regulation (Note 2)		$V_{IN} = 8V$ to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 2)		$I_L = 0$ to 10mA	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S	(Note 8)	−0.3	−0.5	—	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55°C \le T_A \le +125°C$ for REF-02A and REF-02, $0°C \le T_A \le +70°C$ for REF-02E and REF-02H, $I_L = 0mA$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02A/E MIN	REF-02A/E TYP	REF-02A/E MAX	REF-02/H MIN	REF-02/H TYP	REF-02/H MAX	UNITS
Ouput Voltage Change with Temperature (Notes 4, 5)	ΔV_{OT}	$0°C \le T_A \le +70°C$	—	0.02	0.06	—	0.07	0.17	%
		$-55°C \le T_A \le +125°C$	—	0.06	0.15	—	0.18	0.45	
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 8 to 33V) (Note 2)		$0°C \le T_A \le +70°C$	—	0.007	0.012	—	0.007	0.012	%/V
		$-55°C \le T_A \le +125°C$	—	0.009	0.015	—	0.009	0.015	
Load Regulation (I_L = 0 to 8mA) (Note 2)		$0°C \le T_A \le +70°C$	—	0.006	0.010	—	0.007	0.012	%/mA
		$-55°C \le T_A \le +125°C$	—	0.007	0.012	—	0.009	0.015	
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C

NOTES:
1. Guaranteed by design.
2. Line and Load Regulation specifications include the effect of self heating.
3. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
4. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

5. ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
6. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

7. Sample Tested.
8. During sink current test the driver meets the output voltage specified.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25°C$, unless otherwise noted.

			REF-02C			REF-02D			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	V_O	$I_L = 0mA$	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±2.7	±6.0	—	±2.0	±6.0	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 7)	—	12	18	—	12	—	μV_{p-p}
Line Regulation (Note 2)		$V_{IN} = 8V$ to 30V	—	0.009	0.015	—	0.010	0.04	%/V
Load Regulation (Note 2)		$I_L = 0$ to 8mA	—	0.006	0.015	—	—	—	%/mA
		$I_L = 0$ to 4mA	—	—	—	—	0.015	0.04	
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	—	1.0	2.0	mA
Load Current	I_L		8	21	—	8	21	—	mA
Sink Current	I_S	(Note 8)	−0.3	−0.5	—	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$; $I_L = 0mA$, $0°C \le T_A \le +70°C$ for REF-02CJ, CZ, DJ, DZ, DP; $-40°C \le T_A \le +85°C$ for REF-02CP, CS; unless otherwise noted.

			REF-02C			REF-02D			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Ouput Voltage Change with Temperature	ΔV_{OT}	(Notes 4 and 5)	—	0.14	0.45	—	0.49	1.7	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	20	65	—	70	250	ppm/°C
Change in V_O Temperature Coefficient With Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (Note 2)		$V_{IN} = 8V$ to 30V	—	0.011	0.018	—	0.012	0.05	%/V
Load Regulation (Note 2)		$I_L = 0$ to 5mA	—	0.008	0.018	—	0.016	0.05	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C

NOTES:
1. Guaranteed by design.
2. Line and Load Regulation specifications include the effect of self heating.
3. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
4. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

5. ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
6. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

7. Sample Tested.
8. During sink current test the device meets the output voltage specified.

+2.5V Low Power Precision Voltage Reference

REF43

FEATURES

- +2.5 Volt Output ..... ±0.05% Max
- Low Temperature Coefficient ..... 10ppm/°C Max
- Excellent Regulation
  - Load Regulation ..... 20ppm/mA Max
  - Line Regulation ..... 2ppm/V Max
- Supply Current ..... 450μA Max
- Temperature Voltage Output ..... +1.9mV/°C
- Operating Voltage Range ..... +4.5V to +40V
- Extended Industrial Temp Range ..... −40°C to +85°C
- Available in Die Form

ORDERING INFORMATION †

TCV_O	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
10	REF43BJ*	REF43BZ*	–	REF43BRC/883*	MIL
10	REF43FJ	REF43FZ	–	–	XIND
25	REF43GJ	REF43GZ	REF43GP	–	XIND
25	–	–	REF43GS	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

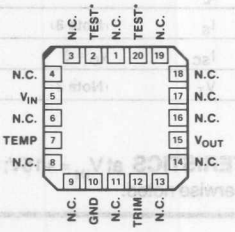
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

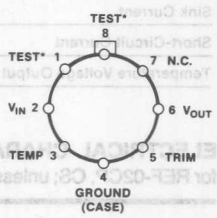
The REF-43 is a low-power precision reference providing a stable +2.5V output independent of variations in supply voltage, load conditions or ambient temperature. It is suitable as a reference level for 8, 10 and 12-bit data acquisition systems, or wherever a stable, known voltage is required.

Tight output tolerances and low thermal drift are assured by zener-zap trimming of both output voltage and its temperature coefficient. A unique curvature correction circuit reduces the thermal curvature which is characteristic of many previous bandgap references.

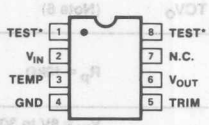
PIN CONNECTIONS



REF-43BRC/883
20-CONTACT LCC
(RC-Suffix)



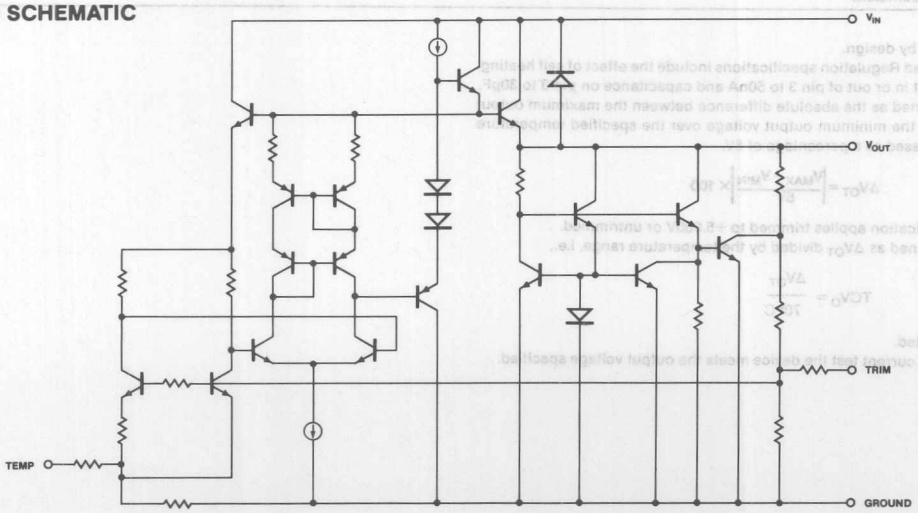
TO-99
(J-Suffix)



8-PIN CERDIP
(Z-Suffix)
8-PIN PLASTIC DIP
(P-Suffix)
8-PIN SO
(S-Suffix)

*RESERVED FOR FACTORY TESTING.
MAKE NO ELECTRICAL CONNECTION TO THESE PINS.

SIMPLIFIED SCHEMATIC



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

The REF-43 may be operated with supply voltages from +4.5V to +40V. The output voltage changes by less than 178μV from one extreme of supply voltage to the other. With only 450μA maximum quiescent current, the REF-43 is ideally suited to applications where power dissipation must be minimized, as in precision battery-powered equipment. The low supply current minimizes drift due to self-heating after power-up.

A temperature output provides a means of determining system ambient temperature. Applications of the REF-43 include A/D and D/A conversion, 4-20mA transmitter/receiver operation, log amplifiers, and power-supply regulators.

For a low-cost 2.5V reference available in small-outline packages consult the REF-03 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 40V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
REF-43B (J, Z) ..... –55°C to +125°C
REF-43F (J, Z) ..... –40°C to +85°C
REF-43G (J, Z, P, S) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +175°C
Junction Temperature Range ..... –65°C to +175°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

8

ELECTRICAL CHARACTERISTICS at V_{IN} = +5V, I_L = 0mA, T_A = 25°C unless otherwise noted.

			REF-43B			REF-43F			REF-43G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage Tolerance		No Load	—	0.04	0.1	—	0.02	0.06	—	0.04	0.1	%
Output Voltage	V_O	No Load	2.4975	2.5000	2.5025	2.4985	2.5000	2.5015	2.4975	2.5000	2.5025	V
Output Voltage Noise	e_{nRMS}	10Hz to 1kHz (Note 1)	—	7	10	—	7	10	—	7	10	μV_{RMS}
Line Regulation		V_{IN} = +4.5V to +40V	—	0.8	2	—	0.8	2	—	0.8	2	ppm/V
Load Regulation		I_L = 0mA to 10mA	—	14	20	—	14	20	—	14	20	ppm/mA
Quiescent Supply Current	I_{SY}	No Load	—	340	450	—	340	450	—	340	450	μA
Load Current (Sourcing)	I_L	(Note 2)	10	20	—	10	20	—	10	20	—	mA
Load Current (Sinking)	I_S	(Note 3)	—	–1.2	—	—	–1.2	—	—	–1.2	—	mA
Short-Circuit Output Current	I_{SC}	Output Shorted to Ground	—	60	—	—	60	—	—	60	—	mA
Temperature Voltage Output	V_{TEMP}		—	567	—	—	567	—	—	567	—	mV
V_{OUT} Adjust Range			—	±95	—	—	±95	—	—	±95	—	mV
Long-Term Output Drift	ΔV_O/Time	(Note 4)	—	1	—	—	1	—	—	1	—	ppm/month

NOTES:
1. Guaranteed but not tested.
2. Guaranteed by load regulation test.
3. Output remains within 2.5V ±2.5mV.
4. Calculated from accelerated life tests at T_A = 150°C. Activation energy = 0.7eV.

REF43

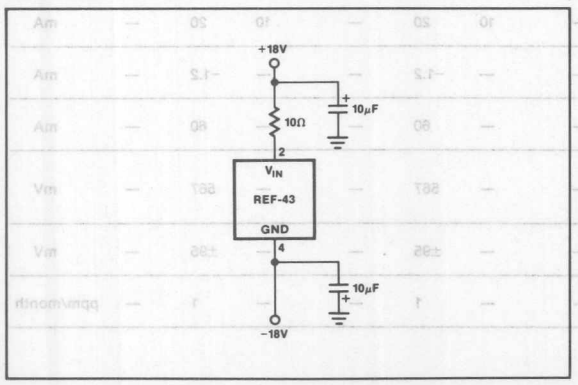
ELECTRICAL CHARACTERISTICS at V_{IN} = +5V, I_L = 0mA, –55°C ≤ T_A ≤ +125°C for the REF-43B and –40°C ≤ T_A ≤ +85°C for the REF-43F/G, unless otherwise noted.

			REF-43B			REF-43F			REF-43G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage Tolerance		No Load	–	0.1	0.2	–	0.06	0.12	–	0.1	0.2	%
Output Voltage	V_O	No Load	2.495	2.500	2.505	2.497	2.500	2.503	2.495	2.500	2.505	V
Output Voltage Temperature Coefficient	TCV_O	–55°C ≤ T_A ≤ +125°C	–	6	10	–	–	–	–	–	–	ppm/°C
		–40°C ≤ T_A ≤ +85°C	–	–	–	–	6	10	–	10	25	
		(Note 1)										
Line Regulation		V_{IN} = +4.5V to +40V	–	1	3	–	1	3	–	1	3	ppm/V
Load Regulation		I_L = 0mA to 10mA	–	25	40	–	20	35	–	25	40	ppm/mA
Quiescent Supply Current	I_{SY}	No Load	–	400	600	–	400	600	–	400	600	µA
Load Current (Sourcing)	I_L	(Note 2)	10	20	–	10	20	–	10	20	–	mA
Temperature Hysteresis of Output Voltage		ΔT = ±25°C	–	100	–	–	100	–	–	100	–	µV
Temperature Voltage Output Tempco	TCV_{TEMP}		–	1.9	–	–	1.9	–	–	1.9	–	mV/°C

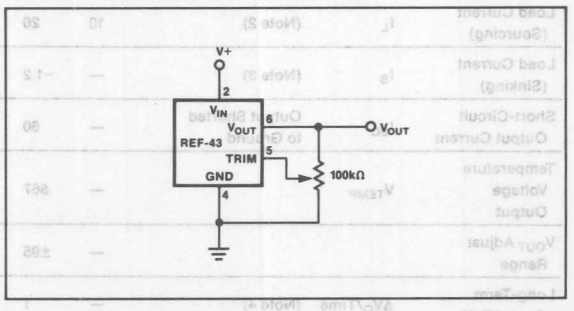
NOTES:

1. Output voltage temperature coefficient is measured by the box method. The tempco is defined as the slope of the diagonal of a box drawn around the output voltage plotted against temperature. V_{OUT} is measured at T_{MIN}, 25°C and T_{MAX} for the applicable temperature range. The lowest of these three readings is subtracted from the highest reading and the resulting difference is divided by (T_{MAX} - T_{MIN}).
2. Guaranteed by Load Regulation test.

BURN-IN CIRCUIT



OUTPUT VOLTAGE TRIM METHOD



Precision Micropower, Low Dropout, Voltage References

REF19x Series*

FEATURES

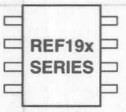
Initial Accuracy: ±2 mV max
Temperature Coefficient: 5 ppm/°C max
Low Supply Current: 45 µA max
Low Dropout Voltage
Load Regulation: 4 ppm/mA
Line Regulation: 4 ppm/V
High Output Current: 30 mA
Short Circuit Protection
Shutdown Mode

APPLICATIONS

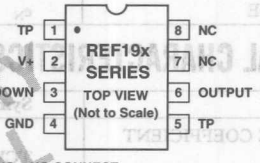
Portable Instrumentation
A-to-D and D-to-A Converters
Smart Sensors
Solar Powered Applications
Loop Current Powered Instruments

PIN CONFIGURATIONS

8-Lead Narrow-Body SO (S Suffix)



8-Lead Epoxy DIP (P Suffix)



NC = NO CONNECT
TP PINS ARE FACTORY TEST POINTS – NO USER CONNECTION

GENERAL DESCRIPTION

REF19x series precision bandgap voltage references utilize a patented temperature drift curvature correction circuit and laser trimming of highly stable thin-film resistors to achieve a very low temperature coefficient and a high initial accuracy.

The REF19x series are micropower, Low Dropout Voltage (LDV) devices providing a stable output voltage from supplies as low as 100 mV above the output voltage and consuming less than 45 µA of supply current. In shutdown mode, which is enabled by applying a low TTL or CMOS level to the shutdown pin, the output is turned off and supply current is further reduced to less than 15 µA.

The REF19x series references are specified over the extended industrial temperature range (–40°C to +85°C) and High Operating Temperature (HOT) range (–40°C to +125°C) for applications such as automotive.

All grades are available in 8-pin SOIC and PDIP. Products are also available in die form. TSSOP 8-pin available Q4, 1994.

Table I.

Part Number	Nominal Output Voltage (V)
REF190*	Adjustable 2 V to 6 V
REF191*	2.048
REF192	2.50
REF193	3.00
REF194	4.50
REF195	5.00
REF196	3.30
REF198	4.096

*Contact factory for specifications and availablility.

*Protected by U.S. Patent No. 5291222.

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PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

REF192–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +2.6 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
INITIAL ACCURACY						
"E" Grade	V_O	I_{OUT} = 1 mA	2.498	2.500	2.502	V
"F" Grade			2.495		2.505	V
"G" Grade			2.490		2.510	V
LINE REGULATION						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	2.6 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA		2	4	ppm/V
"F & G" Grades				4	8	ppm/V
"E" Grade	$\Delta V_O/\Delta I_{LOAD}$	V_S = 3.8 V, 0 ≤ I_{OUT} ≤ 30 mA		2	4	ppm/mA
"F & G" Grades				4	8	ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 3.0 V, I_{LOAD} = 10 mA			0.50	V
		V_S = 3.8 V, I_{LOAD} = 30 mA			1.30	V
LONG-TERM STABILITY	ΔV_O	1000 Hours @ +150°C		2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		50		μV p-p

ELECTRICAL CHARACTERISTICS (@ V_S = +2.65 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT						
"E" Grade	TCV_O/°C	I_{OUT} = 1 mA		2	5	ppm/°C
"F" Grade				5	10	ppm/°C
"G" Grade					25	ppm/°C
LINE REGULATION						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	2.65 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA		5	10	ppm/V
"F & G" Grades				10	20	ppm/V
"E" Grade	$\Delta V_O/\Delta I_{LOAD}$	V_S = 3.8 V, 0 ≤ I_{OUT} ≤ 25 mA		5	10	ppm/mA
"F & G" Grades				10	20	ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 3.0 V, I_{LOAD} = 10 mA			0.50	V
		V_S = 3.8 V, I_{LOAD} = 30 mA			1.30	V

ELECTRICAL CHARACTERISTICS (@ V_S = +2.7 V, –40°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT						
"E" Grade	TCV_O/°C	I_{OUT} = 1 mA		2	7	ppm/°C
"F" Grade				5	15	ppm/°C
"G" Grade					25	ppm/°C
LINE REGULATION						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	2.7 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA		10	20	ppm/V
"F & G" Grades				20	30	ppm/V
"E" Grade	$\Delta V_O/\Delta I_{LOAD}$	V_S = 3.8 V, 0 ≤ I_{OUT} ≤ 20 mA		10	20	ppm/mA
"F & G" Grades				20	30	ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 3.10 V, I_{LOAD} = 10 mA			0.60	V
		V_S = 3.95 V, I_{LOAD} = 30 mA			1.45	V
SHUTDOWN PIN						
Logic High Input Voltage	V_H	V_S = 3.3 V	2.4			V
Logic High Input Current	I_L				–5	μA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				–5	μA
SUPPLY CURRENT		V_S = 3.3 V			45	μA
Sleep Mode					15	μA

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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REF193–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +3.10 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
INITIAL ACCURACY "G" Grade	V_O	I_{OUT} = 1 mA	2.990	3.0	3.010	V
LINE REGULATION "G" Grade	$\Delta V_O/\Delta V_{IN}$ $\Delta V_O/\Delta I_{LOAD}$	3.05 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA V_S = 4.3 V, 0 ≤ I_{OUT} ≤ 30 mA		4 4	8 8	ppm/V ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 3.50 V, I_{LOAD} = 10 mA V_S = 4.30 V, I_{LOAD} = 30 mA			0.50 1.30	V V
LONG-TERM STABILITY	ΔV_O	1000 Hours @ +150°C		2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		50		µV p-p

ELECTRICAL CHARACTERISTICS (@ V_S = +3.15 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT "G" Grade	TCV_O/°C	I_{OUT} = 1 mA			25	ppm/°C
LINE REGULATION "G" Grade	$\Delta V_O/\Delta V_{IN}$ $\Delta V_O/\Delta I_{LOAD}$	3.05 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA V_S = 4.3 V, 0 ≤ I_{OUT} ≤ 25 mA		10 10	20 20	ppm/V ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 3.50 V, I_{LOAD} = 10 mA V_S = 4.30 V, I_{LOAD} = 30 mA			0.50 1.30	V V

ELECTRICAL CHARACTERISTICS (@ V_S = +3.20 V, –40°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT "G" Grade	TCV_O/°C	I_{OUT} = 1 mA			25	ppm/°C
LINE REGULATION "G" Grade	$\Delta V_O/\Delta V_{IN}$ $\Delta V_O/\Delta I_{LOAD}$	3.05 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA V_S = 4.3 V, 0 ≤ I_{OUT} ≤ 20 mA		20 20	30 30	ppm/V ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 3.60 V, I_{LOAD} = 10 mA V_S = 4.45 V, I_{LOAD} = 30 mA			0.60 1.45	V V
SHUTDOWN PIN Logic High Input Voltage Logic High Input Current Logic Low Input Voltage Logic Low Input Current	 V_H I_L V_L I_L	 V_S = 3.3 V	 2.4		 –5 0.8 –5	 V µA V µA
SUPPLY CURRENT Sleep Mode		V_S = 3.3 V			45 15	µA µA

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

8

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

REF194–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +4.6 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
INITIAL ACCURACY						
"E" Grade	V_O	I_{OUT} = 1 mA	4.498	4.5	4.502	V
"F" Grade			4.495		4.505	V
"G" Grade			4.490		4.510	V
LINE REGULATION						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	4.6 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA		2	4	ppm/V
"F & G" Grades				4	8	ppm/V
"E" Grade	$\Delta V_O/\Delta I_{LOAD}$	V_S = 5.8 V, 0 ≤ I_{OUT} ≤ 30 mA		2	4	ppm/mA
"F & G" Grades				4	8	ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 5.00 V, I_{LOAD} = 10 mA			0.50	V
		V_S = 5.8 V, I_{LOAD} = 30 mA			1.30	V
LONG-TERM STABILITY	ΔV_O	1000 Hours @ +150°C		2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		50		µV p-p

ELECTRICAL CHARACTERISTICS (@ V_S = +4.65 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT						
"E" Grade	TCV_O/°C	I_{OUT} = 1 mA		2	5	ppm/°C
"F" Grade				5	10	ppm/°C
"G" Grade					25	ppm/°C
LINE REGULATION						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	4.65 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA		2	4	ppm/V
"F & G" Grades				4	8	ppm/V
"E" Grade	$\Delta V_O/\Delta I_{LOAD}$	V_S = 5.80 V, 0 ≤ I_{OUT} ≤ 25 mA		2	4	ppm/mA
"F & G" Grades				4	8	ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 5.00 V, I_{LOAD} = 10 mA			0.50	V
		V_S = 5.8 V, I_{LOAD} = 30 mA			1.30	V

ELECTRICAL CHARACTERISTICS (@ V_S = +4.70 V, –40°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT						
"E" Grade	TCV_O/°C	I_{OUT} = 1 mA		2	7	ppm/°C
"F" Grade				5	15	ppm/°C
"G" Grade					25	ppm/°C
LINE REGULATION						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	4.70 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA		2	4	ppm/V
"F & G" Grades				4	8	ppm/V
"E" Grade	$\Delta V_O/\Delta I_{LOAD}$	V_S = 5.80 V, 0 ≤ I_{OUT} ≤ 20 mA		2	4	ppm/mA
"F & G" Grades				4	8	ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 5.10 V, I_{LOAD} = 10 mA			0.60	V
		V_S = 5.95 V, I_{LOAD} = 30 mA			1.45	V
SHUTDOWN PIN						
Logic High Input Voltage	V_H	V_S = 3.3 V	2.4			V
Logic High Input Current	I_L				–5	µA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				–5	µA
SUPPLY CURRENT		V_S = 3.3 V			45	µA
Sleep Mode					15	µA

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

REF195–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5.10 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
INITIAL ACCURACY						
"E" Grade	V_O	I_{OUT} = 1 mA	4.998	5.0	5.002	V
"F" Grade			4.995		5.005	V
"G" Grade			4.990		5.010	V
LINE REGULATION						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	5.10 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA		2	4	ppm/V
"F & G" Grades				4	8	ppm/V
"E" Grade	$\Delta V_O/\Delta I_{LOAD}$	V_S = 6.30 V, 0 ≤ I_{OUT} ≤ 30 mA		2	4	ppm/mA
"F & G" Grades				4	8	ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 5.50 V, I_{LOAD} = 10 mA			0.50	V
		V_S = 6.30 V, I_{LOAD} = 30 mA			1.30	V
LONG-TERM STABILITY	ΔV_O	1000 Hours @ +150°C		2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		50		μV p-p

ELECTRICAL CHARACTERISTICS (@ V_S = +5.15 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT						
"E" Grade	TCV_O/°C	I_{OUT} = 1 mA		2	5	ppm/°C
"F" Grade				5	10	ppm/°C
"G" Grade					25	ppm/°C
LINE REGULATION						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	5.15 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA		2	4	ppm/V
"F & G" Grades				4	8	ppm/V
"E" Grade	$\Delta V_O/\Delta I_{LOAD}$	V_S = 6.30 V, 0 ≤ I_{OUT} ≤ 25 mA		2	4	ppm/mA
"F & G" Grades				4	8	ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 5.50 V, I_{LOAD} = 10 mA			0.50	V
		V_S = 6.30 V, I_{LOAD} = 25 mA			1.30	V

PRELIMINARY TECHNICAL DATA

ELECTRICAL CHARACTERISTICS (@ V_S = +5.20 V, –40°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT						
"E" Grade	TCV_O/°C	I_{OUT} = 1 mA		2	7	ppm/°C
"F" Grade				5	15	ppm/°C
"G" Grade					25	ppm/°C
LINE REGULATION						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	5.20 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA		2	4	ppm/V
"F & G" Grades				4	8	ppm/V
"E" Grade	$\Delta V_O/\Delta I_{LOAD}$	V_S = 6.450 V, 0 ≤ I_{OUT} ≤ 20 mA		2	4	ppm/mA
"F & G" Grades				4	8	ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 5.60 V, I_{LOAD} = 10 mA			0.60	V
		V_S = 6.45 V, I_{LOAD} = 20 mA			1.45	V
SHUTDOWN PIN						
Logic High Input Voltage	V_H	V_S = 5.5 V	2.4			V
Logic High Input Current	I_L				–5	μA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				–5	μA
SUPPLY CURRENT		V_S = 5.5 V			45	μA
Sleep Mode					15	μA

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

REF196–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +3.4 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
INITIAL ACCURACY "G" Grade	V_O	I_{OUT} = 1 mA	3.290	3.3	3.310	V
LINE REGULATION "G" Grade	$\Delta V_O/\Delta V_{IN}$ $\Delta V_O/\Delta I_{LOAD}$	3.40 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA V_S = 3.80 V, 0 ≤ I_{OUT} ≤ 30 mA		4 4	8 8	ppm/V ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 3.80 V, I_{LOAD} = 10 mA V_S = 4.60 V, I_{LOAD} = 30 mA			0.50 1.30	V V
LONG-TERM STABILITY	ΔV_O	1000 Hours @ +150°C		2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		50		µV p-p

ELECTRICAL CHARACTERISTICS (@ V_S = +3.45 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT "G" Grade	TCV_O/°C	I_{OUT} = 1 mA			25	ppm/°C
LINE REGULATION "G" Grade	$\Delta V_O/\Delta V_{IN}$ $\Delta V_O/\Delta I_{LOAD}$	3.45 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA V_S = 3.80 V, 0 ≤ I_{OUT} ≤ 25 mA		4 4	8 8	ppm/V ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 3.80 V, I_{LOAD} = 10 mA V_S = 4.60 V, I_{LOAD} = 25 mA			0.50 1.30	V V

ELECTRICAL CHARACTERISTICS (@ V_S = +3.50 V, –40°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT "G" Grade	TCV_O/°C	I_{OUT} = 1 mA			25	ppm/°C
LINE REGULATION "G" Grade	$\Delta V_O/\Delta V_{IN}$ $\Delta V_O/\Delta I_{LOAD}$	3.50 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA V_S = 3.80 V, 0 ≤ I_{OUT} ≤ 20 mA		4 4	8 8	ppm/V ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 3.90 V, I_{LOAD} = 10 mA V_S = 4.75 V, I_{LOAD} = 20 mA			0.60 1.45	V V
SHUTDOWN PIN Logic High Input Voltage Logic High Input Current Logic Low Input Voltage Logic Low Input Current	 V_H I_L V_L I_L	 V_S = 5.5 V	 2.4		 –5 0.8 –5	 V µA V µA
SUPPLY CURRENT Sleep Mode		V_S = 5.5 V			45 15	µA µA

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

REF198–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +4.2 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
INITIAL ACCURACY						
"E" Grade	V_O	I_{OUT} = 1 mA	4.094	4.096	4.098	V
"F" Grade			4.091		4.101	V
"G" Grade			4.086		4.106	V
LINE REGULATION						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	4.2 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA		2	4	ppm/V
"F & G" Grades				4	8	ppm/V
"E" Grade	$\Delta V_O/\Delta I_{LOAD}$	V_S = 5.4 V, 0 ≤ I_{OUT} ≤ 30 mA		2	4	ppm/mA
"F & G" Grades				4	8	ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 4.6 V, I_{LOAD} = 10 mA			0.50	V
		V_S = 5.4 V, I_{LOAD} = 30 mA			1.30	V
LONG-TERM STABILITY	ΔV_O	1000 Hours @ +150°C		2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		50		µV p-p

ELECTRICAL CHARACTERISTICS (@ V_S = +4.2 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT						
"E" Grade	TCV_O/°C	I_{OUT} = 1 mA		2	5	ppm/°C
"F" Grade				5	10	ppm/°C
"G" Grade					25	ppm/°C
LINE REGULATION						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	4.2 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA		2	4	ppm/V
"F & G" Grades				4	8	ppm/V
"E" Grade	$\Delta V_O/\Delta I_{LOAD}$	V_S = 5.4 V, 0 ≤ I_{OUT} ≤ 25 mA		2	4	ppm/mA
"F & G" Grades				4	8	ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 4.6 V, I_{LOAD} = 10 mA			0.50	V
		V_S = 5.4 V, I_{LOAD} = 30 mA			1.30	V

ELECTRICAL CHARACTERISTICS (@ V_S = +4.2 V, –40°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT						
"E" Grade	TCV_O/°C			2	7	ppm/°C
"F" Grade				5	15	ppm/°C
"G" Grade					25	ppm/°C
LINE REGULATION						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	4.2 V ≤ V_S ≤ 15 V, I_{OUT} = 1 mA		2	4	ppm/V
"F & G" Grades				4	8	ppm/V
"E" Grade	$\Delta V_O/\Delta I_{LOAD}$	V_S = 5.0 V, 0 ≤ I_{OUT} ≤ 20 mA		2	4	ppm/mA
"F & G" Grades				4	8	ppm/mA
DROPOUT VOLTAGE	V_S–V_O	V_S = 4.7 V, I_{LOAD} = 10 mA			0.60	V
		V_S = 5.6 V, I_{LOAD} = 30 mA			1.50	V
SHUTDOWN PIN						
Logic High Input Voltage	V_H	V_S = 4.5 V	2.4			V
Logic High Input Current	I_L				–5	µA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				–5	µA
SUPPLY CURRENT		V_S = 4.5 V			45	µA
Sleep Mode					15	µA

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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Parameter	Symbol	Condition	Limits	Units
Initial Accuracy				
REF190	V_O		Adjustable	V
REF191			2.043/2.053	V
REF192			2.495/2.505	V
REF193			2.990/3.010	V
REF194			4.495/4.505	V
REF195			4.995/5.005	V
REF196			3.290/3.310	V
REF198			4.091/4.101	V
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	V_O +1.3 V < V_{IN} < 15 V, I_{OUT} = 30 mA		mV/V
LOAD REGULATION	$\Delta V_O/\Delta I_{LOAD}$	1 mA < I_{LOAD} < 30 mA, V_{IN} = V_O +1.3 V		mV/mA
DROPOUT VOLTAGE	V_O–V+	I_{LOAD} = 10 mA	0.5	V
		I_{LOAD} = 30 mA	1.3	V
STANDBY MODE INPUT				
Logic Input High	V_{IH}		2.4	V
Logic Input Low	V_{IL}		0.8	V
SUPPLY CURRENT		No Load	45	µA
Standby Mode			15	µA

NOTE
For proper operation, a 1 πµF capacitor is required between the output pins and the GND pin of the REF19x. Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +18 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
P, S Packages . . . . . –65°C to +150°C
Operating Temperature Range
REF19x . . . . . –40°C to +85°C
Junction Temperature Range
P, S Packages . . . . . –65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP, and θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
REF19xGP	–40°C to +85°C	8-Pin Plastic DIP	N-8
REF19xGS	–40°C to +85°C	8-Pin SOIC	SO-8
REF19xGBC	+25°C	DICE	

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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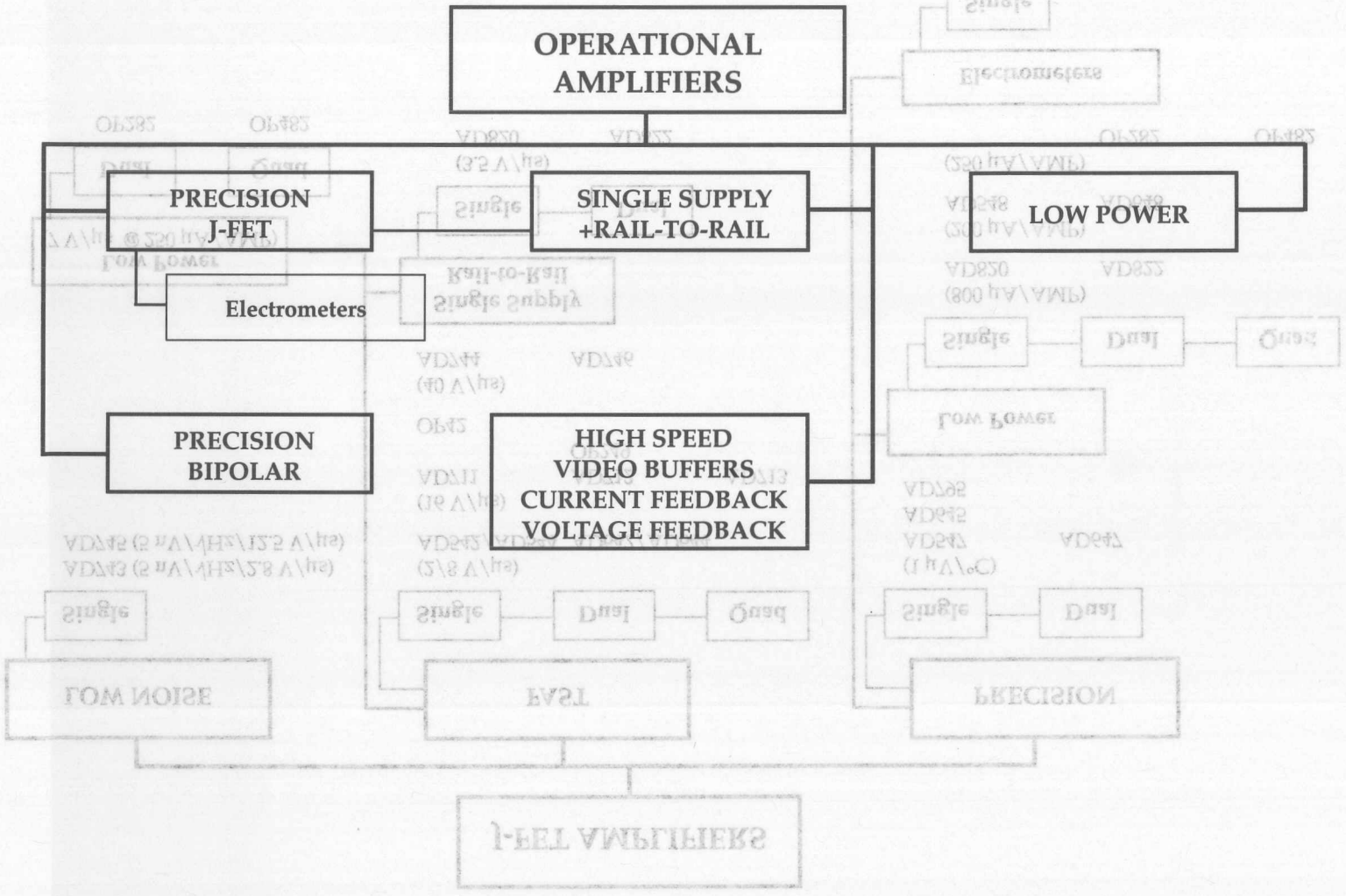
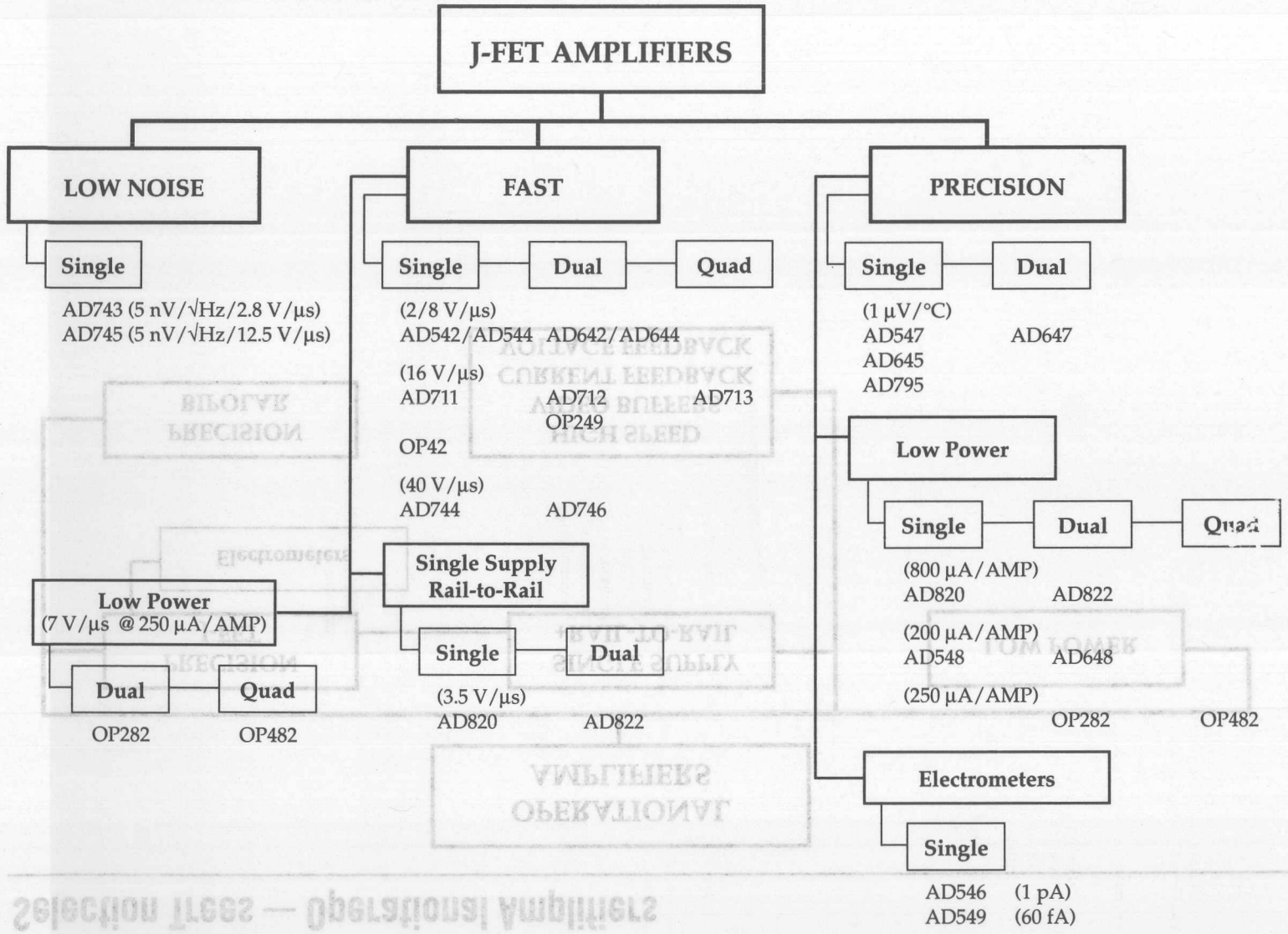
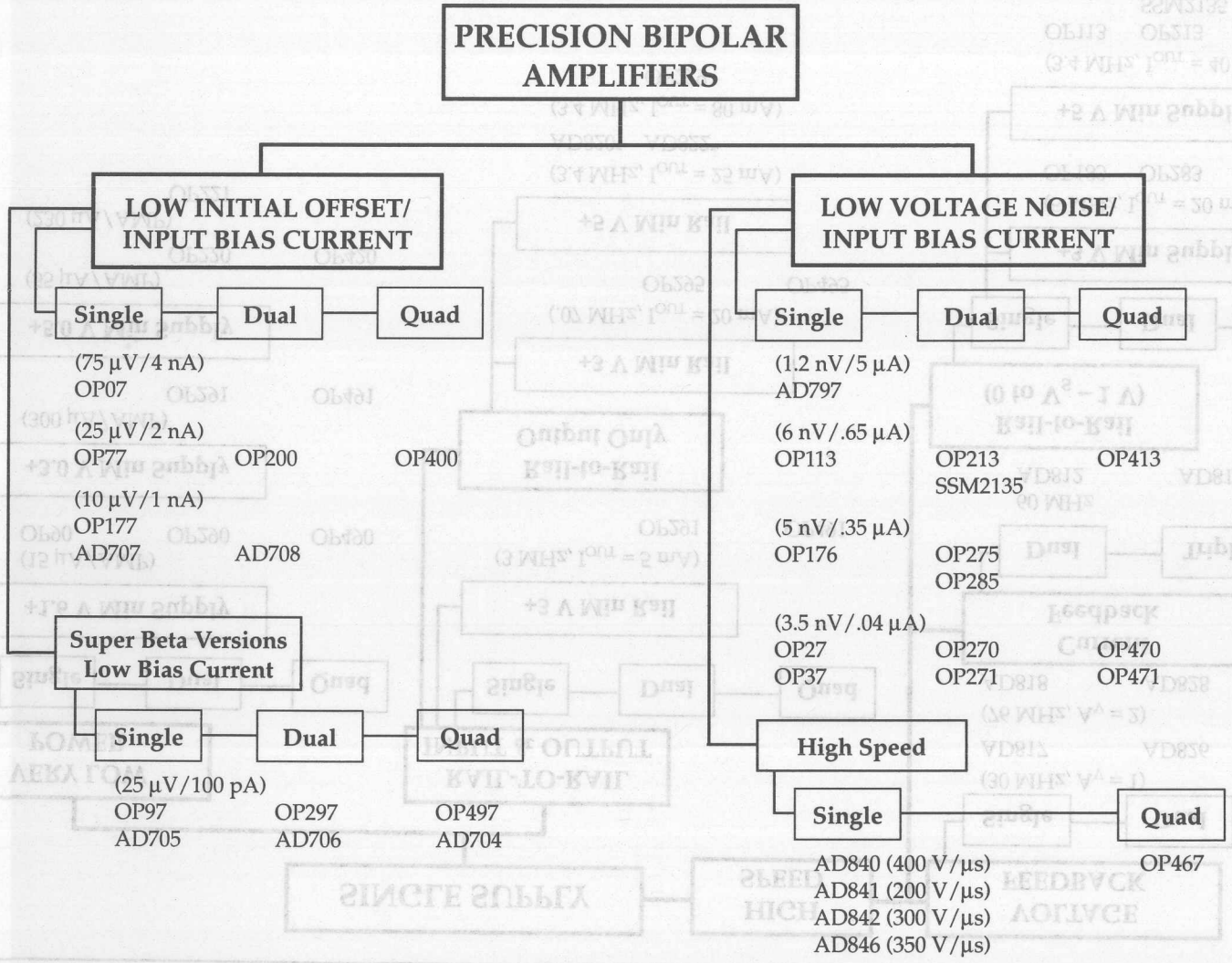
Selection Trees — Operational Amplifiers



Selection Trees — Operational Amplifiers




PRECISION BIPOLAR AMPLIFIERS
LOW INITIAL OFFSET/ INPUT BIAS CURRENT
Single
Dual
Quad
(75 µV/4 nA)
OP07
(25 µV/2 nA)
OP77
OP200
OP400
(10 µV/1 nA)
OP177
AD707
AD708
Super Beta Versions Low Bias Current
Single
Dual
Quad
(25 µV/100 pA)
OP97
AD705
OP297
AD706
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LOW VOLTAGE NOISE/ INPUT BIAS CURRENT
Single
Dual
Quad
(1.2 nV/5 µA)
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(6 nV/.65 µA)
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SSM2135
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(5 nV/.35 µA)
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OP470
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High Speed
Single
Quad
AD840 (400 V/µs)
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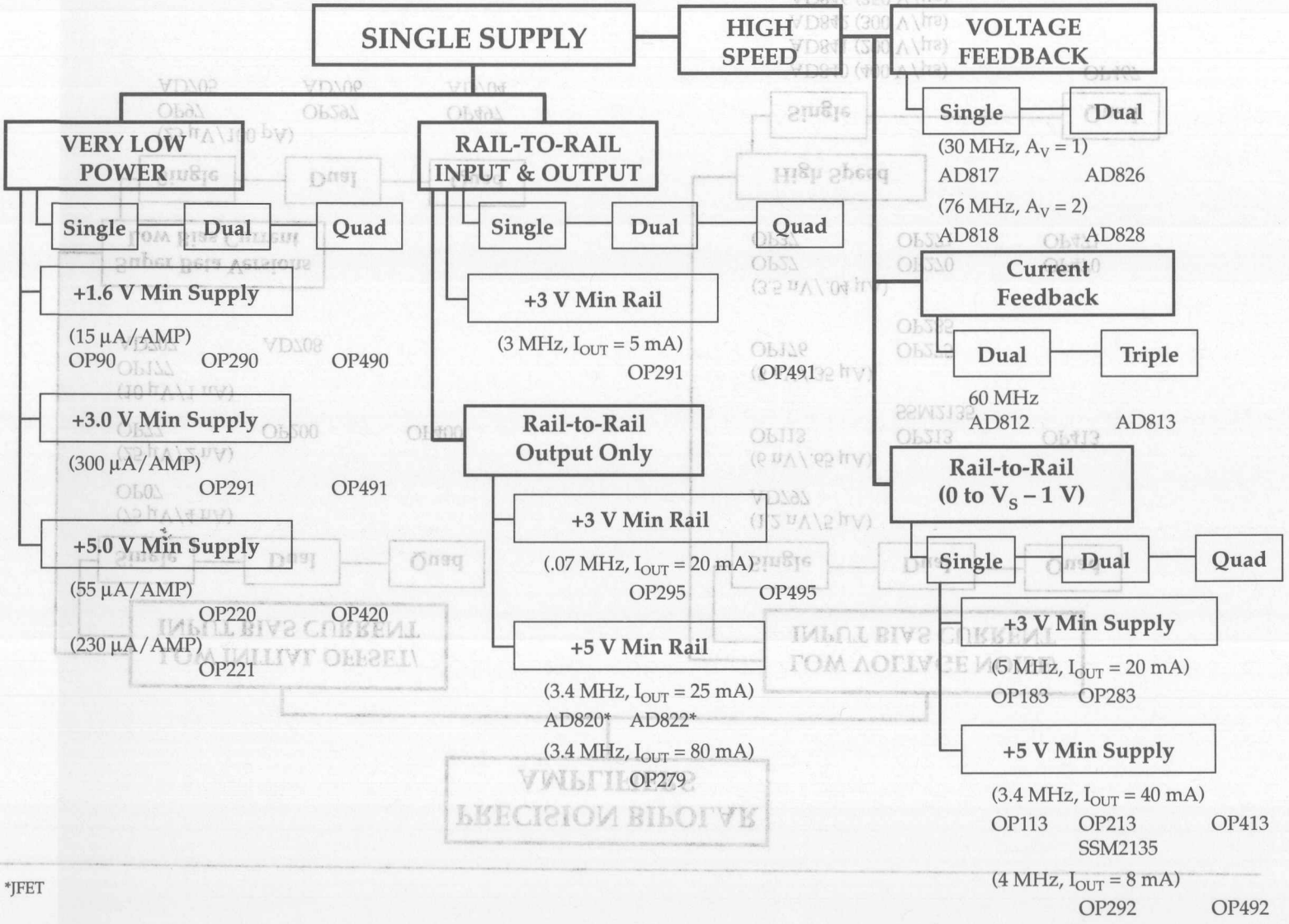
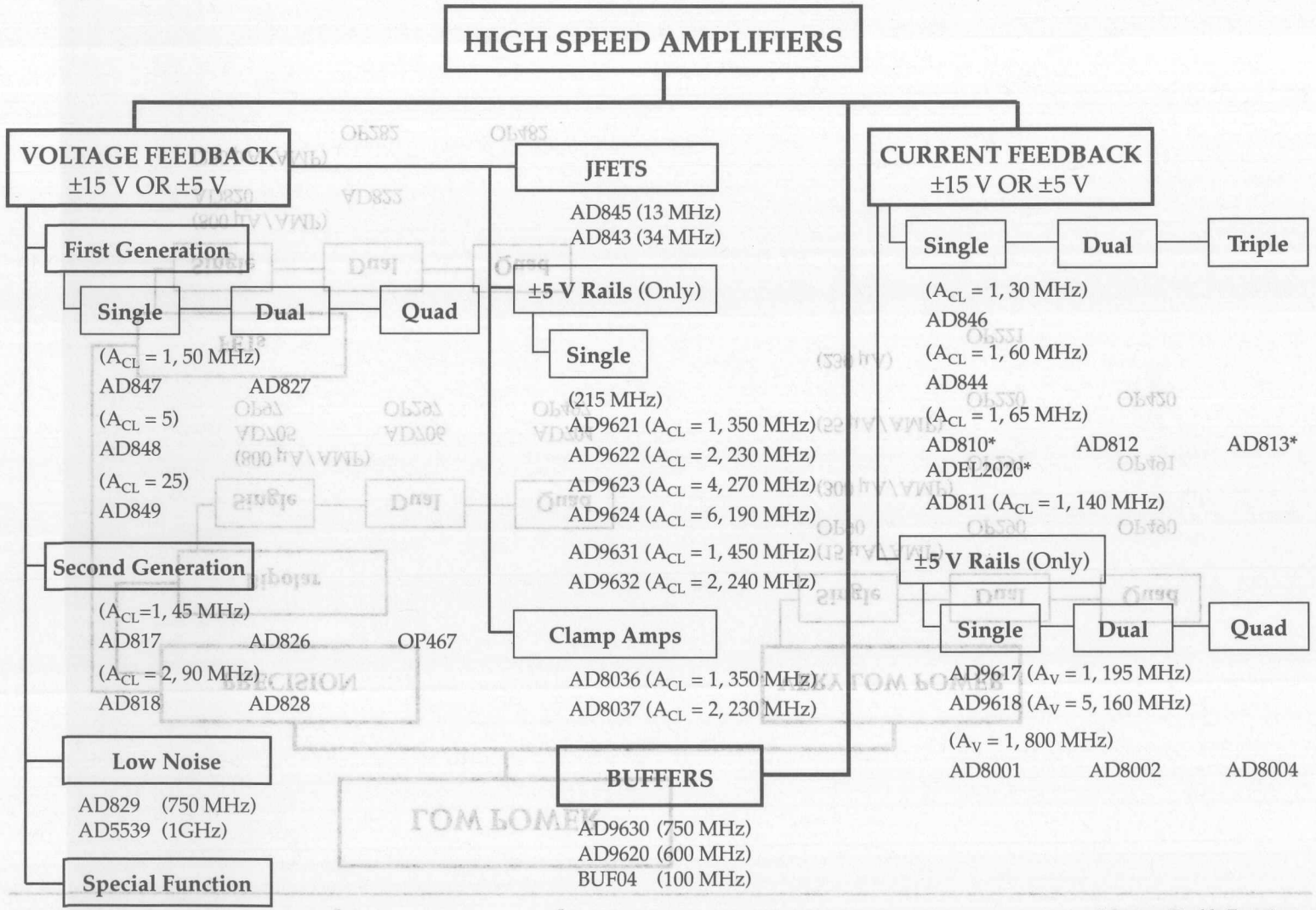
AD842 (300 V/µs)
AD846 (350 V/µs)
OP467

Selection Trees — Operational Amplifiers



*JFET


HIGH SPEED AMPLIFIERS
VOLTAGE FEEDBACK
±15 V OR ±5 V
First Generation
Single
Dual
Quad
(A_CL = 1, 50 MHz)
AD847
AD827
(A_CL = 5)
AD848
(A_CL = 25)
AD849
Second Generation
(A_CL=1, 45 MHz)
AD817
AD826
OP467
(A_CL = 2, 90 MHz)
AD818
AD828
Low Noise
AD829 (750 MHz)
AD5539 (1GHz)
Special Function
AD830 (Differential Input Preamp)
JFETS
AD845 (13 MHz)
AD843 (34 MHz)
±5 V Rails (Only)
Single
(215 MHz)
AD9621 (A_CL = 1, 350 MHz)
AD9622 (A_CL = 2, 230 MHz)
AD9623 (A_CL = 4, 270 MHz)
AD9624 (A_CL = 6, 190 MHz)
AD9631 (A_CL = 1, 450 MHz)
AD9632 (A_CL = 2, 240 MHz)
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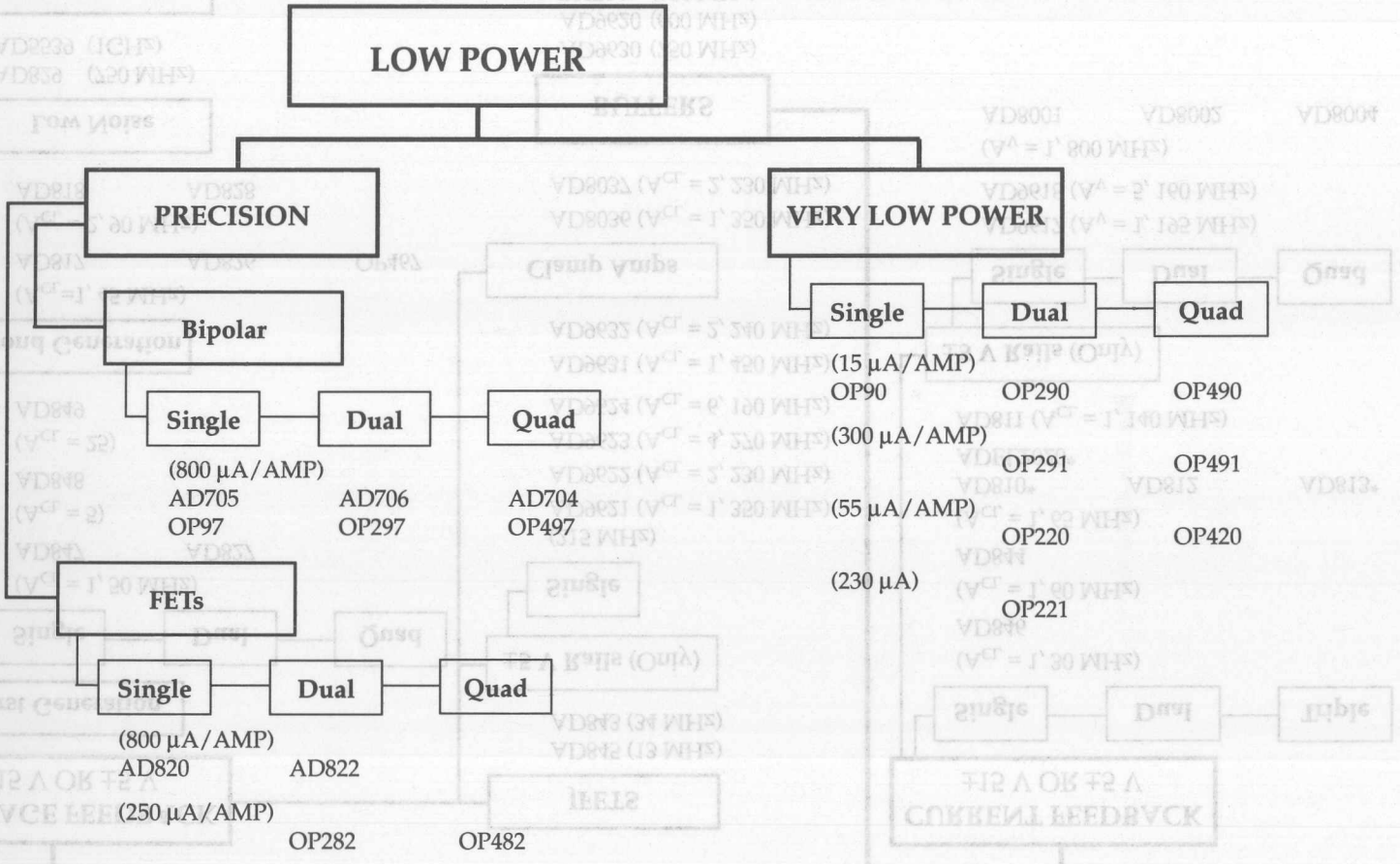
AD8036 (A_CL = 1, 350 MHz)
AD8037 (A_CL = 2, 230 MHz)
BUFFERS
AD9630 (750 MHz)
AD9620 (600 MHz)
BUF04 (100 MHz)
CURRENT FEEDBACK
±15 V OR ±5 V
Single
Dual
Triple
(A_CL = 1, 30 MHz)
AD846
(A_CL = 1, 60 MHz)
AD844
(A_CL = 1, 65 MHz)
AD810*
AD812
AD813*
ADEL2020*
AD811 (A_CL = 1, 140 MHz)
±5 V Rails (Only)
Single
Dual
Quad
AD9617 (A_V = 1, 195 MHz)
AD9618 (A_V = 5, 160 MHz)
(A_V = 1, 800 MHz)
AD8001
AD8002
AD8004
* Output Disable Function

Selection Trees — Operational Amplifiers



Selection Guides—Operational Amplifiers

Single Supply Amplifiers

Model	ISY max mA	V_{OS} max mV	Supply Voltage Range V	GBW typ MHz	SR typ V/μs	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
OP22	0.0002–0.4	0.3–1	+3 to +30	0.25	0.08	H, N, Q, R	I, M/	Programmable	A 2–597
OP90	**0.02**	**0.15–0.45**	**+1.6 to +36**	**0.02**	**—**	**E, N, Q, R**	**I, M/$_S$**	**Micropower, Low Voltage**	**9–375**
OP290	**0.04**	**0.2–0.5**	**+1.6 to +36**	**0.02**	**—**	**E, N, Q, R**	**I, M/$_{DS}$**	**Dual Micropower, Low Voltage**	**9–477**
OP20	0.08	0.25–1	+5 to +30	0.1	0.05	E, N, Q, R	I, M/	Micropower, Low Cost	A 2–585
OP490	**0.08**	**0.5–1**	**+1.6 to +36**	**0.02**	**—**	**E, N, Q, R**	**I, M/$_{DS}$**	**Quad Micropower, Low Voltage**	**9–564**
OP220	**0.17**	**0.15–0.75**	**+5 to +30**	**0.2**	**0.05**	**H, N, Q, R**	**I, M/$_S$**	**Dual Micropower, Low Cost**	**9–436**
OP295	**0.200**	**0.25–1.0**	**+2.4 to +36**	**0.08**	**0.02**	**N, Q, R**	**I, M**	**Rail-to-Rail Dual**	**9–518**
OP80	0.325	1.5	+5 to +16	0.3	0.4	N, Q, H	I, M	Low I_B, CMOS	A 2–727
OP291/491	**0.350**	**0.7**	**+2.7 to +12**	**3**	**0.5**	**N, R**	**I**	**Rail-to-Rail, Micropower**	**9–481**
OP420	**0.36**	**2.5–6**	**+5 to +30**	**0.15**	**0.05**	**E, N, Q, R**	**I, M/$_S$**	**Quad Micropower, Low Cost**	**9–538**
OP21	0.3–0.4	0.1–0.5	+5 to +30	0.6	0.25H,	N, Q, R	I, M/	Low Cost, Low Power	A 2–591
OP495	**0.4**	**0.2–0.5**	**+3 to +36**	**0.08**	**0.02**	**N, Q, R**	**I, M**	**Quad Rail to Rail**	**9–518**
AD820	**0.660**	**0.25–1**	**+4 to +36**	**2**	**3.75**	**N, Q, R**	**C, I, M**	**Fast FET Input Rail to Rail**	**9–170**
OP221	**0.8**	**0.15–0.5**	**+5 to +30**	**0.6**	**0.3**	**H, N, Q, R**	**I, M/$_S$**	**Dual Low Cost, Low Power**	**9–439**
AD822	**1.3**	**0.25–1**	**+4 to +36**	**2**	**3.75**	**N, Q, R**	**C, I, M**	**Dual AD820**	**9–170**
OP183/283	**1.5**	**1.0**	**+3 to +18**	**5**	**10**	**N, R**	**I**	**5 MHz, Low Noise**	**9–420**
OP421	1.8	2.5–6	+5 to +30	1.9	0.5	N, Q, R	I, M/$_D$	Quad Low Cost, Low Power	A 2–993
OP279	**2.5**	**4.0**	**+4.75 to +12**	**2**	**5**	**N, R**	**I**	**Rail-to-Rail Input/Output, 50 mA Out**	**9–459**
AD812	**3.5**	**3.0**	**+3.0 to +15**	**50**	**125**	**N, R**	**I**	**Dual 50 MHz, Current Feedback**	**9–110**
AD813	**3.5**	**3.0**	**+3.0 to +15**	**50**	**100**	**N, R**	**I**	**Triple Current Feedback Video Op Amp**	**9–127**
OP113/213/413	**4**	**0.150**	**+5 to +30**	**3**	**1**	**E, N, P, Q, R**	**I, M**	**Low Noise, Low Drift Op Amp**	**9–382**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]A = *Amplifier Reference Manual*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Selection Guides—Operational Amplifiers

High Speed Amplifiers

Model	SR V/μs typ	GBW MHz typ	Settling Time ns to % typ	A_{CL} min V/V	V_{OS} mV typ	I_{OUT} mA min	Supply Current mA typ	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
AD8004	3000	400	10–0.1	1	5.0	50	3.5	N, R	I	Quad Very High Slew Rate Amplifier	9–291
AD811	2500	1000	65–0.01	1	0.5	100 typ	16.5	E, N, Q, R	I, M	Video Amp, 0.12%/0.01° Differential Gain/Phase Error, 0.1 dB Flatness to 35 MHz	9–107
AD9624	2200	1800	14–0.01	6	2	60	23	N, Q, R	I, M	Voltage Feedback Amp; ±3 V Supply Operation	9–318
AD9623	2100	1080	14–0.01	4	2	60	23	N, Q, R	I, M	Voltage Feedback Amp; −64 dB HD @ 20 MHz	9–315
AD844	2000	900	100–0.1	1	0.05	20	6.5	N, Q, R	I, $M/_S$	Constant 10 ns Rise Time for Any Pulse Input, Current Feedback	9–245
AD9618	1800	8000	10–0.1	−1	0.2	60	31	N, Q, R, Z	C, I, $M/_D$	Low Distortion, Wideband, IMD ≤ −70 dBc at 20 MHz	9–303
AD9617	1600	570	10–0.1	1	0.4	60	34	N, Q, R, Z	C, I, $M/_{DS}$	Low Distortion, Wide Bandwidth, IMD ≤ −70 dBc at 20 MHz	9–300
AD8036	1600	350	16–0.01	1	2	70 typ	17	N, Q, R	I, M	Clamping, Voltage Feedback, ±3 V Supply	9–295
AD8037	1600	240	16–0.01	2	2	70 typ	17	N, Q, R	I, M	Clamping, Voltage Feedback, ±3 V Supply	9–295
AD812	1600	145	50–0.1	1	2	40	3.5	N, R	I	Low Power, Single Supply, Dual	9–110
AD9622	1500	440	14–0.01	2	2	60	23	N, Q, R	I, M	Voltage Feedback Amp; −66 dB HD @ 20 MHz	9–312
AD9632	1500	250	11–0.1	2	2	70 typ	17	N, Q, R	I, M	Low Distortion, Voltage Feedback, ±3 V Supply	9–324
AD9631	1300	320	11–0.1	1	2	70 typ	17	N, Q, R	I, M	Low Distortion, Voltage Feedback, ±3 V Supply	9–324
AD8001	1200	880	10–0.1	1	2.0	50	5	N, Q, R	I	Current Feedback, Low Power, 880 MHz	9–265
AD8002	1200	880	10–0.1	1	2.0	50	5	N, R	I	Dual AD8001	9–278
AD9621	1200	350	11–0.01	1	2	60	23	N, Q, R	I, M	Voltage Feedback Amp; Wide BW; Low Noise	9–309
AD810	1000	650	50–0.1	1	1.5	40	6.8/2.5	N, Q, R	I, M	Video Amp with Disable Feature	9–92
OP260	1000	90	250–0.1	1	1	20	9	E, H, N, Q, R,	I, $M/_{DS}$	Dual Current Feedback	A 2–873
AD5539	600	1400	12–1.0	5	2.0	15	14	N, Q	C, M	General Purpose, High Speed Amp	9–262
AD830	530	100	25–0.1	1	1.5	50	14.5	N, Q, R	C, I, M	Video Difference Amplifier	9–218
ADEL2020	500	300	60–0.1	1	1.5	30	6.8/2.1	N, R	I	Second Source to EL2020	9–329
AD818	500	260	80–0.01	−1	0.5	50	7	N, R	I	Low Power, Video Amp	9–158
AD828	500	260	80-0.01	−1	0.5	50	7	N, R	I	Dual AD818	9–203
AD846	450	450	110–0.01	1	0.025	20 typ	5	N, Q	I, $M/_{DS}$	High Speed, Precision, Current Feedback	9–251
AD813	450	100	50–0.1	1	2	30	3.5	N, R	I	Triple Low Power Video Amp	9–127
AD840	400	400	100–0.01	10	0.1	50	10.5	E, N, Q	C, $M/_{DS}$	Wide Bandwidth Precision, Fast Settling, $A_{VCL} \geq 10$	9–233
AD842	375	80	100–0.01	2	0.3	100	13	E, H, N, Q	C, $M/_D$	Fast Settling, High Current Output, Cable Driver, $A_{VCL} \geq 2$	9–239
AD817	350	50	70–0.01	1	0.5	50	7	N, R	I	Low Power, General Purpose, High I_{OUT}	9–145
AD826	350	50	70–0.01	1	0.5	50	7	N, R	I	Dual AD817	9–187
AD849	300	725	80–0.1	25	0.3	20 typ	5.1	N, Q, R	C, I, M/	High Speed, Low Power Preamp, Drives Capacitive Loads	9–258

Model	SR V/µs typ	GBW MHz typ	Settling Time ns to % typ	A_{CL} min V/V	V_{OS} mV typ	I_{OUT} mA min	Supply Current mA typ	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
AD848	300	175	100–0.1	5	0.2	20 typ	5.1	N, Q, R	C, I, M/	High Speed, Low Power, Drives Capacitive Loads	9–258
AD827	300	50	120–0.1	1	0.5	20 typ	10.5	N, Q, R	C, I, $M/_D$	Dual AD847	9–200
AD847	300	50	120–0.01	1	0.5	20 typ	5.3	N, Q, R	C, I, $M/_{DS}$	High Speed, Low Power, Drives Capacitive Loads	9–254
AD841	300	40[4]	110–0.01	1	0.5	50	11	E, H, N, Q	C, $M/_{DS}$	High Speed, Precision, Drives Capacitive Loads	9–236
AD843	250	34[4]	135–0.01	1	0.5	50	12	E, H, N, Q, R	C, I, $M/_{DS}$	FET Input, Fast Settling, High Speed	9–242
AD829	230	750	65–0.1	1	0.2	20 typ	5.3	N, Q, R	C, I, M	High Speed, Low Noise, Video Amp	9–215
OP467	170	30	170–0.01	1	0.5	10	8	N, P, Q, R	I, M	Quad High Speed	9–541
AD845	100	16[4]	350–0.01	1	0.1	25 typ	10	N, Q, R	I, $M/_S$	FET Input, Fast Settling, High Speed	9–248

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[3]A = *Amplifier Reference Manual*. All other entries refer to this volume.
[4]−3 dB BW
Boldface Type: Data sheet information in this volume.

Selection Guides—Operational Amplifiers

Low Voltage Noise Amplifiers

Model	Voltage Noise en typ 1 kHz nV/√Hz	Voltage Noise en typ 10 kHz nV/√Hz	Current Noise In ± In− typ 1 kHz pA/√Hz	I_B typ nA	V_{OS} mV typ	GBW MHz typ	SR V/µs typ	Settling Time ns to % typ	A_{CL} min V/V	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
AD797	**0.9**	**0.9**	**2**	**500**	**0.025**	**110**	**20**	**—**	**1**	**N, Q, R**	**I, M**	**Ultralow Noise, Low Distortion**	**9–78**
AD829	**1.7**	**1.7**	**1.5**	**3300**	**0.2**	**750**	**230**	**65–0.1**	**1**	**N, Q, R**	**C, I, M**	**High Speed, Low Noise, Video Amp**	**9–215**
AD811	**1.9**	**1.9**	**1.5/20**	**2000**	**0.5**	**1000**	**2500**	**65–0.01**	**1**	**E, N, Q, R**	**I, M**	**High Performance Video Op Amp**	**9–107**
AD9617	**2.0**	**1.3**	**32/32**	**12000**	**0.5**	**570**	**1400**	**10–0.1**	**±1**	**N, Q, R, Z**	**C, I, M/DS**	**Low Distortion, Wide Bandwidth**	**9–300**
AD9618	**2.0**	**1.3**	**32/32**	**10000**	**0.5**	**8000**	**1800**	**9–0.1**	**+5, −1**	**N, Q, R, Z**	**C, I, M/D**	**Low Distortion, Wide Bandwidth**	**9–303**
AD844	**2**	**2.0**	**12/10**	**200**	**0.05**	**900**	**2000**	**100–0.1**	**1**	**N, Q, R**	**I, M/S**	**Current Feedback Amplifier**	**9–245**
AD846	**2**	**2.0**	**6/20**	**100**	**0.025**	**450**	**450**	**110–0.01**	**1**	**N, Q**	**I, M/DS**	**Current Feedback, Precision**	**9–251**
ADEL2020	**2.9**	**2.9**	**1.5/13**	**1000**	**1.5**	**300**	**500**	**60–0.1**	**1**	**N, R**	**I**	**EL2020 Second Source**	**9–329**
AD810	**2.9**	**2.9**	**1.5/13**	**2000**	**1.5**	**650**	**1000**	**125–0.01**	**1**	**N, Q, R**	**I, M**	**Video Op Amp with Disable**	**9–92**
AD849	**3**	**3.0**	**—**	**3300**	**0.3**	**725**	**300**	**80–0.1**	**25**	**N, Q, R**	**C, I, M/**	**High Speed, Low Power**	**9–258**
OP27	**3.0**	**3.0**	**0.4**	**10**	**0.01**	**8**	**2.8**	**—**	**1**	**E, H, N, Q, R**	**C, I, M/JS**	**Low Noise, Precision**	**9–357**
OP227	3	3.0	0.4	10	0.02	8	2.8	—	1	Q	C, I, M/DS	Dual Matched Precision	A 2–843
OP37	**3**	**3.0**	**0.4**	**10**	**0.01**	**63**	**17**	**—**	**1**	**E, H, N, Q, R**	**C, I, M/DS**	**Fast, Precision $A_{VCL} \geq 5$**	**9–361**
AD745	**3.2**	**2.9**	**0.007**	**0.150**	**0.1**	**20**	**12.5**	**5000–0.01**	**5**	**N, Q, R**	**C, I, M**	**Ultralow Noise, High Speed, BiFET Op Amp**	**9–58**
AD743	**3.2**	**2.9**	**0.007**	**0.15**	**0.1**	**4.5**	**2.8**	**—**	**1**	**N, Q, R**	**C, I, M**	**Ultralow Noise FET Input**	**9–52**
OP270	**3.2**	**3.2**	**0.6**	**5**	**0.01**	**5**	**2.4**	**—**	**1**	**E, N, Q, R**	**I, M/DS**	**Dual Monolithic**	**9–447**
OP470	**3.2**	**3.8**	**0.4**	**6**	**0.1**	**6**	**2**	**—**	**1**	**E, N, Q, R**	**I, M/DS**	**Quad Monolithic, Low Noise**	**9–556**
AD9624	**3.5**	**2.3**	**5.8**	**7000**	**2**	**1800**	**2200**	**14–0.01**	**6**	**N, Q, R**	**I, M**	**Low IMD at High Frequencies**	**9–318**
AD812	**3.5**	**3.5**	**1.5/18**	**20000**	**2.0**	**145**	**1600**	**50–0.1**	**1**	**N, R**	**I**	**Dual, Single Supply, Current Feedback**	**9–110**
AD813	**3.5**	**3.5**	**1.5/18**	**30000**	**2.0**	**100**	**450**	**50–0.1**	**1**	**N, R**	**I**	**Triple Video Amplifier**	**9–127**
AD840	**4**	**—**	**—**	**3500**	**0.1**	**400**	**400**	**100–0.01**	**10**	**E, N, Q**	**C, M/DS**	**Wide Bandwidth, Precision**	**9–233**
AD9623	**4.2**	**2.6**	**8**	**6000**	**2**	**1080**	**2100**	**14–0.01**	**4**	**N, Q, R**	**I, M**	**Balanced High Impedance Inputs**	**9–315**
OP113/213/413	**4.7**	**4.7**	**0.4**	**600**	**0.1**	**3.4**	**1.2**	**9000–0.01**	**1**	**N, Q, R**	**I**	**Single Supply—Single, Dual, Quad**	**9–382**
OP467	**6**	**5.5**	**—**	**100**	**1**	**30**	**170**	**170**	**1**	**N, P, Q, R**	**C, I, M**	**Quad, High Speed**	**9–541**
OP275	**6**	**6**	**—**	**—**	**1**	**9**	**22**	**—**	**1**	**N, R**	**I, M**	**Dual Audio Amp**	**9–454**
AD848	**5**	**—**	**—**	**3300**	**0.2**	**175**	**300**	**100–0.1**	**5**	**N, Q, R**	**C, I, M/**	**High Speed, Low Power**	**9–258**
AD9622	**5.5**	**3.8**	**12**	**7000**	**2**	**450**	**1500**	**14–0.01**	**2**	**N, Q, R**	**I, M**	**Fast Pulse Response; Wide BW**	**9–312**
OP176	**6.0**	**6.0**	**0.5**	**175**	**1.0**	**10**	**25**	**1000–0.01**	**1**	**N, R**	**I**	**Bipolar/JFET Audio Op Amp**	**9–397**
OP471	**6.5**	**6.5**	**0.4**	**7**	**0.25**	**6.5**	**8**	**—**	**1**	**E, N, Q, R**	**I, M/DS**	**Quad Monolithic, Fast**	**9–560**
AD9621	**6.6**	**5.5**	**8.2**	**7000**	**2**	**350**	**1200**	**11–0.01**	**1**	**N, Q, R**	**I, M**	**Fast Pulse Response; Wide BW**	**9–309**
AD795	**11**	**9**	**0.0006**	**0.001**	**0.1**	**2**	**1**	**11,000–0.01**	**1**	**N, R**	**C**	**Low Power, Low Noise Photo Diode Preamp**	**9–64**
OP271	**7.6**	**7.6**	**0.6**	**4**	**0.075**	**5**	**8.5**	**—**	**1**	**E, N, Q, R**	**I, M/DS**	**Dual Monolithic, Fast**	**9–451**
AD645	**9**	**8**	**0.0006**	**0.0007**	**0.1**	**2**	**2**	**—**	**1**	**H, N**	**C, I, M**	**FET Input, Low I_B, OPA111 Second Source**	**9–34**

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Low Current Noise, Low Input Bias Current Amplifiers

Model	I_B pA max	I_N f=1 kHz $f_A/\sqrt{Hz}$	Input Impedance Differential Ω‖pF typ	Input Impedance Common Mode Ω‖pF typ	CMRR dB f=1 kHz typ	V_{OS} mV max	V_{OS} TC µV/°C max	BW MHz typ[1]	Package Options[2]	Temp Ranges[3]	Comments	Page[4]
AD549	**0.06–0.25**	**0.11**	**10^{13}‖1**	**10^{15}‖0.8**	**62**	**0.25–1**	**5–20**	**1**	**H**	**C, M/**	**Monolithic, Lowest I_B**	**9–28**
AD515A	0.075–0.3	—	10^{13}‖1.6	10^{15}‖0.8	62	1–3	15–50	1	H	C	Lower Cost AD515 Replacement	A 2–45
OP80	0.25–1	—	—		90	1.5	—	0.3	N, R, H	I, M	Low Cost CMOS	A 2–727
AD546	**0.5–1**	**0.4**	**10^{13}‖1**	**10^{15}‖0.8**	**90**	**1–2**	**20**	**1**	**N**	**C**	**Low Cost 1 pA Amplifier**	**9–22**
AD545A	1–2	—	10^{13}‖1.6	10^{15}‖0.8	62	0.25–1	3–25	1	H	C	Lower Cost AD545 Replacement	A 2–65
AD795	**1–3**	**0.6**	**10^{12}‖2**	**10^{14}‖2.2**	**110**	**0.25–0.5**	**10**	**2**	**N, R**	**C**	**Low Power, Low Noise, Photodiode Preamp**	**9–64**
AD645	**1.5–3**	**0.6**	**10^{13}‖1**	**10^{14}‖3**	**94**	**0.25–0.5**	**1–5**	**2**	**N, H**	**C, I, M**	**Low Noise, Precision BiFET, (OPA111 Second Source)**	**9–34**
OP41	5–20	—	—		98	0.25–2	5–10	0.5	N, R, H	C, I, M/	High Stability JFET	A 2–645
AD548	**10–20**	**1.8**	**10^{12}‖3**	**3×10^{12}‖3**	**84**	**0.25–2**	**2–20**	**1**	**N, Q, R, H**	**C, I, M/**	**Low Power, Low Cost**	**9–25**
AD648	**10–20**	**1.8**	**10^{12}‖3**	**3^{12}‖3**	**84**	**0.3–2**	**3–20**	**1**	**N, Q, R, H**	**C, I, M/**	**Dual AD548**	**9–37**
AD820	**20–30**	**1.8**	**—**	**—**	**100**	**0.25–1**	**5–10**	**2**	**N, Q, R**	**C, I, M**	**Single Supply, Fast, Rail-to-Rail**	**9–170**
AD822	**20–30**	**1.8**	**—**	**—**	**100**	**0.25–1**	**5–10**	**2**	**N, Q, R**	**C, I, M**	**Dual AD820**	**9–170**
AD542	**25–50**	**—**	**—**	**—**	**80**	**0.5–2**	**5–20**	**1**	**H**	**C, M**	**Precision**	**9–19**
AD544	**25–50**	**—**	**—**	**—**	**80**	**0.5–2**	**5–20**	**2**	**H**	**C, M**	**Precision, Low Distortion**	**9–19**
AD711	**25–50**	**10**	**3×10^{12}‖5.5**	**3×10^{12}‖5.5**	**62**	**0.25–2**	**3–20**	**4**	**N, Q, R, H**	**C, I, M/**	**Low Cost BiFET, Excellent AC and DC Performance**	**9–47**
AD642	**35–75**	**—**	**10^{12}‖6**	**10^{12}‖6**	**90**	**0.5–2**	**—**	**1**	**H**	**C, M/**	**Dual Precision**	**9–31**
PM156A	50	10	—		90	2	5	4.5	Q, H	C, $M/_{JS}$	Improved Industry Standard	A 2–1065
PM157A	50	10	—		90	2	5	20	Q, H	C, $M/_{DS}$	Improved Industry Standard	A 2–1065
AD712	**50–75**	**10**	**3^{12}‖5.5**	**3^{12}‖5.5**	**94**	**0.3–3**	**5–20**	**4**	**N, Q, R, H**	**C, I, M/**	**Dual AD711**	**9–47**
AD744	**50–100**	**10**	**3×10^{12}‖5.5**	**3×10^{12}‖5.5**	**88**	**0.25–1**	**3–20**	**13**	**H, N, Q, R**	**C, I, M**	**Fast Settling BiFET**	**9–55**
OP15	50–200	10	—		90	0.5–3	5–15	6	N, Q, R, H	C, I, $M/_{DS}$	Precision BiFET	A 2–571
OP16	50–200	10	—		90	0.5–3	5–15	8	N, Q, R, H	C, I, $M/_{DS}$	Precision BiFET	A 2–571
OP17	50–200	10	—		90	0.5–3	5–15	30	N, Q, R, H	C, I, $M/_{DS}$	Fast, Precision BiFET	A 2–571
OP42	**200–250**	**7**	**10^{12}‖6**		**98**	**0.75–5**	**10**	**10**	**E, H, N, R, Q**	**I, M**	**Fast, Precision BiFET**	**9–365**

[1]Unity gain small signal bandwidth.
[2]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP–Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP–Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[3]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[4]A = *Amplifier Reference Manual*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Selection Guides—Operational Amplifiers

Precision Amplifiers

Model	V_{OS} μV max	V_{OS} TC μV/°C max	Noise μV p-p 0.1–10 Hz typ	GBW MHz typ	Slew Rate V/μs typ	I_B nA max	CMRR dB f = 1 kHz typ	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
OP177	**10–60**	**0.1–1.2**	**0.35**	**0.6**	**0.3**	**1.5–2.8**	**110**	**N, Q, R**	**I, M/**	**Highest Precision**	**9–415**
AD707	**15–90**	**0.1–1.0**	**0.23**	**0.9**	**0.3**	**1.0–2.5**	**100**	**H, N, Q, R**	**C, I, M/**	**High Precision**	**9–44**
OP77	**25–100**	**0.3–1.2**	**0.35**	**0.6**	**0.3**	**2–2.8**	**105**	**E, H, N, Q, R**	**C, I, $M/_{DS}$**	**Next Generation OP07**	**9–370**
AD705	**25–90**	**0.6–1.2**	**0.5**	**0.8**	**0.15**	**0.1–0.15**	**110**	**N, Q, R**	**C, I, M**	**Low I_B Precision Bipolar**	**9–40**
OP97	**25–75**	**0.6–2**	**0.5**	**0.9**	**0.2**	**0.1–0.15**	**100**	**E, H, N, Q, R**	**I, $M/_{DS}$**	**Low Power OP07**	**9–379**
OP27	**25–100**	**0.6–1.8**	**0.08**	**8**	**2.8**	**40–80**	**125**	**E, H, N, Q, R**	**C, I, $M/_{JS}$**	**Low Noise, Precision**	**9–357**
OP37	**25–100**	**0.6–1.8**	**0.08**	**63**	**17**	**40–80**	**125**	**E, H, N, Q, R**	**C, I, $M/_{DS}$**	**Fast, Low Noise, Precision $A_{VCL} \geq 5$**	**9–361**
OP07	**25–150**	**0.6–2.5**	**0.35**	**0.6**	**0.3**	**2–12**	**98**	**E, H, N, Q, R**	**C, I, $M/_{DJS}$**	**Low Offset Voltage**	**9–352**
AD846	**25–200**	**0.8–5.0**	**—**	**75–450**	**450**	**250**	**—**	**N, Q**	**I, $M/_{DS}$**	**High Precision, High Speed**	**9–251**
AD708	**30–100**	**0.3–1.0**	**0.23**	**0.9**	**0.3**	**1.0–2.5**	**100**	**H, N, Q**	**C, I, M/**	**Dual AD707**	**9–44**
AD797	**40–100**	**0.8–1.5**	**0.05**	**100**	**18**	**50–1000 (typ)**	**130**	**N, Q, R**	**I, M**	**Ultralow Noise, Low Distortion Amp**	**9–78**
AD706	**50–100**	**0.5–1.0**	**0.5**	**0.8**	**0.15**	**0.11–0.20**	**110**	**N, Q, R**	**C, I**	**Dual AD705**	**9–40**
OP497	**50–150**	**0.5–1.5**	**0.3**	**0.5**	**0.15**	**0.1–0.2**	**130**	**E, N, Q, R**	**I, M/**	**Quad Precision, Low I_B**	**9–568**
OP297	**50–200**	**0.6–2**	**0.3**	**0.5**	**0.15**	**0.1–0.2**	**105**	**N, Q, R**	**I, $M/_S$**	**Dual Precision, Low Power, Low I_B**	**9–530**
OP113	**75–150**	**0.8–1.5**	**0.12**	**3.4**	**1.2**	**50**	**116**	**N, Q, R**	**I**	**Single Supply, Low Noise**	**9–382**
AD704	**75–150**	**1.0–1.5**	**0.5**	**0.8**	**0.1**	**0.15–0.27**	**110**	**N, Q, R**	**C, I, M**	**Quad AD705**	**9–40**
OP200	**75–200**	**0.5–2**	**0.5**	**0.5**	**0.15**	**2–5**	**110**	**E, N, Q, R**	**I, $M/_{DS}$**	**Dual Monolithic, Precision**	**9–432**
OP270	**75–250**	**1–3**	**0.08**	**5**	**2.4**	**20–60**	**115**	**E, N, Q, R**	**I, $M/_{DS}$**	**Dual Monolithic, Low Power**	**9–447**
OP227	80–180	1–1.8	0.08	8	2.8	40–80	125	Q	I, $M/_{DS}$	Dual Matched, Low Noise	A 2–835
OP207	100–200	1.3–1.8	0.35	0.6	0.2	3–7	98	Q	C, $M/_{DS}$	Dual Matched, Precision	A 2–813
OP213	**100–250**	**0.8–1.5**	**0.12**	**3.4**	**1.2**	**50**	**116**	**N, Q, R**	**I**	**Dual Single Supply, Low Noise**	**9–382**
OP413	**125–275**	**0.8–1.5**	**0.12**	**3.4**	**1.2**	**50**	**116**	**N, Q, R**	**I**	**Quad Single Supply, Low Noise**	**9–382**
AD844	**150–300**	**5**	**—**	**900**	**2000**	**250**	**—**	**N, Q, R**	**I, $M/_S$**	**Precision, High Speed**	**9–245**
OP400	**150–300**	**1.2–2.5**	**0.5**	**0.5**	**0.15**	**3–7**	**110**	**E, N, Q, R**	**C, I, $M/_S$**	**Quad, Monolithic, Precision**	**9–534**
OP90	**150–450**	**2–5**	**3**	**—**	**—**	**15–25**	**80**	**E, N, Q, R**	**I, $M/_S$**	**Micropower, Low Voltage, Single Supply**	**9–375**
OP221	**150–500**	**1.5–3**	**—**	**0.6**	**0.3**	**80–120**	**60**	**H, N, Q, R**	**C, I, $M/_S$**	**Dual Low Power, Single Supply**	**9–439**
OP220	**150–750**	**1.5–3**	**—**	**0.2**	**0.05**	**20–30**	**30**	**H, N, Q, R**	**C, I, $M/_S$**	**Dual Micropower, Single Supply**	**9–436**
OP05	150–1600	0.9–4.5	0.38	0.8	0.3	2.9	—	H, N, Q	C, M/	Instrumentation Amplifier	A 2–519
OP271	**200–400**	**2–5**	**—**	**5**	**8.5**	**20–60**	**125**	**E, N, Q, R**	**I, $M/_{DS}$**	**Dual, Fast, Low Noise**	**9–451**

Model	V_{OS} μV max	V_{OS} TC μV/°C max	Noise μV p-p 0.1–10 Hz typ	GBW MHz typ	Slew Rate V/μs typ	I_B nA max	CMRR dB f = 1 kHz typ	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
OP290	**200–500**	**3–5**	**3**	**0.02**	**—**	**15–25**	**100**	**N, Q, E, R**	**I, $M/_{DS}$**	**Dual Micropower, Low Voltage Single Supply**	**9–477**
OP467	**200–1000**	**3.5**	**6**	**30**	**170**	**—**	**80**	**N, Q, P, R**	**C, I, M**	**Quad High Speed**	**9–541**
AD795	**250–500**	**1–10**	**1**	**2**	**1**	**0.001–0.004**	**110**	**N, R, H**	**C, I, M**	**Low Power, Low Noise FET**	**9–64**
OP20	250–1000	1.5–7	—	0.1	0.05	25–40	30	N, Q, R, H	C, I, M/	Micropower, Single Supply	A 2–585
AD744	**250–1000**	**3–20**	**2**	**13**	**75**	**0.05–0.1**	**100**	**H, N, Q, R**	**C, I, M**	**Fast Settling BiFET**	**9–55**
AD820	**250–1000**	**5–10**	**2**	**2**	**3.75**	**0.02–0.03**	**100**	**N, Q, R**	**C, I, M**	**Single Supply, Rail-to-Rail, FET Input**	**9–170**
AD822	**250–1000**	**5–10**	**2**	**2**	**3.75**	**0.02–0.03**	**100**	**N, Q, R**	**C, I, M**	**FET Dual AD820**	**9–170**
AD711	**250–2000**	**3–20**	**2**	**4**	**20**	**0.025–0.050**	**94**	**N, Q, R, H**	**C, I, M/**	**Precision, High Speed**	**9–47**
AD548	**250–2000**	**2–20**	**2**	**1**	**1.8**	**0.01–0.02**	**83**	**N, Q, R, H**	**C, I, M/**	**Low Power BiFET**	**9–25**
OP41	250–2000	5–10	—	0.5	1.3	0.005–0.02	100	N, R, H	C, I, M/	Low I_B	A 2–645
OP22	300–1000	1.5–3	—	0.25	0.08	5–10	60	N, Q, R, H	C, I, M/	Micropower, Programmable	A 2–597
AD648	**300–2000**	**3–20**	**2**	**1**	**1.8**	**0.01–0.02**	**83**	**N, Q, R, H**	**C, I, M/**	**Dual AD548**	**9–37**
AD712	**300–3000**	**5–20**	**2**	**4**	**20**	**0.05–0.075**	**94**	**N, Q, R, H**	**C, I, M/**	**Dual AD711**	**9–47**
OP470	**400–1000**	**2–4**	**0.08**	**6**	**2**	**25–60**	**110**	**N, Q, E, R**	**C, I, $M/_{DS}$**	**Quad, Low Noise**	**9–556**
AD713	**500–1500**	**15–20**	**2**	**4**	**20**	**0.075–0.150**	**94**	**N, Q, R**	**C, I, $M/_D$**	**Dual AD711**	**9–47**
AD741	500–6000	5–20	—	1	0.5	50–500	100	N, H	C, M/	General Purpose	A 2–213
OP291/491	**700**	**1.1 typ**	**2**	**3**	**0.4**	**50**	**90**	**N, R**	**I**	**Dual, Quad, Rail-to-Rail, 2.7 V**	**9–481**
OP471	**800–1800**	**4–7**	**0.25**	**6.5**	**8**	**25–60**	**108**	**N, Q, E, R**	**C, I, $M/_{DS}$**	**Quad, Fast, Low Noise**	**9–560**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.

[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.

[3]A = *Amplifier Reference Manual*. All other entries refer to this volume.

Boldface Type: Data sheet information in this volume.

Selection Guides—Operational Amplifiers

Low Power/Micropower Amplifiers

Model	ISY max mA	V_{OS} max mV	I_B max nA	GBW typ MHz	SR typ V/μs	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
OP22	0.0002–0.4	0.3–1	5–10	0.25	0.08	H, M, N, Q, R	I, M/	Programmable, Single Supply	A 2–597
OP90	**0.02**	**0.15–0.45**	**15–25**	**0.02**	**—**	**E, N, Q, E**	**I, $M/_S$**	**Micropower, Low Voltage Single Supply**	**9–375**
OP290	**0.04**	**0.2–0.5**	**15–25**	**0.02**	**—**	**E, N, Q, E**	**I, $M/_{DS}$**	**Dual, Micropower, Low Voltage, Single Supply**	**9–477**
OP20	0.08	0.25–1	25–40	0.1	0.05	E, N, Q, R	I, M/	Micropower, Single Supply, Low Cost	A 2–585
OP490	**0.08**	**0.5–1**	**15–25**	**0.02**	**—**	**E, N, Q, R**	**I, $M/_{DS}$**	**Quad, Micropower, Low Voltage, Single Supply**	**9–564**
OP220	**0.17**	**0.15–0.75**	**20–30**	**0.2**	**0.05**	**H, N, Q, R**	**I, $M/_S$**	**Dual, Low Cost, Micropower, Single Supply**	**9–436**
AD548	**0.2**	**0.25–0.2**	**0.01–0.02**	**1.0**	**1.8**	**H, N, Q**	**C, I, M/**	**Precision Low Power BiFET Op Amp**	**9–25**
OP295	**0.3**	**0.2–0.5**	**15**	**0.085**	**0.04**	**N, R**	**I, M**	**Dual Rail-to-Rail**	**9–518**
OP80	0.325	1.5	0.00025–0.001	0.3	0.4	H, N, R	I, M	Low I_B, CMOS	A 2–727
OP420	**0.36**	**2.5–6**	**20–40**	**0.15**	**0.05**	**E, N, Q, R**	**I, $M/_S$**	**Quad, Low Cost, Micropower, Single Supply**	**9–538**
OP21	0.3–0.4	0.1–0.5	100–150	0.6	0.25	H, N, Q, R	I, M/	Low Cost, Low Power, Single Supply	A 2–591
OP291/491	**0.35**	**0.7**	**50**	**3**	**0.4**	**N, R**	**I**	**Rail-to-Rail, 2.7 V Supply**	**9–481**
OP282	**0.5**	**2.0**	**0.1**	**4**	**9**	**N, Q, R**	**I**	**Dual, High Speed, Low Power**	**9–461**
AD648	**0.4**	**0.4–2.0**	**0.005–.01**	**1.0**	**1.8**	**H, N, Q**	**C, I, M/**	**Dual, Precision Low Power BiFET Op Amp**	**9–37**
OP97	**0.6**	**0.025–0.075**	**0.1–0.15**	**0.9**	**0.2**	**E, H, N, Q, R**	**I, $M/_{DS}$**	**Precision, Low I_B**	**9–379**
AD705	**0.6**	**0.025–0.09**	**0.1–0.15**	**0.8**	**0.15**	**N, Q, R**	**C, I, M**	**Picoampere Input Current Bipolar Op Amp**	**9–40**
AD820	**0.66**	**0.25–1**	**0.02–0.03**	**2**	**3.75**	**N, Q, R**	**C, I, M**	**Fast, Single Supply, Rail-to-Rail FET Input**	**9–170**
OP221	**0.8**	**0.15–0.5**	**80–120**	**0.6**	**0.3**	**H, N, Q, R**	**I, $M/_S$**	**Dual, Low Cost, Low Power, Single Supply**	**9–439**
OP41	1	0.25–2	0.005–0.02	0.5	1.3	N, Q, R	I, M/	Low Power, Low I_B	A 2–645
OP482	**1.0**	**3.0**	**0.1**	**4**	**9**	**N, P, Q, R**	**I**	**Quad, High Speed, Low Power**	**9–461**
AD706	**1.2**	**0.05–0.1**	**0.11–0.2**	**0.8**	**0.15**	**N, Q, R**	**C, I, M**	**Dual, Picoampere Input Current Bipolar Op Amp**	**9–40**
OP297	**1.25**	**0.05–0.2**	**0.1–0.2**	**0.5**	**0.15**	**E, N, Q, R**	**I, $M/_S$**	**Dual, Precision, Low I_B**	**9–530**
AD822	**1.3**	**0.25–1**	**0.02–0.03**	**2**	**3.75**	**N, Q, R**	**C, I, M**	**Dual AD820**	**9–170**
OP200	**1.45**	**0.075–0.2**	**2–5**	**0.5**	**0.15**	**E, N, Q, R**	**I, $M/_{DS}$**	**Dual, Precision**	**9–432**
OP183/283	**1.5**	**1.0**	**600**	**5**	**10**	**N, R**	**I**	**5 MHz, Low Noise, Single/Dual**	**9–420**
OP421	1.8	2.5–6	50–150	1.9	0.5	N, Q, R	I, $M/_D$	Quad, Low Cost, Low Power, Single Supply	A 2–993
OP113/213/413	**2.0**	**0.075–0.275**	**50**	**3.4**	**1.2**	**N, Q, R**	**I**	**Low Noise, Low Drift, Single/Dual/Quad**	**9–382**
AD704	**2.4**	**0.075–0.150**	**0.15–0.17**	**1.0**	**0.15**	**N, Q, R**	**C, I, M**	**Quad, Picoampere Input Current Bipolar Op Amp**	**9–40**
OP02	2.4	0.5–5	30–100	1.3	0.5	H, N, Q	C, M/	Improved 741	A 2–503
OP400	**2.9**	**0.15–0.3**	**3–7**	**0.5**	**0.15**	**E, N, Q, R**	**C, I, $M/_{DS}$**	**Quad, Precision**	**9–534**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]A = *Amplifier Reference Manual*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Dual Operational Amplifiers

Model	V_{OS} mV max	V_{OS} TC µV/°C max	I_B nA max	BW MHz typ[1]	Slew Rate V/µs typ	Settling Time to 0.01% µs typ	Package Options[2]	Temp Ranges[3]	Comments	Page[4]
AD708	**0.03–0.1**	**0.3–1.0**	**1–2.5**	**0.9**	**0.3**		**H, N, Q**	**C, I, M/**	**Highest DC Precision; Excellent Matching Between Amps, Dual AD707**	**9–44**
AD706	**0.05–0.10**	**0.6–1.5**	**0.11–0.200**	**0.8**	**0.15**	**—**	**N, Q, R**	**C, I**	**Dual AD705, Low I_B Precision Bipolar**	**9–40**
OP297	**0.05–0.2**	**0.6–2**	**0.1–0.2**	**0.5**	**0.15**	**—**	**N, Q, R**	**I, M/$_S$**	**Precision, Low Power, Low I_B**	**9–530**
OP200	**0.075–0.2**	**0.5–2**	**2–5**	**0.5**	**0.15**	**—**	**E, N, Q, R**	**I, M/$_{DS}$**	**Dual Monolithic, Precision**	**9–432**
OP270	**0.075–0.25**	**1–3**	**20–60**	**5**	**2.4**	**—**	**E, N, Q, R**	**I, M/$_{DS}$**	**Dual Monolithic, Low Noise**	**9–447**
OP227	0.08–0.18	1–1.8	40–80	8	2.8	—	Q	I, M/$_{DS}$	Dual Matched, Low Noise	A 2–843
OP207	0.1–0.2	1.3–1.8	3–7	0.6	0.2	—	Q	C, M/$_{DS}$	Dual Matched, Precision	A 2–813
OP213	**0.1–0.25**	**0.8–1.5**	**50**	**3.4**	**1.2**	**9**	**N, Q, R**	**I**	**Low Noise, Low Drift, Single Supply**	**9–382**
OP221	**0.15–0.5**	**1.5–3**	**80–120**	**0.6**	**0.3**	**—**	**H, N, Q, R**	**C, I, M/$_S$**	**Low Power, Single Supply**	**9–439**
OP220	**0.15–0.75**	**1.5–3**	**20–30**	**0.2**	**0.05**	**—**	**H, N, Q, R**	**C, I, M$_S$**	**Micropower, Single Supply**	**9–436**
OP271	**0.2–0.4**	**2–5**	**20–60**	**5**	**8.5**	**—**	**E, N, Q, R**	**I, M/$_{DS}$**	**Dual Monolithic, Fast, Low Noise**	**9–451**
OP290	**0.2–0.5**	**3–5**	**15–25**	**0.02**	**—**	**—**	**E, N, Q, R**	**I, M/$_{DS}$**	**Micropower, Low Voltage Single Supply**	**9–477**
OP295	**0.2–0.5**	**<10**	**15**	**0.085**	**0.04**	**—**	**N, R**	**I, M**	**Rail-to-Rail**	**9–518**
OP285	**0.25**	**—**	**150**	**8**	**20**	**—**	**N, Q, R**		**Dual High Performance, Low Power**	**9–464**
AD822	**0.25–1**	**5–10**	**0.02–0.03**	**2**	**3.75**	**—**	**N, Q, R**	**C, I, M**	**Single Supply, Rail-to-Rail, Fast FET Input**	**9–170**
AD746	**0.5–1**	**10–20**	**0.15**	**13**	**75**	**0.5**	**N, Q, R**	**C, I, M/**	**Precision, Fast Settling, Dual AD744**	**9–61**
AD648	**0.3–2**	**3–20**	**0.01–0.02**	**1**	**1.8**	**8**	**H, N, Q, R**	**C, I, M/**	**Low Power, BiFET, Dual AD548**	**9–37**
AD712	**0.3–3**	**5–20**	**0.05–0.075**	**4**	**20**	**1**	**H, N, Q, R**	**C, I, M/**	**Excellent AC and DC Performance, Dual AD711**	**9–47**
OP249	**0.5–0.7**	**5–6**	**0.05–0.075**	**4.7**	**22**	**0.9**	**E, H, N, Q, R**	**I, M/$_S$**	**Fast, Low Distortion**	**9–442**
AD642	**0.5–2**	**1–3.5**	**0.035–0.075**	**1**	**3**	**—**	**H**	**C, M/**	**Dual AD542**	**9–31**
AD644	**0.5–2**	**—**	**0.035–0.075**	**2**	**13**	**—**	**H**	**C, M/**	**Dual AD544**	**9–31**
OP291	**0.7**	**1.1 typ**	**50**	**3**	**0.4**	**22**	**N, R**	**I**	**Rail-to-Rail, 2.7 V Supply, Low Power**	**9–481**
OP15	0.75–5	8–20	50–100	1.3	0.5	—	H, N, Q, R	I, M/$_{DS}$	Improved "1458" Dual	A 2–571
OP275	**1**	**—**	**350**	**9**	**22**	**—**	**N, R**		**Dual Audio Amp**	**9–454**
OP283	**1.0**	**4 typ**	**600**	**5**	**10**	**1.5**	**N, R**	**I**	**Low Power, Single Supply**	**9–420**
AD828	**2**	**10 typ**	**6600**	**130**	**450**	**0.08**	**N, R**	**I**	**Low Power Video Amp**	**9–203**
OP215	1–4	10	0.1–0.3	5.7	18	0.9–0.1%	E, H, N, Q, R	C, I, M/$_{DS}$	High Speed, Precision	A 2–819
OP282	**2.0**	**10**	**0.1**	**4.0**	**9**	**1.5**	**N, Q, R**	**I**	**Dual High Speed, Low Power**	**9–461**
AD827	**4.0**	**15**	**7000**	**50**	**300**	**0.120–0.1%**	**N, Q, R**	**C, I, M/$_D$**	**Dual AD847, High Speed, Low Power**	**9–200**
OP279	**4.0**	**4 typ**	**600**	**2**	**5**	**—**	**N, R**	**I**	**Rail-to-Rail, Single Supply, 50 mA Out**	**9–459**
OP260	3.5–7	10	1000–15000	90	1000	0.25–0.1%	E, H, N, Q, R	I, M/$_{DS}$	Dual High Speed, Current Feedback	A 2–873
AD812	**5**	**15 typ**	**1000–20000**	**145**	**1600**	**0.05–0.1%**	**N, R**	**I**	**Dual Current Feedback, Low Power**	**9–110**
AD8002	**5.5**	**10 typ**	**6000–25000**	**880**	**1200**	**0.01–0.1%**	**N, Q, R**	**I**	**880 MHz, Low Power**	**9–278**

[1]Unity gain small signal bandwidth.
[2]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[3]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
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Selection Guides—Operational Amplifiers

Quad Operational Amplifiers

Model	V_{OS} mV max	V_{OS} TC μV/°C max	I_B nA max	BW MHz typ[1]	Slew Rate V/μs typ	Settling Time to 0.01% μs typ	Package Options[2]	Temp Ranges[3]	Comments
AD704	0.075–0.10	1.0–1.5	150–270	0.8	0.10	—	N, Q, R	C, I, M	Quad AD705, Low I_B Precision Bipolar
OP497	0.05–0.15	0.5–1.5	150–200	0.5	0.15	—	E, N, Q, R	I, M/	Low Power, Low I_B Precision Bipolar
OP413	0.125–0.275	0.8–1.5	50	3.4	1.2	9	N, Q, R	I	Low Noise, Low Drift, Single Supply
OP400	0.15–0.3	1.2–2.5	3–7	0.5	0.15	—	E, N, Q, R	C, I, M/$_D$	Quad Monolithic, Precision
OP495	0.2–0.5	<10	15	0.085	0.04	—	N, Q, R	I, M	Rail-to-Rail
OP470	0.4–1	2–4	25–60	6	2	—	E, N, Q, R	C, I, M/$_{DS}$	Quad Monolithic, Low Noise
OP467	0.5	3.5	100	30	170	170	N, P, Q, R		30 MHz, Low Power
OP491	0.7	1.1 typ	50	3	0.4	22	N, R	I	Rail-to-Rail, 2.7 V Supply, Low Power
OP490	0.5–1	5	15–25	0.02	0.012	—	E, N, Q, R	I, M/$_{DS}$	Micropower, Low Voltage, Single Supply
AD713	0.5–1.5	15	35–100	4	20	1	N, Q, R	C, I, M/$_D$	Superior AC and DC Performance, Quad AD711
OP11	0.5–5	10–15	300–500	3	1	—	E, N, Q, R	C, I, M/	Improved Quad "741"
OP471	0.8–1.8	4–7	25–60	6.5	8	—	E, N, Q, R	C, I, M/$_{DS}$	Monolithic, Fast, Low Noise
OP492	2.5	10	700	4	4	—	N, R	I	Single Supply, Low Power, I/O to Ground
OP482	3.0	10	0.1	4.0	9	1.5	N, Q, P, R	I	High Speed, Low Power
OP421	2.5–6	10–15	50–150	1.9	0.5	—	N, Q, R	I, M/	Low Power, Low Cost, Single Supply
OP420	2.5–6	10–25	20–40	0.15	0.05	—	E, N, Q, R	I, M/$_S$	Micropower, Low Cost, Single Supply
AD8004	15	30 typ	15000–25000	400	3000	0.01–0.1%	N, R	I	3000 V/μs, Low Power

Unity Gain Buffers

Model	−3 dB BW MHz typ	SR V/μs min	Settling Time to 0.02% ns typ	Rise Time 1V Step ns typ	I_{OUT} mA min	V_{OS} mV typ	I_{SS} mA max	Package Options[2]	Temp Ranges[3]	Comments
AD9630	750	1800	8	0.9	50	3	26	N, Q, R	I, M/	High Performance, Wide-Band Buffer
AD9620	600	2200	8	0.8	40	2	48	D	I, M	High Performance, Low Harmonic Distortion Buffer
BUF04	110	2000	60 (0.1%)	1.3	40	2	8.5	N, Q, R	I, M	±5 Volt Supply, High Slew
BUF03	50	220	100 (0.1%)	7 (1/2 V)	70	10	25	H	C, M/	High Speed Voltage Follower/Buffer

[1]Unity gain small signal bandwidth.
[2]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic
M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S
Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded C
[3]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerin
temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[4]A = *Amplifier Reference Manual*. All other entries refer to this volume.
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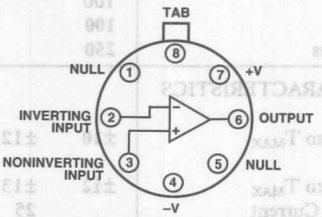
High Performance, BiFET Operational Amplifiers

AD542/AD544/AD547

FEATURES
Ultralow Drift: 1 μV/°C (AD547L)
Low Offset Voltage: 0.25 mV (AD547L)
Low Input Bias Currents: 25 pA max
Low Quiescent Current: 1.5 mA
Low Noise: 2 μV p-p
High Open Loop Gain: 110 dB
High Slew Rate: 13 V/μs
Fast Settling to ±0.01%: 3 μs
Low Total Harmonic Distortion: 0.0025%
Available in Hermetic Metal Can and Die Form
MIL-STD-883B Versions Available
Dual Versions Available: AD642, AD644, AD647

CONNECTION DIAGRAM



NOTE: PIN 4 CONNECTED TO CASE

PRODUCT DESCRIPTION

The BiFET series of precision, monolithic FET-input op amps are fabricated with the most advanced BiFET and laser trimming technologies. The AD542, AD544, AD547 series offers bias currents significantly lower than currently available BiFET devices, 25 pA max, warmed up.

In addition, the offset voltage is laser trimmed to less than 0.25 mV on the AD547L, which is achieved by utilizing Analog Devices' exclusive laser wafer trimming (LWT) process. When combined with the AD547's low offset drift (1 μV/°C), these features offer the user performance superior to existing BiFET op amps at low BiFET pricing.

The AD542 or AD547 is recommended for any operational amplifier application requiring excellent dc performance at low to moderate cost. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common-mode rejection (80 dB, min on the "K" and "L" grades) and high open-loop gain, even under heavy loading, ensures better than "12-bit" linearity in high impedance buffer applications.

The AD544 is recommended for any op amp applications requiring excellent ac and dc performance at low cost. The 2 MHz bandwidth and low offset of the AD544 make it the first choice as an output amplifier for current output D/A converters, such as the AD7541, 12-bit CMOS DAC.

Devices in this series are available in four grades: the "J," "K," and "L" grades are specified over the 0°C to +70°C temperature range and the "S" grade over the –55°C to +125°C operating temperature range. All devices are offered in the hermetically sealed, TO-99 metal can package.

PRODUCT HIGHLIGHTS

1. Improved bipolar and JFET processing results in the lowest bias current available in a monolithic FET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the device will meet its published specifications in actual use.
3. Advanced laser wafer trimming techniques reduce offset voltage drift to 1 μV/°C max and offset voltage to only 0.25 mV max on the AD547L.
4. Low voltage noise (2 μV p-p) and low offset voltage drift enhance performance as a precision op amp.
5. High slew rate (13 V/μs) and fast settling time to 0.01% (3 μs) make the AD544 ideal for D/A, A/D, sample-hold circuits and high speed integrators.
6. Low harmonic distortion (0.0025%) make the AD544 an ideal choice in audio applications.
7. Bare die are available for use in hybrid circuit applications.

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD542/AD544/AD547–SPECIFICATIONS (V_S = ±15 V @ T_A = +25°C unless otherwise noted)

Parameter	AD542 Min	AD542 Typ	AD542 Max	AD544 Min	AD544 Typ	AD544 Max	AD547 Min	AD547 Typ	AD547 Max	Units
OPEN-LOOP GAIN[1]										
V_{OUT} = ±10 V, R_L = 2 kΩ										
J Grade	100			30			100			V/mV
K, L, S Grades	250			50			250			V/mV
T_A = T_{MIN} to T_{MAX}										
J Grade	100			20			100			V/mV
S Grade	100			20			100			V/mV
K, L Grades	250			40			250			V/mV
OUTPUT CHARACTERISTICS										
R_L = 2 kΩ										
T_A = T_{MIN} to T_{MAX}	±10	±12		±10	±12		±10	±12		V
R_L = 10 kΩ										
T_A = T_{MIN} to T_{MAX}	±12	±13		±12	±13		±12	±13		V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1.0			2.0			1.0		MHz
Full Power Response		50			200			50		kHz
Slew Rate, Unity Gain	2.0	3.0		8.0	13.0		2.0	3.0		V/µs
Total Harmonic Distortion					0.0025					%
INPUT OFFSET VOLTAGE[2]										
J Grade			2.0			2.0			1.0	mV
K Grade			1.0			1.0			0.5	mV
L Grade			0.5			0.5			0.25	mV
S Grade			1.0			1.0			0.5	mV
vs. Temperature[3]										
J Grade			20			20			5	µV/°C
K Grade			10			10			2	µV/°C
L Grade			5			5			1	µV/°C
S Grade			15			15			5	µV/°C
vs. Supply, T_A = T_{MIN} to T_{MAX}										
J Grade			200			200			200	µV/V
K, L, S Grades			100			100			100	µV/V
INPUT BIAS CURRENT[4]										
Either Input										
J Grade			50			50			50	pA
K, L, S Grades		10	25		10	25		10	25	pA
Input Offset Current										
J Grade		5	15		5	15		5	15	pA
K, L, S Grades		2	15		2	15		2	15	pA
INPUT IMPEDANCE										
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		Ω|pF
Common Mode		$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$		Ω|pF
INPUT VOLTAGE[5]										
Differential		±20			±20			±20		V
Common Mode	±10	±12		±10	±12		±10	±12		V
Common-Mode Rejection										
V_{IN} = ±10 V										
J Grade	76			76			76			dB
K, L, S Grades	80			80			80			dB

Parameter	AD542 Min	AD542 Typ	AD542 Max	AD544 Min	AD544 Typ	AD544 Max	AD547 Min	AD547 Typ	AD547 Max	Units
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	V
Quiescent Current		1.1	1.5		1.8	2.5		1.1	1.5	mA
VOLTAGE NOISE										
0.1 Hz to 10 Hz										
J Grade		2.0			2.0			2.0		μV p-p
K, L, S Grades		2.0			2.0				4.0	μV p-p
10 Hz		70			35			70		$nV/\sqrt{Hz}$
100 Hz		45			22			45		$nV/\sqrt{Hz}$
1 kHz		30			18			30		$nV/\sqrt{Hz}$
10 kHz		25			16			25		$nV/\sqrt{Hz}$
TEMPERATURE RANGE										
Operating, Rated Performance										
J, K, L Grades		0 to +70			0 to +70			0 to +70		°C
S Grade		–55 to +125			–55 to +125			–55 to +125		°C
Storage		–65 to +150			–65 to +150			–65 to +150		°C
TRANSISTOR COUNT		29			29			29		

NOTES

[1]Open-Loop Gain is specified with V_{OS} both nulled and unnulled.

[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3 μV/°C/mV of nulled offset.

[4]Bias Current specifications are guaranteed at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10 V from ground.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ORDERING GUIDE

Model	Initial Offset Voltage	Offset Voltage Drift	Settling Time to ±0.012% for a 10 V Step	Package Description	Package Option*
AD542JCHIPS	2.0 mV	20 μV/°C	5 μs	Bare Die	
AD542JH	2.0 mV	20 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD542KH	1.0 mV	10 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD542LH	0.5 mV	5 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD542SH	1.0 mV	15 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD542SH/883B	1.0 mV	15 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD544JH	2.0 mV	20 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD544KH	1.0 mV	10 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD544LH	0.5 mV	5 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD544SH	1.0 mV	15 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD544SH/883B	1.0 mV	15 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD547JH	1.0 mV	5 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD547KH	0.5 mV	2 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD547LH	0.25 mV	1 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD547SCHIPS	0.5 mV	5 μV/°C	5 μs	Bare Die	
AD547SH/883B	0.5 mV	5 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A

*For outline information see Package Information section.

1 pA Monolithic Electrometer Operational Amplifier

AD546*

FEATURES

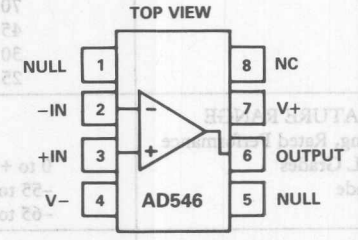
DC PERFORMANCE
- 1 mV max Input Offset Voltage
- Low Offset Drift: 20 μV/°C
- 1 pA max Input Bias Current
- Input Bias Current Guaranteed Over Full Common-Mode Voltage Range

AC PERFORMANCE
- 3 V/μs Slew Rate
- 1 MHz Unity Gain Bandwidth
- Low Input Voltage Noise: 4 μV p–p, 0.1 Hz to 10 Hz
- Available in a Low Cost, 8-Pin Plastic Mini-DIP
- Standard Op Amp Pinout

APPLICATIONS
- Electrometer Amplifiers
- Photodiode Preamps
- pH Electrode Buffers
- Log Ratio Amplifiers

CONNECTION DIAGRAM

8-Pin Plastic
Mini-DIP Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD546 is a monolithic electrometer combining the virtues of low (1 pA) input bias current with the cost effectiveness of a plastic mini-DIP package. Both input offset voltage and input offset voltage drift are laser trimmed, providing very high performance for such a low cost amplifier.

Input bias currents are reduced significantly by using "topgate" JFET technology. The 10^{15} Ω common-mode impedance, resulting from a bootstrapped input stage, insures that input bias current is essentially independent of common-mode voltage variations.

The AD546 is suitable for applications requiring both minimal levels of input bias current and low input offset voltage. Applications for the AD546 include use as a buffer amplifier for current output transducers such as photodiodes and pH probes. It may also be used as a precision integrator or as a low droop rate sample and hold amplifier. The AD546 is pin compatible with standard op amps; its plastic mini-DIP package is ideal for use with automatic insertion equipment.

The AD546 is available in two performance grades, all rated over the 0 to +70°C commercial temperature range, and packaged in an 8-pin plastic mini-DIP.

PRODUCT HIGHLIGHTS

1. The input bias current of the AD546 is specified, 100% tested and guaranteed with the device in the fully warmed-up condition.
2. The input offset voltage of the AD546 is laser trimmed to less than 1 mV (AD546K).
3. The AD546 is packaged in a standard, low cost, 8-pin mini-DIP.
4. A low quiescent supply current of 700 μA minimizes any thermal effects which might degrade input bias current and input offset voltage specifications.

*Covered by Patent No. 4,639,683

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD546J Min	AD546J Typ	AD546J Max	AD546K Min	AD546K Typ	AD546K Max	Units
INPUT BIAS CURRENT[1]								
Either Input	V_{CM} = 0 V		0.2	1		0.2	0.5	pA
Either Input	V_{CM} = ±10 V		0.2	1		0.2	0.5	pA
Either Input @ T_{max}	V_{CM} = 0 V		40			20		pA
Either Input	V_{CM} = ±10 V		40			20		pA
Offset Current	V_{CM} = 0 V		0.17			0.09		pA
Offset Current @ T_{max}	V_{CM} = 0 V		13			7		pA
INPUT OFFSET VOLTAGE[2]								
Initial Offset				2			1	mV
Offset @ T_{max}				3			2	mV
vs. Temp.			20			20		µV/°C
vs. Supply				100			100	µV/V
vs. Supply	T_{min}–T_{max}			100			100	µV/V
Long Term Stability			20			20		µV/month
INPUT VOLTAGE NOISE								
	f = 0.1 Hz to 10 Hz		4			4		µV p–p
	f = 10 Hz		90			90		nV/√Hz
	f = 100 Hz		60			60		nV/√Hz
	f = 1 kHz		35			35		nV/√Hz
	f = 10 kHz		35			35		nV/√Hz
INPUT CURRENT NOISE								
	f = 0.1 Hz to 10 Hz		1.3			1.3		fA rms
	f = 1 kHz		0.4			0.4		fA/√Hz
INPUT IMPEDANCE								
Differential	V_{DIFF} = ±1 V		$10^{13}\|\|1$			$10^{13}\|\|1$		Ω||pF
Common Mode	V_{CM} = ±10 V		$10^{15}\|\|0.8$			$10^{15}\|\|0.8$		Ω||pF
OPEN LOOP GAIN	V_O = ±10 V							
	R_{LOAD} = 10 kΩ	300	1000		300	1000		V/mV
T_{min}–T_{max}	V_O = ±10 V							
	R_{LOAD} = 10 kΩ	300	800		300	800		V/mV
	V_O = ±10 V							
	R_{LOAD} = 2 kΩ	100	250		100	250		V/mV
T_{min}–T_{max}	V_O = ±10 V							
	R_{LOAD} = 2 kΩ	80	200		80	200		V/mV
INPUT VOLTAGE RANGE								
Differential[3]			±20			±20		V
Common-Mode Voltage		−10		+10	−10		+10	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	80	90		84	100		dB
	T_{min} to T_{max}	76	80		76	80		dB
OUTPUT CHARACTERISTICS								
Voltage	R_{LOAD} = 10 kΩ	−12		+12	−12		+12	V
	R_{LOAD} = 2 kΩ	−10		+10	−10		+10	V
Current	Short Circuit	15	20	35	15	20	35	mA
Load Capacitance Stability	Gain = +1		4000			4000		pF

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Model	Conditions	AD546J Min	AD546J Typ	AD546J Max	AD546K Min	AD546K Typ	AD546K Max	Units
FREQUENCY RESPONSE								
Gain BW, Small Signal	G = −1	0.7	1.0		0.7	1.0		MHz
Full Power Response	V_O = 20 V p–p		50			50		kHz
Slew Rate, Unity Gain	G = −1	2	3		2	3		V/μs
Settling Time	to 0.1%		4.5			4.5		μs
	to 0.01%		5			5		μs
Overload Recovery	50% Overdrive Gain = −1		2			2		μs
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±5		±18	±5		±18	V
Quiescent Current			0.60	0.7		0.60	0.7	mA
Transistor Count	# of Transistors		50			50		
PACKAGE OPTIONS[4]								
Plastic Mini-DIP (N-8)			AD546JN			AD546KN		

NOTES

[1]Bias current specifications are guaranteed maximum, at either input, after 5 minutes of operation at T_A = +25°C. Bias current increases by a factor of 2.3 for every 10°C rise in temperature.

[2]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3]Defined as max continuous voltage between inputs, such that neither exceeds ±10 V from ground.

[4]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . 500 mW
Input Voltage[2] . . . . . ±18 V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range . . . . . −65°C to +125°C
Operating Temperature Range . . . . . 0 to +70°C
Lead Temperature Range
(Soldering 60 seconds) . . . . . 300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ESD PRECAUTIONS

Charges as high as 4000 V readily accumulate on the human body and test equipment and discharge without detection. Therefore, reasonable ESD precautions are recommended to avoid functional damage or performance degradation. Unused devices should be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

Precision, Low Power BiFET Op Amp

AD548

FEATURES

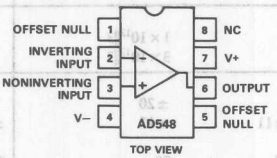
Enhanced Replacement for LF441 and TL061
DC Performance:
- **200μA max Quiescent Current**
- **10pA max Bias Current, Warmed Up (AD548C)**
- **250μV max Offset Voltage (AD548C)**
- **2μV/°C max Drift (AD548C)**
- **2μV p-p Noise, 0.1 to 10Hz**

AC Performance:
- **1.8V/μs Slew Rate**
- **1MHz Unity Gain Bandwidth**

Available in Plastic, Hermetic Cerdip and Hermetic Metal Can Packages and in Chip Form
Available in Tape and Reel in Accordance with EIA-481A Standard
MIL-STD-883B Parts Available
Dual Version Available: AD648
Surface Mount (SOIC) Package Available

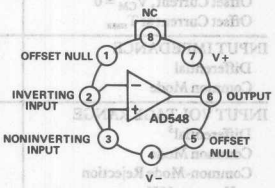
CONNECTION DIAGRAMS

Plastic Mini-DIP (N) Package, Cerdip (Q) Package and SOIC (R) Package

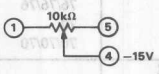


TOP VIEW

TO-99 (H) Package



NOTE: PIN 4 CONNECTED TO CASE



V_{OS} TRIM
TOP VIEW

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PRODUCT DESCRIPTION

The AD548 is a low power, precision monolithic operational amplifier. It offers both low bias current (10pA max, warmed up) and low quiescent current (200μA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD548's entire common-mode voltage range.

The economical J grade has a maximum guaranteed input offset voltage of less than 2mV and an input offset voltage drift of less than 20μV/°C. The C grade reduces input offset voltage to less than 0.25mV and offset voltage drift to less than 2μV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Four additional grades are offered over the commercial, industrial and military temperature ranges.

The AD548 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD548's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common-mode rejection (86dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD548 is pinned out in a standard op amp configuration and is available in six performance grades. The AD548J and AD548K are rated over the commercial temperature range of 0 to +70°C. The AD548A, AD548B and AD548C are rated over the industrial temperature range of −40°C to +85°C. The AD548S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD548 is available in an 8-pin plastic mini-DIP, cerdip, TO-99 metal can, surface mount (SOIC), or in chip form.

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD548 the ideal op amp for high-performance, low-power applications.
2. The AD548 is pin compatible with industry standard op amps such as the LF441, TL061, and AD542, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2mV max) and drift (20μV/°C max) for the AD548J are achieved utilizing Analog Devices' laser drift trimming technology, eliminating the need for external trimming.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. A dual version, the AD648 is also available.
6. Enhanced replacement for LF441 and TL061.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

INPUT OFFSET VOLTAGE										
Initial Offset		0.75	2.0		0.3	0.5		0.10	0.25	mV
T_{min} to T_{max}			3.0/3.0/3.0			0.7/0.8			0.4	mV
vs. Temp.			20			5			2.0	µV/°C
vs. Supply	80			86			86			dB
vs. Supply, T_{min} to T_{max}	76/76/76			80			80			dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT										
Either Input[2], $V_{CM} = 0$		5	20		3	10		3	10	pA
Either Input[2] at T_{max}, $V_{CM} = 0$			0.45/1.3/20			0.25/0.65			0.65	nA
Max Input Bias Current Over Common-Mode Voltage Range			30			15			15	pA
Offset Current, $V_{CM} = 0$		5	10		2	5		2	5	pA
Offset Current at T_{max}			0.25/0.65/10			0.15/0.35			0.35	nA
INPUT IMPEDANCE										
Differential		$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$		Ω|pF
Common Mode		$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$		Ω|pF
INPUT VOLTAGE RANGE										
Differential[3]		±20			±20			±20		V
Common Mode	±11	±12		±11	±12		±11	±12		V
Common-Mode Rejection										
$V_{CM} = \pm 10V$	76	90		82	92		86	98		dB
T_{min} to T_{max}	76/76/76	90		82	92		86	98		dB
$V_{CM} = \pm 11V$	70	84		76	86		76	90		dB
T_{min} to T_{max}	70/70/70	84		76	86		76	90		dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	4.0	µV p-p
f = 10Hz		80			80			80		nV/√Hz
f = 100Hz		40			40			40		nV/√Hz
f = 1kHz		30			30			30		nV/√Hz
f = 10kHz		30			30			30		nV/√Hz
INPUT CURRENT NOISE										
f = 1kHz		1.8			1.8			1.8		fA/√Hz
FREQUENCY RESPONSE										
Unity Gain, Small Signal	0.8	1.0		0.8	1.0		0.8	1.0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain	1.0	1.8		1.0	1.8		1.0	1.8		V/µs
Settling Time to ±0.01%		8			8			8		µs
OPEN LOOP GAIN										
$V_O = \pm 10V$, $R_L \geq 10k\Omega$	300	1000		300	1000		300	1000		V/mV
T_{min} to T_{max}, $R_L \geq 10k\Omega$	300/300/300	700		300	700		300	700		V/mV
$V_O = \pm 10V$, $R_L \geq 5k\Omega$	150	500		150	500		150	500		V/mV
T_{min} to T_{max}, $R_L \geq 5k\Omega$	150/150/150	300		150	300		150	300		V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 10k\Omega$,	±12	±13		±12	±13		±12	±13		V
T_{min} to T_{max}	±12/±12/±12			±12			±12			
Voltage @ $R_L \geq 5k\Omega$,	±11	±12.3		±11	±12.3		±11	±12.3		V
T_{min} to T_{max}	±11/±11/±11			±11			±11			
Short Circuit Current		15			15			15		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		170	200		170	200		170	200	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD548J			AD548K					
Industrial (−40°C to +85°C)		AD548A			AD548B			AD548C		
Military (−55°C to +125°C)		AD548S								
PACKAGE OPTIONS[4]										
Plastic (N-8)		AD548JN			AD548KN					
Cerdip (Q-8)		AD548AQ			AD548BQ					
Metal Can (H-08A)		AD548AH, AD548SH			AD548BH			AD548CQ		
SOIC (R-8)		AD548AR, AD548JR			AD548BR			AD548CH		
Tape and Reel		AD548AR-REEL, AD548JR-REEL			AD548BR-REEL					
Chips Available		AD548J CHIPS								

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperature, the current doubles every 10°C.

[3]Defined as voltages between inputs, such that neither exceeds ±10V from ground.

[4]For outline information see Package Information section.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation[2]	500mW
Input Voltage[3]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (Q, H)	−65°C to +150°C
(N, R)	−65°C to +125°C
Operating Temperature Range	
AD548J/K	0 to +70°C
AD548A/B/C	−40°C to +85°C
AD548S	−55°C to +125°C
Lead Temperature Range (Soldering 60sec)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics

8-Pin SOIC Package: $\theta_{JA} = 160°C/W$, $\theta_{JC} = 42°C/W$

8-Pin Plastic Package: $\theta_{JA} = 90°C/W$

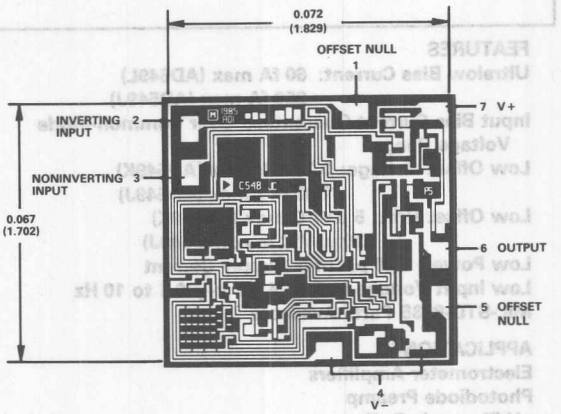
8-Pin Cerdip Package: $\theta_{JC} = 22°C/W$, $\theta_{JA} = 110°C/W$

8-Pin Metal Can Package: $\theta_{JC} = 65°C/W$, $\theta_{JA} = 150°C/W$

[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



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CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although devices feature proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper precautions are recommended to avoid any performance degradation or loss of functionality.

Ultralow Input Bias Current Operational Amplifier

AD549*

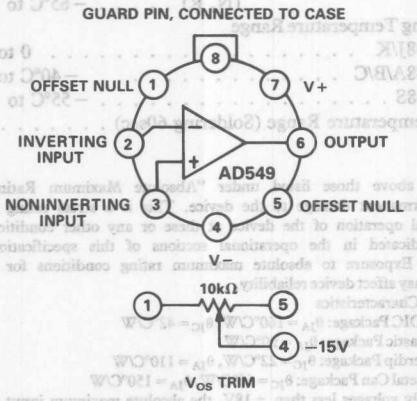
FEATURES

Ultralow Bias Current: 60 fA max (AD549L)
250 fA max (AD549J)
Input Bias Current Guaranteed Over Common-Mode Voltage Range
Low Offset Voltage: 0.25 mV max (AD549K)
1.00 mV max (AD549J)
Low Offset Drift: 5 μV/°C max (AD549K)
20 μV/°C max (AD549J)
Low Power: 700 μA max Supply Current
Low Input Voltage Noise: 4 μV p–p 0.1 to 10 Hz
MIL-STD-883B Parts Available

APPLICATIONS

Electrometer Amplifiers
Photodiode Preamp
pH Electrode Buffer
Vacuum Ion Gage Measurement

CONNECTION DIAGRAM



PRODUCT DESCRIPTION

The AD549 is a monolithic electrometer operational amplifier with very low input bias current. Input offset voltage and input offset voltage drift are laser trimmed for precision performance. The AD549's ultralow input current is achieved with "Topgate" JFET technology, a process development exclusive to Analog Devices. This technology allows the fabrication of extremely low input current JFETs compatible with a standard junction-isolated bipolar process. The 10^{15} Ω common-mode impedance, a result of the bootstrapped input stage, insures that the input current is essentially independent of common-mode voltage.

The AD549 is suited for applications requiring very low input current and low input offset voltage. It excels as a preamp for a wide variety of current output transducers such as photodiodes, photomultiplier tubes, or oxygen sensors. The AD549 can also be used as a precision integrator or low droop sample and hold. The AD549 is pin compatible with standard FET and electrometer op amps, allowing designers to upgrade the performance of present systems at little additional cost.

The AD549 is available in a TO-99 hermetic package. The case is connected to Pin 8 so that the metal case can be independently connected to a point at the same potential as the input terminals, minimizing stray leakage to the case.

The AD549 is available in four performance grades. The J, K, and L versions are rated over the commercial temperature range 0 to +70°C. The S grade is specified over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev C. Extended reliability PLUS screening is also available. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests derived from MIL-STD-883B, Rev C.

PRODUCT HIGHLIGHTS

1. The AD549's input currents are specified, 100% tested and guaranteed after the device is warmed up. Input current is guaranteed over the entire common-mode input voltage range.
2. The AD549's input offset voltage and drift are laser trimmed to 0.25 mV and 5 μV/°C (AD549K), 1 mV and 20 μV/°C (AD549J).
3. A maximum quiescent supply current of 700 μA minimizes heating effects on input current and offset voltage.
4. AC specifications include 1 MHz unity gain bandwidth and 3 V/μs slew rate. Settling time for a 10 V input step is 5 μs to 0.01%.
5. The AD549 is an improved replacement for the AD515, OPA104, and 3528.

*Protected by Patent No. 4,639,683.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C and V_S = +15 V dc, unless otherwise noted)

Model	AD549J			AD549K			AD549L			AD549S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT BIAS CURRENT[1]													
Either Input, V_{CM} = 0 V		150	**250**		75	**100**		40	**60**		75	**100**	fA
Either Input, V_{CM} = ±10 V		150	250		75	100		40	60		75	100	fA
Either Input at T_{max}, V_{CM} = 0 V		11			4.2			2.8			420		pA
Offset Current		50			30			20			30		fA
Offset Current at T_{max}		2.2			1.3			0.85			125		pA
INPUT OFFSET VOLTAGE[2]													
Initial Offset		0.5	**1.0**		0.15	**0.25**		0.3	**0.5**		0.3	**0.5**	mV
Offset at T_{max}			**1.9**			**0.4**			**0.9**			**2.0**	mV
vs. Temperature		10	**20**		2	5		5	**10**		10	**15**	μV/°C
vs. Supply		32	**100**		10	**32**		10	**32**		10	**32**	μV/V
vs. Supply, T_{min} to T_{max}		32	**100**		10	**32**		10	**32**		32	**50**	μV/V
Long-Term Offset Stability		15			15			15			15		μV/Month
INPUT VOLTAGE NOISE													
f = 0.1 Hz to 10 Hz		4			4	**6**		4			4		μV p-p
f = 10 Hz		90			90			90			90		nV/√Hz
f = 100 Hz		60			60			60			60		nV/√Hz
f = 1 kHz		35			35			35			35		nV/√Hz
f = 10 kHz		35			35			35			35		nV/√Hz
INPUT CURRENT NOISE													
f = 0.1 Hz to 10 Hz		0.7			0.5			0.36			0.5		fA rms
f = 1 kHz		0.22			0.16			0.11			0.16		fA/√Hz
INPUT IMPEDANCE													
Differential V_{DIFF} = ±1		10^{13}‖1			10^{13}‖1			10^{13}‖1			10^{13}‖1		Ω‖pF
Common Mode V_{CM} = ±10		10^{15}‖0.8			10^{15}‖0.8			10^{15}‖0.8			10^{15}‖0.8		Ω‖pF
OPEN-LOOP GAIN													
V_O @ ±10 V, R_L = 10 k	**300**	1000		**300**	1000		**300**	1000		**300**	1000		V/mV
V_O @ ±10 V, R_L = 10 k, T_{min} to T_{max}	**300**	800		**300**	800		**300**	800		**300**	800		V/mV
V_O = ±10 V, R_L = 2 k	**100**	250		**100**	250		**100**	250		**100**	250		V/mV
V_O = ±10 V, R_L = 2 k, T_{min} to T_{max}	**80**	200		**80**	200		**80**	200		**25**	150		V/mV
INPUT VOLTAGE RANGE													
Differential[3]			±20			±20			±20			±20	V
Common-Mode Voltage	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	V
Common-Mode Rejection Ratio													
V = +10 V, −10 V	**80**	90		**90**	100		**90**	100		**90**	100		dB
T_{min} to T_{max}	**76**	80		**80**	90		**80**	90		**80**	90		dB
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 10 k, T_{min} to T_{max}	**−12**		**+12**	**−12**		**+12**	**−12**		**+12**	**−12**		**+12**	V
Voltage @ R_L = 2 k, T_{min} to T_{max}	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	V
Short Circuit Current	**15**	20	**35**	**15**	20	**35**	**15**	20	**35**	**15**	20	**35**	mA
T_{min} to T_{max}	**9**			**9**			**9**			**6**			mA
Load Capacitance Stability G = +1		4000			4000			4000			4000		pF
FREQUENCY RESPONSE													
Unity Gain, Small Signal	0.7	1.0		0.7	1.0		0.7	1.0		0.7	1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate	2	3		2	3		2	3		2	3		V/μs
Settling Time, 0.1%		4.5			4.5			4.5			4.5		μs
0.01%		5			5			5			5		μs
Overload Recovery, 50% Overdrive, G = −1		2			2			2			2		μs

9

Model	AD549J			AD549K			AD549L			AD549S			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		**±18**	±5		**±18**	±5		**±18**	±5		**±18**	V
Quiescent Current		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[4]													
TO-99 (H-08A)	AD549JH			AD549KH			AD549LH			AD549SH, AD549SH/883B			
Chips	AD549JChips												

NOTES

[1]Bias current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. Bias current increases by a factor of 2.3 for every 10°C rise in temperature.

[2]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3]Defined as max continuous voltage between the inputs such that neither input exceeds ±10 V from ground.

[4]For outline information see Package Information section.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . 500 mW
Input Voltage . . . . . ±18 V[2]
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (H) . . . . . −65°C to +150°C
Operating Temperature Range
AD549J, K, L . . . . . 0 to +70°C
AD549S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

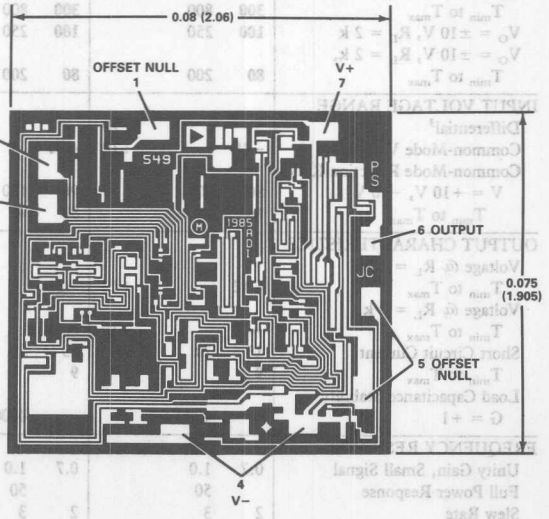
NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



CAUTION:

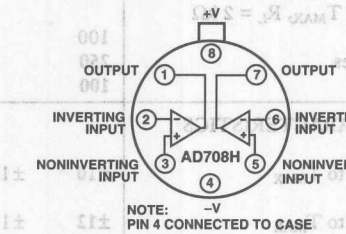
ESD (electrostatic discharge) sensitive device. Charges as high as 4000 V readily accumulate on the human body and test equipment and discharge without detection. Therefore, reasonable ESD precautions are recommended to avoid functional damage or performance degradation. Unused devices should be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

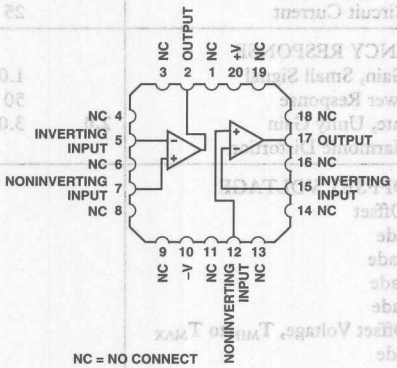
Dual, Low Cost, Precision BiFET Operational Amplifiers

AD642/AD644/AD647

FEATURES
- **Matched Offset Voltage**
- **Matched Offset Voltage over Temperature**
- **Matched Bias Current**
- **Crosstalk: –124 dB @ 1 kHz**
- **Low Bias Current: 35 pA max (Warmed Up)**
- **Low Offset Voltage: 250 μV max (AD647L)**
- **Low Input Voltage Noise: 2.0 μV p-p**
- **High Slew Rate: 13 V/μs (AD644)**
- **Low Quiescent Current**
- **Low Total Harmonic Distortion (0.0015%–AD644)**
- **Standard Dual Amplifier Pin-out**
- **MIL-STD-883B Versions Available**
- **Single Versions Offered: AD542, AD544, AD547**

CONNECTION DIAGRAMS





PRODUCT DESCRIPTION

The AD642/AD644/AD647 series of precision, monolithic FET-input op amps are pairs of matched, high speed, BiFET op amps fabricated with the most advanced BiFET and laser trimming technologies. The AD642, AD644, AD647 series offers matched bias currents significantly lower than currently available dual, BiFET devices, 35 pA max., warmed up. In addition, the offset voltage is laser trimmed to less than 0.25 mV on the AD647L, using Analog Devices' laser wafer trimming (LWT) process.

This product series achieves tight matching and temperature tracking between the amplifiers by using the most advanced ion-implantation and laser wafer drift trimming technologies. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This process optimizes the ability to produce matched amplifiers which have lower initial bias currents than other popular BiFET amplifiers. Laser wafer trimming each amplifier's input offset voltage ensures tight initial match, and combined with superior wafer processing guarantees offset tracking over the temperature range.

The AD642, AD644 and AD647 are recommended for applications requiring excellent ac and dc performance. The matched amplifiers provide a low cost solution for true instrumentation amplifiers, low drift active filters, log ratio amplifiers, and output amplifiers for four quadrant multiplying D/A converters, such as the AD7541, 12-bit CMOS DAC.

Devices in this series are available in four grades: the "J," "K," and "L" grades are specified over the 0°C to +70°C temperature range and the "S" grade over the –55°C to +125°C operating temperature range. All devices are offered in the hermetically sealed, TO-99 metal can package. In addition, the AD647 is also offered in a 20-pin, hermetic, surface mount LCC package.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. Tight matching specifications ensure high performance and eliminate the need to match individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the device will meet its published specifications in actual use.
3. Advanced laser wafer trimming techniques reduce offset voltage to only 0.25 mV max and matched side to side to 0.25 mV (AD647L), thus eliminating the need for external nulling.
4. Low voltage noise (2 μV p-p) and high open-loop gain enhance performance as a precision op amp.
5. High slew rate (13 V/μs) and fast settling time to 0.01% (3.0 μs) make the AD644 ideal for D/A, A/D, sample-hold circuits and high speed integrators.
6. Low harmonic distortion (0.0015%) and low crosstalk (–124 dB) make the AD644 an ideal choice in stereo audio applications
7. Bare die are available for use in hybrid circuit applications.

V_{OUT} = ±10 V, R_L = 2 kΩ											
J Grade	**100**				**30**				**100**			V/mV
K, L, S Grades	**250**				**50**				**250**			V/mV
$T_A = T_{MIN}$ to T_{MAX}, R_L = 2 kΩ											
J Grade	100				20				100			V/mV
K, L Grades	**250**				**40**				**250**			V/mV
S Grade	**100**				**20**				**100**			V/mV
OUTPUT CHARACTERISTICS												
R_L = 2 kΩ												
$T_A = T_{MIN}$ to T_{MAX}	**±10**	±12			**±10**	±12			**±10**	±12		V
R_L = 10 kΩ												
$T_A = T_{MIN}$ to T_{MAX}	**±12**	±13			**±12**	±13			**±12**	±13		V
Short Circuit Current		25				25				25		mA
FREQUENCY RESPONSE												
Unity Gain, Small Signal		1.0				2.0				1.0		MHz
Full Power Response		50				200				50		kHz
Slew Rate, Unity Gain	**2.0**	3.0			**8.0**	13.0			**2.0**	3.0		V/µs
Total Harmonic Distortion						0.0015						%
INPUT OFFSET VOLTAGE[1]												
Initial Offset												
J Grade			**2.0**				**2.0**				**1.0**	mV
K Grade			**1.0**				**1.0**				**0.5**	mV
L Grade			**0.5**				**0.5**				**0.25**	mV
S Grade			**1.0**				**1.0**				**0.5**	mV
Input Offset Voltage, T_{MIN} to T_{MAX}												
J Grade			3.5				3.5				**1.5**	mV
K Grade			**2.0**				**2.0**				**1.0**	mV
L Grade			**1.0**				**1.0**				**0.5**	mV
S Grade			**3.5**				**3.5**				**1.5**	mV
vs. Supply, $T_A = T_{MIN}$ to T_{MAX}												
J Grade			200				200				**200**	µV/V
K, L, S Grades			**100**				**100**				**100**	µV/V
INPUT BIAS CURRENT[2]												
Either Input												
J Grade		10	75			10	75			10	75	pA
K, L, S Grades		10	35			10	35			10	35	pA
Input Offset Current												
J Grade		5				10				5		pA
K, L, S Grades		2				5				2		pA
MATCHING CHARACTERISTICS[3]												
Input Offset Voltage												
J Grade			**1.0**				**1.0**				**1.0**	mV
K Grade			**0.5**				**0.5**				**0.5**	mV
L Grade			**0.25**				**0.25**				**0.25**	mV
S Grade			**0.5**				**0.5**				**0.5**	mV
Input Offset Voltage, T_{MIN} to T_{MAX}												
J Grade			3.5				3.5				**1.5**	mV
K Grade			**2.0**				**2.0**				**1.0**	mV
L Grade			**1.0**				**1.0**				**0.5**	mV
S Grade			**3.5**				**3.5**				**1.5**	mV
Input Bias Current												
J, S Grades			**35**				**35**				**35**	pA
K, L Grades			**25**				**25**				**25**	pA
Crosstalk		–124				–124				–124		dB

INPUT IMPEDANCE								
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$	$\Omega\|pF$
Common Mode		$10^{12}\|6$			$10^{12}\|3$			$10^{12}\|6$	$\Omega\|pF$
INPUT VOLTAGE RANGE									
Differential[4]		±20			±20			±20	V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12	V
Common Mode Rejection									
J Grade	**76**			**76**			**76**		dB
K, L, S Grades	**80**			**80**			**80**		dB
POWER SUPPLY									
Rated Performance		±15			±15			±15	V
Operating	±5		**±18**	±5		**±18**	±5		**±18**	V
Quiescent Current			**2.8**		3.5	**4.5**			**2.8**	mA
VOLTAGE NOISE									
0.1 Hz to 10 Hz									
J Grade		2.0			2.0			2.0		µV p-p
K, L, S Grades		2.0			2.0				**4.0**	µV p-p
10 Hz		70			35			70		$nV/\sqrt{Hz}$
100 Hz		45			22			45		$nV/\sqrt{Hz}$
1 kHz		30			18			30		$nV/\sqrt{Hz}$
10 kHz		25			16			25		$nV/\sqrt{Hz}$
TEMPERATURE RANGE									
Operating, Rated Performance									
J, K, L Grades		0 to +70			0 to +70			0 to +70		°C
S Grade		−55 to +125			−55 to +125			−55 to +125		°C
Storage		−65 to +150			−65 to +150			−65 to +150		°C

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10 V from ground.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ORDERING GUIDE

Model	Package Description	Package Option*
AD642JCHIPS	Bare Die	
AD642JH	8-Pin Hermetic Metal Can	H-08A
AD642KH	8-Pin Hermetic Metal Can	H-08A
AD642LH	8-Pin Hermetic Metal Can	H-08A
AD642SH	8-Pin Hermetic Metal Can	H-08A
AD642SH/883B	8-Pin Hermetic Metal Can	H-08A
AD644JH	8-Pin Hermetic Metal Can	H-08A
AD644KH	8-Pin Hermetic Metal Can	H-08A
AD644LH	8-Pin Hermetic Metal Can	H-08A
AD644SCHIPS	Bare Die	
AD644SH	8-Pin Hermetic Metal Can	H-08A
AD644SH/883B	8-Pin Hermetic Metal Can	H-08A

Model	Package Description	Package Option*
AD647JCHIPS	Bare Die	
AD647JH	8-Pin Hermetic Metal Can	H-08A
AD647KH	8-Pin Hermetic Metal Can	H-08A
AD647LH	8-Pin Hermetic Metal Can	H-08A
AD647SE	20-Pin Hermetic LCC	E-20A
AD647SE/883B	20-Pin Hermetic LCC	E-20A
AD647SH	8-Pin Hermetic Metal Can	H-08A
AD647SH/883B	8-Pin Hermetic Metal Can	H-08A

*For outline information see Package Information section.

Low Noise, Low Drift FET Op Amp

AD645

FEATURES

Improved Replacement for Burr-Brown OPA-111 and OPA-121 Op Amp

LOW NOISE
2 μV p–p max, 0.1 Hz to 10 Hz
10 nV/√Hz max at 10 kHz
11 fA p–p Current Noise 0.1 Hz to 10 Hz

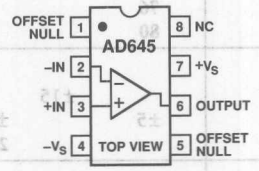
HIGH DC ACCURACY
250 μV max Offset Voltage
1 μV/°C max Drift
1.5 pA max Input Bias Current
114 dB Open-Loop Gain
Available in Plastic Mini-DIP, 8-Pin Header Packages, or Chip Form

IMPROVED DRIFT

APPLICATIONS
Low Noise Photodiode Preamps
CT Scanners
Precision I-V Converters

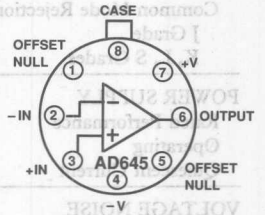
CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) Package



NC = NO CONNECT

TO-99 (H) Package



NOTE: CASE IS CONNECTED TO PIN 8

PRODUCT DESCRIPTION

The AD645 is a low noise, precision FET input op amp. It offers the pico amp level input currents of a FET input device coupled with offset drift and input voltage noise comparable to a high performance bipolar input amplifier.

The AD645 has been improved to offer the lowest offset drift in a FET op amp, 1 μV/°C. Offset voltage drift is measured and trimmed at wafer level for the lowest cost possible. An inherently low noise architecture and advanced manufacturing techniques result in a device with a guaranteed low input voltage noise of 2 μV p–p, 0.1 Hz to 10 Hz. This level of dc performance along with low input currents make the AD645 an excellent choice for high impedance applications where stability is of prime concern.

The AD645 is available in six performance grades. The AD645J and AD645K are rated over the commercial temperature range of 0°C to +70°C. The AD645A, AD645B, and the ultraprecision AD645C are rated over the industrial temperature range of −40°C to 85°C. The AD645S is rated over the military temperature range of −55°C to 125°C and is available processed to MIL-STD-883B.

The AD645 is available in an 8-pin plastic mini-DIP, 8-pin header, or in die form.

PRODUCT HIGHLIGHTS

1. Guaranteed and tested low frequency noise of 2 μV p–p max and 20 nV/√Hz at 100 Hz makes the AD645C ideal for low noise applications where a FET input op amp is needed.
2. Low V_{OS} drift of 1 μV/°C max makes the AD645C an excellent choice for applications requiring ultimate stability.
3. Low input bias current and current noise (11 fA p–p 0.1 Hz to 10 Hz) allow the AD645 to be used as a high precision preamp for current output sensors such as photodiodes, or as a buffer for high source impedance voltage output sensors.

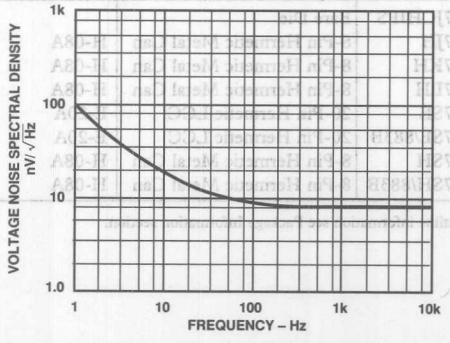


Figure 1. AD645 Voltage Noise Spectral Density vs. Frequency

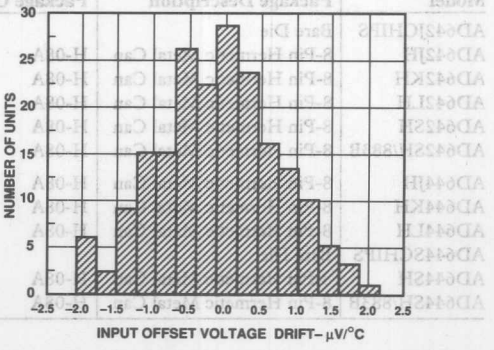


Figure 2. Typical Distribution of Average Input Offset Voltage Drift (196 Units)

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD645J/A			AD645K/B			AD645C			AD645S			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]														
Initial Offset			100	500		50	250		50	250		100	500	μV
Offset	T_{MIN}–T_{MAX}		300	1000		100	400		75	300		500	1500	μV
Drift (Average)			3	10/5		1	5/2		0.5	1		4	10	μV/°C
vs. Supply (PSRR)		90	110		94	110		94	110		90	110		dB
vs. Supply	T_{MIN}–T_{MAX}		100		90	100		90	100		86	95		dB
INPUT BIAS CURRENT[2]														
Either Input	V_{CM} = 0 V		0.7/1.8	3/5		0.7/1.8	1.5/3		1.8	3		1.8	5	pA
Either Input @ T_{MAX}	V_{CM} = 0 V		16/115			16/115			115			1800		pA
Either Input	V_{CM} = +10 V		0.8/1.9			0.8/1.9			1.9			1.9		pA
Offset Current	V_{CM} = 0 V		0.1	1.0		0.1	0.5		0.1	0.5		0.1	1.0	pA
Offset Current @ T_{MAX}	V_{CM} = 0 V		2/6			2/6			6			100		pA
INPUT VOLTAGE NOISE	0.1 to 10 Hz		1.0	3.0		1.0	2.5		1	2		1.0	3.3	μV p–p
	f = 10 Hz		20	50		20	40		20	40		20	50	nV/√Hz
	f = 100 Hz		10	30		10	20		10	20		10	30	nV/√Hz
	f = 1 kHz		9	15		9	12		9	12		9	15	nV/√Hz
	f = 10 kHz		8	10		8	10		8	10		8	10	nV/√Hz
INPUT CURRENT NOISE	f = 0.1 to 10 Hz		11	20		11	15		11	15		11	20	fA p–p
	f = 0.1 thru 20 kHz		0.6	1.1		0.6	0.8		0.6	0.8		0.6	1.1	fA/√Hz
FREQUENCY RESPONSE														
Unity Gain, Small Signal			2			2			2			2		MHz
Full Power Response	V_O = 20 V p–p													
	R_{LOAD} = 2 kΩ	16	32		16	32		16	32		16	32		kHz
Slew Rate, Unity Gain	V_{OUT} = 20 V p–p													
	R_{LOAD} = 2 kΩ	1	2		1	2		1	2		1	2		V/μs
SETTLING TIME[3]														
To 0.1%			6			6			6			6		μs
To 0.01%			8			8			8			8		μs
Overload Recovery[4]	50% Overdrive		5			5			5			5		μs
Total Harmonic Distortion	f = 1 kHz, R_{LOAD} ≥ 2 kΩ, V_O = 3 V rms		0.0006			0.0006			0.0006			0.0006		%
INPUT IMPEDANCE														
Differential	V_{DIFF} = ±1 V		10^{12}‖1			10^{12}‖1			10^{12}‖1			10^{12}‖1		Ω‖pF
Common-Mode			10^{14}‖2.2			10^{14}‖2.2			10^{14}‖2.2			10^{14}‖2.2		Ω‖pF
INPUT VOLTAGE RANGE														
Differential[5]			±20			±20			±20			±20		V
Common-Mode Voltage		±10	+11, −10.4		±10	+11, −10.4		±10	+11, −10.4		±10	+11, −10.4		V
Over Max Oper. Range		±10			±10			±10			±10			V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	90	110		94	110		94	110		90	110		dB
	T_{MIN}–T_{MAX}		100		90	100		90	100		86	100		dB
OPEN-LOOP GAIN	V_O = ±10 V													
	R_{LOAD} ≥ 2 kΩ	114	130		120	130		120	130		114	130		dB
	T_{MIN}–T_{MAX}				114			114			110			dB
OUTPUT CHARACTERISTICS														
Voltage	R_{LOAD} ≥ 2 kΩ	±10	±11		±10	±11		±10	±11		±10	±11		V
	T_{MIN}–T_{MAX}	±10			±10			±10			±10			V
Current	V_{OUT} = ±10 V	±5	±10		±5	±10		±5	±10		±5	±10		mA
	Short Circuit		±15			±15			±15			±15		mA
POWER SUPPLY														
Rated Performance			±15			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			3.0	3.5		3.0	3.5		3.0	3.5		3.0	3.5	mA
Transistor Count	# of Transistors		62			62			62			62		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[3]Gain = −1, R_{LOAD} = 2 kΩ.
[4]Defined as the time required for the amplifier's output to return to normal operation after removal of a 50% overload from the amplifier input.
[5]Defined as the maximum continuous voltage between the inputs such that neither input exceeds ±10 V from ground.
All min and max specifications are guaranteed.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] (@ T_A = +25°C)
8-Pin Header Package . . . . . 500 mW
8-Pin Mini-DIP Package . . . . . 750 mW
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (H) . . . . . −65°C to +150°C
Storage Temperature Range (N) . . . . . −65°C to +125°C
Operating Temperature Range
AD645J/K . . . . . 0°C to +70°C
AD645A/B/C . . . . . −40°C to +85°C
AD645S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering 60 seconds) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics:
8-Pin Plastic Mini-DIP Package: θ_{JA} = 100°C/Watt
8-Pin Header Package: θ_{JA} = 200°C/Watt

CAUTION

ESD (electrostatic discharge) sensitive device. Charges as high as 4000 V readily accumulate on the human body and test equipment and discharge without detection. Therefore, reasonable ESD precautions are recommended to avoid functional damage or performance degradation. Unused devices should be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual.*

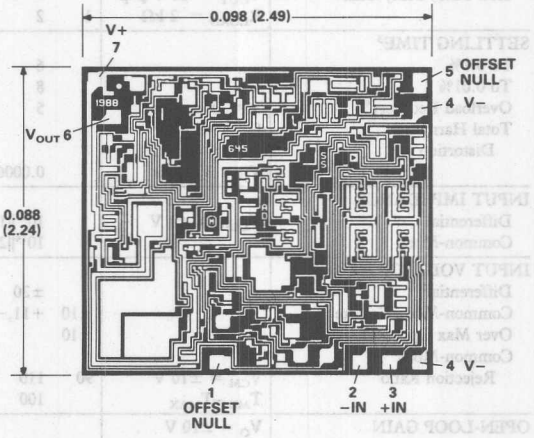
ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD645JN	0°C to +70°C	N-8
AD645KN	0°C to +70°C	N-8
AD645AH	−40°C to +85°C	H-08A
AD645BH	−40°C to +85°C	H-08A
AD645CH	−40°C to +85°C	H-08A
AD645SH/883B	−55°C to +125°C	H-08A

NOTES
[1]Chips are also available.
[2]N = Plastic mini-DIP; H = Metal Can. For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



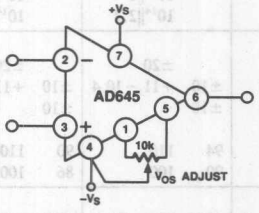


Figure 3. AD645 Offset Null Configuration

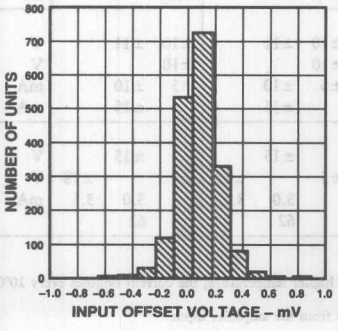


Figure 4. Typical Distribution of Input Offset Voltage (1855 Units)

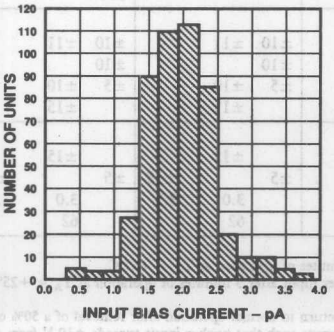


Figure 5. Typical Distribution of Input Bias Current (576 Units)

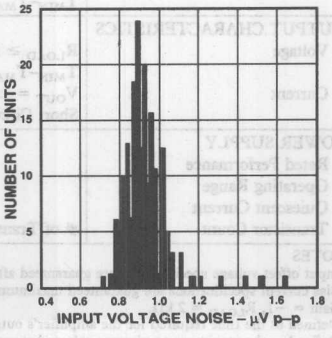


Figure 6. Typical Distribution of 0.1 Hz to 10 Hz Voltage Noise (202 Units)

Dual Precision, Low Power BiFET Op Amp

AD648

FEATURES

DC Performance
- 400 μA max Quiescent Current
- 10 pA max Bias Current, Warmed Up (AD648C)
- 300 μV max Offset Voltage (AD648C)
- 3 μV/°C max Drift (AD648C)
- 2 μV p–p Noise, 0.1 Hz to 10 Hz

AC Performance
- 1.8 V/μs Slew Rate
- 1 MHz Unity Gain Bandwidth

Available in Plastic Mini-DIP, Cerdip, Plastic SOIC and Hermetic Metal Can Packages

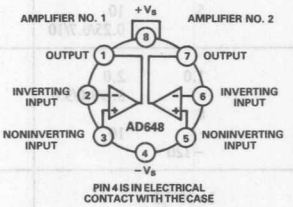
MIL-STD-883B Parts Available

Surface Mount (SOIC) Package Available in Tape and Reel in Accordance with EIA-481A Standard

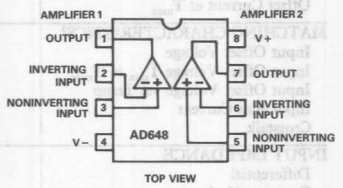
Single Version: AD548

CONNECTION DIAGRAMS

TO-99 (H) Package



Plastic Mini-DIP (N) Package, Plastic SOIC (R) Package and Cerdip (Q) Package



PRODUCT DESCRIPTION

The AD648 is a matched pair of low power, precision monolithic operational amplifiers. It offers both low bias current (10 pA max, warmed up) and low quiescent current (400 μA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD648's entire common-mode voltage range.

The economical J grade has a maximum guaranteed offset voltage of less than 2 mV and an offset voltage drift of less than 20 μV/°C. The C grade reduces offset voltage to less than 0.30 mV and offset voltage drift to less than 3 μV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Five additional grades are offered over the commercial, industrial and military temperature ranges.

The AD648 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD648's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common-mode rejection (86 dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD648 is pinned out in a standard dual op amp configuration and is available in seven performance grades. The AD648J and AD648K are rated over the commercial temperature range of 0 to +70°C. The AD648A, AD648B and AD648C are rated over the industrial temperature range of −40°C to +85°C. The AD648S and AD648T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

The AD648 is available in an 8-pin plastic mini-DIP, cerdip, SOIC, TO-99 metal can, or in chip form.

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD648 the ideal op amp for high performance, low power applications.
2. The AD648 is pin compatible with industry standard dual op amps such as the LF442, TL062, and AD642, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2 mV max) and drift (20 μV/°C max) for the AD648J are achieved utilizing Analog Devices' laser drift trimming technology.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. Matching characteristics are excellent for all grades. The input offset voltage matching between amplifiers in the AD648J is within 2 mV, for the C grade matching is within 0.4 mV.
6. Crosstalk between amplifiers is less than −120 dB at 1 kHz.
7. The AD648 is available in chip form.

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD648—SPECIFICATIONS (@ +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	AD648J/A/S			AD648K/B/T			AD648C			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.75	2.0		0.3	1.0		0.10	0.3	mV
T_{min} to T_{max}			3.0/3.0/3.0			1.5/1.5/2.0			0.5	mV
vs. Temp.			20			10			3.0	µV/°C
vs. Supply	80			86			86			dB
vs. Supply, T_{min} to T_{max}	76/76/76			80			80			dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT										
Either Input,[2] V_{CM} = 0		5	20		3	10		3	10	pA
Either Input[2] at T_{max}, V_{CM} = 0			0.45/1.3/20			0.25/0.65/10			0.65	nA
Max Input Bias Current Over Common-Mode Voltage Range			30			15			15	pA
Offset Current, V_{CM} = 0		5	10		2	5		2	5	pA
Offset Current at T_{max}			0.25/0.7/10			0.15/0.35/5			0.35	nA
MATCHING CHARACTERISTICS[3]										
Input Offset Voltage		1.0	2.0		0.5	1.0		0.2	0.4	mV
Input Offset Voltage T_{min} to T_{max}			3.0/3.0/3.0			1.5/1.5/2.0			0.5	mV
Input Offset Voltage vs. Temp		8			5			2.5		µV/°C
Input Bias Current			10			5			5	pA
Crosstalk		−120			−120			−120		dB
INPUT IMPEDANCE										
Differential		$1\times10^{12}\|\|3$			$1\times10^{12}\|\|3$			$1\times10^{12}\|\|3$		Ω||pF
Common Mode		$3\times10^{12}\|\|3$			$3\times10^{12}\|\|3$			$3\times10^{12}\|\|3$		Ω||pF
INPUT VOLTAGE RANGE										
Differential[4]		±20			±20			±20		V
Common Mode	±11	±12		±11	±12		±11	±12		V
Common-Mode Rejection										
V_{CM} = ±10 V	76			82			86			dB
T_{min} to T_{max}	76/76/76			82			86			dB
V_{CM} = ±11 V	70			76			76			dB
T_{min} to T_{max}	70/70/70			76			76			dB
INPUT VOLTAGE NOISE										
Voltage 0.1 Hz to 10 Hz		2			2			2	4.0	µV p–p
f = 10 Hz		80			80			80		nV/√Hz
f = 100 Hz		40			40			40		nV/√Hz
f = 1 kHz		30			30			30		nV/√Hz
f = 10 kHz		30			30			30		nV/√Hz
INPUT CURRENT NOISE										
f = 1 kHz		1.8			1.8			1.8		fA/√Hz
FREQUENCY RESPONSE										
Unity Gain, Small Signal	0.8	1.0		0.8	1.0		0.8	1.0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain	1.0	1.8		1.0	1.8		1.0	1.8		V/µs
Settling Time to ±0.01%		8			8			8		µs
OPEN-LOOP GAIN										
V_O = ±10 V, $R_L \geq 10$ kΩ	300	1000		300	1000		300	1000		V/mV
T_{min} to T_{max}, $R_L \geq 10$ kΩ	300/300/300	700		300	700		300	700		V/mV
V_O = ±10 V, $R_L \geq 5$ kΩ	150	500		150	500		150	500		V/mV
T_{min} to T_{max}, $R_L \geq 5$ kΩ	150/150/150	300		150	300		150	300		V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 10$ kΩ, T_{min} to T_{max}	±12/±12/±12	±13		±12	±13		±12	±13		V
Voltage @ $R_L \geq 5$ kΩ, T_{min} to T_{max}	±11/±11/±11	±12		±11	±12		±11	±12		V
Short Circuit Current		15			15			15		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current (Both Amplifiers)		340	400		340	400		340	400	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD648J			AD648K					
Industrial (−40°C to +85°C)		AD648A			AD648B			AD648C		
Military (−55°C to +125°C)		AD648S			AD648T					
PACKAGE OPTIONS[5]										
SOIC (R-8)		AD648JR			AD648KR					
Plastic (N-8)		AD648JN			AD648KN					
Cerdip (Q-8)		AD648AQ, AD648SQ, AD648SQ/883B			AD648BQ, AD648TQ, AD648TQ/883B			AD648CQ		
Metal Can (H-08A)		AD648AH			AD648BH, AD648TH/883B					
Tape and Reel		AD648JR-REEL			AD648KR-REEL					
Chips Available		AD648JChips, AD648SChips								

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[3]Matching is defined as the difference between parameters of the two amplifiers.
[4]Defined as voltages between inputs, such that neither exceeds ±10 V from ground.
[5]For outline information see Package Information section.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

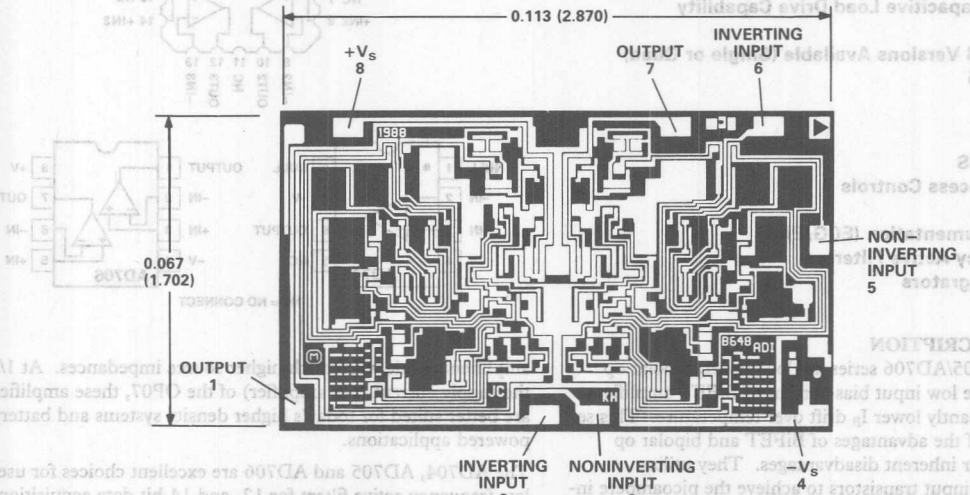
Supply Voltage	±18 V
Internal Power Dissipation[2]	500 mW
Input Voltage[3]	±18 V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (Q, H)	−65°C to +150°C
(N, R)	−65°C to +125°C
Operating Temperature Range	
AD648J/K	0 to +70°C
AD648A/B/C	−40°C to +85°C
AD648S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics
8-Pin Plastic DIP Package: θ_{JA} = 165°C/Watt
8-Pin Cerdip Package: θ_{JC} = 22°C/Watt; θ_{JA} = 110°C/Watt
8-Pin Metal Can Package: θ_{JC} = 65°C/Watt; θ_{JA} = 150°C/Watt
8-Pin SOIC Package: θ_{JC} = 42°C/Watt; θ_{JA} = 160°C/Watt
[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

9

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



FEATURES

HIGH DC PRECISION
- Low Offset Voltage
  - (75 μV max: AD704)
  - (35 μV max: AD705)
  - (50 μV max: AD706)
- Low Offset Drift
  - (1.0 μV/°C max: AD704)
  - (0.6 μV/°C max: AD705)
  - (0.6 μV/°C max: AD706)
- Low Input Bias Currents
  - (150 pA max: AD704)
  - (100 pA max: AD705)
  - (110 pA max: AD706)

LOW NOISE
- 0.5 μV p-p typ Voltage Noise (0.1 Hz to 10 Hz)

LOW POWER
- 600 μA max Supply Current per Amplifier

AC PERFORMANCE
- 0.15 V/μs Slew Rate
- 800 kHz Unity Gain Crossover Frequency
- 10,000 pF Capacitive Load Drive Capability

LOW COST

MIL-STD-883B Versions Available (Single or Quad)

Single: AD705

Dual: AD706

Quad: AD704

APPLICATIONS

Industrial/Process Controls

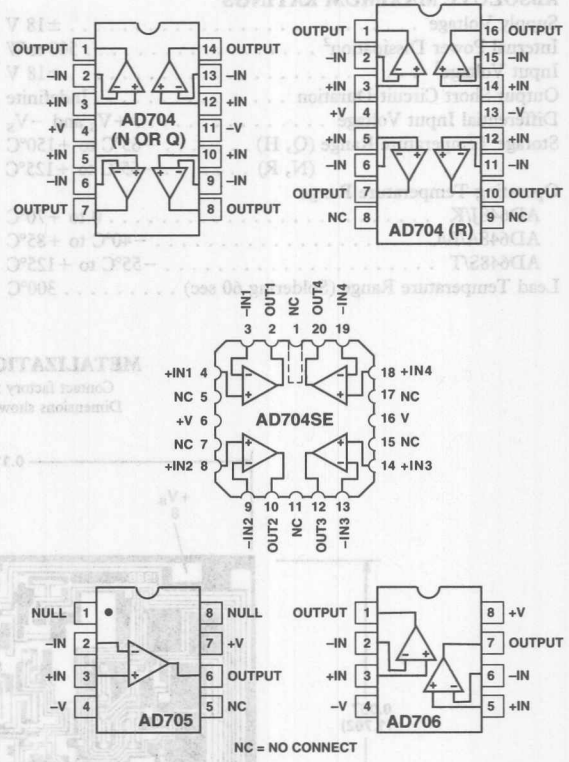
Weigh Scales

Medical Instrumentation (ECG/EKG)

Low Frequency Active Filters

Precision Integrators

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD704/AD705/AD706 series are low power, bipolar op amps that have the low input bias current of BiFET amplifiers, but offer a significantly lower I_B drift over temperature. This series offers many of the advantages of BiFET and bipolar op amps without their inherent disadvantages. They utilize superbeta bipolar input transistors to achieve the picoampere input bias current levels of FET input amplifiers (at room temperature), while their I_B typically increases 5 times vs. BiFET amplifiers which exhibit a 1000× increase over temperature. Superbeta bipolar technology also permits these amplifiers to achieve the microvolt offset voltages and low noise characteristics of a precision bipolar input amplifier.

Since these amplifiers have only 1/20 of the input bias current of an industry standard OP07, the AD704/AD705/AD706 do not require the commonly used "balancing" resistor. Furthermore, the current noise is 1/5 that of the OP07, which makes these amplifiers usable with much higher source impedances. At 1/6 the supply current (per amplifier) of the OP07, these amplifiers are better suited for today's higher density systems and battery powered applications.

The AD704, AD705 and AD706 are excellent choices for use in low frequency active filters for 12- and 14-bit data acquisition systems, in precision instrumentation, and as high quality integrators. These amplifiers are internally compensated for unity gain and are available in various performance grades. The "J" and "K" grades are rated over the commercial temperature range of 0°C to +70°C. The "A" and "B" grades are rated over the industrial temperature range of –40°C to +85°C. The "T" grade is rated over the military temperature range of –55°C to +125°C. Select versions are available processed to MIL-STD-883B, Rev. C.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (V_{CM} = 0 V, V_S = ±15 V @ T_A = +25°C unless otherwise noted)

Parameter	Conditions	Model	J/A Min	J/A Typ	J/A Max	K/B/S Min	K/B/S Typ	K/B/S Max	C/T Min	C/T Typ	C/T Max	Units
INPUT OFFSET VOLTAGE												
Initial Offset		AD704		50	150		30	75		30	100	µV
		AD705		30	90		10	35		10	25	µV
		AD706		30	100		10	50		10	50	µV
Offset	T_{MIN} to T_{MAX}	AD704		100	250		50	150		80	150	µV
		AD705		45	150		25	60		25	60	µV
		AD706		40	150		25	100		25	100	µV
vs. Temp, Average TC		AD704		0.2	1.5		0.2	1.0			1.0	µV/°C
		AD705		0.2	1.2		0.2	0.6		0.2	0.6	µV/°C
		AD706		0.2	1.5		0.2	0.6		0.2	0.6	µV/°C
vs. Supply (PSRR)	V_S = ±2 V to ±18 V	AD704	100	132		112	132		112	132		dB
		AD705	110	129		110	129		114	129		dB
		AD706	110	132		112	132		112	132		dB
vs. Supply, T_{MIN} to T_{MAX}	V_S = ±2.5 V to ±18 V	All	100	126		108	126		108	126		dB
Long-Term Stability		All		0.3			0.3			0.3		µV/Month
INPUT BIAS CURRENT[1]	V_{CM} = 0 V	AD704		100	270		80	150		80	200	pA
		AD705		60	150		30	100		30	100	pA
		AD706		50	200		30	110		30	120	pA
	V_{CM} = ±13.5 V	AD704			300			200			250	pA
		AD705		80	200		50	150		50	150	pA
		AD706			250			160			170	pA
vs. Temp, Average TC		AD704		0.3			0.2			1.0		pA/°C
		AD705		0.3			0.3			0.6		pA/°C
		AD706		0.3			0.2			0.2		pA/°C
T_{MIN} to T_{MAX}	V_{CM} = 0 V	AD704			300			200			600	pA
		AD705		80	250		50	150		90	250	pA
		AD706			300			200			400	pA
T_{MIN} to T_{MAX}	V_{CM} = ±13.5 V	AD704			400			300			700	pA
		AD705		100	450		70	350		120	450	pA
		AD706			400			300			600	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V	AD704		80	250		30	100		50	150	pA
		AD705		40	150		30	100		30	100	pA
		AD706		30	150		30	100		30	100	pA
	V_{CM} = ±13.5 V	AD704			300			150			200	pA
		AD705		40	200		30	150		30	150	pA
		AD706			250			200			200	pA
vs. Temp, Average TC		AD704		0.6			0.4			0.4		pA/°C
		AD705		0.3			0.3			0.4		pA/°C
		AD706		0.3			0.2			0.2		pA/°C
T_{MIN} to T_{MAX}	V_{CM} = 0 V	AD704		100	300		80	200		80	400	pA
		AD705		80	250		50	150		90	250	pA
		AD706		80	250		80	200		80	300	pA
T_{MIN} to T_{MAX}	V_{CM} = ±13.5 V	AD704		100	400		80	300		100	500	pA
		AD705		80	450		50	350		80	450	pA
		AD706		80	350		80	300		80	450	pA
MATCHING CHARACTERISTICS												
Offset Voltage		AD704			250			130			150	µV
		AD706			150			75			75	µV
	T_{MIN} to T_{MAX}	AD704			400			200			250	µV
		AD706			250			150			200	µV
Input Bias Current[2]		AD704			500			300			400	pA
		AD706			300			150			200	pA
	T_{MIN} to T_{MAX}	AD704			600			400			600	pA
		AD706			500			250			400	pA
Common-Mode Rejection[3]		AD704	94			110			104			dB
		AD706	106			110			110			dB
	T_{MIN} to T_{MAX}	AD704	94			104			104			dB
		AD706	106			108			108			dB
Power Supply Rejection[4]		AD704	94			110			110			dB
		AD706	106			110			110			dB
	T_{MIN} to T_{MAX}	AD704	94			106			106			dB
		AD706	104			106			106			dB
Crosstalk @ f = 10 Hz	R_L = 2 kΩ	AD704/6		150			150			150		dB

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Parameter	Conditions	Model	J/A Min	J/A Typ	J/A Max	K/B/S Min	K/B/S Typ	K/B/S Max	C/T Min	C/T Typ	C/T Max	Units
INPUT OFFSET VOLTAGE												
UNITY GAIN												
Crossover Frequency		All		0.8			0.8			0.8		MHz
Slew Rate	G = –1	All		0.15			0.15			0.15		V/μs
	T_{MIN} to T_{MAX}	All		0.15			0.15			0.15		V/μs
INPUT IMPEDANCE												
Differential		All		40‖2			40‖2			40‖2		MΩ‖pF
Common Mode		All		300‖2			300‖2			300‖2		GΩ‖pF
INPUT VOLTAGE RANGE												
Common-Mode Voltage		All	±13.5	±14		±13.5	±14		±13.5	±14		V
Common-Mode	V_{CM} = ±13.5 V	AD704	100	132		114	132		110	132		dB
Rejection Ratio		AD705	110	132		114	132		114	132		dB
		AD706	110	132		114	132		114	132		dB
	T_{MIN} to T_{MAX}	AD704	98	128		108	128		108	128		dB
		AD705	108	128		108	128		108	128		dB
		AD706	108	128		108	128		108	128		dB
INPUT CURRENT NOISE	0.1 Hz to 10 Hz	All		3			3			3		pA p-p
	f = 10 Hz	All		50			50			50		fA/√Hz
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz	AD704		0.5			0.5	2.0		0.5	2.0	μV p-p
		AD705/6		0.5			0.5	1.0		0.5	1.0	μV p-p
	f = 10 Hz	All		17			17			17		nV/√Hz
	f = 1 kHz	All		15	22		15	22		15	22	nV/√Hz
OPEN LOOP GAIN	V_O = ±12 V											
	R_L = 10 kΩ	All	200	2000		400	2000		400	2000		V/mV
	T_{MIN} to T_{MAX}	All	150	1500		300	1500		300	1500		V/mV
	V_O = ±10 V											
	R_L = 2 kΩ	All	200	1000		300	1000		200	1000		V/mV
	T_{MIN} to T_{MAX}	All	150	1000		200	1000		100	1000		V/mV
OUTPUT CHARACTERISTICS												
Voltage Swing, R_L = 10 kΩ	T_{MIN} to T_{MAX}	All	±13	±14		±13	±14		±13	±14		V
Current	Short Circuit	All		±15			±15			±15		mA
Capacitive Load Drive	G = +1	All		10,000			10,000			10,000		pF
POWER SUPPLY												
Rated Performance		All		±15				±15		±15		V
Operating Range		All	±2		±18	±2		±18	±2		±18	V
Quiescent Current		AD704		1.5	2.4		1.5	2.4		1.5	2.4	mA
		AD705		0.38	0.6		0.38	0.6		0.38	0.6	mA
		AD706		0.75	1.2		0.75	1.2		0.75	1.2	mA
	T_{MIN} to T_{MAX}	AD704		1.6	2.6		1.6	2.6		1.6	2.6	mA
		AD705		0.4	0.8		0.4	0.8		0.4	0.8	mA
		AD706		0.8	1.4		0.8	1.4		0.8	1.4	mA
TRANSISTOR COUNT	# of Transistors	AD704		180			180			180		
		AD705		45			45			45		
		AD706		90			90			90		

NOTES
[1]Bias current specifications are guaranteed maximum at either input.
[2]Input bias current match is the maximum difference between corresponding inputs of all amplifiers on the chip.
[3]CMRR match is the difference of $\Delta V_{OS}/\Delta V_{CM}$ between any two amplifiers.
[4]PSRR match is the difference between $\Delta V_{OS}/\Delta V$ SUPPLY for any two amplifiers.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Internal Power Dissipation[2]	650 mW
Input Voltage	$\pm V_S$
Differential Input Voltage[3]	±0.7 V
Output Short Circuit Duration	Indefinite
Storage Temperature Range (N, R)	−65°C to +125°C
Storage Temperature Range (Q, H)	−65°C to +150°C
Operating Temperature Range	
AD70xJ/K	0°C to +70°C
AD70xA/B	−40°C to +85°C
AD70xS/T	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	+300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:

8-Pin Plastic Package:	θ_{JA} = 165°C/Watt
8-Pin Cerdip Package:	θ_{JA} = 110°C/Watt
8-Pin Small Outline Package:	θ_{JA} = 155°C/Watt
14-Pin Plastic Package:	θ_{JA} = 150°C/Watt
14-Pin Cerdip Package:	θ_{JA} = 110°C/Watt
16-Pin SOIC Package:	θ_{JA} = 100°C/Watt
20-Terminal LCC Package:	θ_{JA} = 150°C/Watt

[3]The input pins of these amplifiers are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 V, external series protection resistors should be added to limit the input current to less than 25 mA.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD704AN	−40°C to +85°C	14-Pin Plastic DIP	N-14
AD704AQ	−40°C to +85°C	14-Pin Ceramic DIP	Q-14
AD704AR-16	−40°C to +85°C	16-Pin Plastic SOIC	R-16
AD704AR-16-REEL	−40°C to +85°C	16-Pin Plastic SOIC	R-16
AD704AR-16-REEL7	−40°C to +85°C	16-Pin Plastic SOIC	R-16
AD704BQ	−40°C to +85°C	14-Pin Ceramic DIP	Q-14
AD704JCHIPS	0°C to +70°C	Bare Die	
AD704JN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD704JR-16	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD704JR-16-REEL	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD704JR-16-REEL7	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD704KN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD704SE/883B	−55°C to +125°C	20-Pin Ceramic LCC	E-20A
AD704TQ	−55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD704TQ/883B	−55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD705AQ	−40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD705BQ	−40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD705JCHIPS	0°C to +70°C	Bare Die	
AD705JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD705JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD705JR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD705JR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD705KN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD705TQ	−55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD705TQ/883B	−55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD706AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD706AQ	−40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD706AR	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD706AR-REEL	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD706AR-REEL7	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD706BQ	−40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD706JCHIPS	0°C to +70°C	Bare Die	
AD706JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD706JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD706JR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD706JR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD706KN	0°C to +70°C	8-Pin Plastic	N-8

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

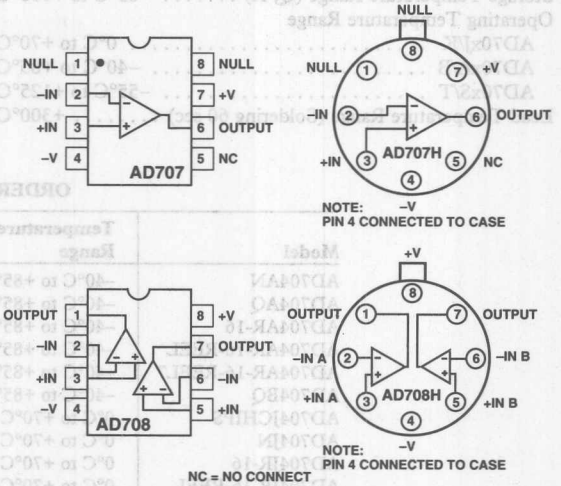
Ultralow Offset and Drift Operational Amplifiers

AD707/AD708

FEATURES

- Very High DC Precision
  - Low Offset Voltages
    - (15 μV max: AD707)
    - (30 μV max: AD708)
  - Low Offset Drift
    - (0.1 μV/°C max: AD707)
    - (0.3 μV/°C max: AD708)
  - Low Input Bias Current: 1 nA max
- Low Noise: 0.35 μV p-p max (0.1 Hz to 10 Hz)
- 130 dB min CMRR
- 120 dB min PSRR
- AC Performance
  - 0.3 V/μs Slew Rate
  - 900 kHz Closed-Loop Bandwidth
- Matching Characteristics
  - 30 μV max Offset Voltage Match
  - 0.3 μV/°C max Offset Drift Match
  - 130 dB min CMRR Match
- MIL-STD-883B Versions Available
- Single: AD707
- Dual: AD708

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD707 (single) and AD708 (dual) are very high precision, monolithic operational amplifiers. Each device offers excellent dc precision with the best available max offset voltage and max offset voltage drift of any single/dual bipolar combination available.

The AD707 and AD708 set new standards for precision op amps by providing 5 V/μV min open-loop gain and guaranteed max input voltage noise of 350 nV p-p (0.1 Hz to 10 Hz). All dc specifications show excellent stability over temperature, with offset voltage drift typically 0.1 μV/°C and input bias current drift of 25 pA/°C max. Both CMRR (130 dB max) and PSRR (120 dB max) are an order of magnitude improved over any available monolithic op amp.

The AD707 and AD708 are available in seven performance grades. The "J" and "K" grades are rated over the commercial temperature range of 0°C to +70°C. The "A," "B" and "C" grades are rated over the industrial temperature range of –40°C to +85°C. The "S" and "T" grades are rated over the military temperature range of –55°C to +125°C. Select versions are also available processed to MIL-STD-883B, Rev. C.

PRODUCT HIGHLIGHTS

1. The combination of outstanding matching and individual specifications make the AD707 and AD708 ideal for constructing high gain, precision instrumentation amplifiers.
2. The low offset voltage drift and low noise of the AD707 and AD708 allow the user to amplify very small signals without sacrificing overall system performance.
3. The AD707 and AD708 can be used where chopper amplifiers are required, but without the inherent noise and application problems.
4. The AD707 is an improved, pin-for-pin replacement for the LT1001, and the AD708 is an improved, pin-for-pin replacement for the LT1002.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (V_{DD} = ±15 V @ T_A = +25°C unless otherwise noted)

Parameter	Conditions	Model	J/A Min	J/A Typ	J/A Max	K/B/S Min	K/B/S Typ	K/B/S Max	C/T Min	C/T Typ	C/T Max	Units
INPUT OFFSET VOLTAGE[1]												
Initial Offset		AD707		30	**90**		10	**25**		5	**15**	µV
		AD708		30	**100**		15	**65/65/50**				µV
vs. Temperature	T_{MIN} to T_{MAX}	AD707		50	100		15	**45**		7/8	**25**	µV
		AD708		50	150		15	65				µV
Drift		AD707		0.3	1.0		0.1	**0.3**		0.03	**0.1**	µV/°C
		AD708		0.3	1.0		0.1	0.4/0.4/**0.4**				µV/°C
Adjustment Range		AD707		±4			±4			±4		mV
Long-Term Stability		Both		0.3			0.3			0.2		µV/Month
INPUT BIAS CURRENT		AD707		1.0	**2.5**		0.5	**1.5**		0.5	**1.0**	nA
		AD708		1.0	**2.5**		0.5	**1.0**				nA
vs. Temperature	T_{MIN} to T_{MAX}	AD707		2.0	4.0		1.5	**3.0**		1.0	**2.0**	nA
		AD708		2.0	4.0		1.0	2.0/2.0/**4.0**				nA
Average Drift		AD707		15	40		15	25/25/35		1	25	pA/°C
		AD708		15	40		10	25/25/30				pA/°C
INPUT OFFSET CURRENT	V_{CM} = 0 V	AD707		0.5	**2.0**		0.3	**1.5**		0.1	**1.0**	nA
		AD708		0.5	2.0		0.1	**1.0**				nA
	T_{MIN} to T_{MAX}	AD707		2.0	4.0		1.5	**3.0**		0.2	**1.5**	nA
		AD708		2.0	4.0		0.2	1.5/1.5/**1.5**				nA
Average Drift		AD707		2	40		1	25/25/35		1	25	pA/°C
		AD708		2	60		1	25				pA/°C
MATCHING CHARACTERISTICS[2]												
Offset Voltage		AD708			**80**			**50/50/50**				µV
	T_{MIN} to T_{MAX}	AD708			150			75/75/**75**				µV
Offset Voltage Drift		AD708			1.0			0.4/0.4/**0.4**				µV/°C
Input Bias Current		AD708			**4.0**			**1.0**				nA
	T_{MIN} to T_{MAX}	AD708			5.0			2.0/2.0/**2.0**				nA
Common-Mode Rejection		AD708	**120**		300	**130/130/120**	140					dB
	T_{MIN} to T_{MAX}	AD708	110		600	130/130/115						dB
Power Supply Rejection		AD708	**110**			**120**						dB
	T_{MIN} to T_{MAX}	AD708	110		500	120						dB
Channel Separation		AD708	135			140						dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz	AD707		0.23	0.6		0.23	0.6		0.23	**0.35**	µV p-p
		AD708		0.23	0.6		0.23	0.6/0.6/**0.6**				µV p-p
	f = 10 Hz	AD707		10.3	15.0		10.3	14.0		10.3	13.0	nV/√Hz
		AD708		10.3	18.0		10.3	12.0				nV/√Hz
	f = 100 Hz	AD707		10.0	13.0		10.0	12.0		10.0	11.0	nV/√Hz
		AD708		10.0	13.0		10.0	11.0				nV/√Hz
	f = 1 kHz	AD707		9.6	11.0		9.6	11.0		9.6	11.0	nV/√Hz
		AD708		9.6	11.0		9.6	11.0				nV/√Hz
INPUT CURRENT NOISE	0.1 Hz to 10 Hz	AD707		14	35		14	30		14	**30**	pA p-p
		AD708		14	35		14	35				pA p-p
	f = 10 Hz	AD707		0.32	0.9		0.32	0.8		0.32	0.8	pA/√Hz
		AD708		0.32	0.9		0.32	0.8				pA/√Hz
	f = 100 Hz	AD707		0.14	0.27		0.14	0.23		0.14	0.23	pA/√Hz
		AD708		0.14	0.27		0.14	0.23				pA/√Hz
	f = 1 kHz	AD707		0.12	0.18		0.12	0.17		0.12	0.17	pA/√Hz
		AD708		0.12	0.18		0.12	0.17				pA/√Hz
COMMON-MODE REJECTION RATIO	V_{CM} = ±13 V	Both	**120**	140		**130**	140		**130**	140		dB
	T_{MIN} to T_{MAX}	Both	120	140		**130**	140		**130**	140		dB
OPEN-LOOP GAIN	V_O = ±10 V											
	$R_L \geq 2$ kΩ	AD707	**3**	13		5	13		**8**	13		V/µV
		AD708	3	10		5/5/4	10					V/µV
	T_{MIN} to T_{MAX}	AD707	3	13		5	13		8	13		V/µV
		AD708	3	10		5/5/4	10/10/**7**					V/µV
POWER SUPPLY REJECTION RATIO	V_S = ±3 V to ±18 V	AD707	110	130		115	130		120	130		dB
		AD708	120	130		120	130					dB
	T_{MIN} to T_{MAX}	AD707	110	130		115	130		120	130		dB
		AD708	110	130		120	130					dB
FREQUENCY RESPONSE												
Closed Loop Bandwidth		Both	0.5	0.9		0.5	0.9		0.5	0.9		MHz
Slew Rate		Both	0.15	0.3		0.15	0.3		0.15	0.3		V/µs

INPUT RESISTANCE												
Differential		AD707	24	100		45	200		60	200		MΩ
		AD708		60			200					MΩ
Common Mode		AD707		200			300			400		GΩ
		AD708		200			400					GΩ
OUTPUT CHARACTERISTICS												
Voltage	$R_L \geq 10$ kΩ	Both	**13.5**	14.0		**13.5**	14.0		**13.5**	14.0		±V
	$R_L \geq 2$ kΩ	Both	**12.5**	13.0		**12.5**	13.0		**12.5**	13.0		±V
	$R_L \geq 1$ kΩ	Both	**12.0**	12.5		**12.0**	12.5		**12.0**	12.5		±V
	$R_L \geq 2$ kΩ											
	T_{MIN} to T_{MAX}	Both	12.0	13.0		**12.0**	13.0		**12.0**	13.0		±V
OPEN-LOOP OUTPUT RESISTANCE		Both		60			60			60		Ω
POWER SUPPLY												
Quiescent Current		AD707		2.5	**3.0**		2.5	**3.0**		2.5	**3.0**	mA
		AD708		4.5	**5.5**		4.5	**5.5**				mA
Power Consumption, No Load	$V_S = \pm 15$ V	AD707		75	**90**		75	**90**		75	**90**	mW
		AD708		135	**165**		135	**165**				mW
	$V_S = \pm 3$ V	AD707		7.5	**9.0**		7.5	**9.0**		7.5	**9.0**	mW
		AD708		12	**18**		12	**18**				mW
		Both	±3		±18	±3		±18	±3		±18	V

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Matching is defined as the difference between parameters of the two amplifiers.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±22 V
Internal Power Dissipation[2] ..... 500 mW
Input Voltage ..... $\pm V_S$
Differential Input Voltage ..... $+V_S$ and $-V_S$
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range (N, R) ..... –65°C to +125°C
Storage Temperature Range (Q, H) ..... –65°C to +150°C
Operating Temperature Range
AD70xJ/K ..... 0°C to +70°C
AD70xA/B ..... –40°C to +85°C
AD70xS/T ..... –55°C to +125°C
Lead Temperature Range
(Soldering 60 sec) ..... +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air: 8-pin plastic package, θ_{JA} = 165°C/Watt; 8-pin cerdip package, θ_{JA} = 110°C/Watt; 8-pin small outline package, θ_{JA} = 155°C/Watt; 8-pin header package, θ_{JA} = 200°C/Watt.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD707AH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD707AQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD707AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD707AR-REEL	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD707AR-REEL7	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD707BH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD707BQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD707CH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD707CQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD707JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD707JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD707JR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD707JR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD707KN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD707KR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD707KR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD707KR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD707SH/883B	–55°C to +125°C	8-Pin Metal Can	H-08A
AD707SQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD707TH/883B	–55°C to +125°C	8-Pin Metal Can	H-08A
AD707TQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD708AH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD708AQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD708BH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD708BQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD708JCHIPS	0°C to +70°C	Bare Die	
AD708JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD708SQ	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD708SQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD707 and AD708 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Precision, Low Cost, High Speed, BiFET Op Amps

AD711/AD712/AD713

FEATURES

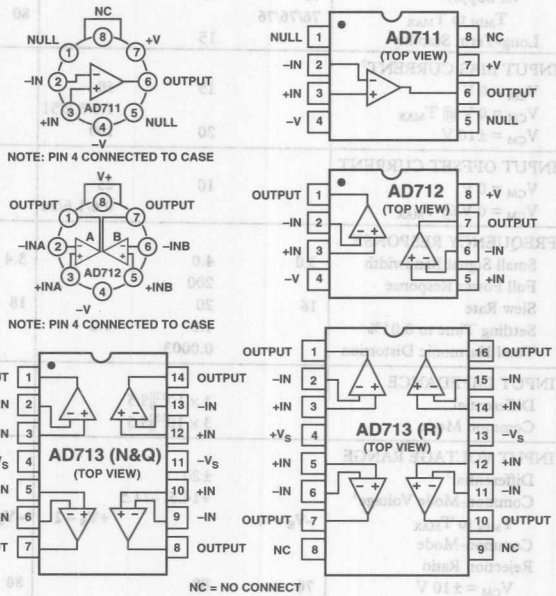
Enhanced Replacements for
TL081; TL082; TL084
LF411; LF412; LF347

AC PERFORMANCE
Settles to ±0.01% in 1.0 µs
16 V/µs min Slew Rate
3 MHz min Unity Gain Bandwidth
0.0003% Total Harmonic Distortion (THD)

DC PERFORMANCE
Low Offset Voltages
(0.25 mV max—AD711C)
(0.30 mV max—AD712C)
(0.50 mV max—AD713K)
Low Offset Drift
(3 µV/°C max—AD711C)
(5 µV/°C max—AD712C)
200 V/mV min Open-Loop Gain
Low Noise (0.1 Hz to 10 Hz)
(4 µV p-p max—AD711C)
(4 µV p-p max—AD712C)
MIL-STD-883B Versions Available
Single: AD711
Dual: AD712
Quad: AD713

APPLICATIONS
Active Filters
Output Buffers for 12- and 14-Bit DACs
Input Buffers for Precision ADCs
Photo Diode Preamplifier Applications

CONNECTION DIAGRAMS



PRODUCT DESCRIPTION

The AD711/AD712/AD713 series are high speed, precision, monolithic operational amplifiers offering high performance at very modest prices. Their very low offset voltage and offset voltage drift are results of advanced laser wafer trimming technology. These benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of these op amps make them suitable for active filter designs. With a slew rate of 16 V/µs and settling times of 1 µs to 0.01%, the AD711/AD712/AD713 series is ideal for use as buffers for 12-bit D/A and A/D converters and as high speed integrators. The settling time is unmatched by any similar IC amplifier. The combination of excellent noise performance and low input current also make these amplifiers useful for photo diode preamplifiers. Common-mode rejection of 88 dB and open loop gain of 400 V/mV insure 12-bit performance even in high speed, unity gain, buffer circuits. These amplifiers are pinned out in standard op amp configurations and are available in various performance grades. The "J" and "K" grades are rated over the commercial temperature range of 0°C to +70°C. The "A," "B," and "C" grades are rated over the industrial temperature range of –40°C to +85°C. The "S" and "T" grades are rated over the military temperature range of –55°C to +125°C. Select versions are available processed to MIL-STD-883B, Rev. C or Standard Military Drawings.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. The AD711/AD712/AD713 series offers excellent overall performance at competitive prices.
2. Analog Devices' advanced processing technology and 100% testing guarantees a low input offset voltage (0.25 mV max AD711C; 0.30 mV max AD712C). Input offset voltages are specified in the warmed up condition. Analog Devices' laser wafer drift trimming process reduces input offset voltage drifts to 3 µV/°C (AD711C) or 5 µV/°C (AD712C).
3. Along with precision dc performance, the AD711, AD712 and AD713 offer excellent dynamic response. They settle to ±0.01% in 1 µs and have a 100% tested minimum slew rate of 16 V/µs. This makes these parts ideal for DAC and ADC buffers, which require a combination of superior ac and dc performance.
4. Analog Devices' well matched, ion-implanted JFETs ensure low input bias currents and low input offset currents. Both input bias and offset currents are guaranteed in the warmed-up condition.

AD711/AD712/AD713–SPECIFICATIONS

AD711 (V_S = ±15 V @ T_A = +25°C unless otherwise noted)

Parameter	J/A/S Min	J/A/S Typ	J/A/S Max	K/B/T Min	K/B/T Typ	K/B/T Max	C Min	C Typ	C Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	2/1/1		0.2	0.5		0.10	0.25	mV
T_{MIN} to T_{MAX}			3/2/2			1.0			0.45	mV
vs. Temp		7	20/20/20		5	10		2	5	µV/°C
vs. Supply	76	95		80	100		86	110		dB
T_{MIN} to T_{MAX}	76/76/76			80			86			dB
Long-Term Stability		15			15			15		µV/Month
INPUT BIAS CURRENT[2]										
V_{CM} = 0 V		15	50		15	50		15	25	pA
V_{CM} = 0 V @ T_{MAX}			1.1/3.2/51			1.1/3.2/51			1.6	nA
V_{CM} = ±10 V		20	100		20	100		20	50	pA
INPUT OFFSET CURRENT										
V_{CM} = 0 V		10	25		5	25		5	10	pA
V_{CM} = 0 V @ T_{MAX}			0.6/1.6/26			0.6/1.6/26			0.65	nA
FREQUENCY RESPONSE										
Small Signal Bandwidth	3.0	4.0		3.4	4.0		3.4	4.0		MHz
Full Power Response		200			200			200		kHz
Slew Rate	16	20		18	20		18	20		V/µs
Settling Time to 0.01%		1.0	1.2		1.0	1.2		1.0	1.2	µs
Total Harmonic Distortion		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω|pF
Common Mode		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω|pF
INPUT VOLTAGE RANGE										
Differential[3]		±20			±20			±20		V
Common-Mode Voltage[4]		+14.5, –11.5			+14.5, –11.5			+14.5, –11.5		
T_{MIN} to T_{MAX}	$-V_S + 4$		$+V_S - 2$	$-V_S + 4$		$+V_S - 2$	$-V_S + 4$		$+V_S - 2$	V
Common-Mode Rejection Ratio										
V_{CM} = ±10 V	76	88		80	88		86	94		dB
T_{MIN} to T_{MAX}	76/76/76	84		80	84		86	90		dB
V_{CM} = ±11 V	70	84		76	84		76	90		dB
T_{MIN} to T_{MAX}	70/70/70	80		74	80		74	84		dB
INPUT VOLTAGE NOISE		2			2			2	4	µV p-p
		45			45			45		nV/√Hz
		22			22			22		nV/√Hz
		18			18			18		nV/√Hz
		16			16			16		nV/√Hz
INPUT CURRENT NOISE		0.01			0.01			0.01		pA/√Hz
OPEN-LOOP GAIN	150	400		200	400		200	400		V/mV
	100/100/100			100			100			V/mV
OUTPUT CHARACTERISTICS										
Voltage	+13, –12.5	+13.9, –13.3		+13, –12.5	+13.9, –13.3		+13, –12.5	+13.9, –13.3		V
	±12/±12/±12	+13.8, –13.1		±12	+13.8, –13.1		±12	+13.8, –13.1		V
Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		2.5	3.4		2.5	3.0		2.5	2.8	mA

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.

[4]Typically exceeding –14.1 V negative common-mode voltage on either input results in an output phase reversal.

Specifications subject to change without notice.

AD712 (V_S = ±15 V @ T_A = +25°C unless otherwise noted)

Parameter	J/A/S Min	J/A/S Typ	J/A/S Max	K/B/T Min	K/B/T Typ	K/B/T Max	C Min	C Typ	C Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	3/1/1		0.2	1.0/0.7/0.7		0.1	0.3	mV
T_{MIN} to T_{MAX}			4/2/2			2.0/1.5/1.5			0.6	mV
vs. Temp		7	20/20/20		7	10		3	5	µV/°C
vs. Supply	76	95		80	100		86	110		dB
T_{MIN} to T_{MAX}	76/76/76			80			86			dB
Long-Term Stability		15			15			15		µV/Month
INPUT BIAS CURRENT[2]										
V_{CM} = 0 V		25	75		20	75		20	50	pA
V_{CM} = 0 V @ T_{MAX}		0.6/1.6/26	1.7/4.8/77		0.5/1.3/20	1.7/4.8/77		1.3	3.2	nA
V_{CM} = ±10 V			100			100			75	pA
INPUT OFFSET CURRENT										
V_{CM} = 0 V		10	25		5	25		5	10	pA
V_{CM} = 0 V @ T_{MAX}		0.3/0.7/11	0.6/1.6/26		0.1/0.3/5	0.6/1.6/26		0.3	0.7	nA
MATCHING CHARACTERISTICS										
Input Offset Voltage			3/1/1			1.0/0.7/0.7			0.3	mV
T_{MIN} to T_{MAX}			4/2/2			2.0/1.5/1.5			0.6	mV
Input Offset Voltage Drift			20/20/20			10			5	µV/°C
Input Bias Current			25			25			10	pA
Crosstalk @ f = 1 kHz		120			120			120		dB
@ f = 100 kHz		90			90			90		dB
FREQUENCY RESPONSE										
Small Signal Bandwidth	3.0	4.0		3.4	4.0		3.4	4.0		MHz
Full Power Response		200			200			200		kHz
Slew Rate	16	20		18	20		18	20		V/µs
Settling Time to 0.01%		1.0	1.2		1.0	1.2		1.0	1.2	µs
Total Harmonic Distortion		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12}\|\|5.5$			$3 \times 10^{12}\|\|5.5$			$3 \times 10^{12}\|\|5.5$		Ω||pF
Common Mode		$3 \times 10^{12}\|\|5.5$			$3 \times 10^{12}\|\|5.5$			$3 \times 10^{12}\|\|5.5$		Ω||pF
INPUT VOLTAGE RANGE										
Differential[3]		±20			±20			±20		V
Common-Mode Voltage[4]		+14.5, –11.5			+14.5, –11.5			+14.5, –11.5		
T_{MIN} to T_{MAX}	$-V_S + 4$		$+V_S - 2$	$-V_S + 4$		$+V_S$ –2	$-V_S + 4$		$+V_S - 2$	V
Common-Mode Rejection Ratio										
V_{CM} = ±10 V	76	88		80	88		86	94		dB
T_{MIN} to T_{MAX}	76/76/76	84		80	84		86	90		dB
V_{CM} = ±11 V	70	84		76	84		76	90		dB
T_{MIN} to T_{MAX}	70/70/70	80		74	80		74	84		dB
INPUT VOLTAGE NOISE		2			2			2		µV p-p
		45			45			45		nV/√Hz
		22			22			22		nV/√Hz
		18			18			18		nV/√Hz
		16			16			16		nV/√Hz
INPUT CURRENT NOISE		0.01			0.01			0.01		pA/√Hz
OPEN-LOOP GAIN	150	400		200	400		200	400		V/mV
	100/100/100			100			100			V/mV
OUTPUT CHARACTERISTICS										
Voltage	+13, –12.5	+13.9, –13.3		+13, –12.5	+13.9, –13.3		+13, –12.5	+13.9, –13.3		V
	±12/±12/±12	+13.8, –13.1		±12	+13.8, –13.1		±12	+13.8, –13.1		V
Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		5.0	6.8		5.0	6.0		5.0	5.6	mA

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[3]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.
[4]Typically exceeding –14.1 V negative common-mode voltage on either input results in an output phase reversal.

Specifications subject to change without notice.

Parameter	Conditions	J/A/S Min	J/A/S Typ	J/A/S Max	K/B/T Min	K/B/T Typ	K/B/T Max	Units
INPUT OFFSET VOLTAGE[1]								
Initial Offset			0.3	**1.5**		0.2	**0.5**	mV
Offset	T_{MIN} to T_{MAX}		0.5	2/2/**2**		0.4	**0.7/0.7/1.0**	mV
vs. Temp			5			5	20/**20/15**	µV/°C
vs. Supply		**78**	95		**84**	100		dB
vs. Supply	T_{MIN} to T_{MAX}	76/76/**76**	95		**84**	100		dB
Long-Term Stability			15			15		µV/
Month								
INPUT BIAS CURRENT[2]	V_{CM} = 0 V		40	**150**		40	**75**	pA
	V_{CM} = 0 V @ T_{MAX}			3.4/9.6/154			1.7/4.8/**77**	nA
	V_{CM} = ±10 V		55	200		55	**120**	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		10	**75**		10	**35**	pA
	V_{CM} = 0 V @ T_{MAX}			1.7/4.8/77			0.8/2.2/**36**	nA
MATCHING CHARACTERISTICS								
Input Offset Voltage			0.5	**1.8**		0.4	**0.8**	mV
Input Offset Voltage	T_{MIN} to T_{MAX}		0.7	2.3/2.3/**2.3**		0.6	**1.0/1.0/1.3**	mV
Input Offset Voltage Drift			8			6	25	µV/°C
Input Bias Current			10	**100**		10	**35**	pA
Crosstalk	f = 1 kHz			–130			–130	dB
	f = 100 kHz			–95			–95	dB
FREQUENCY RESPONSE								
Small Signal Bandwidth	Unity Gain	3.0	4.0		3.4	4.0		MHz
Full Power Response	V_O = 20 V p-p		200			200		kHz
Slew Rate	Unity Gain	**16**	20		**18**	20		V/µs
Settling Time to 0.01%			1.0	1.2		1.0	1.2	µs
Total Harmonic Distortion	f = 1 kHz; $R_L \geq 2$ kΩ; V_O = 3 V rms		0.0003			0.0003		%
INPUT IMPEDANCE								
Differential			$3\times10^{12}\|\|5.5$			$3\times10^{12}\|\|5.5$		Ω||pF
Common Mode			$3\times10^{12}\|\|5.5$			$3\times10^{12}\|\|5.5$		Ω||pF
INPUT VOLTAGE RANGE								
Differential[3]			±20			±20		V
Common-Mode Voltage[4]			+14.5, –11.5			+14.5, –11.5		V
	T_{MIN} to T_{MAX}	–11		+13	**–11**		+13	V
Common Mode	V_{CM} = ±10 V	**78**	88		**84**	94		dB
Rejection Ratio	T_{MIN} to T_{MAX}	76/76/**76**	84		**82**	90		dB
	V_{CM} = ±11 V	**72**	84		**78**	90		dB
	T_{MIN} to T_{MAX}	70/70/**70**	80		**74**	84		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		2			2		µV p-p
	f = 10 Hz		45			45		nV/√Hz
	f = 100 Hz		22			22		nV/√Hz
	f = 1 kHz		18			18		nV/√Hz
	f = 10 kHz		16			16		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.01			0.01		pA/√Hz
OPEN-LOOP GAIN	V_O = ±10 V; $R_L \geq 2$ kΩ	**150**	400		**200**	400		V/mV
	T_{MIN} to T_{MAX}	100/100/**100**			**100**			V/mV
OUTPUT CHARACTERISTICS								
Voltage	$R_L \geq 2$ kΩ	+13, –12.5	+13.9, –13.3		+13, –12.5	+13.9, –13.3		V
	T_{MIN} to T_{MAX}	±12/±12/**±12**	+13.8, –13.1		**±12**	+13.8, –13.1		V
Current	Short Circuit		25			25		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			10.0	**13.5**		10.0	**12.0**	mA
TRANSISTOR COUNT	# of Transistors		120			120		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.

[4]Typically exceeding –14.1 V negative common-mode voltage on either input results in an output phase reversal.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

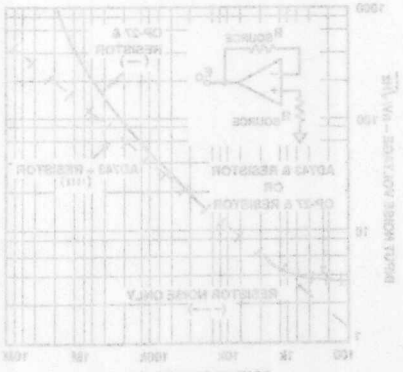
Supply Voltage ..... ±18 V
Internal Power Dissipation[2]
Input Voltage ..... $\pm V_S$
Differential Input Voltage ..... $+V_S$ and $-V_S$
Output Short Circuit Duration (Single Amplifier) ... Indefinite
Storage Temperature Range (N, R) ..... –65°C to +125°C
Storage Temperature Range (Q) ..... –65°C to +150°C
Operating Temperature Range
AD71xJ/K ..... 0°C to +70°C
AD71xA/B ..... –40°C to +85°C
AD71xS/T ..... –55°C to +125°C
Lead Temperature Range (Soldering 60 sec) ..... +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:

8-Pin Plastic Package	θ_{JA} = 165°C/Watt
8-Pin Cerdip Package	θ_{JA} = 110°C/Watt
8-Pin Metal Can Package	θ_{JA} = 150°C/Watt
8-Pin Small Outline Package	θ_{JA} = 155°C/Watt
14-Pin Plastic Package	θ_{JA} = 150°C/Watt
14-Pin Cerdip Package	θ_{JA} = 110°C/Watt
16-Pin SOIC Package	θ_{JA} = 100°C/Watt



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD711AH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD711AQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD711BH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD711BQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD711CH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD711CQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD711JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD711JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711JR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711JR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711KN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD711KR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711KR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711KR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711SCHIPS	–55°C to +125°C	Bare Die	
AD711SQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD711TQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD712ACHIPS	–40°C to +85°C	Bare Die	
AD712AH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD712AQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD712BH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD712BQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD712CH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD712CQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD712JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD712JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712JR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712JR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712KN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD712KR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712KR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712KR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712SCHIPS	–55°C to +125°C	Bare Die	
AD712SQ	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD712SQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD712TQ	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD712TQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD713AQ	–40°C to +85°C	14-Pin Ceramic DIP	Q-14
AD713BQ	–40°C to +85°C	14-Pin Ceramic DIP	Q-14
AD713JCHIPS	0°C to +70°C	Bare Die	
AD713JN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD713JR-16	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713JR-16-REEL	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713JR-16-REEL7	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713KN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD713SCHIPS	–55°C to +125°C	Bare Die	
AD713SQ	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713SQ/883B	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713TQ	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713TQ/883B	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
5962-9063301MCA	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
5962-9063302MCA	–55°C to +125°C	14-Pin Ceramic DIP	Q-14

*For outline information see Package Information section.

9

Ultralow Noise BiFET Op Amp

AD743

FEATURES

ULTRALOW NOISE PERFORMANCE
- 2.9 nV/$\sqrt{Hz}$ at 10 kHz
- 0.38 μV p–p, 0.1 to 10 Hz
- 6.9 fA/$\sqrt{Hz}$ Current Noise at 1 kHz

EXCELLENT DC PERFORMANCE
- 0.5 mV max Offset Voltage
- 250 pA max Input Bias Current
- 1000 V/mV min Open-Loop Gain

AC PERFORMANCE
- 2.8 V/μs Slew Rate
- 4.5 MHz Unity-Gain Bandwidth
- THD = 0.0003% @ 1 kHz
- Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS
- Sonar Preamplifiers
- High Dynamic Range Filters (>140 dB)
- Photodiode and IR Detector Amplifiers
- Accelerometers

PRODUCT DESCRIPTION

The AD743 is an ultralow noise precision, FET input, monolithic operational amplifier. It offers a combination of the ultralow voltage noise generally associated with bipolar input op amps and the very low input current of a FET-input device. Furthermore, the AD743 does not exhibit an output phase reversal when the negative common-mode voltage limit is exceeded.

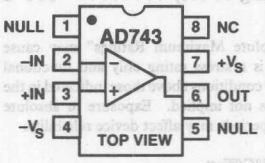
The AD743's guaranteed, maximum input voltage noise of 4.0 nV/$\sqrt{Hz}$ at 10 kHz is unsurpassed for a FET-input monolithic op amp, as is the maximum 1.0 μV p–p, 0.1 to 10 Hz noise. The AD743 also has excellent dc performance with 250 pA maximum input bias current and 0.5 mV maximum offset voltage.

The AD743 is specifically designed for use as a preamp in capacitive sensors, such as ceramic hydrophones. It is available in five performance grades. The AD743J and AD743K are rated over the commercial temperature range of 0°C to +70°C. The AD743A and AD743B are rated over the industrial temperature range of −40°C to +85°C. The AD743S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

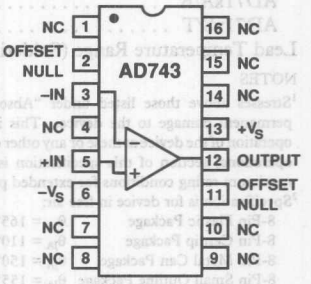
The AD743 is available in 8-pin plastic mini-DIP, 8-pin cerdip, 16-pin SOIC, or in chip form.

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) and 8-Pin Cerdip (Q) Packages

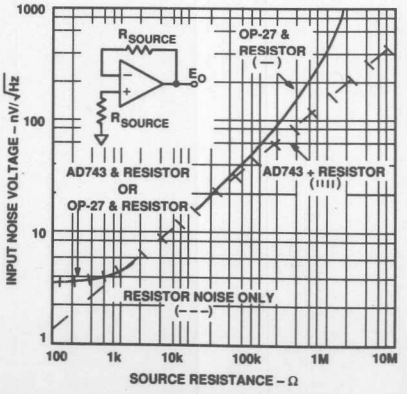


16-Pin SOIC (R) Package



PRODUCT HIGHLIGHTS

1. The low offset voltage and low input offset voltage drift of the AD743 coupled with its ultralow noise performance mean that the AD743 can be used for upgrading many applications now using bipolar amplifiers.
2. The combination of low voltage and low current noise make the AD743 ideal for charge sensitive applications such as accelerometers and hydrophones.
3. The low input offset voltage and low noise level of the AD743 provide >140 dB dynamic range.
4. The typical 10 kHz noise level of 2.9 nV/$\sqrt{Hz}$ permits a three op amp instrumentation amplifier, using three AD743s, to be built which exhibits less than 4.2 nV/$\sqrt{Hz}$ noise at 10 kHz and which has low input bias currents.



Input Noise Voltage vs. Source Resistance

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD743J/A Min	AD743J/A Typ	AD743J/A Max	AD743K/B Min	AD743K/B Typ	AD743K/B Max	AD743S Min	AD743S Typ	AD743S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.25	1.0/0.8		0.1	0.5/0.25		0.25	1.0	mV
Initial Offset	T_{min} to T_{max}			1.5			1.0/0.50			2.0	mV
vs. Temp.	T_{min} to T_{max}		2			1			2		μV/°C
vs. Supply (PSRR)	12 V to 18 V[2]	90	96		100	106		90	96		dB
vs. Supply (PSRR)	T_{min} to T_{max}	88			98	100		88			dB
INPUT BIAS CURRENT[3]											
Either Input	V_{CM} = 0 V		150	400		150	250		150	400	pA
Either Input @ T_{max}	V_{CM} = 0 V			8.8/25.6			5.5/16			413	nA
Either Input	V_{CM} = +10 V		250	600		250	400		300	600	pA
Either Input, V_S = ±5 V	V_{CM} = 0 V		30	200		30	125		30	200	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		40	150		30	75		40	150	pA
Offset Current @ T_{max}	V_{CM} = 0 V			2.2/6.4			1.1/3.2			102	nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	G = −1		4.5			4.5			4.5		MHz
Full Power Response	V_O = 20 V p-p		25			25			25		kHz
Slew Rate, Unity Gain	G = −1		2.8			2.8			2.8		V/μs
Settling Time to 0.01%			6			6			6		μs
Total Harmonic Distortion[4]	f = 1 kHz G = −1		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE											
Differential			1 × 10^{10}‖20			1 × 10^{10}‖20			1 × 10^{10}‖20		Ω‖pF
Common Mode			3 × 10^{11}‖18			3 × 10^{11}‖18			3 × 10^{11}‖18		Ω‖pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+13.3, −10.7			+13.3, −10.7			+13.3, −10.7		V
Over Max Operating Range[6]		−10		+12	−10		+12	−10		+12	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	80	95		90	102		80	95		dB
	T_{min} to T_{max}	78			88			78			dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		0.38			0.38	1.0		0.38		μV p-p
	f = 10 Hz		5.5			5.5	10.0		5.5		nV/√Hz
	f = 100 Hz		3.6			3.6	6.0		3.6		nV/√Hz
	f = 1 kHz		3.2	5.0		3.2	5.0		3.2	5.0	nV/√Hz
	f = 10 kHz		2.9	4.0		2.9	4.0		2.9	4.0	nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		6.9			6.9			6.9		fA/√Hz
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD} ≥ 2 kΩ	1000	4000		2000	4000		1000	4000		V/mV
	T_{min} to T_{max}	800			1800			800			V/mV
	R_{LOAD} = 600 Ω		1200			1200			1200		V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 600 Ω	+13, −12			+13, −12			+13, −12			V
	R_{LOAD} ≥ 600 Ω		+13.6, −12.6			+13.6, −12.6			+13.6, −12.6		V
	T_{min} to T_{max}	+12, −10			+12, −10			+12, −10			V
	R_{LOAD} ≥ 2 kΩ	±12	+13.8, −13.1		±12	+13.8, −13.1		±12	+13.8, −13.1		V
Current	Short Circuit	20	40		20	40		20	40		mA
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±4.8		±18	±4.8		±18	±4.8		±18	V
Quiescent Current			8.1	10.0		8.1	10.0		8.1	10.0	mA
TRANSISTOR COUNT	# of Transistors		50			50			50		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Test conditions: $+V_S$ = 15 V, $-V_S$ = 12 V to 18 V and $+V_S$ = 12 V to +18 V, $-V_S$ = 15 V.
[3]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[4]Gain = −1, R_L = 2 kΩ, C_L = 10 pF.
[5]Defined as voltage between inputs, such that neither exceeds ±10 V from common.
[6]The AD743 does not exhibit an output phase reversal when the negative common-mode limit is exceeded.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD743J/K . . . . . 0°C to +70°C
AD743A/B . . . . . −40°C to +85°C
AD743S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . . 300°C

operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]8-pin plastic package: θ_{JA} = 100°C/Watt, θ_{JC} = 50°C/Watt
8-pin cerdip package: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/Watt
16-pin plastic SOIC package: θ_{JA} = 100°C/Watt, θ_{JC} = 30°C/Watt

ESD SUSCEPTIBILITY

An ESD classification per method 3015.6 of MIL STD 883C has been performed on the AD743. The AD743 is a class 1 device, passing at 1000 V and failing at 1500 V on null pins 1 and 5, when tested, using an IMCS 5000 automated ESD tester. Pins other than null pins fail at greater than 2500 V.

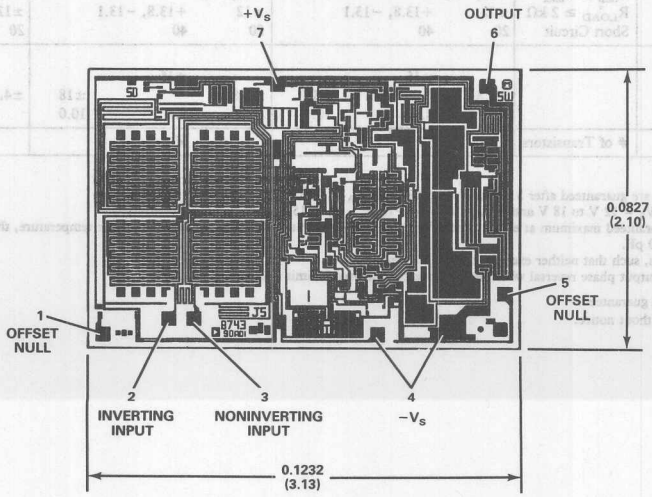
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD743JN	0°C to +70°C	N-8
AD743KN	0°C to +70°C	N-8
AD743AN	−40°C to +85°C	N-8
AD743JR-16	0°C to +70°C	R-16
AD743KR-16	0°C to +70°C	R-16
AD743AR-16	−40°C to +85°C	R-16
AD743AQ	−40°C to +85°C	Q-8
AD743BQ	−40°C to +85°C	Q-8
AD743SQ	−55°C to +125°C	Q-8
AD743SQ/883B	−55°C to +125°C	Q-8
AD743JCHIPS	0°C to +70°C	Die
AD743JR-16-REEL	0°C to +70°C	Tape & Reel
AD743KR-16-REEL	0°C to +70°C	Tape & Reel
AD743AR-16-REEL	−40°C to +85°C	Tape & Reel

*N = Plastic DIP; R = Small Outline IC; Q = Cerdip. For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Precision, 500ns Settling BiFET Op Amp

AD744

FEATURES

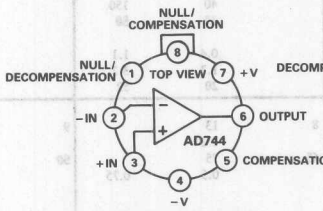
AC PERFORMANCE
- 500ns Settling to 0.01% for 10V Step
- 1.5μs Settling to 0.0025% for 10V Step
- 75V/μs Slew Rate
- 0.0003% Total Harmonic Distortion (THD)
- 13MHz Gain Bandwidth – Internal Compensation
- >200MHz Gain Bandwidth (G = 1000) External Decompensation
- >1000pF Capacitive Load Drive Capability with 10V/μs Slew Rate – External Compensation

DC PERFORMANCE
- 0.25mV max Offset Voltage (AD744C)
- 3μV/°C max Drift (AD744C)
- 250V/mV min Open-Loop Gain (AD744B)
- 4μV p-p max Noise, 0.1Hz to 10Hz (AD744C)
- Available in Plastic Mini-DIP, Plastic SOIC, Hermetic Cerdip, Hermetic Metal Can Packages and Chip Form
- MIL-STD-883B Processing Available
- Surface Mount (SOIC) Package Available in Tape and Reel in Accordance with EIA–481A Standard

APPLICATIONS
- Output Buffers for 12-Bit, 14-Bit and 16-Bit DACs, ADC Buffers, Cable Drivers, Wideband Preamplifiers and Active Filters

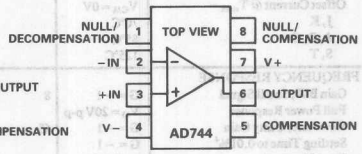
CONNECTION DIAGRAMS

TO-99 (H) Package



NOTE: PIN 4 CONNECTED TO CASE

Plastic Mini-DIP (N), Small Outline (R) and Cerdip (Q) Packages



PRODUCT DESCRIPTION

The AD744 is a fast-settling, precision, FET input, monolithic operational amplifier. It offers the excellent dc characteristics of the AD711 BiFET family with enhanced settling, slew rate, and bandwidth. The AD744 also offers the option of using custom compensation to achieve exceptional capacitive load drive capability.

The single-pole response of the AD744 provides fast settling: 500ns to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12-bit, 14-bit or 16-bit DACs and ADCs. Furthermore, the AD744's low total harmonic distortion (THD) level of 0.0003% and gain bandwidth product of 13MHz make it an ideal amplifier for demanding audio applications. It is also an excellent choice for use in active filters in 12-bit, 14-bit and 16-bit data acquisition systems.

The AD744 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of two or greater. External compensation may be applied to the AD744 for stable operation as a unity gain follower. External compensation also allows the AD744 to drive 1000pF capacitive loads, slewing at 10V/μs with full stability. Alternatively, external decompensation may be used to increase the gain bandwidth of the AD744 to over 200MHz at high gains. This makes the AD744 ideal for use as ac preamps in digital signal processing (DSP) front ends.

The AD744 is available in seven performance grades. The AD744J and AD744K are rated over the commercial temperature range of 0 to +70°C. The AD744A, AD744B and AD744C are rated over the industrial temperature range of −40°C to +85°C. The AD744S and AD744T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes a 168-hour burn-in, as well as other environmental and physical tests.

The AD744 is available in an 8-pin plastic mini-DIP, 8-pin small outline, 8-pin cerdip or TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD744 is a high-speed BiFET op amp that offers excellent performance at competitive prices. It outperforms the OPA602/OPA606, LF356 and LF400.
2. The AD744 offers exceptional dynamic response. It settles to 0.01% in 500ns and has a 100% tested minimum slew rate of 50V/μs (AD744B).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs provide outstanding dc precision. Input offset voltage, input bias current, and input offset current are specified in the warmed-up condition; all are 100% tested.
4. The AD744 has a guaranteed and tested maximum voltage noise of 4μV p-p, 0.1Hz to 10Hz (AD744C).

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD744—SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD744J/A/S Min	AD744J/A/S Typ	AD744J/A/S Max	AD744K/B/T Min	AD744K/B/T Typ	AD744K/B/T Max	AD744C Min	AD744C Typ	AD744C Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.3	1.0		0.25	0.5		0.10	0.25	mV
Offset	$T_{min}-T_{max}$			2/2/2			1.0			0.45	mV
vs. Temp			5	20/20/20		5	10		2	3	μV/°C
vs. Supply[2]		82	95		88	100		92	110		dB
vs. Supply	$T_{min}-T_{max}$	82/82/82			88			92			dB
Long-Term Stability			15			15			15		μV/month
INPUT BIAS CURRENT[3]											
Either Input	$V_{CM}=0V$		30	100		30	100		30	50	pA
Either Input @ T_{max} =	$V_{CM}=0V$										
J, K	70°C		0.7	2.3		0.7	2.3				nA
A, B, C	85°C		1.9	6.4		1.9	6.4		1.9	3.2	nA
S, T	125°C		31	102		31	102				nA
Either Input	$V_{CM}=+10V$		40	150		40	150		40	100	pA
Offset Current	$V_{CM}=0V$		20	50		10	50		10	20	pA
Offset Current @ T_{max} =	$V_{CM}=0V$										
J, K	70°C		0.4	1.1		0.2	1.1				nA
A, B, C	85°C		1.3	3.2		0.6	3.2		0.6	1.3	nA
S, T	125°C		20	52		10	52				nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	$G=-1$	8	13		9	13		9	13		MHz
Full Power Response	$V_O=20V$ p-p		1.2			1.2			1.2		MHz
Slew Rate, Unity Gain	$G=-1$	45	75		50	75		50	75		V/μs
Settling Time to 0.01%[4]	$G=-1$		0.5	0.75		0.5	0.75		0.5	0.75	μs
Total Harmonic Distortion	f = 1kHz, R1≥2kΩ, $V_O=3V$ rms		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE											
Differential			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$		Ω|pF
Common Mode			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$		Ω|pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+14.5, −11.5			+14.5, −11.5			+14.5, −11.5		V
Over Max Operating Range[6]		−11		+13	−11		+13	−11		+13	V
Common-Mode Rejection Ratio	$V_{CM}=\pm10V$	78	88		82	88		86	94		dB
	T_{min} to T_{max}	76/76/76	84		80	84		86	90		dB
	$V_{CM}=\pm11V$	72	84		78	84		80	90		dB
	T_{min} to T_{max}	70/70/70	80		74	80		76	84		dB
INPUT VOLTAGE NOISE	0.1 to 10Hz		2			2			2	4	μV p-p
	f = 10Hz		45			45			45		nV/√Hz
	f = 100Hz		22			22			22		nV/√Hz
	f = 1kHz		18			18			18		nV/√Hz
	f = 10kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE	f = 1kHz		0.01			0.01			0.01		pA/√Hz
OPEN LOOP GAIN[7]	$V_O=\pm10V$										
	$R_{LOAD}\geq2k\Omega$	200	400		250	400		250	400		V/mV
	T_{min} to T_{max}	100/100/100			100			150			V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD}\geq2k\Omega$	+13, −12.5	+13.9, −13.3		+13, −12.5	+13.9, −13.3		+13, −12.5	+13.9, −13.3		V
	T_{min} to T_{max}	±12/±12/±12	+13.8, −13.1		±12	+13.8, −13.1		±12	+13.8, −13.1		V
Current	Short-Circuit		25			25			25		mA
Capacitive Load[8]	Gain = −1			1000			1000			1000	pF
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current			3.5	5.0		3.5	4.0		3.5	4.0	mA
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial (0 to +70°C)			AD744J			AD744K					
Industrial (−40°C to +85°C)			AD744A			AD744B			AD744C		
Military (−55°C to +125°C)			AD744S			AD744T					
PACKAGE OPTIONS[9]											
8-Pin Plastic Mini-DIP (N-8) and SOIC (R-8)			AD744JN, AD744JR			AD744KN, AD744KR					
8-Pin Cerdip (Q-8)			AD744AQ			AD744BQ			AD744CQ		
TO-99 Metal Can (H-08A)			AD744AH								
Tape and Reel			AD744JR-REEL			AD744KR-REEL					
Chips Available			AD744JChips								

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A=+25°C$.

[2]PSRR test conditions: $+V_S=15V$, $-V_S=-12V$ to $-18V$ and $+V_S=12V$ to $18V$, $-V_S=-15V$.

[3]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A=+25°C$. For higher temperature, the current doubles every 10°C.

[4]Gain = −1, $R_L=2k$, $C_L=10pF$, refer to Figure 25.

[5]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[6]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.

[7]Open-Loop Gain is specified with V_{OS} both nulled and unnulled.

[8]Capacitive load drive specified for $C_{COMP}=20pF$ with the device connected as shown in Figure 32. Under these conditions, slew rate = 14V/μs and 0.01% settling time = 1.5μs typical. Refer to Table II for optimum compensation while driving a capacitive load.

[9]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation[2]	500mW
Input Voltage[3]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (Q, H)	−65°C to +150°C
Storage Temperature Range (N, R)	−65°C to +125°C
Operating Temperature Range	
AD744J/K	0 to +70°C
AD744A/B/C	−40°C to +85°C
AD744S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indited in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

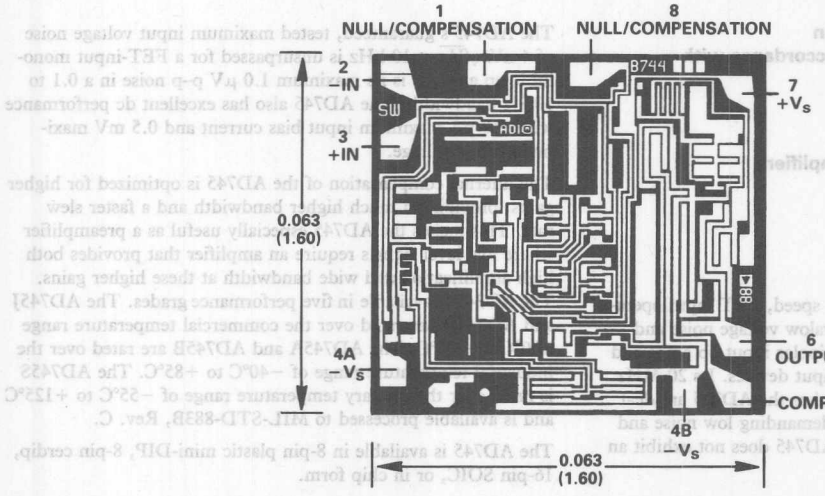
[2]Thermal Characteristics

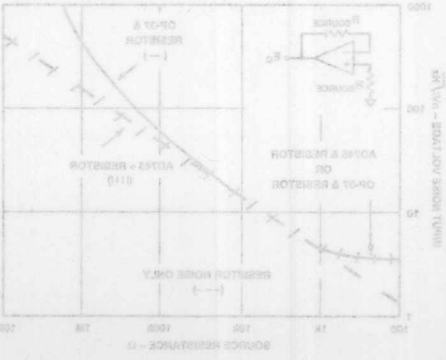
8-Pin Plastic Package: $\theta_{JC} = 33°C/W, \theta_{JA} = 100°C/W$
8-Pin Cerdip Package: $\theta_{JC} = 22°C/W, \theta_{JA} = 110°C/W$
8-Pin Metal Can Package: $\theta_{JC} = 65°C/W, \theta_{JA} = 150°C/W$
8-Pin SOIC Package: $\theta_{JC} = 42°C/W, \theta_{JA} = 160°C/W$

[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).





FEATURES

ULTRALOW NOISE PERFORMANCE
2.9 nV/√Hz at 10 kHz
0.38 μV p–p, 0.1 Hz to 10 Hz
6.9 fA/√Hz Current Noise at 1 kHz

EXCELLENT AC PERFORMANCE
12.5 V/μs Slew Rate
20 MHz Gain Bandwidth Product
THD = 0.0002% @ 1 kHz
Internally Compensated for Gains of +5 (or −4) or Greater

EXCELLENT DC PERFORMANCE
0.5 mV max Offset Voltage
250 pA max Input Bias Current
2000 V/mV min Open Loop Gain
Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

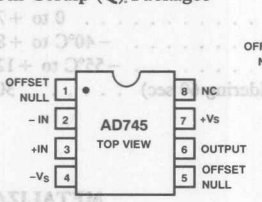
Sonar
Photodiode and IR Detector Amplifiers
Accelerometers
Low Noise Preamplifiers
High Performance Audio

PRODUCT DESCRIPTION

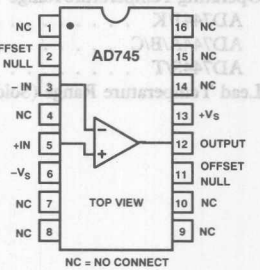
The AD745 is an ultralow noise, high speed, FET input operational amplifier. It offers both the ultralow voltage noise and high speed generally associated with bipolar input op amps and the very low input currents of FET input devices. Its 20 MHz bandwidth and 12.5 V/μs slew rate makes the AD745 an ideal amplifier for high speed applications demanding low noise and high dc precision. Furthermore, the AD745 does not exhibit an output phase reversal.

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) & 8-Pin Cerdip (Q) Packages



16-Pin SOIC (R) Package

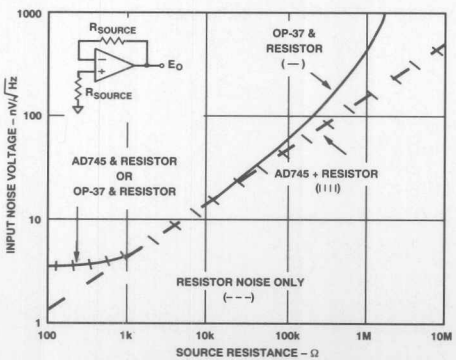


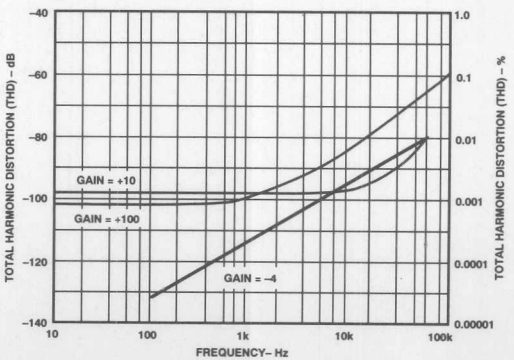
NC = NO CONNECT

The AD745's guaranteed, tested maximum input voltage noise of 4 nV/√Hz at 10 kHz is unsurpassed for a FET-input monolithic op amp, as is its maximum 1.0 μV p–p noise in a 0.1 to 10 Hz bandwidth. The AD745 also has excellent dc performance with 250 pA maximum input bias current and 0.5 mV maximum offset voltage.

The internal compensation of the AD745 is optimized for higher gains, providing a much higher bandwidth and a faster slew rate. This makes the AD745 especially useful as a preamplifier where low level signals require an amplifier that provides both high amplification and wide bandwidth at these higher gains. The AD745 is available in five performance grades. The AD745J and AD745K are rated over the commercial temperature range of 0°C to +70°C. The AD745A and AD745B are rated over the industrial temperature range of −40°C to +85°C. The AD745S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD745 is available in 8-pin plastic mini-DIP, 8-pin cerdip, 16-pin SOIC, or in chip form.





This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD745J/A Min	AD745J/A Typ	AD745J/A Max	AD745K/B Min	AD745K/B Typ	AD745K/B Max	AD745S Min	AD745S Typ	AD745S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.25	1.0/0.8		0.1	0.5/0.25		0.25	1.0	mV
Initial Offset	T_{min} to T_{max}			1.5			1.0/0.50			2.0	mV
vs. Temp.	T_{min} to T_{max}		2			2			2		μV/°C
vs. Supply (PSRR)	12 V to 18 V[2]	90	96		100	106		90	96		dB
vs. Supply (PSRR)	T_{min} to T_{max}	88			98	105		88			dB
INPUT BIAS CURRENT[3]											
Either Input	V_{CM} = 0 V		150	400		150	250		150	400	pA
Either Input @ T_{max}	V_{CM} = 0 V			8.8/25.6			5.5/16			413	nA
Either Input	V_{CM} = +10 V		250	600		250	400		300	600	pA
Either Input, V_S = ±5 V	V_{CM} = 0 V		30	200		30	125		30	200	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		40	150		30	75		40	150	pA
Offset Current @ T_{max}	V_{CM} = 0 V			2.2/6.4			1.1/3.2			102	nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	G = −4		20			20			20		MHz
Full Power Response	V_O = 20 V p-p		120			120			120		kHz
Slew Rate	G = −4		12.5			12.5			12.5		V/μs
Settling Time to 0.01%			5			5			5		μs
Total Harmonic Distortion[4]	f = 1 kHz G = −4		0.0002			0.0002			0.0002		%
INPUT IMPEDANCE											
Differential			$1 \times 10^{10} \| 20$			$1 \times 10^{10} \| 20$			$1 \times 10^{10} \| 20$		Ω||pF
Common Mode			$3 \times 10^{11} \| 18$			$3 \times 10^{11} \| 18$			$3 \times 10^{11} \| 18$		Ω||pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+13.3, −10.7			+13.3, −10.7			+13.3, −10.7		V
Over Max Operating Range[6]		−10		+12	−10		+12	−10		+12	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	80	95		90	102		80	95		dB
	T_{min} to T_{max}	78			88			78			dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		0.38			0.38	1.0		0.38		μV p-p
	f = 10 Hz		5.5			5.5	10.0		5.5		nV/√Hz
	f = 100 Hz		3.6			3.6	6.0		3.6		nV/√Hz
	f = 1 kHz		3.2	5.0		3.2	5.0		3.2	5.0	nV/√Hz
	f = 10 kHz		2.9	4.0		2.9	4.0		2.9	4.0	nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		6.9			6.9			6.9		fA/√Hz
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD} ≥ 2 kΩ	1000	4000		2000	4000		1000	4000		V/mV
	T_{min} to T_{max}	800			1800			800			V/mV
	R_{LOAD} = 600 Ω		1200			1200			1200		V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 600 Ω	+13, −12			+13, −12			+13, −12			V
	R_{LOAD} ≥ 600 Ω		+13.6, −12.6			+13.6, −12.6			+13.6, −12.6		V
	T_{min} to T_{max}	+12, −10			+12, −10			+12, −10			V
	R_{LOAD} ≥ 2 kΩ	±12	+13.8, −13.1		±12	+13.8, −13.1		±12	+13.8, −13.1		V
Current	Short Circuit	20	40		20	40		20	40		mA
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±4.8		±18	±4.8		±18	±4.8		±18	V
Quiescent Current			8	10.0		8	10.0		8	10.0	mA
TRANSISTOR COUNT	# of Transistors		50			50			50		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Test conditions: $+V_S$ = 15 V, $-V_S$ = 12 V to 18 V and $+V_S$ = 12 V to +18 V, $-V_S$ = 15 V.
[3]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[4]Gain = −4, R_L = 2 kΩ, C_L = 10 pF.
[5]Defined as voltage between inputs, such that neither exceeds ±10 V from common.
[6]The AD745 does not exhibit an output phase reversal when the negative common-mode limit is exceeded.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

9

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic Package . . . . . 1.3 W
  Cerdip Package . . . . . 1.1 W
  SOIC Package . . . . . 1.2 W
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
  AD745J/K . . . . . 0°C to +70°C
  AD745A/B . . . . . −40°C to +85°C
  AD745S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . . 300°C

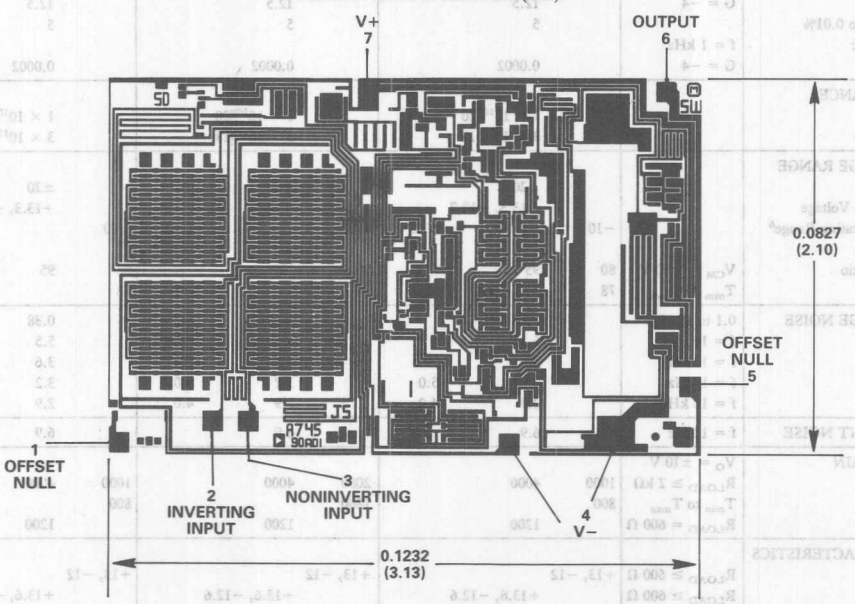
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-pin plastic package: θ_{JA} = 100°C/Watt, θ_{JC} = 50°C/Watt
8-pin cerdip package: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/Watt
16-pin plastic SOIC package: θ_{JA} = 100°C/Watt, θ_{JC} = 30°C/Watt

ESD SUSCEPTIBILITY

An ESD classification per method 3015.6 of MIL STD 883C has been performed on the AD745, which is a class 1 device. Using an IMCS 5000 automated ESD tester, the two null pins will pass at voltages up to 1000 volts, while all other pins will pass at voltages exceeding 2500 volts.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



ORDERING GUIDE

Model	Temperature Range	Package Options*
AD745JN	0°C to +70°C	N-8
AD745KN	0°C to +70°C	N-8
AD745AN	−40°C to +85°C	N-8
AD745JR-16	0°C to +70°C	R-16
AD745AR-16	−40°C to +85°C	R-16
AD745AQ	−40°C to +85°C	Q-8
AD745BQ	−40°C to +85°C	Q-8
AD745SQ	−55°C to +125°C	Q-8
AD745SQ/883B	−55°C to +125°C	Q-8
AD745J Chips	0°C to +70°C	

*N = Plastic DIP; R = Small Outline IC; Q = Cerdip. For outline information see Package Information section.

Dual Precision, 500 ns Settling, BiFET Op Amp

AD746

FEATURES

AC PERFORMANCE
- 500 ns Settling to 0.01% for 10 V Step
- 75 V/μs Slew Rate
- 0.0001% Total Harmonic Distortion (THD)
- 13 MHz Gain Bandwidth
- Internal Compensation for Gains of +2 or Greater

DC PERFORMANCE
- 0.5 mV max Offset Voltage (AD746B)
- 10 μV/°C max Drift (AD746B)
- 175 V/mV min Open Loop Gain (AD746B)
- 2 μV p–p Noise, 0.1 Hz to 10 Hz
- Available in Plastic Mini-DIP, Cerdip and Surface Mount Packages
- Available in Tape and Reel in Accordance with EIA-481A Standard
- MIL-STD-883B Processing also Available
- Single Version: AD744

APPLICATIONS
- Dual Output Buffers for 12- and 14-Bit DACs
- Input Buffers for Precision ADCs, Wideband Preamplifiers and Low Distortion Audio Circuitry

PRODUCT DESCRIPTION

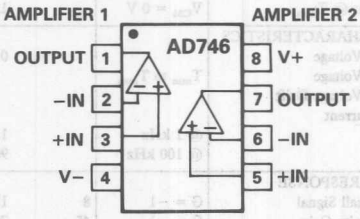
The AD746 is a dual operational amplifier, consisting of two AD744 BiFET op amps on a single chip. These precision monolithic op amps offer excellent dc characteristics plus rapid settling times, high slew rates and ample bandwidths. In addition, the AD746 provides the close matching ac and dc characteristics inherent to amplifiers sharing the same monolithic die.

The single pole response of the AD746 provides fast settling: 500 ns to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12- or 14-bit DACs and ADCs. Furthermore, the AD746's low total harmonic distortion (THD) level of 0.0001% and very close matching ac characteristics make it an ideal amplifier for many demanding audio applications.

The AD746 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of 2 or greater. It is available in four performance grades. The AD746J is rated over the commercial temperature range of 0 to +70°C. The AD746A and AD746B are rated over the industrial temperature range of −40°C to +85°C. The AD746S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

CONNECTION DIAGRAM

Plastic Mini-DIP (N)
Cerdip (Q) and
Plastic SOIC (R) Packages



The AD746 is available in three 8-pin packages: plastic mini-DIP, hermetic cerdip and surface mount (SOIC).

PRODUCT HIGHLIGHTS

1. The AD746 offers exceptional dynamic response for high speed data acquisition systems. It settles to 0.01% in 500 ns and has a 100% tested minimum slew rate of 50 V/μs (AD746B).
2. Outstanding dc precision is provided by a combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs. Input offset voltage, input bias current and input offset current are specified in the warmed-up condition and are 100% tested.
3. Differential and multichannel systems will benefit from the AD746's very close matching of ac characteristics. Input offset voltage specs are fully tested and guaranteed to a maximum of 0.5 mV (AD746B).
4. The AD746 has very close, guaranteed matching of input bias current between its two amplifiers.
5. Unity gain stable version AD712 also available.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD746—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD746J/A Min	AD746J/A Typ	AD746J/A Max	AD746B Min	AD746B Typ	AD746B Max	AD746S Min	AD746S Typ	AD746S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.3	1.5		0.25	0.5		0.3	1.0	mV
Offset	T_{min} to T_{max}			2.0			0.7			1.5	mV
vs. Temperature			12	20		5	10		12	20	μV/°C
vs. Supply[2] (PSRR)		80	95		84	100		80	95		dB
vs. Supply (PSRR)	T_{min} to T_{max}	80			84			80			dB
Long Term Stability			15			15			15		μV/month
INPUT BIAS CURRENT[3]											
Either Input	V_{CM} = 0 V		110	250		110	150		110	250	pA
Either Input @ T_{max}	V_{CM} = 0 V		2.5/7	5.7/16		7	9.6		113	256	nA
Either Input	V_{CM} = +10 V		145	350		145	200		145	350	pA
Offset Current	V_{CM} = 0 V		45	125		45	75		45	125	pA
Offset Current @ T_{max}	V_{CM} = 0 V		1.0/3	2.8/8		3	4.8		45	128	nA
MATCHING CHARACTERISTICS											
Input Offset Voltage			0.6	1.5		0.3	0.5		0.6	1.0	mV
Input Offset Voltage	T_{min} to T_{max}			2.0			0.7			1.5	mV
Input Offset Voltage Drift				20			20			20	μV/°C
Input Bias Current				125			75			125	pA
Crosstalk	@ 1 kHz		120			120			120		dB
	@ 100 kHz		90			90			90		dB
FREQUENCY RESPONSE											
Gain BW, Small Signal	G = −1	8	13		9	13		8	13		MHz
Slew Rate, Unity Gain	G = −1	45	75		50	75		45	75		V/μs
Full Power Response	V_O = 20 V p-p		600			600			600		kHz
Settling Time to 0.01%[4]	G = 1		0.5	0.75		0.5	0.75		0.5	0.75	μs
Total Harmonic	f = 1 kHz										
Distortion	RI≥2 kΩ										
	V_O = 3 V rms		0.0001			0.0001			0.0001		%
INPUT IMPEDANCE											
Differential			$2.5\times10^{11}\|5.5$			$2.5\times10^{11}\|5.5$			$2.5\times10^{11}\|5.5$		Ω|pF
Common Mode			$2.5\times10^{11}\|5.5$			$2.5\times10^{11}\|5.5$			$2.5\times10^{11}\|5.5$		Ω|pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+14.5, −11.5			+14.5, −11.5			+14.5, −11.5		V
Over Max Operating Range[6]		−11		+13	−11		+13	−11		+13	V
Common-Mode Rejection Ratio	V_{CM}=±10 V	78	88		82	88		78	88		dB
	T_{min} to T_{max}	76	84		80	84		76	84		dB
	V_{CM}=±11 V	72	84		78	84		72	84		dB
	T_{min} to T_{max}	70	80		74	80		70	80		dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		2			2			2		μV p-p
	f = 10 Hz		45			45			45		$nV/\sqrt{Hz}$
	f = 100 Hz		22			22			22		$nV/\sqrt{Hz}$
	f = 1 kHz		18			18			18		$nV/\sqrt{Hz}$
	f = 10 kHz		16			16			16		$nV/\sqrt{Hz}$
INPUT CURRENT NOISE	f = 1 kHz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥2 kΩ	150	300		175	300		150	300		V/mV
	T_{min} to T_{max}	75	200		75	200		65	175		V/mV
OUTPUT CHARACTERSTICS											
Voltage	R_{LOAD}≥2 kΩ	+13,−12.5	+13.9, −13.3		+13, −12.5	+13.9, −13.3		+13,−12.5	+13.9, −13.3		V
	T_{min} to T_{max}	±12	+13.8, −13.1		±12	+13.8, −13.1		±12	+13.8, −13.1		V
Current	Short Circuit		25			25			25		mA
Max Capacitive Load	Gain = −1		50			50			50		pF
Driving Capability	Gain= −10		500			500			500		pF
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current			7	10		7	8.0		7	10	mA
TEMPERATURE RANGE											
Rated Performance			0 to +70/−40 to +85			−40 to +85			−55 to +125		°C
PACKAGE OPTIONS[7]											
8-Pin Plastic Mini-DIP (N-8)			AD746JN								
8-Pin Cerdip (Q-8)			AD746AQ			AD746BQ			AD746SQ		
8-Pin Surface Mount (R-8)			AD746JR								
Tape and Reel			AD746JR-REEL								
Chips									AD746SCHIPS		
TRANSISTOR COUNT			54			54			54		

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]PSRR test conditions: $+V_S$ = 15 V, $-V_S$ = −12 V to −18 V and $+V_S$ = 12 V to 18 V, $-V_S$ = −15 V.
[3]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[4]Gain = −1, Rl = 2 k, Cl = 10 pF .
[5]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.
[6]Typically exceeding −14.1 V negative common-mode voltage on either input results in an output phase reversal.
[7]For outline information see Package Information section.

Specifications subject to change without notice.
Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

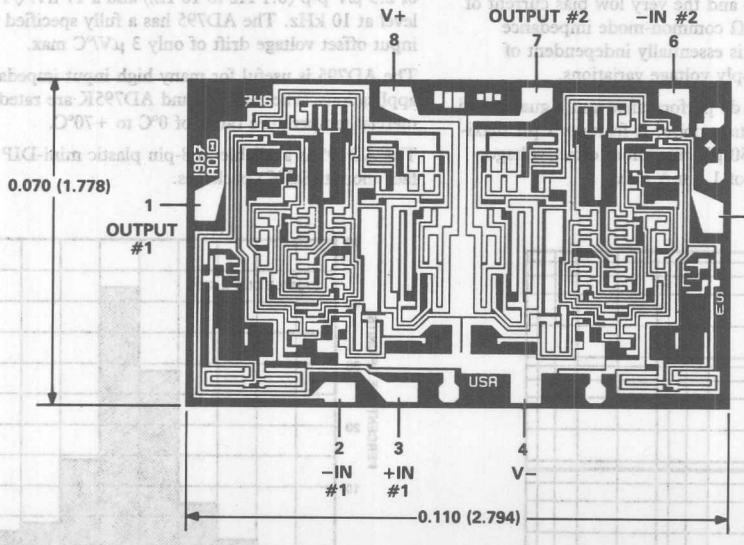
Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 500 mW
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration
(For One Amplifier) . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD746J . . . . . 0 to +70°C
AD746A/B . . . . . −40°C to +85°C
AD746S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering 60 seconds) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 100°C/Watt, θ_{JC} = 50°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/Watt
8-Pin Small Outline Package: θ_{JA} = 160°C/Watt, θ_{JC} = 42°C/Watt

9

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



FEATURES

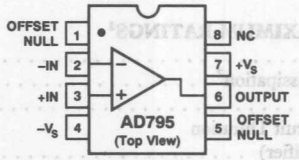
- Low Power Replacement for Burr-Brown OPA-111, OPA-121 Op Amps
- Low Noise
  - 2.5 μV p-p max, 0.1 Hz to 10 Hz
  - 11 nV/√Hz max at 10 kHz
  - 0.6 fA/√Hz at 1 kHz
- High DC Accuracy
  - 250 μV max Offset Voltage
  - 3 μV/°C max Drift
  - 1 pA max Input Bias Current
  - Low Power: 1.5 mA Max Supply Current
- Available in Low Cost Plastic Mini-DIP and Surface Mount (SOIC) Packages

APPLICATIONS

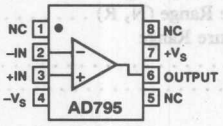
- Low Noise Photodiode Preamps
- CT Scanners
- Precision I-to-V Converters

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) Packages



8-Pin SOIC (R) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

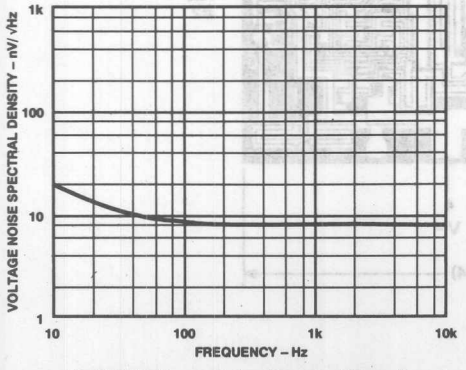
The AD795 is a low noise, precision, FET input operational amplifier. It offers both the low voltage noise and low offset drift of a bipolar input op amp and the very low bias current of a FET-input device. The 10^{14} Ω common-mode impedance insures that input bias current is essentially independent of common-mode voltage and supply voltage variations.

The AD795 has both excellent dc performance and a guaranteed and tested maximum input voltage noise. It features 1 pA maximum input bias current and 250 μV maximum offset voltage, along with low supply current of 1.5 mA max.

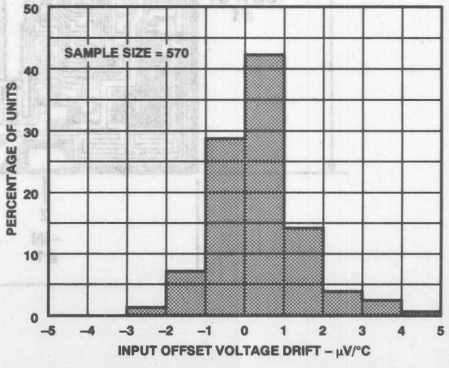
Furthermore, the AD795 features a guaranteed low input noise of 2.5 μV p-p (0.1 Hz to 10 Hz) and a 11 nV/√Hz max noise level at 10 kHz. The AD795 has a fully specified and tested input offset voltage drift of only 3 μV/°C max.

The AD795 is useful for many high input impedance, low noise applications. The AD795J and AD795K are rated over the commercial temperature range of 0°C to +70°C.

The AD795 is available in 8-pin plastic mini-DIP and 8-pin surface mount (SOIC) packages.



AD795 Voltage Noise Spectral Density



Typical Distribution of Average Input Offset Voltage Drift

Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]								
Initial Offset			100	500		50	250	μV
Offset	T_{MIN}–T_{MAX}		300	1000		100	400	μV
vs. Temperature			3	10		1	3	μV/°C
vs. Supply (PSRR)		86	110		90	110		dB
vs. Supply (PSRR)	T_{MIN}–T_{MAX}	84	100		87	100		dB
INPUT BIAS CURRENT[2]								
Either Input	V_{CM} = 0 V		1	2/3		1	1	pA
Either Input @ T_{MAX} =	V_{CM} = 0 V		23			23		pA
Either Input	V_{CM} = +10 V		1			1		pA
Offset Current	V_{CM} = 0 V		0.1	1.0		0.1	0.5	pA
Offset Current @ T_{MAX} =	V_{CM} = 0 V		2			2		pA
OPEN-LOOP GAIN	V_O = ±10 V							
	R_{LOAD} ≥ 10 kΩ	110	120		110	120		dB
	R_{LOAD} ≥ 10 kΩ	100	108		100	108		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		1.0	3.3		1.0	2.5	μV p-p
	f = 10 Hz		20	50		20	40	nV/√Hz
	f = 100 Hz		12	40		12	30	nV/√Hz
	f = 1 kHz		11	17		11	15	nV/√Hz
	f = 10 kHz		9	11		9	11	nV/√Hz
INPUT CURRENT NOISE	f = 0.1 Hz to 10 Hz		13			13		fA p-p
	f = 1 kHz		0.6			0.6		fA/√Hz
FREQUENCY RESPONSE								
Unity Gain, Small Signal	G = −1		1.6			1.6		MHz
Full Power Response	V_O = 20 V p-p							
	R_{LOAD} = 2 kΩ		16			16		kHz
Slew Rate, Unity Gain	V_{OUT} = 20 V p-p							
	R_{LOAD} = 2 kΩ		1			1		V/μs
SETTLING TIME[3]								
To 0.1%	10 V Step		10			10		μs
To 0.01%	10 V Step		11			11		μs
Overload Recovery[4]	50% Overdrive		2			2		μs
Total Harmonic	f = 1 kHz							
Distortion	R1 ≥ 10 kΩ							
	V_O = 3 V rms		−108			−108		dB
INPUT IMPEDANCE								
Differential	V_{DIFF} = ±1 V		10^{12}‖2			10^{12}‖2		Ω‖pF
Common Mode			10^{14}‖2.2			10^{14}‖2.2		Ω‖pF
INPUT VOLTAGE RANGE								
Differential[5]			±20			±20		V
Common-Mode Voltage		±10	±11		±10	±11		V
Over Max Operating Temperature		±10			±10			V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	90	110		94	110		dB
	T_{MIN} to T_{MAX}	86	100		90	100		dB
OUTPUT CHARACTERISTICS								
Voltage	R_{LOAD} ≥ 2 kΩ	V_S−4	V_S−2.5		V_S−4	V_S−2.5		V
	T_{MIN}–T_{MAX}	V_S−4			V_S−4			V
Current	V_{OUT} = ±10 V	±5	±10		±5	±10		mA
	Short Circuit		±15			±15		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±4		±18	±4		±18	V
Quiescent Current			1.3	1.5		1.3	1.5	mA

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[3]Gain = −1, R1 = 10 kΩ.
[4]Defined as the time required for the amplifier's output to return to normal operation after removal of a 50% overload from the amplifier input.
[5]Defined as the maximum continuous voltage between the inputs such that neither input exceeds ±10 V from ground.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] (@ T_A = +25°C)
SOIC Package . . . . . 500 mW
8-Pin Mini-DIP Package . . . . . 750 mW
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD795J/K . . . . . 0°C to +70°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Mini-DIP Package: θ_{JA} = 100°C/Watt
8-Pin Small Outline Package: θ_{JA} = 155°C/Watt

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD795 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD795JN	0°C to +70°C	N-8
AD795KN	0°C to +70°C	N-8
AD795JR	0°C to +70°C	R-8

*N = Plastic mini-DIP; R = SOIC package. For outline information see Package Information section.

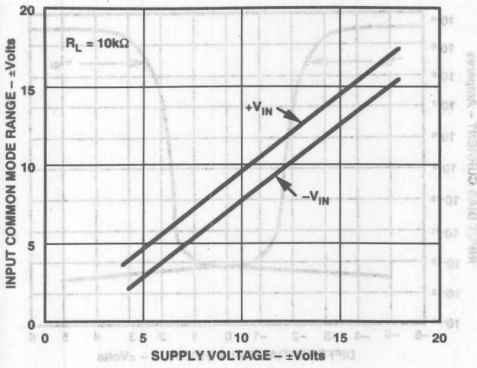


Figure 1. Common-Mode Voltage Range vs. Supply

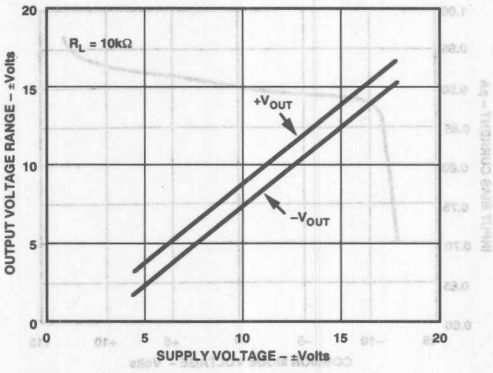


Figure 2. Output Voltage Range vs. Supply Voltage

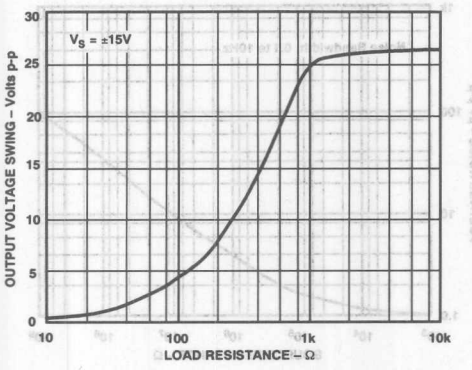


Figure 3. Output Voltage Swing vs. Load Resistance

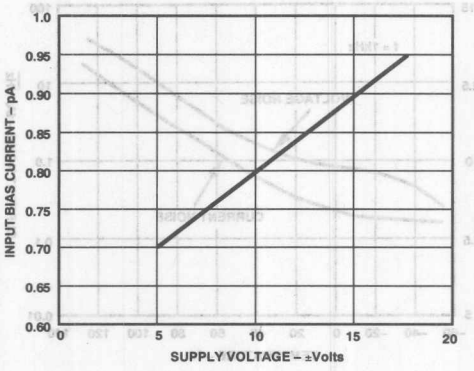


Figure 4. Input Bias Current vs. Supply

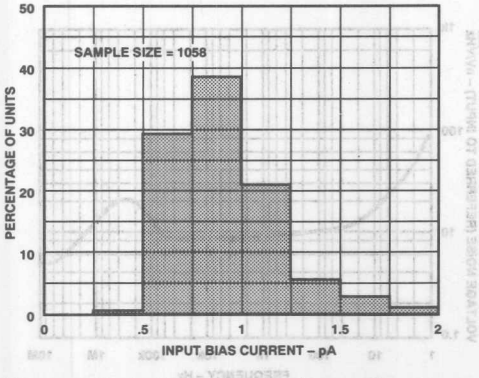


Figure 5. Typical Distribution of Input Bias Current

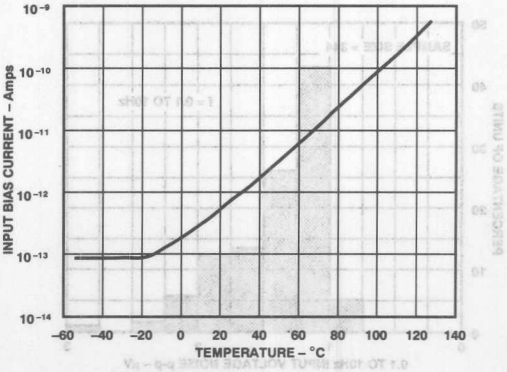


Figure 6. Input Bias Current vs. Temperature

AD795 —Typical Characteristics

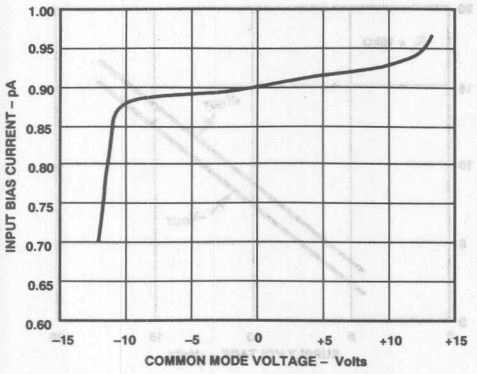


Figure 7. Input Bias Current vs. Common-Mode Voltage

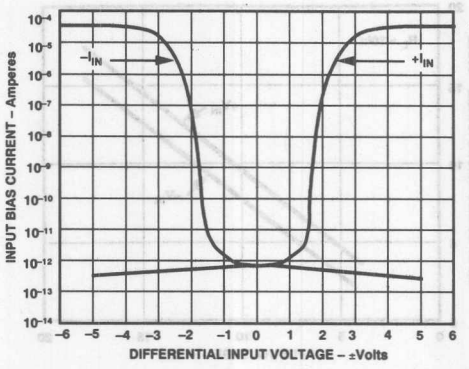


Figure 8. Input Bias Current vs. Differential Input Voltage

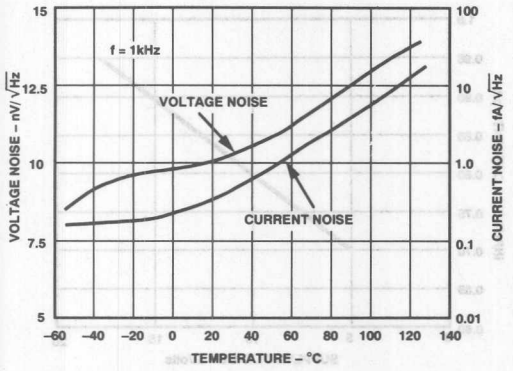


Figure 9. Voltage and Current Noise Spectral Density vs. Temperature

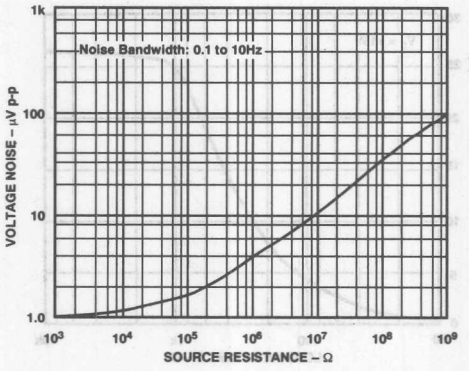


Figure 10. Input Voltage Noise vs. Source Resistance

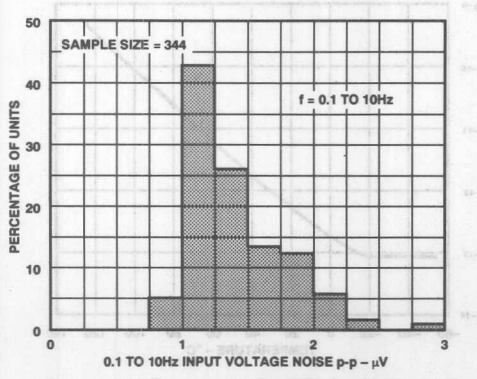


Figure 11. Typical Distribution of Input Voltage Noise

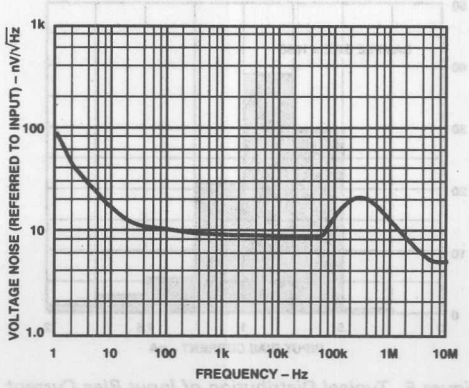


Figure 12. Input Voltage Noise Spectral Density

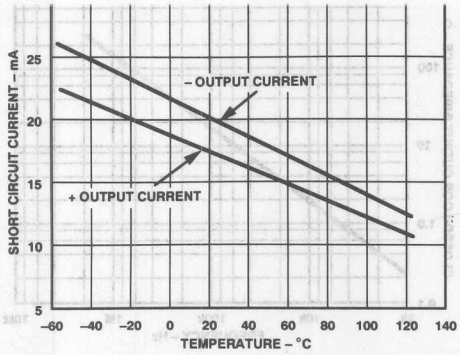


Figure 13. Short Circuit Current Limit vs. Temperature

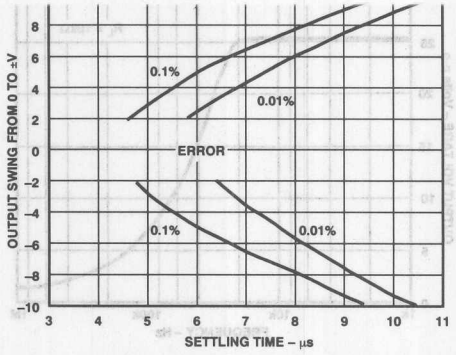


Figure 14. Output Swing and Error vs. Settling Time

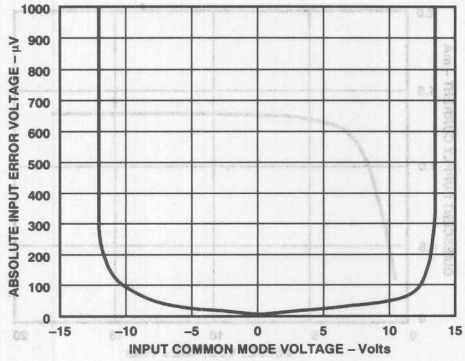


Figure 15. Absolute Input Error Voltage vs. Input Common-Mode Voltage

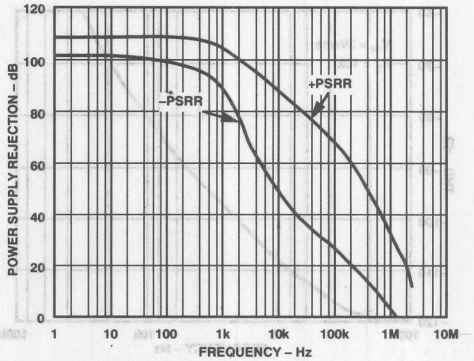


Figure 16. Power Supply Rejection vs. Frequency

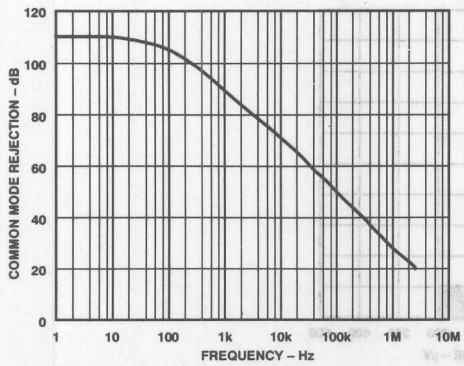


Figure 17. Common-Mode Rejection vs. Frequency

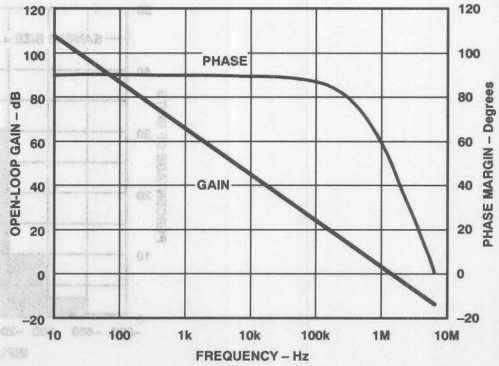


Figure 18. Open-Loop Gain & Phase Margin vs. Frequency

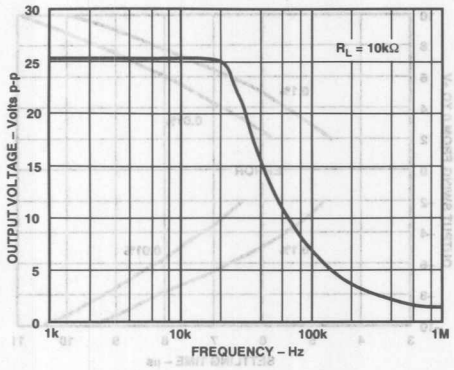


Figure 19. Large Signal Frequency Response

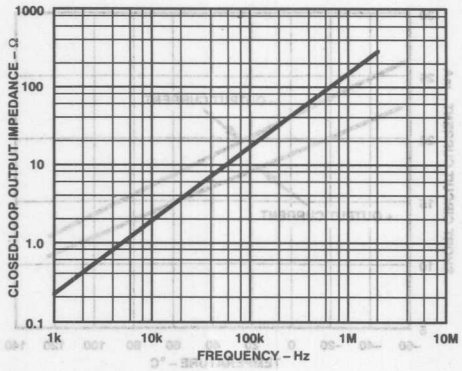


Figure 20. Closed-Loop Output Impedance vs. Frequency

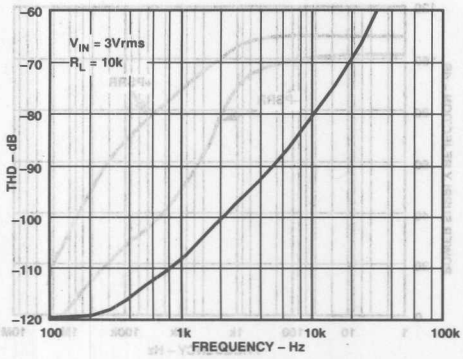


Figure 21. Total Harmonic Distortion vs. Frequency

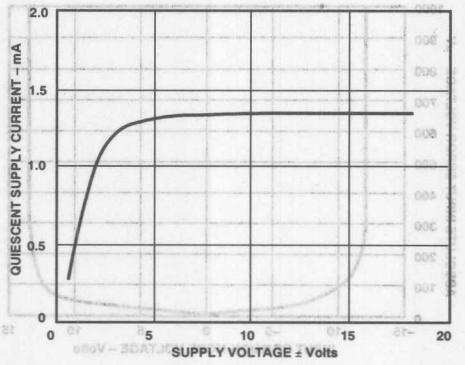


Figure 22. Quiescent Supply Current vs. Supply Voltage Drift

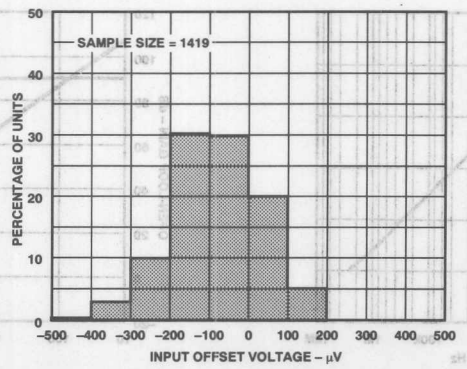


Figure 23. Typical Distribution of Input Offset Voltage

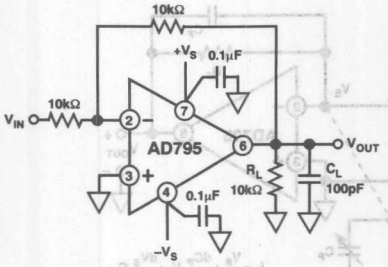


Figure 24. Unity Gain Inverter

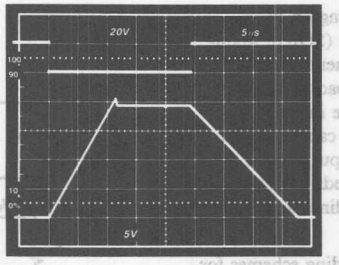


Figure 25. Unity Gain Inverter Large Signal Pulse Response

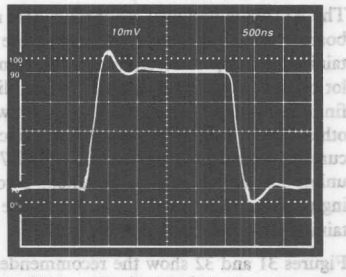


Figure 26. Unity Gain Inverter Small Signal Pulse Response

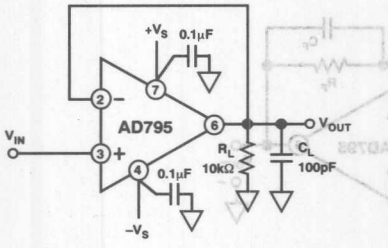


Figure 27. Unity Gain Follower

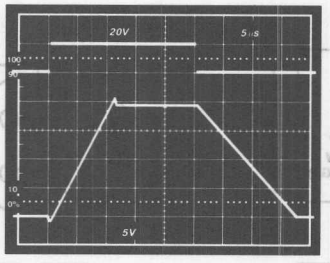


Figure 28. Unity Gain Follower Large Signal Pulse Response

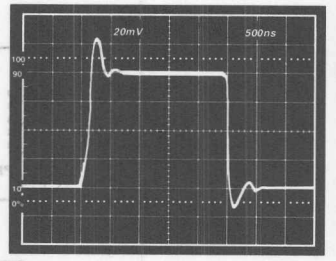


Figure 29. Unity Gain Follower Small Signal Pulse Response

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MINIMIZING INPUT CURRENT

The AD795 is guaranteed to 1 pA max input current with ±15 volt supply voltage at room temperature. Careful attention to how the amplifier is used will maintain or possibly better this performance.

The amplifier's operating temperature should be kept as low as possible. Like other JFET input amplifier's, the AD795's input current will double for every 10°C rise in junction temperature (illustrated in Figure 6). On-chip power dissipation will raise the device operating temperature, causing an increase in input current. Reducing supply voltage to cut power dissipation will reduce the AD795's input current (Figure 4). Heavy output loads can also increase chip temperature, maintaining a minimum load resistance of 10 kΩ in recommended.

CIRCUIT BOARD NOTES

The AD795 is designed for throughhole mounting on PC boards, using either mini-DIP or surface mount (SOIC). Maintaining picoampere resolution in those environments requires a lot of care. Both the board and the amplifier's package have finite resistance. Voltage differences between the input pins and other pins as well as PC board metal traces will cause parasitic currents (Figure 30) larger than the AD795's input current unless special precautions are taken. Two methods of minimizing parasitic leakages are guarding of the input lines and maintaining adequate insulation resistance.

Figures 31 and 32 show the recommended guarding schemes for follower and inverted topologies. Note that for the mini-DIP, the guard trace should be on both sides of the board. On the SOIC, Pin 1 is not connected, and can be safely connected to the guard. The high impedance input trace should be guarded on both edges for its entire length.

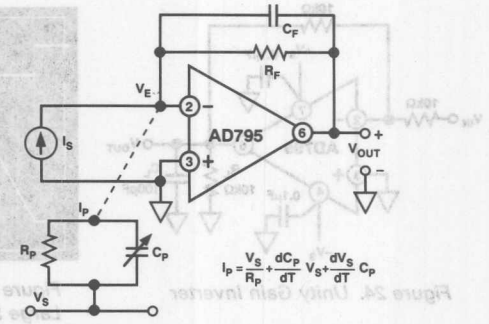

Figure 30. Sources of Parasitic Leakage Currents

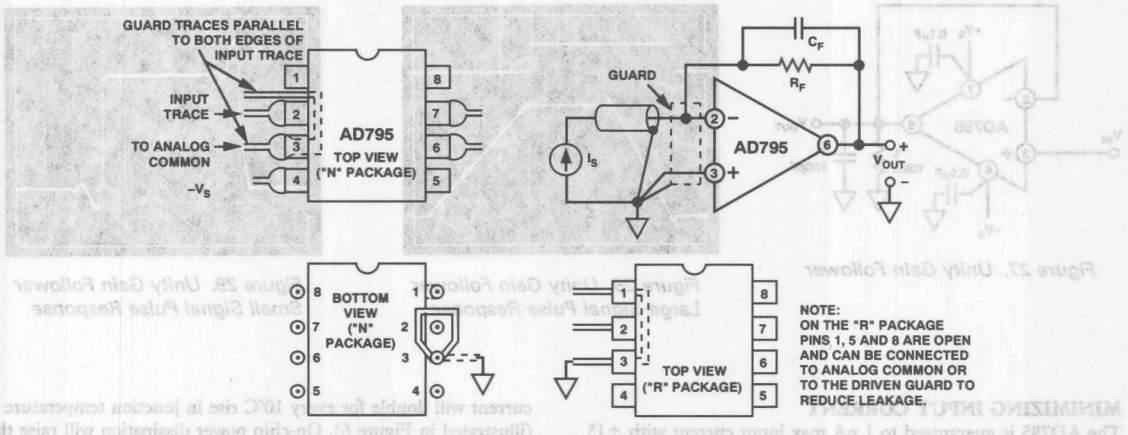

Figure 31. Guarding Scheme–Inverter

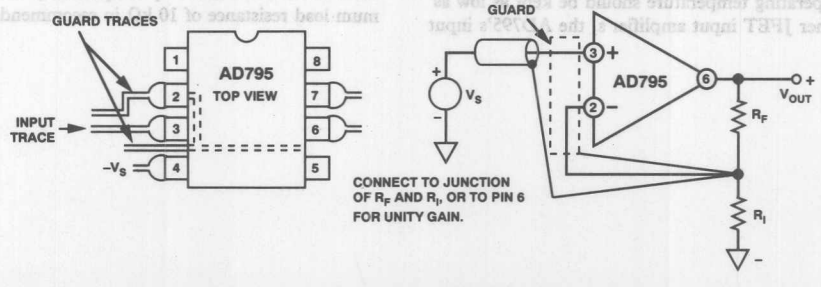

Figure 32. Guard Scheme–Follower

Leakage through the bulk of the circuit board will still occur with the guarding schemes shown in Figures 31 and 32. Standard "G10" type printed circuit board material may not have high enough volume resistivity to hold leakages at the sub-picoampere level particularly under high humidity conditions. One option that eliminates all effects of board resistance is shown in Figure 33. The AD795's sensitive input pin (either Pin 2 when connected as an inverter, or Pin 3 when connected as a follower) is bent up and soldered directly to a Teflon* insulated standoff. Both the signal input and feedback component leads must also be insulated from the circuit board by Teflon standoffs or low-leakage shielded cable.

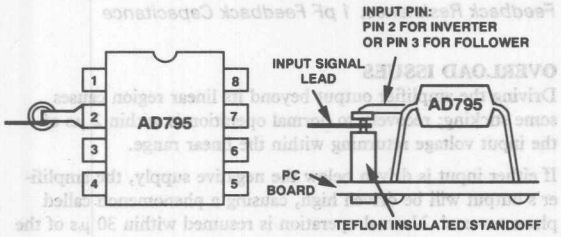

Figure 33. Input Pin to Insulating Standoff

Contaminants such as solder flux on the board's surface and on the amplifier's package can greatly reduce the insulation resistance between the input pin and those traces with supply or signal voltages. Both the package and the board must be kept clean and dry. An effective cleaning procedure is to first swab the surface with high grade isopropyl alcohol, then rinse it with deionized water and, finally, bake it at 100°C for 1 hour. Polypropylene and polystyrene capacitors should not be subjected to the 100°C bake as they will be damaged at temperatures greater than 80°C.

Other guidelines include making the circuit layout as compact as possible and reducing the length of input lines. Keeping circuit board components rigid and minimizing vibration will reduce triboelectric and piezoelectric effects. All precision high impedance circuitry requires shielding from electrical noise and interference. For example, a ground plane should be used under all high value (i.e., greater than 1 MΩ) feedback resistors. In some cases, a shield placed over the resistors, or even the entire amplifier, may be needed to minimize electrical interference originating from other circuits. Referring to the equation in Figure 30, this coupling can take place in either, or both, of two different forms—coupling via time varying fields:

$$\frac{dV}{dT} C_P$$

or by injection of parasitic currents by changes in capacitance due to mechanical vibration:

$$\frac{dCp}{dt} V$$

*Teflon is a registered trademark of E.I. du Pont Co.

Both proper shielding and rigid mechanical mounting of components help minimize error currents from both of these sources.

OFFSET NULLING

The AD795's input offset voltage can be nulled (mini-DIP package only) by using balance Pins 1 and 5, as shown in Figure 34. Nulling the input offset voltage in this fashion will introduce an added input offset voltage drift component of 2.4 μV/°C per millivolt of nulled offset.

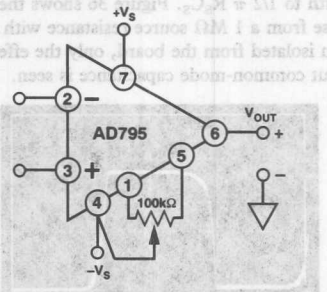

Figure 34. Standard Offset Null Circuit

The circuit in Figure 35 can be used when the amplifier is used as an inverter. This method introduces a small voltage in series with the amplifier's positive input terminal. The amplifier's input offset voltage drift with temperature is not affected. However, variation of the power supply voltages will cause offset shifts.

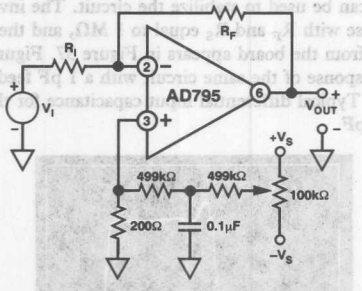

Figure 35. Alternate Offset Null Circuit for Inverter

9

FEEDBACK RESISTANCE

Source and feedback resistances greater than 100 kΩ will magnify the effect of input capacitances (stray and inherent to the AD795) on the ac behavior of the circuit. The effects of common-mode and differential input capacitances should be taken into account since the circuit's bandwidth and stability can be adversely affected.

In a follower, the source resistance, R_S, and input common-mode capacitance, C_S (including capacitance due to board and capacitance inherent to the AD795), form a pole that limits circuit bandwidth to $1/2\ \pi\ R_S C_S$. Figure 36 shows the follower pulse response from a 1 MΩ source resistance with the amplifier's input pin isolated from the board, only the effect of the AD795's input common-mode capacitance is seen.

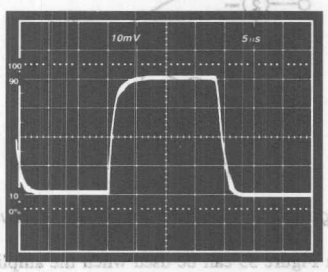

Figure 36. Follower Pulse Response from 1 MΩ Source Resistance

In an inverting configuration, the differential input capacitance forms a pole in the circuit's loop transmission. This can create peaking in the ac response and possible instability. A feedback capacitance can be used to stabilize the circuit. The inverter pulse response with R_F and R_S equal to 1 MΩ, and the input pin isolated from the board appears in Figure 37. Figure 38 shows the response of the same circuit with a 1 pF feedback capacitance. Typical differential input capacitance for the AD795 is 2 pF.

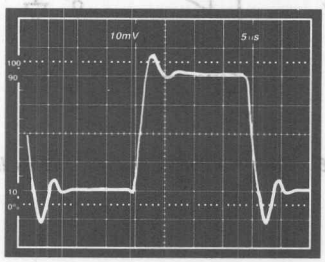

Figure 37. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance

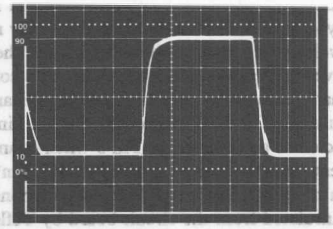

Figure 38. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance, 1 pF Feedback Capacitance

OVERLOAD ISSUES

Driving the amplifier output beyond its linear region causes some sticking; recovery to normal operation is within 2 µs of the input voltage returning within the linear range.

If either input is driven below the negative supply, the amplifier's output will be driven high, causing a phenomenon called phase reversal. Normal operation is resumed within 30 µs of the input voltage returning within the linear range.

Figure 39 shows the AD795's input currents versus differential input voltage. Picoamp level input current is maintained for differential voltages up to several hundred millivolts. This behavior is only important if the AD795 is in an open-loop application where substantial differential voltages are produced.

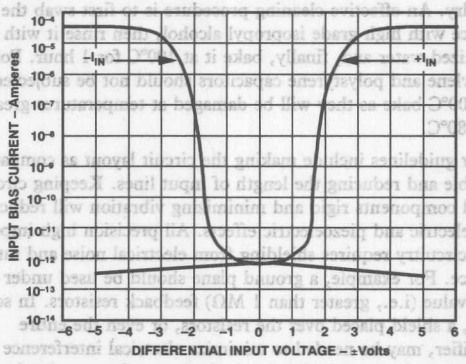

Figure 39. Input Bias Current vs. Differential Input Voltage

INPUT PROTECTION

The AD795 safely handles any input voltage within the supply voltage range. Some applications may subject the input terminals to voltages beyond the supply voltages—in these cases, the following guidelines should be used to maintain the AD795's functionality and performance.

If the inputs are driven more than a 0.5 V below the minus supply, milliamp level currents can be produced through the input terminals. That current should be limited to 10 mA for "transient" overloads (less than 1 second) and 1 mA for continuous overloads, this can be accomplished with a protection resistor in the input terminal (as shown in Figures 40 and 41). The protection resistor's Johnson noise will add to the amplifier's input voltage noise and impact the frequency response.

Driving the input terminals above the positive supply will cause the input current to increase and limit at 40 μA. This condition is maintained until 15 volts above the positive supply—any input voltage within this range does not harm the amplifier. Input voltage above this range causes destructive breakdown and should be avoided.

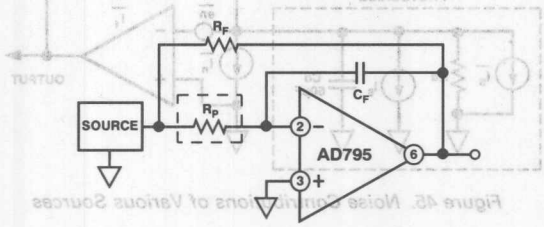

Figure 40. Inverter with Input Current Limit

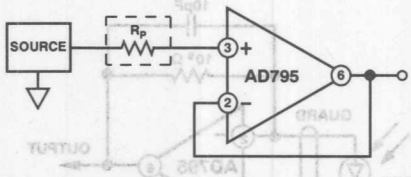

Figure 41. Follower with Input Current Limit

Figure 42 is a schematic of the AD795 as an inverter with an input voltage clamp. Bootstrapping the clamp diodes at the inverting input minimizes the voltage across the clamps and keeps the leakage due to the diodes low. Low leakage diodes (less than 1 pA), such as the FD333's should be used, and should be shielded from light to keep photocurrents from being generated. Even with these precautions, the diodes will measurably increase the input current and capacitance.

In order to achieve the low input bias currents of the AD795, it is not possible to use the same on-chip protection as used in other Analog Devices op amps. This makes the AD795 sensitive to handling and precautions should be taken to minimize ESD exposure whenever possible.

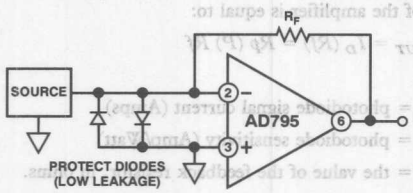

Figure 42. Input Voltage Clamp with Diodes

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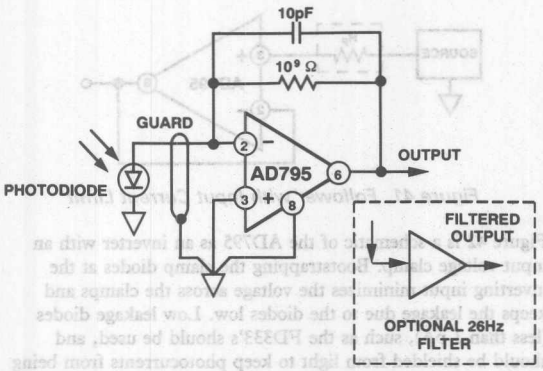


Figure 43. The AD795 Used as a Photodiode Preamplifier

Preamplifier Applications

The low input current and offset voltage levels of the AD795 together with its low voltage noise make this amplifier an excellent choice for preamplifiers used in sensitive photodiode applications. In a typical preamp circuit, shown in Figure 43, the output of the amplifier is equal to:

$$V_{OUT} = I_D\,(Rf) = Rp\,(P)\,Rf$$

where:

I_D = photodiode signal current (Amps)

Rp = photodiode sensitivity (Amp/Watt)

Rf = the value of the feedback resistor, in ohms.

P = light power incident to photodiode surface, in watts.

An equivalent model for a photodiode and its dc error sources is shown in Figure 44. The amplifier's input current, I_B, will contribute an output voltage error which will be proportional to the value of the feedback resistor. The offset voltage error, V_{OS}, will cause a "dark" current error due to the photodiode's finite shunt resistance, Rd. The resulting output voltage error, V_E, is equal to:

$$V_E = (1 + Rf/Rd)\,V_{OS} + Rf\,I_B$$

A shunt resistance on the order of 10^9 ohms is typical for a small photodiode. Resistance Rd is a junction resistance which will typically drop by a factor of two for every 10°C rise in temperature. In the AD795, both the offset voltage and drift are low, this helps minimize these errors.

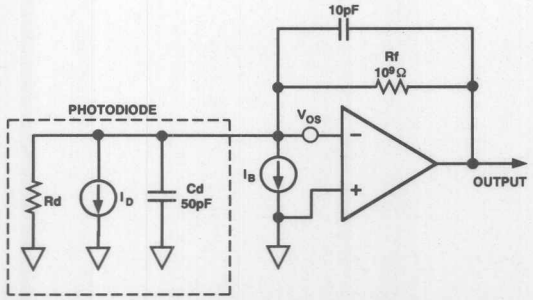


Figure 44. A Photodiode Model Showing DC Error Sources

Minimizing Noise Contributions

The noise level limits the resolution obtainable from any preamplifier. The total output voltage noise divided by the feedback resistance of the op amp defines the minimum detectable signal current. The minimum detectable current divided by the photodiode sensitivity is the minimum detectable light power.

Sources of noise in a typical preamp are shown in Figure 45. The total noise contribution is defined as:

$$\overline{V_{OUT}} = \sqrt{(\overline{i_n^2} + \overline{i_f^2} + \overline{i_s^2})\left(\frac{Rf}{1 + s\,(Cf)\,Rf}\right)^2 + (\overline{en^2})\left(1 + \frac{Rf}{Rd}\left(\frac{1 + s\,(Cd)\,Rd}{1 + s\,(Cf)\,Rf}\right)\right)^2}$$

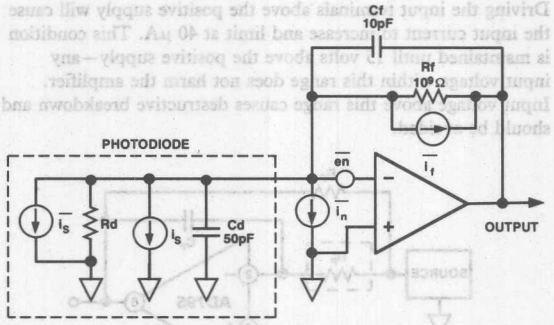


Figure 45. Noise Contributions of Various Sources

Figure 46, a spectral density versus frequency plot of each source's noise contribution, shows that the bandwidth of the amplifier's input voltage noise contribution is much greater than its signal bandwidth. In addition, capacitance at the summing junction results in a "peaking" of noise gain in this configuration. This effect can be substantial when large photodiodes with large shunt capacitances are used. Capacitor Cf sets the signal bandwidth and also limits the peak in the noise gain. Each source's rms or root-sum-square contribution to noise is obtained by integrating the sum of the squares of all the noise sources and then by obtaining the square root of this sum. Minimizing the total area under these curves will optimize the preamplifier's overall noise performance.

An output filter with a passband close to that of the signal can greatly improve the preamplifier's signal to noise ratio. The photodiode preamplifier shown in Figure 45—without a bandpass filter—has a total output noise of 50 μV rms. Using a 26 Hz single pole output filter, the total output noise drops to 23 μV rms, a factor of 2 improvement with no loss in signal bandwidth.

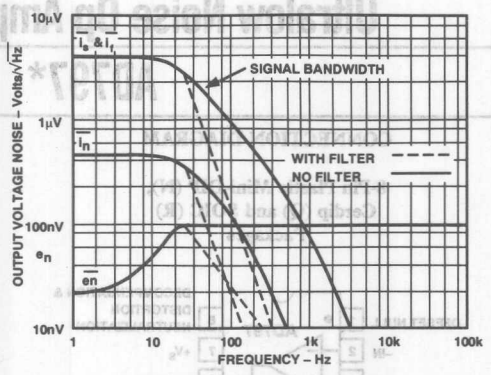


Figure 46. Voltage Noise Spectral Density of the Circuit of Figure 45 with and without an Output Filter

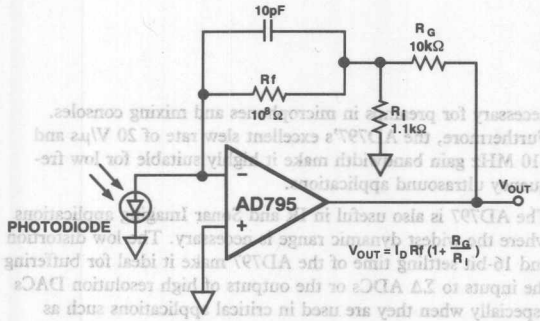


Figure 47. A Photodiode Preamp Employing a "T" Network for Added Gain

Using a "T" Network

A "T" network, shown in Figure 47, can be used to boost the effective transimpedance of an I to V converter, for a given feedback resistor value. However, amplifier noise and offset voltage contributions are also amplified by the "T" network gain. A low noise, low offset voltage amplifier, such as the AD795, is needed for this type of application.

A pH Probe Buffer Amplifier

A typical pH probe requires a buffer amplifier to isolate its 10^6 to 10^9 Ω source resistance from external circuitry. Just such an amplifier is shown in Figure 48. The low input current of the AD795 allows the voltage error produced by the bias current and electrode resistance to be minimal. The use of guarding, shielding, high insulation resistance standoffs, and other such standard methods used to minimize leakage are all needed to maintain the accuracy of this circuit.

The slope of the pH probe transfer function, 50 mV per pH unit at room temperature, has a +3300 ppm/°C temperature coefficient. The buffer of Figure 48 provides an output voltage equal to 1 volt/pH unit. Temperature compensation is provided by resistor RT which is a special temperature compensation resistor, part number Q81, 1 kΩ, 1%, +3500 ppm/°C, available from Tel Labs Inc.

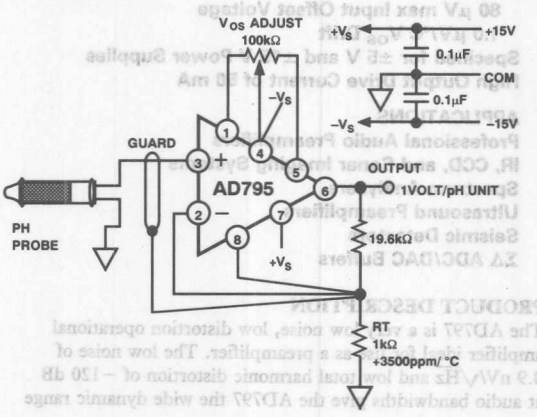


Figure 48. A pH Probe Amplifier

FEATURES

Low Noise
- 0.9 nV/√Hz typ (1.2 nV/√Hz max) Input Voltage Noise at 1 kHz
- 50 nV p–p Input Voltage Noise, 0.1 to 10 Hz

Low Distortion
- −120 dB Total Harmonic Distortion at 20 kHz

Excellent AC Characteristics
- 800 ns Settling Time to 16 Bits (10 V Step)
- 110 MHz Gain Bandwidth (G = 1000)
- 8 MHz Bandwidth (G = 10)
- 280 kHz Full Power Bandwidth at 20 V p–p
- 20 V/μs Slew Rate

Excellent DC Precision
- 80 μV max Input Offset Voltage
- 1.0 μV/°C V_{OS} Drift

Specified for ±5 V and ±15 V Power Supplies

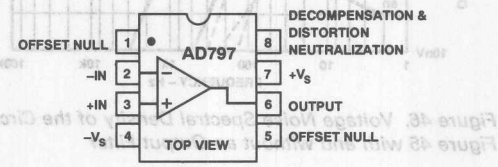
High Output Drive Current of 50 mA

APPLICATIONS

Professional Audio Preamplifiers
IR, CCD, and Sonar Imaging Systems
Spectrum Analyzers
Ultrasound Preamplifiers
Seismic Detectors
ΣΔ ADC/DAC Buffers

CONNECTION DIAGRAM

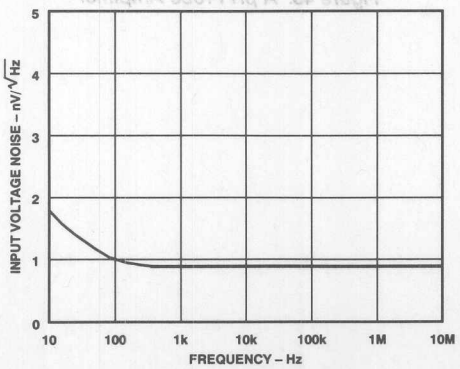
8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



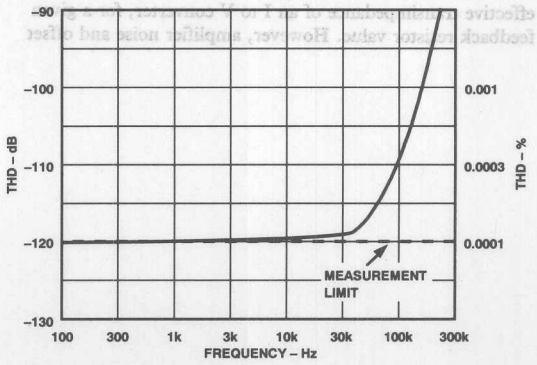
PRODUCT DESCRIPTION

The AD797 is a very low noise, low distortion operational amplifier ideal for use as a preamplifier. The low noise of 0.9 nV/√Hz and low total harmonic distortion of −120 dB at audio bandwidths give the AD797 the wide dynamic range necessary for preamps in microphones and mixing consoles. Furthermore, the AD797's excellent slew rate of 20 V/μs and 110 MHz gain bandwidth make it highly suitable for low frequency ultrasound applications.

The AD797 is also useful in IR and Sonar Imaging applications where the widest dynamic range is necessary. The low distortion and 16-bit settling time of the AD797 make it ideal for buffering the inputs to ΣΔ ADCs or the outputs of high resolution DACs especially when they are used in critical applications such as seismic detection and spectrum analyzers. Key features such as a 50 mA output current drive and the specified power supply voltage range of ±5 to ±15 volts make the AD797 an excellent general purpose amplifier.



AD797 Voltage Noise Spectral Density



THD vs. Frequency

*Patent pending.

INPUT OFFSET VOLTAGE		±5 V, ±15 V		25	80		10	40	μV
	T_{MIN} to T_{MAX}			50	125/180		30	60	μV
Offset Voltage Drift		±5 V, ±15 V		0.2	1.0		0.2	0.6	μV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		0.25	1.5		0.25	0.9	μA
	T_{MIN} to T_{MAX}			0.5	3.0		0.25	2.0	μA
INPUT OFFSET CURRENT		±5 V, ±15 V		100	400		80	200	nA
	T_{MIN} to T_{MAX}			120	600/700		120	300	nA
OPEN-LOOP GAIN	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 2 kΩ		1	20		2	20		V/μV
	T_{MIN}–T_{MAX}		1	6		2	10		V/μV
	R_{LOAD} = 600 Ω		1	15		2	15		V/μV
	T_{MIN} to T_{MAX}		1	5		2	7		V/μV
	@ 20 kHz[2]		14000	20000		14000	20000		V/V
DYNAMIC PERFORMANCE									
Gain Bandwidth Product	G = 1000	±15 V		110			110		MHz
	G = 1000[2]	±15 V		450			450		MHz
−3 dB Bandwidth	G = 10	±15 V		8			8		MHz
Full Power Bandwidth[3]	V_O = 20 V p–p,								
	R_{LOAD} = 1 kΩ	±15 V		280			280		kHz
Slew Rate	R_{LOAD} = 1 kΩ	±15 V	12.5	20		12.5	20		V/μs
Settling Time to 0.0015%	10 V Step	±15 V		800	1200		800	1200	ns
COMMON-MODE REJECTION	V_{CM} = CMVR	±5 V, ±15 V	114	130		120	130		dB
	T_{MIN} to T_{MAX}		110	120		114	120		dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±18 V		114	130		120	130		dB
	T_{MIN} to T_{MAX}		110	120		114	120		dB
INPUT VOLTAGE NOISE	f = 0.1 Hz to 10 Hz	±15 V		50			50		nV p–p
	f = 10 Hz	±15 V		1.7			1.7	2.5	nV/√Hz
	f = 1 kHz	±15 V		0.9	1.2		0.9	1.2	nV/√Hz
	f = 10 Hz–1 MHz	±15 V		1.0	1.3		1.0	1.2	μV rms
INPUT CURRENT NOISE	f = 1 kHz	±15 V		2.0			2.0		pA/√Hz
INPUT COMMON-MODE		±15 V	±11	±12		±11	±12		V
VOLTAGE RANGE		±5 V	±2.5	±3		±2.5	±3		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 2 kΩ	±15 V	±12	±13		±12	±13		V
	R_{LOAD} = 600 Ω	±15 V	±11	±13		±11	±13		V
	R_{LOAD} = 600 Ω	±5 V	±2.5	±3		±2.5	±3		V
Short-Circuit Current		±5 V, ±15 V		80			80		mA
Output Current[4]		±5 V, ±15 V	30	50		30	50		mA
TOTAL HARMONIC DISTORTION	R_{LOAD} = 1 kΩ, C_N = 50 pF	±15 V		−98	−90		−98	−90	dB
	f = 250 kHz, 3 V rms								
	R_{LOAD} = 1 kΩ	±15 V		−120	−110		−120	−110	dB
	f = 20 kHz, 3 V rms								
INPUT CHARACTERISTICS									
Input Resistance (Differential)				7.5			7.5		kΩ
Input Resistance (Common Mode)				100			100		MΩ
Input Capacitance (Differential)[5]				20			20		pF
Input Capacitance (Common Mode)				5			5		pF
OUTPUT RESISTANCE	A_V = +1, f = 1 kHz			3			3		mΩ
POWER SUPPLY									
Operating Range			±5		±18	±5		±18	V
Quiescent Current		±5 V, ±15 V		8.2	10.5		8.2	10.5	mA

NOTES
[1]See standard military drawing for 883B specifications.
[2]Specified using external decompensation capacitor, see applications section.
[3]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.
[4]Output Current for $|V_S - V_{OUT}| > 4$ V, $A_{OL} > 200$ kΩ.
[5]Differential input capacitance consists of 1.5 pF package capacitance and 18.5 pF from the input differential pair.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation @ +25°C[2]
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage[3] . . . . . ±0.7 V
Output Short Circuit Duration . . . . . Indefinite Within max Internal Power Dissipation
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD797A/B . . . . . −40°C to +85°C
AD797S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Internal Power Dissipation:
8-Pin SOIC = 0.9 Watts − $(T_A - 25°C)/\theta_{JA}$
8-Pin Plastic DIP and Cerdip = 1.3 Watts − $(T_A - 25°C)/\theta_{JA}$
Thermal Characteristics
8-Pin Plastic DIP Package: θ_{JA} = 95°C/W
8-Pin Cerdip Package: θ_{JA} = 110°C/W
8-Pin Small Outline Package: θ_{JA} = 155°C/W

[3]The AD797's inputs are protected by back-to-back diodes. To achieve low noise, internal current limiting resistors are not incorporated into the design of this amplifier. If the differential input voltage exceeds ±0.7 V, the input current should be limited to less than 25 mA by series protection resistors. Note, however, that this will degrade the low noise performance of the device.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD797 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

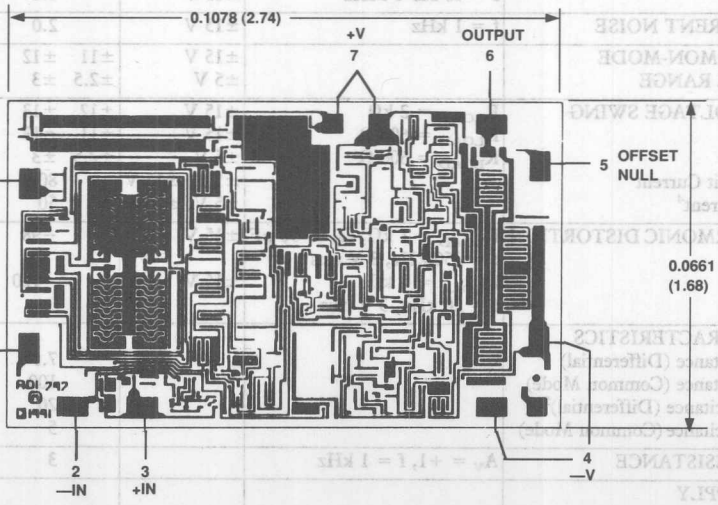
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD797AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD797BN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD797BR	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD797AR	−40°C to +85°C	8-Pin Plastic SOIC	R-8
5962-9313301MPA	−55°C to +125°C	8-Pin Cerdip	Q-8
AD797A Chips	−40°C to +85°C	Die	

*For outline information see Package Information section.

METALIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm)



NOTE
The AD797 has double layer metal. Only one layer is shown here for clarity.

Typical Characteristics

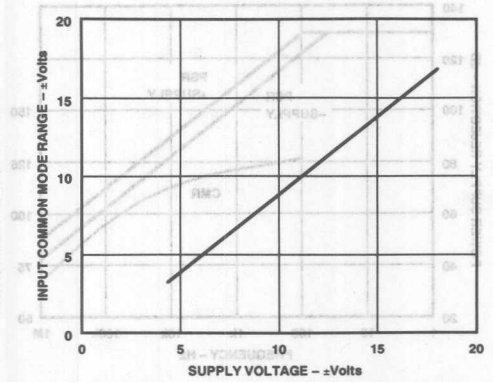


Figure 1. Common-Mode Voltage Range vs. Supply

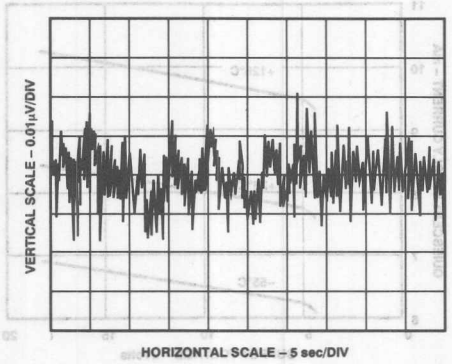


Figure 4. 0.1 Hz to 10 Hz Noise

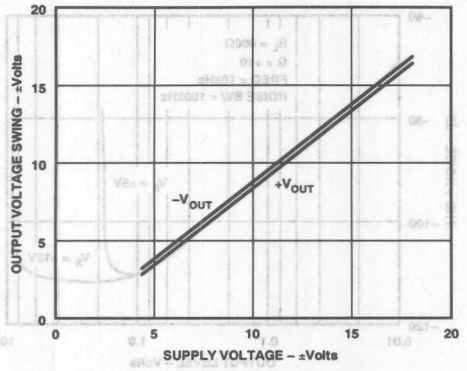


Figure 2. Output Voltage Swing vs. Supply

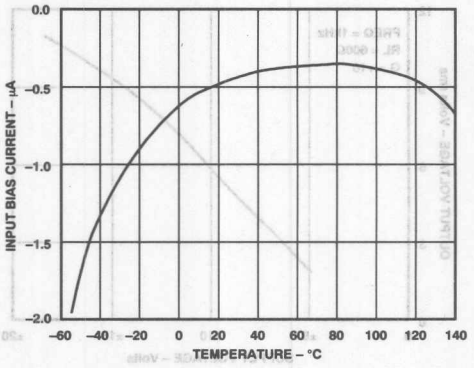


Figure 5. Input Bias Current vs. Temperature

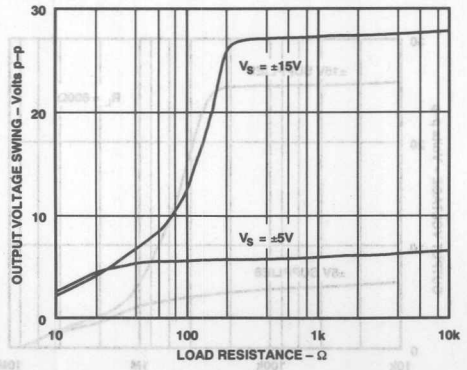


Figure 3. Output Voltage Swing vs. Load Resistance

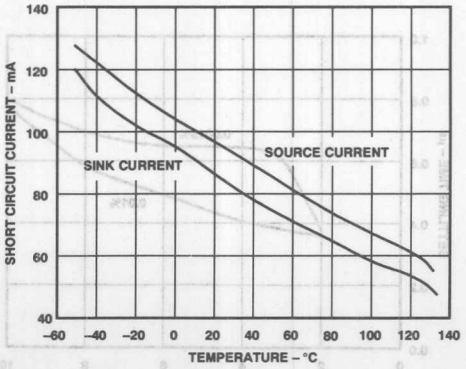


Figure 6. Short Circuit Current vs. Temperature

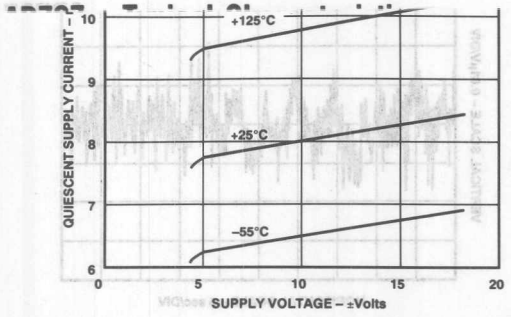


Figure 7. Quiescent Supply Current vs. Supply Voltage

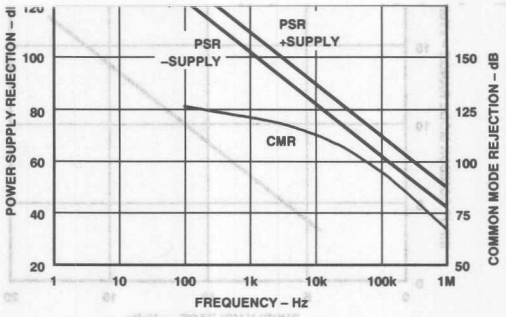


Figure 10. Power Supply and Common-Mode Rejection vs. Frequency

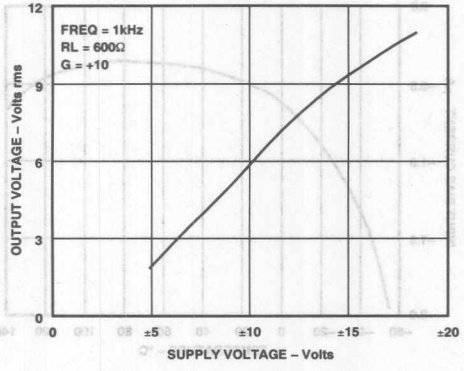


Figure 8. Output Voltage vs. Supply for 0.01% Distortion

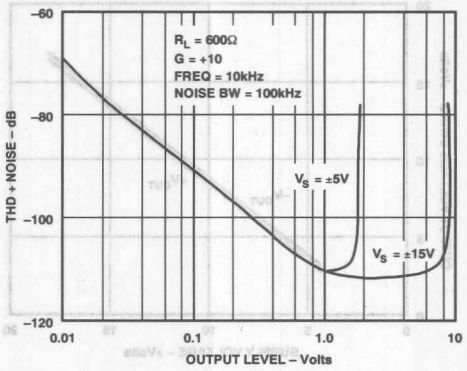


Figure 11. Total Harmonic Distortion (THD) + Noise vs. Output Level

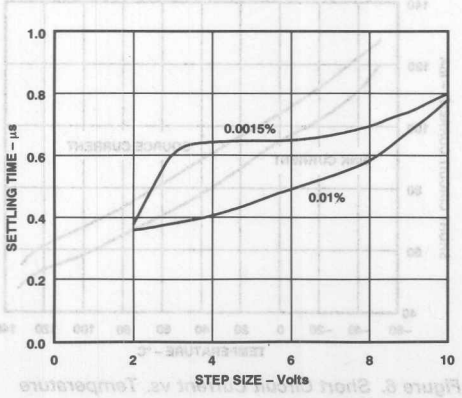


Figure 9. Settling Time vs. Step Size (±)

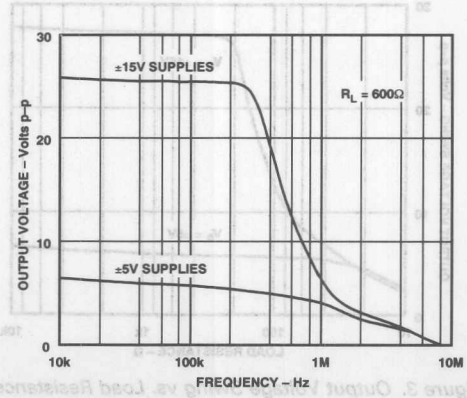


Figure 12. Large Signal Frequency Response

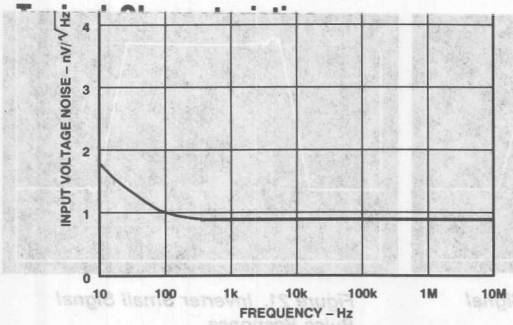


Figure 13. Input Voltage Noise Spectral Density

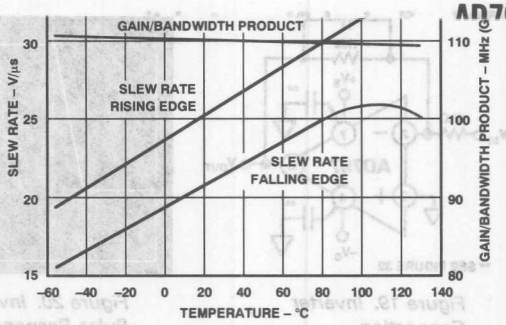


Figure 16. Slew Rate & Gain/Bandwidth Product vs. Temperature

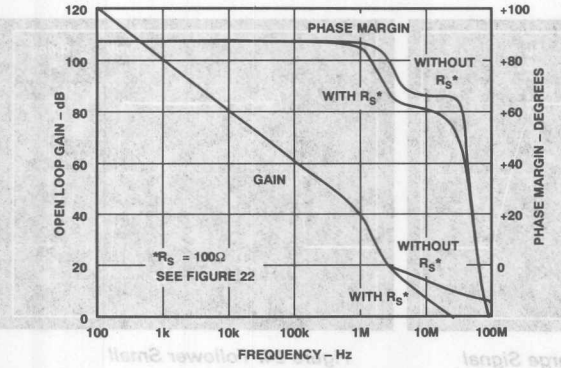


Figure 14. Open-Loop Gain & Phase vs. Frequency

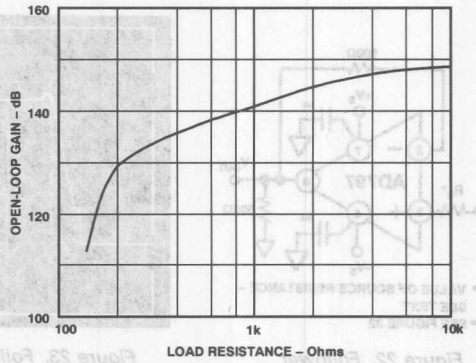


Figure 17. Open-Loop Gain vs. Resistive Load

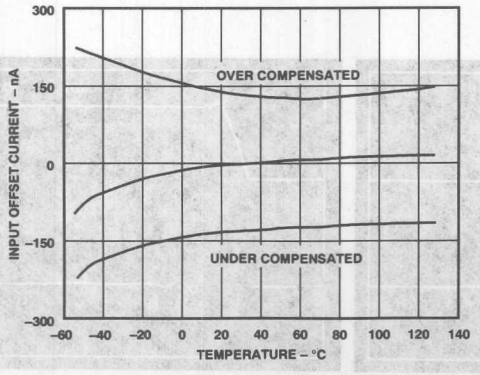


Figure 15. Input Offset Current vs. Temperature

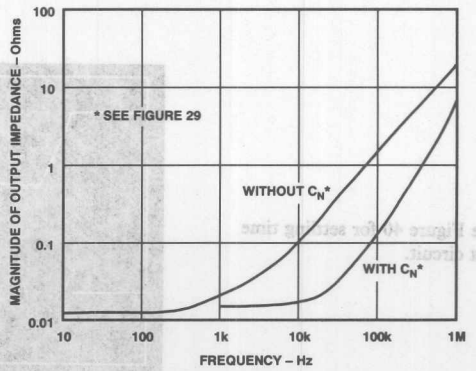


Figure 18. Magnitude of Output Impedance vs. Frequency

AD797—Typical Characteristics

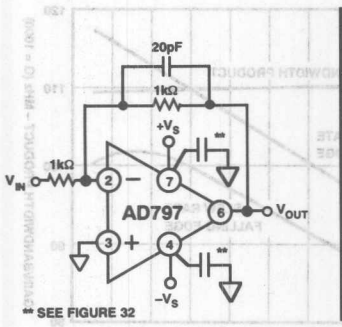


Figure 19. Inverter Connection

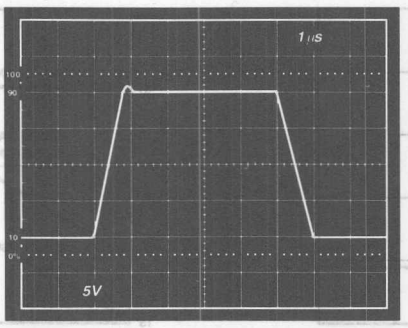


Figure 20. Inverter Large Signal Pulse Response

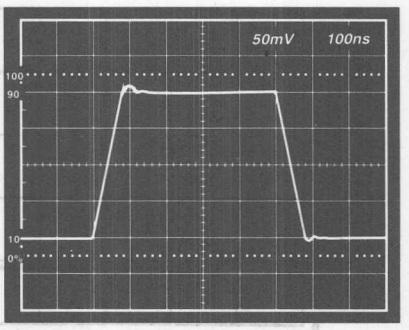


Figure 21. Inverter Small Signal Pulse Response

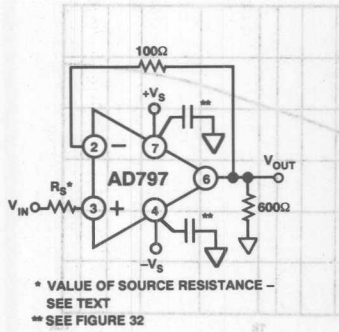


Figure 22. Follower Connection

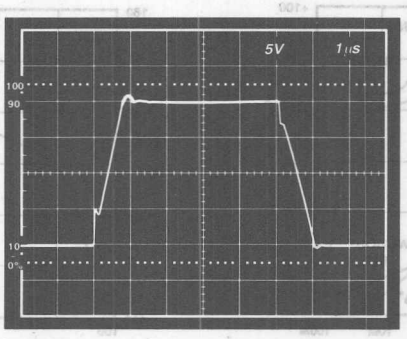


Figure 23. Follower Large Signal Pulse Response

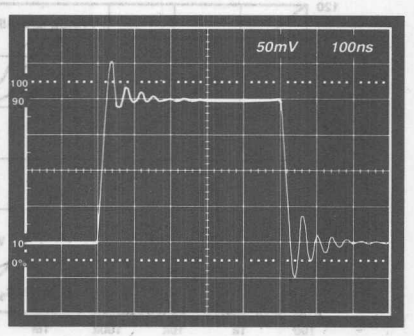


Figure 24. Follower Small Signal Pulse Response

See Figure 40 for settling time test circuit.

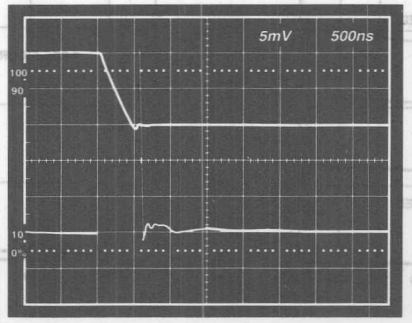


Figure 25. 16-Bit Settling Time Positive Input Pulse

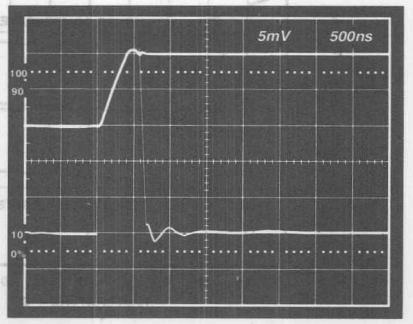


Figure 26. 16-Bit Settling Time Negative Input Pulse

THEORY OF OPERATION

The new architecture of the AD797 was developed to overcome inherent limitations in previous amplifier designs. Previous precision amplifiers used three stages to ensure high open-loop gain, Figure 27b, at the expense of additional frequency compensation components. Slew rate and settling performance are usually compromised, and dynamic performance is not adequate beyond audio frequencies. As can be seen in Figure 27b, the first stage gain is rolled off at high frequencies by the compensation network. Second stage noise and distortion will then appear at the input and degrade performance. The AD797 on the other hand, uses a single ultrahigh gain stage to achieve dc as well as dynamic precision. As shown in the simplified schematic (Figure 28), nodes A, B, and C all track in voltage forcing the operating points of all pairs of devices in the signal path to match. By exploiting the inherent matching of devices fabricated on the same IC chip, high open-loop gain, CMRR, PSRR, and low V_{OS} are all guaranteed by pairwise device *matching* (i.e., NPN to NPN & PNP to PNP), and not absolute parameters such as beta and early voltage.

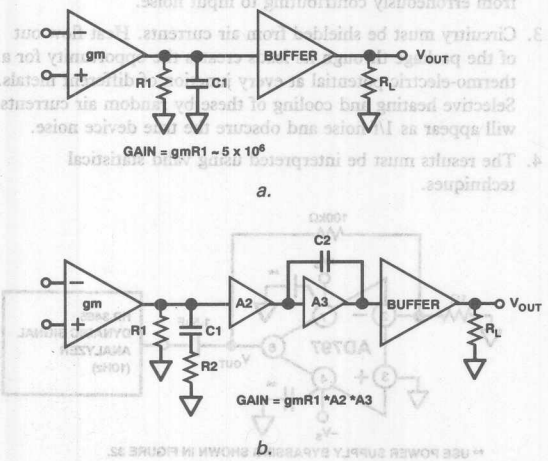


Figure 27. Model of AD797 vs. That of a Typical Three-Stage Amplifier

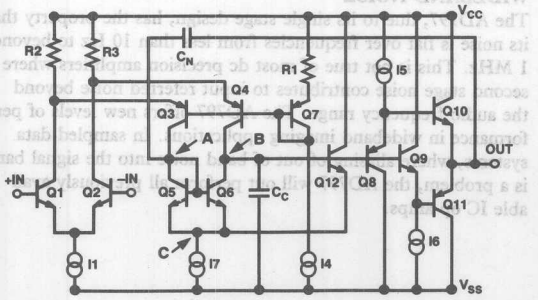


Figure 28. AD797 Simplified Schematic

This matching benefits not just dc precision but since it holds up dynamically, both distortion and settling time are also reduced. This single stage has a voltage gain of $>5 \times 10^6$ and V_{OS} <80 μV, while at the same time providing THD + noise of less than −120 dB and true 16 bit settling in less than 800 ns. The elimination of second stage noise effects has the additional benefit of making the low noise of the AD797 (<0.9 nV/$\sqrt{\text{Hz}}$) extend to beyond 1 MHz. This means new levels of performance for sampled data and imaging systems. All of this performance as well as load drive in excess of 30 mA are made possible by Analog Devices' advanced Complementary Bipolar (CB) process.

Another unique feature of this circuit is that the addition of a single capacitor, C_N (Figure 28), enables cancellation of distortion due to the output stage. This can best be explained by referring to a simplified representation of the AD797 using idealized blocks for the different circuit elements (Figure 29).

A single equation yields the open-loop transfer function of this amplifier, solving it (at Node B) yields:

$$\frac{V_O}{V_{IN}} = \frac{gm}{\frac{C_N}{A} j\omega - C_N j\omega - \frac{C_C}{A} j\omega}$$

gm = the transconductance of Q1 and Q2
A = the gain of the output stage, (~1)
V_O = voltage at the output
V_{IN} = differential input voltage

When C_N is equal to C_C this gives the ideal single pole op amp response:

$$\frac{V_O}{V_{IN}} = \frac{gm}{j\omega C}$$

The terms in A, which include the properties of the output stage such as output impedance and distortion, cancel by simple subtraction, and therefore the distortion cancellation does not affect the stability or frequency response of the amplifier. With only 500 μA of output stage bias the AD797 delivers a 1 kHz sine wave into 600 Ω at 7 V rms with only 1 ppm of distortion.

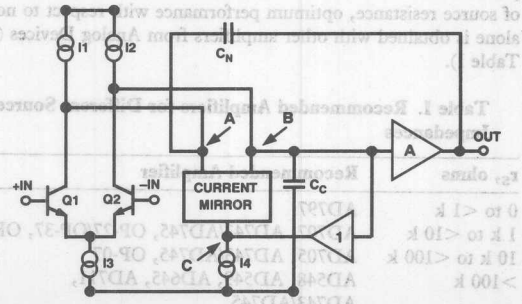


Figure 29. AD797 Block Diagram

current. It is important then to consider the total input referred noise ($e_N total$), which includes contributions from voltage noise (e_N), current noise (i_N), and resistor noise ($\sqrt{4\ kTr_S}$).

$$e_N total = [e_N^2 + 4\ kTr_S + 4\ (i_N r_S)^2]^{1/2} \quad \text{Equation 1}$$

where r_S = total input source resistance.

This equation is plotted for the AD797 in Figure 30. Since optimum dc performance is obtained with matched source resistances, this case is considered even though it is clear from Equation 1 that eliminating the balancing source resistance will lower the total noise by reducing the total r_S by a factor of two.

At very low source resistance (r_S <50 Ω), the amplifiers' voltage noise dominates. As source resistance increases the Johnson noise of r_S dominates until at higher resistances (r_S >2 kΩ) the current noise component is larger than the resistor noise.

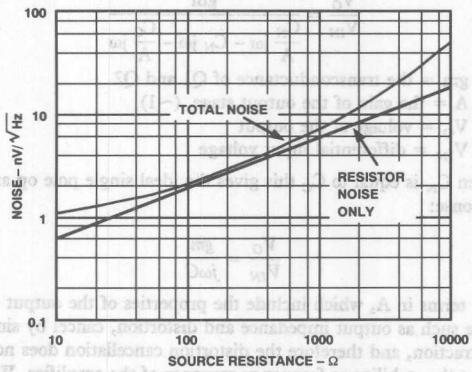


Figure 30. Noise vs. Source Resistance

The AD797 is the optimum choice for low noise performance provided the source resistance is kept <1 kΩ. At higher values of source resistance, optimum performance with respect to noise alone is obtained with other amplifiers from Analog Devices (see Table I).

Table I. Recommended Amplifiers for Different Source Impedances

r_S, ohms	Recommended Amplifier
0 to <1 k	AD797
1 k to <10 k	AD707, AD743/AD745, OP-27/OP-37, OP-07
10 k to <100 k	AD705, AD743/AD745, OP-07
>100 k	AD548, AD549, AD645, AD711, AD743/AD745

techniques can be used to make this measurement. The usual technique involves amplifying, filtering, and measuring the amplifiers noise for a predetermined test time. The noise bandwidth of the filter is corrected for and the test time is carefully controlled since the measurement time acts as an additional low frequency roll-off.

The plot in Figure 4 was made using a slightly different technique. Here an FFT based instrument (Figure 31) is used to generate a 10 Hz "brickwall" filter. A low frequency pole at 0.1 Hz is generated with an external ac coupling capacitor, the instrument being dc coupled.

Several precautions are necessary to get optimum low frequency noise performance:

1. Care must be used to account for the effects of r_S, even a 10 Ω resistor has 0.4 nV$\sqrt{\text{Hz}}$ of noise (an error of 9% when root sum squared with 0.9 nV$\sqrt{\text{Hz}}$).
2. The test set up must be fully warmed up to prevent e_{OS} drift from erroneously contributing to input noise.
3. Circuitry must be shielded from air currents. Heat flow out of the package through its leads creates the opportunity for a thermo-electric potential at every junction of different metals. Selective heating and cooling of these by random air currents will appear as 1/f noise and obscure the true device noise.
4. The results must be interpreted using valid statistical techniques.

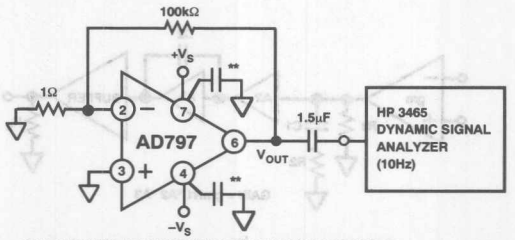


Figure 31. Test Setup for Measuring 0.1 Hz to 10 Hz Noise

WIDEBAND NOISE

The AD797, due to its single stage design, has the property that its noise is flat over frequencies from less than 10 Hz to beyond 1 MHz. This is not true of most dc precision amplifiers where second stage noise contributes to input referred noise beyond the audio frequency range. The AD797 offers new levels of performance in wideband imaging applications. In sampled data systems, where aliasing of out of band noise into the signal band is a problem, the AD797 will out perform all previously available IC op amps.

BYPASSING CONSIDERATIONS

To take full advantage of the very wide bandwidth and dynamic range capabilities of the AD797 requires some precautions. First, multiple bypassing is recommended in any precision application. A 1.0 μF–4.7 μF tantalum in parallel with 0.1 μF ceramic bypass capacitors are sufficient in most applications. When driving heavy loads a larger demand is placed on the supply bypassing. In this case selective use of larger values of tantalum capacitors and damping of their lead inductance with small value (1.1 Ω to 4.7 Ω) carbon resistors can be an improvement. Figure 32 summarizes bypassing recommendations. The symbol (**) is used throughout this data sheet to represent the parallel combination of a 0.1 μF and a 4.7 μF capacitor.

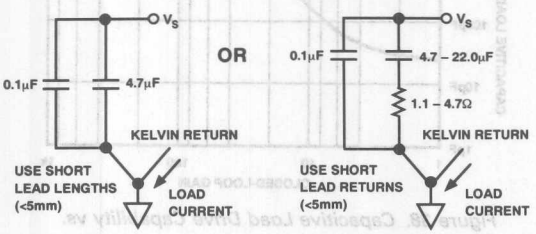


Figure 32. Recommended Power Supply Bypassing

THE NONINVERTING CONFIGURATION

Ultralow noise requires very low values of r_{BB}' (the internal parasitic resistance) for the input transistors (≈ 6 Ω). This implies very little damping of input and output reactive interactions. With the AD797, additional input series damping is required for stability with direct input to output feedback. A 100 Ω resistor in the inverting input (Figure 33) is sufficient; the 100 Ω balancing resistor (R2) is recommended, but is not required for stability. The noise penalty is minimal (e_N*total* ≈2.1 nV$\sqrt{\text{Hz}}$), which is usually insignificant. Best response flatness is obtained with the addition of a small capacitor (C_L <33 pF) in parallel with the 100 Ω resistor (Figure 34). The input source resistance and capacitance will also affect the response slightly and experimentation may be necessary for best results.

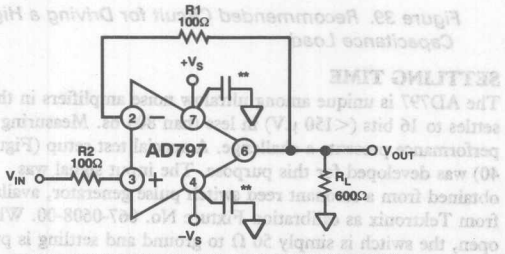


Figure 33. Voltage Follower Connection

Low noise preamplification is usually done in the noninverting mode (Figure 35). For lowest noise the equivalent resistance of the feedback network should be as low as possible. The 30 mA minimum drive current of the AD797 makes it easier to achieve this. The feedback resistors can be made as low as possible with due consideration to load drive and power consumption. Table II gives some representative values for the AD797 as a low noise follower. Operation on 5 volt supplies allows the use of a 100 Ω or less feedback network (R1+ R2). Since the AD797 shows no unusual behavior when operating near its maximum rated current, it is suitable for driving the AD600/AD602 (Figure 47) while preserving their low noise performance.

Optimum flatness and stability at noise gains >1 sometimes requires a small capacitor (C_L) connected across the feedback resistor (R1, Figure 35). Table II includes recommended values of C_L for several gains. In general, when R2 is greater than 100 Ω and C_L is greater than 33 pF, a 100 Ω resistor should be placed in series with C_L. Source resistance matching is assumed, and the AD797 should never be operated with unbalanced source resistance >200 kΩ/G.

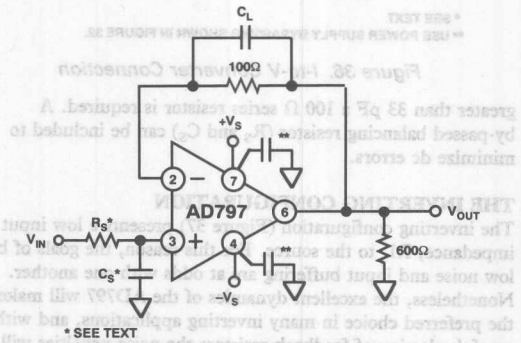


Figure 34. Alternative Voltage Follower Connection

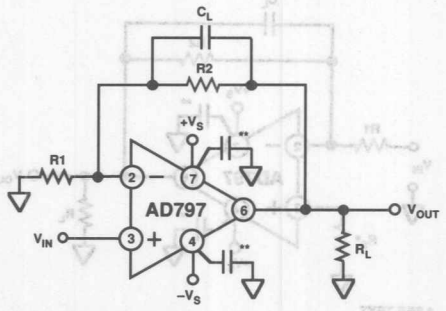
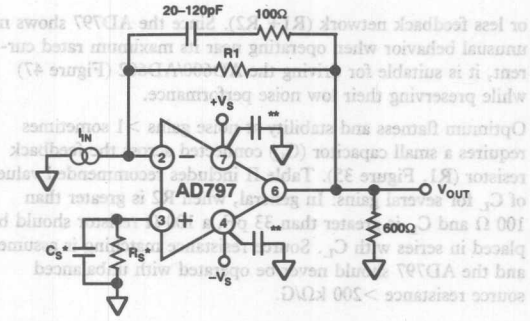


Figure 35. Low Noise Preamplifier

Table II. Values for Follower with Gain Circuit

Gain	R1	R2	C_L	Noise (Excluding r_S)
2	1 kΩ	1 kΩ	≈20 pF	3.0 nV$\sqrt{\text{Hz}}$
2	300 Ω	300 Ω	≈10pF	1.8 nV$\sqrt{\text{Hz}}$
10	33.2 Ω	300 Ω	≈5 pF	1.2 nV$\sqrt{\text{Hz}}$
20	16.5 Ω	316 Ω		1.0 nV$\sqrt{\text{Hz}}$
>35	10 Ω	(G–1) 10 Ω		0.98 nV$\sqrt{\text{Hz}}$

The I-to-V converter is a special case of the follower configuration. When the AD797 is used in an I-to-V converter, for instance as a DAC buffer, the circuit of Figure 36 should be used. The value of C_L depends on the DAC and again, if C_L is



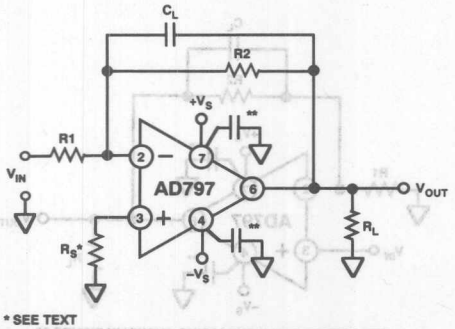
* SEE TEXT
** USE POWER SUPPLY BYPASSING SHOWN IN FIGURE 32.

Figure 36. I-to-V Converter Connection

greater than 33 pF a 100 Ω series resistor is required. A by-passed balancing resistor (R_S and C_S) can be included to minimize dc errors.

THE INVERTING CONFIGURATION

The inverting configuration (Figure 37) presents a low input impedance, R1, to the source. For this reason, the goals of both low noise and input buffering are at odds with one another. Nonetheless, the excellent dynamics of the AD797 will make it the preferred choice in many inverting applications, and with careful selection of feedback resistors the noise penalties will be minimal. Some examples are presented in Table II and Figure 37.



* SEE TEXT
** USE POWER SUPPLY BYPASSING SHOWN IN FIGURE 32.

Figure 37. Inverting Amplifier Connection

Table III. Values for Inverting Circuit

Gain	R1	R2	C_L	Noise (Excluding r_S)
−1	1 kΩ	1 kΩ	≈20 pF	3.0 nV/√Hz
−1	300 Ω	300 Ω	≈10 pF	1.8 nV/√Hz
−10	150 Ω	1500 Ω	≈5 pF	1.8 nV/√Hz

DRIVING CAPACITIVE LOADS

The capacitive load driving capabilities of the AD797 are displayed in Figure 38. At gains over 10 usually no special precautions are necessary. If more drive is desirable the circuit in Figure 39 should be used. Here a 5000 pF load can be driven cleanly at any noise gain > = 2.

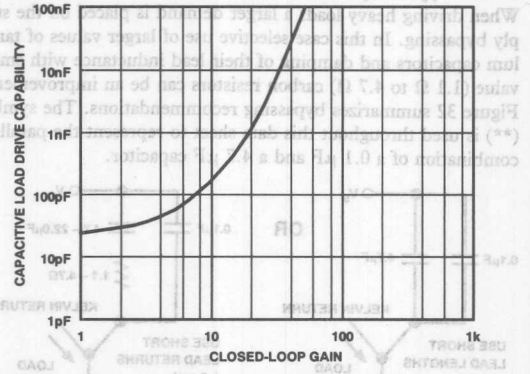
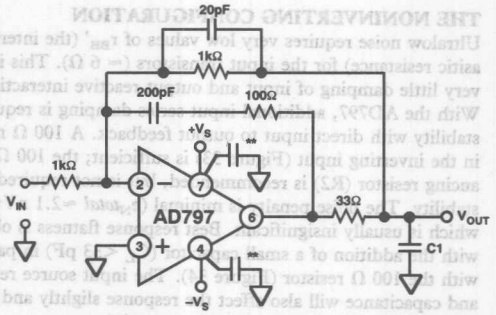


Figure 38. Capacitive Load Drive Capability vs. Closed-Loop Gain



** USE POWER SUPPLY BYPASSING SHOWN IN FIGURE 32.

Figure 39. Recommended Circuit for Driving a High Capacitance Load

SETTLING TIME

The AD797 is unique among ultralow noise amplifiers in that it settles to 16 bits (<150 μV) in less than 800 ns. Measuring this performance presents a challenge. A special test setup (Figure 40) was developed for this purpose. The input signal was obtained from a resonant reed switch pulse generator, available from Tektronix as calibration Fixture No. 067-0608-00. When open, the switch is simply 50 Ω to ground and settling is purely a passive pulse decay and inherently flat. The low repetition rate signal was captured on a digital oscilloscope after being amplified and clamped twice. The selection of plug-in for the oscilloscope was made for minimum overload recovery.

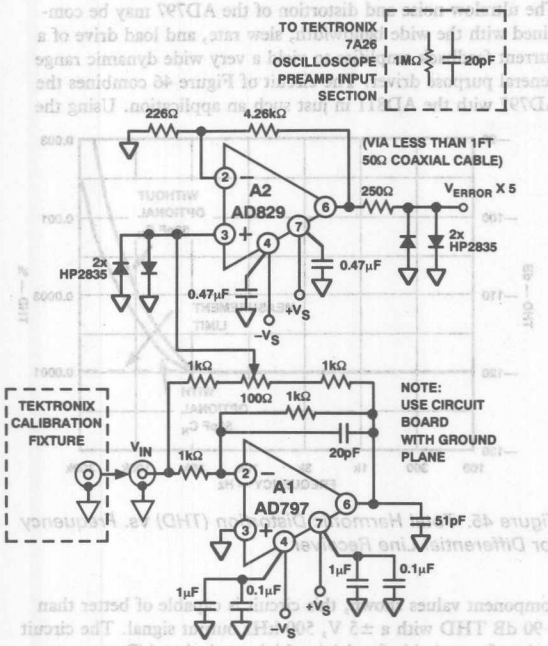


Figure 40. Settling Time Test Circuit

DISTORTION REDUCTION

The AD797 has distortion performance (THD < −120 dB, @ 20 kHz, 3 V rms, RL = 600 Ω) unequaled by most voltage feedback amplifiers.

At higher gains and higher frequencies THD will increase due to reduction in loop gain. However in contrast to most conventional voltage feedback amplifiers the AD797 provides two effective means of reducing distortion, as gain and frequency are increased; cancellation of the output stage's distortion and gain bandwidth enhancement by decompensation. By applying these techniques gain bandwidth can be increased to 450 MHz at G = 1000 and distortion can be held to −100 dB at 20 kHz for G = 100.

The unique design of the AD797 provides for cancellation of the output stage's distortion (patent pending). To achieve this a capacitance equal to the effective compensation capacitance, usually 50 pF, is connected between Pin 8 and the output (C2 in Figure 41). Use of this feature will improve distortion performance when the closed loop gain is more than 10 or when frequencies of interest are greater than 30 kHz.

Bandwidth enhancement via decompensation is achieved by connecting a capacitor from Pin 8 to ground (C1 in Figure 41) effectively subtracting from the value of the internal compensation capacitance (50 pF), yielding a smaller effective compensation capacitance and, therefore, a larger bandwidth. The benefits of this begin at closed loop gains of 100 and up. A maximum value of ≈33 pF at gains of 1000 and up is recommended. At a gain of 1000 the bandwidth is 450 kHz.

Table IV and Figure 42 summarize the performance of the AD797 with distortion cancellation and decompensation.

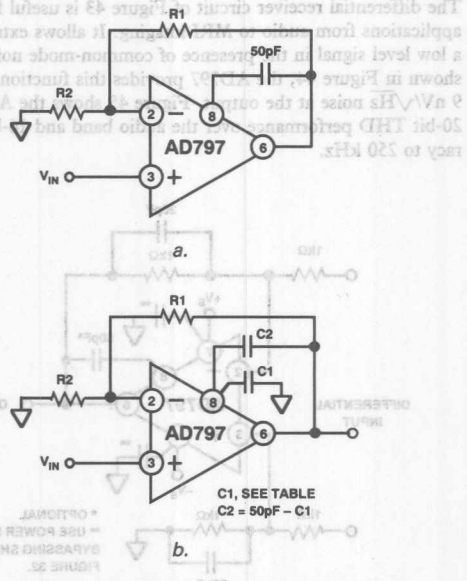


Figure 41. Recommended Connections for Distortion Cancellation and Bandwidth Enhancement

Table IV. Recommended External Compensation

	A/B		A			B		
	R1 Ω	R2 Ω	C1 (pF)	C2 (pF)	3 dB BW	C1 (pF)	C2 (pF)	3 dB BW
G = 10	909	100	0	50	6 MHz	0	50	6 MHz
G = 100	1 k	10	0	50	1 MHz	15	33	1.5 MHz
G = 1000	10 k	10	0	50	110 kHz	33	15	450 kHz

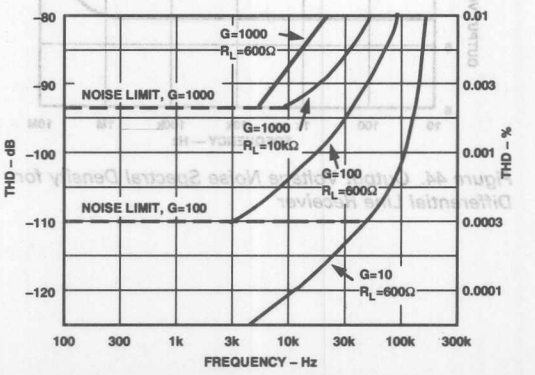


Figure 42. Total Harmonic Distortion (THD) vs. Frequency @ 3 V rms for Figure 41b

Differential Line Receiver

The differential receiver circuit of Figure 43 is useful for many applications from audio to MRI imaging. It allows extraction of a low level signal in the presence of common-mode noise. As shown in Figure 44, the AD797 provides this function with only 9 nV/$\sqrt{\text{Hz}}$ noise at the output. Figure 45 shows the AD797's 20-bit THD performance over the audio band and 16-bit accuracy to 250 kHz.

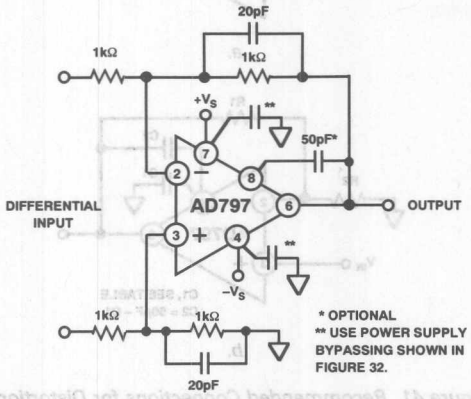


Figure 43. Differential Line Receiver

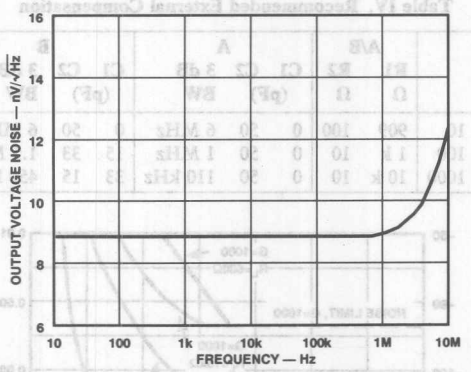


Figure 44. Output Voltage Noise Spectral Density for Differential Line Receiver

A General Purpose ATE/Instrumentation Input/Output Driver

The ultralow noise and distortion of the AD797 may be combined with the wide bandwidth, slew rate, and load drive of a current feedback amplifier to yield a very wide dynamic range general purpose driver. The circuit of Figure 46 combines the AD797 with the AD811 in just such an application. Using the

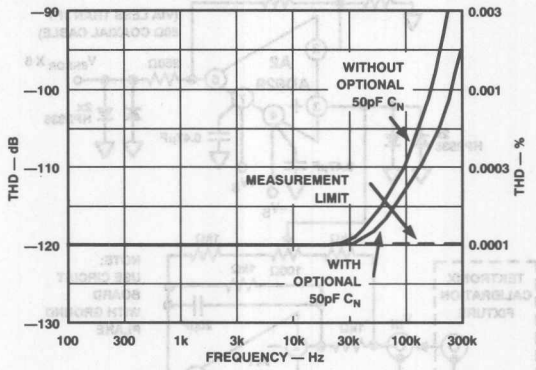


Figure 45. Total Harmonic Distortion (THD) vs. Frequency for Differential Line Receiver

component values shown, this circuit is capable of better than −90 dB THD with a ±5 V, 500 kHz output signal. The circuit is therefore suitable for driving high resolution A/D converters and as an output driver in automatic test equipment (ATE) systems. Using a 100 kHz sine wave, the circuit will drive a 600 Ω load to a level of 7 V rms with less than −109 dB THD, and a 10 kΩ load at less than −117 dB THD.

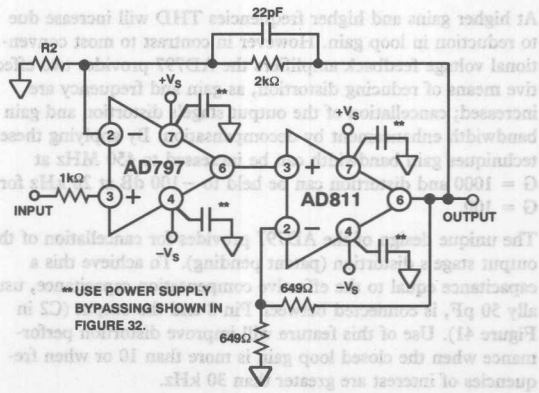


Figure 46. A General Purpose ATE/Instrumentation Input/Output Driver

Ultrasound/Sonar Imaging Preamp

The AD600 variable gain amplifier provides the time controlled gain (TCG) function necessary for very wide dynamic range sonar and low frequency ultrasound applications. Under some circumstances, it is necessary to buffer the input of the AD600 to preserve its low noise performance. To optimize dynamic range this buffer should have at most 6 dB of gain. The combination of low noise and low gain is difficult to achieve. The input buffer circuit shown in Figure 47 provides 1 nV$\sqrt{\text{Hz}}$ noise performance at a gain of two (dc to 1 MHz) by using 26.1 Ω resistors in its feedback path. Distortion is only −50 dBc @ 1 MHz at a 2 volt p–p output level and drops rapidly to better than −70 dBc at an output level of 200 mV p–p.

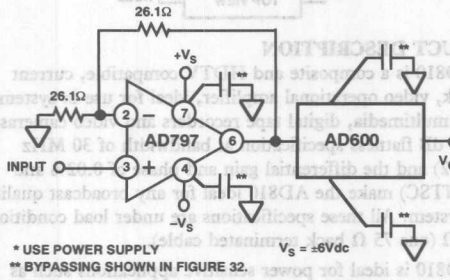


Figure 47. An Ultrasound Preamplifier Circuit

Amorphous (Photodiode) Detector

Large area photodiodes $C_S \geq 500$ pF and certain image detectors (amorphous Si), have optimum performance when used in conjunction with amplifiers with very low voltage rather than very low current noise. Figure 48 shows the AD797 used with an amorphous Si (C_S = 1000 pF) detector. The response is adjusted for flatness using capacitor C_L, while the noise is dominated by voltage noise amplified by the ac noise gain. The 797's excellent input noise performance gives 27 μV rms total noise in a 1 MHz bandwidth, as shown by Figure 49.

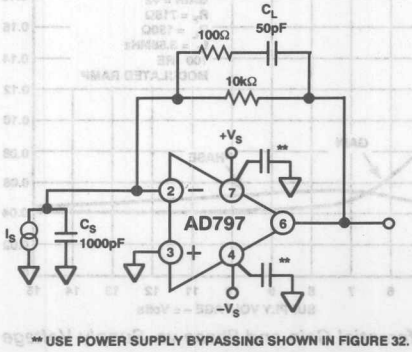


Figure 48. Amorphous Detector Preamp

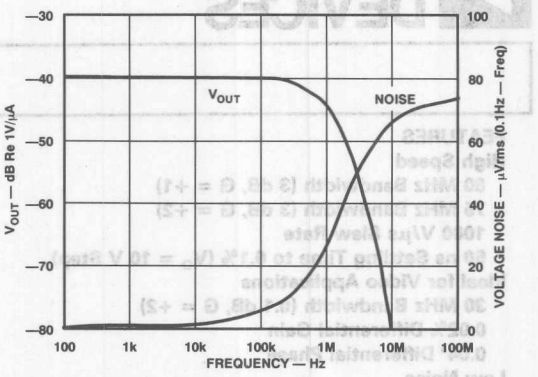


Figure 49. Total Integrated Voltage Noise & V_{OUT} of Amorphous Detector Preamp

Professional Audio Signal Processing—DAC Buffers

The low noise and low distortion of the AD797 make it an ideal choice for professional audio signal processing. An ideal I-to-V converter for a current output DAC would simply be a resistor to ground, were it not for the fact that most DACs do not operate linearly with voltage on their output. Standard practice is to operate an op amp as an I-to-V converter creating a virtual ground at its inverting input. Normally, clock energy and current steps must be absorbed by the op amp's output stage. However, in the configuration of Figure 50, Capacitor C_F shunts high frequency energy to ground, while correctly reproducing the desired output with extremely low THD and IMD.

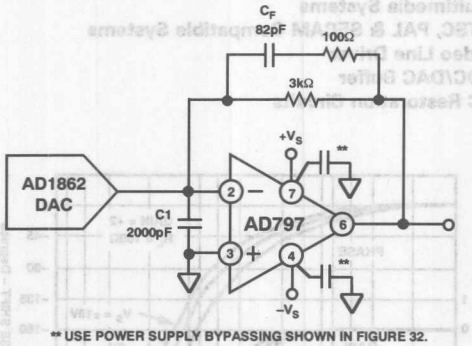


Figure 50. A Professional Audio DAC Buffer

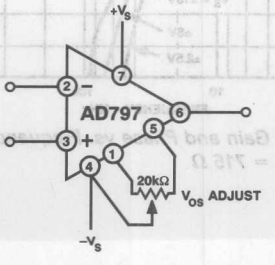


Figure 51. Offset Null Configuration

FEATURES

High Speed
- 80 MHz Bandwidth (3 dB, G = +1)
- 75 MHz Bandwidth (3 dB, G = +2)
- 1000 V/μs Slew Rate
- 50 ns Settling Time to 0.1% (V_O = 10 V Step)

Ideal for Video Applications
- 30 MHz Bandwidth (0.1 dB, G = +2)
- 0.02% Differential Gain
- 0.04° Differential Phase

Low Noise
- 2.9 nV/$\sqrt{Hz}$ Input Voltage Noise
- 13 pA/$\sqrt{Hz}$ Inverting Input Current Noise

Low Power
- 8.0 mA Supply Current max
- 2.1 mA Supply Current (Power-Down Mode)

High Performance Disable Function
- Turn-Off Time 100 ns
- Break Before Make Guaranteed
- Input to Output Isolation of 64 dB (OFF State)

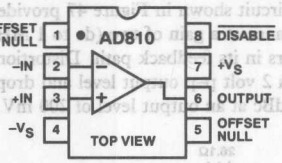
Flexible Operation
- Specified for ±5 V and ±15 V Operation
- ±2.9 V Output Swing Into a 150 Ω Load (V_S = ±5 V)

APPLICATIONS

Professional Video Cameras
Multimedia Systems
NTSC, PAL & SECAM Compatible Systems
Video Line Driver
ADC/DAC Buffer
DC Restoration Circuits

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), SOIC (R) and Cerdip (Q) Packages

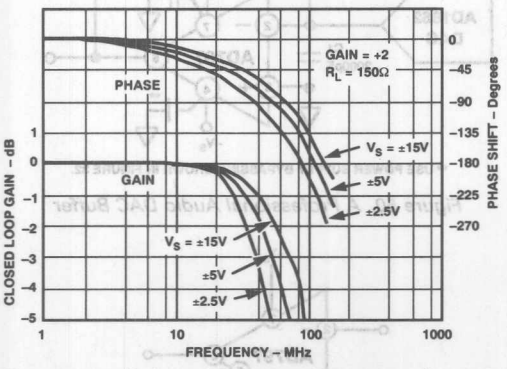


PRODUCT DESCRIPTION

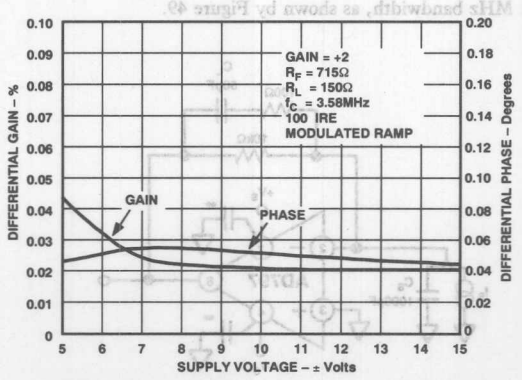
The AD810 is a composite and HDTV compatible, current feedback, video operational amplifier, ideal for use in systems such as multimedia, digital tape recorders and video cameras. The 0.1 dB flatness specification at bandwidth of 30 MHz (G = +2) and the differential gain and phase of 0.02% and 0.04° (NTSC) make the AD810 ideal for any broadcast quality video system. All these specifications are under load conditions of 150 Ω (one 75 Ω back terminated cable).

The AD810 is ideal for power sensitive applications such as video cameras, offering a low power supply current of 8.0 mA max. The disable feature reduces the power supply current to only 2.1 mA, while the amplifier is not in use, to conserve power. Furthermore the AD810 is specified over a power supply range of ±5 V to ±15 V.

The AD810 works well as an ADC or DAC buffer in video systems due to its unity gain bandwidth of 80 MHz. Because the AD810 is a transimpedance amplifier, this bandwidth can be maintained over a wide range of gains while featuring a low noise of 2.9 nV/$\sqrt{Hz}$ for wide dynamic range applications.



Closed-Loop Gain and Phase vs. Frequency, G = +2, R_L = 150, R_F = 715 Ω



Differential Gain and Phase vs. Supply Voltage

SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, R_L = 150 Ω unless otherwise noted)

Parameter	Conditions	V_S	AD810A Min	AD810A Typ	AD810A Max	AD810S[1] Min	AD810S[1] Typ	AD810S[1] Max	Units
DYNAMIC PERFORMANCE									
3 dB Bandwidth	(G = +2) R_{FB} = 715	±5 V	40	50		40	50		MHz
	(G = +2) R_{FB} = 715	±15 V	55	75		55	75		MHz
	(G = +1) R_{FB} = 1000	±15 V	40	80		40	80		MHz
	(G = +10) R_{FB} = 270	±15 V	50	65		50	65		MHz
0.1 dB Bandwidth	(G = +2) R_{FB} = 715	±5 V	13	22		13	22		MHz
	(G = +2) R_{FB} = 715	±15 V	15	30		15	30		MHz
Full Power Bandwidth	V_O = 20 V p-p,								
	R_L = 400 Ω	±15 V		16			16		MHz
Slew Rate[2]	R_L = 150 Ω	±5 V		350			350		V/µs
	R_L = 400 Ω	±15 V		1000			1000		V/µs
Settling Time to 0.1%	10 V Step, G = −1	±15 V		50			50		ns
Settling Time to 0.01%	10 V Step, G = −1	±15 V		125			125		ns
Differential Gain	f = 3.58 MHz	±15 V		0.02	0.05		0.02	0.05	%
	f = 3.58 MHz	±5 V		0.04	0.07		0.04	0.07	%
Differential Phase	f = 3.58 MHz	±15 V		0.04	0.07		0.04	0.07	Degrees
	f = 3.58 MHz	±5 V		0.045	0.08		0.045	0.08	Degrees
Total Harmonic Distortion	f = 10 MHz, V_O = 2 V p-p								
	R_L = 400 Ω, G = +2	±15 V		−61			−61		dBc
INPUT OFFSET VOLTAGE		±5 V, ±15 V		1.5	6		1.5	6	mV
	T_{MIN}–T_{MAX}	±5 V, ±15 V		2	7.5		4	15	mV
Offset Voltage Drift				7			15		µV/°C
INPUT BIAS CURRENT									
−Input	T_{MIN}–T_{MAX}	±5 V, ±15 V		0.7	5		0.8	5	µA
+Input	T_{MIN}–T_{MAX}	±5 V, ±15 V		2	7.5		2	10	µA
OPEN-LOOP	T_{MIN}–T_{MAX}								
TRANSRESISTANCE	V_O = ±10 V, R_L = 400 Ω	±15 V	1.0	3.5		1.0	3.5		MΩ
	V_O = ±2.5 V, R_L = 100 Ω	±5 V	0.3	1.2		0.2	1.0		MΩ
OPEN-LOOP	T_{MIN}–T_{MAX}								
DC VOLTAGE GAIN	V_O = ±10 V, R_L = 400 Ω	±15 V	86	100		80	100		dB
	V_O = ±2.5 V, R_L = 100 Ω	±5 V	76	88		72	88		dB
COMMON-MODE REJECTION	T_{MIN}–T_{MAX}								
V_{OS}	V_{CM} = ±12 V	±15 V	56	64		56	64		dB
	V_{CM} = ±2.5 V	±5 V	52	60		50	60		dB
±Input Current	T_{MIN}–T_{MAX}	±5 V, ±15 V		0.1	0.4		0.1	0.4	µA/V
POWER SUPPLY REJECTION		±4.5 V to ±18 V							
V_{OS}	T_{MIN}–T_{MAX}		65	72		60	72		dB
±Input Current	T_{MIN}–T_{MAX}			0.05	0.3		0.05	0.3	µA/V
INPUT VOLTAGE NOISE	f = 1 kHz	±5 V, ±15 V		2.9			2.9		nV/√Hz
INPUT CURRENT NOISE	$-I_{IN}$, f = 1 kHz	±5 V, ±15 V		13			13		pA/√Hz
	$+I_{IN}$, f = 1 kHz	±5 V, ±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE		±5 V	±2.5	±3.0		±2.5	±3		V
VOLTAGE RANGE		±15 V	±12	±13		±12	±13		V
OUTPUT CHARACTERISTICS									
Output Voltage Swing[3]	R_L = 150 Ω, T_{MIN}–T_{MAX}	±5 V	±2.5	±2.9		±2.5	±2.9		V
	R_L = 400 Ω	±15 V	±12.5	±12.9		±12.5	±12.9		V
	R_L = 400 Ω, T_{MIN}–T_{MAX}	±15 V	±12			±12			V
Short-Circuit Current		±15 V		150			150		mA
Output Current	T_{MIN}–T_{MAX}	±5 V, ±15 V	40	60		30	60		mA
OUTPUT RESISTANCE	Open Loop (5 MHz)			15			15		Ω
INPUT CHARACTERISTICS									
Input Resistance	+Input	±15 V	2.5	10		2.5	10		MΩ
	−Input	±15 V		40			40		Ω
Input Capacitance	+Input	±15 V		2			2		pF
DISABLE CHARACTERISTICS[4]									
OFF Isolation	f = 5 MHz, See Figure 43			64			64		dB
OFF Output Impedance	See Figure 43			(R_F+R_G)‖13 pF			(R_F+R_G)‖13 pF		

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Parameter	Conditions	V_S	AD810A Min	AD810A Typ	AD810A Max	AD810S[1] Min	AD810S[1] Typ	AD810S[1] Max	Units
Turn On Time[5]	Z_{OUT} = Low, See Figure 54			170			170		ns
Turn Off Time	Z_{OUT} = High			100			100		ns
Disable Pin Current	Disable Pin = 0 V	±5 V		50	75		50	75	µA
		±15 V		290	400		290	400	µA
Min Disable Pin Current to Disable	T_{MIN}–T_{MAX}	±5 V, ±15 V		30			30		µA
POWER SUPPLY									
Operating Range	+25°C to T_{MAX}		±2.5		±18	±2.5		±18	V
	T_{MIN}		±3.0		±18	±3.5		±18	V
Quiescent Current		±5 V		6.7	7.5		6.7	7.5	mA
		±15 V		6.8	8.0		6.8	8.0	mA
	T_{MIN}–T_{MAX}	±5 V, ±15 V		8.3	10.0		9	11.0	mA
Power-Down Current		±5 V		1.8	2.3		1.8	2.3	mA
		±15 V		2.1	2.8		2.1	2.8	mA

NOTES
[1]See Analog Devices Military Data Sheet for 883B Specifications.
[2]Slew rate measurement is based on 10% to 90% rise time with the amplifier configured for a gain of −10.
[3]Voltage Swing is defined as useful operating range, not the saturation range.
[4]Disable guaranteed break before make.
[5]Turn On Time is defined with ±5 V supplies using complementary output CMOS to drive the disable pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . Observe Derating Curves
Output Short Circuit Duration . . . . Observe Derating Curves
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
Plastic DIP . . . . . −65°C to +125°C
Cerdip . . . . . −65°C to +150°C
Small Outline IC . . . . . −65°C to +125°C
Operating Temperature Range
AD810A . . . . . −40°C to +85°C
AD810S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 90°C/Watt; 8-Pin Cerdip Package: θ_{JA} = 110°C/Watt; 8-Pin SOIC Package: θ_{JA} = 150°C/Watt.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD810 features ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

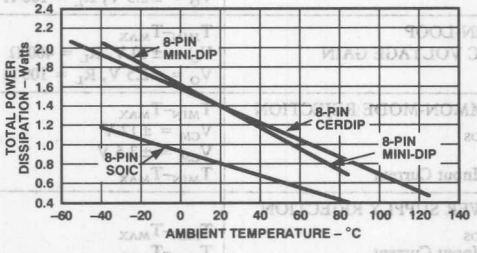
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD810AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD810AR	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD810AR-REEL	−40°C to +85°C	8-Pin Plastic SOIC	R-8
5962-9313201MPA	−55°C to +125°C	8-Pin Cerdip	Q-8

*For outline information see Package Information section.

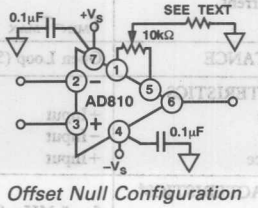
MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD810 is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 145°C. For the cerdip package, the maximum junction temperature is 175°C. If these maximums are exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the "overheated" condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves.



Maximum Power Dissipation vs. Temperature

While the AD810 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions.



Offset Null Configuration

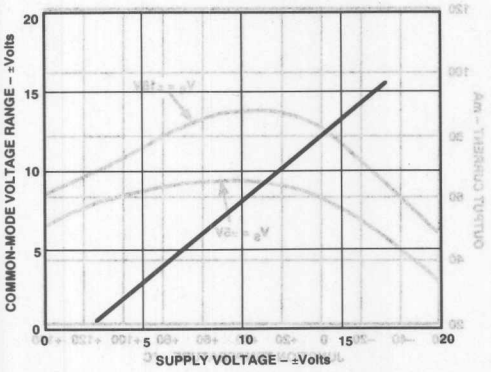


Figure 1. Input Common-Mode Voltage Range vs. Supply Voltage

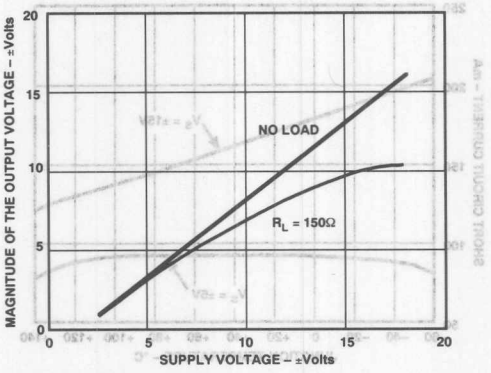


Figure 2. Output Voltage Swing vs. Supply

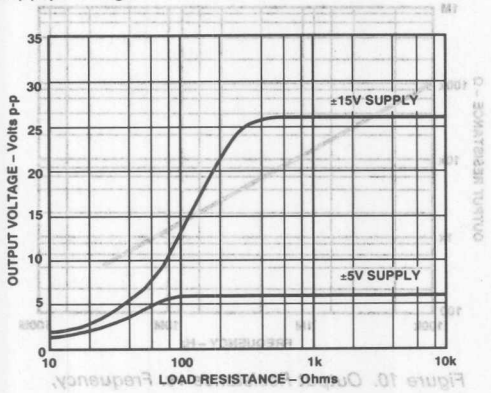


Figure 3. Output Voltage Swing vs. Load Resistance

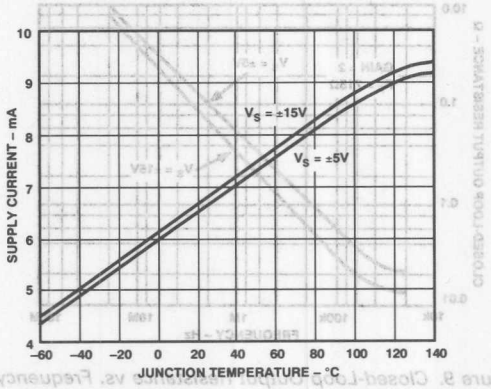


Figure 4. Supply Current vs. Junction Temperature

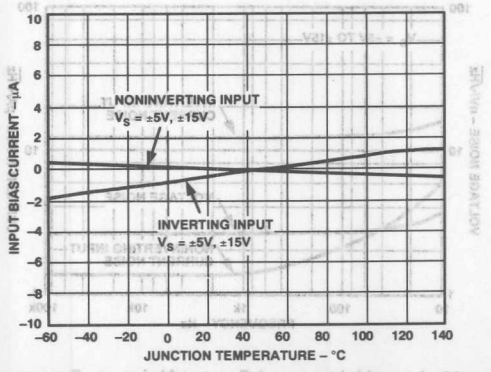


Figure 5. Input Bias Current vs. Temperature

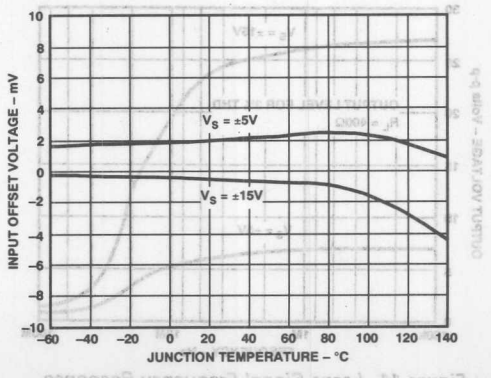


Figure 6. Input Offset Voltage vs. Junction Temperature

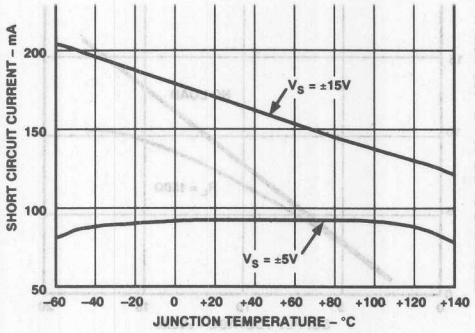


Figure 7. Short Circuit Current vs. Temperature

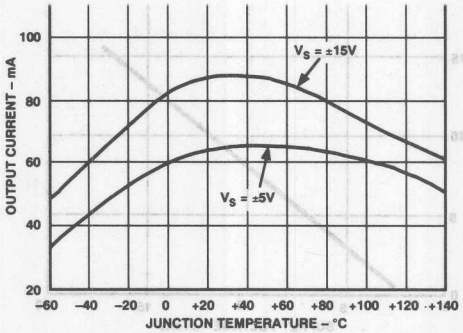


Figure 8. Linear Output Current vs. Temperature

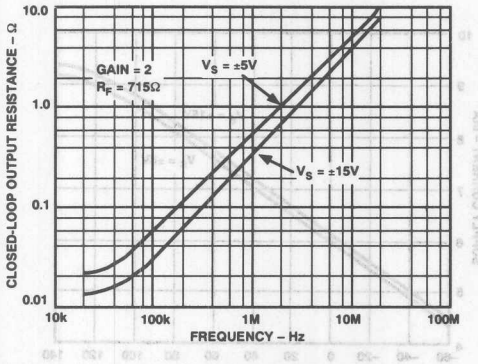


Figure 9. Closed-Loop Output Resistance vs. Frequency

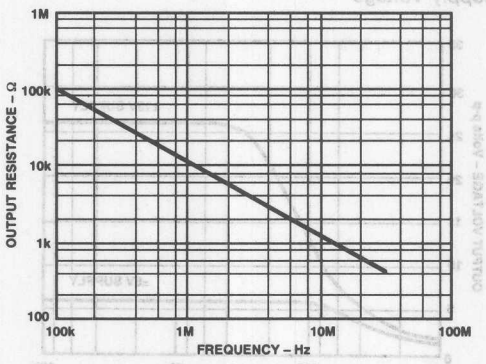


Figure 10. Output Resistance vs. Frequency, Disabled State

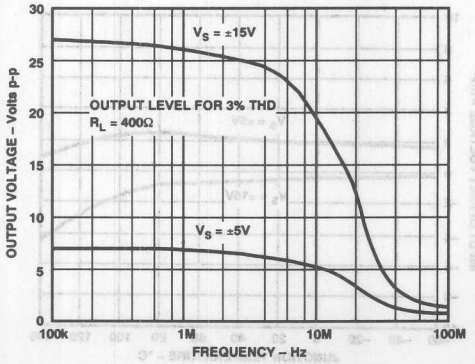


Figure 11. Large Signal Frequency Response

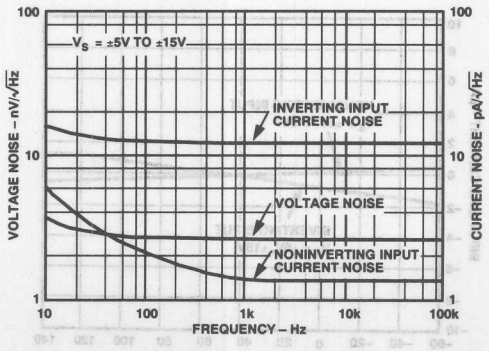


Figure 12. Input Voltage and Current Noise vs. Frequency

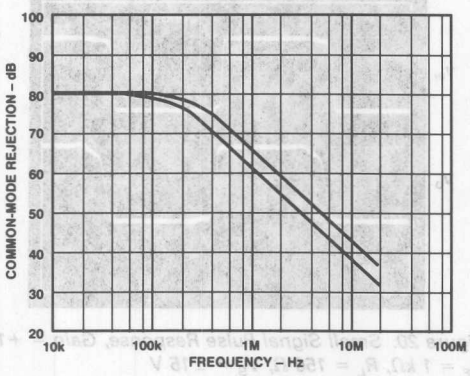


Figure 13. Common-Mode Rejection vs. Frequency

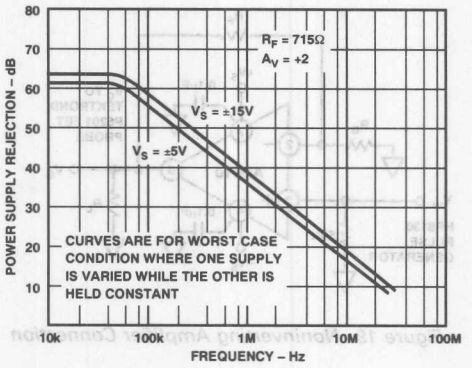


Figure 14. Power Supply Rejection vs. Frequency

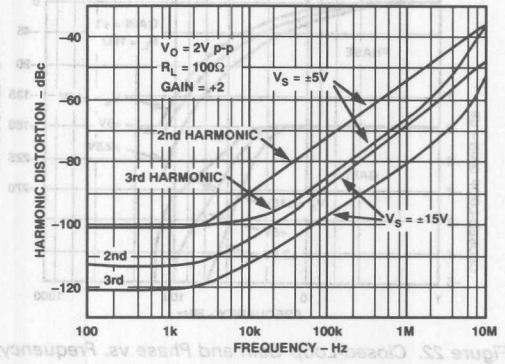


Figure 15. Harmonic Distortion vs. Frequency (R_L = 100 Ω)

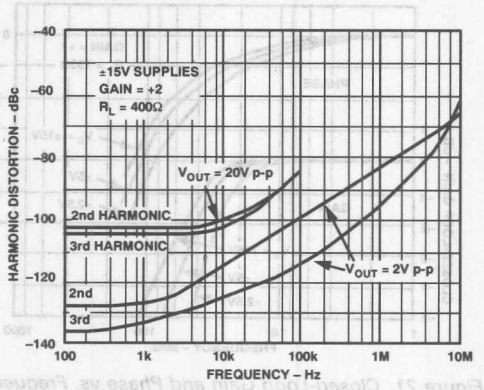


Figure 16. Harmonic Distortion vs. Frequency (R_L = 400 Ω)

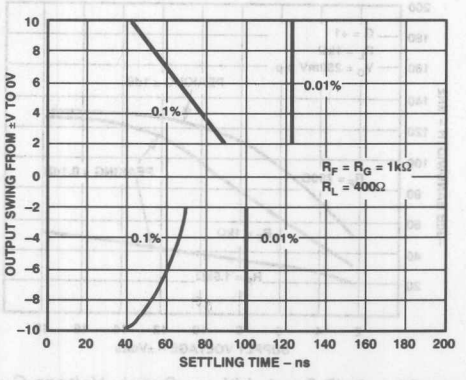


Figure 17. Output Swing and Error vs. Settling Time

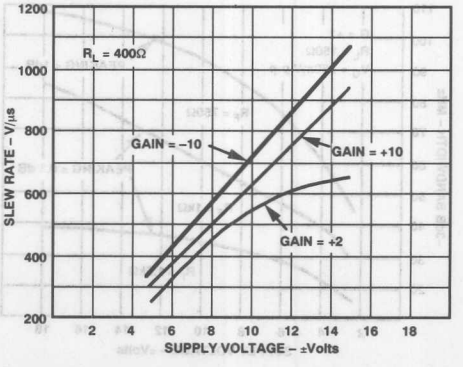


Figure 18. Slew Rate vs. Supply Voltage

AD810 — Typical Characteristics, Noninverting Connection

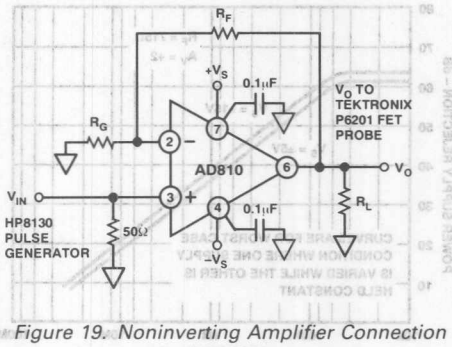


Figure 19. Noninverting Amplifier Connection

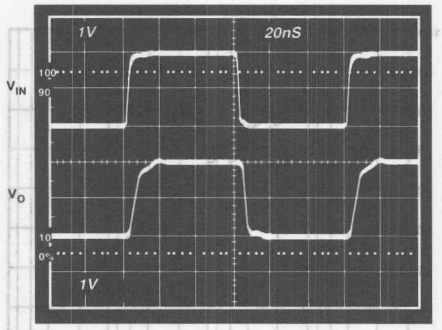


Figure 20. Small Signal Pulse Response, Gain = +1, R_F = 1 kΩ, R_L = 150 Ω, V_S = ±15 V

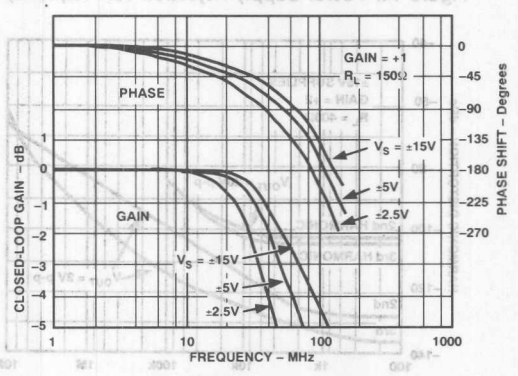


Figure 21. Closed-Loop Gain and Phase vs. Frequency, G = +1. R_F = 1 kΩ for ±15 V, 910 Ω for ±5 V and ±2.5 V

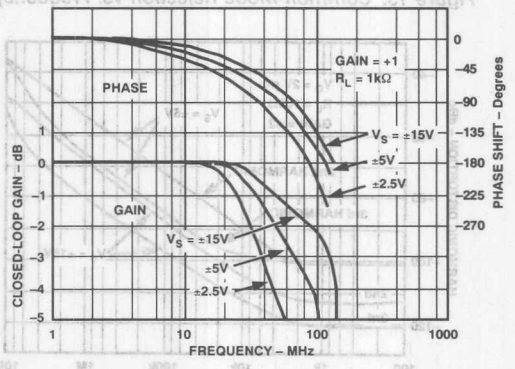


Figure 22. Closed-Loop Gain and Phase vs. Frequency, G = +1, R_F = 1 kΩ for ±15 V, 910 Ω for ±5 V and ±2.5 V

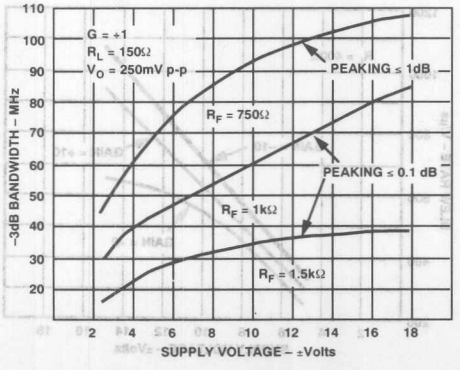


Figure 23. Bandwidth vs. Supply Voltage, Gain = +1, R_L = 150 Ω

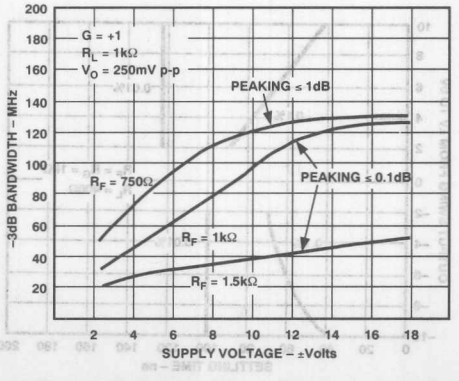


Figure 24. −3 dB Bandwidth vs. Supply Voltage G = +1, R_L = 1 kΩ

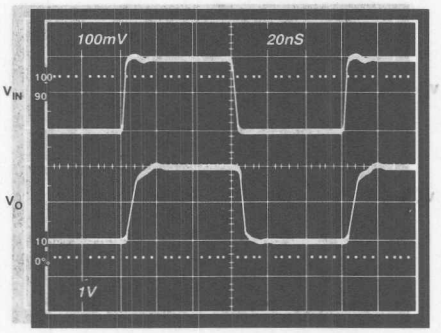


Figure 25. Small Signal Pulse Response, Gain = +10, R_F = 442 Ω, R_L = 150 Ω, V_S = ±15 V

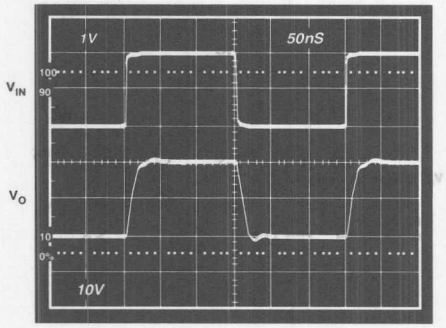


Figure 26. Large Signal Pulse Response, Gain = +10, R_F = 442 Ω, R_L = 400 Ω, V_S = ±15 V

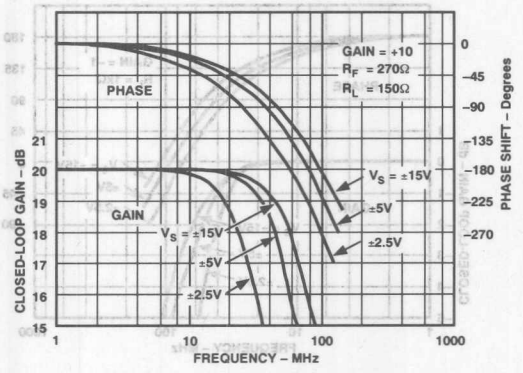


Figure 27. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 150 Ω

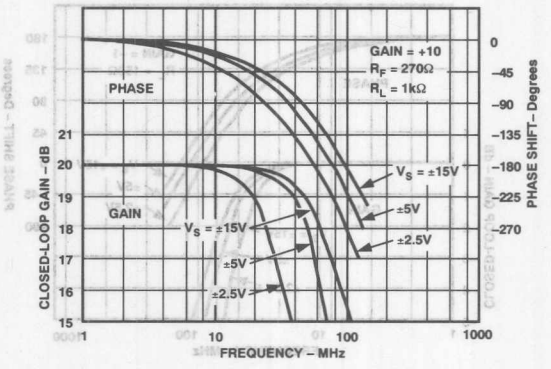


Figure 28. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 1 kΩ

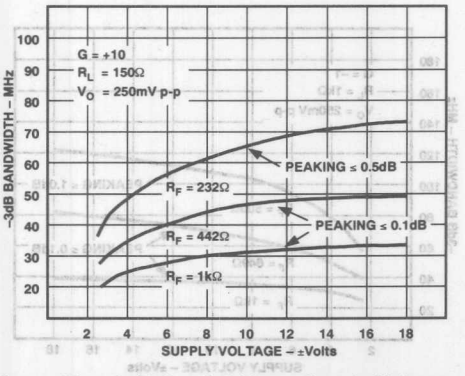


Figure 29. −3 dB Bandwidth vs. Supply Voltage, Gain = +10, R_L = 150 Ω

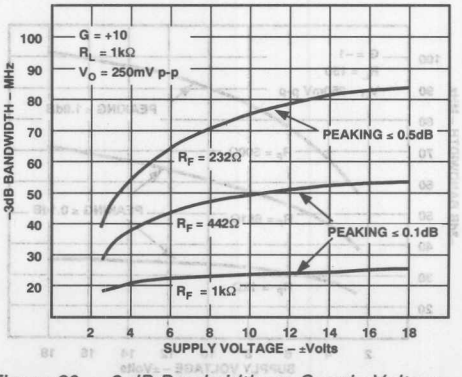


Figure 30. −3 dB Bandwidth vs. Supply Voltage, Gain = +10, R_L = 1 kΩ

AD810 — Typical Characteristics, Inverting Connection

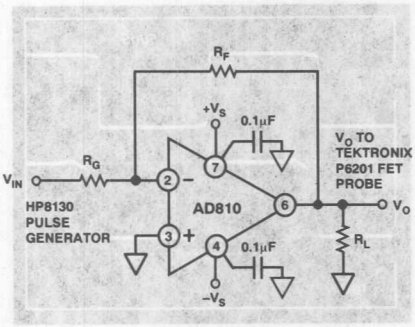


Figure 31. Inverting Amplifier Connection

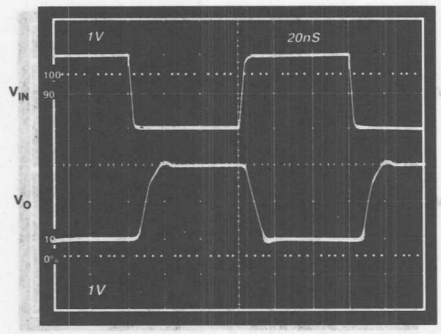


Figure 32. Small Signal Pulse Response, Gain = −1, R_F = 681 Ω, R_L = 150 Ω, V_S = ±5 V

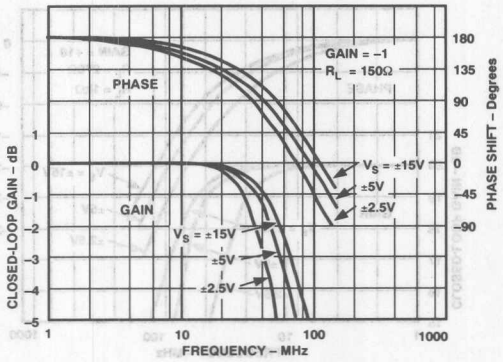


Figure 33. Closed-Loop Gain and Phase vs. Frequency, G = −1, R_L = 150 Ω, R_F = 681 Ω for ±15 V, 620 Ω for ±5 V and ±2.5 V

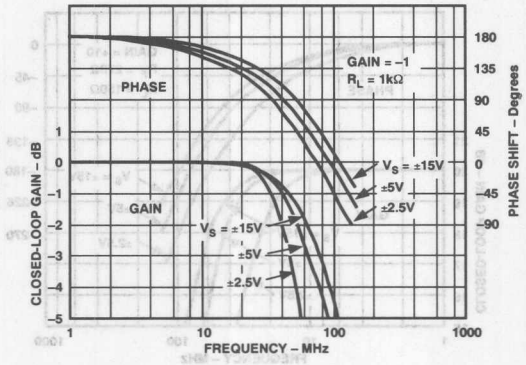


Figure 34. Closed-Loop Gain and Phase vs. Frequency, G = −1, R_L = 1 kΩ, R_F = 681 Ω for V_S = ±15 V, 620 Ω for ±5 V and ±2.5 V

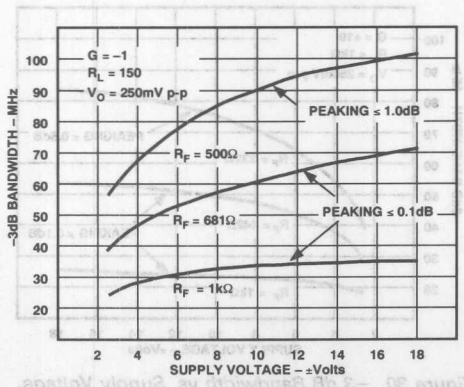


Figure 35. −3 dB Bandwidth vs. Supply Voltage, Gain = −1, R_L = 150 Ω

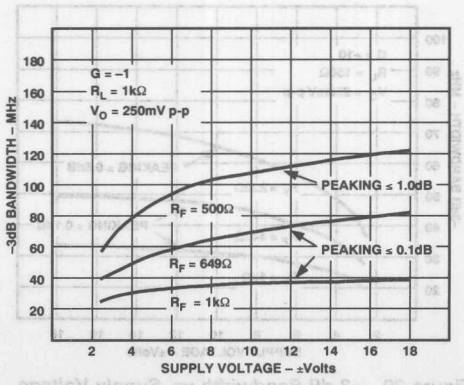


Figure 36. −3 dB Bandwidth vs. Supply Voltage, Gain = −1, R_L = 1 kΩ

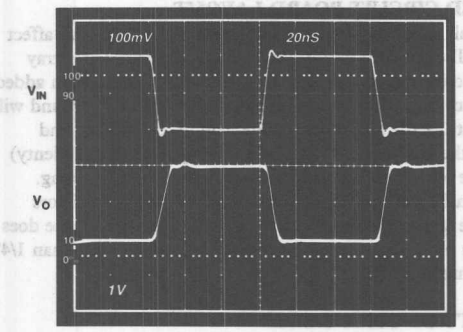


Figure 37. Small Signal Pulse Response, Gain = −10, R_F = 442 Ω, R_L = 150 Ω, V_S = ±15 V

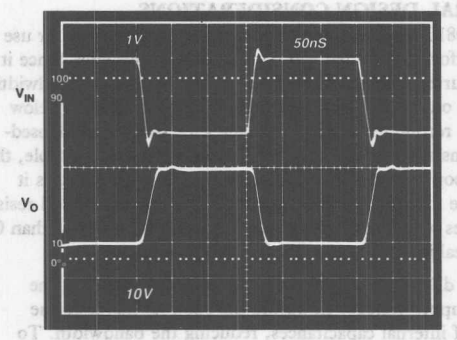


Figure 38. Large Signal Pulse Response, Gain = −10, R_F = 442 Ω, R_L = 400 Ω, V_S = ±15 V

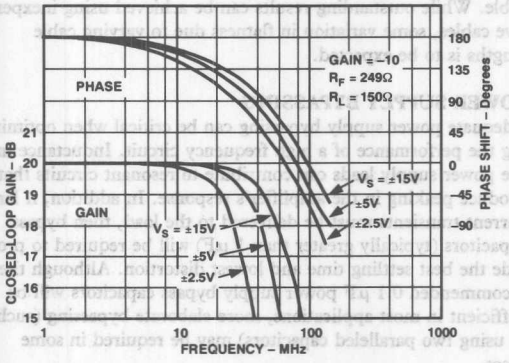


Figure 39. Closed-Loop Gain and Phase vs. Frequency, G = −10, R_L = 150 Ω

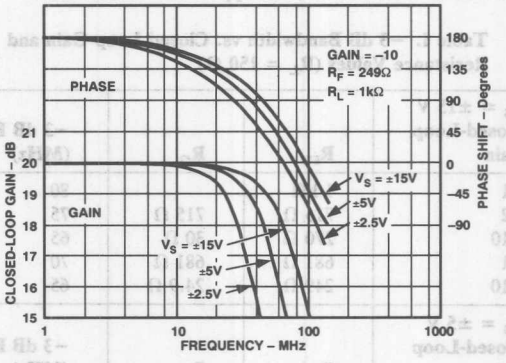


Figure 40. Closed-Loop Gain and Phase vs. Frequency, G = −10, R_L = 1 kΩ

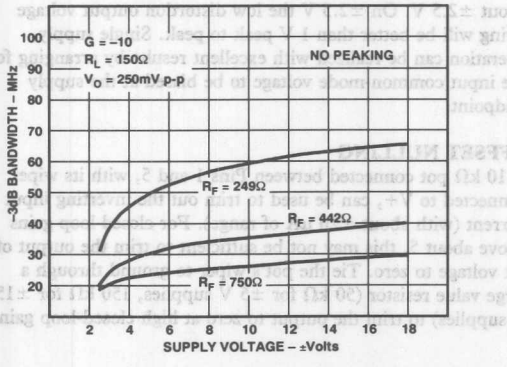


Figure 41. −3 dB Bandwidth vs. Supply Voltage, G = −10, R_L = 150 Ω

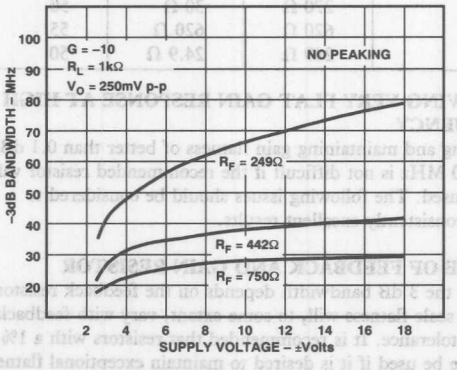


Figure 42. −3 dB Bandwidth vs. Supply Voltage, G = −10, R_L = 1 kΩ

AD810 — Applications

GENERAL DESIGN CONSIDERATIONS

The AD810 is a current feedback amplifier optimized for use in high performance video and data acquisition systems. Since it uses a current feedback architecture, its closed-loop bandwidth depends on the value of the feedback resistor. Table I below contains recommended resistor values for some useful closed-loop gains and supply voltages. As you can see in the table, the closed-loop bandwidth is not a strong function of gain, as it would be for a voltage feedback amp. The recommended resistor values will result in maximum bandwidths with less than 0.1 dB of peaking in the gain vs. frequency response.

The −3 dB bandwidth is also somewhat dependent on the power supply voltage. Lowering the supplies increases the values of internal capacitances, reducing the bandwidth. To compensate for this, smaller values of feedback resistor are sometimes used at lower supply voltages. The characteristic curves illustrate that bandwidths of over 100 MHz on 30 V total and over 50 MHz on 5 V total supplies can be achieved.

Table I. −3 dB Bandwidth vs. Closed-Loop Gain and Resistance Values (R_L = 150 Ω)

V_S = ±15 V Closed-Loop Gain	R_{FB}	R_G	−3 dB BW (MHz)
+1	1 kΩ		80
+2	715 Ω	715 Ω	75
+10	270 Ω	30 Ω	65
−1	681 Ω	681 Ω	70
−10	249 Ω	24.9 Ω	65
V_S = ±5 V Closed-Loop Gain	**R_{FB}**	**R_G**	**−3 dB BW (MHz)**
+1	910 Ω		50
+2	715 Ω	715 Ω	50
+10	270 Ω	30 Ω	50
−1	620 Ω	620 Ω	55
−10	249 Ω	24.9 Ω	50

ACHIEVING VERY FLAT GAIN RESPONSE AT HIGH FREQUENCY

Achieving and maintaining gain flatness of better than 0.1 dB above 10 MHz is not difficult if the recommended resistor values are used. The following issues should be considered to ensure consistently excellent results.

CHOICE OF FEEDBACK AND GAIN RESISTOR

Because the 3 dB bandwidth depends on the feedback resistor, the fine scale flatness will, to some extent, vary with feedback resistor tolerance. It is recommended that resistors with a 1% tolerance be used if it is desired to maintain exceptional flatness over a wide range of production lots.

PRINTED CIRCUIT BOARD LAYOUT

As with all wideband amplifiers, PC board parasitics can affect the overall close-loop performance. Most important are stray capacitances at the output and inverting input nodes. (An added capacitance of 2 pF between the inverting input and ground will add about 0.2 dB of peaking in the gain of 2 response, and increase the bandwidth to 105 MHz.) A space (3/16″ is plenty) should be left around the signal lines to minimize coupling. Also, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths less than 1/4″ are recommended.

QUALITY OF COAX CABLE

Optimum flatness when driving a coax cable is possible only when the driven cable is terminated at each end with a resistor matching its characteristic impedance. If coax were ideal, then the resulting flatness would not be affected by the length of the cable. While outstanding results can be achieved using inexpensive cables, some variation in flatness due to varying cable lengths is to be expected.

POWER SUPPLY BYPASSING

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can contribute to resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 μF) will be required to provide the best settling time and lowest distortion. Although the recommended 0.1 μF power supply bypass capacitors will be sufficient in most applications, more elaborate bypassing (such as using two paralleled capacitors) may be required in some cases.

POWER SUPPLY OPERATING RANGE

The AD810 will operate with supplies from ±18 V down to about ±2.5 V. On ±2.5 V the low distortion output voltage swing will be better than 1 V peak to peak. Single supply operation can be realized with excellent results by arranging for the input common-mode voltage to be biased at the supply midpoint.

OFFSET NULLING

A 10 kΩ pot connected between Pins 1 and 5, with its wiper connected to V+, can be used to trim out the inverting input current (with about ±20 μA of range). For closed-loop gains above about 5, this may not be sufficient to trim the output offset voltage to zero. Tie the pot's wiper to ground through a large value resistor (50 kΩ for ±5 V supplies, 150 kΩ for ±15 V supplies) to trim the output to zero at high closed-loop gains.

CAPACITIVE LOADS

When used with the appropriate feedback resistor, the AD810 can drive capacitive loads exceeding 1000 pF directly without oscillation. By using the curves in Figure 45 to chose the resistor value, less than 1 dB of peaking can easily be achieved without sacrificing much bandwidth. Note that the curves were generated for the case of a 10 kΩ load resistor, for smaller load resistances, the peaking will be less than indicated by Figure 45.

Another method of compensating for large load capacitances is to insert a resistor in series with the loop output as shown in Figure 43. In most cases, less than 50 Ω is all that is needed to achieve an extremely flat gain response.

Figures 44 to 46 illustrate the outstanding performance that can be achieved when driving a 1000 pF capacitor.

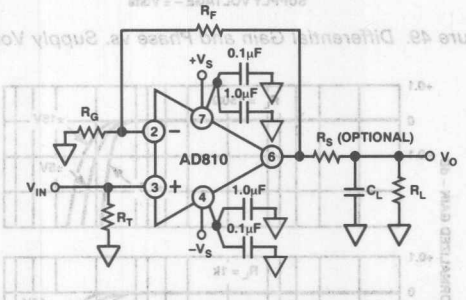


Figure 43. Circuit Options for Driving a Large Capacitive Load

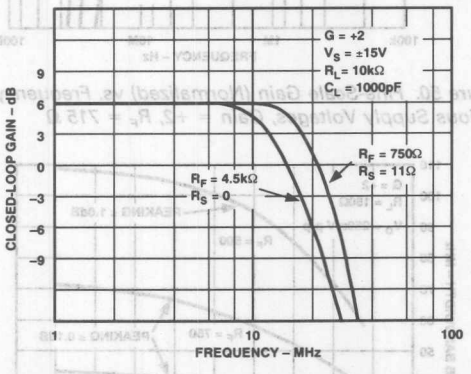


Figure 44. Performance Comparison of Two Methods for Driving a Large Capacitive Load

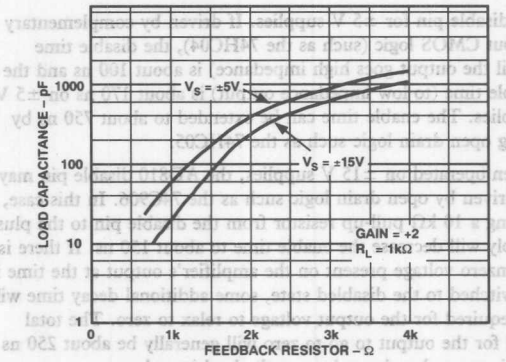


Figure 45. Max Load Capacitance for Less than 1 dB of Peaking vs. Feedback Resistor

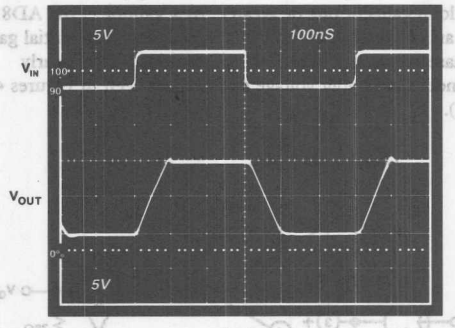


Figure 46. AD810 Driving a 1000 pF Load, Gain = +2, R_F = 750 Ω, R_S = 11 Ω, R_L = 10 kΩ

DISABLE MODE

By pulling the voltage on Pin 8 to common (0 V), the AD810 can be put into a disabled state. In this condition, the supply current drops to less than 2.8 mA, the output becomes a high impedance, and there is a high level of isolation from input to output. In the case of a line driver for example, the output impedance will be about the same as for a 1.5 kΩ resistor (the feedback plus gain resistors) in parallel with a 13 pF capacitor (due to the output) and the input to output isolation will be better than 65 dB at 1 MHz.

Leaving the disable pin disconnected (floating) will leave the AD810 operational in the enabled state.

In cases where the amplifier is driving a high impedance load, the input to output isolation will decrease significantly if the input signal is greater than about 1.2 V peak to peak. The isolation can be restored back to the 65 dB level by adding a dummy load (say 150 Ω) at the amplifier output. This will attenuate the feedthrough signal. (This is not an issue for multiplexer applications where the outputs of multiple AD810s are tied together as long as at least one channel is in the ON state.) The input impedance of the disable pin is about 35 kΩ in parallel with a few pF. When grounded, about 50 μA flows out of the disable

supplies. The enable time can be extended to about 750 ns by using open drain logic such as the 74HC05.

When operated on ±15 V supplies, the AD810 disable pin may be driven by open drain logic such as the 74C906. In this case, adding a 10 kΩ pull-up resistor from the disable pin to the plus supply will decrease the enable time to about 150 ns. If there is a nonzero voltage present on the amplifier's output at the time it is switched to the disabled state, some additional decay time will be required for the output voltage to relax to zero. The total time for the output to go to zero will generally be about 250 ns and is somewhat dependent on the load impedance.

OPERATION AS A VIDEO LINE DRIVER

The AD810 is designed to offer outstanding performance at closed-loop gains of one or greater. At a gain of 2, the AD810 makes an excellent video line driver. The low differential gain and phase errors and wide −0.1 dB bandwidth are nearly independent of supply voltage and load (as seen in Figures 49 and 50).

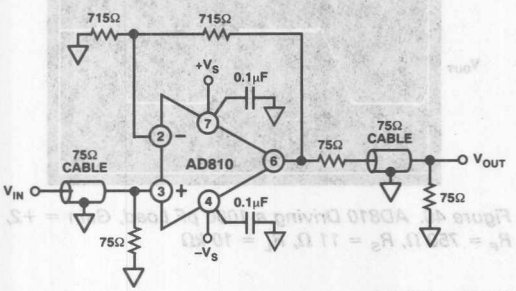


Figure 47. A Video Line Driver Operating at a Gain of +2

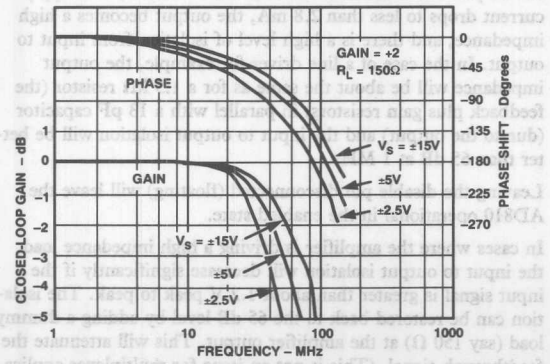


Figure 48. Closed-Loop Gain and Phase vs. Frequency, G = +2, R_L = 150, R_F = 715 Ω

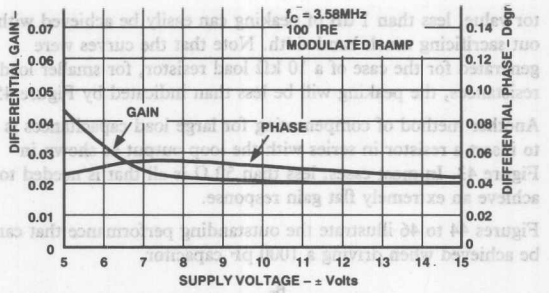


Figure 49. Differential Gain and Phase vs. Supply Voltage

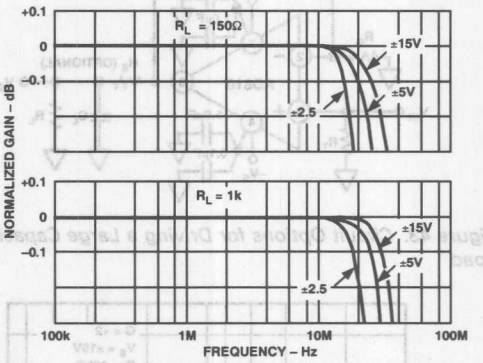


Figure 50. Fine-Scale Gain (Normalized) vs. Frequency for Various Supply Voltages, Gain = +2, R_F = 715 Ω

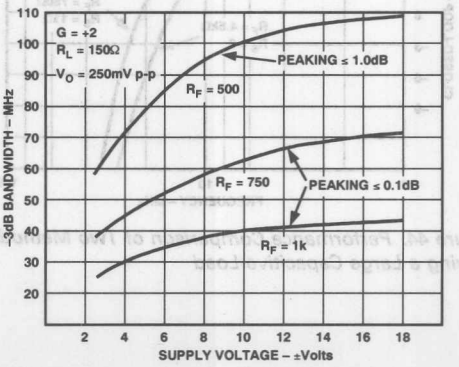


Figure 51. −3 dB Bandwidth vs. Supply Voltage, Gain = +2, R_L = 150 Ω

2:1 VIDEO MULTIPLEXER

The outputs of two AD810s can be wired together to form a 2:1 mux without degrading the flatness of the gain response. Figure 54 shows a recommended configuration which results in −0.1 dB bandwidth of 20 MHz and OFF channel isolation of 77 dB at 10 MHz on ±5 V supplies. The time to switch between channels is about 0.75 μs when the disable pins are driven by open drain output logic. Adding pull-up resistors to the logic outputs or using complementary output logic (such as the 74HC04) reduces the switching time to about 180 ns. The switching time is only slightly affected by the signal level.

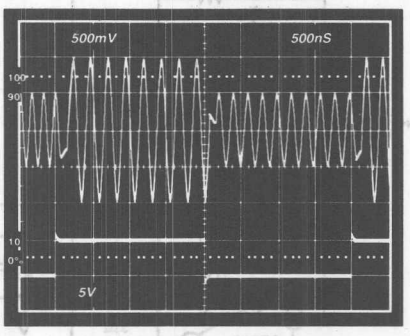


Figure 52. Channel Switching Time for the 2:1 Mux

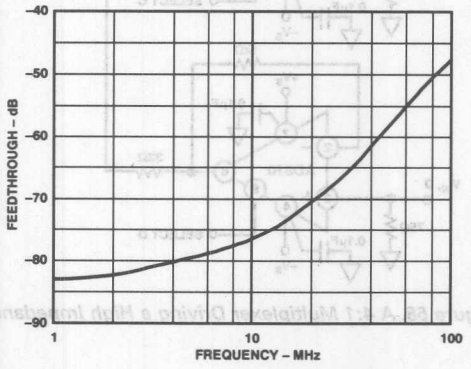


Figure 53. 2:1 Mux OFF Channel Feedthrough vs. Frequency

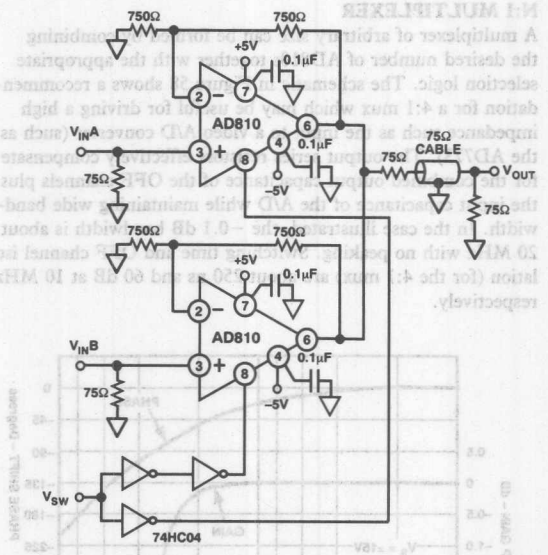


Figure 54. A Fast Switching 2:1 Video Mux

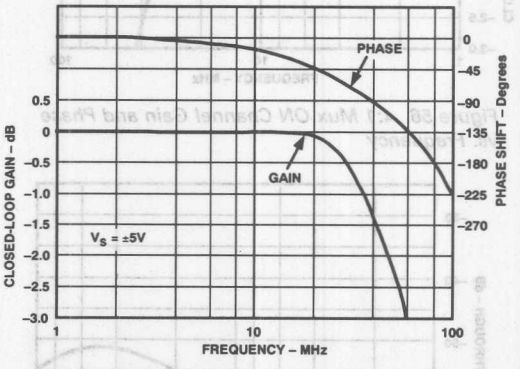


Figure 55. 2:1 Mux ON Channel Gain and Phase vs. Frequency

9

N:1 MULTIPLEXER

A multiplexer of arbitrary size can be formed by combining the desired number of AD810s together with the appropriate selection logic. The schematic in Figure 58 shows a recommendation for a 4:1 mux which may be useful for driving a high impedance such as the input to a video A/D converter (such as the AD773). The output series resistors effectively compensate for the combined output capacitance of the OFF channels plus the input capacitance of the A/D while maintaining wide bandwidth. In the case illustrated, the −0.1 dB bandwidth is about 20 MHz with no peaking. Switching time and OFF channel isolation (for the 4:1 mux) are about 250 ns and 60 dB at 10 MHz, respectively.

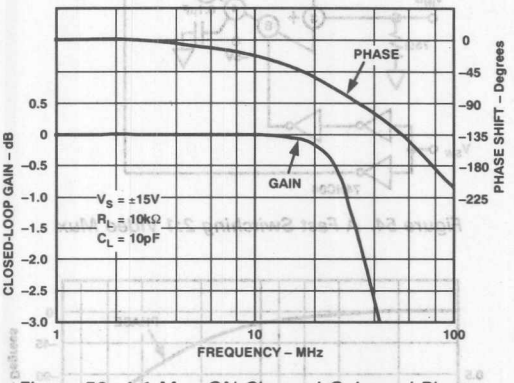


Figure 56. 4:1 Mux ON Channel Gain and Phase vs. Frequency

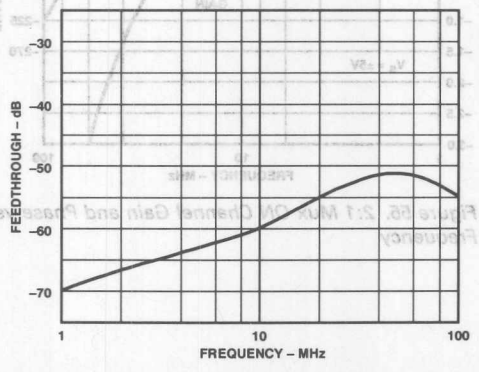


Figure 57. 4:1 Mux OFF Channel Feedthrough vs. Frequency

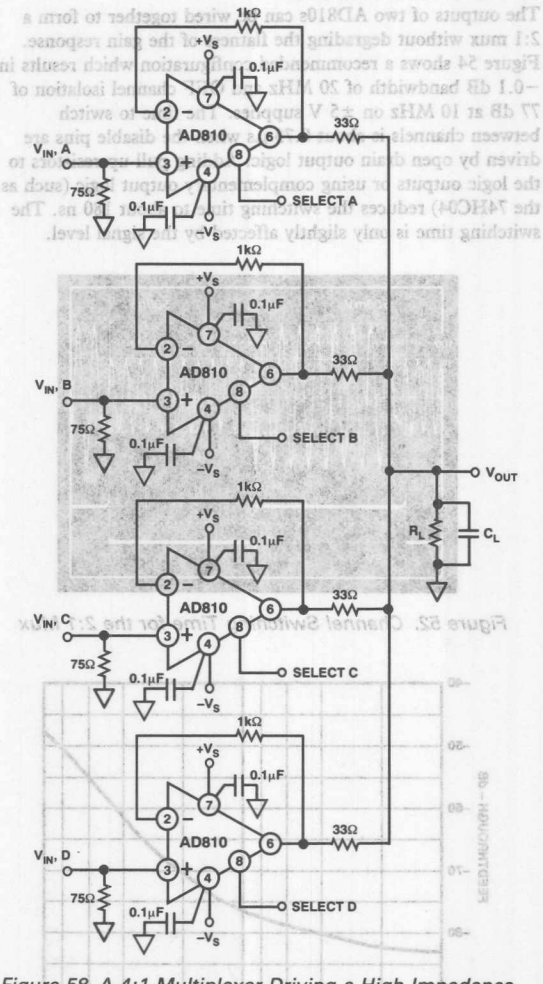


Figure 58. A 4:1 Multiplexer Driving a High Impedance

ANALOG DEVICES

High Performance Video Op Amp

AD811

FEATURES

High Speed
- 140 MHz Bandwidth (3 dB, G = +1)
- 120 MHz Bandwidth (3 dB, G = +2)
- 35 MHz Bandwidth (0.1 dB, G = +2)
- 2500 V/μs Slew Rate
- 25 ns Settling Time to 0.1% (For a 2 V Step)
- 65 ns Settling Time to 0.01% (For a 10 V Step)

Excellent Video Performance (R_L = 150 Ω)
- 0.01% Differential Gain, 0.01° Differential Phase
- Voltage Noise of 1.9 nV/√Hz

Low Distortion: THD = −74 dB @ 10 MHz

Excellent DC Precision
- 3 mV max Input Offset Voltage

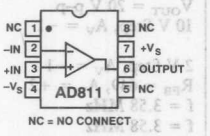
Flexible Operation
- Specified for ±5 V and ±15 V Operation
- ±2.3 V Output Swing into a 75 Ω Load (V_S = ±5 V)

APPLICATIONS

- Video Crosspoint Switchers, Multimedia Broadcast Systems
- HDTV Compatible Systems
- Video Line Drivers, Distribution Amplifiers
- ADC/DAC Buffers
- DC Restoration Circuits
- Medical—Ultrasound, PET, Gamma & Counter Applications

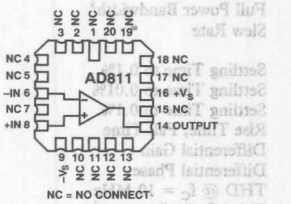
CONNECTION DIAGRAMS

8-Pin Plastic (N-8), Cerdip (Q-8) and SOIC (R-8) Packages



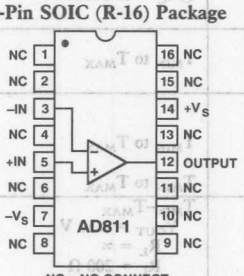
NC = NO CONNECT

20-Pin LCC (E-20A) Package



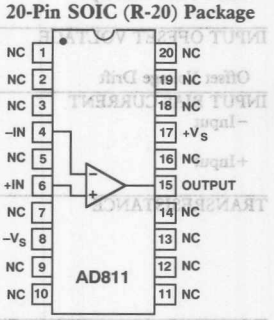
NC = NO CONNECT

16-Pin SOIC (R-16) Package



NC = NO CONNECT

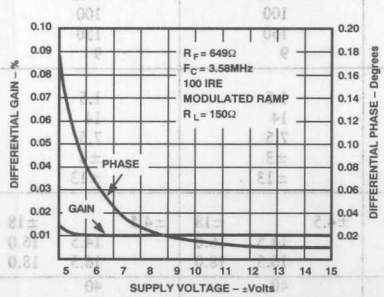
20-Pin SOIC (R-20) Package



NC = NO CONNECT

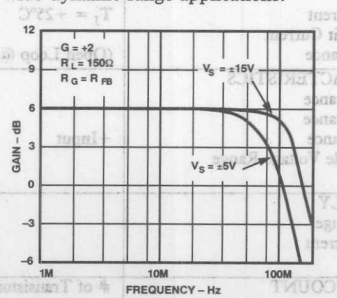
PRODUCT DESCRIPTION

The AD811 is a wideband current-feedback operational amplifier, optimized for broadcast quality video systems. The −3 dB bandwidth of 120 MHz at a gain of +2 and differential gain and phase of 0.01% and 0.01° (R_L = 150 Ω) make the AD811 an excellent choice for all video systems. The AD811 is designed to meet a stringent 0.1 dB gain flatness specification to a bandwidth of 35 MHz (G = +2) in addition to the low differential gain and phase errors. This performance is achieved whether driving one or two back terminated 75 Ω cables, with a low power supply current of 16.5 mA. Furthermore, the AD811 is specified over a power supply range of ±4.5 V to ±18 V.



The AD811 is also excellent for pulsed applications where transient response is critical. It can achieve a maximum slew rate of greater than 2500 V/μs with a settling time of less than 25 ns to 0.1% on a 2 volt step and 65 ns to 0.01% on a 10 volt step.

The AD811 is ideal as an ADC or DAC buffer in data acquisition systems due to its low distortion up to 10 MHz and its wide unity gain bandwidth. Because the AD811 is a current feedback amplifier, this bandwidth can be maintained over a wide range of gains. The AD811 also offers low voltage and current noise of 1.9 nV/√Hz and 20 pA/√Hz, respectively, and excellent dc accuracy for wide dynamic range applications.



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD811—SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, R_{LOAD} = 150 Ω unless otherwise noted)

Model	Conditions	V_S	AD811J/A[1] Min	AD811J/A[1] Typ	AD811J/A[1] Max	AD811S[2] Min	AD811S[2] Typ	AD811S[2] Max	Units
DYNAMIC PERFORMANCE									
Small Signal Bandwidth (No Peaking)									
−3 dB									
G = +1	R_{FB} = 562 Ω	±15 V		140			140		MHz
G = +2	R_{FB} = 649 Ω	±15 V		120			120		MHz
G = +2	R_{FB} = 562 Ω	±5 V		80			80		MHz
G = +10	R_{FB} = 511 Ω	±15 V		100			100		MHz
0.1 dB Flat									
G = +2	R_{FB} = 562 Ω	±5 V		25			25		MHz
	R_{FB} = 649 Ω	±15 V		35			35		MHz
Full Power Bandwidth[3]	V_{OUT} = 20 V p-p	±15 V		40			40		MHz
Slew Rate	V_{OUT} = 4 V p-p	±5 V		400			400		V/μs
	V_{OUT} = 20 V p-p	±15 V		2500			2500		V/μs
Settling Time to 0.1%	10 V Step, A_V = −1	±15 V		50			50		ns
Settling Time to 0.01%				65			65		ns
Settling Time to 0.1%	2 V Step, A_V = −1	±5 V		25			25		ns
Rise Time, Fall Time	R_{FB} = 649, A_V = +2	±15 V		3.5			3.5		ns
Differential Gain	f = 3.58 MHz	±15 V		0.01			0.01		%
Differential Phase	f = 3.58 MHz	±15 V		0.01			0.01		Degree
THD @ f_C = 10 MHz	V_{OUT} = 2 V p-p, A_V = +2	±15 V		−74			−74		dBc
Third Order Intercept[4]	@ f_C = 10 MHz	±5 V		36			36		dBm
		±15 V		43			43		dBm
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.5	3		0.5	3	mV
	T_{MIN} to T_{MAX}				5			5	mV
Offset Voltage Drift				5			5		μV/°C
INPUT BIAS CURRENT									
−Input		±5 V, ±15 V		2	5		2	5	μA
	T_{MIN} to T_{MAX}				15			30	μA
+Input		±5 V, ±15 V		2	10		2	10	μA
	T_{MIN} to T_{MAX}				20			25	μA
TRANSRESISTANCE	T_{MIN}–T_{MAX}								
	V_{OUT} = ±10 V								
	R_L = ∞	±15 V	0.75	1.5		0.75	1.5		MΩ
	R_L = 200 Ω	±15 V	0.5	0.75		0.5	0.75		MΩ
	V_{OUT} = ±2.5 V								
	R_L = 150 Ω	±5 V	0.25	0.4		0.125	0.4		MΩ
COMMON-MODE REJECTION									
V_{OS} (vs. Common Mode)									
T_{MIN}–T_{MAX}	V_{CM} = ±2.5	±5 V	56	60		50	60		dB
T_{MIN}–T_{MAX}	V_{CM} = ±10 V	±15 V	60	66		56	66		dB
Input Current (vs. Common Mode)	T_{MIN}–T_{MAX}			1	3		1	3	μA/V
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V								
V_{OS}	T_{MIN}–T_{MAX}		60	70		60	70		dB
+Input Current	T_{MIN}–T_{MAX}			0.3	2		0.3	2	μA/V
−Input Current	T_{MIN}–T_{MAX}			0.4	2		0.4	2	μA/V
INPUT VOLTAGE NOISE	f = 1 kHz			1.9			1.9		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz			20			20		pA/√Hz
OUTPUT CHARACTERISTICS									
Voltage Swing, Useful Operating Range[5]		±5 V		±2.9			±2.9		V
		±15 V		±12			±12		V
Output Current	T_J = +25°C			100			100		mA
Short-Circuit Current				150			150		mA
Output Resistance	(Open Loop @ 5 MHz)			9			9		Ω
INPUT CHARACTERISTICS									
+Input Resistance				1.5			1.5		MΩ
−Input Resistance				14			14		Ω
Input Capacitance	+Input			7.5			7.5		pF
Common-Mode Voltage Range		±5 V		±3			±3		V
		±15 V		±13			±13		V
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		14.5	16.0		14.5	16.0	mA
		±15 V		16.5	18.0		16.5	18.0	mA
TRANSISTOR COUNT	# of Transistors			40			40		

NOTES
[1]The AD811JR is specified with ±5 V power supplies only, with operation up to ±12 volts.
[2]See Analog Devices' military data sheet for 883B tested specifications.
[3]FPBW = slew rate/(2 π V_{PEAK})
[4]Output power level, tested at a closed loop gain of two.
[5]Useful operating range is defined as the output voltage at which linearity begins to degrade.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
AD811JR Grade Only	±12 V
Internal Power Dissipation[2]	Observe Derating Curves
Output Short Circuit Duration	Observe Derating Curves
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	±6 V
Storage Temperature Range (Q, E)	−65°C to +150°C
Storage Temperature Range (N, R)	−65°C to +125°C
Operating Temperature Range	
AD811J	0°C to +70°C
AD811A	−40°C to +85°C
AD811S	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	+300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]8-Pin Plastic Package: θ_{JA} = 90°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt
16-Pin SOIC Package: θ_{JA} = 85°C/Watt
20-Pin SOIC Package: θ_{JA} = 80°C/Watt
20-Pin LCC Package: θ_{JA} = 70°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package*
AD811AN	−40°C to +85°C	N-8
AD811AR-16	−40°C to +85°C	R-16
AD811AR-20	−40°C to +85°C	R-20
AD811JR	0°C to +70°C	R-8
AD811SQ/883B	−55°C to +125°C	Q-8
5962-9313001MPA	−55°C to +125°C	Q-8
AD811SE/883B	−55°C to +125°C	E-20A
5962-9313001M2A	−55°C to +125°C	E-20A
AD811ACHIPS	−40°C to +85°C	Die
AD811SCHIPS	−55°C to +125°C	Die

*E = Ceramic Leadless Chip Carrier; N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD811 is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 145°C. For the cerdip and LCC packages, the maximum junction temperature is 175°C. If these maximums are exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the "overheated" condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves in Figures 17 and 18.

While the AD811 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. One important example is when the amplifier is driving a reverse terminated 75 Ω cable and the cable's far end is shorted to a power supply. With power supplies of ±12 volts (or less) at an ambient temperature of +25°C or less, if the cable is shorted to a supply rail, then the amplifier will not be destroyed, even if this condition persists for an extended period.

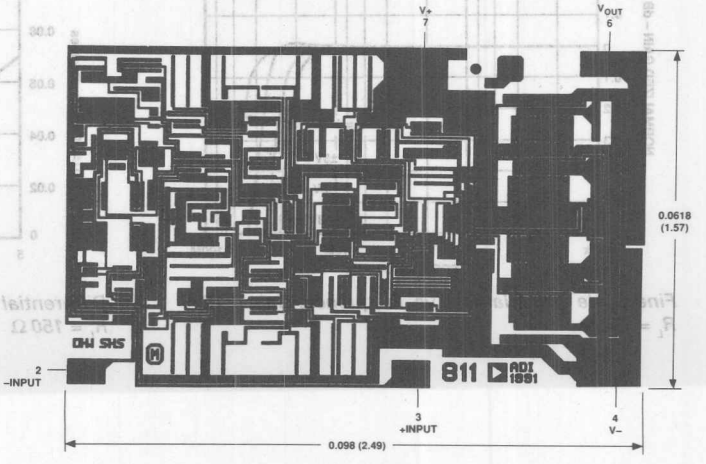
ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD811 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

9

METALIZATION PHOTOGRAPH

Contact Factory for Latest Dimensions.
Dimensions Shown in Inches and (mm).



FEATURES

Two Video Amplifiers in One 8-Pin SOIC Package
Optimized for Driving Cables in Video Systems
Excellent Video Specifications (R_L = 150 Ω):
- **Gain Flatness 0.1 dB to 40 MHz**
- **0.02% Differential Gain Error**
- **0.02° Differential Phase Error**

Low Power
- **Operates on Single +3 V Supply**
- **5.5 mA/Amplifier Max Power Supply Current**

High Speed
- **145 MHz Unity Gain Bandwidth (3 dB)**
- **1600 V/μs Slew Rate**

Easy to Use
- **50 mA Output Current**
- **Output Swing to 1 V of Rails (150 Ω Load)**

APPLICATIONS

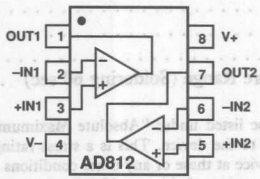
Video Line Driver
Professional Cameras
Video Switchers
Special Effects

PRODUCT DESCRIPTION

The AD812 is a low power, single supply, dual video amplifier. Each of the amplifiers have 50 mA of output current and are optimized for driving one back terminated video load (150 Ω) each. Each amplifier is a current feedback amplifier and features gain flatness of 0.1 dB to 40 MHz while offering differential gain and phase error of 0.02% and 0.02°. This makes the AD812 ideal for professional video electronics such as cameras and video switchers.

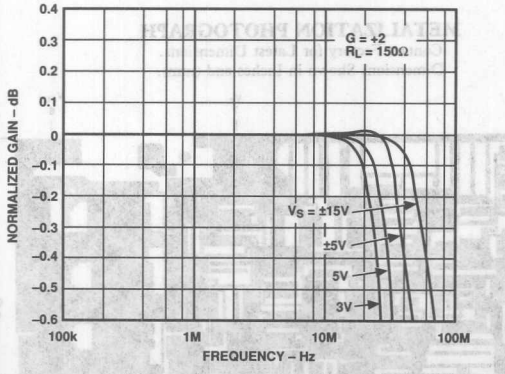
PIN CONFIGURATION

8-Pin Plastic Mini-DIP & SOIC

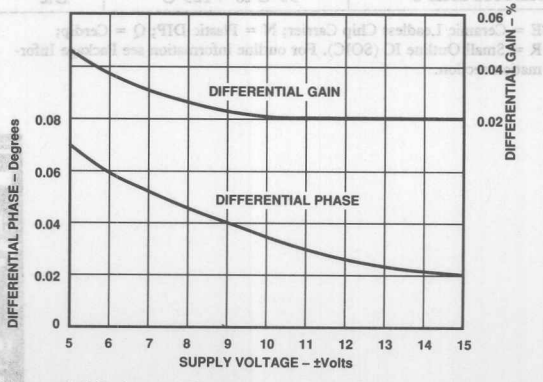


The AD812 offers low power of 4.0 mA per amplifier max (V_S = +5 V) and can run on a single +3 V power supply. The outputs of each amplifier swing to within one volt of either supply rail to easily accommodate video signals of 1 Vp-p. Also, at gains of +2 the AD812 can swing 3 V p-p on a single +5 V power supply. All this is offered in a small 8-pin plastic DIP or 8-pin SOIC package. These features make this dual amplifier ideal for portable and battery powered applications where size and power is critical.

The outstanding bandwidth of 145 MHz along with 1600 V/μs of slew rate make the AD812 useful in many general purpose high speed applications where a single +5 V or dual power supplies up to ±15 V are available. The AD812 is available in the industrial temperature range of –40°C to +85°C.



Fine-Scale Gain Flatness vs. Frequency, Gain = +2, R_L = 150 Ω



Differential Gain and Phase vs. Supply Voltage, Gain = +2, R_L = 150 Ω

SPECIFICATIONS

Dual Supply (@ T_A = +25°C, R_L = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD812A Min	AD812A Typ	AD812A Max	Units
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	G = +2, No Peaking	±5 V	50	65		MHz
		±15 V	75	100		MHz
	Gain = +1	±15 V	100	145		MHz
Bandwidth for 0.1 dB Flatness	G = +2	±5 V	20	30		MHz
		±15 V	25	40		MHz
Slew Rate[1]	G = +2, R_L = 1 kΩ	±5 V	275	425		V/µs
	20 V Step	±15 V	1400	1600		V/µs
	G = –1, R_L = 1 kΩ	±5 V		250		V/µs
		±15 V		600		V/µs
Settling Time to 0.1%	G = –1, R_L = 1 kΩ					
	V_O = 3 V Step	±5 V		50		ns
	V_O = 10 V Step	±15 V		40		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	f_C = 1 MHz, R_L = 1 kΩ	±15 V		–90		dBc
Input Voltage Noise	f = 10 kHz	±5 V, ±15 V		3.5		nV/√Hz
Input Current Noise	f = 10 kHz, +In	±5 V, ±15 V		1.5		pA/√Hz
	f = 10 kHz, –In	±5 V, ±15 V		18		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω	±5 V		0.05	0.1	%
		±15 V		0.02	0.06	%
Differential Phase Error		±5 V		0.07	0.15	Degrees
		±15 V		0.02	0.06	Degrees
DC PERFORMANCE						
Input Offset Voltage		±5 V, ±15 V		2	5	mV
	T_{MIN} – T_{MAX}				12	mV
Offset Drift		±5 V, ±15 V		15		µV/°C
–Input Bias Current		±5 V, ±15 V		7	20	µA
	T_{MIN} – T_{MAX}				38	µA
+Input Bias Current		±5 V, ±15 V		0.3	1.0	µA
	T_{MIN} – T_{MAX}				1.0	µA
Open-Loop Voltage Gain	V_O = ±2.5 V, R_L = 150 Ω	±5 V	70	76		dB
	T_{MIN} – T_{MAX}		69			dB
	V_O = ±10 V, R_L = 1 kΩ	±15 V	78	82		dB
	T_{MIN} – T_{MAX}		75			dB
Open-Loop Transresistance	V_O = ±2.5 V, R_L = 150 Ω	±5 V	350	550		kΩ
	T_{MIN} – T_{MAX}		270			kΩ
	V_O = ±10 V, R_L = 1 kΩ	±15 V	500	800		kΩ
	T_{MIN} – T_{MAX}		370			kΩ
INPUT CHARACTERISTICS						
Input Resistance	+Input	±15 V		15		MΩ
	–Input			65		Ω
Input Capacitance	+Input			1.7		pF
Input Common-Mode		±5 V		4.0		±V
Voltage Range		±15 V		13.5		±V
Common Mode Rejection Ratio						
Input Offset Voltage	V_{CM} = ±2.5 V	±5 V	54	58		dB
–Input Current				2	3.0	µA/V
+Input Current				0.07	0.15	µA/V
Input Offset Voltage	V_{CM} = ±12 V	±15 V	56	60		dB
–Input Current				1.5	3.0	µA/V
+Input Current				0.05	0.1	µA/V

AD812—SPECIFICATIONS

Dual Supply (Continued)

Model	Conditions	V_S	AD812A Min	AD812A Typ	AD812A Max	Units
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 150 Ω, T_{MIN} – T_{MAX}	±5 V	3.5	3.8		±V
	R_L = 1 kΩ, T_{MIN} – T_{MAX}	±15 V	13.6	14.0		±V
Output Current		±5 V	30	40		mA
		±15 V	40	50		mA
Short Circuit Current	G = +2, R_F = 715 Ω	±15 V		100		mA
	V_{IN} = 2 V					
Output Resistance	Open-Loop	±15 V		15		Ω
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz	±5 V, ±15 V		–75		dB
Gain Flatness Match	G = +2, f = 40 MHz	±15 V		0.1		dB
DC						
Input offset Voltage	T_{MIN} – T_{MAX}	±5 V, ±15 V		0.5	3.6	mV
–Input Bias Current	T_{MIN} – T_{MAX}	±5 V, ±15 V		2	16	µA
POWER SUPPLY						
Operating Range			±1.2		±18	V
Quiescent Current	Per Amplifier	±5 V		3.5	4.0	mA
		±15 V		4.5	5.5	mA
	T_{MIN} – T_{MAX}	±15 V			6.0	mA
Power Supply Rejection Ratio						
Input Offset Voltage	V_S = ±1.5 V to ±15 V		72	80		dB
–Input Current				0.3	0.6	µA/V
+Input Current				0.005	0.05	µA/V

Single Supply (@ T_A = +25°C, R_L = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD812A Min	AD812A Typ	AD812A Max	Units
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	G = +2, No Peaking	+5 V	35	50		MHz
		+3 V	30	40		MHz
Bandwidth for 0.1 dB Flatness	G = +2	+5 V	13	20		MHz
		+3 V	10	18		MHz
Slew Rate[1]	G = +2, R_L = 1 kΩ	+5 V		125		V/µs
		+3 V		60		V/µs
NOISE/HARMONIC PERFORMANCE						
Input Voltage Noise	f = 10 kHz	+5 V, +3 V		3.5		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz, +In	+5 V, +3 V		1.5		$pA/\sqrt{Hz}$
	f = 10 kHz, –In	+5 V, +3 V		18		$pA/\sqrt{Hz}$
Differential Gain Error[2]	NTSC, G = +2, R_L = 150 Ω	+5 V		0.07		%
	G = +1	+3 V		0.15		%
Differential Phase Error[2]	G = +2	+5 V		0.06		Degrees
	G = +1	+3 V		0.15		Degrees
DC PERFORMANCE						
Input Offset Voltage		+5 V, +3 V		1.5	3	mV
	$T_{MIN} - T_{MAX}$				4.5	mV
Offset Drift		+5 V, +3 V		7		µV/°C
–Input Bias Current		+5 V, +3 V		2	10	µA
	$T_{MIN} - T_{MAX}$				12	µA
+Input Bias Current		+5 V, +3 V		0.2	1.0	µA
	$T_{MIN} - T_{MAX}$				1.0	µA
Open-Loop Voltage Gain	V_O = +2.5 V p-p	+5 V	69	73		dB
	V_O = +0.7 V p-p	+3 V		70		dB
Open-Loop Transresistance	V_O = +2.5 V p-p	+5 V	250	400		kΩ
	V_O = +0.7 V p-p	+3 V		300		kΩ
INPUT CHARACTERISTICS						
Input Resistance	+Input	+5 V		15		MΩ
	–Input	+5 V		90		Ω
Input Capacitance	+Input			2		pF
Input Common-Mode Voltage Range		+5 V	1.0		4.0	V
		+3 V	1.0		2.0	V
Common-Mode Rejection Ratio						
Input Offset Voltage	V_{CM} = 1.25 V to 3.75 V	+5 V	52	55		dB
–Input Current				3	5	µA/V
+Input Current				0.1	0.2	µA/V
Input Offset Voltage	V_{CM} = 1 V to 2 V	+3 V		52		dB
–Input Current				3.5		µA/V
+Input Current				0.1		µA/V

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AD812—SPECIFICATIONS

Single Supply (Continued)

Model	Conditions	V_S	AD812A Min	AD812A Typ	AD812A Max	Units
OUTPUT CHARACTERISTICS						
Output Voltage Swing p-p	R_L = 1 kΩ, T_{MIN} – T_{MAX}	+5 V	3.0	3.2		V p-p
	R_L = 150 Ω, T_{MIN} – T_{MAX}	+5 V	2.8	3.1		V p-p
		+3 V	1.0	1.3		V p-p
Output Current		+5 V	20	30		mA
		+3 V	15	25		mA
Short Circuit Current	G = +2, R_F = 715 Ω V_{IN} = 1 V	+5 V		40		mA
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz	+5 V, +3 V		–72		dB
Gain Flatness Match	G = +2, f = 20 MHz	+5 V, +3 V		0.1		dB
DC						
Input offset Voltage	T_{MIN} – T_{MAX}	+5 V, +3 V		0.5	2.8	mV
–Input Bias Current	T_{MIN} – T_{MAX}	+5 V, +3 V		2	11	µA
POWER SUPPLY						
Operating Range			2.4		36	V
Quiescent Current	Per Amplifier	+5 V		3.2	4.0	mA
		+3 V		3.0	3.5	mA
	T_{MIN} – T_{MAX}	+5 V			4.5	mA
Power Supply Rejection Ratio						
Input Offset Voltage	V_S = +3 V to +30 V		72	80		dB
–Input Current				0.3	0.6	µA/V
+Input Current				0.005	0.05	µA/V
TRANSISTOR COUNT				56		

NOTES
[1]Slew rate measurement is based on 10% to 90% rise time in the specified closed-loop gain.
[2]Single supply differential gain and phase are measured with the ac coupled circuit of Figure 50.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.3 Watts
Small Outline (R) . . . . . 0.9 Watts
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±1.2 V
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range N, R . . . . . –65°C to +125°C
Operating Temperature Range . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 seconds) . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air: 8-Pin Plastic Package: θ_{JA} = 90°C/Watt; 8-Pin SOIC Package: θ_{JA} = 140°C/Watt.

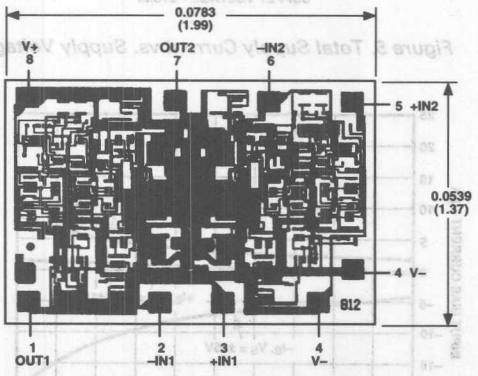
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD812AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD812AR-8	–40°C to +85°C	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.

METALIZATION PHOTO

Dimensions shown in inches and (mm).

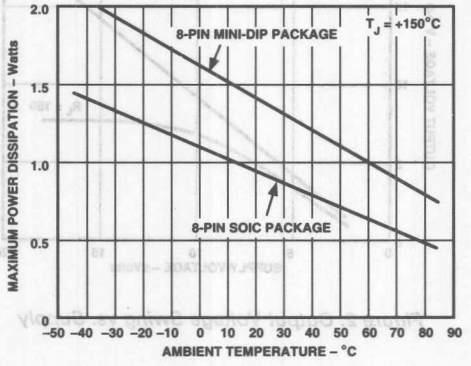


MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD812 is limited by the associated rise in junction temperature. The maximum safe junction temperature for the plastic encapsulated parts is determined by the glass transition temperature of the plastic, about 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD812 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150 degrees) is not exceeded under all conditions. To ensure proper operation, it is important to observe the derating curves.

It must also be noted that in high (noninverting) gain configurations (with low values of gain resistor), a high level of input overdrive can result in a large input error current, which may result in a significant power dissipation in the input stage. This power must be included when computing the junction temperature rise due to total internal power.



Plot of Maximum Power Dissipation vs. Temperature

9

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD812 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

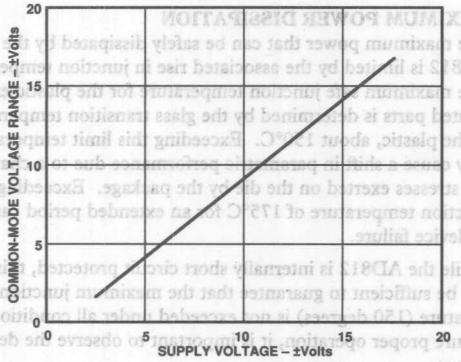


Figure 1. Input Common-Mode Voltage Range vs. Supply Voltage

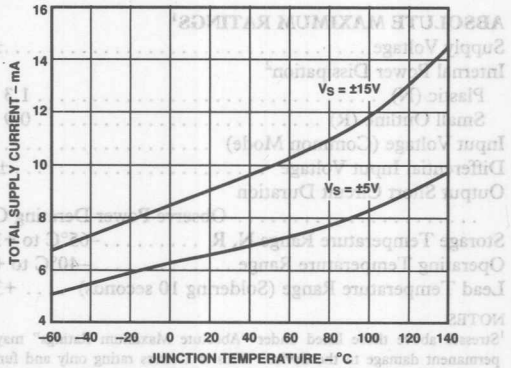


Figure 4. Total Supply Current vs. Junction Temperature

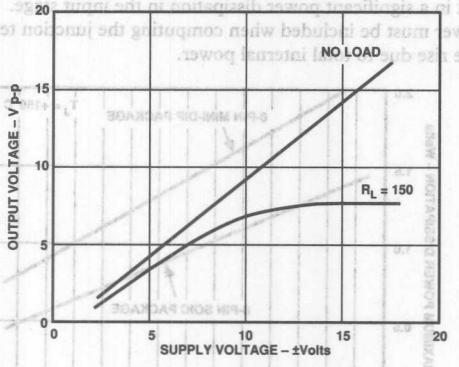


Figure 2. Output Voltage Swing vs. Supply

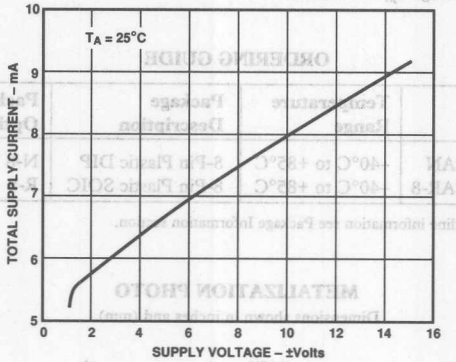


Figure 5. Total Supply Current vs. Supply Voltage

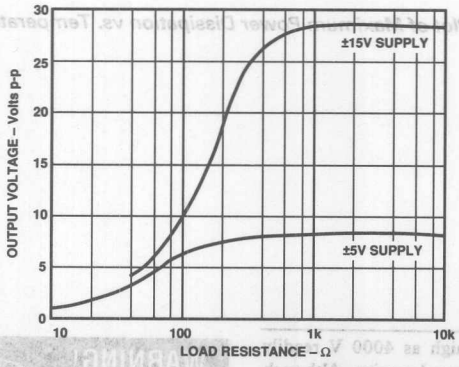


Figure 3. Output Voltage Swing vs. Load Resistance

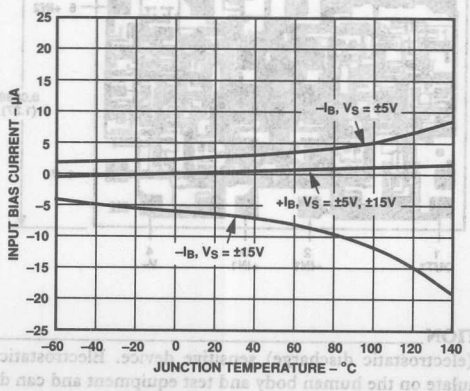


Figure 6. Input Bias Current vs. Junction Temperature

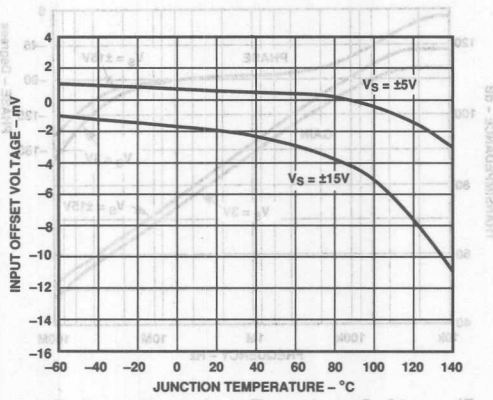


Figure 7. Input Offset Voltage vs. Junction Temperature

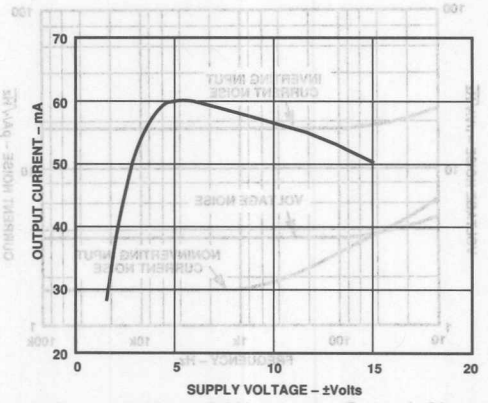


Figure 10. Linear Output Current vs. Supply Voltage

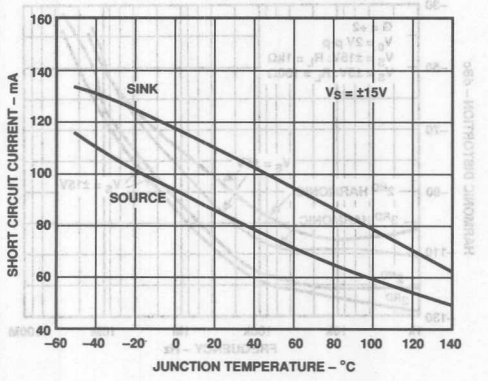


Figure 8. Short Circuit Current vs. Junction Temperature

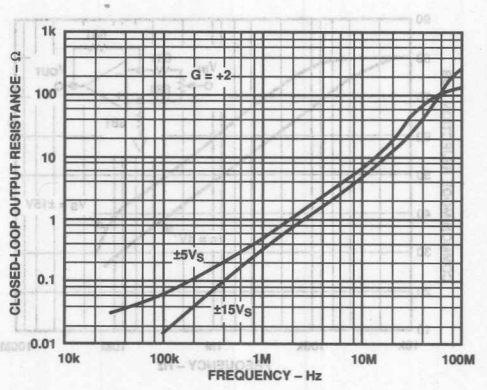


Figure 11. Closed-Loop Output Resistance vs. Frequency

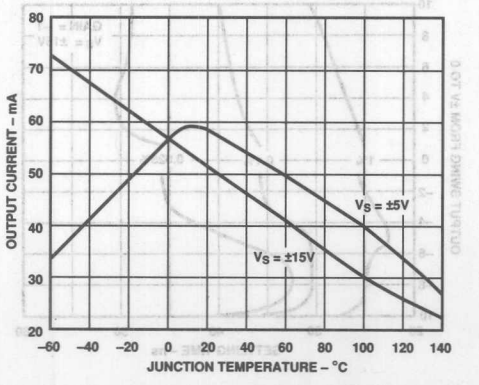


Figure 9. Linear Output Current vs. Junction Temperature

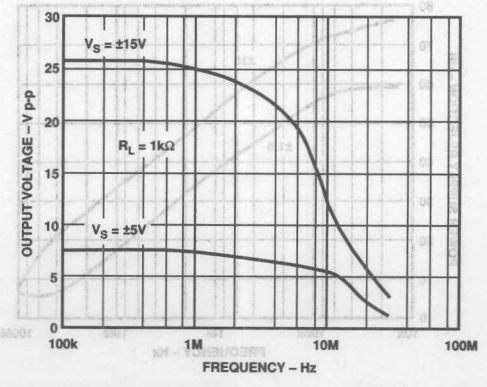


Figure 12. Large Signal Frequency Response

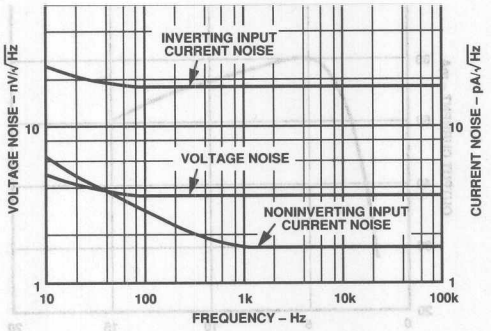


Figure 13. Input Current and Voltage Noise vs. Frequency

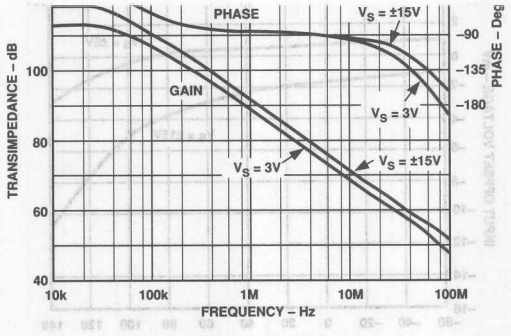


Figure 16. Open-Loop Transimpedance vs. Frequency (Relative to 1 Ω)

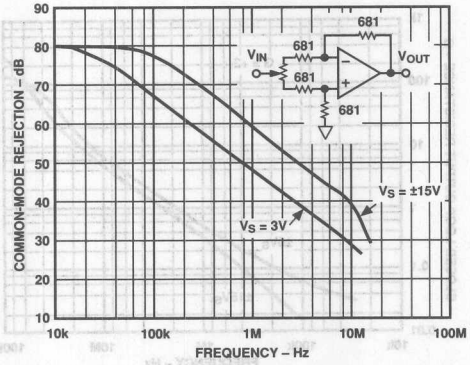


Figure 14. Common-Mode Rejection vs. Frequency

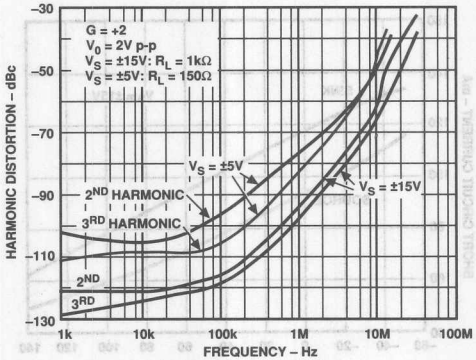


Figure 17. Harmonic Distortion vs. Frequency

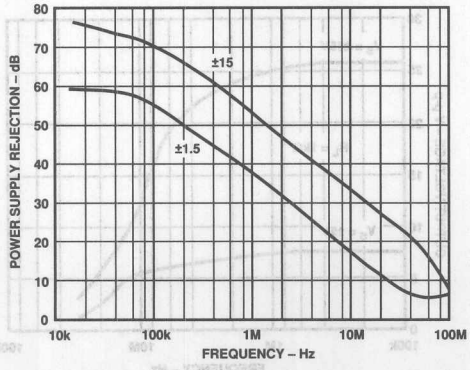


Figure 15. Power Supply Rejection vs. Frequency

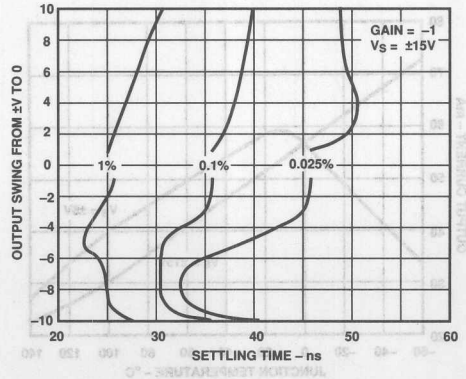


Figure 18. Output Swing and Error vs. Settling Time

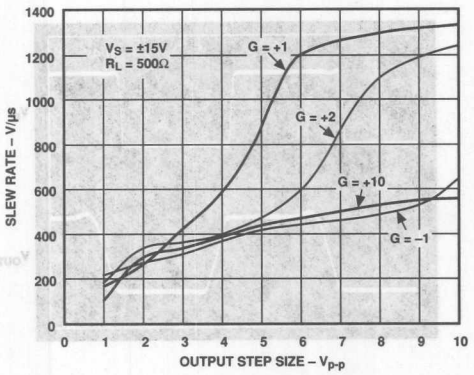


Figure 19. Slew Rate vs. Output Step Size

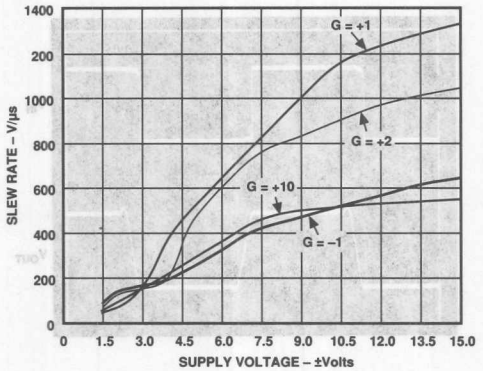


Figure 22. Maximum Slew Rate vs. Supply Voltage

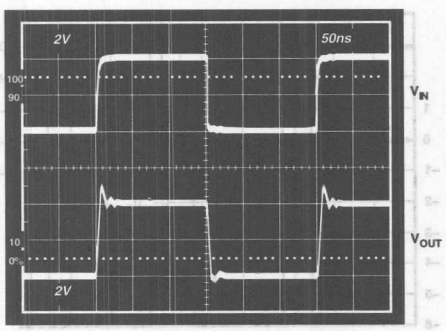


Figure 20. Large Signal Pulse Response, Gain = +1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

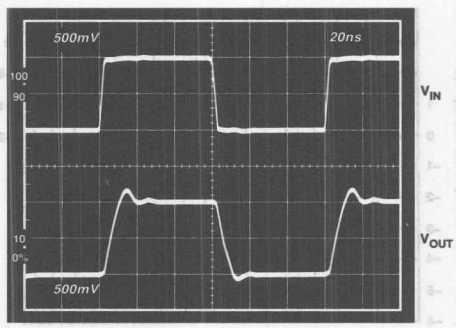


Figure 23. Small Signal Pulse Response, Gain = +1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

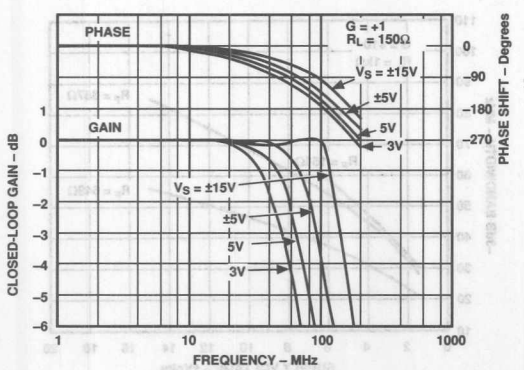


Figure 21. Closed-Loop Gain and Phase vs. Frequency, G = +1

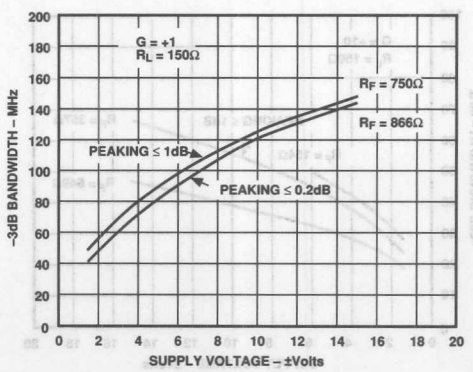


Figure 24. –3 dB Bandwidth vs. Supply Voltage, G = +1

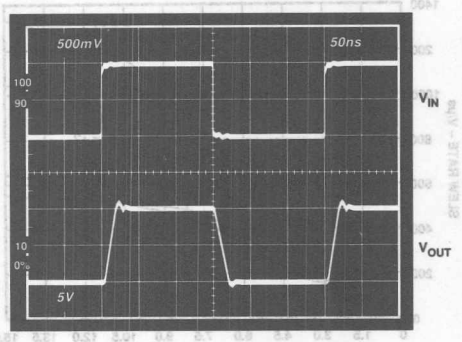


Figure 25. Large Signal Pulse Response, Gain = +10, (R_F = 357 Ω, R_L = 500 Ω, V_S = ±15 V)

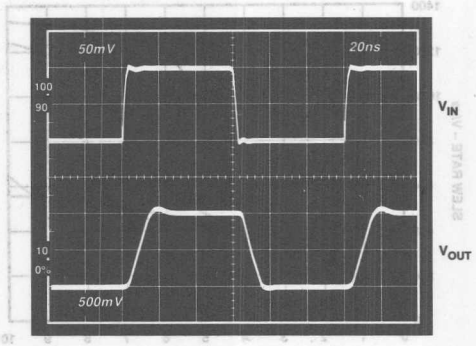


Figure 28. Small Signal Pulse Response, Gain = +10, (R_F = 357 Ω, R_L = 150 Ω, V_S = ±5 V)

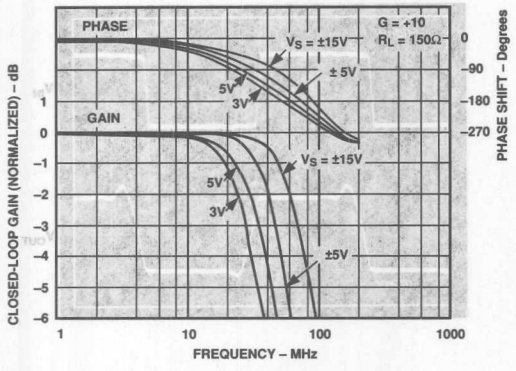


Figure 26. Closed-Loop Gain and Phase vs. Frequency, Gain = +10, R_L = 150 Ω

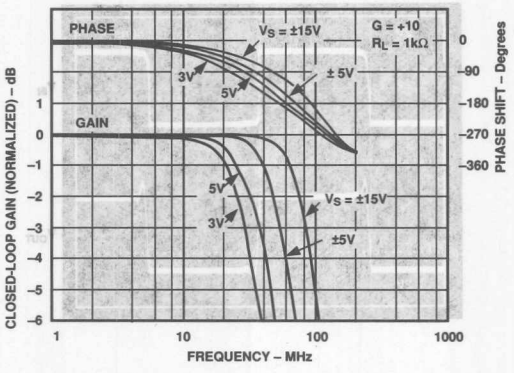


Figure 29. Closed-Loop Gain and Phase vs. Frequency, Gain = +10, R_L = 1 kΩ

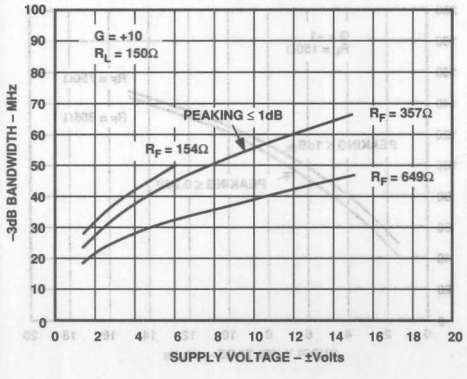


Figure 27. –3 dB Bandwidth vs. Supply Voltage, Gain = +10, R_L = 150 Ω

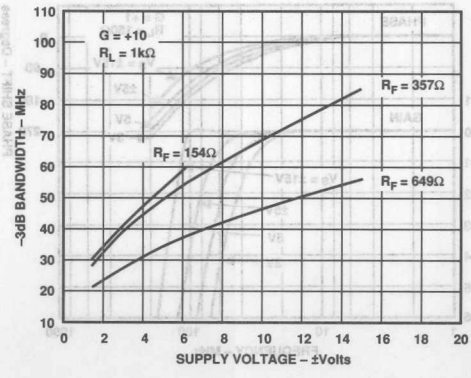


Figure 30. –3 dB Bandwidth vs. Supply Voltage, Gain = +10, R_L = 1 k Ω

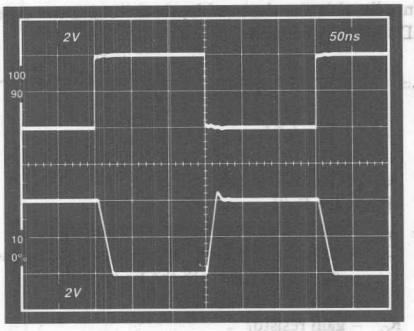


Figure 31. Large Signal Pulse Response, Gain = –1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

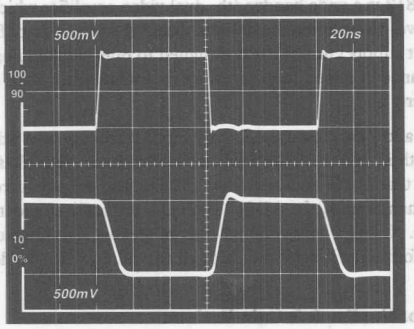


Figure 34. Small Signal Pulse Response, Gain = –1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

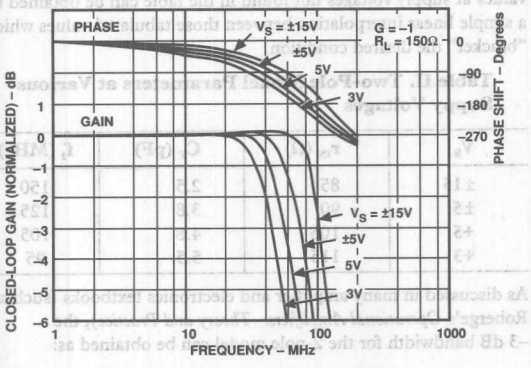


Figure 32. Closed-Loop Gain and Phase vs. Frequency, Gain = –1, R_L = 150 Ω

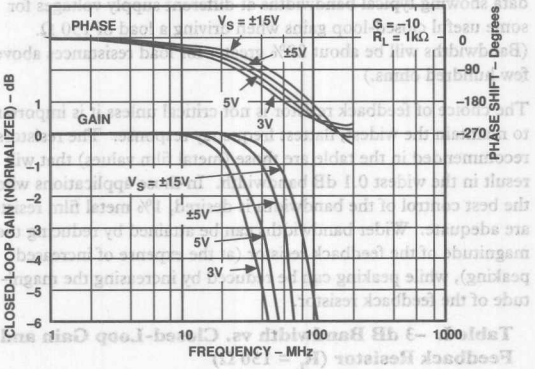


Figure 35. Closed-Loop Gain and Phase vs. Frequency, Gain = –10, R_L = 1 kΩ

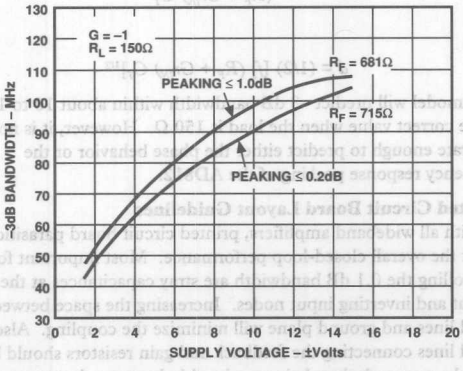


Figure 33. –3 dB Bandwidth vs. Supply Voltage, Gain = –1, R_L = 150 Ω

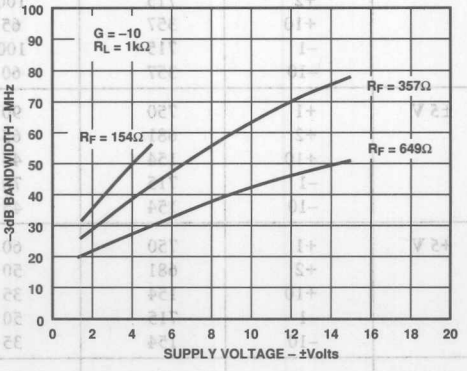


Figure 36. –3 dB Bandwidth vs. Supply Voltage, Gain = –10, R_L = 1 kΩ

General Considerations

The AD812 is a wide bandwidth, dual video amplifier which offers a high level of performance on less than 5.5 mA per amplifier of quiescent supply current. It is designed to offer outstanding performance at closed-loop inverting or noninverting gains of one or greater.

Built on a low cost, complementary bipolar process, and achieving bandwidth in excess of 100 MHz, differential gain and phase errors of better than 0.1% and 0.1° (into 150 Ω), and output current greater than 40 mA, the AD812 is an exceptionally efficient video amplifier. Using a conventional current feedback architecture, its high performance is achieved through careful attention to design details.

Choice of Feedback & Gain Resistors

Because it is a current feedback amplifier, the closed-loop bandwidth of the AD812 depends on the value of the feedback resistor. The bandwidth also depends on the supply voltage. In addition, attenuation of the open-loop response when driving load resistors less than about 250 Ω will affect the bandwidth. Table I contains data showing typical bandwidths at different supply voltages for some useful closed-loop gains when driving a load of 150 Ω. (Bandwidths will be about 20% greater for load resistances above a few hundred ohms.)

The choice of feedback resistor is not critical unless it is important to maintain the widest, flattest frequency response. The resistors recommended in the table are those (metal film values) that will result in the widest 0.1 dB bandwidth. In those applications where the best control of the bandwidth is desired, 1% metal film resistors are adequate. Wider bandwidths can be attained by reducing the magnitude of the feedback resistor (at the expense of increased peaking), while peaking can be reduced by increasing the magnitude of the feedback resistor.

Table I. –3 dB Bandwidth vs. Closed-Loop Gain and Feedback Resistor (R_L = 150 Ω)

V_S	Gain	R_F, Ω	BW, MHz
±15 V	+1	866	145
	+2	715	100
	+10	357	65
	–1	715	100
	–10	357	60
±5 V	+1	750	90
	+2	681	65
	+10	154	45
	–1	715	70
	–10	154	45
+5 V	+1	750	60
	+2	681	50
	+10	154	35
	–1	715	50
	–10	154	35
+3 V	+1	750	50
	+2	681	40
	+10	154	30
	–1	715	40
	–10	154	25

To estimate the –3 dB bandwidth for closed-loop gains or feedback resistors not listed in the above table, the following two pole model for the AD812 many be used:

$$A_{CL} = \frac{G}{S^2\left[\frac{(R_F + Gr_{IN})\,C_T}{2\pi f_2}\right] + S\,(R_F + Gr_{IN})\,C_T + 1}$$

where:
A_{CL} = closed-loop gain
$G = 1 + R_F/R_G$
r_{in} = input resistance of the inverting input
C_T = "transcapacitance," which forms the open-loop dominant pole with the tranresistance
R_F = feedback resistor
R_G = gain resistor
f_2 = frequency of second (non-dominant) pole
$S = 2\pi j f$

Appropriate values for the model parameters at different supply voltages are listed in Table II. Reasonable approximations for these values at supply voltages not found in the table can be obtained by a simple linear interpolation between those tabulated values which "bracket" the desired condition.

Table II. Two-Pole Model Parameters at Various Suppy Voltages

V_S	r_{IN} (Ω)	C_T (pF)	f_2 (MHz)
±15	85	2.5	150
±5	90	3.8	125
+5	105	4.8	105
+3	115	5.5	95

As discussed in many amplifier and electronics textbooks (such as Roberge's *Operational Amplifiers: Theory and Practice*), the –3 dB bandwidth for the 2-pole model can be obtained as:

$$f_3 = f_N\,[1 - 2d^2 + (2 - 4d^2 + 4d^4)^{1/2}]^{1/2}$$

where:

$$f_N = \left[\frac{f_2}{(R_F + Gr_{IN})\,C_T}\right]^{1/2}$$

and:

$$d = (1/2)\,[f_2\,(R_F + Gr_{IN})\,C_T]^{1/2}$$

This model will predict –3 dB bandwidth within about 10 to 15% of the correct value when the load is 150 Ω. However, it is not an accurate enough to predict either the phase behavior or the frequency response peaking of the AD812.

Printed Circuit Board Layout Guidelines

As with all wideband amplifiers, printed circuit board parasitics can affect the overall closed-loop performance. Most important for controlling the 0.1 dB bandwidth are stray capacitances at the output and inverting input nodes. Increasing the space between signal lines and ground plane will minimize the coupling. Also, signal lines connecting the feedback and gain resistors should be kept short enough that their associated inductance does not cause high frequency gain errors.

Power Supply Bypassing

Adequate power supply bypassing can be very important when optimizing the performance of high speed circuits. Inductance in the supply leads can (for example) contribute to resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to a load, then large (greater than 1 µF) bypass capacitors are required to produce the best settling time and lowest distortion. Although 0.1 µF capacitors may be adequate in some applications, more elaborate bypassing is required in other cases.

When multiple bypass capacitors are connected in parallel, it is important to be sure that the capacitors themselves do not form resonant circuits. A small (say 5 Ω) resistor may be required in series with one of the capacitors to minimize this possibility.

As discussed below, power supply bypassing can have a significant impact on crosstalk performance.

Achieving Low Crosstalk

Measured crosstalk from the output of amplifier 2 to the input of amplifier 1 of the AD812 is shown in Figure 37. The crosstalk from the output of amplifier 1 to the input of amplifier 2 is a few dB better than this due to the additional distance between critical signal nodes.

A carefully laid-out PC board should be able to achieve the level of crosstalk shown in the figure. The most significant contributors to difficulty in achieving low crosstalk are inadequate power supply bypassing, overlapped input and/or output signal paths, and capacitive coupling between critical nodes.

The bypass capacitors must be connected to the ground plane at a point close to and between the ground reference points for the two loads. (The bypass of the negative power supply is particularly important in this regard.) There are two amplifiers in the package, and low impedance signal return paths must be provided for each load. (Using a parallel combination of 1 µF, 0.1 µF, and 0.01 µF bypass capacitors will help to achieve optimal crosstalk.)

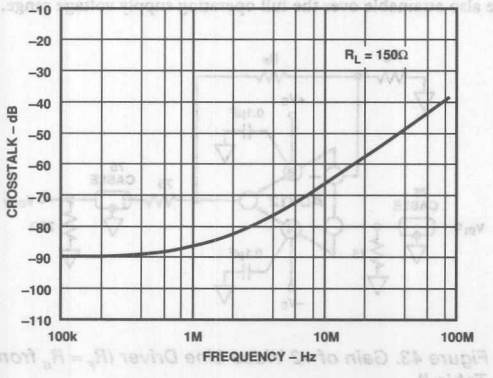


Figure 37. Crosstalk vs. Frequency

The input and output signal return paths must also be kept from overlapping. Since ground connections are not of perfectly zero impedance, current in one ground return path can produce a voltage drop in another ground return path if they are allowed to overlap.

Electric field coupling external to (and across) the package can be reduced by arranging for a narrow strip of ground plane to be run between the pins (parallel to the pin rows). Doing this on both sides of the board can reduce the high frequency crosstalk by about 5 dB or 6 dB.

Driving Capacitive Loads

When used with the appropriate output series resistor, any load capacitance can be driven without peaking or oscillation. In most cases, less than 50 Ω is all that is needed to achieve an extremely flat frequency response. As illustrated in Figure 41, the AD812 can be very attractive for driving largely capacitive loads. In this case, the AD812's high output short circuit current allows for a 150 V/µs slew rate when driving a 510 pF capacitor.

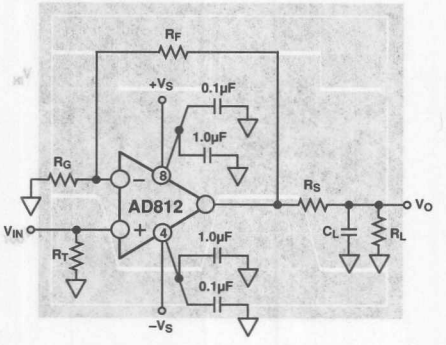


Figure 38. Circuit for Driving a Capacitive Load

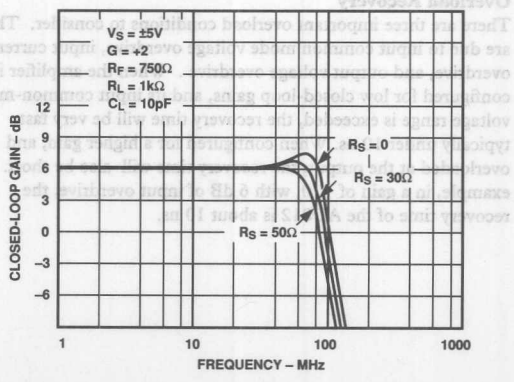


Figure 39. Response to a Small Load Capacitor at ±5 V

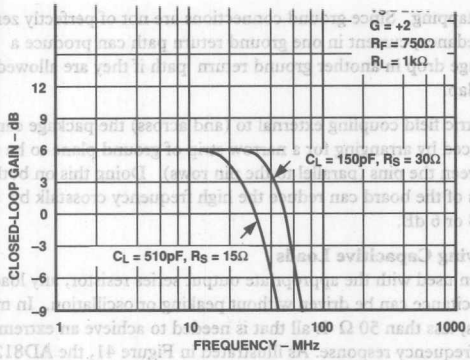


Figure 40. Response to Large Load Capacitor, $V_S = \pm 15$ V

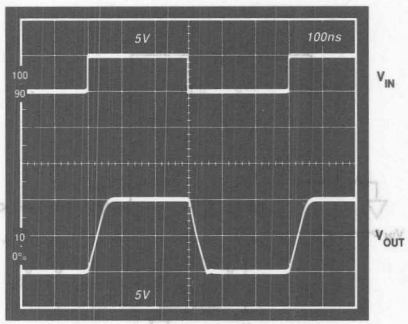


Figure 41. Pulse Response of Circuit of Figure 38 with C_L = 510 pF, R_L = 1 kΩ, $R_F = R_G$ = 715 Ω, R_S = 15 Ω

Overload Recovery

There are three important overload conditions to consider. They are due to input common mode voltage overdrive, input current overdrive, and output voltage overdrive . When the amplifier is configured for low closed-loop gains, and its input common-mode voltage range is exceeded, the recovery time will be very fast, typically under 10 ns. When configured for a higher gain, and overloaded at the output, the recovery time will also be short. For example, in a gain of +10, with 6 dB of input overdrive, the recovery time of the AD812 is about 10 ns.

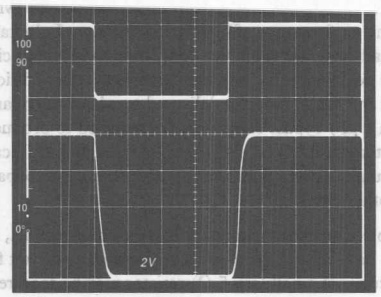


Figure 42. 6 dB Overload Recovery; G = 10, R_L = 500 Ω, $V_S = \pm 5$ V

In the case of high gains with very high levels of input overdrive, a longer recovery time may occur. For example, if the input common-mode voltage range is exceeded in a gain of +10, the recovery time will be on the order of 100 ns. This is primarily due to current overloading of the input stage.

As noted in the warning under "Maximum Power Dissipation", a high level of input overdrive in a high noninverting gain circuit can result in a large current flow in the input stage. For differential input voltages of less than about 1.25 V, this will be internally limited to less than 20 mA (decreasing with supply voltage). For input overdrives which result in higher differential input voltages, power dissipation in the input stage must be considered. It is recommended that external diode clamps be used in cases where the differential input voltage is expected to exceed 1.25 V.

High Performance Video Line Driver

At a gain of +2, the AD812 makes an excellent driver for a back terminated 75 Ω video line. Low differential gain and phase errors and wide 0.1 dB bandwidth can be realized over a wide range of power supply voltage. Outstanding gain and group delay matching are also attainable over the full operating supply voltage range.

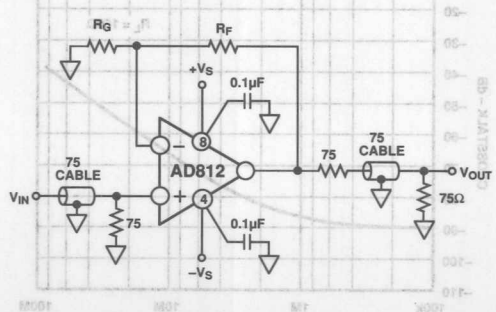


Figure 43. Gain of +2 Video Line Driver ($R_F = R_G$ from Table I)

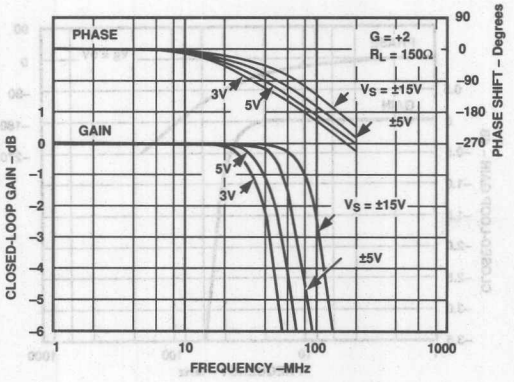


Figure 44. Closed-Loop Gain and Phase vs. Frequency for the Line Driver

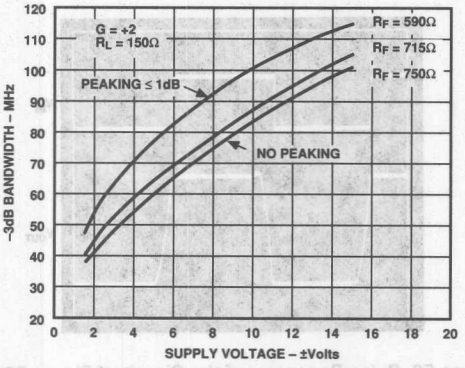


Figure 45. –3 dB Bandwidth vs. Supply Voltage, Gain = +2, R_L = 150 Ω

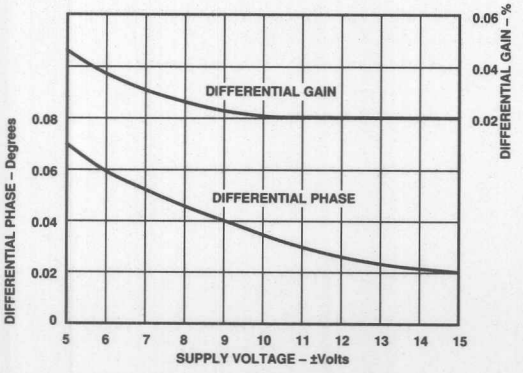


Figure 46. Differential Gain and Phase vs. Supply Voltage, Gain = +2, R_L = 150 Ω

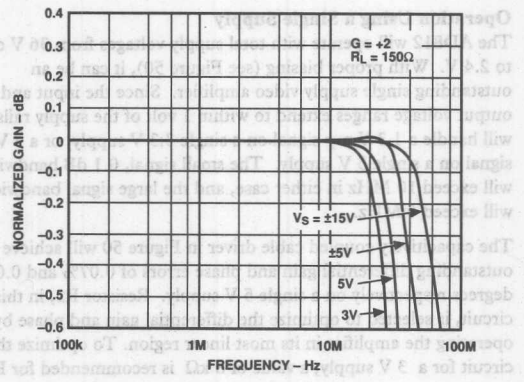


Figure 47. Fine-Scale Gain Flatness vs. Frequency, Gain = +2, R_L = 150 Ω

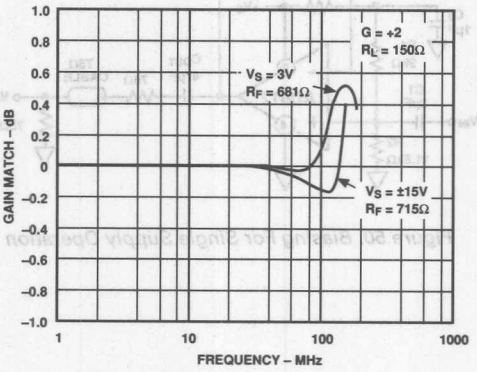


Figure 48. Closed-Loop Gain Matching vs. Frequency, Gain = +2, R_L = 150 Ω

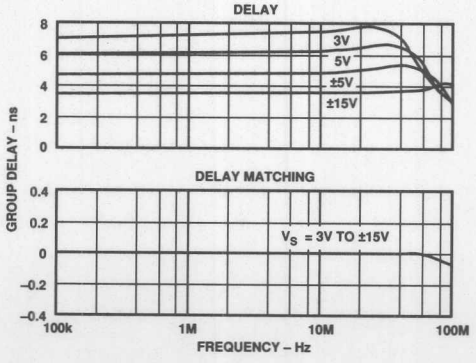


Figure 49. Group Delay and Group Delay Matching vs. Frequency, G = +2, R_L = 150 Ω

Operation Using a Single Supply

The AD812 will operate with total supply voltages from 36 V down to 2.4 V. With proper biasing (see Figure 50), it can be an outstanding single supply video amplifier. Since the input and output voltage ranges extend to within 1 volt of the supply rails, it will handle a 1.3 V p-p signal on a single 3.3 V supply, or a 3 V p-p signal on a single 5 V supply. The small signal, 0.1 dB bandwidths will exceed 10 MHz in either case, and the large signal bandwidths will exceed 6 MHz.

The capacitively coupled cable driver in Figure 50 will achieve outstanding differential gain and phase errors of 0.07% and 0.06 degrees respectively on a single 5 V supply. Resistor R2, in this circuit, is selected to optimize the differential gain and phase by operating the amplifier in its most linear region. To optimize the circuit for a 3 V supply, a value of 8 kΩ is recommended for R2.

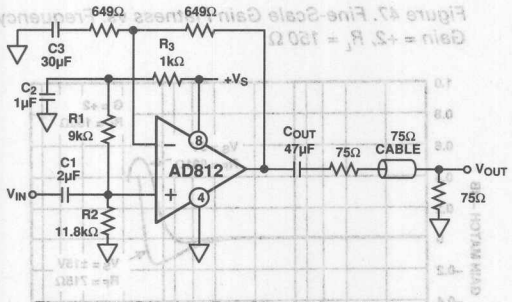


Figure 50. Biasing For Single Supply Operation

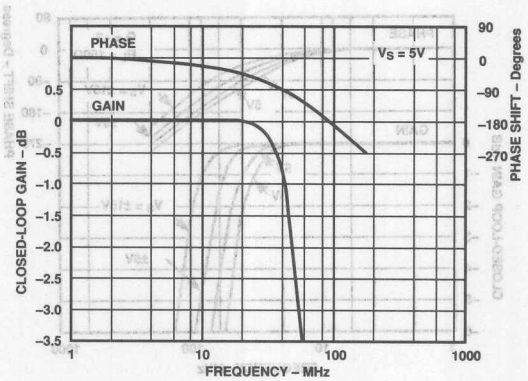


Figure 51. Closed-Loop Gain and Phase vs. Frequency, Circuit of Figure 50

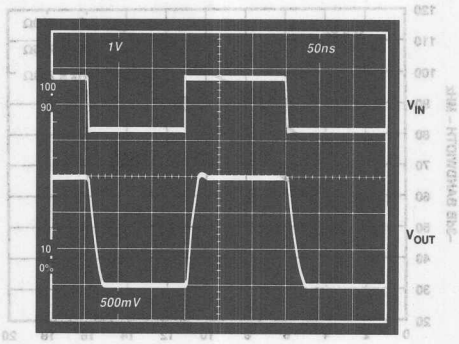


Figure 52. Pulse Response of the Circuit of Figure 50 with V_S = 5 V

Single Supply, Low Power Triple Video Amplifier

AD813

FEATURES

- Low Cost
- Three Video Amplifiers in One Package
- Optimized for Driving Cables in Video Systems
- Excellent Video Specifications (R_L = 150 Ω)
  - Gain Flatness 0.1 dB to 50 MHz
  - 0.03% Differential Gain Error
  - 0.06° Differential Phase Error
- Low Power
  - Operates on Single +3 V to ±15 V Power Supplies
  - 5.5 mA/Amplifier Max Power Supply Current
- High Speed
  - 125 MHz Unity Gain Bandwidth (–3 dB)
  - 500 V/µs Slew Rate
- High Speed Disable Function per Channel
  - Turn-Off Time 80 ns
- Easy to Use
  - 50 mA Output Current
  - Output Swing to 1 V of Rails

APPLICATIONS

- Video Line Driver
- LCD Drivers
- Computer Video Plug-In Boards
- Ultrasound
- RGB Amplifier
- CCD Based Systems

PRODUCT DESCRIPTION

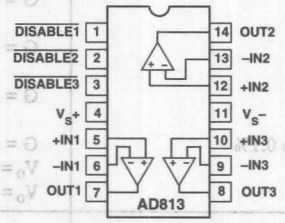
The AD813 is a low power, single supply triple video amplifier. Each of the three current feedback amplifiers has 50 mA of output current, and is optimized for driving one back terminated video load (150 Ω). The AD813 features gain flatness of 0.1 dB to 50 MHz while offering differential gain and phase error of 0.03% and 0.06°. This makes the AD813 ideal for broadcast and consumer video electronics.

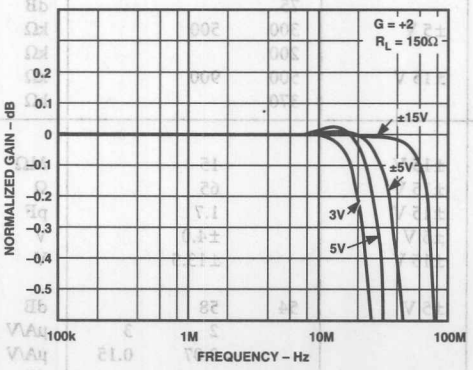
The AD813 offers low power of 5.5 mA per amplifier max and runs on a single +3 V power supply. The outputs of each amplifier swing to within one volt of either supply rail to easily accommodate video signals. While operating on a single +5 V supply the AD813 still achieves 0.1 dB flatness to 20 MHz and 0.05% & 0.05° of differential gain and phase performance. All this is offered in a small 14-pin plastic DIP or SOIC package. These features make this triple amplifier ideal for portable and battery powered applications where size and power are critical.

The outstanding bandwidth of 125 MHz along with 500 V/µs of slew rate make the AD813 useful in many general purpose, high speed applications where a single +3 V or dual power supplies up to ±15 V are needed. Furthermore the AD813 contains a high speed disable function for each amplifier in order to power down the amplifier or high impedance the output. This can then be used in video multiplexing applications. The AD813 is available in the industrial temperature range of –40°C to +85°C in plastic DIP and SOIC packages as well as chips.

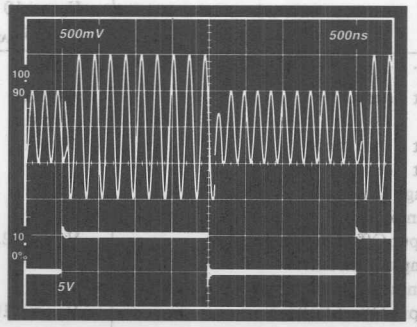
PIN CONFIGURATION

14-Pin DIP & SOIC Package





Fine-Scale Gain Flatness vs. Frequency, G = +2, R_L = 150 Ω



Channel Switching Characteristics for a 3:1 Mux

AD813—SPECIFICATIONS

DYNAMIC PERFORMANCE						
–3 dB Bandwidth	G = +2, No Peaking	±5 V	45	65		MHz
		±15 V	75	100		MHz
Bandwidth for 0.1dB Flatness	G = +2	±5 V	15	25		MHz
		±15 V	25	50		MHz
Slew Rate[1]	G = +2, R_L = 1 kΩ	±5 V		150		V/µs
		±15 V	150	250		V/µs
	G = –1, R_L = 1 kΩ	±5 V		225		V/µs
		±15 V		450		V/µs
Settling Time to 0.1%	G = –1, R_L = 1 kΩ					
	V_O = 3 V Step	±5 V		50		ns
	V_O = 10 V Step	±15 V		40		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	f_C = 1 MHz, R_L = 1 kΩ	±15 V		–90		dBc
Input Voltage Noise	f = 10 kHz	±5 V, ±15 V		3.5		nV√Hz
Input Current Noise	f = 10 kHz, +In	±5 V, ±15 V		1.5		pA√Hz
	–In	±5 V, ±15 V		18		pA√Hz
Differential Gain Error	NTSC, G = ±2, R_L = 150 Ω	±5 V		0.08		%
		±15 V		0.03	0.09	%
Differential Phase Error		±5 V		0.13		Degrees
		±15 V		0.06	0.12	Degrees
DC PERFORMANCE						
Input Offset Voltage		±5 V, ±15 V		2	5	mV
	T_{MIN}–T_{MAX}				12	mV
Offset Drift		±5 V, ±15 V		15		µV/°C
–Input Bias Current		±5 V, ±15 V		5	30	µA
	T_{MIN}–T_{MAX}				35	µA
+Input Bias Current		±5 V, ±15 V		0.5	1.5	µA
	T_{MIN}–T_{MAX}				2	µA
Open-Loop Voltage Gain	V_O = ±2.5 V, R_L = 150 Ω	±5 V	69	76		dB
	T_{MIN}–T_{MAX}		66			dB
	V_O = ±10 V, R_L = 1 kΩ	±15 V	76	82		dB
	T_{MIN}–T_{MAX}		75			dB
Open-Loop Transresistance	V_O = ±2.5 V, R_L = 150 Ω	±5 V	300	500		kΩ
	T_{MIN}–T_{MAX}		200			kΩ
	V_O = ±10 V, R_L = 1 kΩ	±15 V	500	900		kΩ
	T_{MIN}–T_{MAX}		370			kΩ
INPUT CHARACTERISTICS						
Input Resistance	+Input	±15 V		15		MΩ
	–Input	±15 V		65		Ω
Input Capacitance	+Input	±15 V		1.7		pF
Input Common Mode		±5 V		±4.0		V
Voltage Range		±15 V		±13.5		V
Common-Mode Rejection Ratio						
Input Offset Voltage	V_{CM} = ±2.5 V	±5 V	54	58		dB
–Input Current				2	3	µA/V
±Input Current				0.07	0.15	µA/V
Input Offset Voltage	V_{CM} = ±10 V	±15 V	57	62		dB
–Input Current				1.5	2.5	µA/V
+Input Current				0.05	0.1	µA/V

Model	Conditions	V_S	AD813A Min	AD813A Typ	AD813A Max	Units
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 150 Ω, T_{MIN}–T_{MAX}	±5 V	3.5	3.8		±V
	R_L = 1 kΩ, T_{MIN}–T_{MAX}	±15 V	13.6	14.0		±V
Output Current		±5 V	25	40		mA
		±15 V	30	50		mA
Short Circuit Current	G = +2, R_F = 715 Ω	±15 V		100		mA
	V_{IN} = 2 V					
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz	±5 V, ±15 V		–65		dB
Gain Flatness Match	G = +2, f = 40 MHz	±15 V		0.1		dB
DC						
Input Offset Voltage	T_{MIN}–T_{MAX}	±5 V, ±15 V		0.5	2.5	mV
–Input Bias Current	T_{MIN}–T_{MAX}	±5 V, ±15 V		2	10	µA
POWER SUPPLY						
Operating Range			±1.2		±18	V
Quiescent Current	Per Amplifier	±5 V		3.5	4.0	mA
		±15 V		4.5	5.5	mA
	T_{MIN}–T_{MAX}	±15 V			6.7	mA
Quiescent Current, Powered Down	Per Amplifier	±5 V		0.5	0.6	mA
		±15 V		0.75	0.9	mA
Power Supply Rejection Ratio						
Input Offset Voltage	V_S = ±1.5 V to ±15 V		72	80		dB
–Input Current				0.3	0.7	µA/V
+Input Current				0.005	0.05	µA/V
DISABLE CHARACTERISTICS						
Off Isolation	f = 5 MHz	±5 V, ±15 V		–57		dB
Off Output Impedance	G = +1	±5 V, ±15 V		12.5		pF
Channel-to-Channel Isolation	2 or 3 Channels Mux, f = 5 MHz	±5 V, ±15 V		–65		dB
Turn-On Time		±5 V, ±15 V		100		ns
Turn-Off Time				80		ns

NOTES

[1]Slew rate measurement is based on 10% to 90% rise time in the specified closed-loop gain.

Specifications subject to change without notice.

9

AD813–SPECIFICATIONS

Single Supply (@ T_A = + 25°C, R_L = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD813A Min	AD813A Typ	AD813A Max	Units
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	G = +2, No Peaking	+5 V	35	50		MHz
		+3 V	25	40		MHz
Bandwidth for 0.1 dB Flatness	G = +2	+5 V	12	20		MHz
		+3 V	8	15		MHz
Slew Rate[1]	G = +2, R_L = 1 kΩ	+5 V		100		V/µs
		+3 V		50		V/µs
NOISE/HARMONIC PERFORMANCE						
Input Voltage Noise	f = 10 kHz	+5 V, +3 V		3.5		nV√Hz
Input Current Noise	f = 10 kHz, +In	+5 V, +3 V		1.5		pA√Hz
	–In	+5 V, +3 V		18		pA√Hz
Differential Gain Error[2]	NTSC, G = +2, R_L = 150 Ω	+5 V		0.05		%
	G = +1	+3 V		0.2		%
Differential Phase Error[2]	G = +2	+5 V		0.05		Degrees
	G = +1	+3 V		0.2		Degrees
DC PERFORMANCE						
Input Offset Voltage		+5 V, +3 V		1.5	3	mV
	T_{MIN}–T_{MAX}				10	mV
Offset Drift		+5 V, +3 V		7		µV/°C
–Input Bias Current		+5 V, +3 V		7	30	µA
	T_{MIN}–T_{MAX}				35	µA
+Input Bias Current		+5 V, +3 V		0.5	1.5	µA
	T_{MIN}–T_{MAX}				2	µA
Open-Loop Voltage Gain	V_O = +2.5 V p-p	+5 V	67	70		dB
	V_O = +0.7 V p-p	+3 V		69		dB
Open-Loop Transresistance	V_O = +3 V p-p	+5 V	200	300		kΩ
	V_O = +1 V p-p	+3 V		225		kΩ
INPUT CHARACTERISTICS						
Input Resistance	+Input	+5 V, +3 V		15		MΩ
	–Input	+5 V		90		Ω
Input Capacitance	+Input			2		pF
Input Common Mode Voltage Range		+5 V	1.0		4.0	V
		+3 V	1.0		2.0	V
Common-Mode Rejection Ratio						
Input Offset Voltage	V_{CM} = 1.25 V to 3.75 V	+5 V	54	58		dB
–Input Current				3	5	µA/V
+Input Current				0.1	0.2	µA/V
Input Offset Voltage	V_{CM} = 1 V to 2 V	+3 V		56		dB
–Input Current				3.5		µA/V
+Input Current				0.1		µA/V

Model	Conditions	V_S	AD813A Min	Typ	Max	Units
OUTPUT CHARACTERISTICS						
Output Voltage Swing p-p	R_L = 150 Ω, T_{MIN}–T_{MAX}	+5 V	3.0	3.2		±V p-p
		+3 V	1.0	1.3		±V p-p
Output Current		+5 V	20	30		mA
		+3 V	15	25		mA
Short Circuit Current	G = +2, R_F = 715 Ω	+5 V		40		mA
	V_{IN} = 1 V					
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz	+5 V, +3 V		–65		dB
Gain Flatness Match	G = +2, f = 20 MHz	+5 V, +3 V		0.1		dB
DC						
Input Offset Voltage	T_{MIN}–T_{MAX}	+5 V, +3 V		0.5	2.5	mV
–Input Bias Current	T_{MIN}–T_{MAX}	+5 V, +3 V		2	10	µA
POWER SUPPLY						
Operating Range			2.4		36	V
Quiescent Current	Per Amplifier	+5 V		3.2	4.0	mA
		+3 V		3.0	3.5	mA
	T_{MIN}–T_{MAX}	+5 V			5.0	mA
Quiescent Current, Powered Down	Per Amplifier	+5 V		0.4	0.5	mA
		+3 V		0.4	0.5	mA
Power Supply Rejection Ratio						
Input Offset Voltage	V_S = +3.0 V to +30 V			76		dB
–Input Current				0.3		µA/V
+Input Current				0.005		µA/V
DISABLE CHARACTERISTICS						
Off Isolation	f = 5 MHz	+5 V, +3 V		–55		dB
Off Output Impedance	G = +1	+5 V, +3 V		13		pF
Channel-to-Channel Isolation	2 or 3 Channel Mux, f = 5 MHz	+5 V, +3 V		–65		dB
Turn-On Time		+5 V, +3 V		100		ns
Turn-Off Time				80		ns
TRANSISTOR COUNT				111		

NOTES
[1]Slew rate measurement is based on 10% to 90% rise time in the specified closed-loop gain.
[2]Single supply differential gain and phase are measured with the ac coupled circuit of Figure 49.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.6 Watts
Small Outline (R) . . . . . 1.0 Watts
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Output Short Circuit Duration . . . Observe Power Derating Curves
Storage Temperature Range N, R . . . . . –65°C to +125°C
Operating Temperature Range
AD813A . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
14-Pin Plastic DIP Package: θ_{JA} = 75°C/Watt
14-Pin SOIC Package: θ_{JA} = 120°C/Watt

ORDERING GUIDE

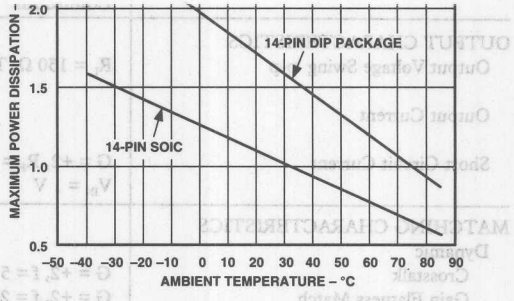
Model	Temperature Range	Package Description	Package Options*
AD813AN	–40°C to +85°C	14-Pin Plastic DIP	N-14
AD813AR-14	–40°C to +85°C	14-Pin Plastic SOIC	R-14
AD813A Chips	–40°C to +85°C	Die Form	

*For outline information see Package Information section.

maximum safe junction temperature for the plastic encapsulated parts is determined by the glass transition temperature of the plastic, about 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD813 is internally short circuit protected, this may not be enough to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is important to observe the derating curves.

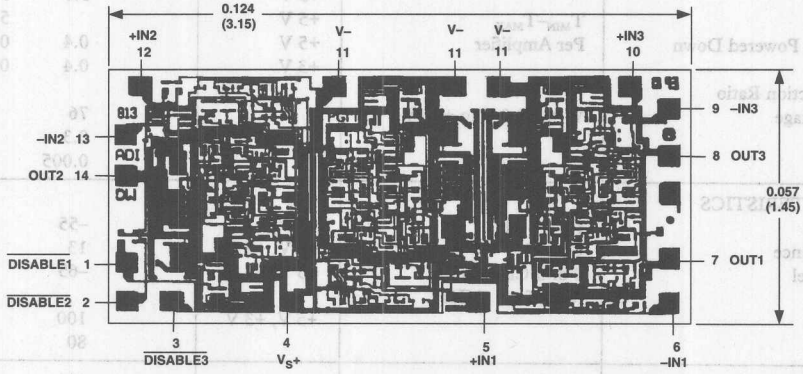
It must also be noted that in (noninverting) gain configurations (with low values of gain resistor), a high level of input overdrive can result in a large input error current, which may result in a significant power dissipation in the input stage. This power must be included when computing the junction temperature rise due to total internal power.



Maximum Power Dissipation vs. Ambient Temperature

METALIZATION PHOTO

Dimensions shown in inches and (mm).



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD813 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

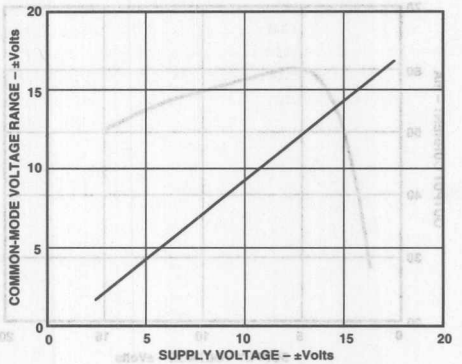


Figure 1. Input Common-Mode Voltage Range vs. Supply Voltage

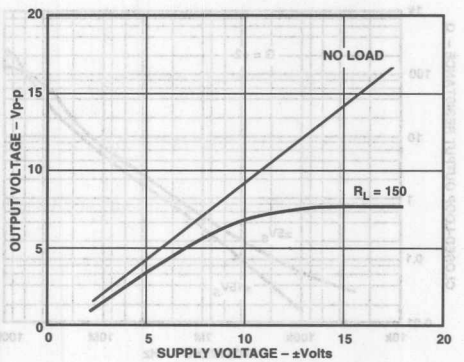


Figure 2. Output Voltage Swing vs. Supply

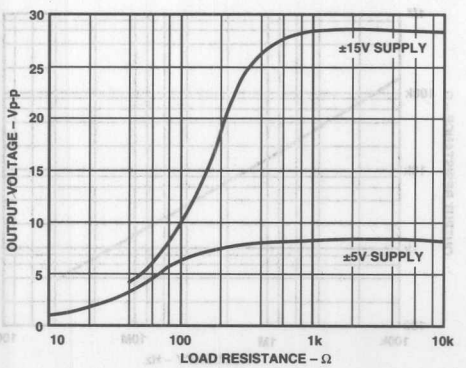


Figure 3. Output Voltage Swing vs. Load Resistance

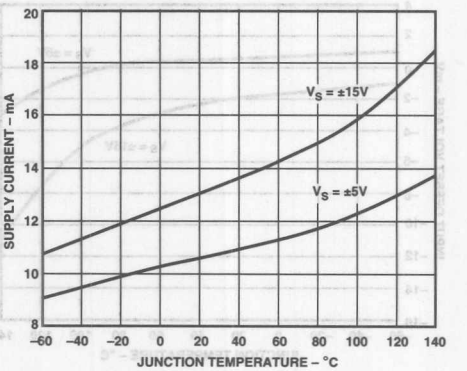


Figure 4. Supply Current vs. Junction Temperature

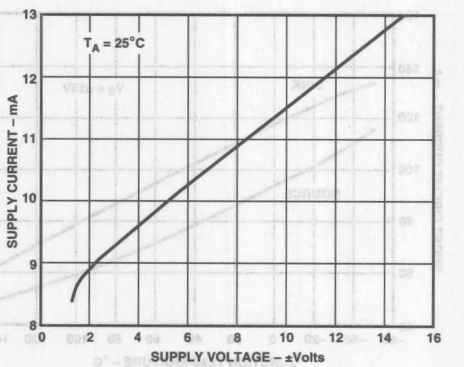


Figure 5. Supply Current vs. Supply Voltage at Low Voltages

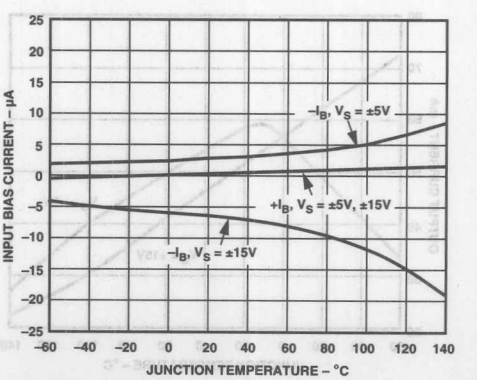


Figure 6. Input Bias Current vs. Junction Temperature

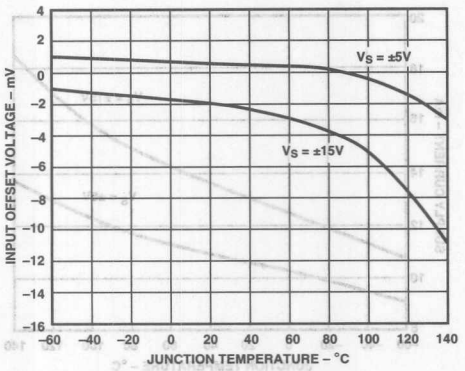


Figure 7. Input Offset Voltage vs. Junction Temperature

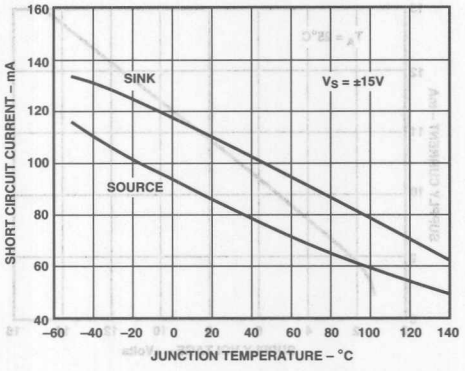


Figure 8. Short Circuit Current vs. Junction Temperature

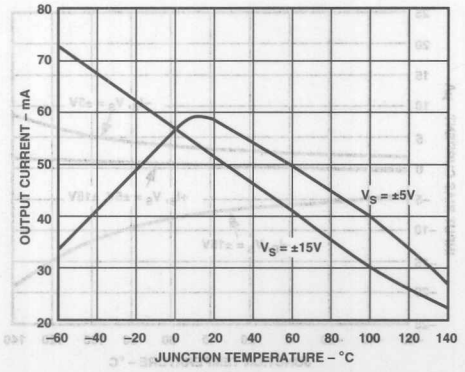


Figure 9. Linear Output Current vs. Junction Temperature

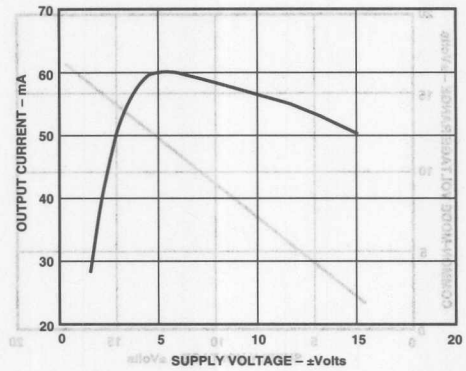


Figure 10. Linear Output Current vs. Supply Voltage

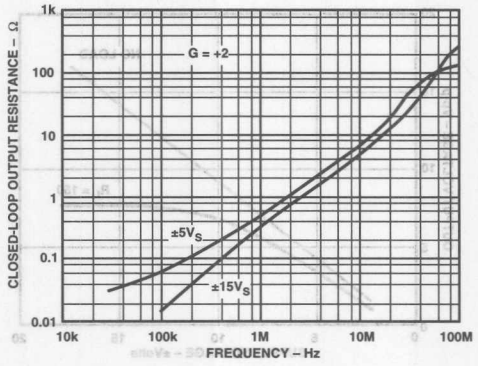


Figure 11. Closed-Loop Output Resistance vs. Frequency

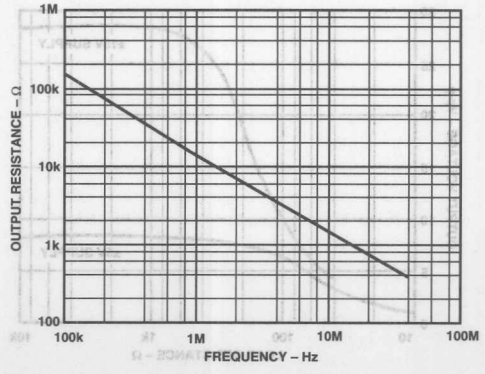


Figure 12. Output Resistance vs. Frequency, Disabled State

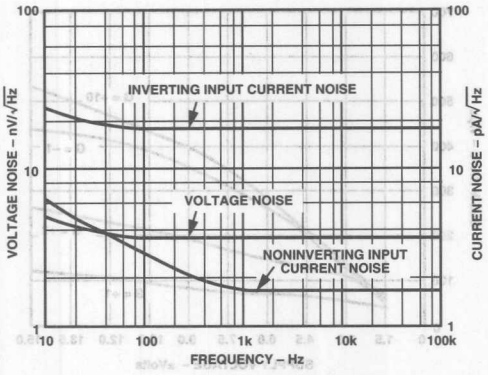


Figure 13. Input Current and Voltage Noise vs. Frequency

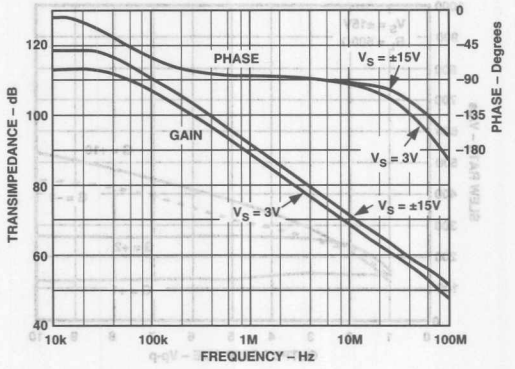


Figure 16. Open-Loop Transimpedance vs. Frequency (Relative to 1 Ω)

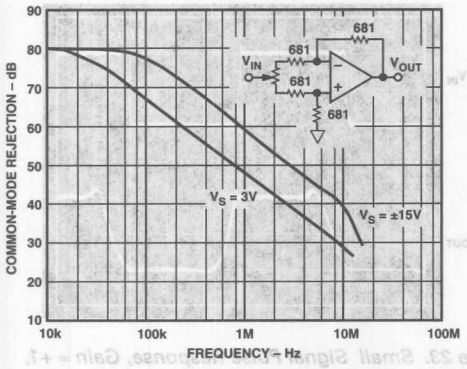


Figure 14. Common-Mode Rejection vs. Frequency

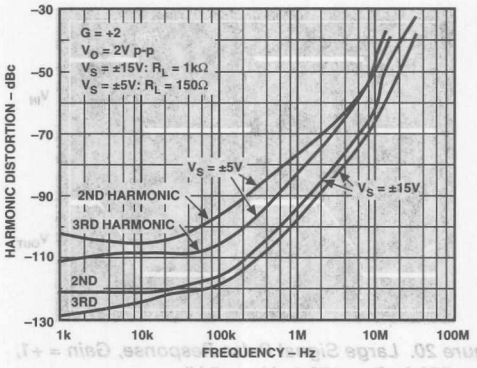


Figure 17. Harmonic Distortion vs. Frequency

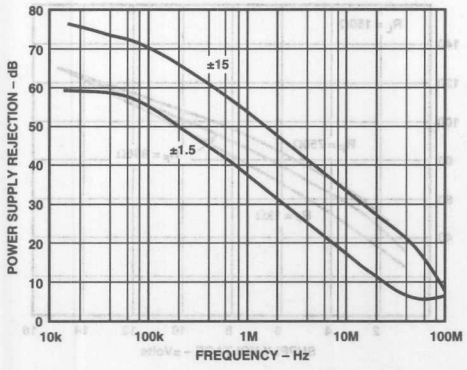


Figure 15. Power Supply Rejection vs. Frequency

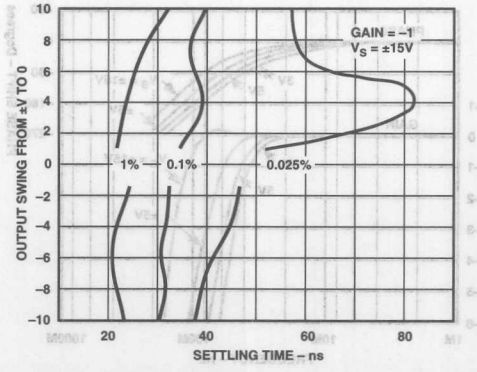


Figure 18. Output Swing and Error vs. Settling Time

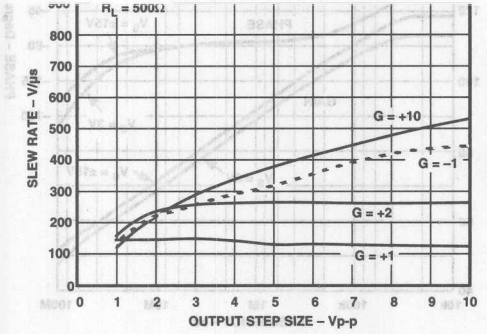


Figure 19. Slew Rate vs. Output Step Size

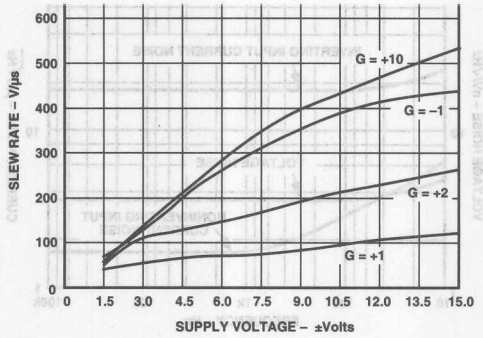


Figure 22. Maximum Slew Rate vs. Supply Voltage

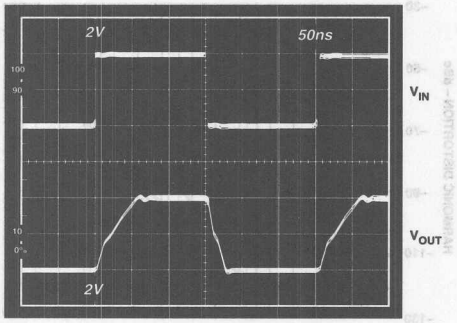


Figure 20. Large Signal Pulse Response, Gain = +1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

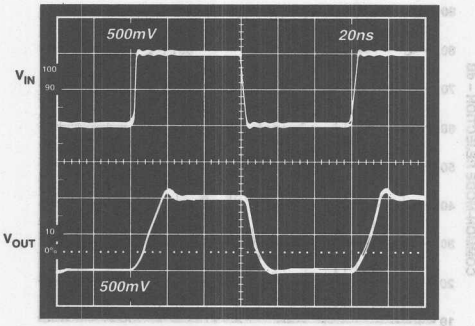


Figure 23. Small Signal Pulse Response, Gain = +1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

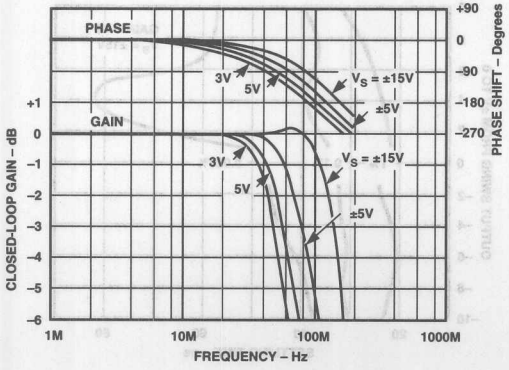


Figure 21. Closed-Loop Gain and Phase vs. Frequency, G = +1

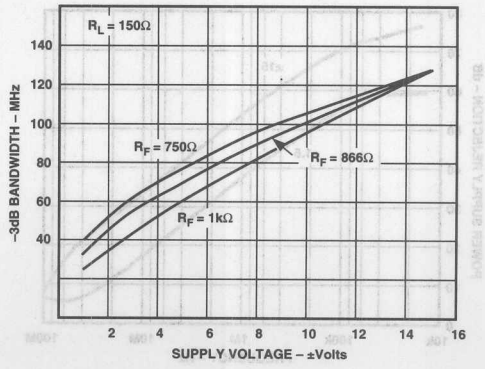


Figure 24. –3 dB Bandwidth vs. Supply Voltage, G = +1

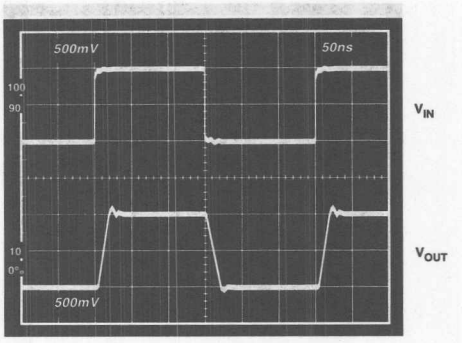


Figure 25. Large Signal Pulse Response, Gain = +10, (R_F = 357 Ω, R_L = 500 Ω, V_S = ±15 V)

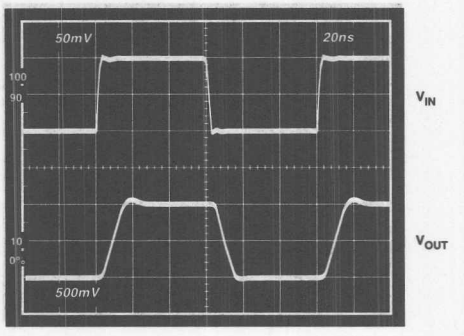


Figure 28. Small Signal Pulse Response, Gain = +10, (R_F = 357 Ω, R_L = 150 Ω, V_S = ±5 V)

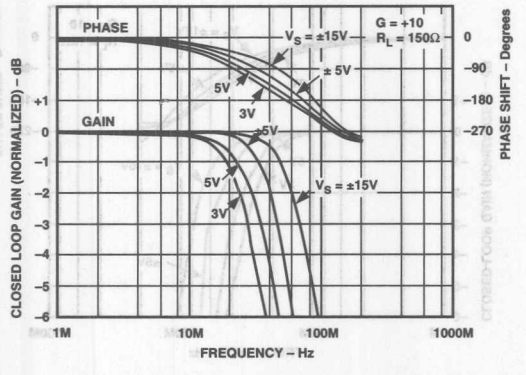


Figure 26. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 150 Ω

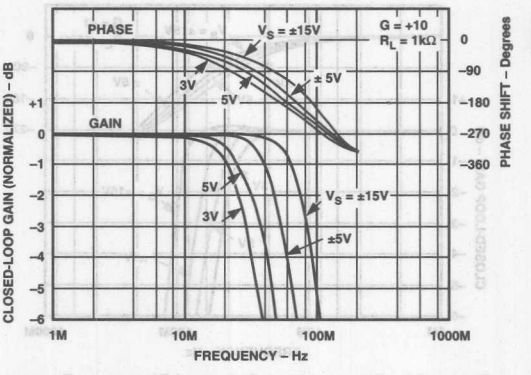


Figure 29. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 1 kΩ

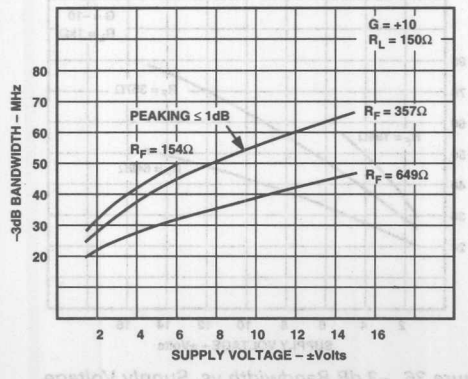


Figure 27. –3 dB Bandwidth vs. Supply Voltage, G = +10, R_L = 150 Ω

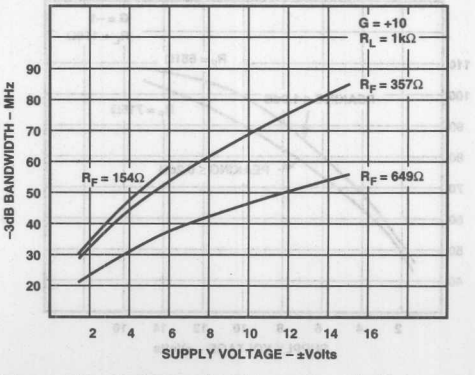


Figure 30. –3 dB Bandwidth vs. Supply Voltage G = +10, R_L = 1 kΩ

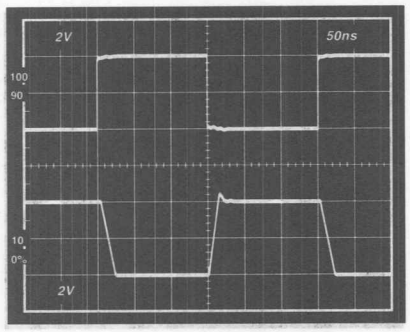


Figure 31. Large Signal Pulse Response, Gain = –1,

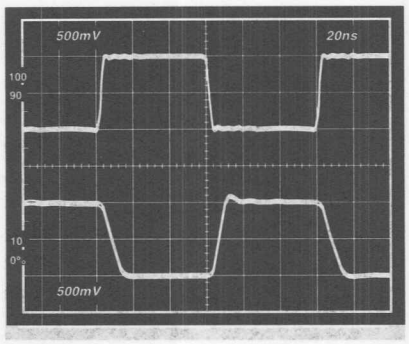


Figure 34. Small Signal Pulse Response, Gain = –1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

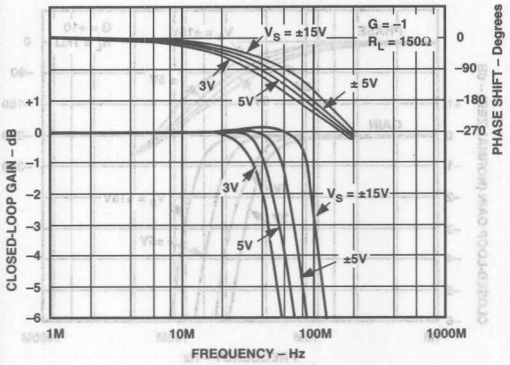


Figure 32. Closed-Loop Gain and Phase vs. Frequency, G = –1, R_L = 150 Ω

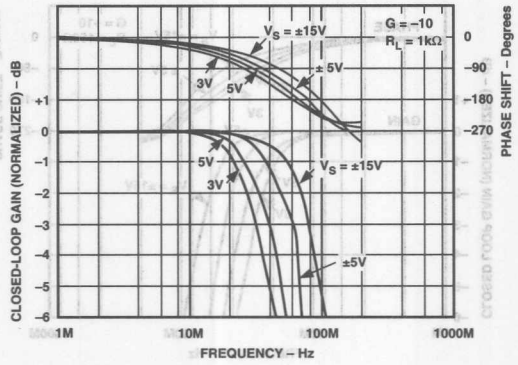


Figure 35. Closed-Loop Gain and Phase vs. Frequency, G = –10, R_L = 1 kΩ

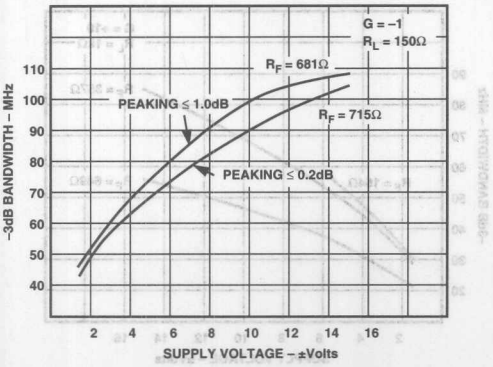


Figure 33. –3 dB Bandwidth vs. Supply Voltage, G = –1, R_L = 150 Ω

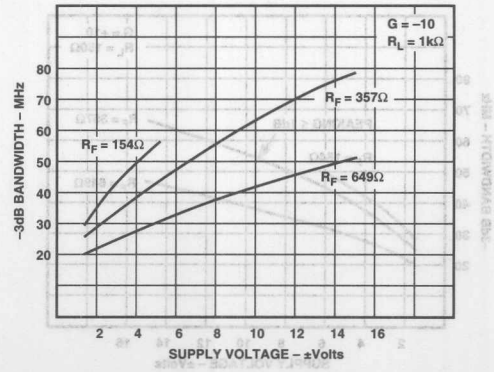


Figure 36. –3 dB Bandwidth vs. Supply Voltage, G = –10, R_L = 1 kΩ

General Consideration

The AD813 is a wide bandwidth, triple video amplifier that offers a high level of performance on less than 5.5 mA per amplifier of quiescent supply current. With its fast acting power down switch, it is designed to offer outstanding functionality and performance at closed-loop inverting or noninverting gains of one or greater.

Built on a low cost, complementary bipolar process, and achieving bandwidth in excess of 100 MHz, differential gain and phase errors of better than 0.1% and 0.1° (into 150 Ω), and output current greater than 40 mA, the AD813 is an exceptionally efficient video amplifier. Using a conventional current feedback architecture, its high performance is achieved through careful attention to design details.

Choice of Feedback & Gain Resistors

Because it is a current feedback amplifier, the closed-loop bandwidth of the AD813 depends on the value of the feedback resistor. The bandwidth also depends on the supply voltage. In addition, attenuation of the open-loop response when driving load resistors less than about 250 Ω will also affect the bandwidth. Table I contains data showing typical bandwidths at different supply voltages for some useful closed-loop gains when driving a load of 150 Ω. (Bandwidths will be about 20% greater for load resistances above a few hundred ohms.)

Table I. –3 dB Bandwidth vs. Closed-Loop Gain and Feedback Resistor, (R_L = 150 Ω)

V_S (V)	Gain	R_F (Ω)	BW (MHz)
±15	+1	866	125
	+2	681	100
	+10	357	60
	–1	681	100
	–10	357	55
±5	+1	750	75
	+2	649	65
	+10	154	40
	–1	649	70
	–10	154	40
+5	+1	715	60
	+2	619	50
	+10	154	30
	–1	619	50
	–10	154	30
+3	+1	681	50
	+2	619	40
	+10	154	25
	–1	619	40
	–10	154	20

The choice of feedback resistor is not critical unless it is important to maintain the widest, flattest frequency response. The resistors recommended in the table are those (metal film values) that will result in the widest 0.1 dB bandwidth. In those applications where the best control of the bandwidth is desired, 1% metal film resistors are adequate. Wider bandwidths can be attained by reducing the magnitude of the feedback resistor (at the expense of increased peaking), while peaking can be reduced by increasing the magnitude of the feedback resistor.

To estimate the –3 dB bandwidth for closed-loop gains or feedback resistors not listed in the above table, the following two pole model for the AD813 may be used:

$$A_{CL} = \frac{G}{S^2\left[\frac{(R_F + Gr_{IN})C_T}{2\pi f_2}\right] + S\,(R_F + Gr_{IN})\,C_T + 1}$$

Where: A_{CL} = closed-loop gain from "transcapacitance"
G = $1 + R_F/R_G$
r_{IN} = input resistance of the inverting input
C_T = "transcapacitance," which forms the open-loop dominant pole with the transresistance
R_F = feedback resistor
R_G = gain resistor
f_2 = frequency of second (nondominant) pole
s = $2\pi j f$

Appropriate values for the model parameters at different supply voltages are listed in Table II. Reasonable approximations for these values at supply voltages not found in the table can be obtained by a simple linear interpolation between those tabulated values which 'bracket' the desired condition.

Table II. Two Pole Model Parameters at Various Supplies

V_S (V)	r_{IN} (Ω)	C_T (pF)	f_2 (MHz)
±15	85	2.5	150
±5	90	3.8	125
+5	105	4.8	105
+3	115	5.5	95

As discussed in many amplifier and electronics textbooks (such as Roberge's *Operational Amplifiers: Theory and Practice*), the –3 dB bandwidth for the 2-pole model can be obtained as:

$$f_3 = f_n\left[1 - 2d^2 + (2 - 4d^2 + 4d^4)^{1/2}\right]^{1/2}$$

where:

$$f_n = \left[\frac{f_2}{(R_F + Gr_{IN})\,C_T}\right]^{1/2}$$

and:

$$d = \frac{1}{2}\left[f_2 (R_F + Gr_{IN})\,C_T\right]^{1/2}$$

This model will predict –3 dB bandwidth within about 10% to 15% of the correct value when the load is 150 Ω. However, it is not accurate enough to predict either the phase behavior or the frequency response peaking of the AD813.

9

As with all wideband amplifiers, printed circuit board parasitics can affect the overall closed-loop performance. Most important for controlling the 0.1 dB bandwidth are stray capacitances at the output and inverting input nodes. Increasing the space between signal lines and ground plane will minimize the coupling. Also, signal lines connecting the feedback and gain resistors should be kept short enough that their associated inductance does not cause high frequency gain errors.

Power Supply Bypassing

Adequate power supply bypassing can be very important when optimizing the performance of high speed circuits. Inductance in the supply leads can (for example) contribute to resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to a load, then large (greater than 1 µF) bypass capacitors are required to produce the best settling time and lowest distortion. Although 0.1 µF capacitors may be adequate in some applications, more elaborate bypassing is required in other cases.

When multiple bypass capacitors are connected in parallel, it is important to be sure that the capacitors themselves do not form resonant circuits. A small (say 5 Ω) resistor may be required in series with one of the capacitors to minimize this possibility.

As discussed below, power supply bypassing can have a significant impact on crosstalk performance.

Achieving Low Crosstalk

Measured crosstalk from the output of Amplifier 2 to the input of Amplifier 1 of the AD813 is shown in Figure 37. All other crosstalk combinations, (from the output of one amplifier to the input of another), are a few dB better than this due to the additional distance between critical signal nodes.

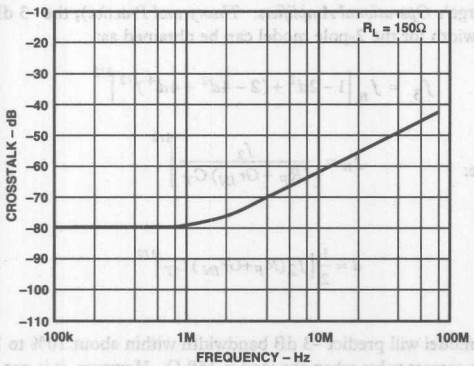


Figure 37. Worst Case Crosstalk vs. Frequency

difficulty in achieving low crosstalk are inadequate power supply bypassing, overlapped input and/or output signal paths, and capacitive coupling between critical nodes.

The bypass capacitors must be connected to the ground plane at a point close to and between the ground reference points for the loads. (The bypass of the negative power supply is particularly important in this regard.) This requires careful planning as there are three amplifiers in the package, and low impedance signal return paths must be provided for each load. (Using a parallel combination of 1 µF, 0.1 µF, and 0.01 µF bypass capacitors will help to achieve optimal crosstalk.)

The input and output signal return paths (to the bypass caps) must also be kept from overlapping. Since ground connections are not of perfectly zero impedance, current in one ground return path can produce a voltage drop in another ground return path if they are allowed to overlap.

Electric field coupling external to (and across) the package can be reduced by arranging for a narrow strip of ground plane to be run between the pins (parallel to the pin rows). Doing this on both sides of the board can reduce the high frequency crosstalk by about 5 dB or 6 dB.

Driving Capacitive Loads

When used with the appropriate output series resistor, any load capacitance can be driven without peaking or oscillation. In most cases, less than 50 Ω is all that is needed to achieve an extremely flat frequency response. As illustrated in Figure 41, the AD813 can be very attractive for driving large capacitive loads. In this case, the AD813's high output short circuit current allows for a 150 V/µs slew rate when driving a 510 pF capacitor.

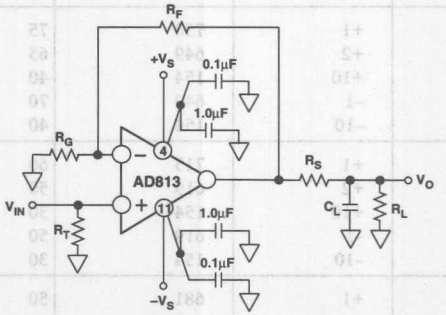


Figure 38. Circuit for Driving a Capacitive Load

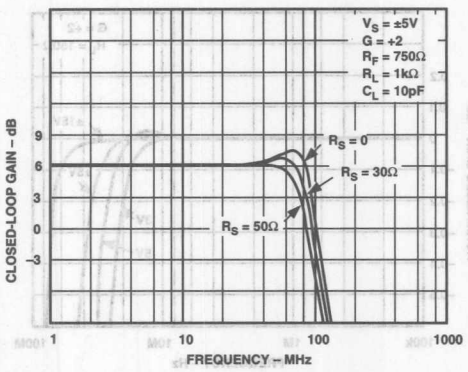


Figure 39. Response to a Small Load Capacitor at V_S = ±5 V

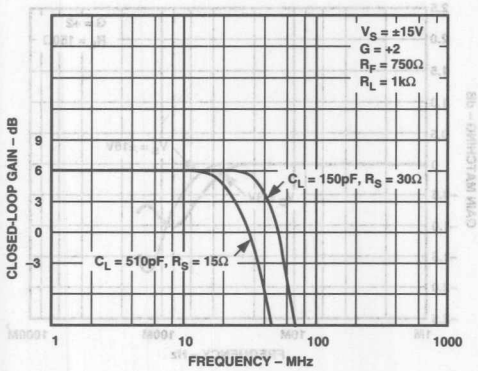


Figure 40. Response to a Large Load Capacitor at V_S = ±15 V

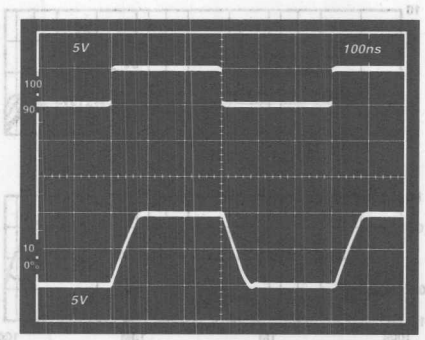


Figure 41. Circuit of Figure 38 Driving a 510 pF Load Capacitor, V_S = ±15 V (R_L = 1 kΩ, R_F = R_G = 750 Ω, R_S = 15 Ω)

Overload Recovery

There are three important overload conditions to consider. They are due to: input common-mode voltage overdrive, output voltage overdrive, and input current overdrive. When the amplifier is configured for low closed-loop gains, and the input common-mode voltage range is exceeded, the recovery time will be very fast, typically under 30 ns. When configured for a higher gain, and overloaded at the output, the recovery time will also be short. For example, in a gain of +10, with 6 dB of input overdrive, the recovery time of the AD813 is about 25 ns (see Figure 42).

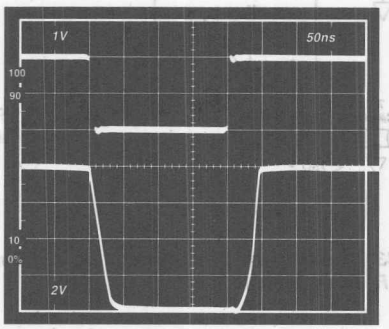


Figure 42. 6 dB Overload Recovery, G = +10, (R_L = 500 Ω, R_F = 357 Ω, V_S = ±5 V)

In the case of high gains with very high levels of input overdrive, a longer recovery time will occur. For example, if the input common-mode voltage range is exceeded in the gain of +10, the recovery time will be on the order of 100 ns. This is primarily due to current overloading of the input stage.

As noted in the warning under "Maximum Power Dissipation," a high level of input overdrive in a high noninverting gain circuit can result in a large current flow in the input stage. Though this current is internally limited to about 40 mA, its effect on the total power dissipation may be significant.

High Performance Video Line Driver

At a gain of +2, the AD813 makes an excellent driver for a back terminated 75 Ω video line. Low differential gain and phase errors and wide 0.1 dB bandwidth can be realized over a wide range of power supply voltage. Excellent gain and group delay matching are also attainable over the full operating supply voltage range.

Figures 47 and 48 show the worst case matching; the match between amplifiers 2 and 3 is typically much better than this.

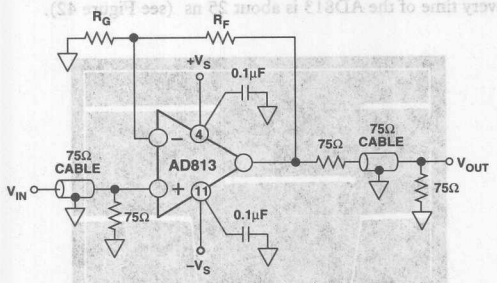


Figure 43. A Video Line Driver Operating at a Gain of +2 ($R_F = R_G$ from Table I)

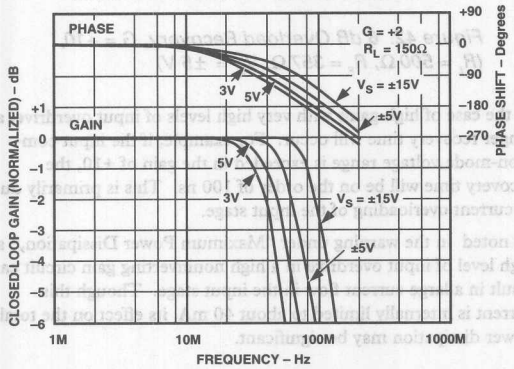


Figure 44. Closed-Loop Gain & Phase vs. Frequency for the Line Driver

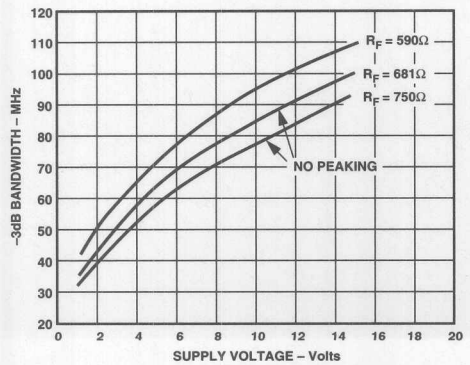


Figure 45. –3 dB Bandwidth vs. Supply Voltage for Gain = +2, R_L = 150 Ω

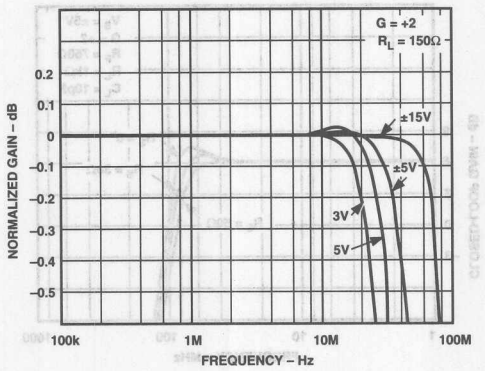


Figure 46. Fine-Scale Gain (Normalized) vs. Frequency

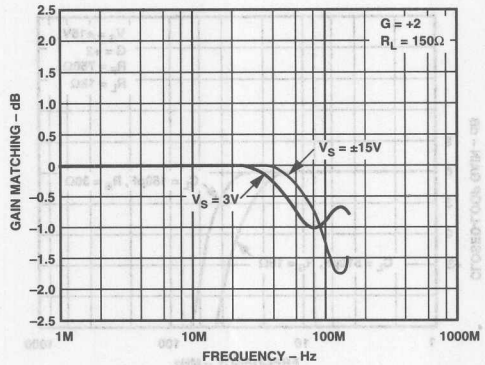


Figure 47. Closed-Loop Gain Matching vs. Frequency

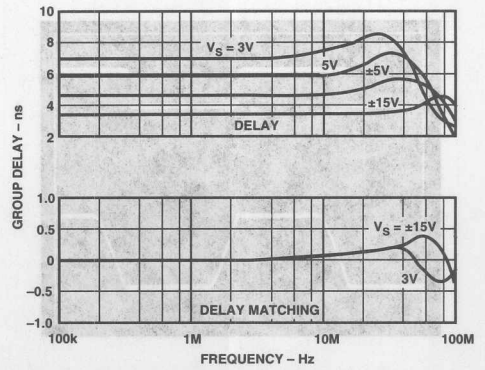


Figure 48. Group Delay and Group Delay Matching vs. Frequency, G = +2, R_L = 150 Ω

Operation Using a Single Supply

The AD813 will operate with total supply voltages from 36 V down to 2.4 V. With proper biasing (see Figure 49) it can make an outstanding single supply video amplifier. Since the input and output voltage ranges extend to within 1 V of the supply rails, it will handle a 1.3 V peak-to-peak signal on a single 3.3 V supply, or a 3 V peak-to-peak signal on a single 5 V supply. The small signal 0.1 dB bandwidths will exceed 10 MHz in either case, and the large signal bandwidths will exceed 6 MHz.

The capacitively coupled cable driver in Figure 49 will achieve outstanding differential gain and phase errors of 0.05% and 0.05 degrees respectively on a single 5 V supply. Resistor R2, in this circuit, is selected to optimize the differential gain and phase by biasing the amplifier in its most linear region.

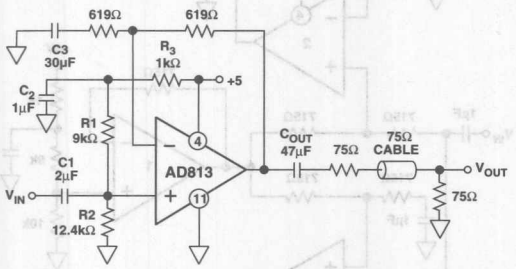


Figure 49. Biasing for Single Supply Operation

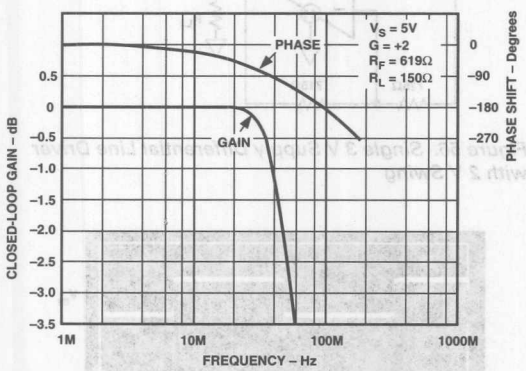


Figure 50. Closed-Loop Gain and Phase vs. Frequency, Circuit of Figure 49

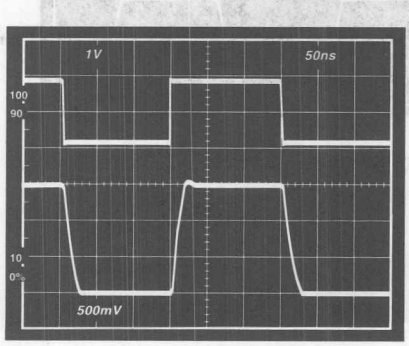


Figure 51. Pulse Response for the Circuit of Figure 49 with $+V_S$ = 5 V

Disable Mode Operation

Pulling the voltage on any one of the Disable pins about 2.5 V down from the positive supply will put the corresponding amplifier into a disabled, powered down, state. In this condition, the amplifier's quiescent supply current drops to about 0.5 mA, its output becomes a high impedance, and there is a high level of isolation from input to output. In the case of the gain of two line driver for example, the impedance at the output node will be about the same as for a 1.4 kΩ resistor (the feedback plus gain resistors) in parallel with a 12.5 pF capacitor and the input to output isolation will be about 65 dB at 1 MHz.

Leaving the Disable pin disconnected (floating) will leave the corresponding amplifier operational, in the enabled state. The input impedance of the disable pins is about 35 kΩ in parallel with a few pF. When grounded, about 50 µA flows out of a disable pin on ±5 V supplies.

Input voltages greater than about 1.5 V peak-to-peak will defeat the isolation. In addition, large signals (greater than 3 V peak-to-peak) applied to the output node will cause the output impedance to drop significantly.

When the Disable pins are driven by complementary output CMOS logic (such as the 74HC04), the disable time is about 80 ns (until the output goes high impedance) and the enable time is about 100 ns (to low impedance output) on ±15 V supplies. When operated on ±15 V supplies, the disable pins should be driven by open drain logic. In this case, pull-up resistors from the disable pins to the plus supply will ensure minimum switching time.

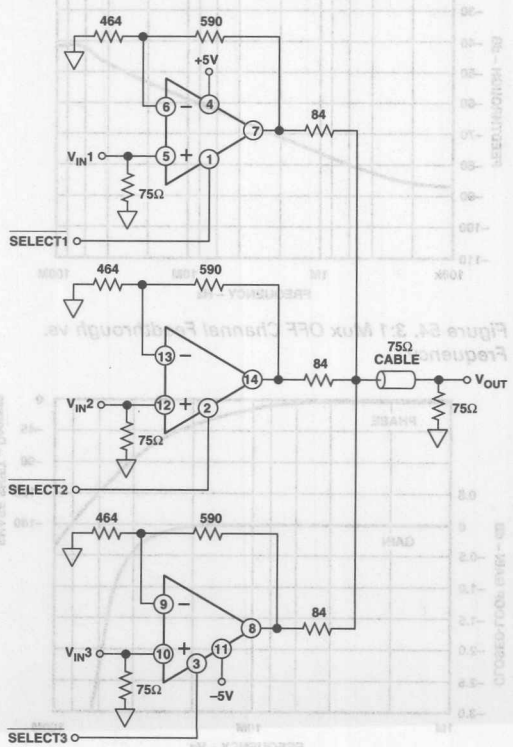


Figure 52. A Fast Switching 3:1 Video Mux (Supply Bypassing Not Shown)

3:1 Video Multiplexer

Wiring the amplifier outputs together will form a 3:1 mux with outstanding gain flatness. Figure 52 shows a recommended configuration which results in –0.1 dB bandwidth of 20 MHz and OFF channel isolation of 60 dB at 10 MHz on ±5 V supplies. The time to switch between channels is about 180 ns. Switching time is only slightly affected by signal level.

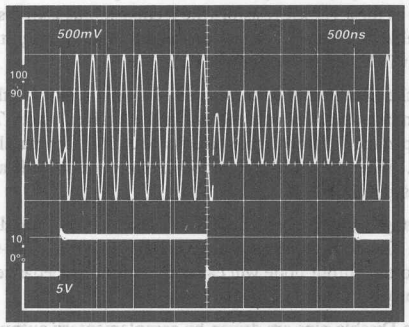


Figure 53. Channel Switching Characteristic for the 3:1 Mux

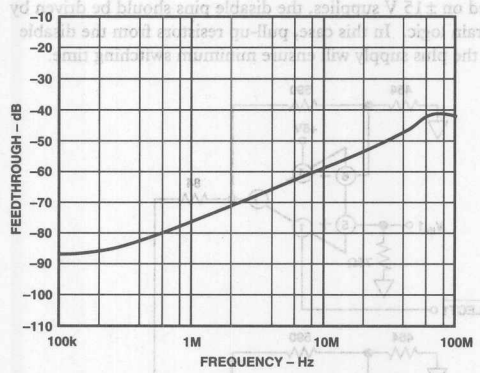


Figure 54. 3:1 Mux OFF Channel Feedthrough vs. Frequency

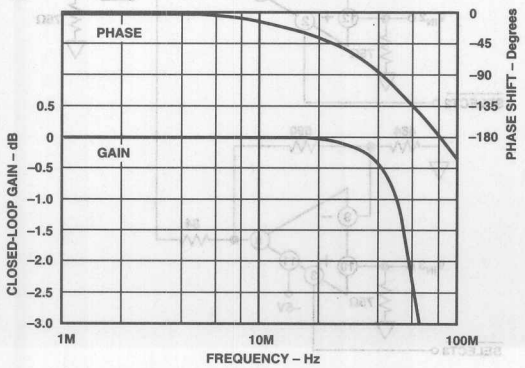


Figure 55. 3:1 Mux ON Channel Gain and Phase vs. Frequency

Single Supply Differential Line Driver

Due to its outstanding overall performance on low supply voltages, the AD813 makes possible exceptional differential transmission on very low power. The circuit of Figure 56 will convert a single-ended, ground referenced signal to a differential signal whose common-mode reference is set to one half the supply voltage. This allows for a greater than 2 V peak-to-peak signal swing on a single 3 V power supply. A bandwidth over 30 MHz is achieved with 20 mA of output drive on only 30 mW of quiescent power (excluding load current).

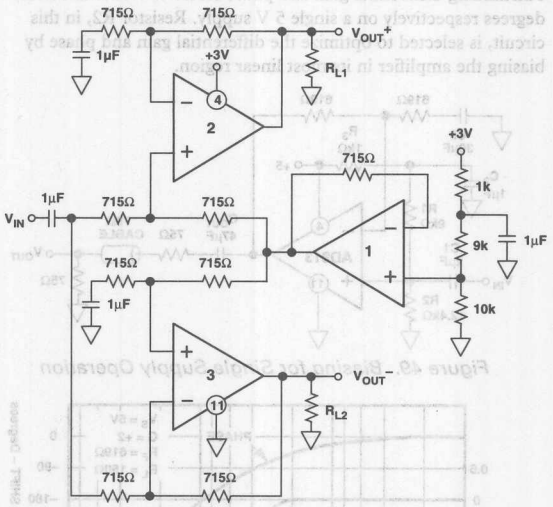


Figure 56. Single 3 V Supply Differential Line Driver with 2 V Swing

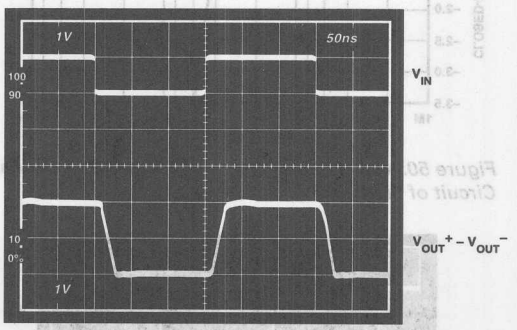


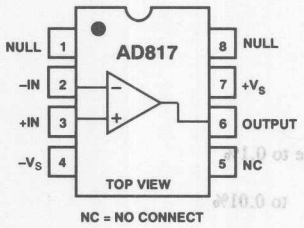
Figure 57. Differential Driver Pulse Response (V_S = 3 V, $R_{L1} = R_{L2}$ = 200 Ω)

High Speed, Low Power Wide Supply Range Amplifier

AD817

FEATURES
Low Cost
High Speed
50 MHz Unity Gain Bandwidth
350 V/μs Slew Rate
45 ns Settling Time to 0.1% (10 V Step)
Flexible Power Supply
Specified for Single (+5 V) and Dual (±5 V to ±15 V) Power Supplies
Low Power: 7.5 mA max Supply Current
High Output Drive Capability
Drives Unlimited Capacitive Load
50 mA Minimum Output Current
Excellent Video Performance
70 MHz 0.1 dB Bandwidth (Gain = +1)
0.04% & 0.08° Differential Gain & Phase Errors @ 3.58 MHz
Available in 8-Pin SOIC and 8-Pin Plastic Mini-DIP

CONNECTION DIAGRAM
8-Pin Plastic Mini-DIP (N), and SOIC (R) Packages



9

PRODUCT DESCRIPTION

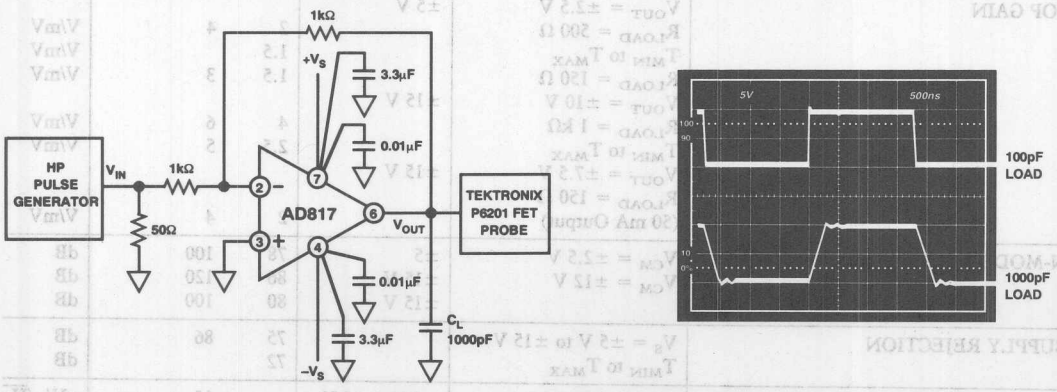
The AD817 is a low cost, low power, single/dual supply, high speed op amp which is ideally suited for a broad spectrum of signal conditioning and data acquisition applications. This breakthrough product also features high output current drive capability and the ability to drive an unlimited capacitive load while still maintaining excellent signal integrity.

The 50 MHz unity gain bandwidth, 350 V/μs slew rate and settling time of 45 ns (0.1%) make possible the processing of high speed signals common to video and imaging systems. Furthermore, professional video performance is attained by offering differential gain & phase errors of 0.04% & 0.08° @ 3.58 MHz and 0.1 dB flatness to 70 MHz (gain = +1).

The AD817 is fully specified for operation with a single +5 V power supply and with dual supplies from ±5 V to ±15 V. This power supply flexibility, coupled with a very low supply current of 7.5 mA and excellent ac characteristics under all power supply conditions, make the AD817 the ideal choice for many demanding yet power sensitive applications.

In applications such as ADC buffers and line drivers the AD817 simplifies the design task with its unique combination of a 50 mA minimum output current and the ability to drive unlimited capacitive loads.

The AD817 is available in 8-pin plastic mini-DIP and SOIC packages.



AD817 Driving a Large Capacitive Load

Parameter	Conditions	V_S	Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
Unity Gain Bandwidth		±5 V	30	35		MHz
		±15 V	45	50		MHz
		0, +5 V	25	29		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	±5 V	18	30		MHz
		±15 V	40	70		MHz
		0, +5 V	10	20		MHz
Full Power Bandwidth[1]	V_{OUT} = 5 V p-p					
	R_{LOAD} = 500 Ω	±5 V		15.9		MHz
	V_{OUT} = 20 V p-p					
	R_{LOAD} = 1 kΩ	±15 V		5.6		MHz
Slew Rate	R_{LOAD} = 1 kΩ	±5 V	200	250		V/µs
	Gain = −1	±15 V	300	350		V/µs
		0, +5 V	150	200		V/µs
Settling Time to 0.1%	−2.5 V to +2.5 V	±5 V		45		ns
	0 V–10 V Step, A_V = −1	±15 V		45		ns
to 0.01%	−2.5 V to +2.5 V	±5 V		70		ns
	0 V–10 V Step, A_V = −1	±15 V		70		ns
Total Harmonic Distortion	F_C = 1 MHz	±15 V		63		dB
Differential Gain Error	NTSC	±15 V		0.04	0.08	%
(Rl = 150 Ω)	Gain = +2	±5 V		0.05	0.1	%
		0, +5 V		0.11		%
Differential Phase Error	NTSC	±15 V		0.08	0.1	Degrees
(Rl = 150 Ω)	Gain = +2	±5 V		0.06	0.1	Degrees
		0, +5 V		0.14		Degrees
INPUT OFFSET VOLTAGE		±5 V to ±15 V		0.5	2	mV
	T_{MIN} to T_{MAX}				3	mV
Offset Drift				10		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	6.6	µA
	T_{MIN}				10	µA
	T_{MAX}				4.4	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		25	200	nA
	T_{MIN} to T_{MAX}				500	nA
Offset Current Drift				0.3		nA/°C
OPEN LOOP GAIN	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		2	4		V/mV
	T_{MIN} to T_{MAX}		1.5			V/mV
	R_{LOAD} = 150 Ω		1.5	3		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		4	6		V/mV
	T_{MIN} to T_{MAX}		2.5	5		V/mV
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 150 Ω					
	(50 mA Output)		2	4		V/mV
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5	78	100		dB
	V_{CM} = ±12 V	±15 V	86	120		dB
		±15 V	80	100		dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		75	86		dB
	T_{MIN} to T_{MAX}		72			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±5 V, ±15 V		15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±5 V, ±15 V		1.5		pA/√Hz

Parameter	Conditions	V_S	AD817A Min	AD817A Typ	AD817A Max	Units
INPUT COMMON-MODE VOLTAGE RANGE		±5 V	+3.8	+4.3		V
			−2.7	−3.4		V
		±15 V	+13	+14.3		V
			−12	−13.4		V
		0, +5 V	+3.8	+4.3		V
			+1.2	+0.9		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.3	3.8		±V
	R_{LOAD} = 150 Ω	±5 V	3.2	3.6		±V
	R_{LOAD} = 1 kΩ	±15 V	13.3	13.7		±V
	R_{LOAD} = 500 Ω	±15 V	12.8	13.4		±V
	R_{LOAD} = 500 Ω	0, +5 V	+1.5, +3.5			V
Output Current		±15 V	50			mA
		±5 V	50			mA
		0, +5 V	30			mA
Short-Circuit Current		±15 V		90		mA
INPUT RESISTANCE				300		kΩ
INPUT CAPACITANCE				1.5		pF
OUTPUT RESISTANCE	Open Loop			8		Ω
POWER SUPPLY						
Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current		±5 V		7.0	7.5	mA
	T_{MIN} to T_{MAX}	±5 V			7.5	mA
		±15 V			7.5	mA
	T_{MIN} to T_{MAX}	±15 V		7.0	7.5	mA

NOTE
[1]Full power bandwidth = slew rate/2 π V_{PEAK}.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

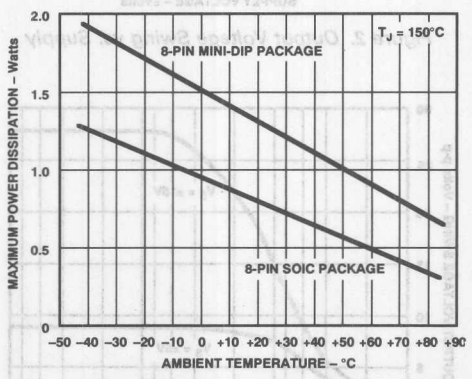
Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . See Derating Curves
Small Outline (R) . . . . . See Derating Curves
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Output Short Circuit Duration . . . . . See Derating Curves
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 10 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air: 8-pin plastic package, θ_{JA} = 100°C/watt; 8-pin SOIC package, θ_{JA} = 155°C/watt.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD817AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD817AR	−40°C to +85°C	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.



Maximum Power Dissipation vs. Temperature for Different Package Types

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD817 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

AD817—Typical Characteristics

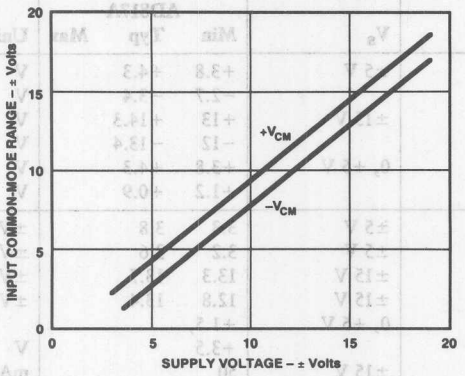


Figure 1. Common-Mode Voltage Range vs. Supply

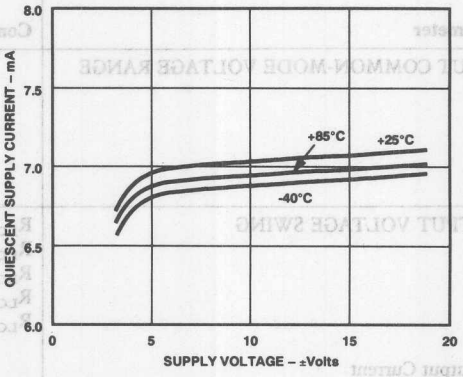


Figure 4. Quiescent Supply Current vs. Supply Voltage for Various Temperatures

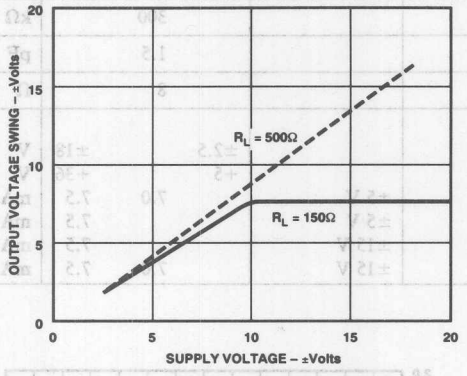


Figure 2. Output Voltage Swing vs. Supply

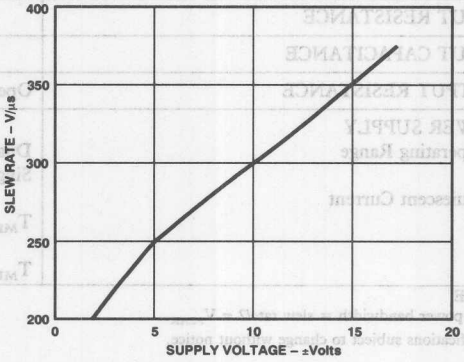


Figure 5. Slew Rate vs. Supply Voltage

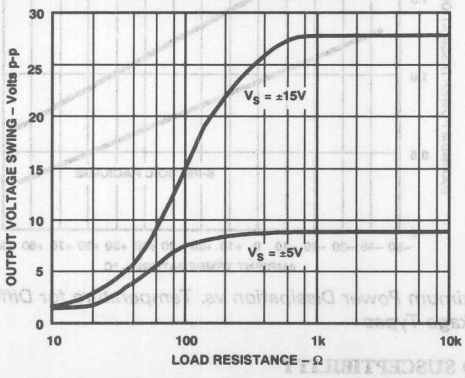


Figure 3. Output Voltage Swing vs. Load Resistance

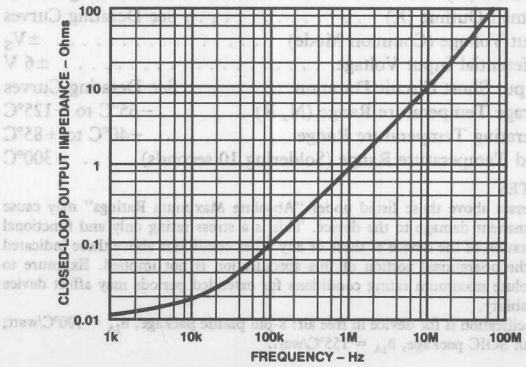


Figure 6. Closed-Loop Output Impedance vs. Frequency

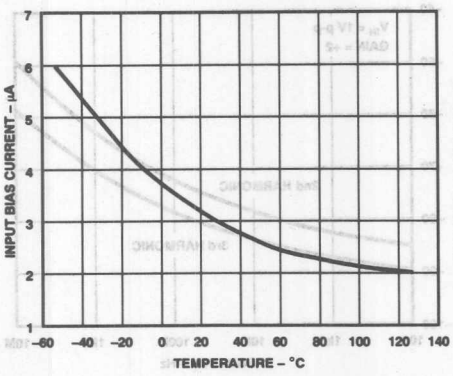


Figure 7. Input Bias Current vs. Temperature

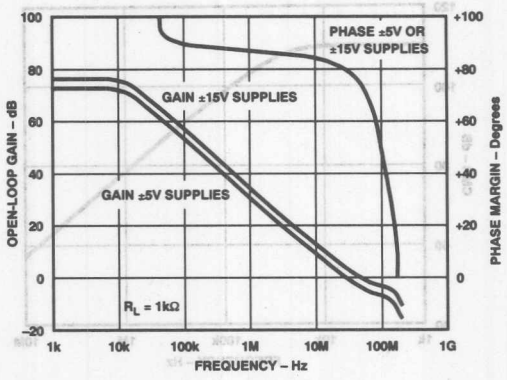


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

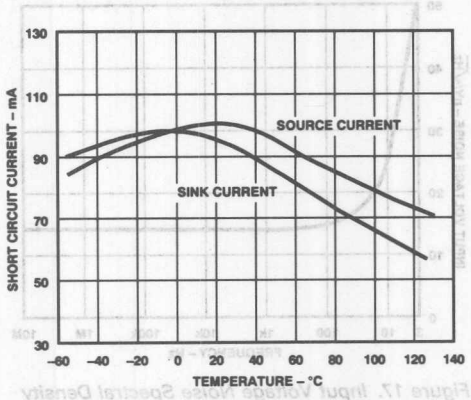


Figure 8. Short Circuit Current vs. Temperature

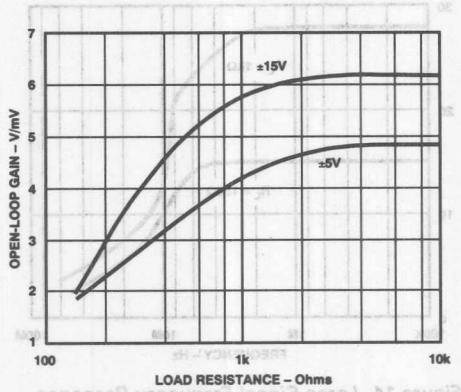


Figure 11. Open Loop Gain vs. Load Resistance

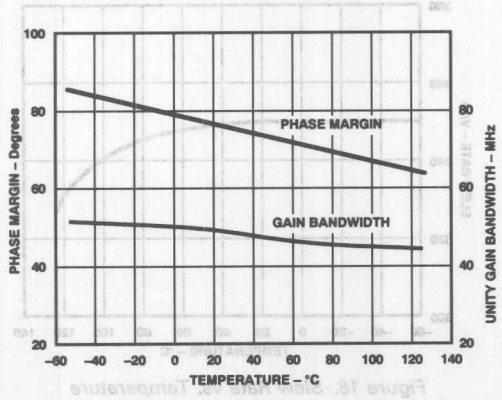


Figure 9. Unity Gain Bandwidth and Phase Margin vs. Temperature

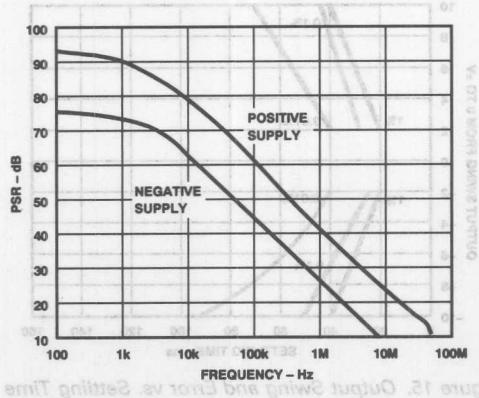


Figure 12. Power Supply Rejection vs. Frequency

AD817 — Typical Characteristics

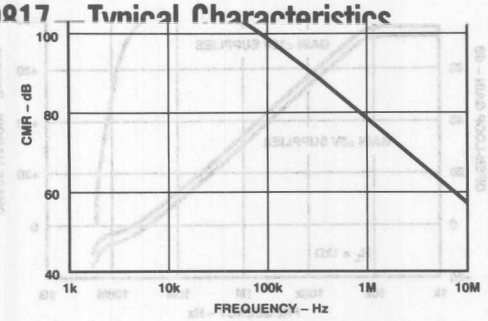


Figure 13. Common-Mode Rejection vs. Frequency

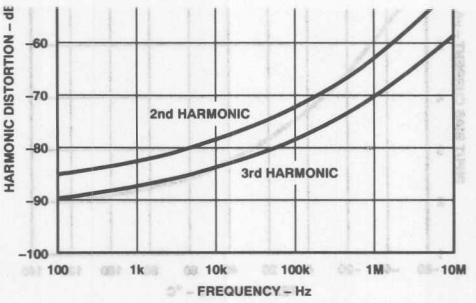


Figure 16. Harmonic Distortion vs. Frequency

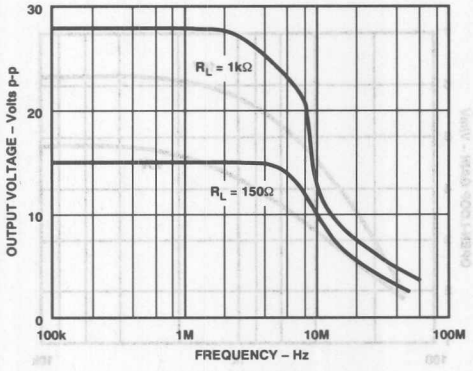


Figure 14. Large Signal Frequency Response

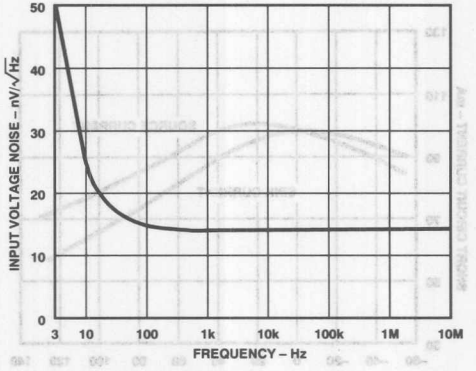


Figure 17. Input Voltage Noise Spectral Density

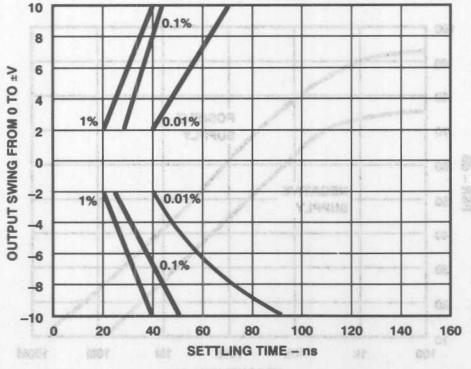


Figure 15. Output Swing and Error vs. Settling Time

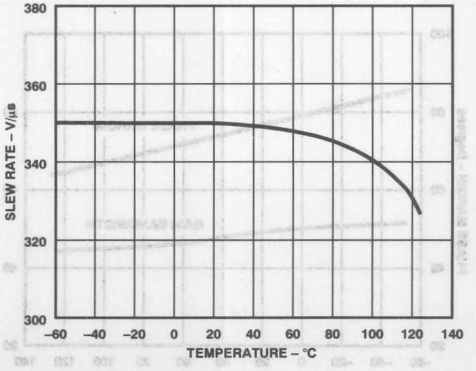


Figure 18. Slew Rate vs. Temperature

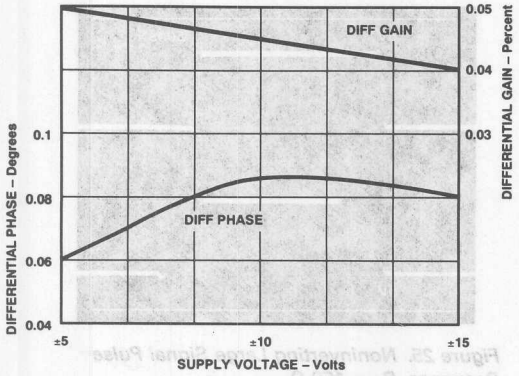


Figure 19. Differential Gain and Phase vs. Supply Voltage

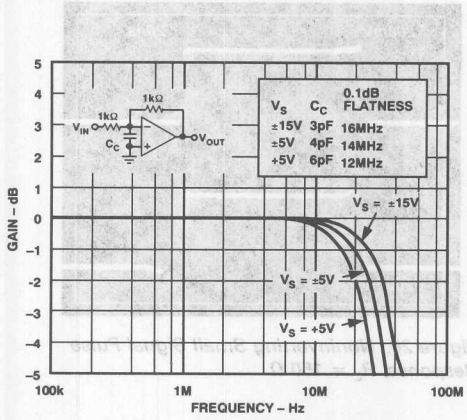


Figure 20. Closed-Loop Gain vs. Frequency, Gain = −1

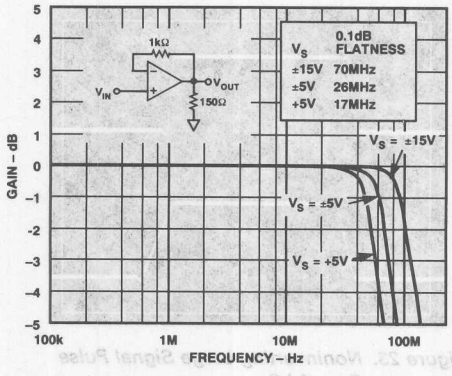


Figure 21. Closed-Loop Gain vs. Frequency, Gain = +1

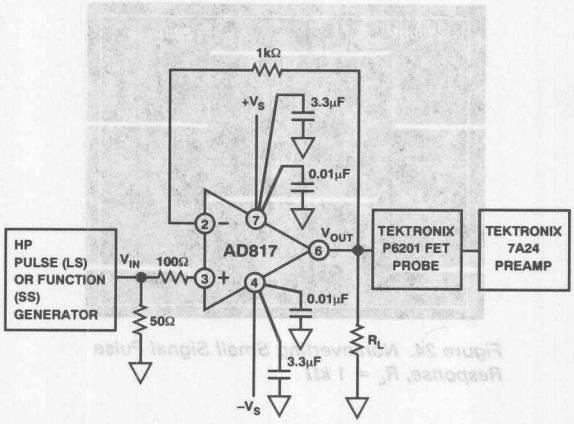


Figure 22. Noninverting Amplifier Connection

9

AD817—Typical Characteristics

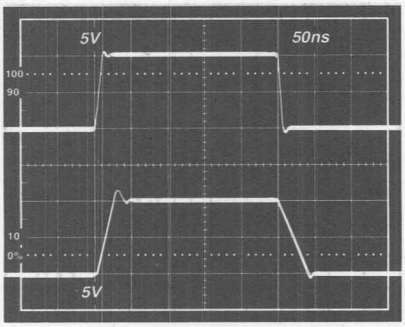


Figure 23. Noninverting Large Signal Pulse Response, R_L = 1 kΩ

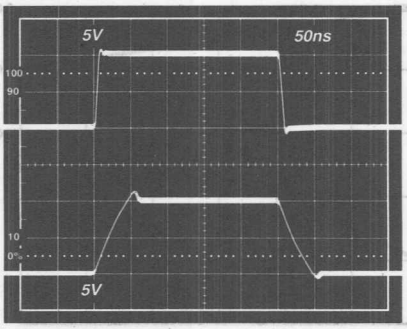


Figure 25. Noninverting Large Signal Pulse Response, R_L = 150 Ω

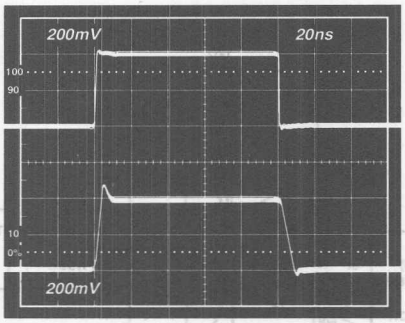


Figure 24. Noninverting Small Signal Pulse Response, R_L = 1 kΩ

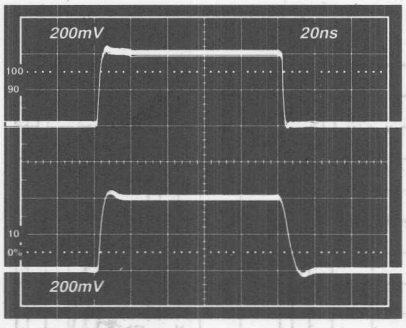


Figure 26. Noninverting Small Signal Pulse Response, R_L = 150 Ω

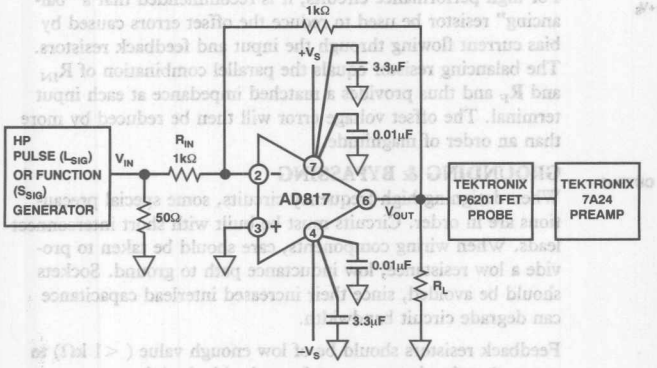


Figure 27. Inverting Amplifier Connection

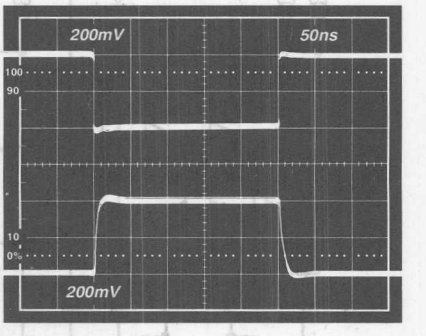


Figure 29. Inverting Small Signal Pulse Response, R_L = 1 kΩ

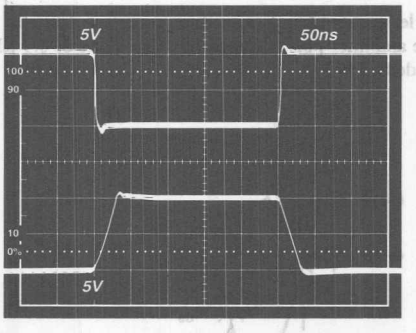


Figure 28. Inverting Large Signal Pulse Response, R_L = 1 kΩ

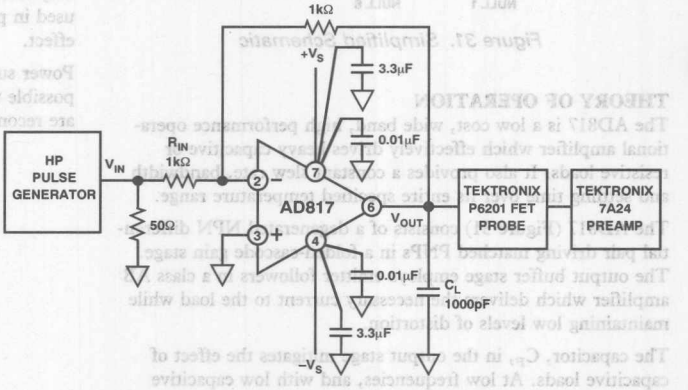


Figure 30a. Inverting Amplifier Driving a 1000 pF Capacitive Load

DRIVING CAPACITIVE LOADS

The internal compensation of the AD817, together with its high output current drive, permit excellent large signal performance while driving extremely high capacitive loads.

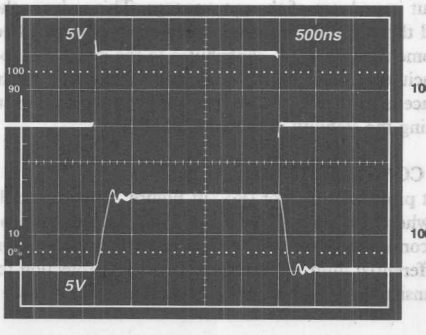


Figure 30b. Inverting Amplifier Pulse Response While Driving Capacitive Loads

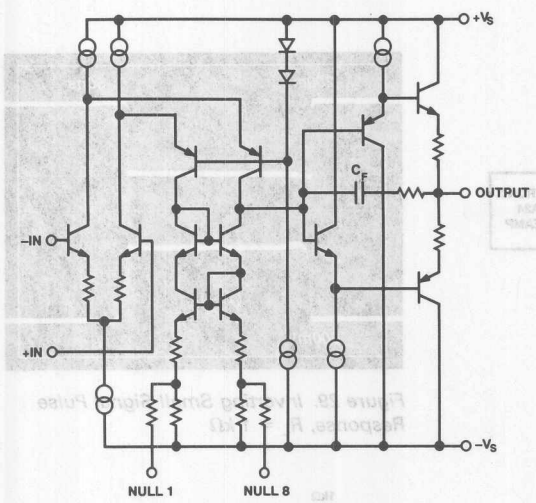


Figure 31. Simplified Schematic

THEORY OF OPERATION

The AD817 is a low cost, wide band, high performance operational amplifier which effectively drives heavy capacitive or resistive loads. It also provides a constant slew rate, bandwidth and settling time over its entire specified temperature range.

The AD817 (Figure 31) consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which delivers the necessary current to the load while maintaining low levels of distortion.

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. At low frequencies, and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, C_F is bootstrapped and does not contribute to the overall compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is incompletely bootstrapped. Effectively, some fraction of C_F contributes to the overall compensation capacitance, reducing the unity gain bandwidth. As the load capacitance is further increased, the bandwidth continues to fall, maintaining the stability of the amplifier.

INPUT CONSIDERATIONS

An input protection resistor (R_{IN} in Figure 22) is required in circuits where the input to the AD817 will be subjected to transient or continuous overload voltages exceeding the +6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a "balancing" resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of R_{IN} and R_F and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

GROUNDING & BYPASSING

When designing high frequency circuits, some special precautions are in order. Circuits must be built with short interconnect leads. When wiring components, care should be taken to provide a low resistance, low inductance path to ground. Sockets should be avoided, since their increased interlead capacitance can degrade circuit bandwidth.

Feedback resistors should be of low enough value (<1 kΩ) to assure that the time constant formed with the inherent stray capacitance at the amplifier's summing junction will not limit performance. This parasitic capacitance, along with the parallel resistance of R_F/R_{IN}, form a pole in the loop transmission which may result in peaking. A small capacitance (1–5 pF) may be used in parallel with the feedback resistor to neutralize this effect.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. Ceramic disc capacitors of 0.1 μF are recommended.

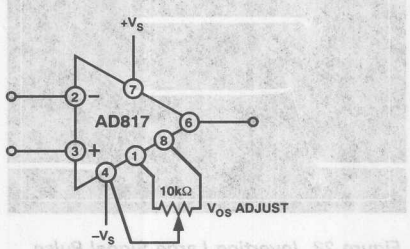


Figure 32. Offset Null Configuration

OFFSET NULLING

The input offset voltage of the AD817 is inherently very low. However, if additional nulling is required, the circuit shown in Figure 32 can be used. The null range of the AD817 in this configuration is ±15 mV.

AD817 SETTLING TIME

Settling time is comprised primarily of two regions. The first is the slew time in which the amplifier is overdriven, where the output voltage rate of change is at its maximum. The second is the linear time period required for the amplifier to settle to within a specified percent of the final value.

Measuring the rapid settling time of AD817 (45 ns to 0.1% and 70 ns to 0.01%—10 V step) requires applying an input pulse with a very fast edge and an extremely flat top. With the AD817 configured in a gain of −1, a clamped false summing junction responds when the output error is within the sum of two diode voltages (≈ 1 volt). The signal is then amplified 20 times by a clamped amplifier whose output is connected directly to a sampling oscilloscope. Figures 33 and 34 show the settling time of the AD817, with a 10 volt step applied.

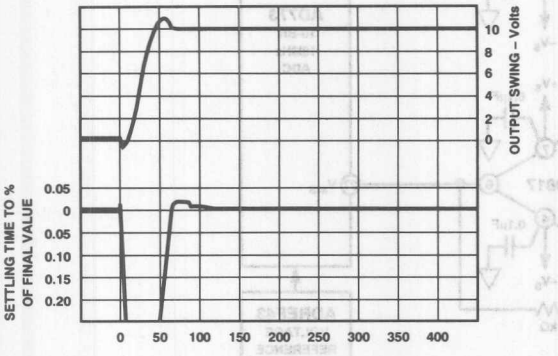


Figure 33. Settling Time in ns 0 V to +10 V

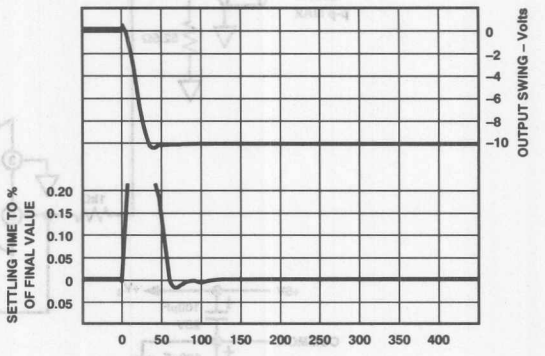


Figure 34. Settling Time in ns 0 V to −10 V

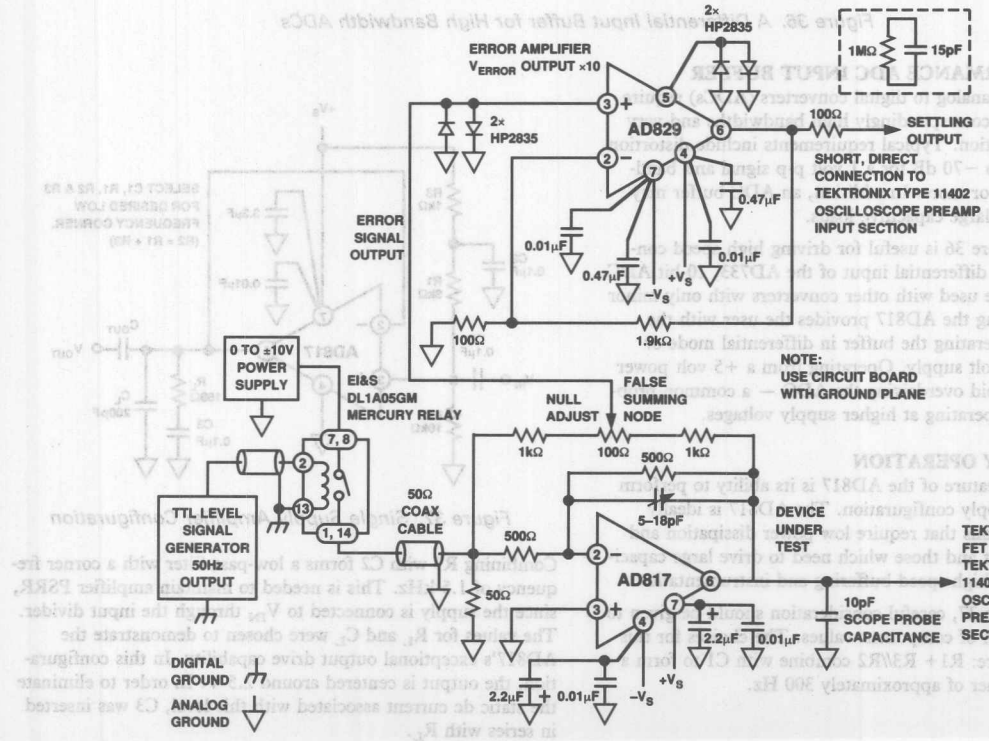


Figure 35. Settling Time Test Circuit

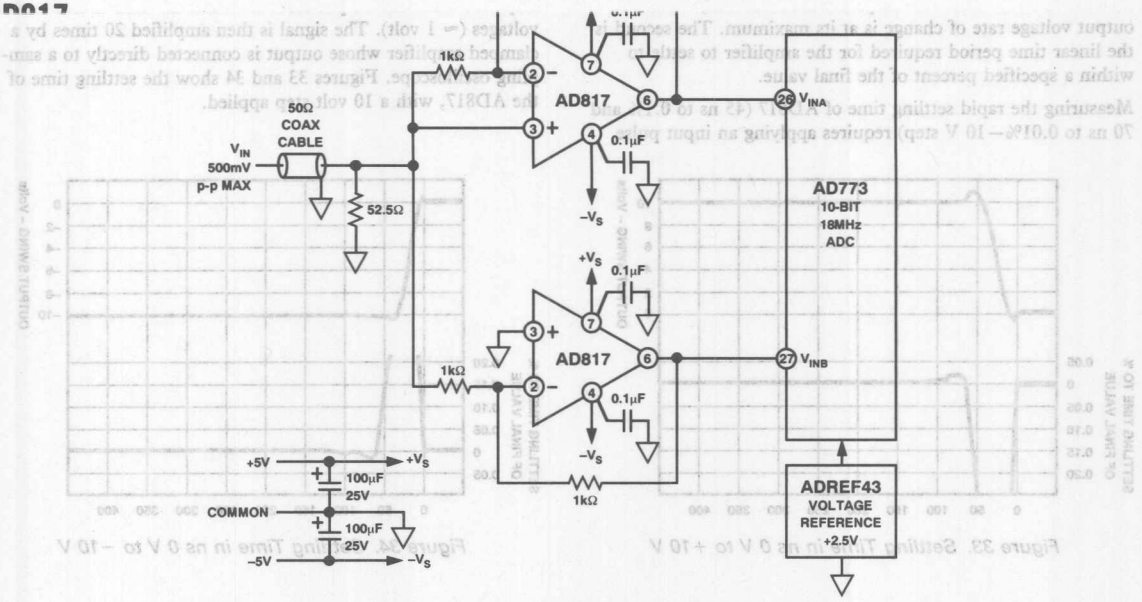


Figure 36. A Differential Input Buffer for High Bandwidth ADCs

A HIGH PERFORMANCE ADC INPUT BUFFER

High performance analog to digital converters (ADCs) require input buffers with correspondingly high bandwidths and very low levels of distortion. Typical requirements include distortion levels of −60 dB to −70 dB for a 1 volt p-p signal and bandwidths of 10 MHz or more. In addition, an ADC buffer may need to drive very large capacitive loads.

The circuit of Figure 36 is useful for driving high speed converters such as the differential input of the AD733, 10-bit ADC. This circuit may be used with other converters with only minor modifications. Using the AD817 provides the user with the option of either operating the buffer in differential mode or from a single +5 volt supply. Operating from a +5 volt power supply helps to avoid overdriving the ADC — a common problem with buffers operating at higher supply voltages.

SINGLE SUPPLY OPERATION

Another exciting feature of the AD817 is its ability to perform well in a single supply configuration. The AD817 is ideally suited for applications that require low power dissipation and high output current and those which need to drive large capacitive loads, such as high speed buffering and instrumentation.

Referring to Figure 37, careful consideration should be given to the proper selection of component values. The choices for this particular circuit are: R1+ R3//R2 combine with C1 to form a low frequency corner of approximately 300 Hz.

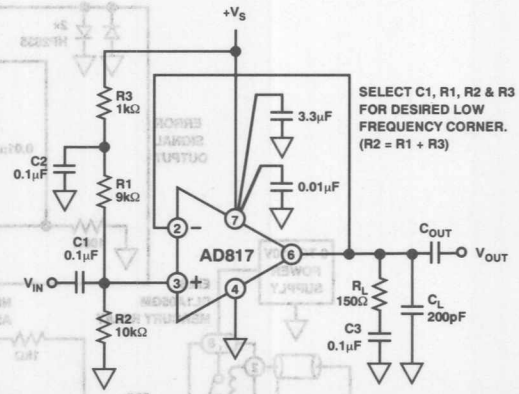


Figure 37. Single Supply Amplifier Configuration

Combining R3 with C2 forms a low-pass filter with a corner frequency of 1.5 kHz. This is needed to maintain amplifier PSRR, since the supply is connected to V_{IN} through the input divider. The values for R_L and C_L were chosen to demonstrate the AD817's exceptional output drive capability. In this configuration, the output is centered around 2.5 V. In order to eliminate the static dc current associated with this level, C3 was inserted in series with R_L.

HIGH SPEED DAC BUFFER

The wide bandwidth and fast settling time of the AD817 make it a very good output buffer for high speed current-output D/A converters like the AD668. As shown in Figure 38, the op amp establishes a summing node at ground for the DAC output. The output voltage is determined by the amplifier's feedback resistor (10.24 V for a 1 kΩ resistor). Note that since the DAC generates a positive current to ground, the voltage at the amplifier output will be negative. A 100 Ω series resistor between the noninverting amplifier input and ground minimizes the offset effects of op amp input bias currents.

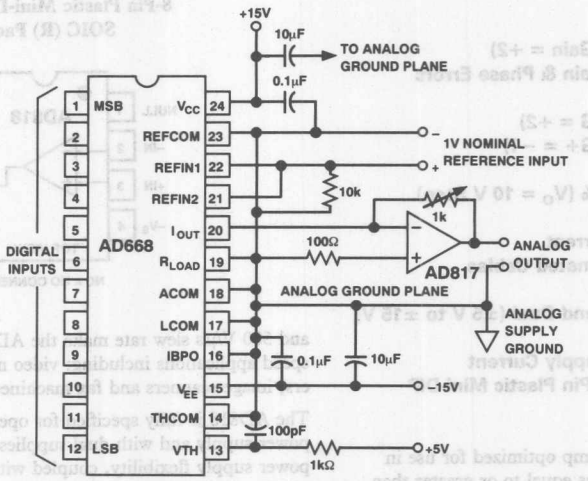


Figure 38. High Speed DAC Buffer

Low Cost, Low Power Video Op Amp

AD818

FEATURES

Low Cost
Excellent Video Performance
- **55 MHz 0.1 dB Bandwidth (Gain = +2)**
- **0.01% & 0.05° Differential Gain & Phase Errors**

High Speed
- **130 MHz Bandwidth (3 dB, G = +2)**
- **100 MHz Bandwidth (3 dB, G+ = −1)**
- **500 V/μs Slew Rate**
- **80 ns Settling Time to 0.01% (V_O = 10 V Step)**

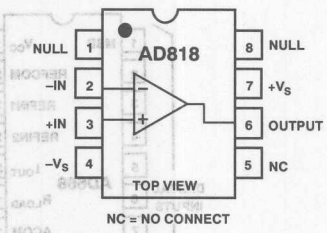
High Output Drive Capability
- **50 mA Minimum Output Current**
- **Ideal for Driving Back Terminated Cables**

Flexible Power Supply
- **Specified for Single (+5 V) and Dual (±5 V to ±15 V) Power Supplies**
- **Low Power: 7.5 mA max Supply Current**

Available in 8-Pin SOIC and 8-Pin Plastic Mini-DIP

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N), and SOIC (R) Packages



NC = NO CONNECT

PRODUCT DESCRIPTION

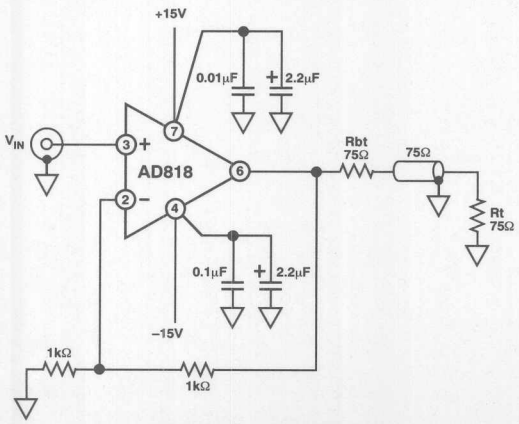
The AD818 is a low cost, video op amp optimized for use in video applications which require gains equal to or greater than +2 or −1. The AD818 low differential gain and phase errors, single supply functionality, low power and high output drive make it ideal for cable driving applications such as video cameras and professional video equipment.

With video specs like 0.1 dB flatness to 55 MHz and low differential gain and phase errors of 0.01% and 0.05°, along with 50 mA of output current, the AD818 is an excellent choice for any video application. The 130 MHz 3 dB bandwidth (G = +2) and 500 V/μs slew rate make the AD818 useful in many high speed applications including: video monitors, CATV, color copiers, image scanners and fax machines.

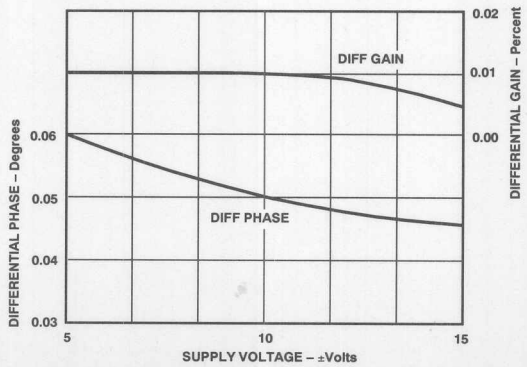
The AD818 is fully specified for operation with a single +5 V power supply and with dual supplies from ±5 V to ±15 V. This power supply flexibility, coupled with a very low supply current of 7.5 mA and excellent ac characteristics under all power supply conditions, make the AD818 the ideal choice for many demanding yet power sensitive applications.

The AD818 is a voltage feedback op amp and excels as a gain stage in high speed and video systems (gain = >2 or −1). It achieves a settling time of 45 ns to 0.1%, with a low input offset voltage of 2 mV max.

The AD818 is available in low cost, small 8-pin plastic mini-DIP and SOIC packages.



AD818 Video Line Driver



AD818 Differential Gain and Phase vs. Supply

SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	V_S	AD818A Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
−3 dB Bandwidth	Gain = +2	±5 V	70	95		MHz
		±15 V	100	130		MHz
		0, +5 V	40	55		MHz
	Gain = −1	±5 V	50	70		MHz
		±15 V	70	100		MHz
		0, +5 V	30	50		MHz
Bandwidth for 0.1 dB Flatness	Gain = +2	±5 V	20	43		MHz
	C_C = 2 pF	±15 V	40	55		MHz
		0, +5 V	10	18		MHz
	Gain = −1	±5 V	18	34		MHz
	C_C = 2 pF	±15 V	40	72		MHz
		0, +5 V	10	19		MHz
Full Power Bandwidth[1]	V_{OUT} = 5 V p-p					
	R_{LOAD} = 500 Ω	±5 V		25.5		MHz
	V_{OUT} = 20 V p-p					
	R_{LOAD} = 1 kΩ	±15 V		8.0		MHz
Slew Rate	R_{LOAD} = 1 kΩ	±5 V	350	400		V/µs
	Gain = −1	±15 V	450	500		V/µs
		0, +5 V	250	300		V/µs
Settling Time to 0.1%	−2.5 V to +2.5 V	±5 V		45		ns
	0 V–10 V Step, A_V = −1	±15 V		45		ns
to 0.01%	−2.5 V to +2.5 V	±5 V		80		ns
	0 V–10 V Step, A_V = −1	±15 V		80		ns
Total Harmonic Distortion	F_C = 1 MHz	±15 V		63		dB
Differential Gain Error	NTSC	±15 V		0.005	0.01	%
(Rl = 150 Ω)	Gain = +2	±5 V		0.01	0.02	%
		0, +5 V		0.08		%
Differential Phase Error	NTSC	±15 V		0.045	0.09	Degrees
(Rl = 150 Ω)	Gain = +2	±5 V		0.06	0.09	Degrees
		0, +5 V		0.1		Degrees
Cap Load Drive				10		pF
INPUT OFFSET VOLTAGE		±5 V to ±15 V		0.5	2	mV
	T_{MIN} to T_{MAX}				3	mV
Offset Drift				10		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	6.6	µA
	T_{MIN}				10	µA
	T_{MAX}				4.4	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		25	200	nA
	T_{MIN} to T_{MAX}				500	nA
Offset Current Drift				0.3		nA/°C
OPEN-LOOP GAIN	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		3	5		V/mV
	T_{MIN} to T_{MAX}		2			V/mV
	R_{LOAD} = 150 Ω		2	4		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		6	9		V/mV
	T_{MIN} to T_{MAX}		3			V/mV
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 150 Ω					
	(50 mA Output)		3	5		V/mV
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	82	100		dB
	V_{CM} = ±12 V	±15 V	86	120		dB
	T_{MIN} to T_{MAX}	±15 V	84	100		dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		80	90		dB
	T_{MIN} to T_{MAX}		80			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±5 V, ±15 V		10		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±5 V, ±15 V		1.5		pA/√Hz

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Parameter	Conditions	V_S	AD818A Min	Typ	Max	Units
INPUT COMMON-MODE VOLTAGE RANGE		±5 V	+3.8	+4.3		V
			−2.7	−3.4		V
		±15 V	+13	+14.3		V
			−12	−13.4		V
		0, +5 V	+3.8	+4.3		V
			+1.2	+0.9		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.3	3.8		±V
	R_{LOAD} = 150 Ω	±5 V	3.2	3.6		±V
	R_{LOAD} = 1 kΩ	±15 V	13.3	13.7		±V
	R_{LOAD} = 500 Ω	±15 V	12.8	13.4		±V
	R_{LOAD} = 500 Ω	0, +5 V	+1.5, +3.5			V
Output Current		±15 V	50			mA
		±5 V	50			mA
		0, +5 V	30			mA
Short-Circuit Current		±15 V		90		mA
INPUT RESISTANCE				300		kΩ
INPUT CAPACITANCE				1.5		pF
OUTPUT RESISTANCE	Open Loop			8		Ω
POWER SUPPLY						
Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current		±5 V		7.0	7.5	mA
	T_{MIN} to T_{MAX}	±5 V			7.5	mA
		±15 V			7.5	mA
	T_{MIN} to T_{MAX}	±15 V		7.0	7.5	mA

NOTE
[1]Full power bandwidth = slew rate/2 π V_{PEAK}.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

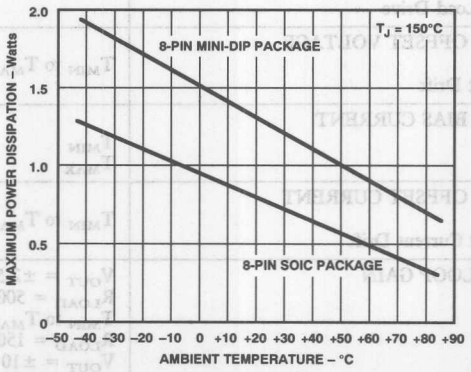
Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . See Derating Curves
Small Outline (R) . . . . . See Derating Curves
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Output Short Circuit Duration . . . . . See Derating Curves
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 10 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air: 8-pin plastic package, θ_{JA} = 90°C/watt; 8-pin SOIC package, θ_{JA} = 155°C/watt.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD818AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD818AR	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD818AR-REEL	−40°C to +85°C	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.



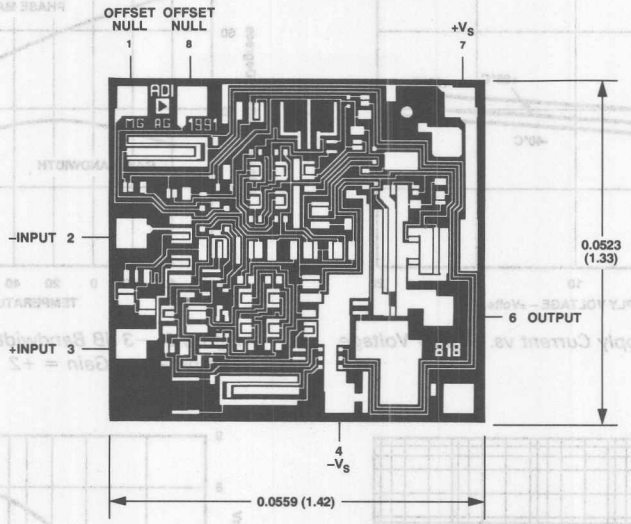
Maximum Power Dissipation vs. Temperature for Different Package Types

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD817 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



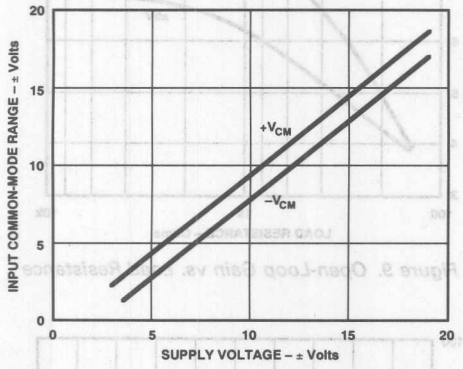


Figure 1. Common-Mode Voltage Range vs. Supply

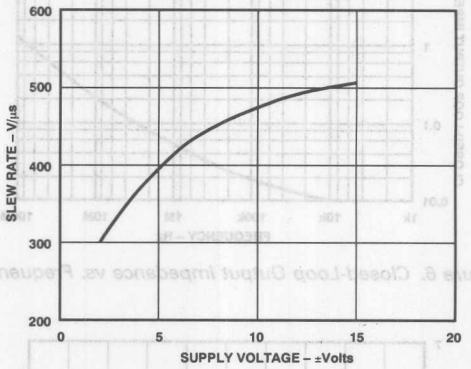


Figure 3. Slew Rate vs. Supply Voltage

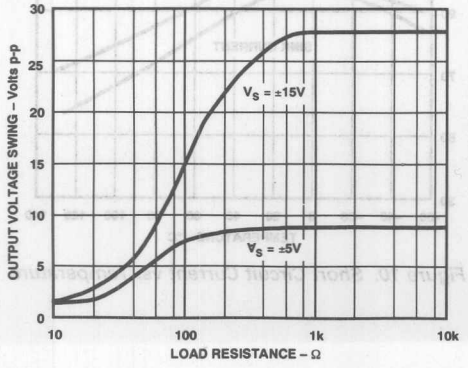


Figure 2. Output Voltage Swing vs. Load Resistance

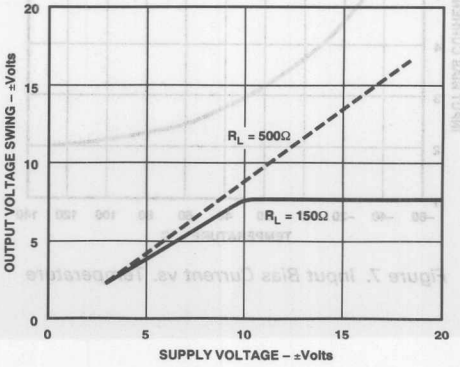


Figure 4. Output Voltage Swing vs. Supply

AD818 —Typical Characteristics

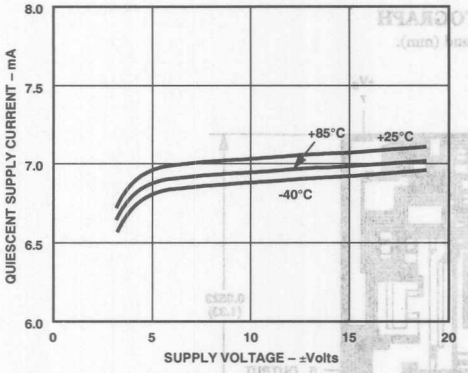


Figure 5. Quiescent Supply Current vs. Supply Voltage

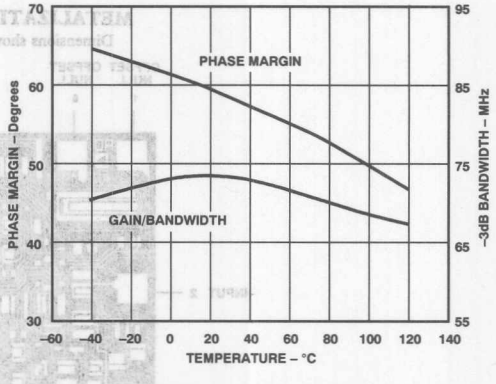


Figure 8. −3 dB Bandwidth and Phase Margin vs. Temperature. Gain = +2

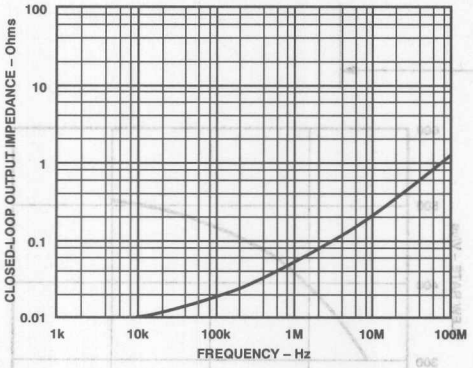


Figure 6. Closed-Loop Output Impedance vs. Frequency

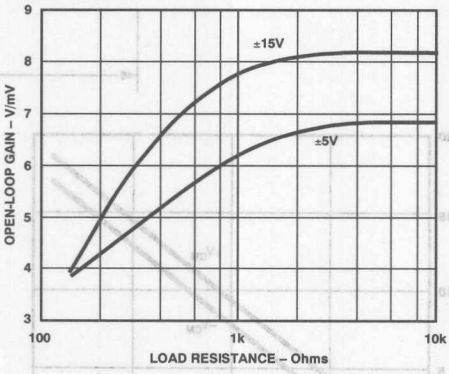


Figure 9. Open-Loop Gain vs. Load Resistance

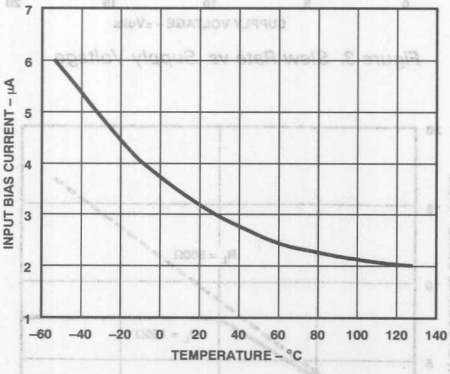


Figure 7. Input Bias Current vs. Temperature

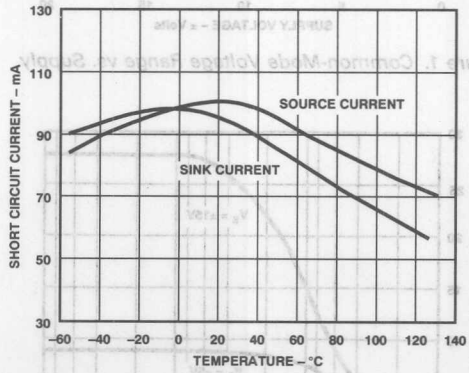


Figure 10. Short Circuit Current vs. Temperature

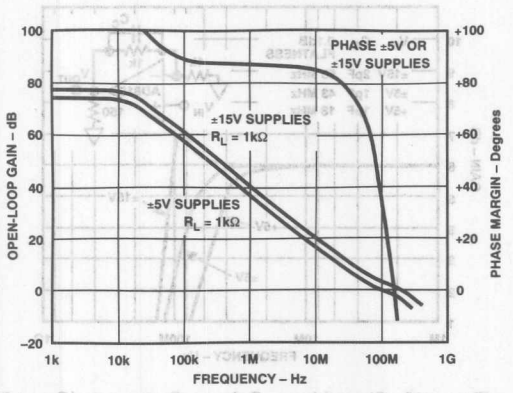


Figure 11. Open-Loop Gain and Phase Margin vs. Frequency

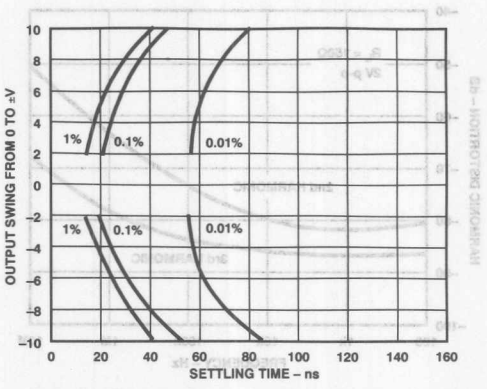


Figure 14. Output Swing and Error vs. Settling Time

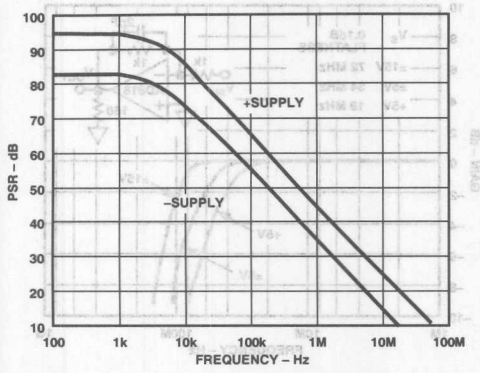


Figure 12. Power Supply Rejection vs. Frequency

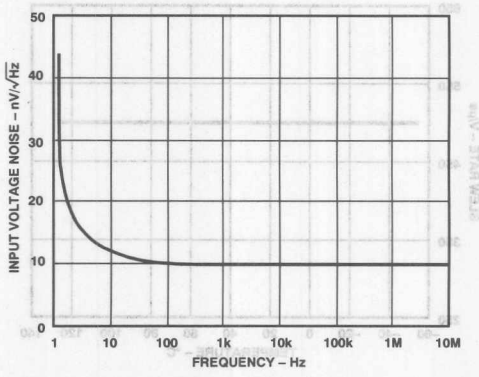


Figure 15. Input Voltage Noise Spectral Density vs. Frequency

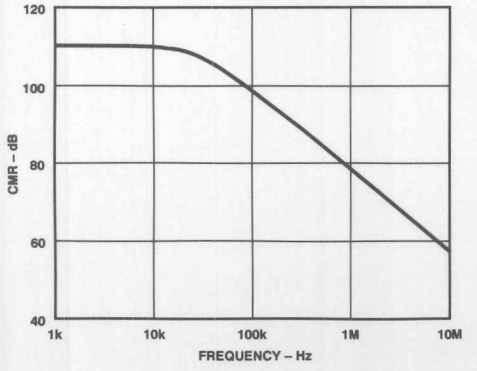


Figure 13. Common-Mode Rejection vs. Frequency

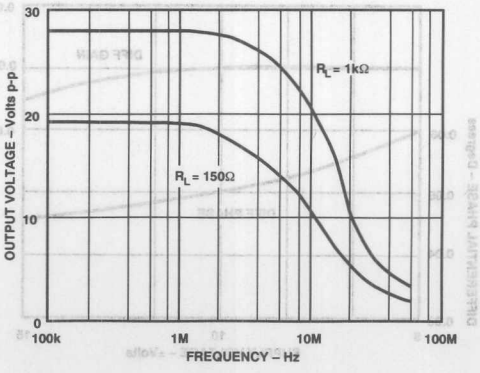


Figure 16. Output Voltage vs. Frequency

AD818—Typical Characteristics

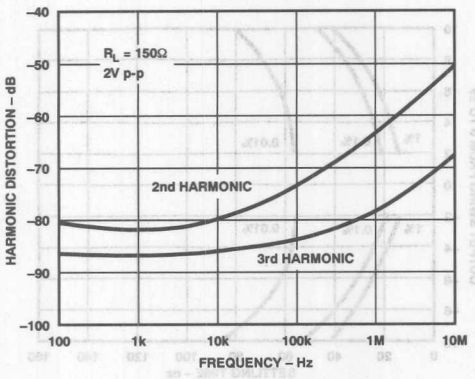


Figure 17. Harmonic Distortion vs. Frequency

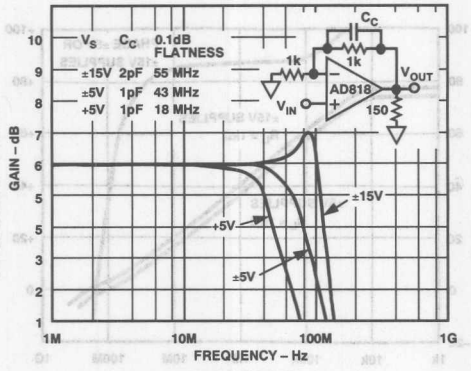


Figure 20. Closed-Loop Gain vs. Frequency (G = +2)

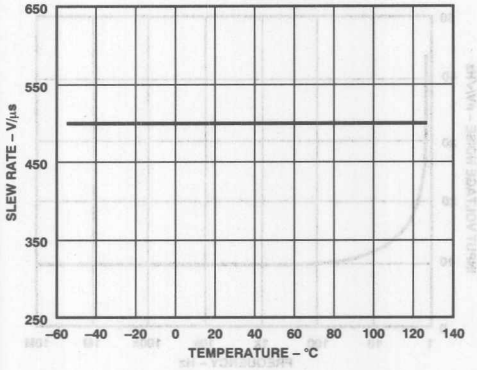


Figure 18. Slew Rate vs. Temperature

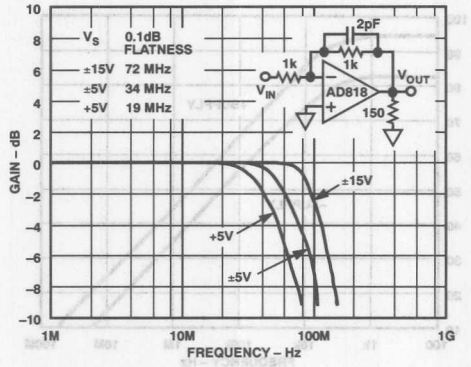


Figure 21. Closed-Loop Gain vs. Frequency (G = –1)

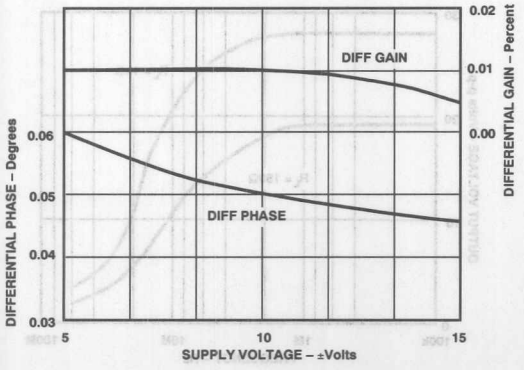


Figure 19. Differential Gain and Phase vs. Supply Voltage

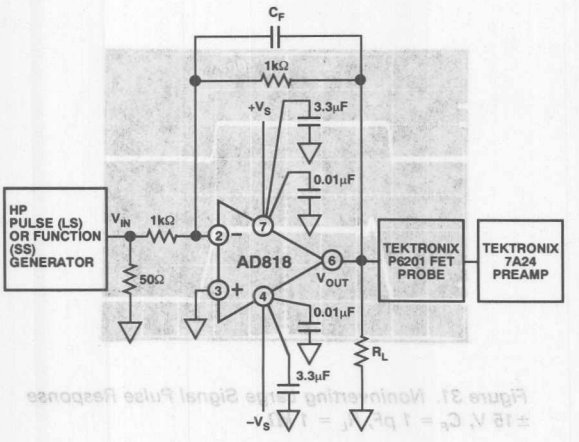


Figure 22. Inverting Amplifier Connection

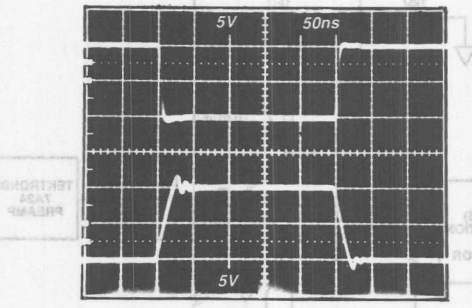


Figure 25. Inverter Large Signal Pulse Response ±15 V_S, C_F = 1 pF, R_L = 1 kΩ

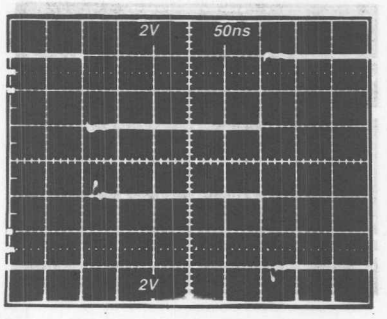


Figure 23. Inverter Large Signal Pulse Response ±5 V_S, C_F = 1 pF, R_L = 1 kΩ

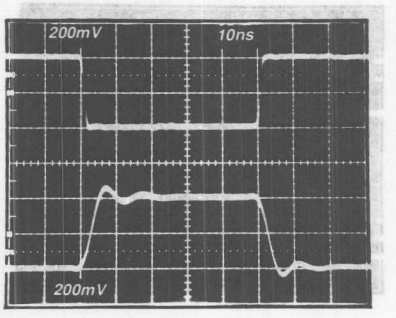


Figure 26. Inverter Small Signal Pulse Response ±15 V_S, C_F = 1 pF, R_L = 150 Ω

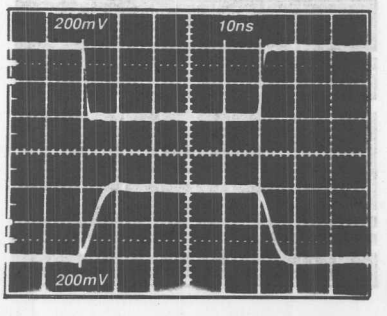


Figure 24. Inverter Small Signal Pulse Response ±5 V_S, C_F = 1 pF, R_L = 150 Ω

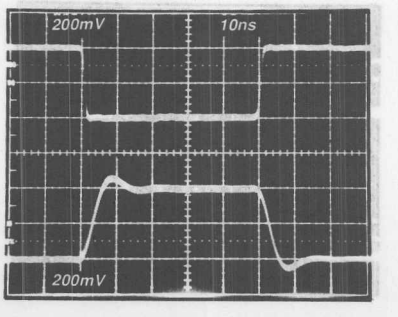


Figure 27. Inverter Small Signal Pulse Response ±5 V_S, C_F = 0 pF, R_L = 150 Ω

AD818—Typical Characteristics

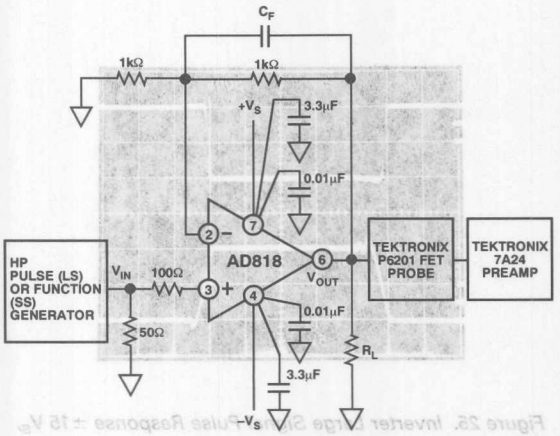


Figure 28. Noninverting Amplifier Connection

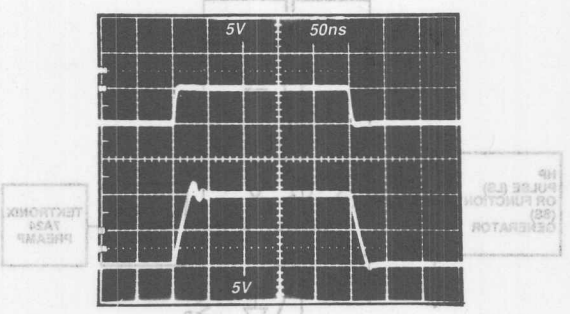


Figure 31. Noninverting Large Signal Pulse Response ±15 V, C_F = 1 pF, R_L = 1 kΩ

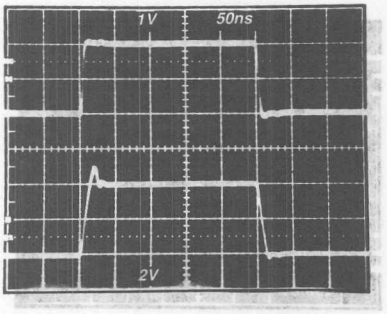


Figure 29. Noninverting Large Signal Pulse Response ±5 V, C_F = 1 pF, R_L = 1 kΩ

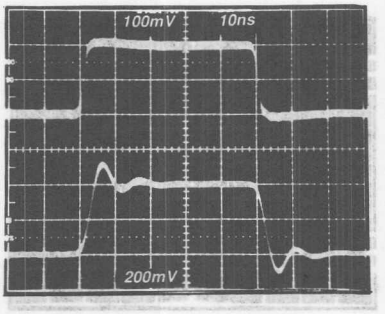


Figure 32. Noninverting Small Signal Pulse Response ±15 V, C_F = 1 pF, R_L = 150 Ω

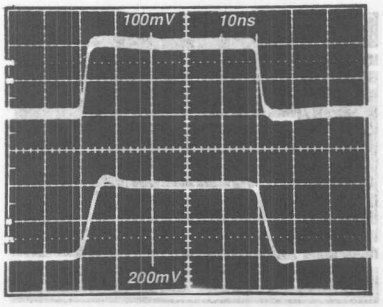


Figure 30. Noninverting Small Signal Pulse Response ±5 V, C_F = 1 pF, R_L = 150 Ω

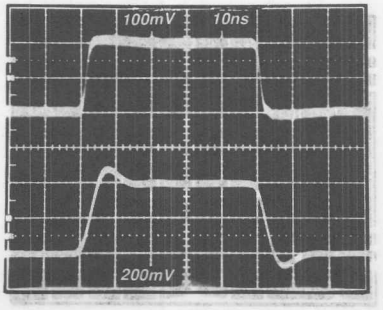


Figure 33. Noninverting Small Signal Pulse Response ±5 V, C_F = 0 pF, R_L = 150 Ω

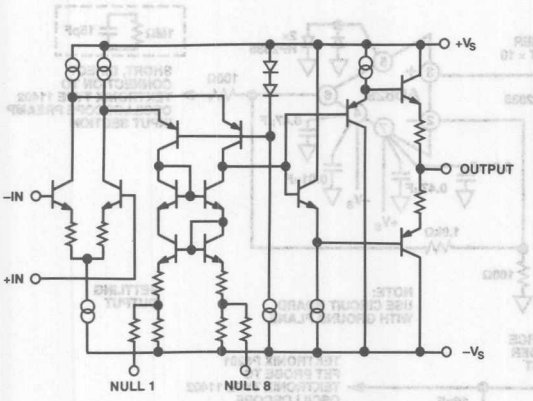


Figure 34. AD818 Simplified Schematic

THEORY OF OPERATION

The AD818 is a low cost, video operational amplifier designed to excel in high performance, high output current video applications.

The AD818 (Figure 34) consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which delivers the necessary current to the load, while maintaining low levels of distortion.

The AD818 will drive terminated cables and capacitive loads of 10 pF or less. As the closed-loop gain is increased, the AD818 will drive heavier cap loads without oscillating.

INPUT CONSIDERATIONS

An input protection resistor (R_{IN} in Figure 28) is required in circuits where the input to the AD818 will be subjected to transient of continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a "balancing" resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of R_{IN} and R_F and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

GROUNDING AND BYPASSING

When designing high frequency circuits, some special precautions are in order. Circuits must be built with short interconnect leads. When wiring components, care should be taken to provide a low resistance, low inductance path to ground. Sockets should be avoided, since their increased interlead capacitance can degrade circuit bandwidth.

Feedback resistors should be of low enough value (≤1 kΩ) to assure that the time constant formed with the inherent stray capacitance at the amplifier's summing junction will not limit performance. This parasitic capacitance, along with the parallel resistance of R_F/R_{IN}, form a pole in the loop transmission which may result in peaking. A small capacitance (1–5 pF) may be used in parallel with the feedback resistor to neutralize this effect.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. Ceramic disc capacitors of 0.1 μF are recommended.

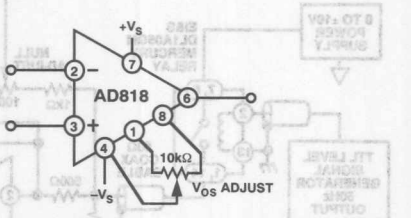


Figure 35. Offset Null Configuration

OFFSET NULLING

The input offset voltage of the AD818 is inherently very low. However, if additional nulling is required, the circuit shown in Figure 35 can be used. The null range of the AD818 in this configuration is ±10 mV.

SINGLE SUPPLY OPERATION

Another exciting feature of the AD818 is its ability to perform well in a single supply configuration. The AD818 is ideally suited for applications that require low power dissipation and high output current.

Referring to Figure 36, careful consideration should be given to the proper selection of component values. The choices for this particular circuit are: R1 + R3||R2 combine with C1 to form a low frequency corner of approximately 10 kHz. C4 was inserted in series with R4 to maintain amplifier stability at high frequency.

Combining R3 with C2 forms a low pass filter with a corner frequency of approximately 500 Hz. This is needed to maintain amplifier PSRR, since the supply is connected to V_{IN} through the input divider. The values for R2 and C2 were chosen to demonstrate the AD818's exceptional output drive capability. In this configuration, the output is centered around 2.5 V. In order to eliminate the static dc current associated with this level, C3 was inserted in series with R_L.

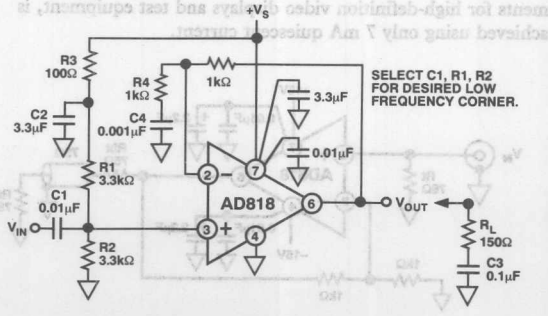


Figure 36. Single Supply Amplifier Configuration

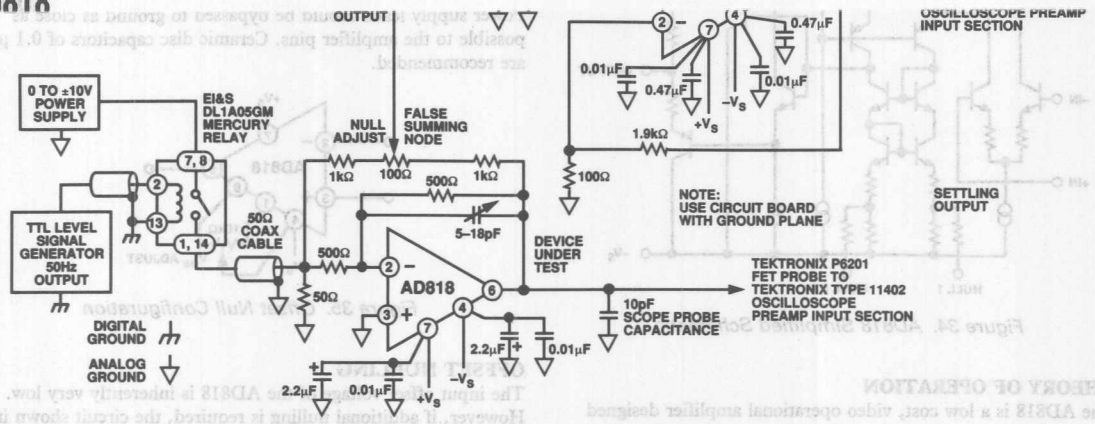


Figure 37. Settling Time Test Circuit

AD818 SETTLING TIME

Settling time is comprised primarily of two regions. The first is the slew time in which the amplifier is overdriven, where the output voltage rate of change is at its maximum. The second is the linear time period required for the amplifier to settle to within a specified percent of the final value.

Measuring the rapid settling time of AD818 (45 ns to 0.1% and 80 ns to 0.01%—10 V step) requires applying an input pulse with a very fast edge and an extremely flat top. With the AD818 configured in a gain of −1, a clamped false summing junction responds when the output error is within the sum of two diode voltages (approximately 1 volt). The signal is then amplified 20 times by a clamped amplifier whose output is connected directly to a sampling oscilloscope.

A High Performance Video Line Driver

The buffer circuit shown in Figure 38 will drive a back-terminated 75 Ω video line to standard video levels (1 V p-p) with 0.1 dB gain flatness to 55 MHz with only 0.05° and 0.01% differential phase and gain at the 3.58 MHz NTSC subcarrier frequency. This level of performance, which meets the requirements for high-definition video displays and test equipment, is achieved using only 7 mA quiescent current.

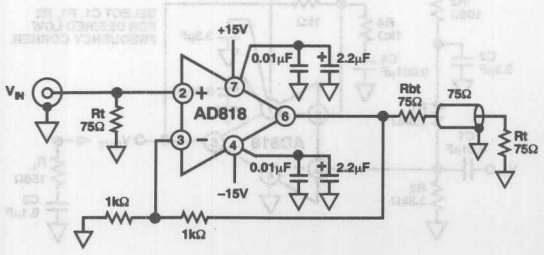


Figure 38. Video Line Driver

DIFFERENTIAL LINE RECEIVER

The differential receiver circuit of Figure 39 is useful for many applications from audio to video. It allows extraction of a low level signal in the presence of common-mode noise. As shown in Figure 40, the AD818 provides this function with only 10nV/$\sqrt{\text{Hz}}$ noise at the output.

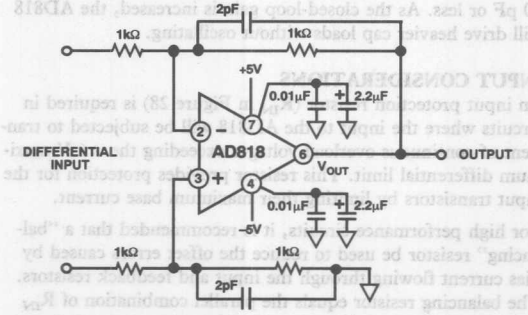


Figure 39. Differential Line Receiver

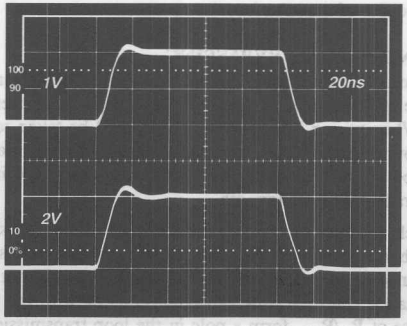
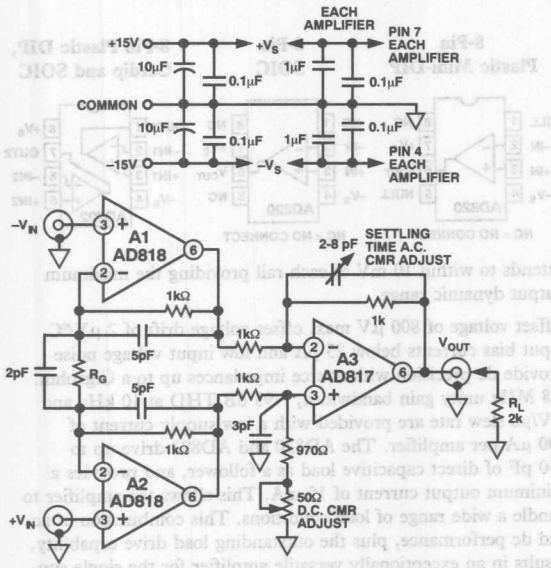


Figure 40. Performance of Line Receiver, R_L = 150 Ω, G = +2

A HIGH SPEED, THREE OP AMP IN AMP

The circuit of Figure 41 uses three high speed op amps: two AD818s and an AD817. This high speed circuit lends itself well to CCD imaging and other video speed applications. It has the optional flexibility of both dc and ac trims for common-mode rejection, plus the ability to adjust for minimum settling time.



BANDWIDTH, SETTLING TIME, & TOTAL HARMONIC DISTORTION VS. GAIN

GAIN	R_G	CADJ (pF)	SMALL SIGNAL BANDWIDTH	SETTLING TIME TO 0.1%	THD + NOISE BELOW INPUT LEVEL @ 10kHz
3	1k	2-8	14.7 MHz	200ns	82 dB
10	222Ω	2-8	4.5 MHz	370ns	81 dB
100	20Ω	2-8	960 kHz	2.5µs	71 dB

Figure 41. High Speed 3 Op Amp In Amp

All brand or product names mentioned are trademarks or registered trademarks of their respective holders.

Single Supply, Rail-to-Rail Low Power FET-Input Op Amps

AD820/AD822

FEATURES

TRUE SINGLE SUPPLY OPERATION
- Output Swings Rail to Rail
- Input Voltage Range Extends Below Ground
- Single Supply Capability from +3 V to +36 V
- Dual Supply Capability from ±1.5 V to ±18 V

HIGH LOAD DRIVE
- Capacitive Load Drive of 350 pF, G = 1
- Minimum Output Current of 15 mA

EXCELLENT AC PERFORMANCE FOR LOW POWER
- 800 μA Max Quiescent Current per Amplifier
- Unity Gain Bandwidth: 1.8 MHz
- Slew Rate of 3.0 V/μs

GOOD DC PERFORMANCE
- 800 μV Max Input Offset Voltage
- 2 μV/°C Typ Offset Voltage Drift
- 25 pA Max Input Bias Current

LOW NOISE
- 13 nV/$\sqrt{Hz}$ @ 10 kHz

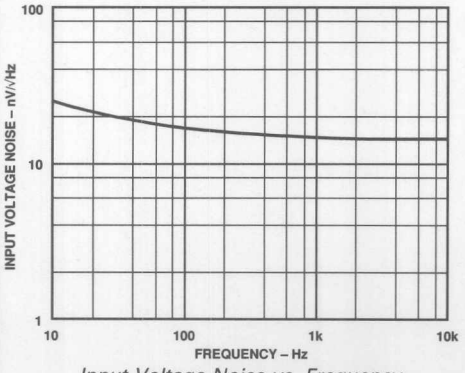
NO PHASE INVERSION

APPLICATIONS

Battery Powered Precision Instrumentation
Photodiode Preamps
Active Filters
12- to 14-Bit Data Acquisition Systems
Medical Instrumentation
Low Power References and Regulators

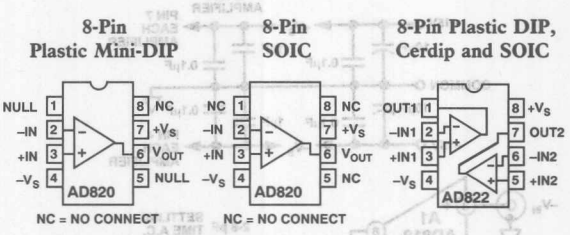
PRODUCT DESCRIPTION

The AD820/AD822 are precision, low power FET input op amps that can operate from a single supply of +3.0 V to +36 V, or dual supplies of ±1.5 V to ±18 V. They have true single supply capability with an input voltage range extending below the negative rail, allowing them to accommodate input signals below ground in the single supply mode. Output voltage swing extends to within 10 mV of each rail providing the maximum output dynamic range.



Input Voltage Noise vs. Frequency

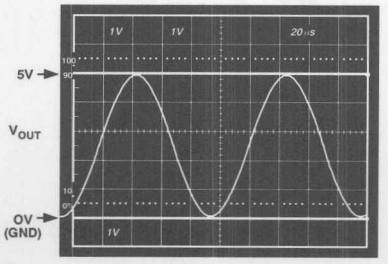
CONNECTION DIAGRAMS



Offset voltage of 800 μV max, offset voltage drift of 2 μV/°C, input bias currents below 25 pA and low input voltage noise provide dc precision with source impedances up to a Gigaohm. 1.8 MHz unity gain bandwidth, −93 dB THD at 10 kHz and 3 V/μs slew rate are provided with a low supply current of 800 μA per amplifier. The AD820 and AD822 drive up to 350 pF of direct capacitive load as a follower, and provides a minimum output current of 15 mA. This allows the amplifier to handle a wide range of load conditions. This combination of ac and dc performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for the single supply user.

The AD820 and AD822 are available in four performance grades. The A and B grades are rated over the industrial temperature range of −40°C to +85°C. There is a 3 volt grade—the AD820A-3V or AD822A-3V, rated over the industrial temperature range. The AD822 is also available in a mil grade, is rated over the military temperature range of −55°C to +125°C, and is processed on a standard military drawing.

The AD820 is offered in 8-pin plastic DIP and SOIC packaging while the AD822 is offered in three varieties of 8-pin package: plastic DIP, hermetic cerdip and surface mount (SOIC) as well as die form.



Gain of +2 Amplifier; V_S = +5, 0, V_{IN} = 2.5 V Sine Centered at 1.25 Volts, R_L = 100 kΩ

SPECIFICATIONS

(V_S = 0, 5 V @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted)

Parameter	Conditions	AD820A/AD822A Min	AD820A/AD822A Typ	AD820A/AD822A Max	AD820B/AD822B Min	AD820B/AD822B Typ	AD820B/AD822B Max	AD822S[1] Min	AD822S[1] Typ	AD822S[1] Max	Units
DC PERFORMANCE											
Initial Offset			0.1	0.8		0.1	0.4		0.1	0.8	mV
Max Offset over Temperature			0.5	1.2		0.5	0.9		0.5		mV
Offset Drift			2.0			2.0			2.0		µV/°C
Input Bias Current	V_{CM} = 0 V to 4 V		2	25		2	10		2	25	pA
at T_{MAX}			0.5	5		0.5	2.5		0.5		nA
Input Offset Current			2	20		2	10		2	20	pA
at T_{MAX}			0.5			0.5			1.5		nA
Open-Loop Gain	V_O = 0.2 V to 4 V										
	R_L = 100 kΩ (AD820)	400	1000		400	1000					V/mV
	R_L = 100 kΩ (AD822)	500	1000		500	1000		500	1000		V/mV
T_{MIN} to T_{MAX}	R_L = 100 kΩ	400			400						V/mV
	R_L = 10 kΩ	80	150		80	150		80	150		V/mV
T_{MIN} to T_{MAX}	R_L = 10 kΩ	80			80						V/mV
	R_L = 1 kΩ	15	30		15	30		15	30		V/mV
T_{MIN} to T_{MAX}	R_L = 1 kΩ	10			10						V/mV
NOISE/HARMONIC PERFORMANCE											
Input Voltage Noise											
	0.1 Hz to 10 Hz		2			2			2		µV p-p
	f = 10 Hz		25			25			25		nV/√Hz
	f = 100 Hz		21			21			21		nV/√Hz
	f = 1 kHz		16			16			16		nV/√Hz
	f = 10 kHz		13			13			13		nV/√Hz
Input Current Noise	0.1 Hz to 10 Hz		18			18			18		fA p-p
	f = 1 kHz		0.8			0.8			0.8		fA /√Hz
Harmonic Distortion	R_L = 10 kΩ										
f = 10 kHz	V_O = 0.25 V to 4.75 V		−93			−93			−93		dB
DYNAMIC PERFORMANCE											
Unity Gain Frequency			1.8			1.8			1.8		MHz
Full Power Response	V_O p-p = 4.5 V		210			210			210		kHz
Slew Rate			3			3			3		V/µs
Settling Time											
to 0.1%	V_O = 0.2 V to 4.5 V		1.4			1.4			1.4		µs
to 0.01%			1.8			1.8			1.8		µs
MATCHING CHARACTERISTICS	AD822 Only										
Initial Offset				1.0			0.5			1.6	mV
Max Offset over Temperature				1.6			1.3				mV
Offset Drift			3			3			3		µV/°C
Input Bias Currents				20			10			20	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ		−130			−130			−130		dB
f = 100 kHz			−93			−93			−93		dB
INPUT CHARACTERISTICS											
Common-Mode Voltage Range[2]		−0.2		4	−0.2		4	−0.2		4	V
T_{MIN} to T_{MAX}		−0.2		4	−0.2		4				V
CMRR (AD820)	V_{CM} = 0 V to +2 V	66	80		72	80					dB
CMRR (AD822)	V_{CM} = 0 V to +2 V	66	80		69	80		66	80		dB
T_{MIN} to T_{MAX}		66			66						dB
Input Impedance											
Differential			$10^{13}\|0.5$			$10^{13}\|0.5$			$10^{13}\|0.5$		Ω|pF
Common Mode			$10^{13}\|2.8$			$10^{13}\|2.8$			$10^{13}\|2.8$		Ω|pF
OUTPUT CHARACTERISTICS											
Output Saturation Voltage[3]											
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10				mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20				mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80				mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160				mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000				mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900				mV
Operating Output Current		15			15			15			mA
T_{MIN} to T_{MAX}		12			12						mA
Short Circuit Current			25			25			25		mA
Capacitive Load Drive			350			350			350		pF
POWER SUPPLY											
Quiescent Current/Amplifier			620	800		620	800		620		µA
	T_{MIN} to T_{MAX}			800			800				µA
Power Supply Rejection		70	80		66	80		70	80		dB
	T_{MIN} to T_{MAX}	70			66						dB

9

Initial Offset			0.1	0.8		0.1	0.4		0.1		mV
Max Offset over Temperature			0.5	1.5		0.5	1		0.5		mV
Offset Drift			2.0			2.0			2.0		μV/°C
Input Bias Current	V_{CM} = −5 V to 4 V		2	25		2	10		2	25	pA
at T_{MAX}			0.5	5		0.5	2.5		0.5		nA
Input Offset Current			2	20		2	10		2		pA
at T_{MAX}			0.5			0.5			1.5		nA
Open-Loop Gain	V_O = −4 V to 4 V										
	R_L = 100 kΩ	400	1000		400	1000		400	1000		V/mV
T_{MIN} to T_{MAX}	R_L = 100 kΩ	400			400						V/mV
	R_L = 10 kΩ	80	150		80	150		80	150		V/mV
T_{MIN} to T_{MAX}	R_L = 10 kΩ	80			80						V/mV
	R_L = 1 kΩ	20	30		20	30		20	30		V/mV
T_{MIN} to T_{MAX}	R_L = 1 kΩ	10			10						V/mV
NOISE/HARMONIC PERFORMANCE											
Input Voltage Noise											
	0.1 Hz to 10 Hz		2			2			2		μV p-p
	f = 10 Hz		25			25			25		nV/√Hz
	f = 100 Hz		21			21			21		nV/√Hz
	f = 1 kHz		16			16			16		nV/√Hz
	f = 10 kHz		13			13			13		nV/√Hz
Input Current Noise	0.1 Hz to 10 Hz		18			18			18		fA p-p
	f = 1 kHz		0.8			0.8			0.8		fA /√Hz
Harmonic Distortion	R_L = 10 kΩ										
f = 10 kHz	V_O = ±4.5 V		−93			−93			−93		dB
DYNAMIC PERFORMANCE											
Unity Gain Frequency			1.9			1.9			1.9		MHz
Full Power Response	V_O p-p = 9 V		105			105			105		kHz
Slew Rate			3			3			3		V/μs
Settling Time											
to 0.1%	V_O = 0 V to ±4.5 V		1.4			1.4			1.4		μs
to 0.01%			1.8			1.8			1.8		μs
MATCHING CHARACTERISTICS	AD822 Only										
Initial Offset				1.0			0.5			1.6	mV
Max Offset over Temperature				3			2			2	mV
Offset Drift			3			3					μV/°C
Input Bias Currents				25			10			25	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ		−130			−130			−130		dB
f = 100 kHz			−93			−93			−93		dB
INPUT CHARACTERISTICS											
Common-Mode Voltage Range[2]		−5.2		4	−5.2		4	−5.2		4	V
T_{MIN} to T_{MAX}		−5.2		4	−5.2		4				V
CMRR (AD820)	V_{CM} = −5 V to +2 V	66	80		72	80					dB
CMRR (AD822)	V_{CM} = −5 V to +2 V	66	80		69	80		66	80		dB
T_{MIN} to T_{MAX}		66			66						dB
Input Impedance											
Differential			$10^{13}\|0.5$			$10^{13}\|0.5$			$10^{13}\|0.5$		Ω|pF
Common Mode			$10^{13}\|2.8$			$10^{13}\|2.8$			$10^{13}\|2.8$		Ω|pF
OUTPUT CHARACTERISTICS											
Output Saturation Voltage[3]											
V_{OL}–V_{EE}	I_{SINK} = 20 μA		5	7		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10				mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 μA		10	14		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20				mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80				mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160				mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000				mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900				mV
Operating Output Current		15			15			15			mA
T_{MIN} to T_{MAX}		12			12			12			mA
Short Circuit Current			25			25			25		mA
Capacitive Load Drive			350			350			350		pF
POWER SUPPLY											
Quiescent Current/Amplifier			650	800		650	800		650		μA
	T_{MIN} to T_{MAX}			800			800				μA
Power Supply Rejection	V_S = 5 V to 15 V	70	80		66	80			80		dB
	T_{MIN} to T_{MAX}	70			66						dB

(V_S = ±15 V @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0 V unless otherwise noted)

Parameter	Conditions	AD820A/AD822A Min	AD820A/AD822A Typ	AD820A/AD822A Max	AD820B/AD822B Min	AD820B/AD822B Typ	AD820B/AD822B Max	AD822S[1] Min	AD822S[1] Typ	AD822S[1] Max	Units
DC PERFORMANCE											
Initial Offset	AD820		0.4	2		0.3	1				mV
	AD822		0.4	2		0.3	1.5		0.4	2.0	mV
Max Offset over Temperature	AD820		0.5	3		0.5	2				mV
	AD822		0.5	3		0.5	2.5		0.5		mV
Offset Drift			2.0			2.0			2.0		µV/°C
Input Bias Current	V_{CM} = 0 V, AD820		2	25		2	10				pA
	V_{CM} = 0 V, AD822		2	25		2	12		2	25	pA
	V_{CM} = −10 V		40			40			40		pA
at T_{MAX}	V_{CM} = 0 V		0.5	5		0.5	2.5		0.5		pA
Input Offset Current	AD820		2	20		2	10				pA
	AD822		2	20		2	12		2	20	pA
at T_{MAX}			0.5			0.5			1.5		nA
Open-Loop Gain	V_O = −10 V to +10 V										
	R_L = 100 kΩ	500	2000		500	2000		500	2000		V/mV
T_{MIN} to T_{MAX}	R_L = 100 kΩ	500			500						V/mV
	R_L = 10 kΩ	100	500		100	500		100	500		V/mV
T_{MIN} to T_{MAX}	R_L = 10 kΩ	100			100						V/mV
	R_L = 1 kΩ	30	45		30	45		30	45		V/mV
T_{MIN} to T_{MAX}	R_L = 1 kΩ	20			20						V/mV
NOISE/HARMONIC PERFORMANCE											
Input Voltage Noise	0.1 Hz to 10 Hz		2			2			2		µV p-p
	f = 10 Hz		25			25			25		nV/√Hz
	f = 100 Hz		21			21			21		nV/√Hz
	f = 1 kHz		16			16			16		nV/√Hz
	f = 10 kHz		13			13			13		nV/√Hz
Input Current Noise	0.1 Hz to 10 Hz		18			18			18		fA p-p
	f = 1 kHz		0.8			0.8			0.8		fA /√Hz
Harmonic Distortion	R_L = 10 kΩ										
f = 10 kHz	V_O = ±10 V		−85			−85			−85		dB
DYNAMIC PERFORMANCE											
Unity Gain Frequency			1.9			1.9			1.9		MHz
Full Power Response	V_O p-p = 20 V		45			45			45		kHz
Slew Rate			3			3			3		V/µs
Settling Time											
to 0.1%	V_O = 0 V to ±10 V		4.1			4.1			4.1		µs
to 0.01%			4.5			4.5			4.5		µs
MATCHING CHARACTERISTICS	AD822 Only										
Initial Offset				3			2			0.8	mV
Max Offset over Temperature				4			2.5			1.0	mV
Offset Drift			3			3					µV/°C
Input Bias Currents				25			12			25	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ		−130			−130			−130		dB
f = 100 kHz			−93			−93			−93		dB
INPUT CHARACTERISTICS											
Common-Mode Voltage Range[2]		−15.2		14	−15.2		14	−15.2		14	V
T_{MIN} to T_{MAX}		−15.2		14	−15.2		14				V
CMRR	V_{CM} = −15 V to +12 V	70	80		74	90		70	90		dB
T_{MIN} to T_{MAX}		70			74						dB
Input Impedance											
Differential			$10^{13}\|0.5$			$10^{13}\|0.5$			$10^{13}\|0.5$		Ω|pF
Common Mode			$10^{13}\|2.8$			$10^{13}\|2.8$			$10^{13}\|2.8$		Ω|pF
OUTPUT CHARACTERISTICS											
Output Saturation Voltage[3]											
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10				mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20				mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80				mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160				mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000				mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900				mV
Operating Output Current		20			20			20			mA
T_{MIN} to T_{MAX}		15			15			15			mA
Short Circuit Current			45			45			45		mA
Capacitive Load Drive			350			350			350		pF
POWER SUPPLY											
Quiescent Current/Amplifier			700	900		700	900		700		µA
	T_{MIN} to T_{MAX}			900			900				µA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		66	80		70	80		dB
	T_{MIN} to T_{MAX}	70			66						dB

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AD820/AD822—SPECIFICATIONS (V_S = 0, 3 V @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted)

Parameter	Conditions	AD820A-3V Min	AD820A-3V Typ	AD820A-3V Max	AD822A-3V Min	AD822A-3V Typ	AD822A-3V Max	Units
DC PERFORMANCE								
Initial Offset			0.2	1		0.2	1	mV
Max Offset over Temperature			0.5	1.5		0.5	1.5	mV
Offset Drift			1			1		µV/°C
Input Bias Current	V_{CM} = 0 V to +2 V		2	25		2	25	pA
at T_{MAX}			0.5	5		0.5	5	nA
Input Offset Current			2	20		2	20	pA
at T_{MAX}			0.5			0.5		nA
Open Loop Gain	V_O = 0.2 V to 2 V							
	R_L = 100 kΩ	300	1000		300	1000		V/mV
T_{MIN} to T_{MAX}	R_L = 100 kΩ	400			300			V/mV
	R_L = 10 kΩ	60	150		60	150		V/mV
T_{MIN} to T_{MAX}	R_L = 10 kΩ	80			60			V/mV
	R_L = 1 kΩ	10	30		10	30		V/mV
T_{MIN} to T_{MAX}	R_L = 1 kΩ	8			8			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise	0.1 Hz to 10 Hz		2			2		µV p-p
	f = 10 Hz		25			25		nV/√Hz
	f = 100 Hz		21			21		nV/√Hz
	f = 1 kHz		16			16		nV/√Hz
	f = 10 kHz		13			13		nV/√Hz
Input Current Noise	0.1 Hz to 10 Hz		18			18		fA p-p
	f = 1 kHz		0.8			0.8		fA /√Hz
Harmonic Distortion	R_L = 10 kΩ							
f = 10 kHz	V_O = ±1.25 V		−92			−92		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.5			1.5		MHz
Full Power Response	V_O p-p = 2.5 V		240			240		kHz
Slew Rate			3			3		V/µs
Settling Time								
to 0.1%	V_O = 0.2 V to 2.5 V		1			1		µs
to 0.01%			1.4			1.4		µs
MATCHING CHARACTERISTICS								
Initial Offset							1	mV
Max Offset over Temperature							2	mV
Offset Drift						2		µV/°C
Input Bias Currents							10	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ					−130		dB
f = 100 kHz						−93		dB
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[2]		−0.2		2	−0.2		2	V
T_{MIN} to T_{MAX}		−0.2		2	−0.2		2	V
CMRR	V_{CM} = 0 V to +1 V	60	74		60	74		dB
T_{MIN} to T_{MAX}		60			60			dB
Input Impedance								
Differential			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[3]								
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 10 mA		200	400		200	400	mV
T_{MIN} to T_{MAX}				400			400	mV
V_{CC}–V_{OH}	I_{SOURCE} = 10 mA		500	1000		500	1000	mV
T_{MIN} to T_{MAX}				1000			1000	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Short Circuit Current			25			25		mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current/Amplifier			620	800		620	800	µA
	T_{MIN} to T_{MAX}			800			800	µA
Power Supply Rejection		70	80		66	80		dB
	T_{MIN} to T_{MAX}	70			66			dB

NOTES
[1]See standard military drawing for 883B specifications.
[2]This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range ($+V_S$ –1 V) to $+V_S$. Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 volt below the positive supply.
[3]V_{OL}–V_{EE} is defined as the difference between the lowest possible output voltage (V_{OL}) and the minus voltage supply rail (V_{EE}).
V_{CC}–V_{OH} is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).
Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD820 and AD822 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation
  Plastic DIP (N) . . . . . Observe Derating Curves
  Cerdip (Q) . . . . . Observe Derating Curves
  SOIC (R) . . . . . Observe Derating Curves
Input Voltage . . . . . ($+V_S$ + 0.2 V) to − (20 V + V_S)
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . ±30 V
Storage Temperature Range (N) . . . . . −65°C to +125°C
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (R) . . . . . −65°C to +150°C
Operating Temperature Range
  AD820A/B . . . . . −40°C to +85°C
  AD822A/B . . . . . −40°C to +85°C
  AD822S . . . . . −55°C to +125°C
Lead Temperature Range
  (Soldering 60 sec) . . . . . +260°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic DIP Package: θ_{JA} = 90°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin SOIC Package: θ_{JA} = 160°C/Watt

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD820 or AD822 is limited by the associated rise in junction temperature. For plastic packages, the maximum safe junction temperature is 145°C. For the cerdip packages, the maximum junction temperature is 175°C. If these maximums are exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the "overheated" condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves shown in Figure 24.

While the AD820 and AD822 are internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. With power supplies ±12 volts (or less) at an ambient temperature of +25°C or less, if the output node is shorted to a supply rail, then the amplifier will not be destroyed, even if this condition persists for an extended period.

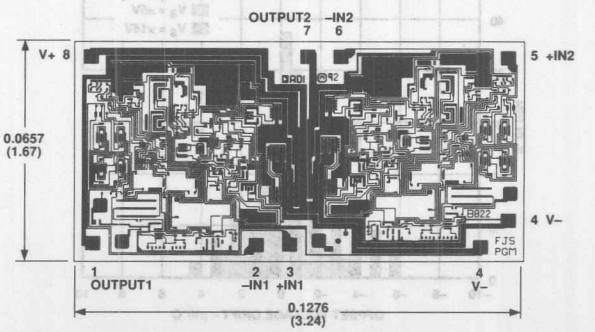
ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD820AN	−40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD820BN	−40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD820AR	−40°C to +85°C	8-Pin SOIC	R-8
AD820BR	−40°C to +85°C	8-Pin SOIC	R-8
AD820AR-3V	−40°C to +85°C	8-Pin SOIC	R-8
AD820AN-3V	−40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD822AN	−40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD822BN	−40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD822AR	−40°C to +85°C	8-Pin SOIC	R-8
AD822BR	−40°C to +85°C	8-Pin SOIC	R-8
AD822AR-3V	−40°C to +85°C	8-Pin SOIC	R-8
AD822AN-3V	−40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD822A Chips	−40°C to +85°C	Die	
Standard Military Drawing[3]	−55°C to +125°C	8-Pin Cerdip	Q-8

NOTES
[1]AD822 Spice model is available on ADI Model Disc.
[2]For outline information see Package Information section.
[3]Contact factory for availability.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



NOTE: BACK OF DIE IS AT $+V_S$ POTENTIAL.

AD820/AD822—Typical Characteristics

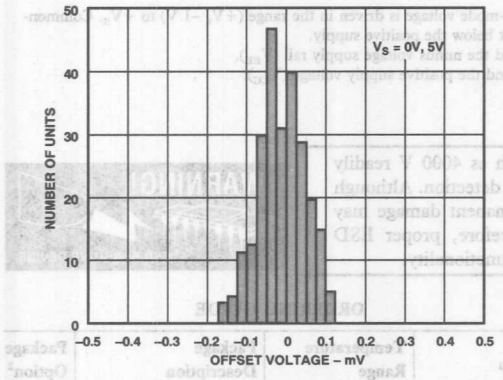


Figure 1a. AD820 Typical Distribution of Offset Voltage (248 Units)

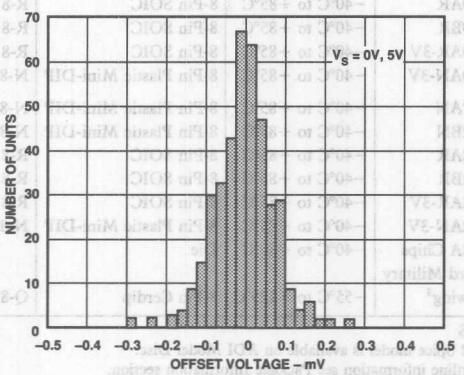


Figure 1b. AD822 Typical Distribution of Offset Voltage (390 Units)

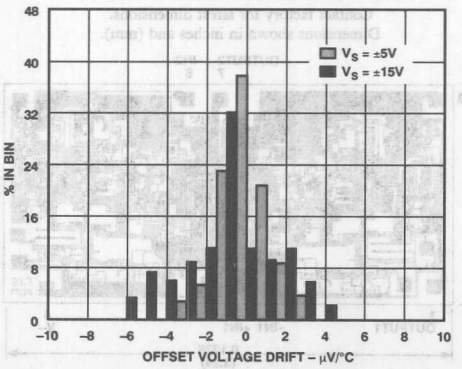


Figure 2a. AD820 Typical Distribution of Offset Voltage Drift (120 Units)

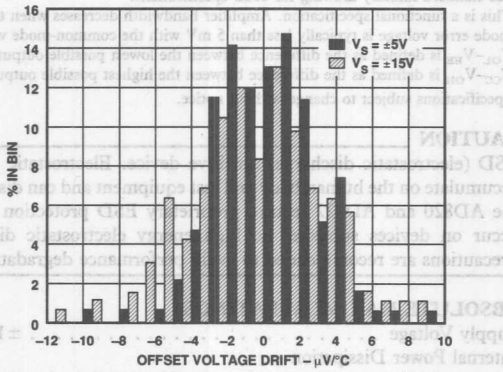


Figure 2b. AD822 Typical Distribution of Offset Voltage Drift (100 Units)

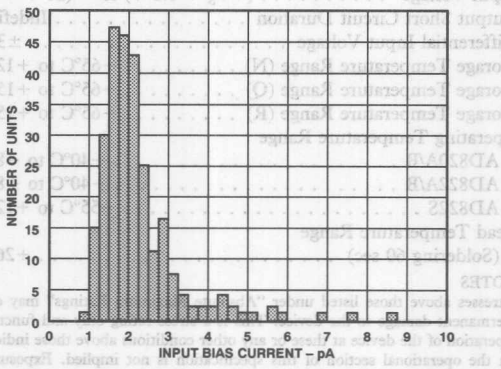


Figure 3. Typical Distribution of Input Bias Current (213 Units)

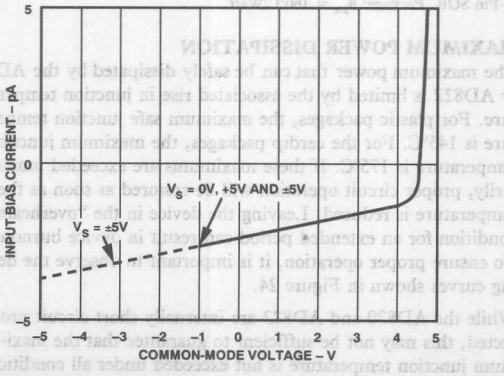


Figure 4. Input Bias Current vs. Common-Mode Voltage; V_S = +5 V, 0 V and V_S = ±5 V

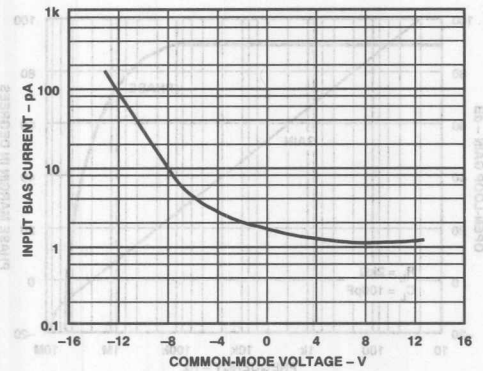


Figure 5. Input Bias Current vs. Common-Mode Voltage; V_S = ±15 V

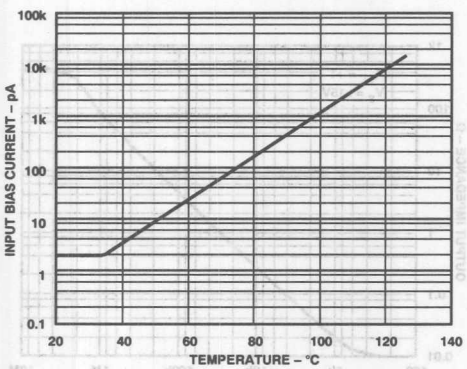


Figure 6. Input Bias Current vs. Temperature; V_S = 5 V, V_{CM} = 0

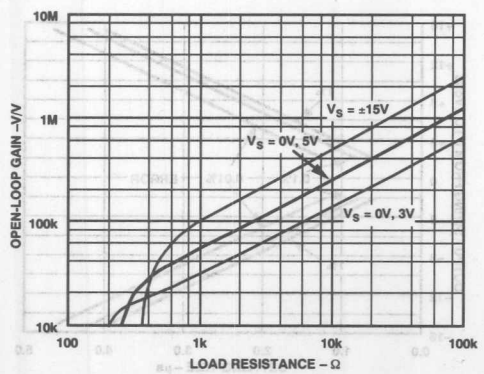


Figure 7a. AD820 Open-Loop Gain vs. Load Resistance

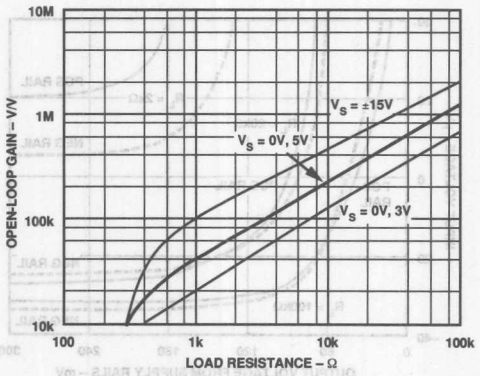


Figure 7b. AD822 Open-Loop Gain vs. Load Resistance

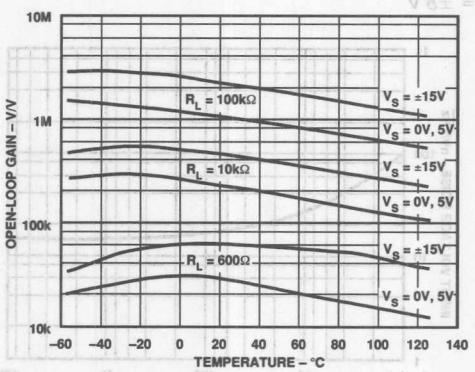


Figure 8. Open-Loop Gain vs. Temperature

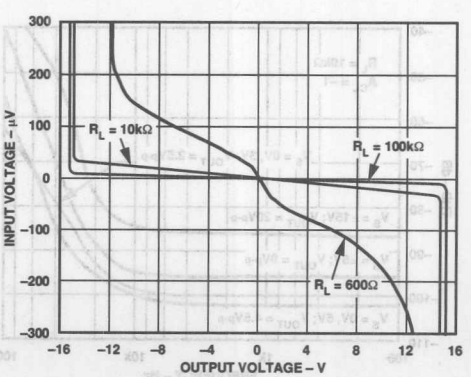


Figure 9. Input Error Voltage vs. Output Voltage for Resistive Loads

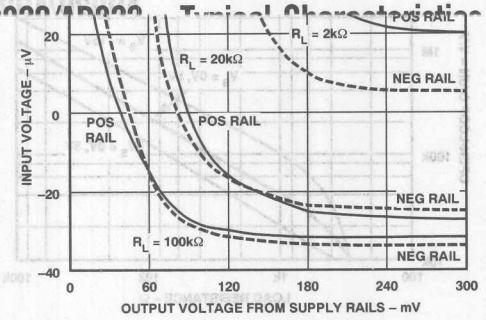


Figure 10. Input Error Voltage with Output Voltage within 300 mV of Either Supply Rail for Various Resistive Loads; V_S = ±5 V

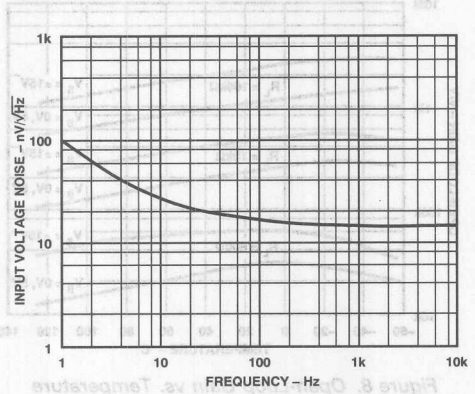


Figure 11. Input Voltage Noise vs. Frequency

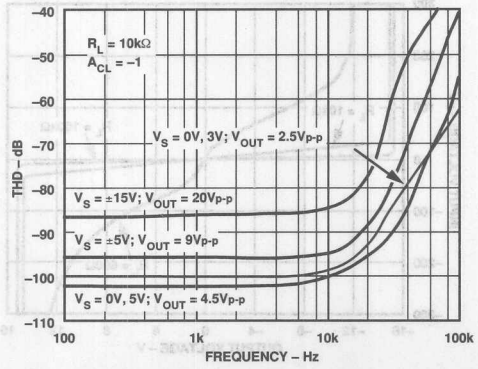


Figure 12. Total Harmonic Distortion vs. Frequency

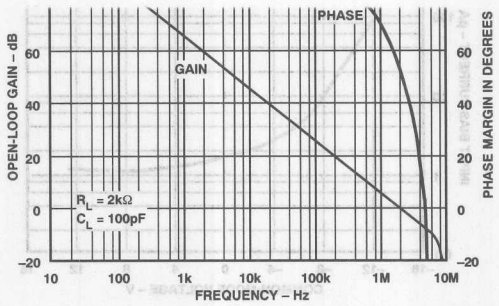


Figure 13. Open-Loop Gain and Phase Margin vs. Frequency

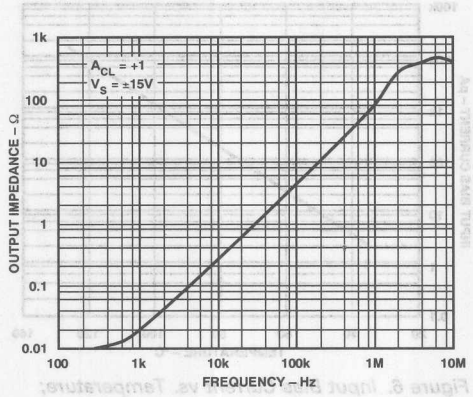


Figure 14. Output Impedance vs. Frequency

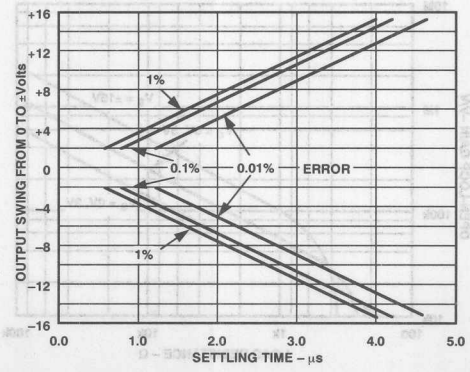


Figure 15. Output Swing and Error vs. Settling Time

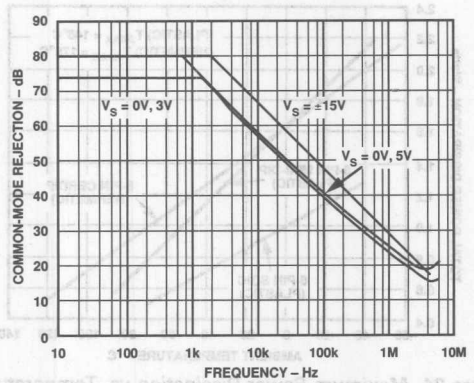


Figure 16. Common-Mode Rejection vs. Frequency

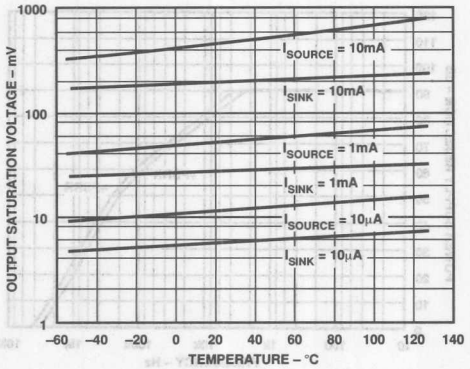


Figure 19. Output Saturation Voltage vs. Temperature

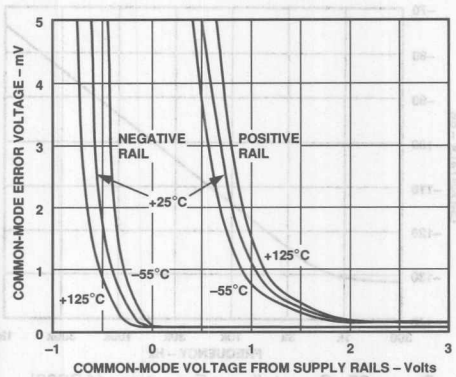


Figure 17. Absolute Common-Mode Error vs. Common-Mode Voltage from Supply Rails ($V_S - V_{CM}$)

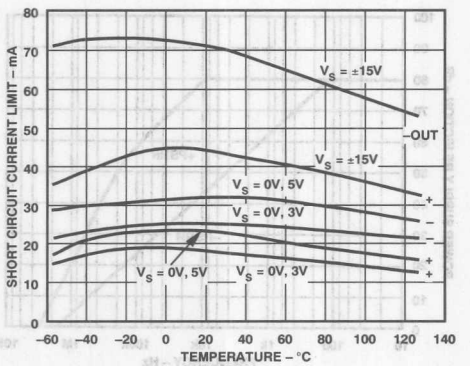


Figure 20. Short Circuit Current Limit vs. Temperature

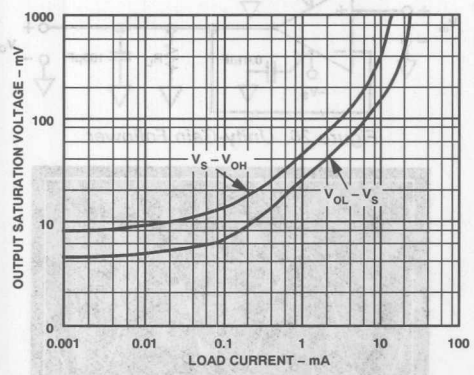


Figure 18. Output Saturation Voltage vs. Load Current

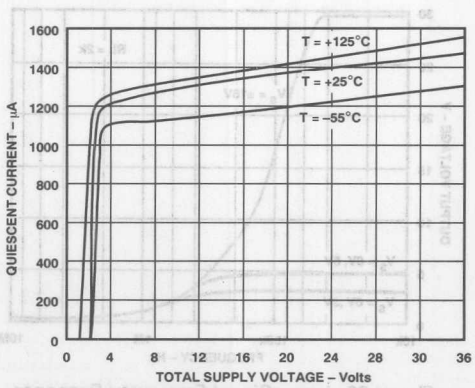


Figure 21. Quiescent Current vs. Supply Voltage vs. Temperature

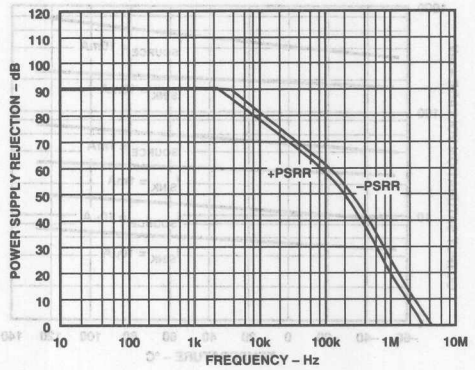


Figure 22a. AD820 Power Supply Rejection vs. Frequency

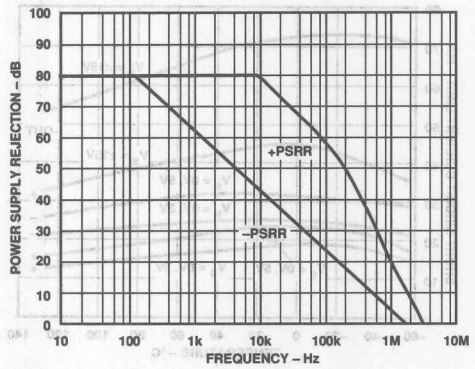


Figure 22b. AD822 Power Supply Rejection vs. Frequency

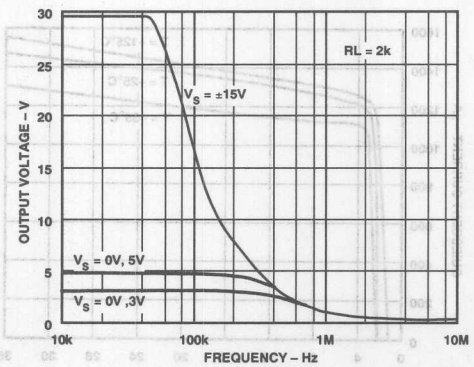


Figure 23. Large Signal Frequency Response

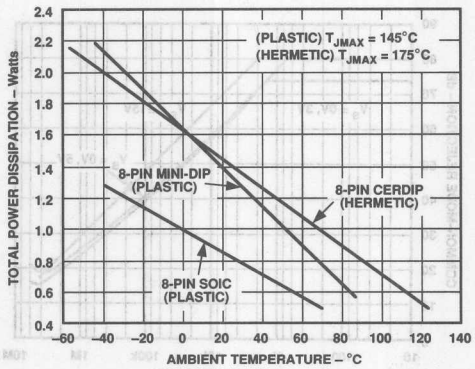


Figure 24. Maximum Power Dissipation vs. Temperature for Plastic and Hermetic Packages

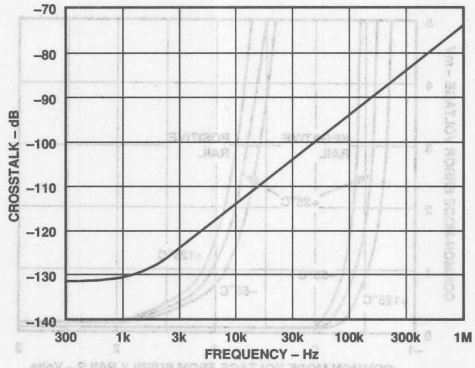


Figure 25. Crosstalk vs. Frequency (AD822)

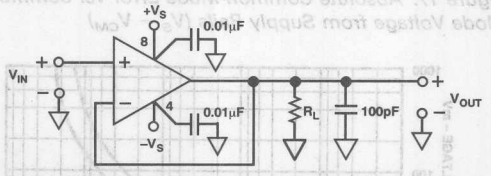


Figure 26. Unity-Gain Follower

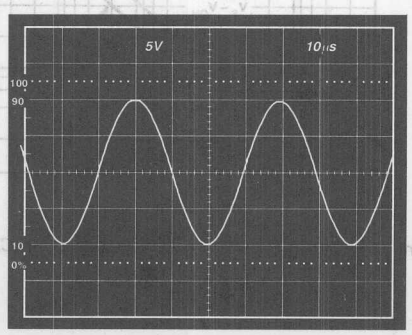


Figure 27. 20 V p-p, 25 kHz Sine Wave Input; Unity Gain Follower; R_L = 600 Ω, V_S = ±15 V

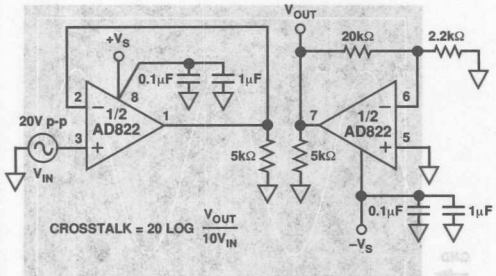


Figure 28. Crosstalk Test Circuit

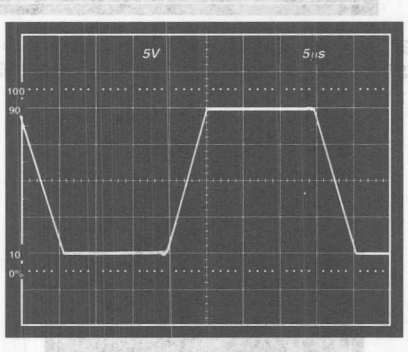


Figure 29. Large Signal Response Unity Gain Follower; V_S = ±15 V, R_L = 10 kΩ

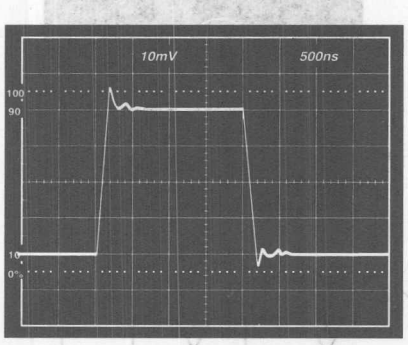


Figure 30. Small Signal Response Unity Gain Follower; V_S = ±15 V, R_L = 10 kΩ

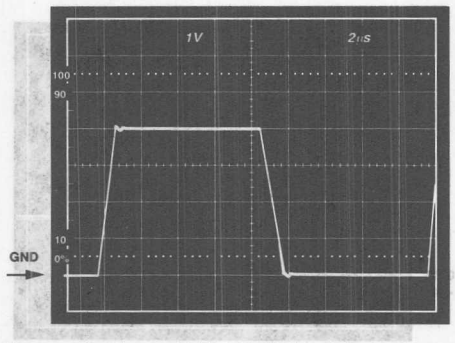


Figure 31. V_S = +5 V, 0 V; Unity Gain Follower Response to 0 V to 4 V Step

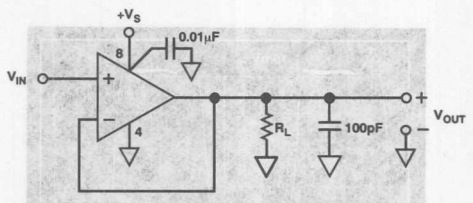


Figure 32. Unity-Gain Follower

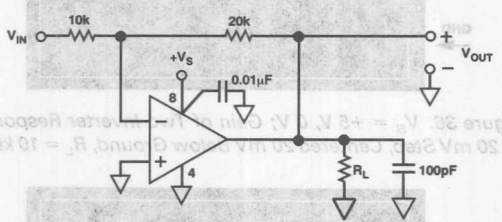


Figure 33. Gain of Two Inverter

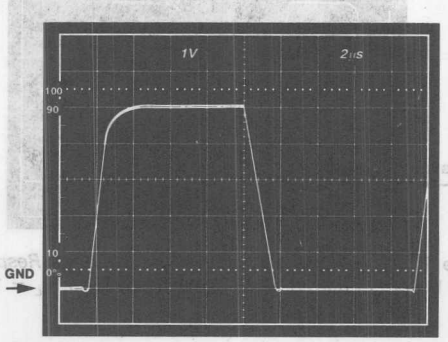


Figure 34. V_S = +5 V, 0 V; Unity Gain Follower Response to 0 V to 5 V Step

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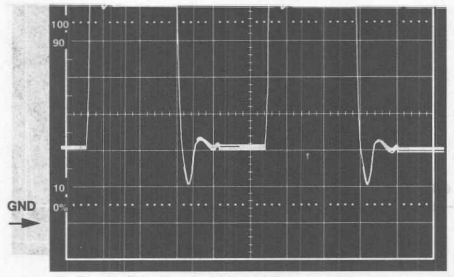

Figure 35. V_S = +5 V, 0 V; Unity Gain Follower Response, to 40 mV Step Centered 40 mV Above Ground, R_L = 10 kΩ

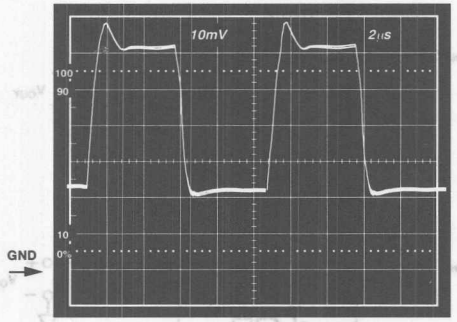

Figure 36. V_S = +5 V, 0 V; Gain of Two Inverter Response to 20 mV Step, Centered 20 mV Below Ground, R_L = 10 kΩ

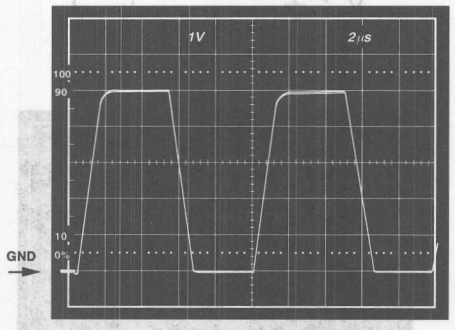

Figure 37. V_S = +5 V, 0 V; Gain of Two Inverter Response to 2.5 V Step Centered −1.25 V Below Ground, R_L = 10 kΩ

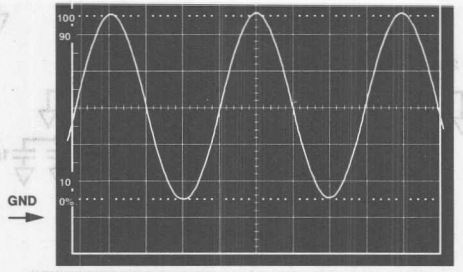

Figure 38. V_S = 3 V, 0 V; Gain of Two Inverter, V_{IN} = 1.25 V, 25 kHz, Sine Wave Centered at −0.75 V, R_L = 600 Ω

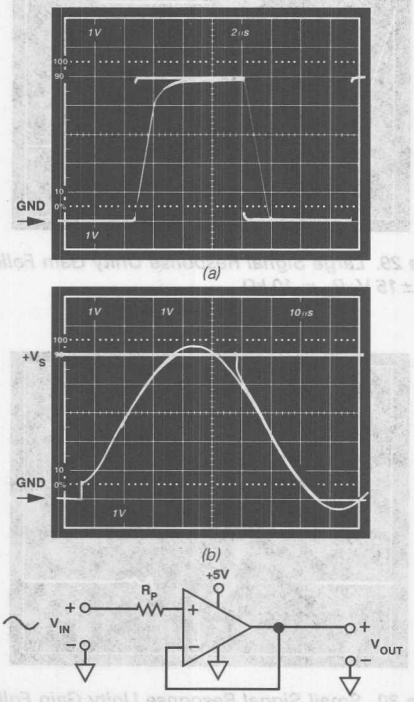

Figure 39. (a) Response with R_P = 0; V_{IN} from 0 to $+V_S$ (b) V_{IN} = 0 to $+V_S$ + 200 mV, V_{OUT} = 0 to $+V_S$, R_P = 49.9 kΩ

APPLICATION NOTES

INPUT CHARACTERISTICS

In the AD820 and AD822, n-channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $-V_S$ to 1 V less than $+V_S$. Driving the input voltage closer to the positive rail will cause a loss of amplifier bandwidth (as can be seen by comparing the large signal responses shown in Figures 31 and 34) and increased common-mode voltage error as illustrated in Figure 17.

The AD820 and AD822 do not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 39a shows the response of a voltage follower to a 0 V to +5 V ($+V_S$) square wave input. The input and output are superimposed. The output tracks the input up to $+V_S$ without phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output wave form. For input voltages greater than $+V_S$, a resistor in series with the noninverting input will prevent phase reversal, at the expense of greater input voltage noise. This is illustrated in Figure 39b.

Since the input stage uses n-channel JFETs, input current during normal operation is negative; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S - 0.4V$, the input current will reverse direction as internal device junctions become forward biased. This is illustrated in Figure 4.

A current limiting resistor should be used in series with the input of the AD820 or AD822 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV, or if an input voltage will be applied to the AD820 or AD822 when $\pm V_S = 0$. The amplifier will be damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 volts of continuous overvoltage, and increases the input voltage noise by a negligible amount.

Input voltages less than $-V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 volts below the minus supply voltage as long as the total voltage from the positive supply to the input terminal is less than 36 volts. In addition, the input stage typically maintains picoamp level input currents across that input voltage range.

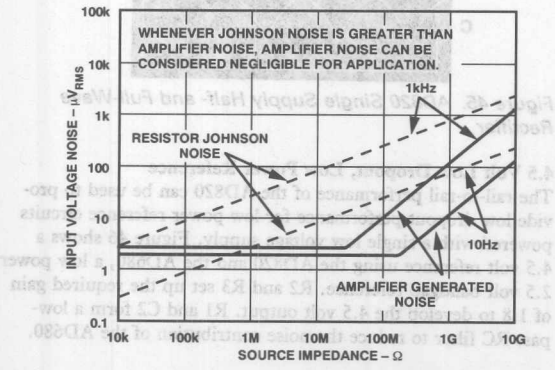

Figure 40. Total Noise vs. Source Impedance

The AD820 and AD822 are designed for 13 nV/$\sqrt{\text{Hz}}$ wideband input voltage noise and maintain low noise performance to low frequencies (refer to Figure 11). This noise performance, along with the low input current and current noise means that the AD820 and AD822 contribute negligible noise for applications with source resistances greater than 10 kΩ and signal bandwidths greater than 1 kHz. This is illustrated in Figure 40.

OUTPUT CHARACTERISTICS

The AD820/AD822's unique bipolar rail-to-rail output stage swings within 5 mV of the minus supply and 10 mV of the positive supply with no external resistive load. The approximate output saturation resistance is 40 Ω sourcing and 20 Ω sinking. This can be used to estimate output saturation voltage when driving heavier current loads. For instance, when sourcing 5 mA, the saturation voltage to the positive supply rail will be 200 mV, when sinking 5 mA, the saturation voltage to the minus rail will be 100 mV.

The amplifier's open-loop gain characteristic will change as a function of resistive load, as shown in Figures 7 through 10. For load resistances over 20 kΩ, the AD820/AD822's input error voltage is virtually unchanged until the output voltage is driven to 180 mV of either supply.

If the AD820/AD822's output is overdriven so as to saturate either of the output devices, the amplifier will recover within 2 μs of its input returning to the amplifier's linear operating region.

Direct capacitive loads will interact with the amplifier's effective output impedance to form an additional pole in the amplifier's feedback loop, which can cause excessive peaking on the pulse response or loss of stability. Worst case is when the amplifier is used as a unity gain follower. Figure 41 shows the AD820/AD822's pulse response as a unity gain follower driving 350 pF. This amount of overshoot indicates approximately 20 degrees of phase margin—the system is stable, but is nearing the edge. Configurations with less loop gain, and as a result less loop bandwidth, will be much less sensitive to capacitance load effects. Figure 42 is a plot of capacitive load that will result in a 20 degree phase margin versus noise gain for the AD820/AD822. Noise gain is the inverse of the feedback attenuation factor provided by the feedback network in use.

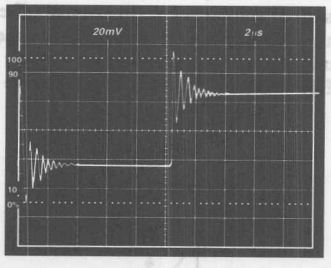

Figure 41. Small Signal Response of AD820/AD822 as Unity Gain Follower Driving 350 pF Capacitive Load

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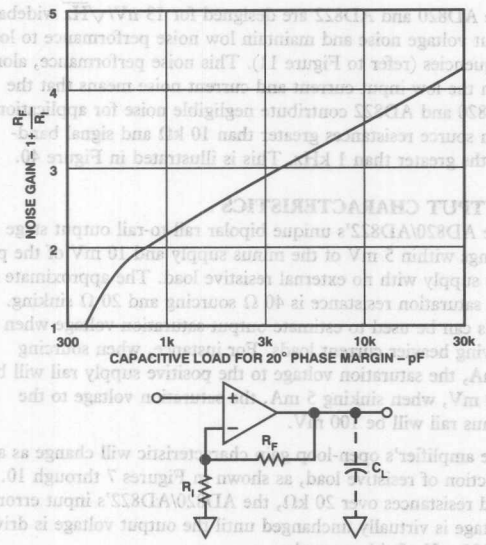

Figure 42. Capacitive Load Tolerance vs. Noise Gain

Figure 43 shows a method for extending capacitance load drive capability for a unity gain follower. With these component values, the circuit will drive 5,000 pF with a 10% overshoot.

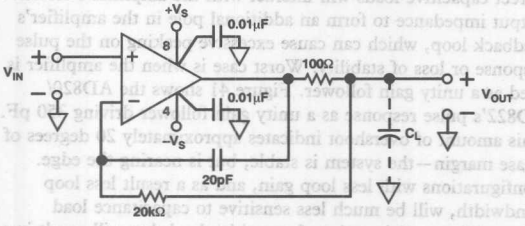

Figure 43. Extending Unity Gain Follower Capacitive Load Capability Beyond 350 pF

OFFSET VOLTAGE ADJUSTMENT

The AD820's offset voltage is low, so external offset voltage nulling is not usually required. Figure 44 shows the recommended technique for AD820's packaged in plastic DIPs. Adjusting offset voltage in this manner will change the offset

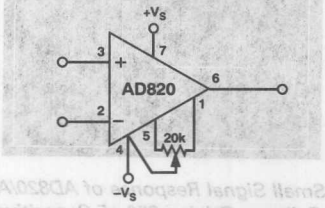

Figure 44. AD820 Offset Null

voltage temperature drift by 4 µV/°C for every millivolt of induced offset. The null pins are not functional for AD820s in the SO-8 "R" package.

APPLICATIONS—AD820

Single Supply Half-Wave and Full-Wave Rectifiers

An AD820 configured as a unity gain follower and operated with a single supply can be used as a simple half-wave rectifier. The AD820's inputs maintain picoamp level input currents even when driven well below the minus supply. The rectifier puts that behavior to good use, maintaining an input impedance of over $10^{11}\Omega$ for input voltages from 1 volt from the positive supply to 20 volts below the negative supply.

The full and half-wave rectifier shown in Figure 45 operates as follows: when V_{IN} is above ground, R1 is bootstrapped through the unity gain follower A1 and the loop of amplifier A2. This forces the inputs of A2 to be equal, thus no current flows through R1 or R2, and the circuit output tracks the input. When V_{IN} is below ground, the output of A1 is forced to ground. The noninverting input of amplifier A2 sees the ground level output of A1, therefore A2 operates as a unity gain inverter. The output at node C is then a full-wave rectified version of the input. Node B is a buffered half-wave rectified version of the input. Input voltages up to ±18 volts can be rectified, depending on the voltage supply used.

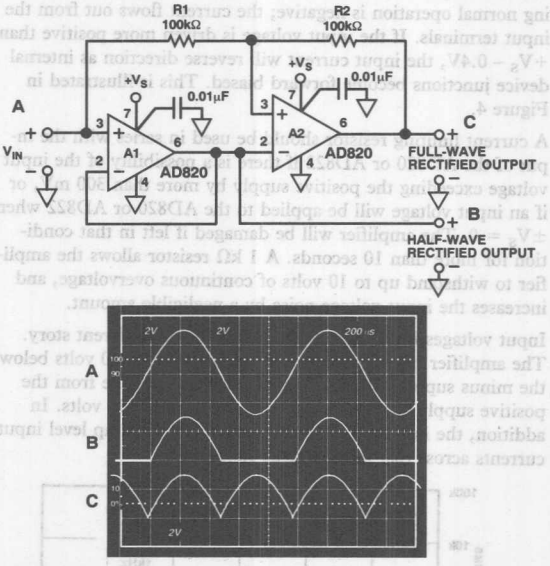

Figure 45. AD820 Single Supply Half- and Full-Wave Rectifier

4.5 Volt Low Dropout, Low Power Reference

The rail-to-rail performance of the AD820 can be used to provide low dropout performance for low power reference circuits powered with a single low voltage supply. Figure 46 shows a 4.5 volt reference using the AD820 and the AD680, a low power 2.5 volt bandgap reference. R2 and R3 set up the required gain of 1.8 to develop the 4.5 volt output. R1 and C2 form a low-pass RC filter to reduce the noise contribution of the AD680.

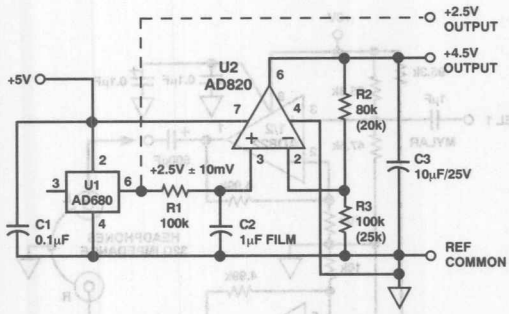

Figure 46. AD820 Single Supply 4.5 Volt Low Dropout Reference

With a 1 mA load, this reference maintains the 4.5 volt output with a supply voltage down to 4.7 volts. The amplitude of the recovery transient for a 1 mA to 10 mA step change in load current is under 20 mV, and settles out in a few microseconds. Output voltage noise is less than 10 µV rms in a 25 kHz noise bandwidth.

Low Power Three-Pole Sallen Key Low-Pass Filter

The AD820's high input impedance makes it a good selection for active filters. High value resistors can be used to construct low frequency filters with capacitors much less than 1 µF. The AD820's picoamp level input currents contribute minimal dc errors.

Figure 47 shows an example, a 10 Hz three-pole Sallen Key Filter. The high value used for R1 minimizes interaction with signal source resistance. Pole placement in this version of the filter minimizes the Q associated with the two-pole section of the filter. This eliminates any peaking of the noise contribution of resistors R1, R2, and R3, thus minimizing the inherent output voltage noise of the filter.

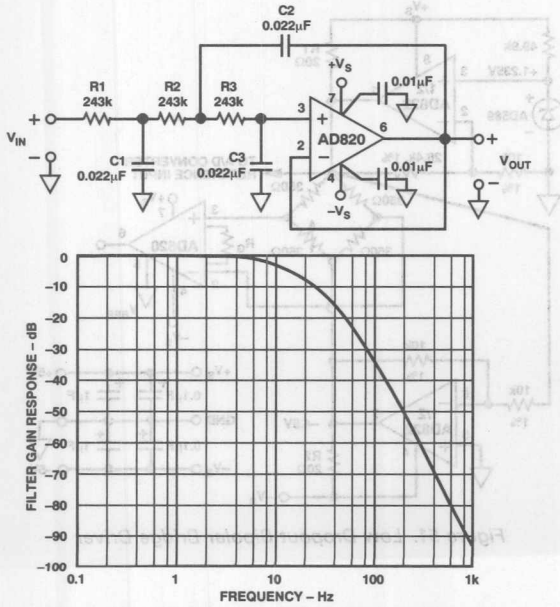

Figure 47. AD820 10 Hz Sallen Key Low-Pass Filter

APPLICATIONS–AD822

Single Supply Voltage-to-Frequency Converter

The circuit shown in Figure 48 uses the AD822 to drive a low power timer, which produces a stable pulse of width t_1. The positive going output pulse is integrated by R1-C1 and used as one input to the AD822, which is connected as a differential integrator. The other input (nonloading) is the unknown voltage, V_{IN}. The AD822 output drives the timer trigger input, closing the overall feedback loop.

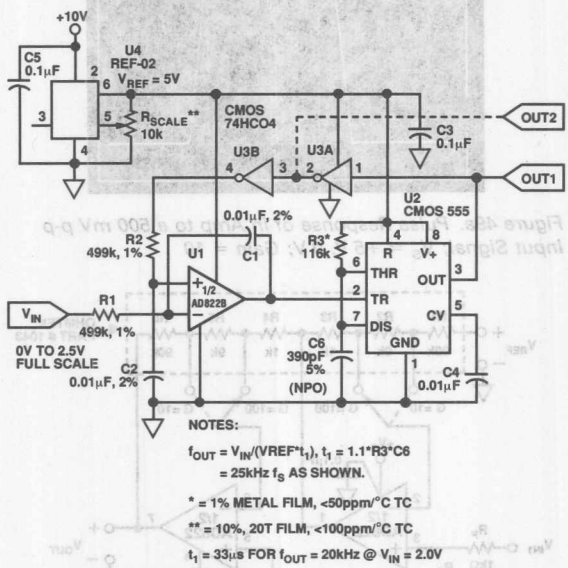

Figure 48. Single Supply Voltage-to-Frequency Converter

Typical AD822 bias currents of 2 pA allow megaohm-range source impedances with negligible dc errors. Linearity errors on the order of 0.01% full scale can be achieved with this circuit. This performance is obtained with a 5 volt single supply which delivers less than 1 mA to the entire circuit.

Single Supply Programmable Gain Instrumentation Amplifier

The AD822 can be configured as a single supply instrumentation amplifier that is able to operate from single supplies down to 3 V, or dual supplies up to ± 15 V. Using only one AD822 rather than three separate op amps, this circuit is cost and power efficient. AD822 FET inputs' 2 pA bias currents minimize offset errors caused by high unbalanced source impedances.

Table I. AD822 In Amp Performance

Parameters	V_S = 3 V, 0 V	V_S = ±5 V
CMRR	74 dB	80 dB
Common-Mode Voltage Range	−0.2 V to +2 V	−5.2 V to +4 V
3 dB BW, G = 10	180 kHz	180 kHz
G = 100	18 kHz	18 kHz
$t_{SETTLING}$ 2 V Step (V_S = 0 V, 3 V)	2 µs	
5 V (V_S = ±5 V)		5 µs
Noise @ f = 1 kHz, G = 10	270 nV/√Hz	270 nV/√Hz
G = 100	2.2 µV/√Hz	2.2 µV/√Hz
I_{SUPPLY} (Total)	1.10 mA	1.15 mA

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An array of precision thin-film resistors sets the in amp gain to be either 10 or 100. These resistors are laser-trimmed to ratio match to 0.01%, and have a maximum differential TC of 5 ppm/°C.

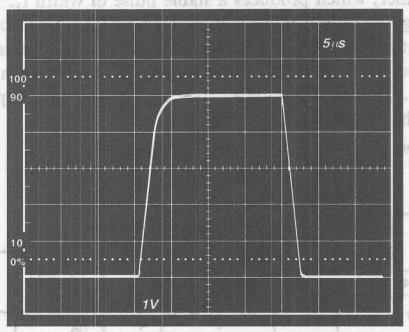


Figure 49a. Pulse Response of In Amp to a 500 mV p-p Input Signal; V_S = +5 V, 0 V; Gain = 10

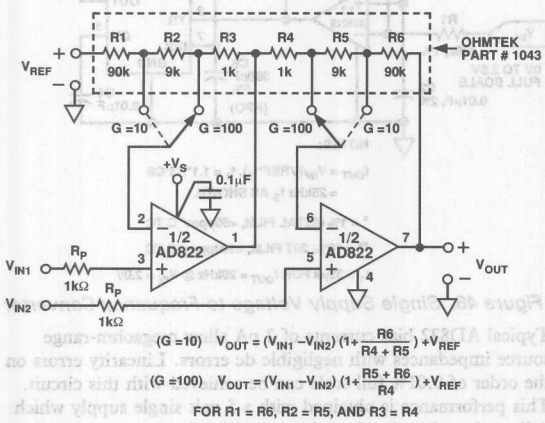


Figure 49b. A Single Supply Programmable Instrumentation Amplifier

3 Volt, Single Supply Stereo Headphone Driver

The AD822 exhibits good current drive and THD+N performance, even at 3 V single supplies. At 1 kHz, total harmonic distortion plus noise (THD+N) equals −62 dB (0.079%) for a 300 mV p-p output signal. This is comparable to other single supply op amps which consume more power and cannot run on 3 V power supplies.

In Figure 50, each channel's input signal is coupled via a 1 µF Mylar capacitor. Resistor dividers set the dc voltage at the noninverting inputs so that the output voltage is midway between the power supplies (+1.5 V). The gain is 1.5. Each half of the AD822 can then be used to drive a headphone channel. A 5 Hz high-pass filter is realized by the 500 µF capacitors and the headphones, which can be modeled as 32 ohm load resistors to ground. This ensures that all signals in the audio frequency range (20 Hz–20 kHz) are delivered to the headphones.

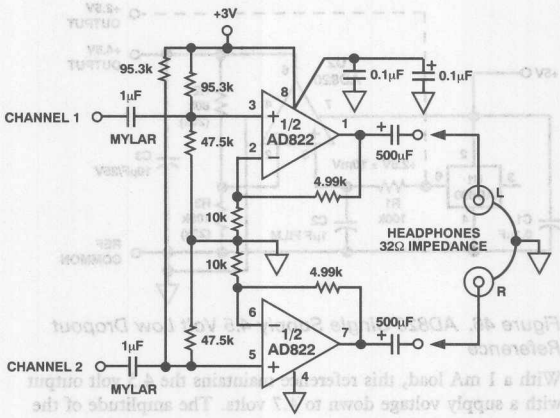


Figure 50. 3 Volt Single Supply Stereo Headphone Driver

Low Dropout Bipolar Bridge Driver

The AD822 can be used for driving a 350 ohm Wheatstone bridge. Figure 51 shows one half of the AD822 being used to buffer the AD589—a 1.235 V low power reference. The output of +4.5 V can be used to drive an A/D converter front end. The other half of the AD822 is configured as a unity-gain inverter, and generates the other bridge input of −4.5 V. Resistors R1 and R2 provide a constant current for bridge excitation. The AD620 low power instrumentation amplifier is used to condition the differential output voltage of the bridge. The gain of the AD620 is programmed using an external resistor R_G, and determined by:

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

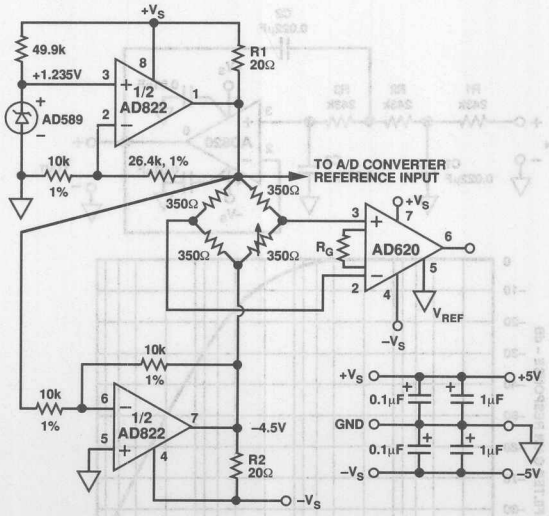


Figure 51. Low Dropout Bipolar Bridge Driver

ANALOG DEVICES

High Speed, Low Power Dual Operational Amplifier

AD826

FEATURES

High Speed:
- 50 MHz Unity Gain Bandwidth
- 350 V/μs Slew Rate
- 70 ns Settling Time to 0.01%

Low Power:
- 7.5 mA Max Power Supply Current Per Amp

Easy to Use:
- Drives Unlimited Capacitive Loads
- 50 mA Min Output Current Per Amplifier
- Specified for +5 V, ±5 V and ±15 V Operation
- 2.0 V p-p Output Swing into a 150 Ω Load (V_S = +5 V)

Good Video Performance
- Differential Gain & Phase Error of 0.07% & 0.11°

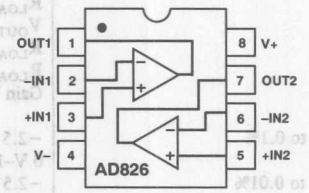
Excellent DC Performance:
- 2.0 mV Max Input Offset Voltage

APPLICATIONS

- Unity Gain ADC/DAC Buffer
- Cable Drivers
- 8- and 10-Bit Data Acquisition Systems
- Video Line Driver
- Active Filters

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP and SO Package



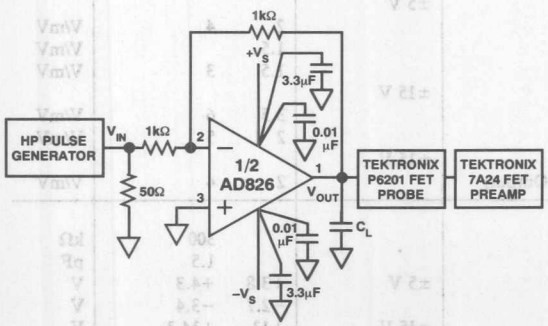
PRODUCT DESCRIPTION

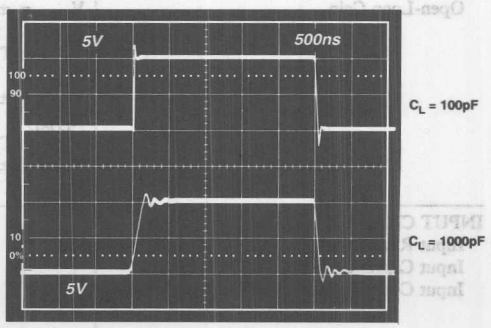
The AD826 is a dual, high speed voltage feedback op amp. It is ideal for use in applications which require unity gain stability and high output drive capability, such as buffering and cable driving. The 50 MHz bandwidth and 350 V/μs slew rate make the AD826 useful in many high speed applications including: video, CATV, copiers, LCDs, image scanners and fax machines.

The AD826 features high output current drive capability of 50 mA min per amp, and is able to drive unlimited capacitive loads. With a low power supply current of 15 mA max for both amplifiers, the AD826 is a true general purpose operational amplifier.

The AD826 is ideal for power sensitive applications such as video cameras and portable instrumentation. The AD826 can operate from a single +5 V supply, while still achieving 25 MHz of bandwidth. Furthermore the AD826 is fully specified from a single +5 V to ±15 V power supplies.

The AD826 excels as an ADC/DAC buffer or active filter in data acquisition systems and achieves a settling time of 70 ns to 0.01%, with a low input offset voltage of 2 mV max. The AD826 is available in small 8-pin plastic mini-DIP and SO packages.





Driving a Large Capacitive Load

9

AD826—SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	V_S	Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
Unity Gain Bandwidth		±5 V	30	35		MHz
		±15 V	45	50		MHz
		0, +5 V	25	29		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	±5 V	10	20		MHz
		±15 V	25	55		MHz
		0, +5 V	10	20		MHz
Full Power Bandwidth[1]	V_{OUT} = 5 V p-p					
	R_{LOAD} = 500 Ω	±5 V		15.9		MHz
	V_{OUT} = 20 V p-p					
	R_{LOAD} = 1 kΩ	±15 V		5.6		MHz
Slew Rate	R_{LOAD} = 1 kΩ	±5 V	200	250		V/µs
	Gain = −1	±15 V	300	350		V/µs
		0, +5 V	150	200		V/µs
Settling Time to 0.1%	−2.5 V to +2.5 V	±5 V		45		ns
	0 V–10 V Step, A_V = −1	±15 V		45		ns
to 0.01%	−2.5 V to +2.5 V	±5 V		70		ns
	0 V–10 V Step, A_V = −1	±15 V		70		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	F_C = 1 MHz	±15 V		−78		dB
Input Voltage Noise	f = 10 kHz	±5 V, ±15 V		15		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz	±5 V, ±15 V		1.5		$pA/\sqrt{Hz}$
Differential Gain Error	NTSC	±15 V		0.07	0.1	%
(Rl = 150 Ω)	Gain = +2	±5 V		0.12	0.15	%
		0, +5 V		0.15		%
Differential Phase Error	NTSC	±15 V		0.11	0.15	Degrees
(Rl = 150 Ω)	Gain = +2	±5 V		0.12	0.15	Degrees
		0, +5 V		0.15		Degrees
DC PERFORMANCE						
Input Offset Voltage		±5 V to ±15 V		0.5	2	mV
	T_{MIN} to T_{MAX}				3	mV
Offset Drift				10		µV/°C
Input Bias Current		±5 V, ±15 V		3.3	6.6	µA
	T_{MIN}				10	µA
	T_{MAX}				4.4	µA
Input Offset Current		±5 V, ±15 V		25	200	nA
	T_{MIN} to T_{MAX}				500	nA
Offset Current Drift				0.3		nA/°C
Open-Loop Gain	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		2	4		V/mV
	T_{MIN} to T_{MAX}		1.5			V/mV
	R_{LOAD} = 150 Ω		1.5	3		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		3.5	6		V/mV
	T_{MIN} to T_{MAX}		2	5		V/mV
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 150 Ω (50 mA Output)		2	4		V/mV
INPUT CHARACTERISTICS						
Input Resistance				300		kΩ
Input Capacitance				1.5		pF
Input Common-Mode Voltage Range		±5 V	+3.8	+4.3		V
			−2.7	−3.4		V
		±15 V	+13	+14.3		V
			−12	−13.4		V
		0, +5 V	+3.8	+4.3		V
			+1.2	+0.9		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}	±5 V	80	100		dB
	V_{CM} = ±12 V	±15 V	86	120		dB
	T_{MIN} to T_{MAX}	±15 V	80	100		dB

Parameter	Conditions	V_S	Min	Typ	Max	Units
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_{LOAD} = 500 Ω	±5 V	3.3	3.8		±V
	R_{LOAD} = 150 Ω	±5 V	3.2	3.6		±V
	R_{LOAD} = 1 kΩ	±15 V	13.3	13.7		±V
	R_{LOAD} = 500 Ω	±15 V	12.8	13.4		±V
	R_{LOAD} = 500 Ω	0, +5 V	+1.5, +3.5			V
Output Current		±15 V	50			mA
		±5 V	50			mA
		0, +5 V	30			mA
Short-Circuit Current		±15 V		90		mA
Output Resistance	Open Loop			8		Ω
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	f = 5 MHz	±15 V		−80		dB
Gain Flatness Match	G = +1, f = 40 MHz	±15 V		0.2		dB
Slew Rate Match	G = −1	±15 V		10		V/μs
DC						
Input Offset Voltage Match	T_{MIN}–T_{MAX}	±5 V to ±15 V		0.5	2	mV
Input Bias Current Match	T_{MIN}–T_{MAX}	±5 V to ±15 V		0.06	0.8	μA
Open-Loop Gain Match	V_O = ±10 V, R_{LOAD} = 1 kΩ, T_{MIN}–T_{MAX}	±15 V	0.15	0.01		mV/V
Common-Mode Rejection Ratio Match	V_{CM} = ±12 V, T_{MIN}–T_{MAX}	±15 V	80	100		dB
Power Supply Rejection Ratio Match	±5 V to ±15 V, T_{MIN}–T_{MAX}		80	100		dB
POWER SUPPLY						
Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current/Amplifier		±5 V		6.6	7.5	mA
	T_{MIN} to T_{MAX}	±5 V			7.5	mA
		±15 V			7.5	mA
	T_{MIN} to T_{MAX}	±15 V		6.8	7.5	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±15 V, T_{MIN} to T_{MAX}		75	86		dB

NOTE
[1]Full power bandwidth = slew rate/2 π V_{PEAK}.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . See Derating Curves
Small Outline (R) . . . . . See Derating Curves
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Output Short Circuit Duration . . . . . See Derating Curves
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 10 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air: 8-pin plastic package, θ_{JA} = 100°C/watt; 8-pin SOIC package, θ_{JA} = 155°C/watt.

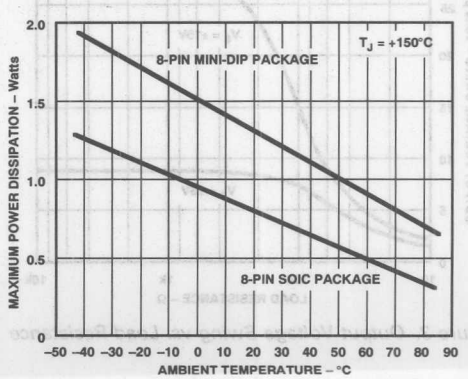
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD826AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD826AR	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD826AR-REEL	−40°C to +85°C	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD826 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.



Maximum Power Dissipation vs. Temperature for Different Package Types

AD826—Typical Characteristics

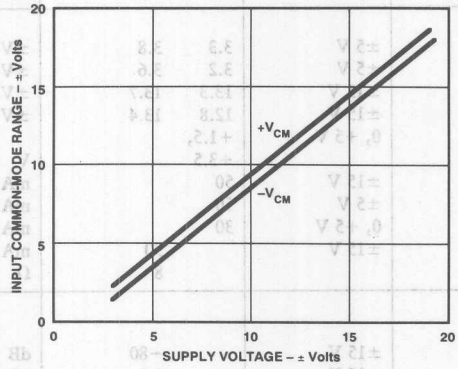


Figure 1. Common-Mode Voltage Range vs. Supply

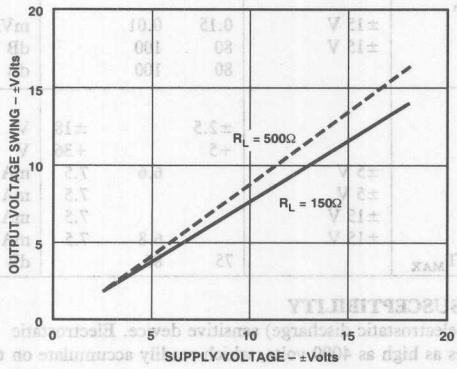


Figure 2. Output Voltage Swing vs. Supply

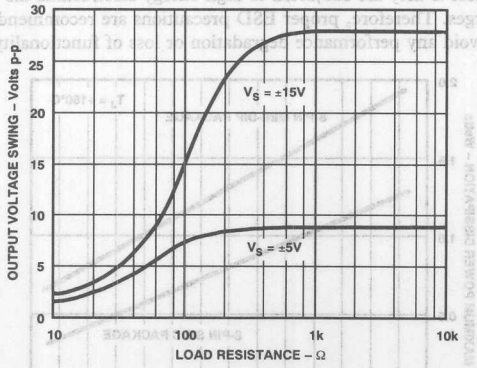


Figure 3. Output Voltage Swing vs. Load Resistance

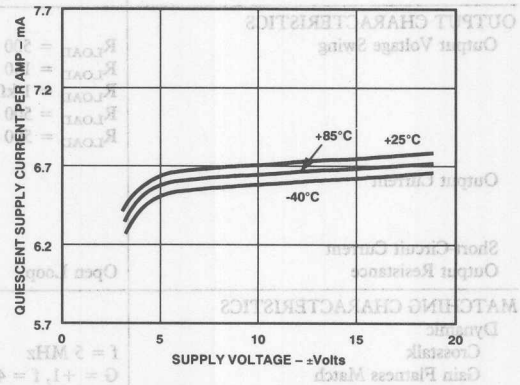


Figure 4. Quiescent Supply Current per Amp vs. Supply Voltage for Various Temperatures

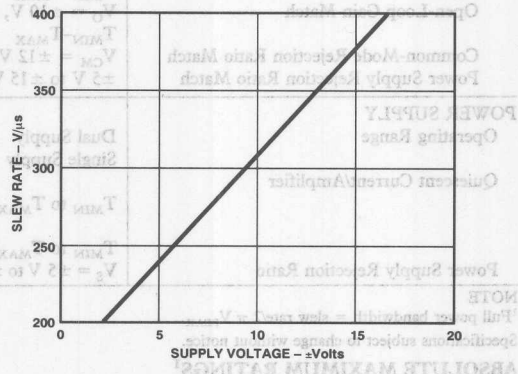


Figure 5. Slew Rate vs. Supply Voltage

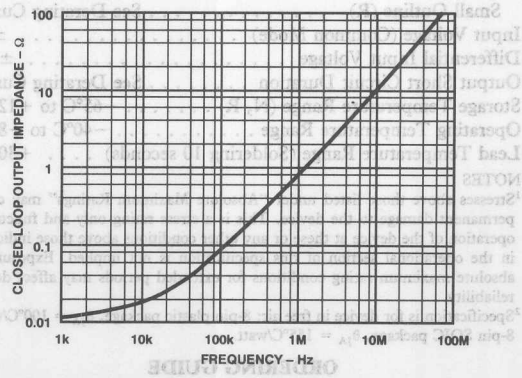


Figure 6. Closed-Loop Output Impedance vs. Frequency

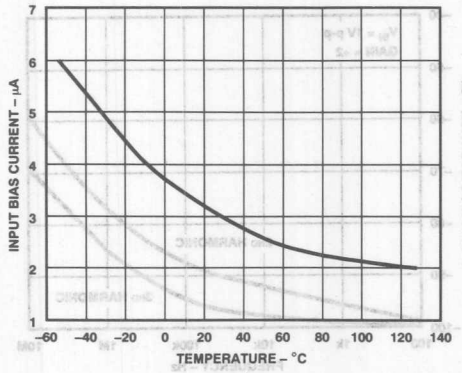


Figure 7. Input Bias Current vs. Temperature

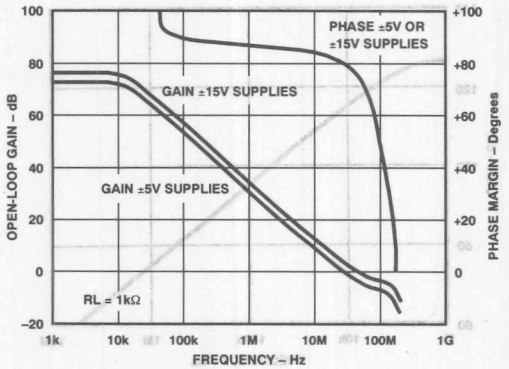


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

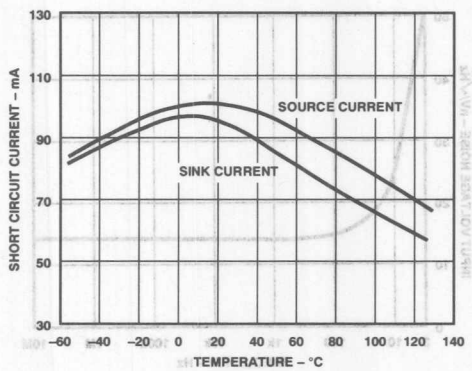


Figure 8. Short Circuit Current vs. Temperature

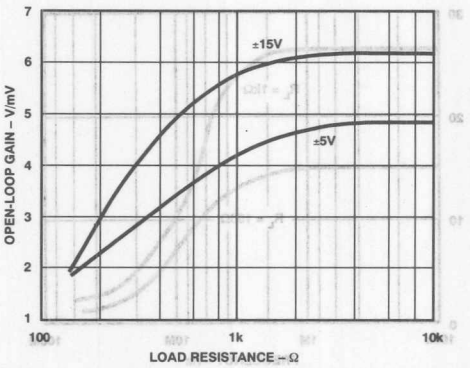


Figure 11. Open-Loop Gain vs. Load Resistance

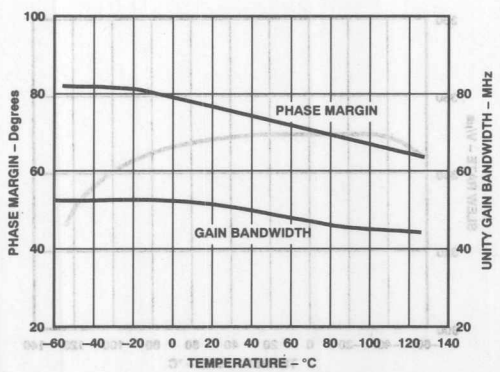


Figure 9. Unity Gain Bandwidth and Phase Margin vs. Temperature

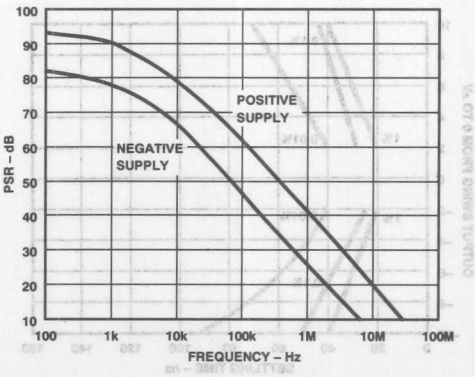


Figure 12. Power Supply Rejection vs. Frequency

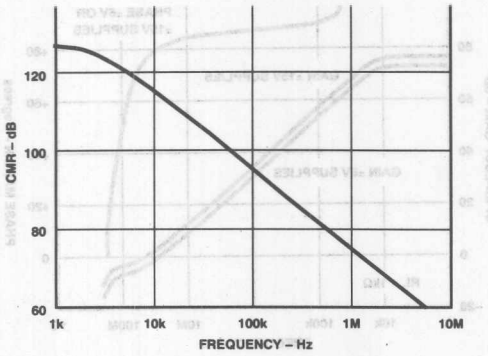


Figure 13. Common-Mode Rejection vs. Frequency

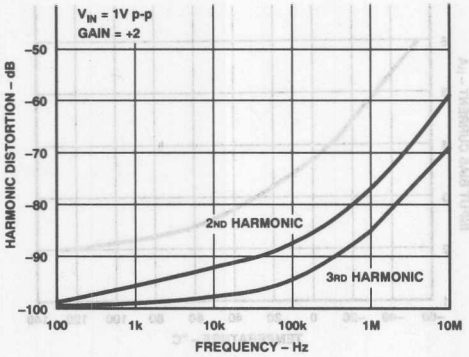


Figure 16. Harmonic Distortion vs. Frequency

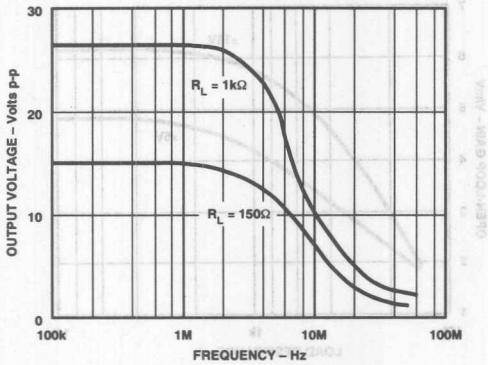


Figure 14. Large Signal Frequency Response

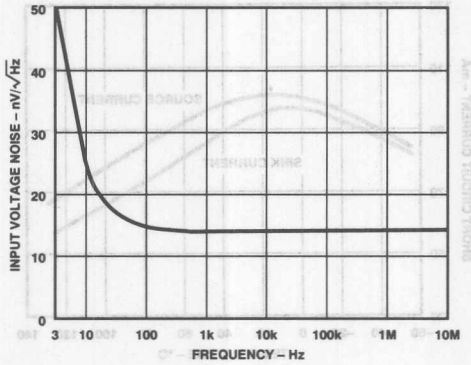


Figure 17. Input Voltage Noise Spectral Density

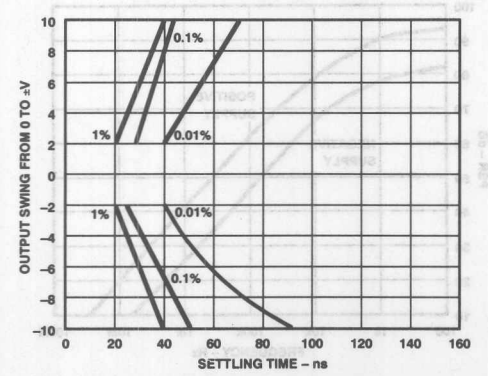


Figure 15. Output Swing and Error vs. Settling Time

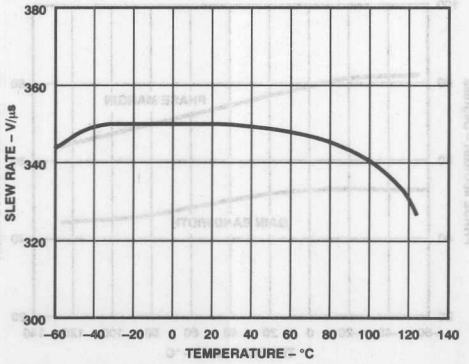


Figure 18. Slew Rate vs. Temperature

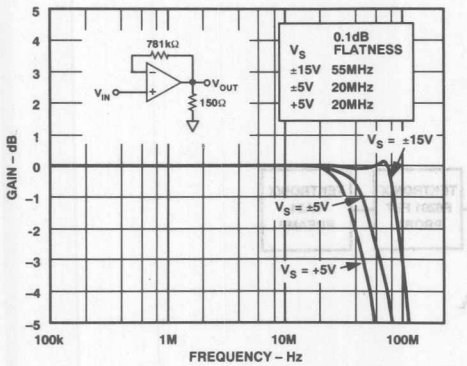


Figure 19. Closed-Loop Gain vs. Frequency

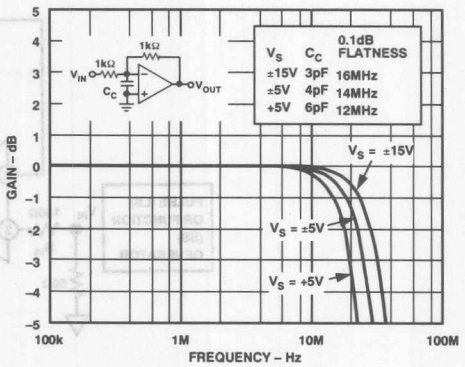


Figure 22. Closed-Loop Gain vs. Frequency, Gain = −1

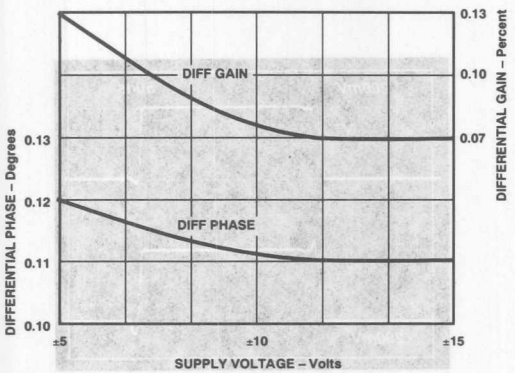


Figure 20. Differential Gain and Phase vs. Supply Voltage

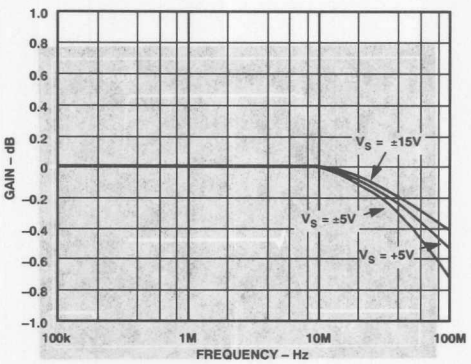


Figure 23. Gain Flatness Matching vs. Supply, G = +1

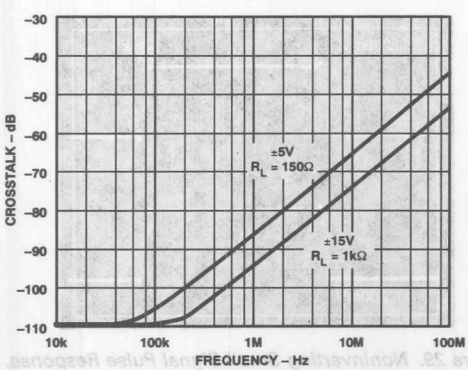


Figure 21. Crosstalk vs. Frequency

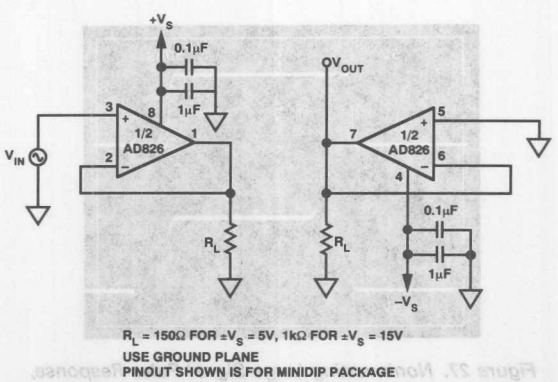


Figure 24. Crosstalk Test Circuit

AD826—Typical Characteristics

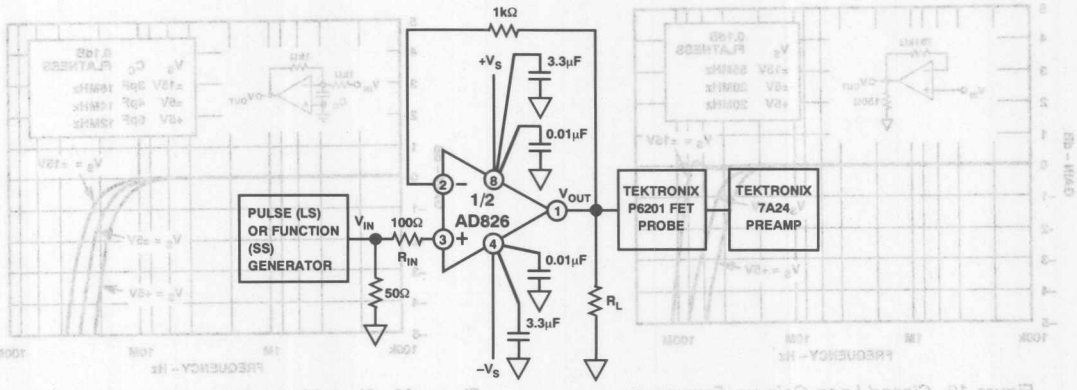


Figure 25. Noninverting Amplifier Configuration

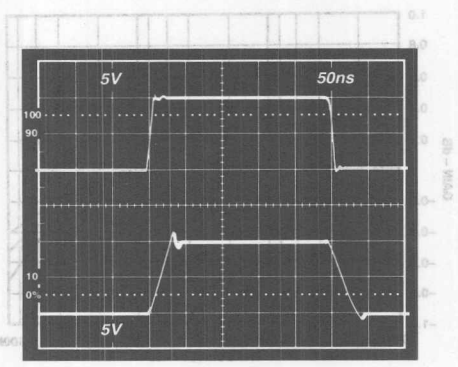


Figure 26. Noninverting Large Signal Pulse Response, R_L = 1 kΩ

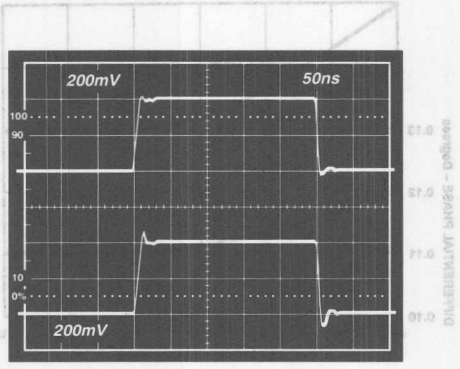


Figure 28. Noninverting Small Signal Pulse Response, R_L = 1 kΩ

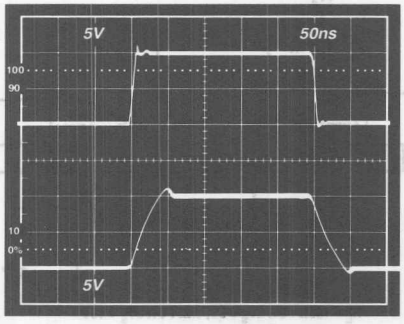


Figure 27. Noninverting Large Signal Pulse Response, R_L = 150 Ω

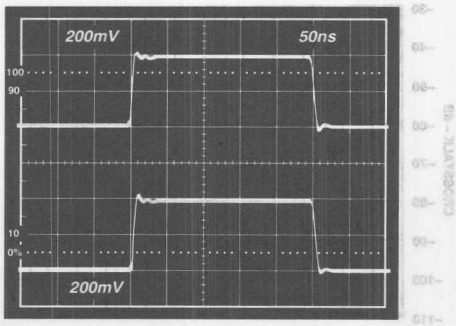


Figure 29. Noninverting Small Signal Pulse Response, R_L = 150 Ω

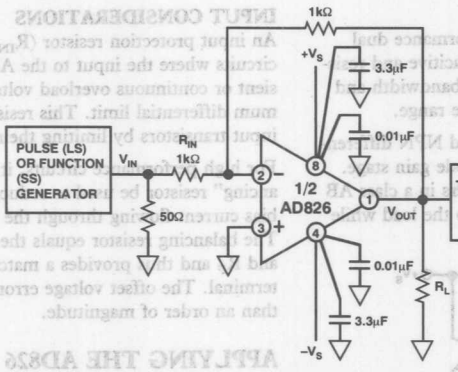


Figure 30. Inverting Amplifier Configuration

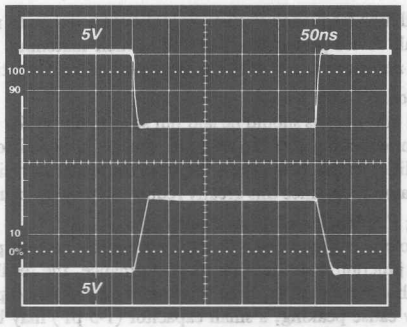


Figure 31. Inverting Large Signal Pulse Response, R_L = 1 kΩ

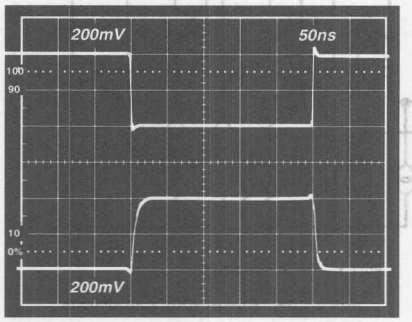


Figure 33. Inverting Small Signal Pulse Response, R_L = 1 kΩ

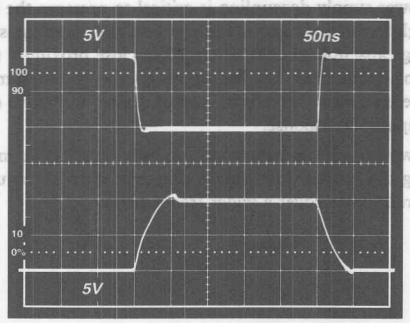


Figure 32. Inverting Large Signal Pulse Response, R_L = 150 Ω

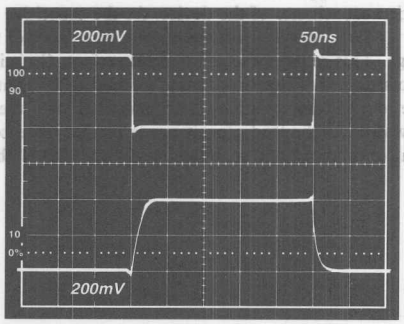


Figure 34. Inverting Small Signal Pulse Response, R_L = 150 Ω

THEORY OF OPERATION

The AD826 is a low cost, wide band, high performance dual operational amplifier which can drive heavy capacitive and resistive loads. It also achieves a constant slew rate, bandwidth and settling time over its entire specified temperature range.

The AD826 (Figure 35) consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which delivers the necessary current to the load while maintaining low levels of distortion.

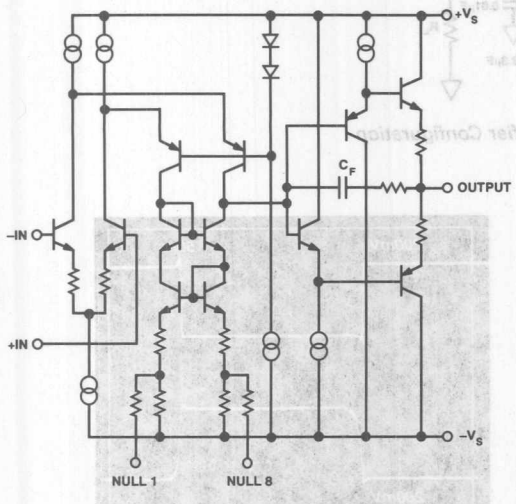


Figure 35. Simplified Schematic

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. With low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, C_F is bootstrapped and does not contribute to the overall compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is incompletely bootstrapped. Effectively, some fraction of C_F contributes to the overall compensation capacitance, reducing the unity gain bandwidth. As the load capacitance is further increased, the bandwidth continues to fall, maintaining the stability of the amplifier.

INPUT CONSIDERATIONS

An input protection resistor (R_{IN} in Figure 25) is required in circuits where the input to the AD826 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a "balancing" resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of R_{IN} and R_F and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

APPLYING THE AD826

The AD826 is a breakthrough dual amp that delivers precision and speed at low cost with low power consumption. The AD826 offers excellent static and dynamic matching characteristics, combined with the ability to drive heavy resistive and capacitive loads.

As with all high frequency circuits, care should be taken to maintain overall device performance as well as their matching. The following items are presented as general design considerations.

Circuit Board Layout

Input and output runs should be laid out so as to physically isolate them from remaining runs. In addition, the feedback resistor of each amplifier should be placed away from the feedback resistor of the other amplifier, since this greatly reduces inter-amp coupling.

Choosing Feedback and Gain Resistors

In order to prevent the stray capacitance present at each amplifier's summing junction from limiting its performance, the feedback resistors should be ≤ 1 kΩ. Since the summing junction capacitance may cause peaking, a small capacitor (1-5 pF) may be paralleled with Rf to neutralize this effect. Finally, sockets should be avoided, because of their tendency to increase interlead capacitance.

Power Supply Bypassing

Proper power supply decoupling is critical to preserve the integrity of high frequency signals. In carefully laid out designs, decoupling capacitors should be placed in close proximity to the supply pins, while their lead lengths should be kept to a minimum. These measures greatly reduce undesired inductive effects on the amplifier's response.

Though two 0.1 μF capacitors will typically be effective in decoupling the supplies, several capacitors of different values can be paralleled to cover a wider frequency range.

±SINGLE SUPPLY OPERATION

An exciting feature of the AD826 is its ability to perform well in a single supply configuration (see Figure 37). The AD826 is ideally suited for applications that require low power dissipation and high output current and those which need to drive large capacitive loads, such as high speed buffering and instrumentation.

Referring to Figure 36, careful consideration should be given to the proper selection of component values. The choices for this particular circuit are: (R1+ R3)||R2 combine with C1 to form a low frequency corner of approximately 30 Hz.

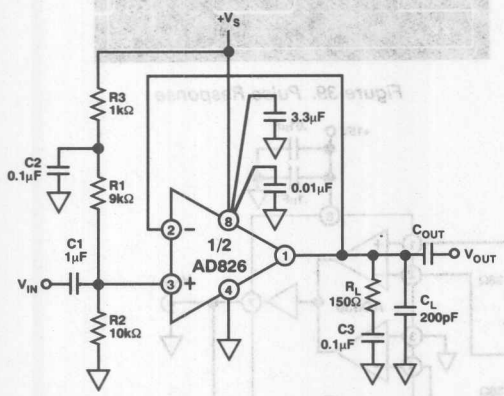


Figure 36. Single Supply Amplifier Configuration

R3 and C2 reduce the effect of the power supply changes on the output by low pass filtering with a corner at $\frac{1}{2\pi R_3 C_2}$.

The values for R_L and C_L were chosen to demonstrate the AD826's exceptional output drive capability. In this configuration, the output is centered around 2.5 V. In order to eliminate the static dc current associated with this level, C3 was inserted in series with R_L.

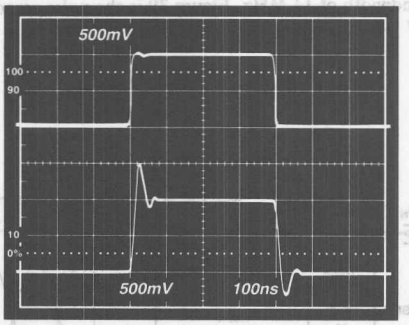


Figure 37. Single Supply Pulse Response, G = +1, R_L = 150 Ω, C_L = 200 pF

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PARALLEL AMPS PROVIDE 100 mA TO LOAD

By taking advantage of the superior matching characteristics of the AD826, enhanced performance can easily be achieved by employing the circuit in Figure 38. Here, two identical cells are paralleled to obtain even higher load driving capability than that of a single amplifier (100 mA min guaranteed). R1 and R2 are included to limit current flow between amplifier outputs that would arise in the presence of any residual mismatch.

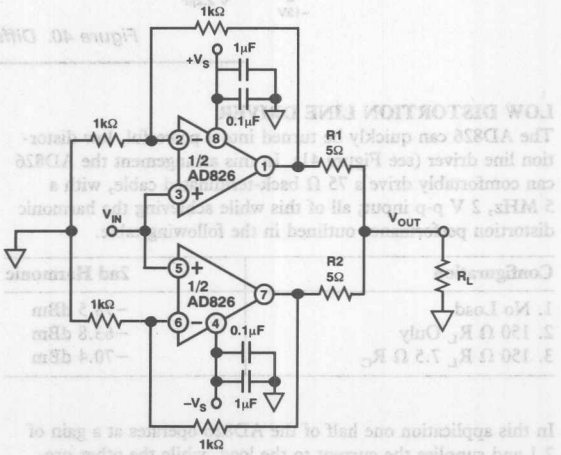

Figure 38. Parallel Amp Configuration

SINGLE-ENDED TO DIFFERENTIAL LINE DRIVER

Outstanding CMRR (>80 dB @ 5 MHz), high bandwidth, wide supply voltage range, and the ability to drive heavy loads, make the AD826 an ideal choice for many line driving applications. In this application, the AD830 high speed video difference amp serves as the differential line receiver on the end of a back terminated, 50 ft., twisted-pair transmission line (see Figure 40). The overall system is configured in a gain of +1 and has a −3 dB bandwidth of 14 MHz. Figure 39 is the pulse response with a 2 V p-p, 1 MHz signal input.

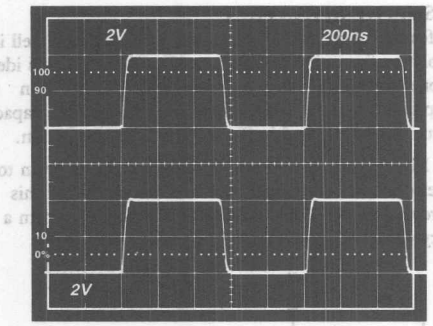

Figure 39. Pulse Response

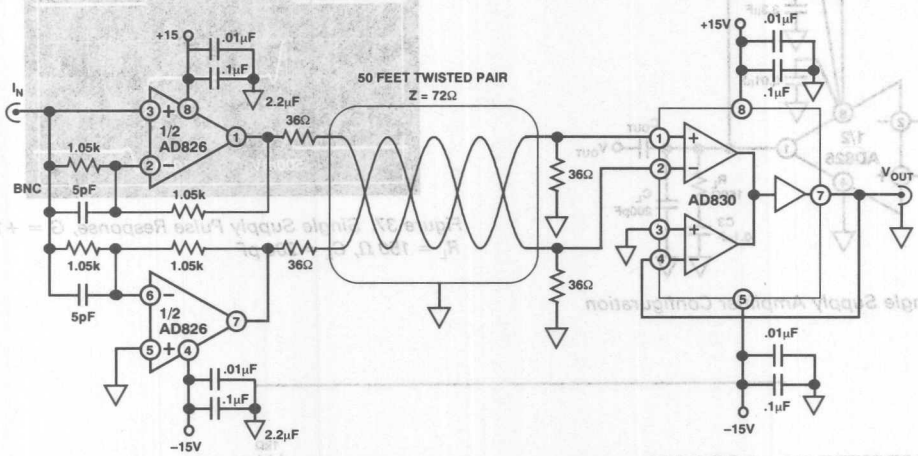

Figure 40. Differential Line Driver

LOW DISTORTION LINE DRIVER

The AD826 can quickly be turned into a powerful, low distortion line driver (see Figure 41). In this arrangement the AD826 can comfortably drive a 75 Ω back-terminated cable, with a 5 MHz, 2 V p-p input; all of this while achieving the harmonic distortion performance outlined in the following table.

Configuration	2nd Harmonic
1. No Load	−78.5 dBm
2. 150 Ω R_L Only	−63.8 dBm
3. 150 Ω R_L 7.5 Ω R_C	−70.4 dBm

In this application one half of the AD826 operates at a gain of 2.1 and supplies the current to the load, while the other provides the overall system gain of 2. This is important for two reasons: the first is to keep the bandwidth of both amplifiers the same, and the second is to preserve the AD826's ability to operate from low supply voltages. R_C varies with the load and must be chosen to satisfy the following equation:

$$R_C = MR_L,$$

where M is defined by $[(M+1)\ G_S = G_D]$ and G_D = Driver's Gain, G_S = System Gain.

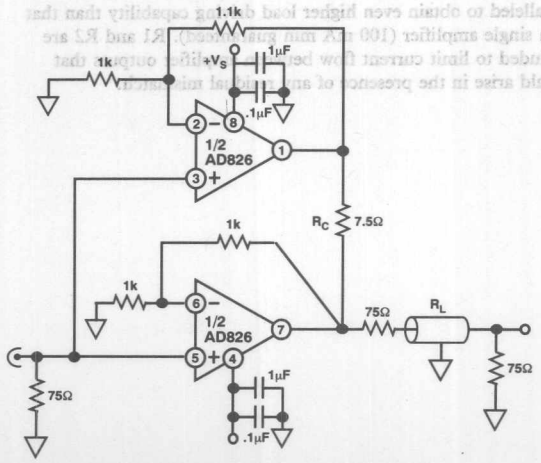

Figure 41. Low Distortion Amplifier

HIGH PERFORMANCE ADC BUFFER

Figure 42 is a schematic of a 12-bit high speed analog-to-digital converter. The AD826 dual op amp takes a single ended input and drives the AD872 A/D converter differentially, thus reducing 2nd harmonic distortion. Figure 43 is a FFT of a 1 MHz input, sampled at 10 MHz with a THD of −78 dB. The AD826 can be used to amplify low level signals so that the entire range of the converter is used. The ability of the AD826 to perform on a ±5 volt supply or even with a single 5 volts combined with its rapid settling time and ability to deliver high current to complicated loads make it a very good flash A/D converter buffer as well as a very useful general purpose building block.

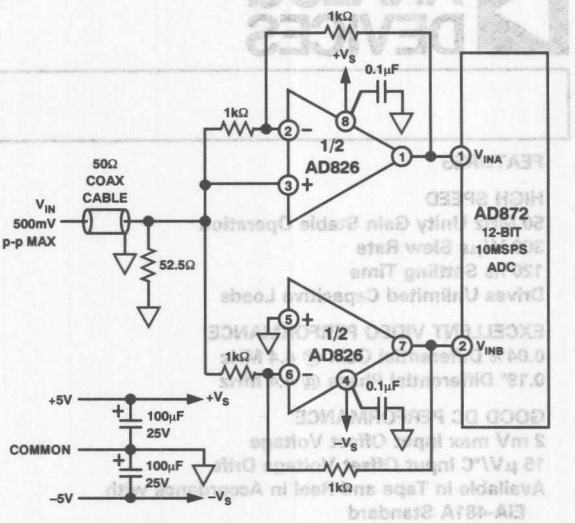

Figure 42. A Differential Input Buffer for High Bandwidth ADCs

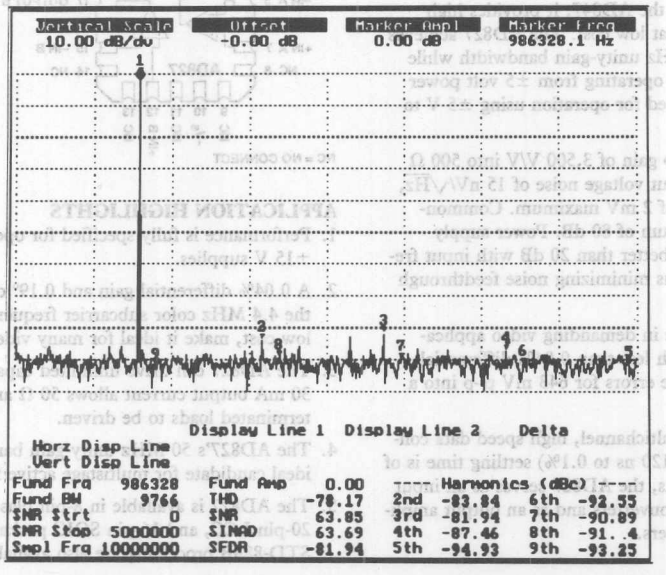

Figure 43. FFT, Buffered A/D Converter

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FEATURES

HIGH SPEED
50 MHz Unity Gain Stable Operation
300 V/μs Slew Rate
120 ns Settling Time
Drives Unlimited Capacitive Loads

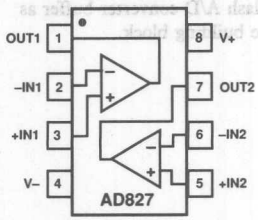
EXCELLENT VIDEO PERFORMANCE
0.04% Differential Gain @ 4.4 MHz
0.19° Differential Phase @ 4.4 MHz

GOOD DC PERFORMANCE
2 mV max Input Offset Voltage
15 μV/°C Input Offset Voltage Drift
Available in Tape and Reel in Accordance with EIA-481A Standard

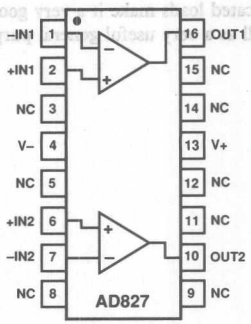
LOW POWER
Only 10 mA Total Supply Current for Both Amplifiers
±5 V to ±15 V Supplies

CONNECTION DIAGRAMS

8-Pin Plastic (N) and Cerdip (Q) Packages

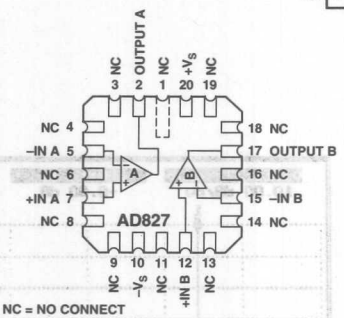


16-Pin Small Outline (R) Package



NC = NO CONNECT

20-Pin LCC (E) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD827 is a dual version of Analog Devices' industry-standard AD847 op amp. Like the AD847, it provides high speed, low power performance at low cost. The AD827 achieves a 300 V/μs slew rate and 50 MHz unity-gain bandwidth while consuming only 100 mW when operating from ±5 volt power supplies. Performance is specified for operation using ±5 V to ±15 V power supplies.

The AD827 offers an open-loop gain of 3,500 V/V into 500 Ω loads. It also features a low input voltage noise of 15 nV/$\sqrt{\text{Hz}}$, and a low input offset voltage of 2 mV maximum. Common-mode rejection ratio is a minimum of 80 dB. Power supply rejection ratio is maintained at better than 20 dB with input frequencies as high as 1 MHz, thus minimizing noise feedthrough from switching power supplies.

The AD827 is also ideal for use in demanding video applications, driving coaxial cables with less than 0.04% differential gain and 0.19° differential phase errors for 643 mV p–p into a 75 Ω reverse terminated cable.

The AD827 is also useful in multichannel, high speed data conversion systems where its fast (120 ns to 0.1%) settling time is of importance. In such applications, the AD827 serves as an input buffer for 8-bit to 10-bit A/D converters and as an output amplifier for high speed D/A converters.

APPLICATION HIGHLIGHTS

1. Performance is fully specified for operation using ±5 V to ±15 V supplies.
2. A 0.04% differential gain and 0.19° differential phase error at the 4.4 MHz color subcarrier frequency, together with its low cost, make it ideal for many video applications.
3. The AD827 can drive unlimited capacitive loads, while its 30 mA output current allows 50 Ω and 75 Ω reverse-terminated loads to be driven.
4. The AD827's 50 MHz unity-gain bandwidth makes it an ideal candidate for multistage active filters.
5. The AD827 is available in 8-pin plastic mini-DIP and cerdip, 20-pin LCC, and 16-pin SOIC packages. Chips and MIL-STD-883B processing are also available.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD827J Min	AD827J Typ	AD827J Max	AD827A/S Min	AD827A/S Typ	AD827A/S Max	Units
DC PERFORMANCE									
Input Offset Voltage[1]		±5 V		0.5	2		0.3	2	mV
	T_{min} to T_{max}				3.5			4	mV
		±15 V			4			4	mV
	T_{min} to T_{max}				6			6	mV
Offset Voltage Drift		±5 V to ±15 V		15			15		µV/°C
Input Bias Current		±5 V to ±15 V		3.3	7		3.3	7	µA
	T_{min} to T_{max}				8.2			9.5	µA
Input Offset Current		±5 V to ±15 V		50	300		50	300	nA
	T_{min} to T_{max}				400			400	nA
Offset Current Drift		±5 V to ±15 V		0.5			0.5		nA/°C
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	±5 V	78	95		80	95		dB
	V_{CM} = ±12 V	±15 V	78	95		80	95		dB
	T_{min} to T_{max}	±5 V to ±15 V	75			75			dB
Power Supply Rejection Ratio		±5 V to ±15 V	75	86		75	86		dB
	T_{min} to T_{max}		72			72			dB
Open-Loop Gain									
	V_O = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		2	3.5		2	3.5		V/mV
	T_{min} to T_{max}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		3	5.5		3	5.5		V/mV
	T_{min} to T_{max}		1.5			1.5			V/mV
MATCHING CHARACTERISTICS									
Input Offset Voltage		±5 V		0.4			0.2		mV
Crosstalk	f = 5 MHz	±5 V		85			85		dB
DYNAMIC PERFORMANCE									
Unity-Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_O = 5 V p–p,								
	R_{LOAD} = 500 Ω	±5 V		12.7			12.7		MHz
	V_O = 20 V p–p,								
	R_{LOAD} = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 500 Ω	±5 V		200			200		V/µs
	R_{LOAD} = 1 kΩ	±15 V		300			300		V/µs
Settling Time to 0.1%	A_V = −1								
	−2.5 V to +2.5 V	±5 V		65			65		ns
	−5 V to +5 V	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			50			50		Degrees
Differential Gain Error	f = 4.4 MHz	±15 V		0.04			0.04		%
Differential Phase Error	f = 4.4 MHz	±15 V		0.19			0.19		Degrees
Input Voltage Noise	f = 10 kHz	±15 V		15			15		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz	±15 V		1.5			1.5		$pA/\sqrt{Hz}$
Input Common-Mode Voltage Range		±5 V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15 V		+14.3			+14.3		V
				−13.4			−13.4		V
Output Voltage Swing	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3.0		2.5	3.0		±V
	R_{LOAD} = 1 kΩ	±15 V	12	13.3		12	13.3		±V
	R_{LOAD} = 500 Ω	±15 V	10	12.2		10	12.2		±V
Short-Circuit Current Limit		±5 V to ±15 V		32			32		mA
INPUT CHARACTERISTICS									
Input Resistance				300			300		kΩ
Input Capacitance				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω

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Model	Conditions	V_S	AD827J Min	AD827J Typ	AD827J Max	AD827A/S Min	AD827A/S Typ	AD827A/S Max	Units
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		10	13		10	13	mA
	T_{min} to T_{max}				16			16.5/17.5	mA
		±15 V		10.5	13.5		10.5	13.5	mA
	T_{min} to T_{max}				16.5			17/18	mA
TRANSISTOR COUNT				92			92		

NOTES

[1]Offset voltage for the AD827 is guaranteed after power is applied and the device is fully warmed up. All other specifications are measured using high speed test equipment, approximately 1 second after power is applied.

[2]Full Power Bandwidth = Slew Rate/2π V_{PEAK}.

[3]Gain = +1, rising edge.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) Package (Derate at 10 mW/°C) . . . . . 1.5 W
Cerdip (Q) Package (Derate at 8.7 mW/°C) . . . . . 1.3 W
Small Outline (R) Package (Derate at 10 mW/°C) . . . . 1.5 W
LCC (E) Package (Derate at 6.7 mW/°C) . . . . . 1.0 W
Input Common Mode Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 6 V
Output Short Circuit Duration[3] . . . . . Indefinite
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Operating Temperature Range
AD827J . . . . . 0 to +70°C
AD827A . . . . . −40°C to +85°C
AD827S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering to 60 sec) . . . . . 300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.
Thermal Characteristics:
Mini-DIP: θ_{JA} = 100°C/Watt; θ_{JC} = 33°C/Watt
Cerdip: θ_{JA} = 110°C/Watt; θ_{JC} = 30°C/Watt
16-Pin Small Outline Package: θ_{JA} = 100°C/Watt
20-Pin LCC: θ_{JA} = 150°C/Watt; θ_{JC} = 35°C/Watt

[3]Indefinite short circuit duration is only permissible as long as the absolute maximum power rating is not exceeded.

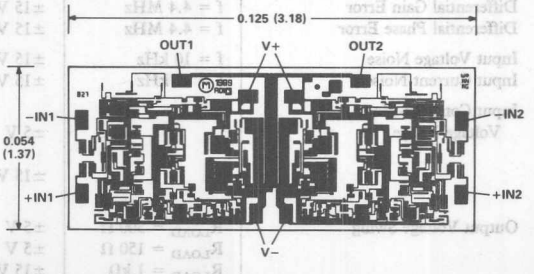
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD827JN	0 to +70°C	8-Pin Plastic DIP	N-8
AD827JR	0 to +70°C	16-Pin Plastic SO	R-16
AD827AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD827SQ	−55°C to +125°C	8-Pin Cerdip	Q-8
AD827SQ/883B	−55°C to +125°C	8-Pin Cerdip	Q-8
5962-9211701MPA	−55°C to +125°C	8-Pin Cerdip	Q-8
AD827SE/883B	−55°C to +125°C	20-Pin LCC	E-20A
5962-9211701M2A	−55°C to +125°C	20-Pin LCC	E-20A
AD827JR-REEL	0 to +70°C	Tape & Reel	
AD827JChips	0 to +70°C	Die	
AD827SChips	−55°C to +125°C	Die	

*For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).
Substrate is connected to V+.



Dual, Low Power Video Op Amp

AD828

FEATURES

Excellent Video Performance
- Differential Gain & Phase Error of 0.01% & 0.05°

High Speed
- 130 MHz 3 dB Bandwidth (G = +2)
- 450 V/μs Slew Rate
- 80 ns Settling Time to 0.01%

Low Power
- 15 mA Max Power Supply Current

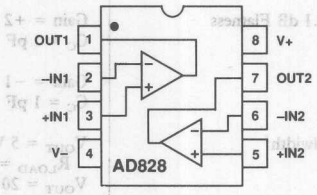
High Output Drive Capability:
- 50 mA Minimum Output Current per Amplifier
- Ideal for Driving Back Terminated Cables

Flexible Power Supply
- Specified for +5 V, ±5 V and ±15 V Operation
- ±3.2 V min Output Swing into a 150 Ω Load (V_S = ±5 V)

Excellent DC Performance
- 2.0 mV Input Offset Voltage

Available in 8-Pin SOIC and 8-Pin Plastic Mini-DIP

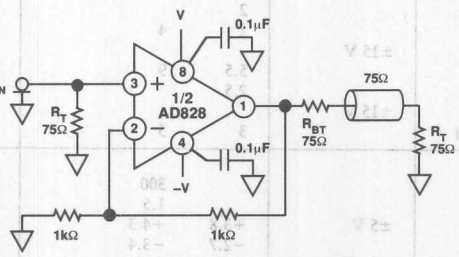
FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD828 is a low cost, dual video op amp optimized for use in video applications which require gains of +2 or greater and high output drive capability, such as cable driving. Due to its low power and single supply functionality, along with excellent differential gain and phase errors, the AD828 is ideal for power sensitive applications such as video cameras and professional video equipment.

With video specs like 0.1 dB flatness to 40 MHz and low differential gain and phase errors of 0.01% and 0.05°, along with 50 mA of output current per amplifier, the AD828 is an excellent choice for any video application. The 130 MHz gain bandwidth and 450 V/μs slew rate make the AD828 useful in many high speed applications including: video monitors, CATV, color copiers, image scanners and fax machines.

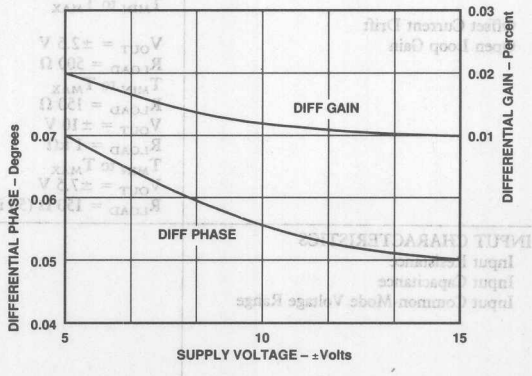


AD828 Video Line Driver

The AD828 is fully specified for operation with a single +5 V power supply and with dual supplies from ±5 V to ±15 V. This power supply flexibility, coupled with a very low supply current of 15 mA and excellent ac characteristics under all power supply conditions, make the AD828 the ideal choice for many demanding yet power sensitive applications.

The AD828 is a voltage feedback op amp which excels as a gain stage (gains >+2) or active filter in high speed and video systems and achieves a settling time of 45 ns to 0.1%, with a low input offset voltage of 2 mV max.

The AD828 is available in low cost, small 8-pin plastic mini-DIP and SOIC packages.



AD828–SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	V_S	AD828 Min	AD828 Typ	AD828 Max	Units
DYNAMIC PERFORMANCE						
−3 dB Bandwidth	Gain = +2	±5 V	60	85		MHz
		±15 V	100	130		MHz
		0, +5 V	30	45		MHz
	Gain = −1	±5 V	35	55		MHz
		±15 V	60	90		MHz
		0, +5 V	20	35		MHz
Bandwidth for 0.1 dB Flatness	Gain = +2	±5 V	30	43		MHz
	C_C = 1 pF	±15 V	30	40		MHz
		0, +5 V	10	18		MHz
	Gain = −1	±5 V	15	25		MHz
	C_C = 1 pF	±15 V	30	50		MHz
		0, +5 V	10	19		MHz
Full Power Bandwidth[1]	V_{OUT} = 5 V p-p					
	R_{LOAD} = 500 Ω	±5 V		22.3		MHz
	V_{OUT} = 20 V p-p					
	R_{LOAD} = 1 kΩ	±15 V		7.2		MHz
Slew Rate	R_{LOAD} = 1 kΩ	±5 V	300	350		V/μs
	Gain = −1	±15 V	400	450		V/μs
		0, +5 V	200	250		V/μs
Settling Time to 0.1%	−2.5 V to +2.5 V	±5 V		45		ns
	0–10 V Step, A_V = −1	±15 V		45		ns
to 0.01%	−2.5 V to +2.5 V	±5 V		80		ns
	0–10 V Step, A_V = −1	±15 V		80		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	F_C = 1 MHz	±15 V		−78		dB
Input Voltage Noise	f = 10 kHz	±5 V, ±15 V		10		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz	±5 V, ±15 V		1.5		$pA/\sqrt{Hz}$
Differential Gain Error	NTSC	±15 V		0.01	0.02	%
(R_L = 150 Ω)	Gain = +2	±5 V		0.02	0.03	%
		0, +5 V		0.08		%
Differential Phase Error	NTSC	±15 V		0.05	0.09	Degrees
(R_L = 150 Ω)	Gain = +2	±5 V		0.07	0.1	Degrees
		0, +5 V		0.1		Degrees
DC PERFORMANCE						
Input Offset Voltage		±5 V, ±15 V		0.5	2	mV
	T_{MIN} to T_{MAX}				3	mV
Offset Drift				10		μV/°C
Input Bias Current		±5 V, ±15 V		3.3	6.6	μA
	T_{MIN}				10	μA
	T_{MAX}				4.4	μA
Input Offset Current		±5 V, ±15 V		25	200	nA
	T_{MIN} to T_{MAX}				500	nA
Offset Current Drift				0.3		nA/°C
Open Loop Gain	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		3	5		V/mV
	T_{MIN} to T_{MAX}		2			V/mV
	R_{LOAD} = 150 Ω		2	4		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		5.5	9		V/mV
	T_{MIN} to T_{MAX}		2.5			V/mV
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 150 Ω (50 mA Output)		3	5		V/mV
INPUT CHARACTERISTICS						
Input Resistance				300		kΩ
Input Capacitance				1.5		pF
Input Common-Mode Voltage Range		±5 V	+3.8	+4.3		V
			−2.7	−3.4		V
		±15 V	+13	+14.3		V
			−12	−13.4		V
		0, +5 V	+3.8	+4.3		V
			+1.2	+0.9		V
Common-Mode Rejection Ratio	V_{CM} = +2.5 V, T_{MIN}–T_{MAX}	±5 V	82	100		dB
	V_{CM} = ±12 V	±15 V	86	120		dB
	T_{MIN} to T_{MAX}	±15 V	84	100		dB

Parameter	Conditions	V_S	AD828 Min	AD828 Typ	AD828 Max	Units
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_{LOAD} = 500 Ω	±5 V	3.3	3.8		±V
	R_{LOAD} = 150 Ω	±5 V	3.2	3.6		±V
	R_{LOAD} = 1 kΩ	±15 V	13.3	13.7		±V
	R_{LOAD} = 500 Ω	±15 V	12.8	13.4		±V
	R_{LOAD} = 500 Ω	0, +5 V	+1.5, +3.5			±V
Output Current		±15 V	50			mA
		±5 V	40			mA
		0, +5 V	30			mA
Short-Circuit Current		±15 V		90		mA
Output Resistance	Open Loop			8		Ω
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	f = 5 MHz	±15 V		−80		dB
Gain Flatness Match	G = +1, f = 40 MHz	±15 V		0.2		dB
Skew Rate Match	G = −1	±15 V		10		V/μs
DC						
Input Offset Voltage Match	T_{MIN}–T_{MAX}	±5 V, ±15 V		0.5	2	mV
Input Bias Current Match	T_{MIN}–T_{MAX}	±5 V, ±15 V		0.06	0.8	μA
Open-Loop Gain Match	V_O = ±10 V, R_L = 1 kΩ T_{MIN}–T_{MAX}	±15 V		0.01	0.15	mV/V
Common-Mode Rejection Ratio Match	V_{CM} = ±12 V, T_{MIN}–T_{MAX}	±15 V	80	100		dB
Power Supply Rejection Ratio Match	±5 V to ±15 V, T_{MIN}–T_{MAX}		80	100		dB
POWER SUPPLY						
Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current		±5V		14.0	15	mA
	T_{MIN} to T_{MAX}	±5 V		14.0	15	mA
	T_{MIN} to T_{MAX}	±5 V			15	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±15 V, T_{MIN}–T_{MAX}		80	90		dB

NOTES
[1]Full power bandwidth = slew rate/2 π V_{PEAK}.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

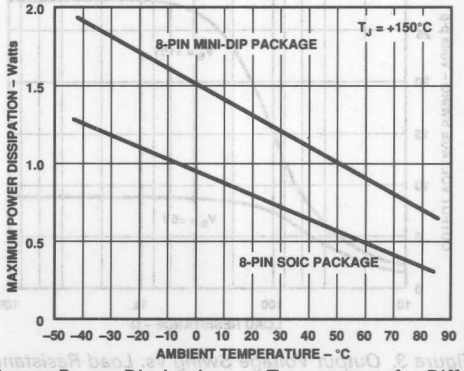
Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic DIP (N) . . . . . See Derating Curves
Small Outline (R) . . . . . See Derating Curves
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Output Short Circuit Duration . . . . . See Derating Curves
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 10 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin Plastic DIP Package: θ_{JA} = 100°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD828AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD828AR	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD828AR-REEL	−40°C to +85°C	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.



Maximum Power Dissipation vs. Temperature for Different Package Types

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD828 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

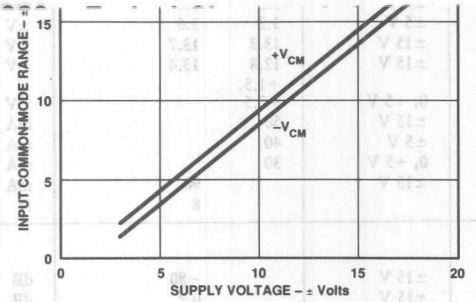


Figure 1. Common-Mode Voltage Range vs. Supply Voltage

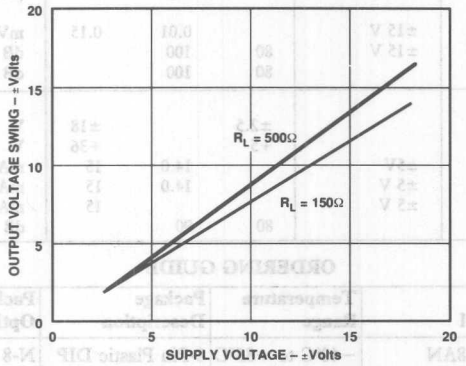


Figure 2. Output Voltage Swing vs. Supply Voltage

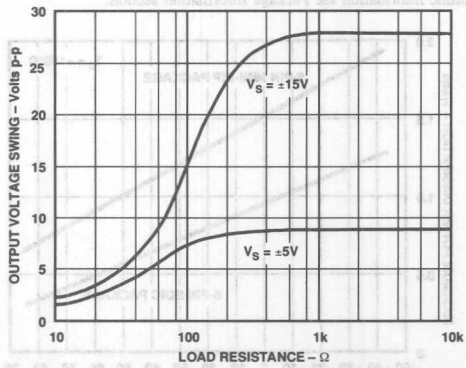


Figure 3. Output Voltage Swing vs. Load Resistance

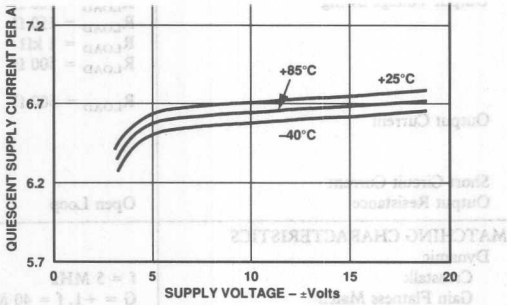


Figure 4. Quiescent Supply Current per Amp vs. Supply Voltage for Various Temperatures

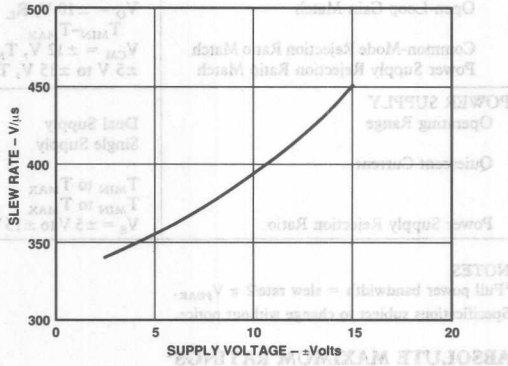


Figure 5. Slew Rate vs. Supply Voltage

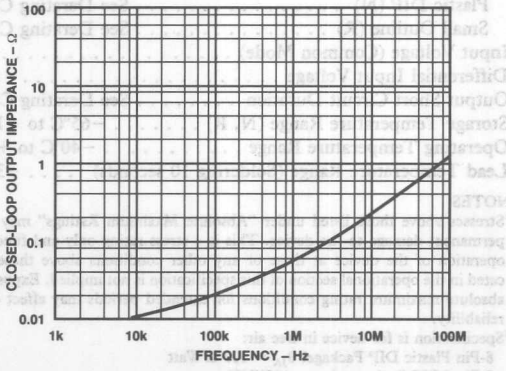


Figure 6. Closed-Loop Output Impedance vs. Frequency

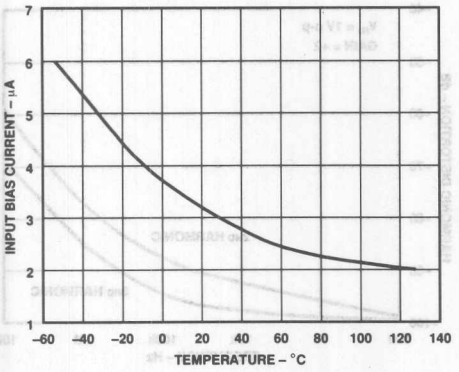


Figure 7. Input Bias Current vs. Temperature

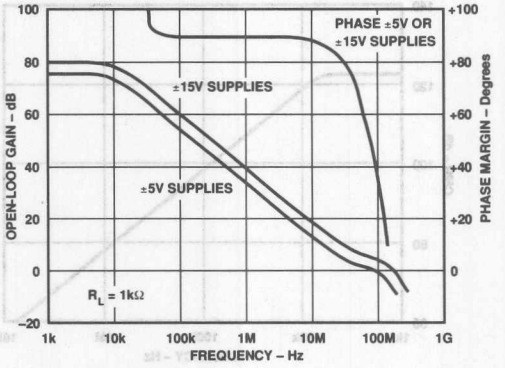


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

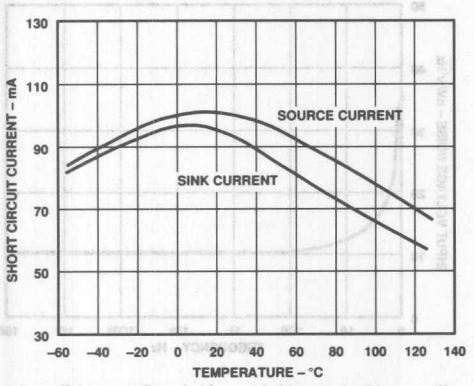


Figure 8. Short Circuit Current vs. Temperature

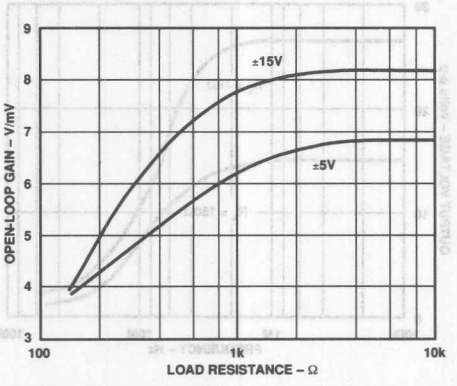


Figure 11. Open-Loop Gain vs. Load Resistance

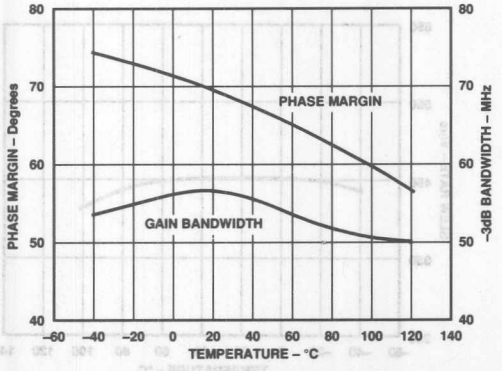


Figure 9. −3 dB Bandwidth and Phase Margin vs. Temperature. Gain = +2

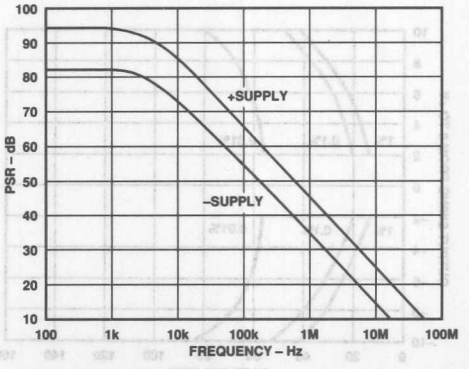


Figure 12. Power Supply Rejection vs. Frequency

9

AD828—Typical Characteristics

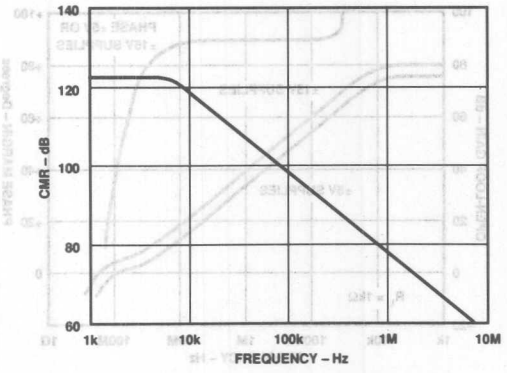


Figure 13. Common-Mode Rejection vs. Frequency

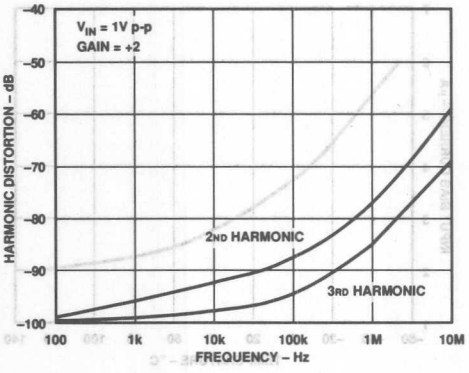


Figure 16. Harmonic Distortion vs. Frequency

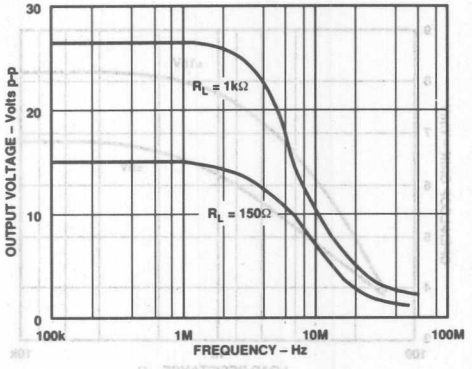


Figure 14. Large Signal Frequency Response

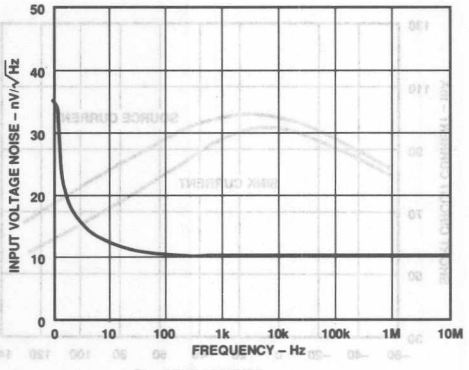


Figure 17. Input Voltage Noise Spectral Density vs. Frequency

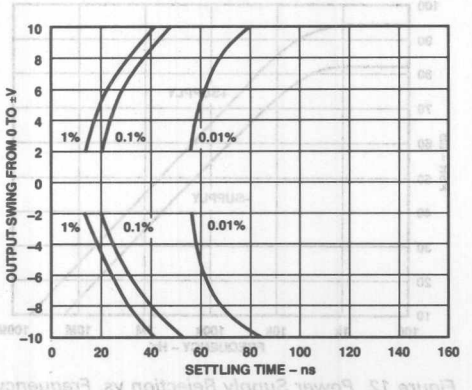


Figure 15. Output Swing and Error vs. Settling Time

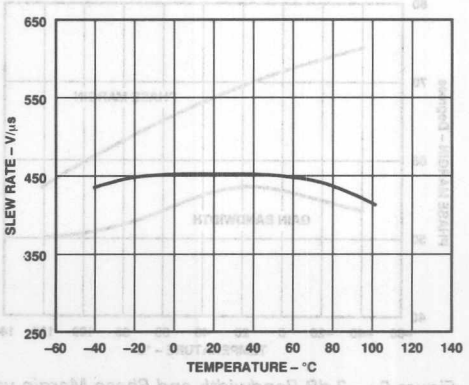


Figure 18. Slew Rate vs. Temperature

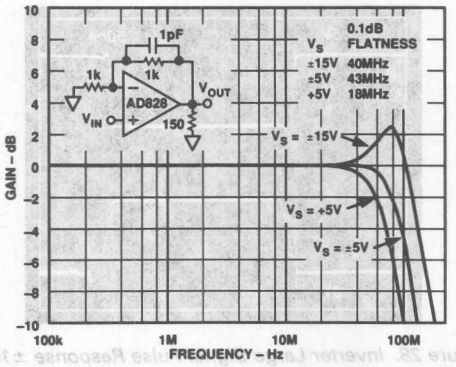


Figure 19. Closed-Loop Gain vs. Frequency

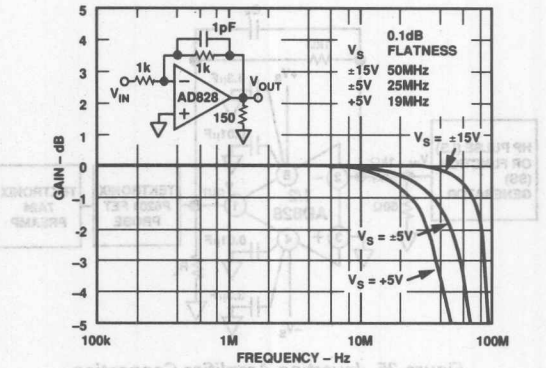


Figure 22. Closed-Loop Gain vs. Frequency, G = −1

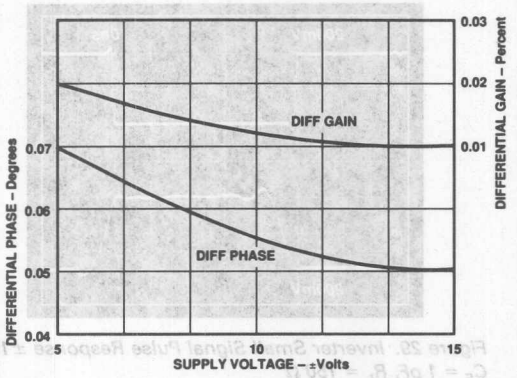


Figure 20. Differential Gain and Phase vs. Supply Voltage

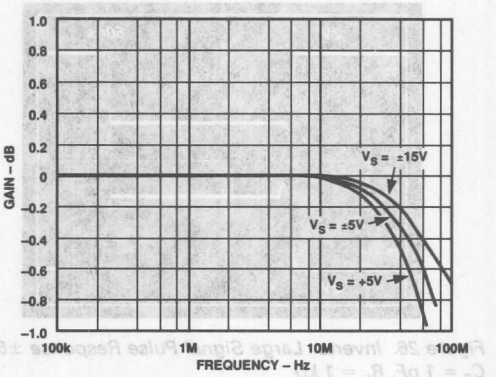


Figure 23. Gain Flatness Matching vs. Supply, G = +2

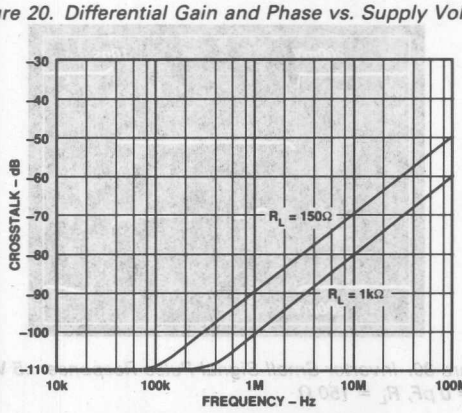


Figure 21. Crosstalk vs. Frequency

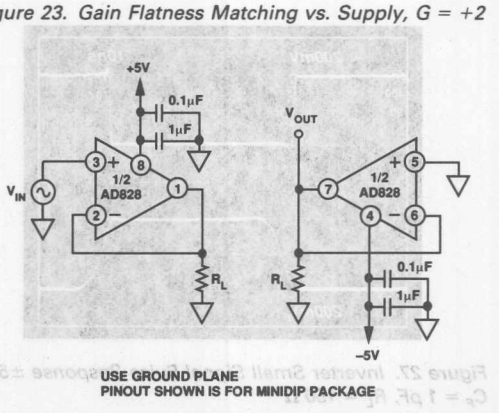


Figure 24. Crosstalk Test Circuit

AD828—Typical Characteristics

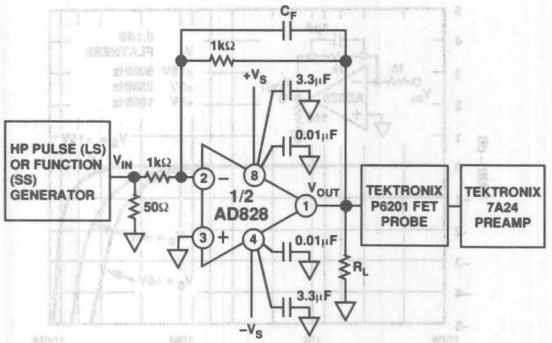


Figure 25. Inverting Amplifier Connection

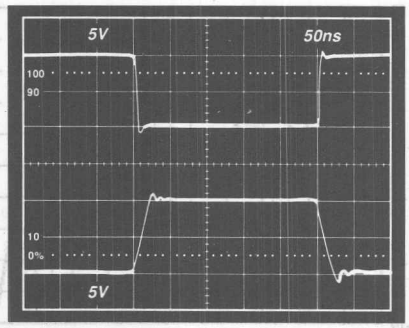


Figure 28. Inverter Large Signal Pulse Response ±15 V_S, C_F = 1 pF, R_L = 1 kΩ

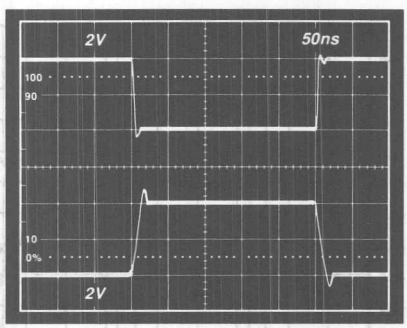


Figure 26. Inverter Large Signal Pulse Response ±5 V_S, C_F = 1 pF, R_L = 1 kΩ

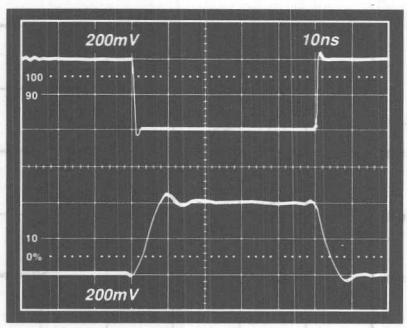


Figure 29. Inverter Small Signal Pulse Response ±15 V_S, C_F = 1 pF, R_L = 150 Ω

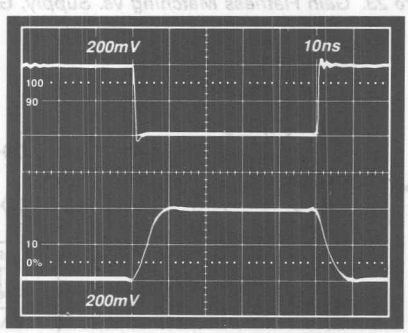


Figure 27. Inverter Small Signal Pulse Response ±5 V_S, C_F = 1 pF, R_L = 150 Ω

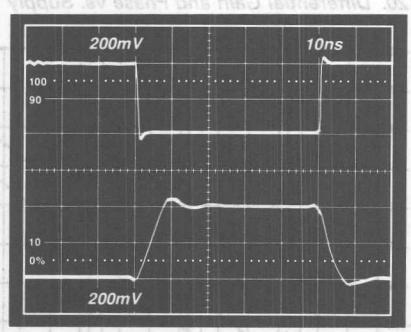


Figure 30. Inverter Small Signal Pulse Response ±5 V_S C_F = 0 pF, R_L = 150 Ω

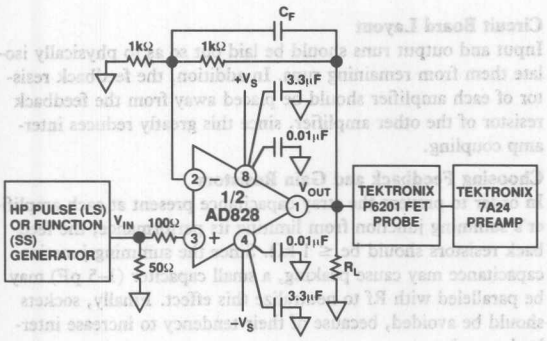


Figure 31. Noninverting Amplifier Connection

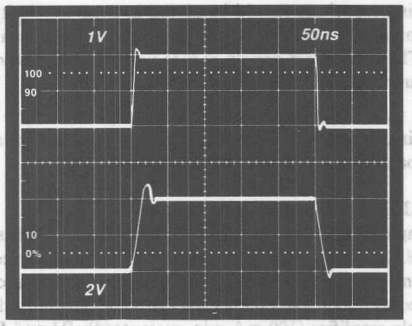


Figure 32. Noninverting Large Signal Pulse Response ± 5 V_S, C_F = 1 pF, R_L = 1 kΩ

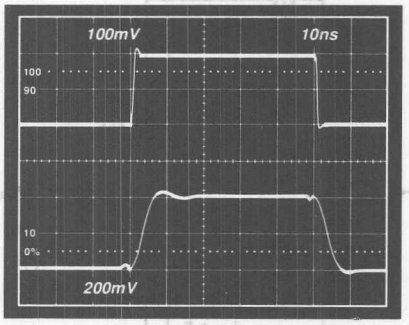


Figure 33. Noninverting Small Signal Pulse Response ± 5 V_S, C_F = 1 pF, R_L = 150 Ω

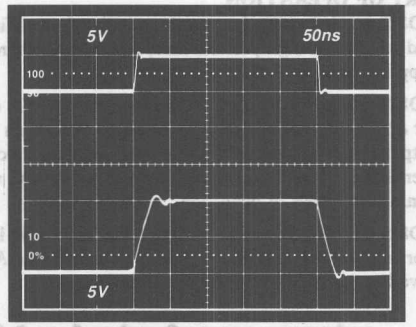


Figure 34. Noninverting Large Signal Pulse Response ± 15 V_S, C_F = 1 pF, R_L = 1 kΩ

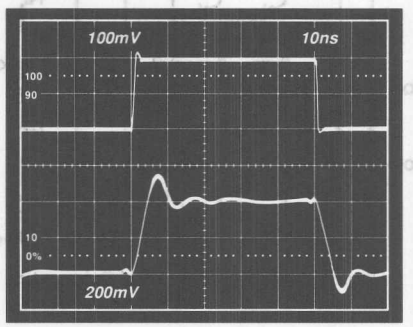


Figure 35. Noninverting Small Signal Pulse Response ± 15 V_S, C_F = 1 pF, R_L = 150 Ω

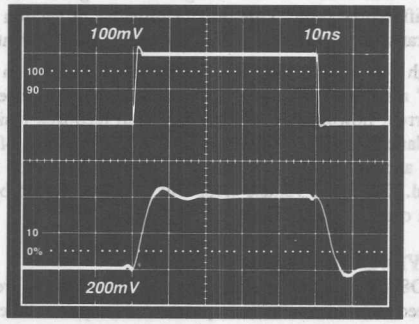


Figure 36. Noninverting Small Signal Pulse Response ± 5 V_S, C_F = 0 pF, R_L = 150 Ω

9

THEORY OF OPERATION

The AD828 is a low cost, dual video operational amplifier designed to excel in high performance, high output current video applications.

The AD828 (Figure 37) consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier that delivers the necessary current to the load while maintaining low levels of distortion.

The AD828 will drive terminated cables and capacitive loads of 10 pF or less. As the closed-loop gain is increased, the AD828 will drive heavier cap loads without oscillating.

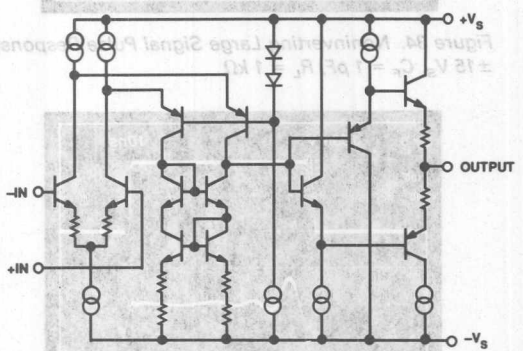


Figure 37. AD828 Simplified Schematic

INPUT CONSIDERATIONS

An input protection resistor (R_{IN} in Figure 31) is required in circuits where the input to the AD828 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a "balancing" resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of R_{IN} and R_F and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

APPLYING THE AD828

The AD828 is a breakthrough dual amp that delivers precision and speed at low cost with low power consumption. The AD828 offers excellent static and dynamic matching characteristics, combined with the ability to drive heavy resistive loads.

As with all high frequency circuits, care should be taken to maintain overall device performance as well as their matching. The following items are presented as general design considerations.

Circuit Board Layout

Input and output runs should be laid out so as to physically isolate them from remaining runs. In addition, the feedback resistor of each amplifier should be placed away from the feedback resistor of the other amplifier, since this greatly reduces interamp coupling.

Choosing Feedback and Gain Resistors

In order to prevent the stray capacitance present at each amplifier's summing junction from limiting its performance, the feedback resistors should be ≤ 1 kΩ. Since the summing junction capacitance may cause peaking, a small capacitor (1–5 pF) may be paralleled with Rf to neutralize this effect. Finally, sockets should be avoided, because of their tendency to increase interlead capacitance.

Power Supply Bypassing

Proper power supply decoupling is critical to preserve the integrity of high frequency signals. In carefully laid out designs, decoupling capacitors should be placed in close proximity to the supply pins, while their lead lengths should be kept to a minimum. These measures greatly reduce undesired inductive effects on the amplifier's response.

Though two 0.1 μF capacitors will typically be effective in decoupling the supplies, several capacitors of different values can be paralleled to cover a wider frequency range.

PARALLEL AMPS PROVIDE 100 mA TO LOAD

By taking advantage of the superior matching characteristics of the AD828, enhanced performance can easily be achieved by employing the circuit in Figure 38. Here, two identical cells are paralleled to obtain even higher load driving capability than that of a single amplifier (100 mA min guaranteed). R1 and R2 are included to limit current flow between amplifier outputs that would arise in the presence of any residual mismatch.

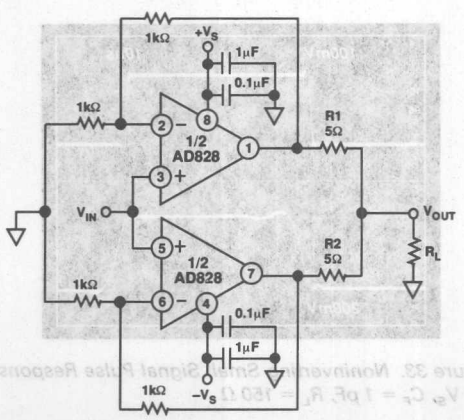


Figure 38. Parallel Amp Configuration

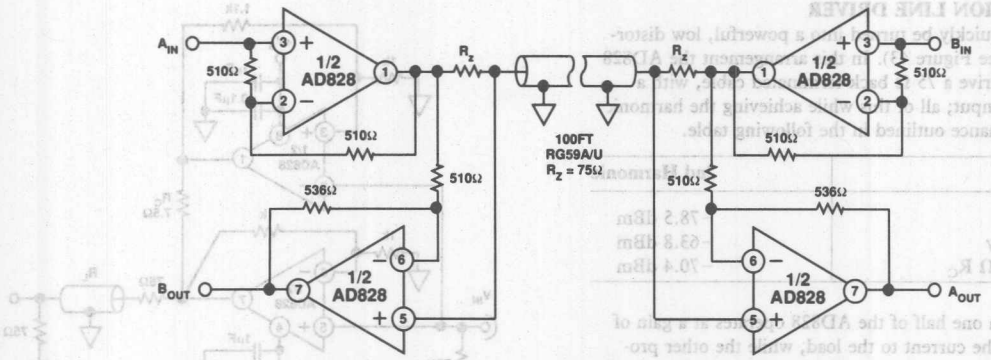


Figure 39. Bidirectional Transmission CKT

Full-Duplex Transmission

Superior load handling capability (50 mA min/amp), high bandwidth, wide supply voltage range and excellent crosstalk rejection makes the AD828 an ideal choice even for the most demanding high speed transmission applications.

The schematic below shows a pair of AD828s configured to drive 100 feet of coaxial cable in a full-duplex fashion.

Two different NTSC video signals are simultaneously applied at A_{IN} and B_{IN} and are recovered at A_{OUT} and B_{OUT}, respectively. This situation is illustrated in Figures 40 and 41. These pictures clearly show that each input signal appears undisturbed at its output, while the unwanted signal is eliminated at either receiver.

The transmitters operate as followers, while the receivers' gain is chosen to take full advantage of the AD828's unparalled CMRR. (In practice this gain is adjusted slightly from its theoretical value to compensate for cable nonidealities and losses.) R_Z is chosen to match the characteristic impedance of the cable employed.

Finally, although a coaxial cable was used, the same topology applies unmodified to a variety of cables (such, as twisted pairs often used in telephony).

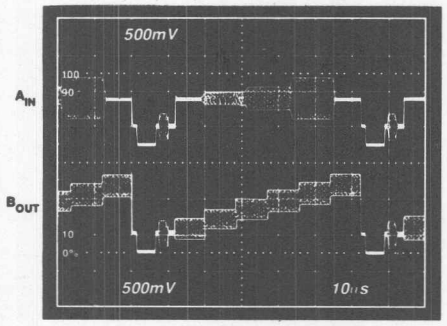


Figure 40. A Transmission/B Reception

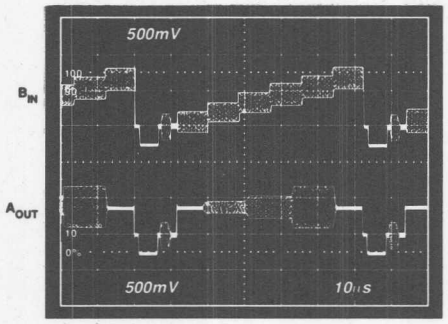


Figure 41. B Transmission/A Reception

A High Performance Video Line Driver

The buffer circuit shown in Figure 42 will drive a back-terminated 75 Ω video line to standard video levels (1 V p-p) with 0.1 dB gain flatness to 40 MHz with only 0.05° and 0.01% differential phase and gain at the 3.58 MHz NTSC subcarrier frequency. This level of performance, which meets the requirements for high-definition video displays and test equipment, is achieved using only 7 mA quiescent current/amplifier.

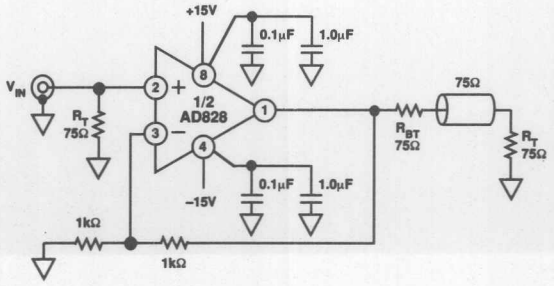


Figure 42. Video Line Driver

tion line driver (see Figure 43). In this arrangement the AD828 can comfortably drive a 75 Ω back-terminated cable, with a 5 MHz, 2 V p-p input; all of this while achieving the harmonic distortion performance outlined in the following table.

Configuration	2nd Harmonic
1. No Load	−78.5 dBm
2. 150 Ω R_L Only	−63.8 dBm
3. 150 Ω R_L 7.5 Ω R_C	−70.4 dBm

In this application one half of the AD828 operates at a gain of 2.1 and supplies the current to the load, while the other provides the overall system gain of 2. This is important for two reasons: the first is to keep the bandwidth of both amplifiers the same, and the second is to preserve the AD828's ability to operate from low supply voltage. R_C varies with the load and must be chosen to satisfy the following equation:

$$R_C = MR_L,$$

where M is defined by $[(M+1)\ G_S = G_D]$ and G_D = Driver's Gain, G_S = System Gain.

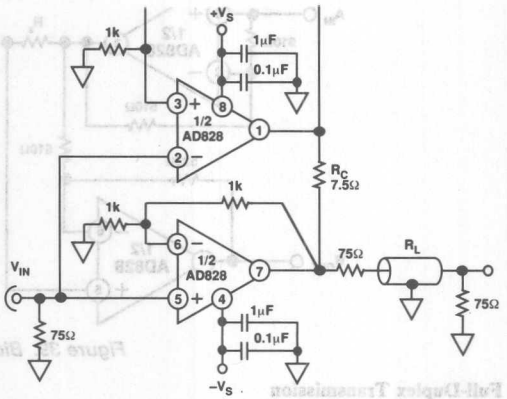


Figure 43. Low Distortion Amplifier

High Speed, Low Noise Video Op Amp

AD829

FEATURES

High Speed
- 120 MHz Bandwidth, Gain = −1
- 230 V/μs Slew Rate
- 90 ns Settling Time to 0.1%

Ideal for Video Applications
- 0.02% Differential Gain
- 0.04° Differential Phase

Low Noise
- 1.7 nV/√Hz Input Voltage Noise
- 1.5 pA/√Hz Input Current Noise

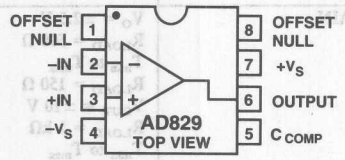
Excellent DC Precision
- 1 mV max Input Offset Voltage (Over Temp)
- 0.3 μV/°C Input Offset Drift

Flexible Operation
- Specified for ±5 V to ±15 V Operation
- ±3 V Output Swing into a 150 Ω Load
- External Compensation for Gains 1 to 20
- 5 mA Supply Current

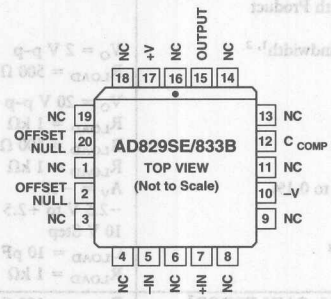
Available in Tape and Reel in Accordance with EIA-481A Standard

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



20-Pin LCC Pinout



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD829 is a low noise (1.7 nV/√Hz), high speed op amp with custom compensation that provides the user with gains from ±1 to ±20 while maintaining a bandwidth greater than 50 MHz. The AD829's 0.04° differential phase and 0.02% differential gain performance at 3.58 MHz and 4.43 MHz, driving reverse-terminated 50 Ω or 75 Ω cables, makes it ideally suited for professional video applications. The AD829 achieves its 230 V/μs uncompensated slew rate and 750 MHz gain bandwidth product while requiring only 5 mA of current from the power supplies.

The AD829's external compensation pin gives it exceptional versatility. For example, compensation can be selected to optimize the bandwidth for a given load and power supply voltage. As a gain-of-two line driver, the −3 dB bandwidth can be increased to 95 MHz at the expense of 1 dB of peaking. In addition, the AD829's output can also be clamped at its external compensation pin.

The AD829 has excellent dc performance. It offers a minimum open-loop gain of 30 V/mV into loads as low as 500 Ω, low input voltage noise of 1.7 nV/√Hz, and a low input offset voltage of 1 mV maximum. Common-mode rejection and power supply rejection ratios are both 120 dB.

The AD829 is also useful in multichannel, high speed data conversion where its fast (90 ns to 0.1%) settling time is of importance. In such applications, the AD829 serves as an input buffer for 8-to-10-bit A/D converters and as an output I/V converter for high speed D/A converters.

The AD829 provides many of the same advantages that a transimpedance amplifier offers, while operating as a traditional voltage feedback amplifier. A bandwidth greater than 50 MHz can be maintained for a range of gains by changing the external compensation capacitor. The AD829 and the transimpedance amplifier are both unity gain stable and provide similar voltage noise performance (1.7 nV/√Hz). However, the current noise of the AD829 (1.5 pA/√Hz) is less than 10% of the noise of transimpedance amps. Furthermore, the inputs of the AD829 are symmetrical.

PRODUCT HIGHLIGHTS

1. Input voltage noise of 2 nV/√Hz, current noise of 1.5 pA/√Hz and 50 MHz bandwidth, for gains of 1 to 20, make the AD829 an ideal preamp.
2. Differential phase error of 0.04° and a 0.02% differential gain error, at the 3.58 MHz NTSC and 4.43 MHz PAL and SECAM color subcarrier frequencies, make it an outstanding video performer for driving reverse-terminated 50 Ω and 75 Ω cables to ±1 V (at their terminated end).
3. The AD829 can drive heavy capacitive loads.
4. Performance is fully specified for operation from ±5 V to ±15 V supplies.
5. Available in plastic, cerdip, and small outline packages. Chips and MIL-STD-883B parts are also available.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD829—SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	Conditions	V_S	AD829J Min	AD829J Typ	AD829J Max	AD829 A/S Min	AD829 A/S Typ	AD829 A/S Max	Units
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.2	1		0.1	0.5	mV
	T_{min} to T_{max}				1			0.5	mV
Offset Voltage Drift		±5 V, ±15 V		0.3			0.3		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	7		3.3	7	µA
	T_{min} to T_{max}				8.2			9.5	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	500		50	500	nA
	T_{min} to T_{max}				500			500	nA
Offset Current Drift		±5 V, ±15 V		0.5			0.5		nA/°C
OPEN-LOOP GAIN	V_O = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		30	65		30	65		V/mV
	T_{min} to T_{max}		20			20			V/mV
	R_{LOAD} = 150 Ω			40			40		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		50	100		50	100		V/mV
	T_{min} to T_{max}		20			20			V/mV
	R_{LOAD} = 500 Ω			85			85		V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth Product		±5 V		600			600		MHz
		±15 V		750			750		MHz
Full Power Bandwidth[1, 2]	V_O = 2 V p-p								
	R_{LOAD} = 500 Ω	±5 V		25			25		MHz
	V_O = 20 V p-p								
	R_{LOAD} = 1 kΩ	±15 V		3.6			3.6		MHz
Slew Rate[2]	R_{LOAD} = 500 Ω	±5 V		150			150		V/µs
	R_{LOAD} = 1 kΩ	±15 V		230			230		V/µs
Settling Time to 0.1%	A_V = −19								
	−2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step	±15 V		90			90		ns
Phase Margin[2]	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			60			60		Degrees
DIFFERENTIAL GAIN ERROR[3]	R_{LOAD} = 100 Ω	±15 V							
	C_{COMP} = 30 pF			0.02			0.02		%
DIFFERENTIAL PHASE ERROR[3]	R_{LOAD} = 100 Ω	±15 V							
	C_{COMP} = 30 pF			0.04			0.04		Degrees
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	100	120		100	120		dB
	V_{CM} = ±12 V	±15 V	100	120		100	120		dB
	T_{min} to T_{max}		96			96			dB
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V		98	120		98	120		dB
	T_{min} to T_{max}		94			94			dB
INPUT VOLTAGE NOISE	f = 1 kHz	±15 V		1.7	2		1.7	2	nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				−3.8			−3.8		V
		±15 V		+14.3			+14.3		V
				−13.8			−13.8		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3.0		2.5	3.0		±V
	R_{LOAD} = 50 Ω	±5 V		1.4			1.4		±V
	R_{LOAD} = 1 kΩ	±15 V	12	13.3		12	13.3		±V
	R_{LOAD} = 500 Ω	±15 V	10	12.2		10	12.2		±V
Short Circuit Current		±5 V, ±15 V		32			32		mA
INPUT CHARACTERISTICS									
Input Resistance (Differential)				13			13		kΩ
Input Capacitance (Differential)[4]				5			5		pF
Input Capacitance (Common Mode)				1.5			1.5		pF
CLOSED-LOOP OUTPUT RESISTANCE	A_V = +1, f = 1 kHz			2			2		mΩ

Model	Conditions	V_S	AD829J Min	AD829J Typ	AD829J Max	AD829 A/S Min	AD829 A/S Typ	AD829 A/S Max	Units
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		5	6.5		5	6.5	mA
	T_{min} to T_{max}				8.0			8.2/8.7	mA
		±15 V		5.3	6.8		5.3	6.8	mA
	T_{min} to T_{max}				8.3			8.5/9.0	mA
TRANSISTOR COUNT	Number of Transistors			46			46		

NOTES
[1]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.
[2]Tested at Gain = +20, C_{COMP} = 0 pF.
[3]3.58 MHz (NTSC) and 4.43 MHz (PAL & SECAM).
[4]Differential input capacitance consists of 1.5 pF package capacitance plus 3.5 pF from the input differential pair.
Specifications subject to change without notice.

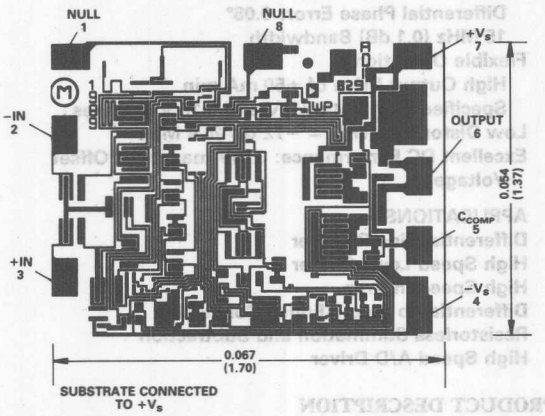
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.3 Watts
Small Outline (R) . . . . . 0.9 Watts
Cerdip (Q) . . . . . 1.3 Watts
LCC (E) . . . . . 0.8 Watts
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage[3] . . . . . ±6 Volts
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (Q, E) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD829J . . . . . 0 to +70°C
AD829A . . . . . −40°C to +85°C
AD829S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.
Thermal characteristics:
8-pin plastic package: θ_{JA} = 100°C/watt (derate at 8.7 mW/°C)
8-pin cerdip package: θ_{JA} = 110°C/watt (derate at 8.7 mW/°C)
20-pin LCC package: θ_{JA} = 150°C/watt
8-pin small outline package: θ_{JA} = 155°C/watt (derate at 6 mW/°C).
[3]If the differential voltage exceeds 6 volts, external series protection resistors should be added to limit the input current.

METALIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD829 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD829JN	0 to +70°C	8-Pin Plastic Mini-DIP	N-8
AD829JR	0 to +70°C	8-Pin Plastic SOIC	R-8
AD829JR-REEL	0 to +70°C	Tape & Reel	
AD829AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD829SQ	−55°C to +125°C	8-Pin Cerdip	Q-8
AD829SQ/883B	−55°C to +125°C	8-Pin Cerdip	Q-8
5962-9312901MPA	−55°C to +125°C	8-Pin Cerdip	Q-8
AD829SE/883B	−55°C to +125°C	20-Pin LCC	E-20A
5962-9312901M2A	−55°C to +125°C	20-Pin LCC	E-20A
AD829JChips	0 to +70°C	Die	
AD829SChips	−55°C to +125°C	Die	

*E = Leadless Chip Carrier (Ceramic); N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC).
For outline information see Package Information section.

AD830

FEATURES

Differential Amplification
- Wide Common-Mode Voltage Range: +12.8 V, −12 V
- Differential Voltage Range: ±2 V
- High CMRR: 60 dB @ 4 MHz
- Built-in Differential Clipping Level: ±2.3 V

Fast Dynamic Performance
- 85 MHz Unity Gain Bandwidth
- 35 ns Settling Time to 0.1%
- 360 V/μs Slew Rate

Symmetrical Dynamic Response

Excellent Video Specifications
- Differential Gain Error: 0.06%
- Differential Phase Error: 0.08°
- 15 MHz (0.1 dB) Bandwidth

Flexible Operation
- High Output Drive of ±50 mA min
- Specified with Both ±5 V and ±15 V Supplies

Low Distortion: THD = −72 dB @ 4 MHz

Excellent DC Performance: 3 mV max Input Offset Voltage

APPLICATIONS

Differential Line Receiver

High Speed Level Shifter

High Speed In-Amp

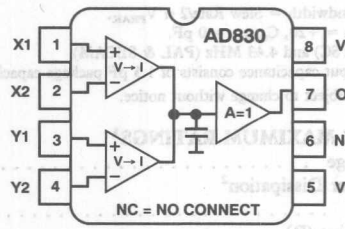
Differential to Single Ended Conversion

Resistorless Summation and Subtraction

High Speed A/D Driver

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages

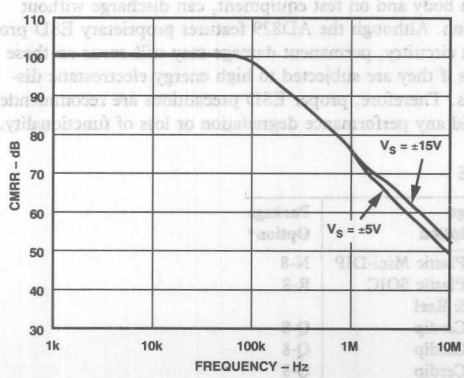


PRODUCT DESCRIPTION

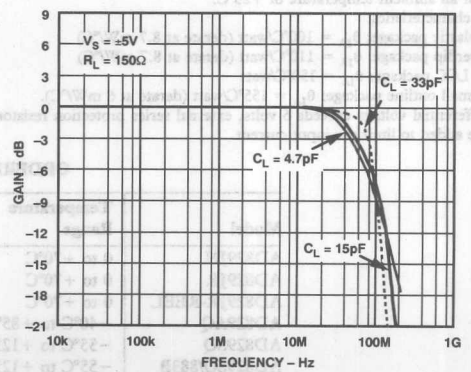
The AD830 is a wideband, differencing amplifier designed for use at video frequencies but also useful in many other applications. It accurately amplifies a fully differential signal at the input and produces an output voltage referred to a user-chosen level. The undesired common-mode signal is rejected, even at high frequencies. High impedance inputs ease interfacing to finite source impedances and thus preserve the excellent common-mode rejection. In many respects, it offers significant improvements over discrete difference amplifier approaches, in particular in high frequency common-mode rejection.

The wide common-mode and differential-voltage range of the AD830 make it particularly useful and flexible in level shifting applications, but at lower power dissipation than discrete solutions. Low distortion is preserved over the many possible differential and common-mode voltages at the input and output.

Good gain flatness and excellent differential gain of 0.06% and phase of 0.08° make the AD830 suitable for many video system applications. Furthermore, the AD830 is suited for general purpose signal processing from dc to 10 MHz.



Common-Mode Rejection Ratio vs. Frequency



Closed-Loop Gain vs. Frequency, Gain = +1

SPECIFICATIONS (V_S = ±15 V, R_{LOAD} = 150 Ω, C_{LOAD} = 5 pF, T_A = +25°C unless otherwise noted) AD830

Parameter	Conditions	AD830J/A Min	AD830J/A Typ	AD830J/A Max	AD830S[1] Min	AD830S[1] Typ	AD830S[1] Max	Units
DYNAMIC CHARACTERISTICS								
3 dB Small Signal Bandwidth	Gain = 1, V_{OUT} = 100 mV rms	75	85		75	85		MHz
0.1 dB Gain Flatness Frequency	Gain = 1, V_{OUT} = 100 mV rms	11	15		11	15		MHz
Differential Gain Error	0 to +0.7 V, Frequency = 4.5 MHz		0.06	0.09		0.06	0.09	%
Differential Phase Error	0 to +0.7 V, Frequency = 4.5 MHz		0.08	0.12		0.08	0.12	Degrees
Slew Rate	2 V Step, R_L = 500 Ω		360			360		V/μs
	4 V Step, R_L = 500 Ω		350			350		V/μs
3 dB Large Signal Bandwidth	Gain = 1, V_{OUT} = 1 V rms	38	45		38	45		MHz
Settling Time, Gain = 1	V_{OUT} = 2 V Step, to 0.1%		25			25		ns
	V_{OUT} = 4 V Step, to 0.1%		35			35		ns
Harmonic Distortion	2 V p-p, Frequency = 1 MHz		−82			−82		dBc
	2 V p-p, Frequency = 4 MHz		−72			−72		dBc
Input Voltage Noise	Frequency = 10 kHz		27			27		nV/√Hz
Input Current Noise			1.4			1.4		pA/√Hz
DC PERFORMANCE								
Offset Voltage	Gain = 1		±1.5	±3		±1.5	±3	mV
	Gain = 1, T_{MIN}–T_{MAX}			±5			±7	mV
Open Loop Gain	DC	64	69		64	69		dB
Gain Error	R_L = 1 kΩ, G = ±1		±0.1	±0.6		±0.1	±0.6	%
Peak Nonlinearity, R_L = 1 kΩ,	−1 V ≤ X ≤ +1 V		0.01	0.03		0.01	0.03	% FS
Gain = 1	−1.5 V ≤ X ≤ +1.5 V		0.035	0.07		0.035	0.07	% FS
	−2 V ≤ X ≤ +2 V		0.15	0.4		0.15	0.4	% FS
Input Bias Current	V_{IN} = 0 V, +25°C to T_{MAX}		5	10		5	10	μA
	V_{IN} = 0 V, T_{MIN}		7	13		8	17	μA
Input Offset Current	V_{IN} = 0 V, T_{MIN}–T_{MAX}		0.1	1		0.1	1	μA
INPUT CHARACTERISTICS								
Differential Voltage Range	V_{CM} = 0		±2.0			±2.0		V
Differential Clipping Level[2]	Pins 1 and 2 Inputs Only	±2.1	±2.3		±2.1	±2.3		V
Common-Mode Voltage Range	V_{DM} = ±1 V	−12.0		+12.8	−12.0		+12.8	V
CMRR	DC, Pins 1, 2, ±10 V	90	100		90	100		dB
	DC, Pins 1, 2, ±10 V, T_{MIN}–T_{MAX}	88			86			dB
	Frequency = 4 MHz	55	60		55	60		dB
Input Resistance			370			370		kΩ
Input Capacitance			2			2		pF
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L ≥ 1 kΩ	±12	+13.8, −13.8		±12	+13.8, −13.8		V
	R_L ≥ 1 kΩ, ±16.5 V_S	±13	+15.3, −14.7		±13	+15.3, −14.7		V
Short Circuit Current	Short to Ground		±80			±80		mA
Output Current	R_L = 150 Ω	±50			±50			mA
POWER SUPPLIES								
Operating Range		±4		±16.5	±4		±16.5	V
Quiescent Current	T_{MIN}–T_{MAX}		14.5	17		14.5	17	mA
+ PSRR (to V_P)	DC, G = 1		86			86		dB
− PSRR (to V_N)	DC, G = 1		68			68		dB
PSRR	DC, G = 1, ±5 to ±15 V_S	66	71		66	71		dB
PSRR	DC, G = 1, ±5 to ±15 V_S, T_{MIN}–T_{MAX}	62	68		60	68		dB

NOTES
[1]See Standard Military Drawing 5962-9313001MPA for specifications.
[2]Clipping level function on X channel only.
Specifications subject to change without notice.

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AD830—SPECIFICATIONS (V_S = ±5 V, R_{LOAD} = 150 Ω, C_{LOAD} = 5 pF, T_A = +25°C unless otherwise noted)

Parameter	Conditions	AD830J/A Min	AD830J/A Typ	AD830J/A Max	AD830S[1] Min	AD830S[1] Typ	AD830S[1] Max	Units
DYNAMIC CHARACTERISTICS								
3 dB Small Signal Bandwidth	Gain = 1, V_{OUT} = 100 mV rms	35	40		35	40		MHz
0.1 dB Gain Flatness Frequency	Gain = 1, V_{OUT} = 100 mV rms	5	6.5		5	6.5		MHz
Differential Gain Error	0 to +0.7 V, Frequency = 4.5 MHz, G=+2		0.14	0.18		0.14	0.18	%
Differential Phase Error	0 to +0.7 V, Frequency = 4.5 MHz, G=+2		0.32	0.4		0.32	0.4	Degrees
Slew Rate, Gain = 1	2 V Step, R_L = 500 Ω		210			210		V/µs
	4 V Step, R_L = 500 Ω		240			240		V/µs
3 dB Large Signal Bandwidth	Gain = 1, V_{OUT} = 1 V rms	30	36		30	36		MHz
Settling Time	V_{OUT} = 2 V Step, to 0.1%		35			35		ns
	V_{OUT} = 4 V Step, to 0.1%		48			48		ns
Harmonic Distortion	2 V p-p, Frequency = 1 MHz		−69			−69		dBc
	2 V p-p, Frequency = 4 MHz		−56			−56		dBc
Input Voltage Noise	Frequency = 10 kHz		27			27		nV/√Hz
Input Current Noise			1.4			1.4		pA/√Hz
DC PERFORMANCE								
Offset Voltage	Gain = 1		±1.5	±3		±1.5	±3	mV
	Gain = 1, T_{MIN}–T_{MAX}			±4			±5	mV
Open Loop Gain	DC	60	65		60	65		dB
Unity Gain Accuracy	R_L = 1 kΩ		±0.1	±0.6		±0.1	±0.6	%
Peak Nonlinearity, R_L = 1 kΩ	−1 V ≤ X ≤ +1 V		0.01	0.03		0.01	0.03	% FS
	−1.5 V ≤ X ≤ +1.5 V		0.045	0.07		0.045	0.07	% FS
	−2 V ≤ X ≤ +2 V		0.23	0.4		0.23	0.4	% FS
Input Bias Current	V_{IN} = 0 V, +25°C to T_{MAX}		5	10		5	10	µA
	V_{IN} = 0 V, T_{MIN}		7	13		8	17	µA
Input Offset Current	V_{IN} = 0 V, T_{MIN} to T_{MAX}		0.1	1		0.1	1	µA
INPUT CHARACTERISTICS								
Differential Voltage Range	V_{CM} = 0		±2.0			±2.0		V
Differential Clipping Level[2]	Pins 1 and 2 Inputs Only	±2.0	±2.2		±2.0	±2.2		V
Common-Mode Voltage Range	V_{DM} = ±1 V	−2.0		+2.9	−2.0		+2.9	V
CMRR	DC, Pins 1, 2, +4 V to −2 V	90	100		90	100		dB
	DC, Pins 1, 2, +4 V to −2 V, T_{MIN}–T_{MAX}	88			86			dB
	Frequency = 4 MHz	55	60		55	60		dB
Input Resistance			370			370		kΩ
Input Capacitance			2			2		pF
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L ≥ 150 Ω	±3.2	±3.5		±3.2	±3.5		V
	R_L ≥ 150 Ω, ±4 V_S	±2.2	+2.7, −2.4		±2.2	+2.7, −2.4		V
Short Circuit Current	Short to Ground		−55, +70			−55, +70		mA
Output Current		±40			±40			mA
POWER SUPPLIES								
Operating Range		±4		±16.5	±4		±16.5	V
Quiescent Current	T_{MIN}–T_{MAX}		13.5	16		13.5	16	mA
+ PSRR (to V_P)	DC, G = 1, Offset		86			86		dB
− PSRR (to V_N)	DC, G = 1, Offset		68			68		dB
PSRR (Dual Supply)	DC, G = 1, ±5 to ±15 V_S	66	71		66	71		dB
PSRR (Dual Supply)	DC, G = 1, ±5 to ±15 V_S, T_{MIN}–T_{MAX}	62	68		60	68		dB

NOTES
[1]See Standard Military Drawing 5962-9313001MPA for specifications.
[2]Clipping level function on X channel only.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . Observe Derating Curves
Output Short Circuit Duration . . . . . Observe Derating Curves
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . $\pm V_S$
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N) . . . . . −65°C to +125°C
Storage Temperature Range (R) . . . . . −65°C to +125°C
Operating Temperature Range
AD830J . . . . . 0°C to +70°C
AD830A . . . . . −40°C to +85°C
AD830S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 90°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD830 is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 145°C. For the cerdip, the maximum junction temperature is 175°C. If these maximums are exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the AD830 in the "overheated" condition for an extended period can result in permanent damage to the device. To ensure proper operation, it is important to observe the recommended derating curves.

While the AD830 output is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. If the output is shorted to a supply rail for an extended period, then the amplifier may be permanently destroyed.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD830 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

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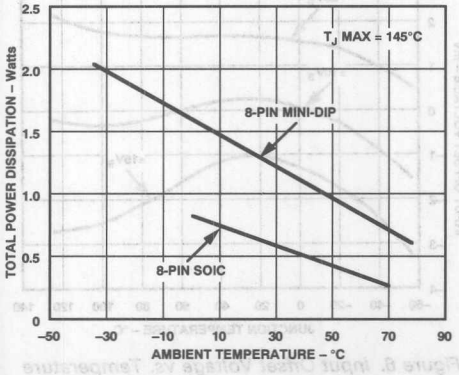
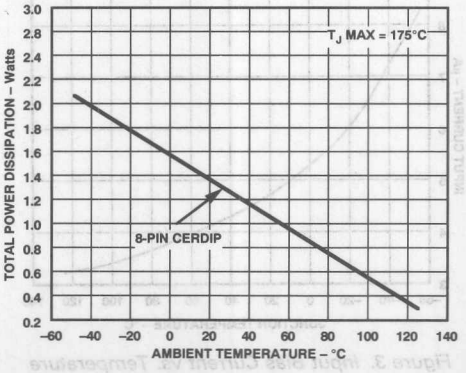
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD830AN	−40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD830JR	0°C to +70°C	8-Pin SOIC	R-8
5962-9313001MPA[2]	−55°C to +125°C	8-Pin Cerdip	Q-8

NOTES
[1]For outline information see Package Information section.
[2]See standard military drawing 5962-9313001MPA.



Maximum Power Dissipation vs. Temperature, Mini-DIP and SOIC Packages



Maximum Power Dissipation vs. Temperature, Cerdip Package

AD830—Typical Characteristics

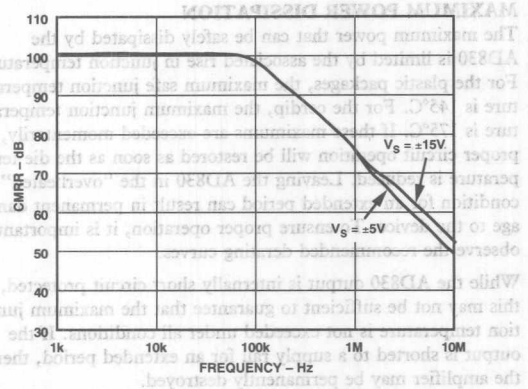


Figure 1. Common-Mode Rejection Ratio vs. Frequency

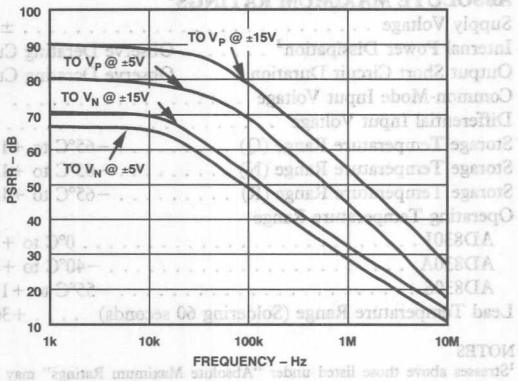


Figure 4. Power Supply Rejection Ratio vs. Frequency

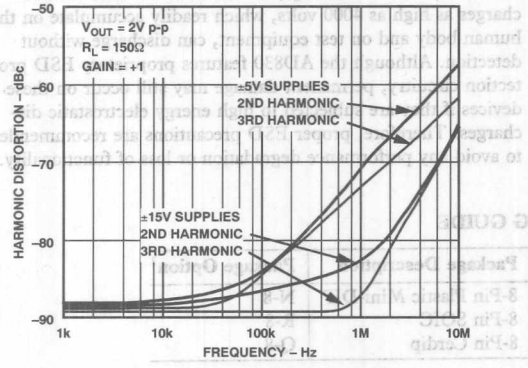


Figure 2. Harmonic Distortion vs. Frequency

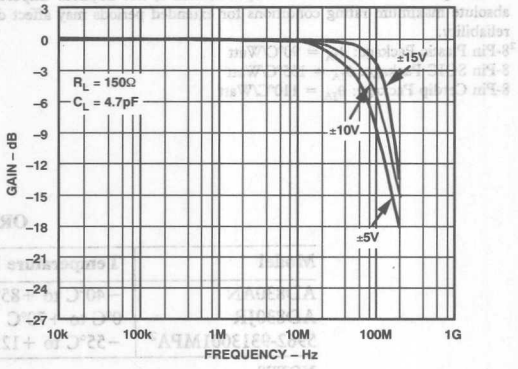


Figure 5. Closed-Loop Gain vs. Frequency G = +1

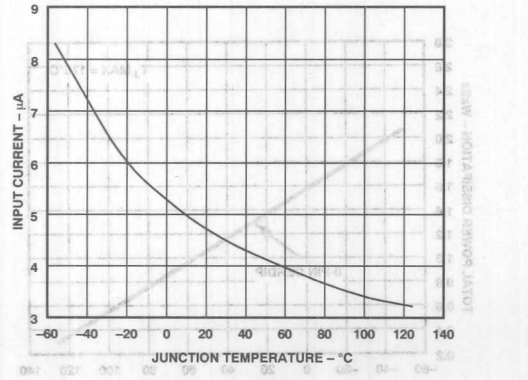


Figure 3. Input Bias Current vs. Temperature

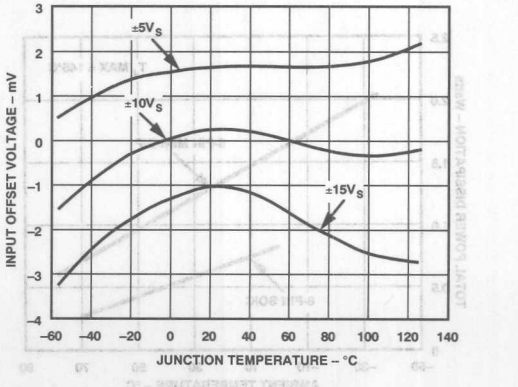


Figure 6. Input Offset Voltage vs. Temperature

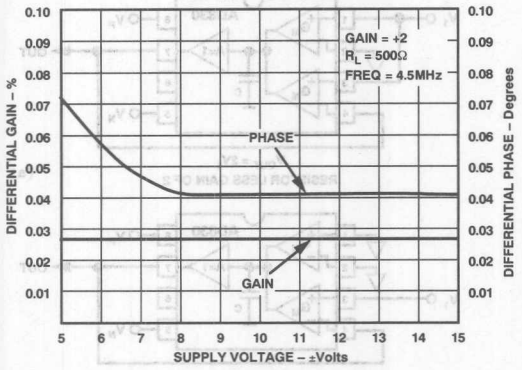


Figure 7. Differential Gain and Phase vs. Supply Voltage, R_L = 500 Ω

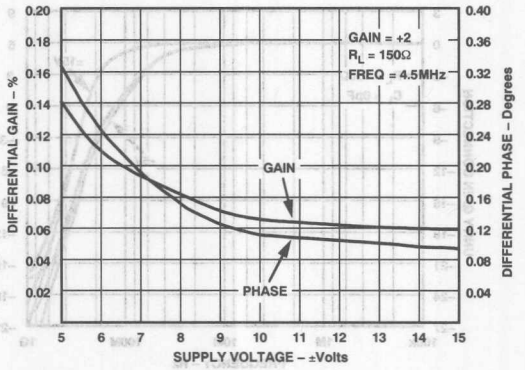


Figure 10. Differential Gain and Phase vs. Supply Voltage, R_L = 150 Ω

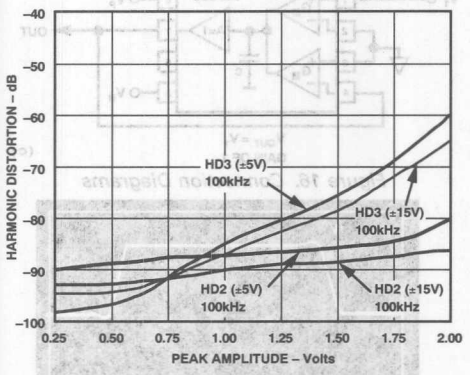


Figure 8. Harmonic Distortion vs. Peak Amplitude, Frequency = 100 kHz

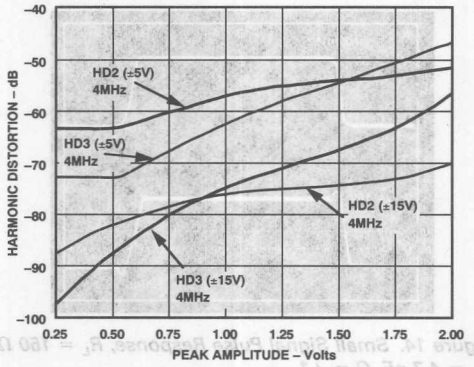


Figure 11. Harmonic Distortion vs. Peak Amplitude, Frequency = 4 MHz

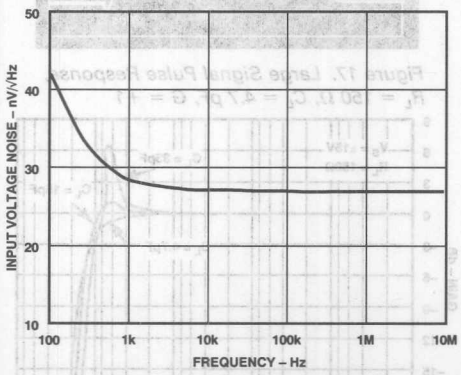


Figure 9. Noise Spectral Density

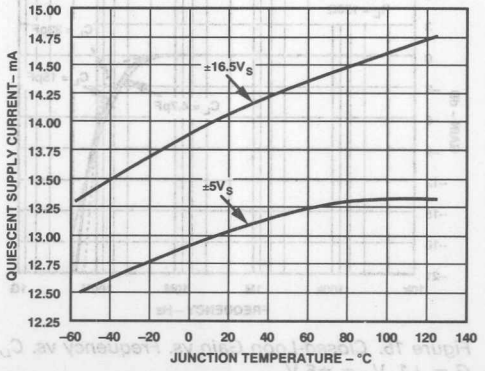


Figure 12. Supply Current vs. Junction Temperature

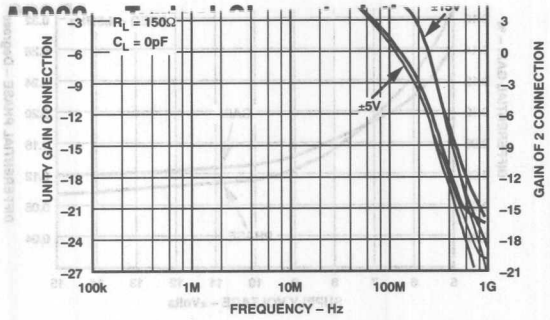


Figure 13. Closed-Loop Gain vs. Frequency for the Three Common Connections of Figure 16

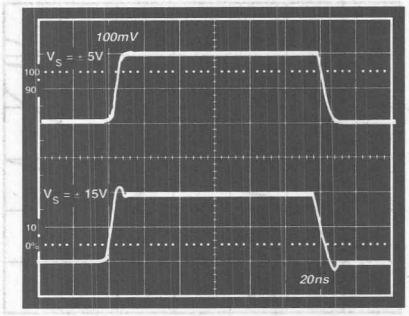


Figure 14. Small Signal Pulse Response, R_L = 150 Ω, C_L = 4.7 pF, G = +1

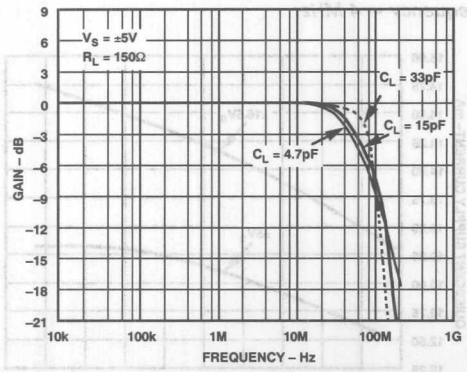


Figure 15. Closed-Loop Gain vs. Frequency vs. C_L, G = +1. V_S = ±5 V

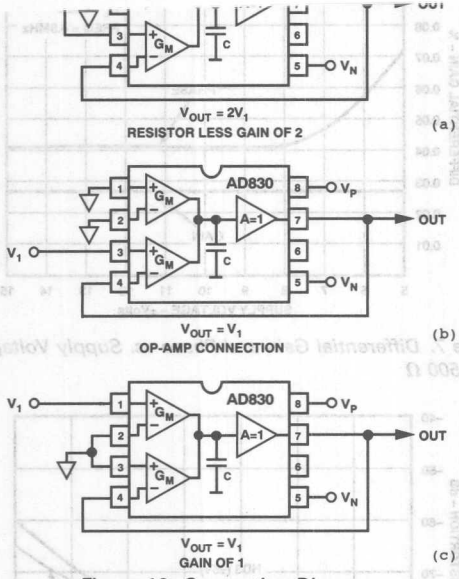


Figure 16. Connection Diagrams

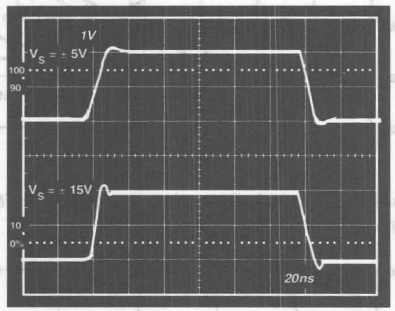


Figure 17. Large Signal Pulse Response, R_L = 150 Ω, C_L = 4.7 pF, G = +1

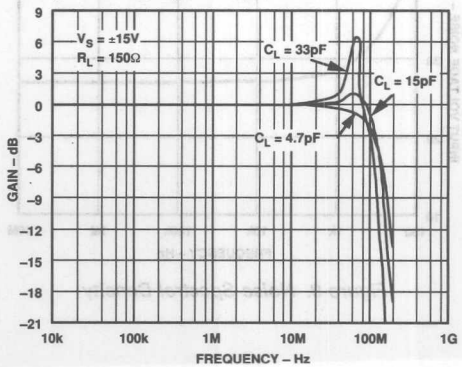


Figure 18. Closed-Loop Gain vs. Frequency, vs. C_L, G = +1. V_S = ±15 V

In the past, when differential amplification was needed to reject common-mode signals superimposed with a desired signal; most often the solution used was the classic op amp based difference amplifier shown in Figure 19. The basic function $V_O = V_1 - V_2$ is simply achieved, but the overall performance is poor and the circuit possesses many serious problems that make it difficult to realize a robust design with moderate to high levels of performance.

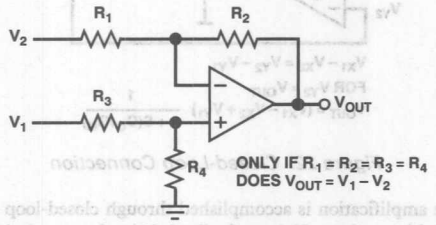


Figure 19. Op Amp Based Difference Amplifier

PROBLEMS WITH THE OP AMP BASED APPROACH

- Low Common-Mode Rejection Ratio (CMRR)
- Low Impedance Inputs
- CMRR Highly Sensitive to the Value of Source R
- Different Input Impedance for the + and − Input
- Poor High Frequency CMRR
- Requires Very Highly Matched Resistors R_1–R_4 to Achieve High CMRR
- Halves the Bandwidth of the Op Amp
- High Power Dissipation in the Resistors for Large Common-Mode Voltage

listed problems with the discrete difference amplifier approach. Its topology, discussed in detail in a later section, by design acts as a difference amplifier. The circuit of Figure 20 shows how simply the AD830 is configured to produce the difference of two signals V_1 and V_2, in which the applied differential signal is exactly reproduced at the output relative to a separate output common. Any common-mode voltage present at the input is removed by the AD830.

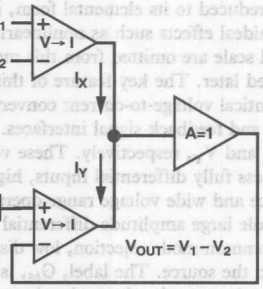
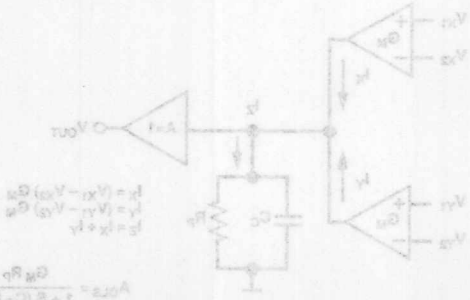


Figure 20. AD830 as a Difference Amplifier

ADVANTAGEOUS PROPERTIES OF THE AD830

- High Common-Mode Rejection Ratio (CMRR)
- High Impedance Inputs
- Symmetrical Dynamic Response for +1 and −1 Gain
- Low Sensitivity to the Value of Source R
- Equal Input Impedance for the + and − Input
- Excellent High Frequency CMRR
- No Halving of the Bandwidth
- Constant Power Distortion vs. Common-Mode Voltage
- Highly Matched Resistors Not Needed



UNDERSTANDING THE AD830 TOPOLOGY

The AD830 represents Analog Devices' first amplifier product to embody a powerful alternative amplifier topology. Referred to as active feedback, the topology used in the AD830 provides inherent advantages in the handling of differential signals, differing system commons, level shifting and low distortion, high frequency amplification. In addition, it makes possible the implementation of many functions not realizable with single op amp circuits or is superior to op amp based equivalent circuits. With this in mind, it is important to understand the internal structure of the AD830.

The topology, reduced to its elemental form, is shown below in Figure 21. Nonideal effects such as nonlinearity, bias currents and limited full scale are omitted from this model for simplicity, but are discussed later. The key feature of this topology is the use of two, identical voltage-to-current converters, G_M, that make up input and feedback signal interfaces. They are labeled with inputs V_X and V_Y, respectively. These voltage to current converters possess fully differential inputs, high linearity, high input impedance and wide voltage range operation. This enables the part to handle large amplitude differential signals; they also provide high common-mode rejection, low distortion and negligible loading on the source. The label, G_M, is meant to convey that the transconductance is a large signal quantity, unlike in the front-end of most op amps. The two G_M stage current outputs I_X and I_Y, sum together at a high impedance node which is characterized by an equivalent resistance and capacitance connected to an "ac common." A unity voltage gain stage follows the high impedance node to provide buffering from loads. Relative to either input, the open loop gain, A_{OL}, is set by the transconductance, G_M, working into the resistance, R_P; $A_{OL} = G_M \times R_P$. The unity gain frequency $\omega_{0\ dB}$ for the open loop gain is established by the transconductance, G_M, working into the capacitance, C_C; $\omega_{0\ dB} = G_M/C_C$. The open loop description of the AD830 is shown below for completeness.

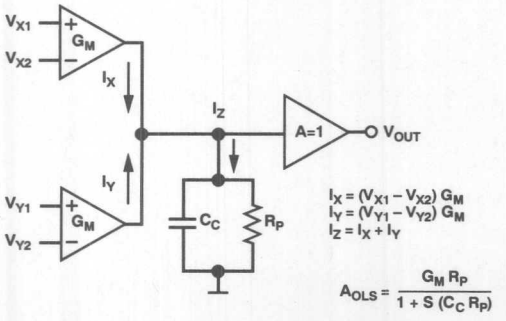


Figure 21. Topology Diagram

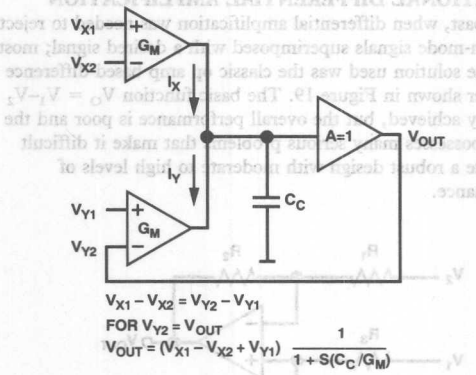


Figure 22. Closed-Loop Connection

Precise amplification is accomplished through closed-loop operation of this topology. Voltage feedback is implemented via the Y G_M stage in which where the output is connected to the $-Y$ input for negative feedback as shown in Figure 22. An input signal is applied across the X G_M stage, either fully differentially or single-ended referred to common. It produces a current signal which is summed at the high impedance node with the output current from the Y G_M stage. Negative feedback nulls this sum to a small error current necessary to develop the output voltage at the high impedance node. The error current is usually negligible, so the null condition essentially forces the Y G_M output stage current to exactly equal the X G_M output current. Since the two transconductances are identical, the differential voltage across the Y inputs equals the negative of the differential voltage across the X input; $V_Y = -V_X$ or more precisely $V_{Y2}–V_{Y1} = V_{X1}–V_{X2}$. This simple relation provides the basis to easily analyze any function possible to synthesize with the AD830, including any feedback situation.

The bandwidth of the circuit is defined by the G_M and the capacitor C_C. The highly linear G_M stages give the amplifier a single pole response, excluding the output amplifier and loading effects. *It is important to note that the bandwidth and general dynamic behavior is symmetrical (identical) for the noninverting and the inverting connections of the AD830.* In addition, the input impedance and CMRR are the same for either connections. This is very advantageous and unlike in a voltage or current feedback amplifier, where there is a distinct difference in performance between the inverting and noninverting gain. The practical importance of this cannot be overemphasized and is a key feature offered by the AD830 amplifier topology.

INTERFACING THE INPUT

Common-Mode Voltage Range

The common-mode range of the AD830 is defined by the amplitude of the differential input signal and the supply voltage. The general definition of common-mode voltage, V_{CM}, is usually applied to a symmetrical differential signal centered about a particular voltage as illustrated by the diagram in Figure 23. This is the meaning implied here for common-mode voltage. The internal circuitry establishes the maximum allowable voltage on the input or feedback pins for a given supply voltage. This constraint and the differential input voltage sets the common-mode voltage limit. Figure 24 shows a curve of the common-mode voltage range vs. differential voltage for three supply voltage settings.

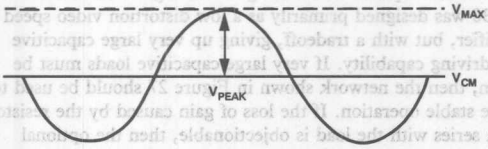


Figure 23. Common-Mode Definition

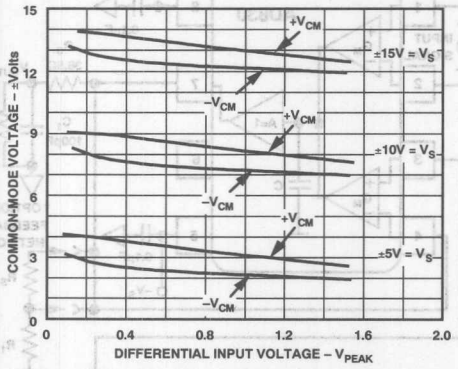
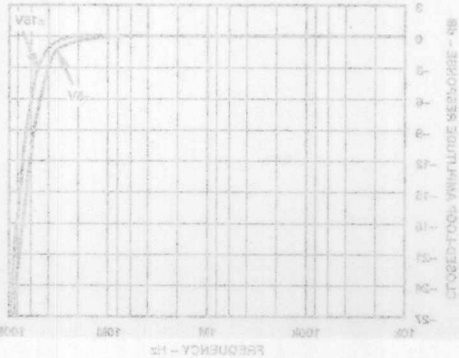


Figure 24. Input Common-Mode Voltage Range vs. Differential Input Voltage



Differential Voltage Range

The maximum applied differential voltage is limited by the clipping range of the input stages. This is nominally set at 2.4 volts magnitude and depicted in the crossplot (X-Y) photo of Figure 25. The useful linear range of the input stages is set at 2 volts, but is actually a function of the distortion required for a particular application. The distortion increases for larger differential input voltages. A plot of relative distortion versus input differential voltage is shown in Figures 8 and 11 in the Typical Characteristics section. The distortion characteristics could impose a secondary limit to the differential input voltage for high accuracy applications.

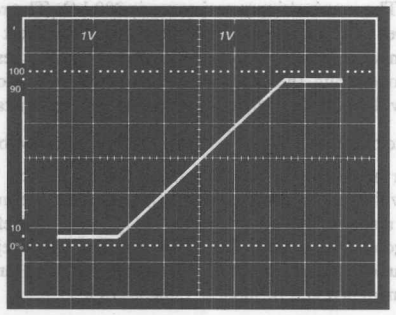


Figure 25. Clipping Behavior

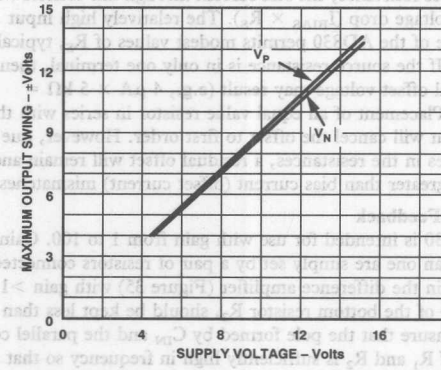


Figure 26. Maximum Output Swing vs. Supply

Swapping between inverting and noninverting gain is possible simply by reversing the input connections. The response of the amplifier is identical in either connection, except for the sign change. The bandwidth, high impedance, transient behavior, etc., of the AD830, is symmetrical for both polarities of gain. This is very advantageous and unlike an op amp.

Input Impedance

The relatively high input impedance of the AD830, for a differential receiver amplifier, permits connections to modest impedance sources without much loading or loss of common-mode rejection. The nominal input resistance is 300 kΩ. The real limit to the upper value of the source resistance is in its effect on common-mode rejection and bandwidth. If the source resistance is in only one input, then the low frequency common-mode rejection will be lowered to $\approx R_{IN}/R_S$. The source resistance/input capacitance pole ($f = \frac{1}{2\pi} \times R_S \times C_{IN}$) limits the bandwidth. Furthermore, the high frequency common-mode rejection will be additionally lowered by the difference in the frequency response caused by the $R_S \times C_{IN}$ pole. Therefore, to maintain good low and high frequency common-mode rejection, it is recommended that the source resistances of the + and − inputs be matched and of modest value (≤10 kΩ).

Handling Bias Currents

The bias currents are typically 4 μA flowing into each pin of the G_M stages of the AD830. Since all applications possess some finite source resistance, the bias current through this resistor will create a voltage drop ($I_{BIAS} \times R_S$). The relatively high input impedance of the AD830 permits modest values of R_S, typically ≤10 kΩ. If the source resistance is in only one terminal, then an objectional offset voltage may result (e.g., 4 μA × 5 kΩ = 20 mV). Placement of an equal value resistor in series with the other input will cancel the offset to first order. However, due to mismatches in the resistances, a residual offset will remain and likely be greater than bias current (offset current) mismatches.

Applying Feedback

The AD830 is intended for use with gain from 1 to 100. Gains greater than one are simply set by a pair of resistors connected as shown in the difference amplifier (Figure 35) with gain >1. The value of the bottom resistor R_2, should be kept less than 1 kΩ to insure that the pole formed by C_{IN} and the parallel connection of R_1 and R_2 is sufficiently high in frequency so that it does not introduce excessive phase shift around the loop and destabilizes the amplifier. A compensating resistor, equal to the parallel combination of R_1 and R_2, should be placed in series with the other Y G_M stage input to preserve the high frequency common-mode rejection and to lower the offset voltage induced by the input bias current.

Output Common Mode

The output swing of the AD830 is defined by the differential input voltage, the gain and the output common. Depending on the anticipated signal span, the output common (or ground) may be set anywhere between the allowable peak output voltage in a manner similar to that described for input voltage common mode. A plot of the peak output voltage versus supply is shown in Figure 26. A prediction of the common-mode range versus

Output Current

The absolute peak output current is set by the short circuit current limiting, typically greater that 60 mA. The maximum drive capability is rated at 50 mA, but without a guarantee of distortion performance. Best distortion performance is obtained by keeping the output current ≤20 mA. Attempting to drive large voltages into low valued resistances (e.g., 10 V into 150 Ω) will cause an apparent lowering of the limit for output signal swing, but is just the current limiting behavior.

Driving Cap Loads

The AD830 is capable of driving modest sized capacitive loads while maintaining its rated performance. Several curves of bandwidth versus capacitive load are given in Figures 15 and 18. The AD830 was designed primarily as a low distortion video speed amplifier, but with a tradeoff, giving up very large capacitive load driving capability. If very large capacitive loads must be driven, then the network shown in Figure 27 should be used to insure stable operation. If the loss of gain caused by the resistor R_S in series with the load is objectionable, then the optional feedback network shown may be added to restore the lost gain.

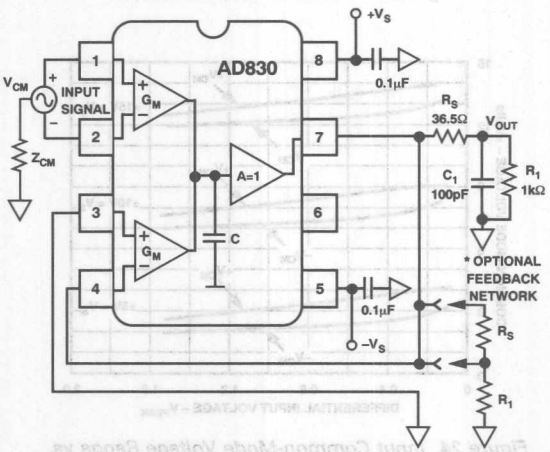


Figure 27. Circuit for Driving Large Capacitive Loads

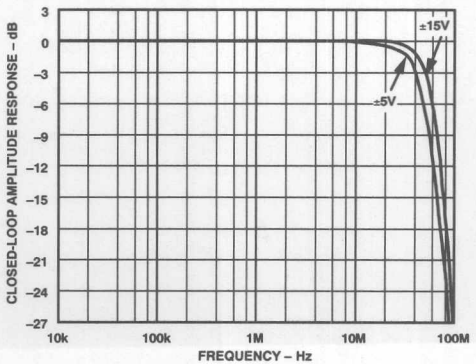


Figure 28. Closed-Loop Response vs. Frequency with 100 pF Load and Series Resistor Compensation

SUPPLIES, BYPASSING AND GROUNDING (Figure 29)

The AD830 is capable of operating over a wide range of supply voltages, both single and dual supplies. The coupling may be dc or ac provided the input and output voltages stay within the specified common-mode voltage limits. For dual supplies, the device works from ±4 V to ±16.5 V. Single supply operation is possible over +8 V to +33 V. It is also possible to operate the part with split supply voltages (e.g., +24 V, −5 V) for special applications such as level shifting. The primary constraint is that the total potential between the two supplies does not exceed 33 V.

Inclusion of power supply bypassing capacitors is necessary to achieve stable behavior and the specified performance. It is especially important when driving low resistance loads. At a minimum, connect a 0.1 μF ceramic capacitor at the supply lead of the AD830 package. In addition, for the best by passing, we recommend connecting a 0.01 μF ceramic capacitor and 4.7 μF tantalum capacitor to the supply lead going to the AD830.

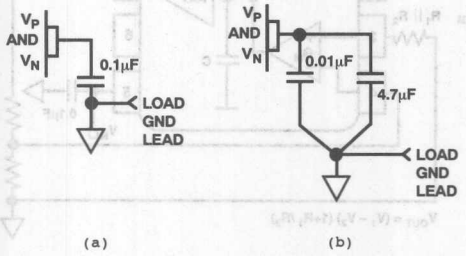


Figure 29. Supply Decoupling Options

The AD830 is designed by its functionality to be capable of rejecting noise and dissimilar potentials in the ground lines. Therefore, proper care is necessary to realize the benefits of the differential amplification of the part. Separation of the input and output grounds is crucial in rejection of the common mode noise at the inputs and eliminating any ground drops on the input signal line. For example, connecting the ground of a coaxial cable to the AD830 output common (board ground) could degrade the CMR and also introduce power-down loading on cable grounds. However, it is also necessary as in any electronic system, to provide a return path for bias currents back to their original power supply. This is accomplished by providing a connection between the differing grounds through a modest impedance labeled Z_{CM} (e.g., 100 Ω).

Single Supply Operation

The AD830 is capable of operating in single power supply applications down to a voltage of +8 V, with the generalized connection shown in Figure 30. There is a constraint on the common-mode voltage at the input and output which establishes the range for these voltages. Direct coupling may be used for input and output voltages which lie in these ranges. Any gain network applied needs to be referred to the output common connection or have an appropriate offset voltage. In situations where the signal lies at a common voltage outside the common mode range of the AD830 direct coupling will not work, so ac coupling should be used. A tested application included later in this data sheet (Figure 42), shows how to easily accomplish coupling to the AD830. For single supply operation where direct coupling is desired the input and output common-mode curves (Figures 31 and 32) should be used.

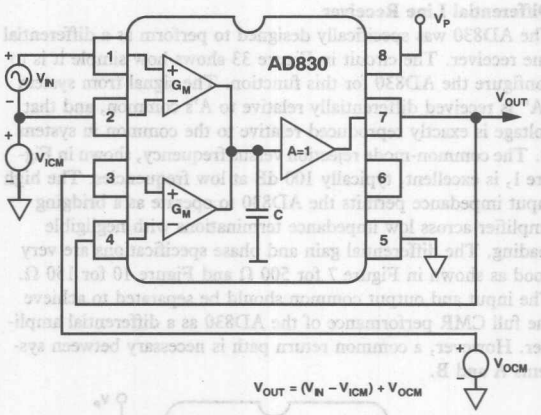


Figure 30. General Single Supply Connection

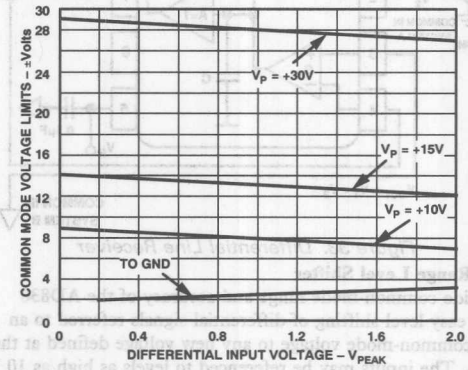


Figure 31. Input Common-Mode Range for Single Supply

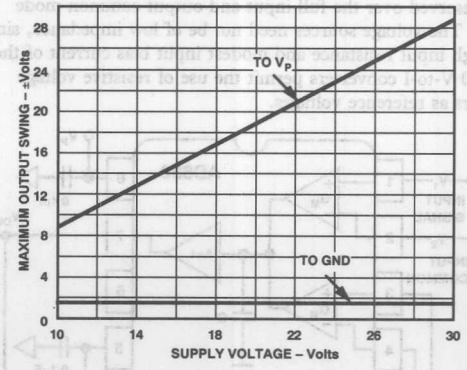


Figure 32. Output Swing Limit for Single Supply

Differential Line Receiver

The AD830 was specifically designed to perform as a differential line receiver. The circuit in Figure 33 shows how simple it is to configure the AD830 for this function. The signal from system "A" is received differentially relative to A's common, and that voltage is exactly reproduced relative to the common in system B. The common-mode rejection versus frequency, shown in Figure 1, is excellent, typically 100 dB at low frequencies. The high input impedance permits the AD830 to operate as a bridging amplifier across low impedance terminations with negligible loading. The differential gain and phase specifications are very good as shown in Figure 7 for 500 Ω and Figure 10 for 150 Ω. The input and output common should be separated to achieve the full CMR performance of the AD830 as a differential amplifier. However, a common return path is necessary between systems A and B.

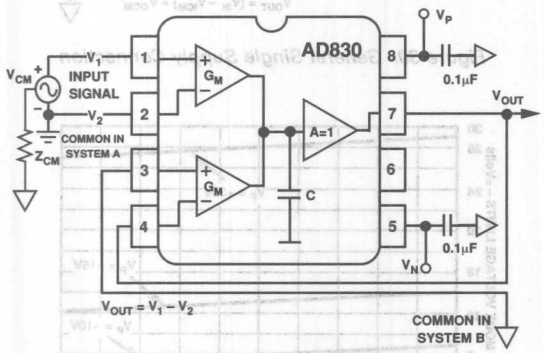


Figure 33. Differential Line Receiver

Wide Range Level Shifter

The wide common-mode range and accuracy of the AD830 allows easy level shifting of differential signals referred to an input common-mode voltage to any new voltage defined at the output. The inputs may be referenced to levels as high as 10 V at the inputs with a ±2 V swing about 10 V. In the circuit of Figure 34, the output voltage, V_{OUT}, is defined by the simple equation shown below. The excellent linearity and low distortion are preserved over the full input and output common-mode range. The voltage sources need not be of low impedance, since the high input resistance and modest input bias current of the AD830 V-to-I converters permit the use of resistive voltage dividers as reference voltages.

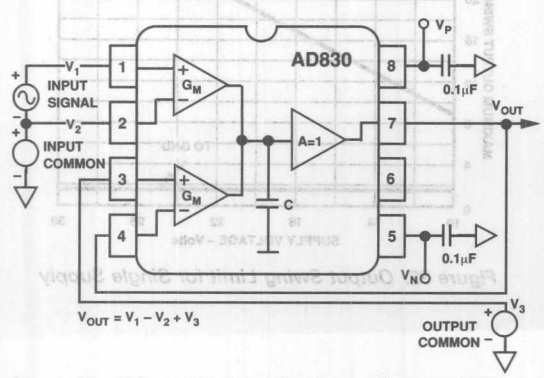


Figure 34. Differential Amplification with Level Shifting

Difference Amplifier with Gain > 1

The AD830 can provide instrumentation amplifier style differential amplification at gains greater than 1. The input signal is connected differentially and the gain is set via feedback resistors as shown in Figure 35. The gain, $G = (R_2 + R_1)/R_2$. The AD830 can provide either inverting or noninverting differential amplification. The polarity of the gain is established by the polarity of the connection at the input. Feedback resistors R_2 should generally be $R_2 \leq 1\ k\Omega$ to maintain closed-loop stability and also keep bias current induced offsets low. Highest CMRR and lowest dc offsets are preserved by including a compensating resistor in series with Pin 3. The gain may be as high as 100.

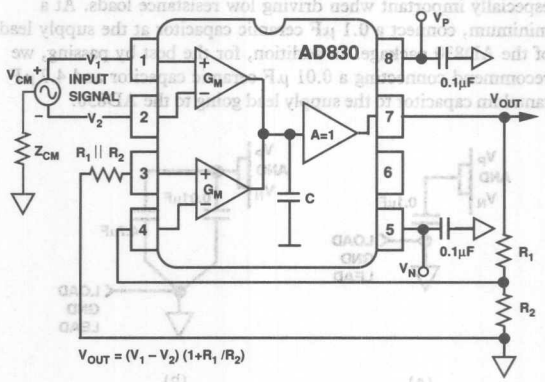


Figure 35. Gain of G Differential Amplifier, G > 1

Offsetting the Output with Gain

Some applications, such as A/D drivers, require that the signal be amplified and also offset, typically to accommodate the input range of the device. The AD830 can offset the output signal very simply through Pin 3 even with gain > 1. The voltage applied to Pin 3 must be attenuated by an appropriate factor so that $V_3 \times G$ = desired offset. In Figure 36, a resistive divider from a voltage reference is used to produce the attenuated offset voltage.

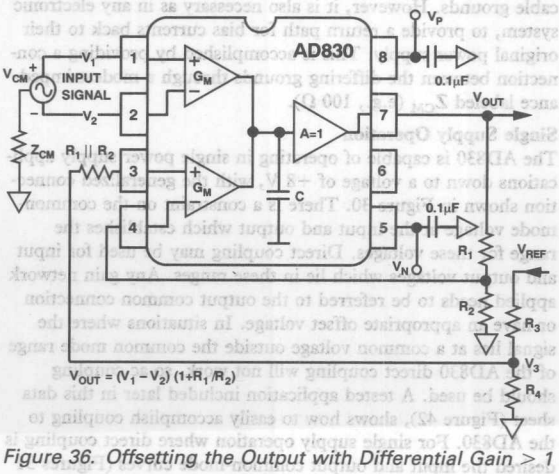


Figure 36. Offsetting the Output with Differential Gain > 1

Loop Through or Line Bridging Amplifier (Figure 37)
The AD830 is ideally suited for use as a video line bridging amplifier. The video signal is tapped from the conductor of the cable relative to its shield. The high input impedance of the AD830 provides negligible loading on the cable. More significantly, the benign loading is maintained while the AD830 is powered-down. Coupled with its good video load driving performance, the AD830 is well suited to video cable monitoring applications.

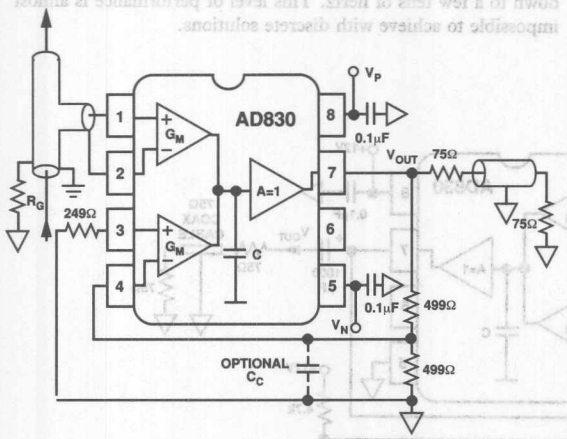


Figure 37. Cable Tap Amplifier

Resistorless Summing
Direct, two input, resistorless summing is easily realized from the general unity gain mode. By grounding V_{X2} and applying the two inputs to V_{X1} and V_{Y1}, the output is the exact sum of the applied voltages V_1 and V_3, relative to common; $V_{OUT} = V_1 + V_3$. A diagram of this simple, but potent application is shown below in Figure 38. The AD830 summing circuit possesses several virtues not present in the classic op amp based summing circuits. It has high impedance inputs, no resistors, very precise summing, high reverse isolation and noninverting gain. Achieving this function and performance with op amps requires significantly more components.

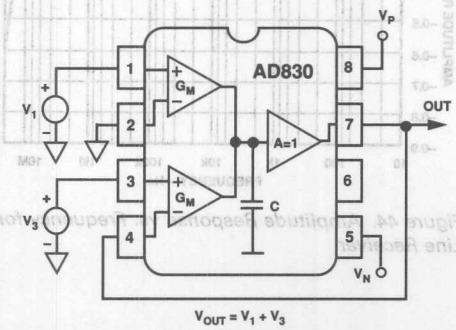


Figure 38. Resistorless Summing Amplifier

2× Gain Bandwidth Line Driver
A gain of two, without the use of resistors, is possible with the AD830. This is accomplished by grounding V_{X2}, tying the two inputs V_{X1} and V_{Y1} together and applying the input, V_{IN}, to this wired connection. The output is exactly twice the applied voltage, V_{IN}; $V_{OUT} = 2 \times V_{IN}$. Figure 39 below shows the connections for this highly useful application. The most notable characteristic of this alternative gain of two is that there is no loss of bandwidth as in a voltage feedback op amp based gain of +2 where the bandwidth is halved, therefore, the gain bandwidth is doubled. Also, this circuit is accurate without the need for any precise valued resistors, as in the op amp equivalents, and it possess excellent differential gain and phase performance as shown in Figures 40 and 41.

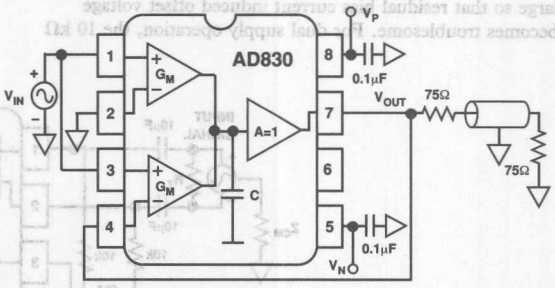


Figure 39. Full Bandwidth Line Driver (G = +2)

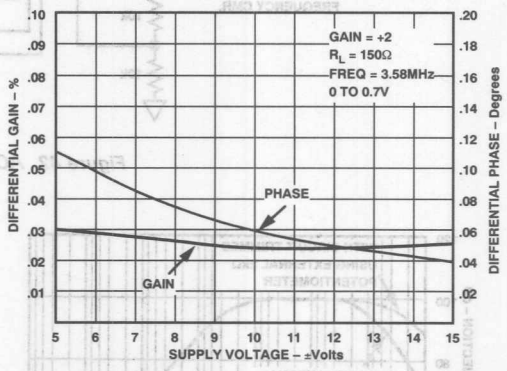


Figure 40. Differential Gain and Phase for the Circuit of Figure 39

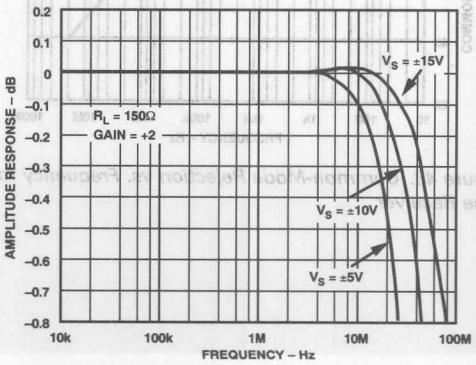


Figure 41. 0.1 dB Gain Flatness for the Circuit of Figure 39

fier on a single or bipolar supply voltages. All that is needed is inclusion of a few noncritical passive components as illustrated below in Figure 42. A simple resistive network at the X G_M input establishes a common-mode bias. Here, the common mode is centered at 6 volts, but in principle can be any voltage within the common-mode limits of the AD830. The 10 kΩ resistors to each input bias the X G_M stage with sufficiently high impedance to keep the input coupling corner frequency low, but not too large so that residual bias current induced offset voltage becomes troublesome. For dual supply operation, the 10 kΩ preserve the high frequency CMR. However, a simple resistive divider will work fine and good high frequency CMR can be maintained by placing a compensating resistor in series with the +Y input. The excellent CMRR response of the circuit is shown in Figure 43. A plot of the 0.1 dB flatness from 10 Hz is also shown. With the use of 10 μF capacitors, the CMR is >90 dB down to a few tens of hertz. This level of performance is almost impossible to achieve with discrete solutions.

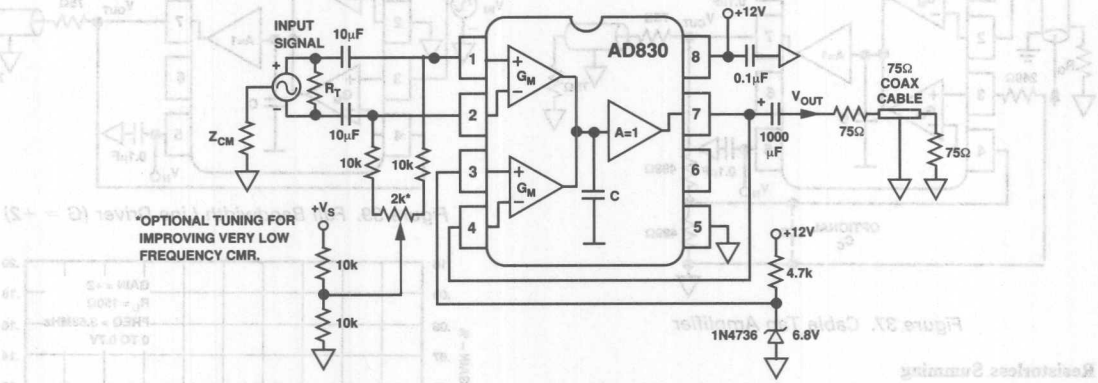


Figure 42. AC Coupled Line Receiver

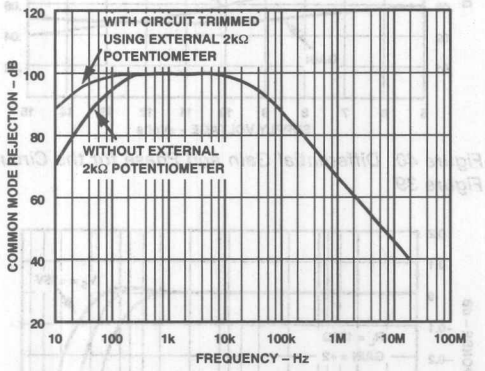


Figure 43. Common-Mode Rejection vs. Frequency for Line Receiver

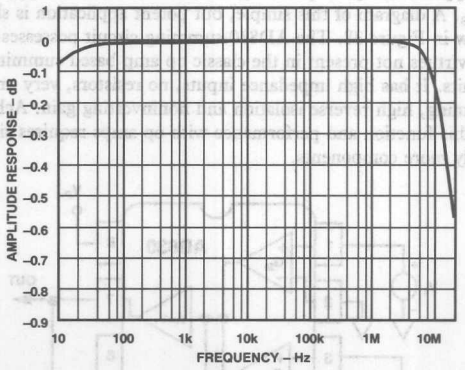


Figure 44. Amplitude Response vs. Frequency for Line Receiver

FEATURES

Wideband AC Performance
- Gain Bandwidth Product: 400 MHz (Gain ≥ 10)
- Fast Settling: 100 ns to 0.01% for a 10 V Step
- Slew Rate: 400 V/μs
- Stable at Gains of 10 or Greater
- Full Power Bandwidth: 6.4 MHz for 20 V p–p into a 500 Ω Load

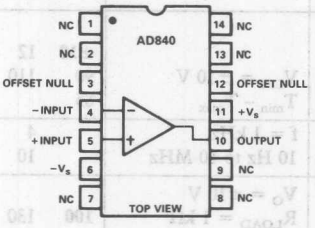
Precision DC Performance
- Input Offset Voltage: 0.3 mV max
- Input Offset Drift: 3 μV/°C typ
- Input Voltage Noise: 4 nV/$\sqrt{Hz}$
- Open-Loop Gain: 130 V/mV into a 1 kΩ Load
- Output Current: 50 mA min
- Supply Current: 12 mA max

APPLICATIONS

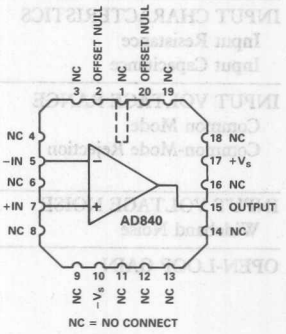
- Video and Pulse Amplifiers
- DAC and ADC Buffers
- Line Drivers
- Available in 14-Pin Plastic DIP, Hermetic Cerdip and 20-Pin LCC Packages and in Chip Form
- MIL-STD-883B Processing Available

CONNECTION DIAGRAMS

Plastic DIP (N) Package and Cerdip (Q) Package



LCC (E) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD840 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. This high speed/high precision family includes, among others, the AD841, which is unity-gain stable, and the AD842, which is stable at a gain of two or greater and has 100 mA minimum output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 400 MHz gain bandwidth product, the AD840 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in 100 ns for a 10 volt step.

The AD840 remains stable over its full operating temperature range at closed-loop gains of 10 or greater. It also offers a low quiescent current of 12 mA maximum, a minimum output current drive capability of 50 mA, a low input voltage noise of 4 nV/$\sqrt{Hz}$ and a low input offset voltage of 0.3 mV maximum (AD840K).

The 400 V/μs slew rate of the AD840, along with its 400 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD840 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD840 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD840 make it ideal for DAC and ADC buffers, line drivers and all types of video instrumentation circuitry.
2. The AD840 is truly a precision amplifier. It offers 12-bit accuracy to 0.01% or better and wide bandwidth, performance previously available only in hybrids.
3. The AD840's thermally balanced layout and the high speed of the CB process allow the AD840 to settle to 0.01% in 100 ns without the long "tails" that occur with other fast op amps.
4. Laser wafer trimming reduces the input offset voltage to 0.3 mV max on the K grade, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for additional versatility.
5. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where circuit gain will be 10 or greater.
6. The AD840 is an enhanced replacement for the HA2540.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD840—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD840J			AD840K			AD840S			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]			0.2	1		0.1	0.3		0.2	1	mV
	$T_{min} - T_{max}$			1.5			0.7			2	mV
Offset Drift			5			3			5		µV/°C
INPUT BIAS CURRENT			3.5	8		3.5	5		3.5	8	µA
	$T_{min} - T_{max}$			10			6			12	µA
INPUT OFFSET CURRENT			0.1	0.4		0.1	0.2		0.1	0.4	µA
	$T_{min} - T_{max}$			0.5			0.3			0.6	µA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			30			30			30		kΩ
Input Capacitance			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		±10	12		±10	12		±10	12		V
Common-Mode Rejection	$V_{CM} = \pm 10$ V	90	110		106	115		90	110		dB
	$T_{min} - T_{max}$	85			90			85			dB
INPUT VOLTAGE NOISE	f = 1 kHz		4			4			4		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		10			10			10		µV rms
OPEN-LOOP GAIN	$V_O = \pm 10$ V										
	R_{LOAD} = 1 kΩ	100	130		100	130		100	130		V/mV
	$T_{min} - T_{max}$	50	80		75	100		50	80		V/mV
	R_{LOAD} = 500 Ω	75			100			75			V/mV
	$T_{min} - T_{max}$	50			75			50			V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD} \geq 500\ \Omega$										
	$T_{min} - T_{max}$	±10			±10			±10			V
Current	$V_{OUT} = \pm 10$ V	50			50			50			mA
Output Resistance	Open Loop		15			15			15		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV p–p										
	$A_V = -10$		400			400			400		MHz
Full Power Bandwidth[2]	V_O = 20 V p–p										
	$R_{LOAD} \geq 500\ \Omega$	5.5	6.4		5.5	6.4		5.5	6.4		MHz
Rise Time	$A_V = -10$		10			10			10		ns
Overshoot[3]	$A_V = -10$		20			20			20		%
Slew Rate[3]	$A_V = -10$	350	400		350	400		350	400		V/µs
Settling Time[3] –10 V Step	$A_V = -10$										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
OVERDRIVE RECOVERY	–Overdrive		190			190			190		ns
	+Overdrive		350			350			350		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.025			0.025			0.025		%
DIFFERENTIAL PHASE	f = 4.4 MHz		0.04			0.04			0.04		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	V
Quiescent Current			12	14		12	14		12	14	mA
	$T_{min} - T_{max}$			16			16			18	mA
Power Supply Rejection Ratio	$V_S = \pm 5$ V to ±18 V	90	100		94	100		90	100		dB
	$T_{min} - T_{max}$	80			86			80			dB
TEMPERATURE RANGE											
Rated Performance[4]		0		+75	0		+75	−55		+125	°C
TRANSISTOR COUNT	# of Transistors		72			72			72		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full power bandwidth = slew rate/2π V_{PEAK}.
[3]Refer to Figures 22 and 23.
[4]"S" grade T_{min}–T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.
All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.5 W
Cerdip (Q) . . . . . 1.3 W
LCC (E) . . . . . 1.0 W
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
Q, E . . . . . −65°C to +150°C
N . . . . . −65°C to +125°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.

Thermal Characteristics:

	θ_{JC}	θ_{JA}	Derate at
Cerdip Package	30°C/W	110°C/W	8.7 mW/°C
Plastic Package	30°C/W	100°C/W	10 mW/°C
LCC Package	35°C/W	150°C/W	6.7 mW/°C

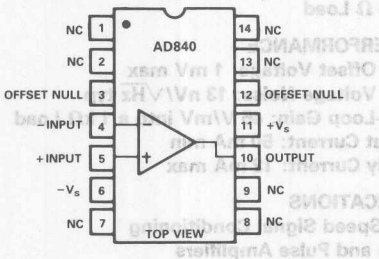
Recommended Heat Sink:
Aavid Engineering© #602B

ORDERING GUIDE

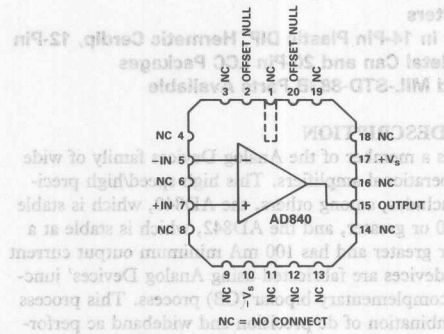
Model[1]	Package Options[2]
AD840JN	N-14
AD840KN	N-14
AD840JQ	Q-14
AD840KQ	Q-14
AD840SQ	Q-14
AD840SQ-883B	Q-14
5962-89640012A	Q-14
AD840SE-883B	E-20A
5962-8964001CA	E-20A

NOTES
[1]J and S Grade Chips also available.
[2]N = Plastic DIP; Q = Cerdip; E = LCC (Leadless Ceramic Chip Carrier). For outline information see Package Information section.

Plastic DIP (N) Package and Cerdip (Q) Package



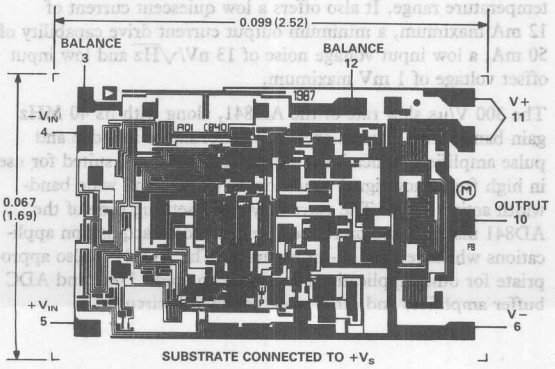
LCC (E) Package



AD840 Connection Diagrams

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Wideband, Unity-Gain Stable, Fast Settling Op Amp

AD841

FEATURES

AC PERFORMANCE
- Unity-Gain Bandwidth: 40 MHz
- Fast Settling: 110 ns to 0.01%
- Slew Rate: 300 V/μs
- Full Power Bandwidth: 4.7 MHz for 20 V p–p into a 500 Ω Load

DC PERFORMANCE
- Input Offset Voltage: 1 mV max
- Input Voltage Noise: 13 nV/$\sqrt{\text{Hz}}$ typ
- Open-Loop Gain: 45 V/mV into a 1 kΩ Load
- Output Current: 50 mA min
- Supply Current: 12 mA max

APPLICATIONS
- High Speed Signal Conditioning
- Video and Pulse Amplifiers
- Data Acquisition Systems
- Line Drivers
- Active Filters
- Available in 14-Pin Plastic DIP, Hermetic Cerdip, 12-Pin TO-8 Metal Can and 20-Pin LCC Packages
- Chips and MIL-STD-883B Parts Available

PRODUCT DESCRIPTION

The AD841 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This high speed/high precision family includes, among others, the AD840, which is stable at a gain of 10 or greater, and the AD842, which is stable at a gain of two or greater and has 100 mA minimum output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 40 MHz unity-gain bandwidth product, the AD841 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in 110 ns for a 10 volt step.

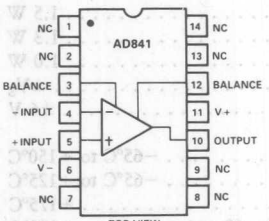
Unlike many high frequency amplifiers, the AD841 requires no external compensation. It remains stable over its full operating temperature range. It also offers a low quiescent current of 12 mA maximum, a minimum output current drive capability of 50 mA, a low input voltage noise of 13 nV/$\sqrt{\text{Hz}}$ and low input offset voltage of 1 mV maximum.

The 300 V/μs slew rate of the AD841, along with its 40 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is well suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD841 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD841 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

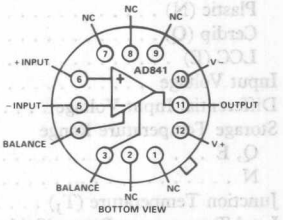
CONNECTION DIAGRAMS

Plastic DIP (N) Package and Cerdip (Q) Package



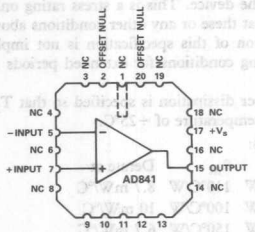
TOP VIEW
NC = NO CONNECT

TO-8 (H) Package



BOTTOM VIEW
NOTE: CAN TIED TO V+
NC = NO CONNECT

LCC (E) Package



NC = NO CONNECT

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD841 make it ideal for DAC and ADC buffers, and all types of video instrumentation circuitry.
2. The AD841 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth performance previously available only in hybrids.
3. The AD841's thermally balanced layout and the speed of the CB process allow the AD841 to settle to 0.01% in 110 ns without the long "tails" that occur with other fast op amps.
4. Laser wafer trimming reduces the input offset voltage to 1 mV max on the K grade, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for additional versatility.
5. The AD841 is an enhanced replacement for the HA2541.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD841J Min	AD841J Typ	AD841J Max	AD841K Min	AD841K Typ	AD841K Max	AD841S[1] Min	AD841S[1] Typ	AD841S[1] Max	Units
INPUT OFFSET VOLTAGE[2]			0.8	**2.0**		0.5	**1.0**		0.5	**2.0**	mV
	T_{min}–T_{max}			5.0			**3.3**			5.5	mV
Offset Drift			35			35			35		µV/°C
INPUT BIAS CURRENT			3.5	**8**		3.5	**5**		3.5	**8**	µA
	T_{min}–T_{max}			10			**6**			**12**	µA
Input Offset Current			0.1	**0.4**		0.1	**0.2**		0.1	**0.4**	µA
	T_{min}–T_{max}			0.5			**0.3**			**0.6**	µA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			200			200			200		kΩ
Input Capacitance			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**	12		**±10**	12		**±10**	12		V
Common Mode Rejection	V_{CM} = ±10 V	**86**	100		**103**	109		**86**	100		dB
	T_{min}–T_{max}	80			**100**			80			dB
INPUT VOLTAGE NOISE	f = 1 kHz		15			15			15		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		47			47			47		µV rms
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	25	45		25	45		25	45		V/mV
	T_{min}–T_{max}	12			**20**			**12**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω										
	T_{min}–T_{max}	±10			**±10**			**±10**			V
Current	V_{OUT} = ±10 V	**50**			**50**			**50**			mA
OUTPUT RESISTANCE	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Unity Gain Bandwidth	V_{OUT} = 90 mV p–p		40			40			40		MHz
Full Power Bandwidth[3]	V_O = 20 V p–p										
	R_{LOAD}≥500 Ω	3.1	4.7		3.1	4.7		3.1	4.7		MHz
Rise Time[4]	A_V = −1		10			10			10		ns
Overshoot[4]	A_V = −1		10			10			10		%
Slew Rate[4]	A_V = −1	200	300		200	300		200	300		V/µs
Settling Time – 10 V Step	A_V = −1										
	to 0.1%		90			90			90		ns
	to 0.01%		110			110			110		ns
OVERDRIVE RECOVERY	−Overdrive		200			200			200		ns
	+Overdrive		700			700			700		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.03			0.03			0.03		%
Differential Phase	f = 4.4 MHz		0.022			0.022			0.022		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		**±18**	±5		**±18**	±5		**±18**	V
Quiescent Current			11	**12**		11	**12**		11	**12**	mA
	T_{min}–T_{max}			14			**14**			**16**	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±18 V	**86**	100		**90**	100		**86**	100		dB
	T_{min}–T_{max}	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[5]		0		+75	0		+75	−55		+125	°C
PACKAGE OPTIONS[6]											
LCC (E-20A)								AD841SE, AD841SE/883B			
Cerdip (Q-14)		AD841JQ			AD841KQ			AD841SQ, AD841SQ/883B			
Plastic (N-14)		AD841JN			AD841KN						
TO-8 (H-12)		AD841JH			AD841KH			AD841SH, AD841SH/883B			
Chips		AD841J CHIPS						AD841S CHIPS			

NOTES

[1]Standard Military Drawing Available: 5962-89641012A – (SE/883B); 5962-8964101CA – (SQ/883B)

[2]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[3]Full power bandwidth = Slew Rate/2π V_{PEAK}.

[4]Refer to Figure 19.

[5]"S" grade T_{min} and T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.

[6]For outline information see Package Information section.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

Internal Power Dissipation

TO-8 (H)	1.4 W
Plastic (N)	1.5 W
Cerdip (Q)	1.3 W
Input Voltage	$\pm V_S$
Differential Input Voltage	±6 V
Storage Temperature Range	
Q, H, E	−65°C to +150°C
N	−65°C to +125°C
Junction Temperature	+175°C
Lead Temperature Range (Soldering 60 sec)	+300°C

permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

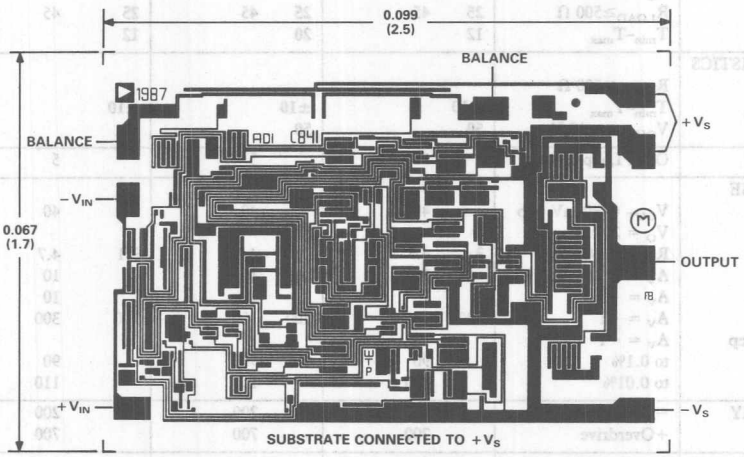
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.

Thermal Characteristics:

	θ_{JC}	θ_{JA}	θ_{SA}	
Cerdip Package	35°C/W	110°C/W	38°C/W	Recommended Heat Sink:
TO-8 Package	30°C/W	100°C/W	37°C/W	Aavid Engineering ©#602B
Plastic Package	30°C/W	100°C/W		
LCC Package	35°C/W	150°C/W		

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Wideband, High Output Current, Fast Settling Op Amp

AD842

FEATURES

AC PERFORMANCE
- Gain Bandwidth Product: 80 MHz (Gain = 2)
- Fast Settling: 100 ns to 0.01% for a 10 V Step
- Slew Rate: 375 V/μs
- Stable at Gains of 2 or Greater
- Full Power Bandwidth: 6.0 MHz for 20 V p–p

DC PERFORMANCE
- Input Offset Voltage: 1 mV max
- Input Offset Drift: 14 μV/°C
- Input Voltage Noise: 9 nV/$\sqrt{Hz}$ typ
- Open-Loop Gain: 90 V/mV into a 500 Ω Load
- Output Current: 100 mA min
- Quiescent Supply Current: 14 mA max

APPLICATIONS
- Line Drivers
- DAC and ADC Buffers
- Video and Pulse Amplifiers
- Available in Plastic DIP, Hermetic Metal Can, Hermetic Cerdip, SOIC and LCC Packages and in Chip Form
- MIL-STD-883B Parts Available
- Available in Tape and Reel in Accordance with EIA-481A Standard

PRODUCT DESCRIPTION

The AD842 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This family includes, among others, the AD840 which is stable at a gain of 10 or greater and the AD841 which is unity-gain stable. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 80 MHz gain bandwidth, the AD842 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in less than 100 ns for a 10 volt step.

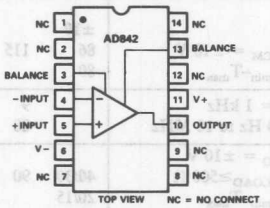
The AD842 also offers a low quiescent current of 13 mA, a high output current drive capability (100 mA minimum), a low input voltage noise of 9 nV$\sqrt{Hz}$ and a low input offset voltage (1 mV maximum).

The 375 V/μs slew rate of the AD842, along with its 80 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD842 makes this amplifier the preferred choice for data acquisition applications which require 12-bit accuracy. The AD842 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

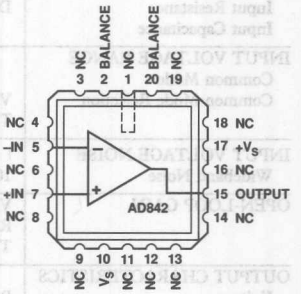
This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

CONNECTION DIAGRAMS

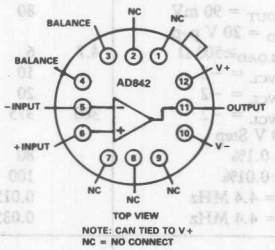
Plastic DIP (N) Package and Cerdip (Q) Package



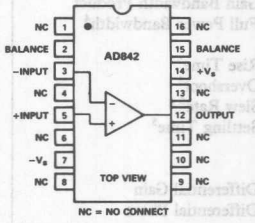
LCC (E) Package



TO-8 (H) Package



SOIC (R-16) Package



APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD842 make it ideal for DAC and ADC buffers amplifiers, lines drivers and all types of video instrumentation circuitry.
2. The AD842 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth; performance previously available only in hybrids.
3. Laser-wafer trimming reduces the input offset voltage of 1 mV max, thus eliminating the need for external offset nulling in many applications.
4. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where the circuit gain will be 2 or greater.
5. The AD842 is an enhanced replacement for the HA2542.

AD842—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD842J/JR[1] Min	Typ	Max	AD842K Min	Typ	Max	AD842S[2] Min	Typ	Max	Units
INPUT OFFSET VOLTAGE[3]			0.5	1.5		0.3	1.0		0.5	1.5	mV
	T_{min}–T_{max}			2.5/3			1.5			3.5	mV
Offset Drift			14			14			14		µV/°C
INPUT BIAS CURRENT			4.2	8		3.5	5		4.2	8	µA
	T_{min}–T_{max}			10			6			12	µA
Input Offset Current			0.1	0.4		0.05	0.2		0.1	0.4	µA
	T_{min}–T_{max}			0.5			0.3			0.6	µA
INPUT CHARACTERISTICS											
Input Resistance	Differential Mode		100			100			100		kΩ
Input Capacitance			2.0			2.0			2.0		pF
INPUT VOLTAGE RANGE											
Common Mode		±10			±10			±10			V
Common-Mode Rejection	V_{CM} = ±10 V	86	115		90	115		86	115		dB
	T_{min}–T_{max}	80			86			80			dB
INPUT VOLTAGE NOISE	f = 1 kHz		9			9			9		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		28			28			28		µV rms
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	40/30	90		50	90		40	90		V/mV
	T_{min}–T_{max}	20/15			25			20			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	±10			±10			±10			V
Current	V_{OUT} = ±10 V	100			100			100			mA
	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV		80			80			80		MHz
Full Power Bandwidth[4]	V_O = 20 V p–p										
	R_{LOAD}≥500 Ω	4.7	6		4.7	6		4.7	6		MHz
Rise Time[5]	A_{VCL} = −2		10			10			10		ns
Overshoot[5]	A_{VCL} = −2		20			20			20		%
Slew Rate[5]	A_{VCL} = −2	300	375		300	375		300	375		V/µs
Settling Time[5]	10 V Step										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
Differential Gain	f = 4.4 MHz		0.015			0.015			0.015		%
Differential Phase	f = 4.4 MHz		0.035			0.035			0.035		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	V
Quiescent Current			13/14	14/16		13	14		13	14	mA
	T_{min}–T_{max}			16/19.5			16			19	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±18 V	86	100		90	105		86	100		dB
	T_{min}–T_{max}	80			86			80			dB
TEMPERATURE RANGE											
Rated Performance[6]		0		+75	0		+75	−55		+125	°C
PACKAGE OPTIONS[7]											
Plastic (N-14)		AD842JN			AD842KN			AD842SQ, AD842SQ/883B			
Cerdip (Q-14)		AD842JQ			AD842KQ						
SOIC (R-16)		AD842JR-16									
Tape and Reel		AD842JR-16-REEL									
TO-8 (H-12A)		AD842JH			AD842KH			AD842SH			
LCC (E-20A)								AD842SE/883B			
Chips		AD842JCHIPS						AD842SCHIPS			

NOTES

[1]AD842JR specifications differ from those of the AD842JN, JQ and JH due to the thermal characteristics of the SOIC package.

[2]Standard Military Drawing available 5962-8964201xx
2A – (SE/883B); XA – (SH/883B); CA – (SQ/883B).

[3]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[4]FPBW Slew Rate/2π V_{PEAK}.

[5]Refer to Figures 22 and 23.

[6]"S" grade T_{min} and T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.

[7]For outline information see Package Information section.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Internal Power Dissipation[2]	
Plastic (N)	1.3 W
Cerdip (Q)	1.1 W
TO-8 (H)	1.3 W
SOIC (R)	1.3 W
LCC (E)	1.0 W
Input Voltage	$\pm V_S$
Differential Input Voltage	±6 V
Storage Temperature Range	
(Q, H, E)	−65°C to +150°C
(N, R)	−65°C to +125°C
Junction Temperature	+175°C
Lead Temperature Range (Soldering 60 sec)	+300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Maximum internal power dissipation is specified so that T_J does not exceed +150°C at an ambient temperature of +25°C.

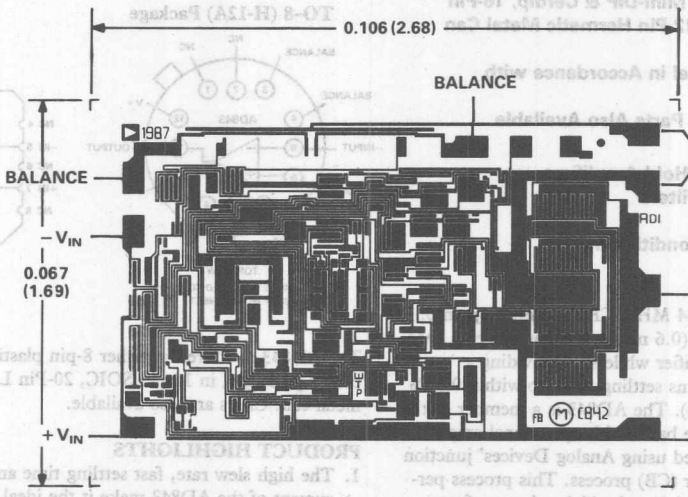
Thermal Characteristics:

	θ_{JC}	θ_{JA}	θ_{SA}
Plastic Package	30°C/W	100°C/W	
Cerdip Package	30°C/W	110°C/W	38°C/W
TO-8 Package	30°C/W	100°C/W	27°C/W
16-Pin SOIC Package	30°C/W	100°C/W	
20-Pin LCC Package	35°C/W	150°C/W	

Recommended heat sink: Aavid Engineering© #602B

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



9

Fast Settling Op Amp

AD843

FEATURES

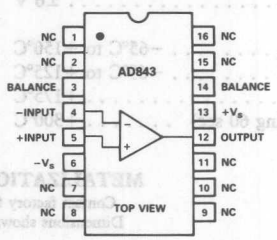
AC PERFORMANCE
- Unity Gain Bandwidth: 34 MHz
- Fast Settling: 135 ns to 0.01%
- Slew Rate: 250 V/μs
- Stable at Gains of 1 or Greater
- Full Power Bandwidth: 3.9 MHz

DC PERFORMANCE
- Input Offset Voltage: 1 mV max (AD843K/B)
- Input Bias Current: 0.6 nA typ
- Input Voltage Noise: 19 nV/$\sqrt{Hz}$
- Open Loop Gain: 30 V/mV into a 500 Ω Load
- Output Current: 50 mA min
- Supply Current: 13 mA max
- Available in 8-Pin Plastic Mini-DIP & Cerdip, 16-Pin SOIC, 20-Pin LCC and 12-Pin Hermetic Metal Can Packages
- Available in Tape and Reel in Accordance with EIA-481A Standard
- Chips and MIL-STD-883B Parts Also Available

APPLICATIONS
- High Speed Sample-and-Hold Amplifiers
- High Bandwidth Active Filters
- High Speed Integrators
- High Frequency Signal Conditioning

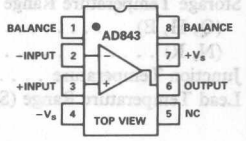
CONNECTION DIAGRAMS

16-Pin SOIC (R-16) Package



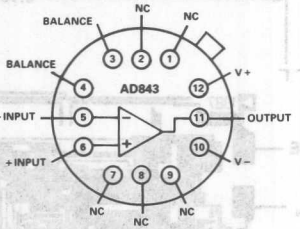
NC = NO CONNECT

Plastic (N-8) and Cerdip (Q-8) Package



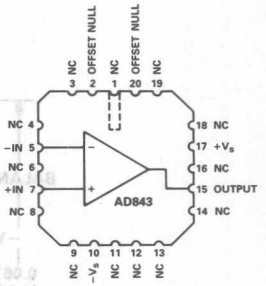
NC = NO CONNECT

TO–8 (H-12A) Package



NOTE: CAN TIED TO V+
NC = NO CONNECT

LCC (E-20A) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD843 is a fast settling, 34 MHz, CBFET input op amp. The AD843 combines the low (0.6 nA) input bias currents characteristic of a FET input amplifier while still providing a 34 MHz bandwidth and a 135 ns settling time (to within 0.01% of final value for a 10 volt step). The AD843 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp.

The 250 V/μs slew rate and 0.6 nA input bias current of the AD843 ensure excellent performance in high speed sample-and-hold applications and in high speed integrators. This amplifier is also ideally suited for high bandwidth active filters and high frequency signal conditioning circuits.

Unlike many high frequency amplifiers, the AD843 requires no external compensation and it remains stable over its full operating temperature range. It is available in five performance grades: the AD843J and AD843K are rated over the commercial temperature range of 0°C to +70°C. The AD843A and AD843B are rated over the industrial temperature range of −40°C to +85°C. The AD843S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD843 is offered in either 8-pin plastic DIP or hermetic cerdip packages, in 16-pin SOIC, 20-Pin LCC, or in a 12-pin metal can. Chips are also available.

PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time and low input bias current of the AD843 make it the ideal amplifier for 12-bit D/A and A/D buffers, for high speed sample-and-hold amplifiers and for high speed integrator circuits. The AD843 can replace many FET input hybrid amplifiers such as the LH0032, LH4104 and OPA600.
2. Fully differential inputs provide outstanding performance in all standard high frequency op amp applications such as signal conditioning and active filters.
3. Laser wafer trimming reduces the input offset voltage to 1 mV max (AD843K and AD843B).
4. Although external offset nulling is unnecessary in many applications, offset null pins are provided.
5. The AD843 does not require external compensation at closed loop gains of 1 or greater.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

INPUT OFFSET VOLTAGE[1]			1.0	**2.0**		0.5	**1.0**		1.0	**2.0**	mV
	T_{min}–T_{max}		1.7	4.0		1.2	**2.0**		3.0	**4.5**	mV
Offset Drift			12			12	35		12		µV/°C
INPUT BIAS CURRENT	Initial (T_J = +25°C)		50			40			50		pA
	Warmed-Up[2]		0.8	**2.5**		0.6	**1.0**		0.8	**2.5**	nA
	T_{min}–T_{max}			60/160			23/65			2600	nA
INPUT OFFSET CURRENT	Initial (T_J = +25°C)		30			20			30		pA
	Warmed-Up[2]		0.25	**1.0**		0.2	**0.4**		0.25	**1.0**	nA
	T_{min}–T_{max}			23/64			9/26			1025	nA
INPUT CHARACTERISTICS											
Input Resistance			10^{10}			10^{10}			10^{10}		Ω
Input Capacitance			6			6			6		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**	+12, −13		**±10**	+12, −13		**±10**	+12, −13		V
COMMON MODE REJECTION	V_{CM} = ±10 V	**60**	72		**70**	76		**60**	72		dB
	T_{min}–T_{max}	60	72		**68**	76		**60**	72		dB
INPUT VOLTAGE NOISE	f = 10 kHz		19			19			19		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		60			60			60		µV rms
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	**15**	25		**20**	30		**15**	30		V/mV
	T_{min}–T_{max}	10	20		**10**	25		**10**	25		V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	**±10**	+11.5, −12.6		**±10**	+11.5, −12.6		**±10**	+11.5, −12.6		V
Current	V_{OUT} = ±10 V	**50**			**50**			**50**			mA
Output Resistance	Open Loop		12			12			12		Ω
FREQUENCY RESPONSE											
Unity Gain Bandwidth	V_{OUT} = 90 mV p–p		34			34			34		MHz
Full Power Bandwidth[3]	V_O = 20 V p–p										
	Rl≥500 Ω	2.5	3.9		2.5	3.9		2.5	3.9		MHz
Rise Time	A_{VCL} = −1		10			10			10		ns
Overshoot	A_{VCL} = −1		15			15			15		%
Slew Rate	A_{VCL} = −1	160	250		160	250		160	250		V/µs
Settling Time	10 V Step										
	A_{VCL} = −1										
	to 0.1%		95			95			95		ns
	to 0.01%		135			135			135		ns
Overdrive Recovery	−Overdrive		200			200			200		ns
	+Overdrive		700			700			700		ns
Differential Gain	f = 4.4 MHz		0.025			0.025			0.025		%
Differential Phase	f = 4.4 MHz		0.025			0.025			0.025		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			12	**13**		12	**13**		12	**13**	mA
	T_{min}–T_{max}		12.3	14		12.3	**14**		12.5	**16**	mA
Rejection Ratio	±5 V to ±18 V	**65**	76		**70**	80		**65**	76		dB
Rejection Ratio	T_{min}–T_{max}	62	76		**68**	80		**62**	76		dB
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial (0 to +70°C)			AD843J			AD843K					
Industrial (−40°C to +85°C)			AD843A			AD843B					
Military (−55°C to +125°C)[4]									AD843S		
PACKAGE OPTIONS[5]											
Plastic (N-8)			AD843JN			AD843KN					
Cerdip (Q-8)			AD843AQ			AD843BQ			AD843SQ, AD843SQ/883B		
Metal Can (H-12A)						AD843BH			AD843SH, AD843SH/883B		
LCC (E-20A)									AD843SE/883B		
SOIC (R-16)			AD843JR								
Tape & Reel			AD843JR-REEL								
Chips			AD843JChips						AD843SChips		

9

NOTES
[1]Standard Military Drawings Available: 5962-9098001M2A (SE/883B), 5962-9098001MXA (SH/883B), 5962-9098001MPA (SQ/883B).
[2]Specifications are guaranteed after 5 minutes at T_A = +25°C.
[3]Full power bandwidth = Slew Rate/2 πV peak.
[4]All "S" grade T_{min}–T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.
[5]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested on all production units.

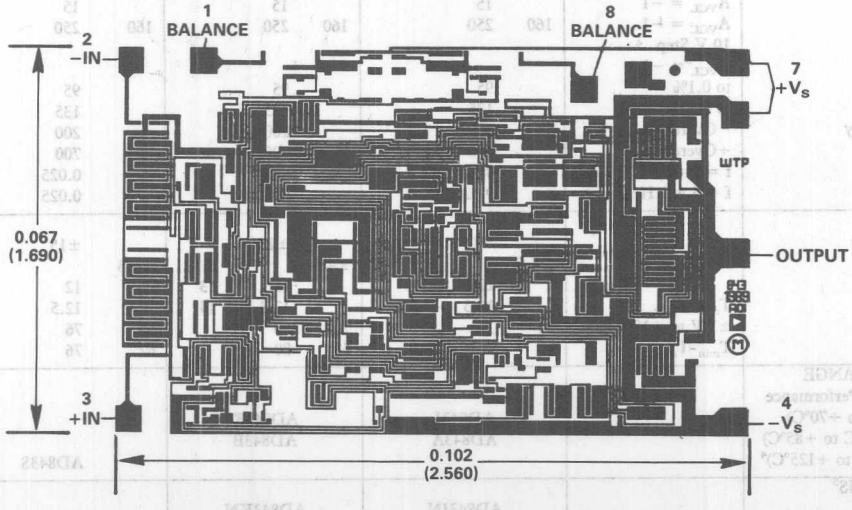
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Internal Power Dissipation[2]	
Plastic Package	1.50 Watts
Cerdip Package	1.35 Watts
12-Pin Header Package	1.80 Watts
16-Pin SOIC Package	1.50 Watts
20-Pin LCC Package	1.00 Watt
Input Voltage	$\pm V_S$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (N, R)	−65°C to +125°C
Storage Temperature Range (Q, H, E)	−65°C to +150°C
Operating Temperature Range	
AD843J/K	0 to +70°C
AD843A/B	−40°C to +85°C
AD843S	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	+300°C
ESD Rating	500 V

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 100°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
12-Pin Header Package: θ_{JA} = 80°C/Watt
16-Pin SOIC Package: θ_{JA} = 100°C/Watt
20-Pin LCC Package: θ_{JA} = 150°C/Watt

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



60 MHz, 2000 V/μs Monolithic Op Amp

AD844

FEATURES

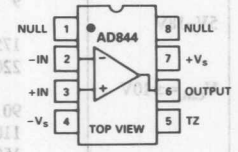
Wide Bandwidth: 60MHz at Gain of −1
33MHz at Gain of −10
Very High Output Slew Rate: Up to 2000V/μs
20MHz Full Power Bandwidth, 20V pk-pk, R_L=500Ω
Fast Settling: 100ns to 0.1% (10V Step)
Differential Gain Error: 0.03% at 4.4MHz
Differential Phase Error: 0.15° at 4.4MHz
High Output Drive: ±50mA into 50Ω Load
Low Offset Voltage: 150μV max (B Grade)
Low Quiescent Current: 6.5mA
Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

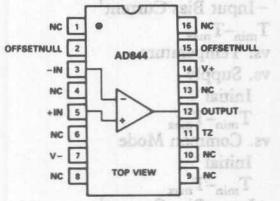
Flash ADC Input Amplifiers
High Speed Current DAC Interfaces
Video Buffers and Cable Drivers
Pulse Amplifiers

CONNECTION DIAGRAMS

8-Pin Plastic (N), and Cerdip (Q) Packages



16-Pin SOIC (R) Package



PRODUCT DESCRIPTION

The AD844 is a high speed monolithic operational amplifier fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current to voltage applications and as an inverting mode amplifier, it is also suitable for use in many non-inverting applications.

The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth which is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps. Peak output rate of change can be over 2000V/μs for a full 20V output step. Settling time is typically 100ns to 0.1%, and essentially independent of gain. The AD844 can drive 50Ω loads to ±2.5V with low distortion and is short circuit protected to 80mA.

The AD844 is available in four performance grades and three package options. In the 16-pin SOIC (R) package, the AD844J is specified for the commercial temperature range of 0 to +70°C. The AD844A and AD844B are specified for the industrial temperature range of −40°C to +85°C and are available in the cerdip (Q) package. The AD844A is also available in an 8-pin plastic mini-DIP (N). The AD844S is specified over the military temperature range of −55°C to +125°C. It is available in the 8-pin cerdip (Q) package. "A" and "S" grade chips and devices processed to MIL-STD-883B, REV. C are also available.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. The AD844 is a versatile, low cost component providing an excellent combination of ac and dc performance. It may be used as an alternative to the EL2020 and CLC400/1.
2. It is essentially free from slew rate limitations. Rise and fall times are essentially independent of output level.
3. The AD844 can be operated from ±4.5V to ±18V power supplies and is capable of driving loads down to 50Ω, as well as driving very large capacitive loads using an external network.
4. The offset voltage and input bias currents of the AD844 are laser trimmed to minimize dc errors; V_{OS} drift is typically 1μV/°C and bias current drift is typically 9nA/°C.
5. The AD844 exhibits excellent differential gain and differential phase characteristics, making it suitable for a variety of video applications with bandwidths up to 60MHz.
6. The AD844 combines low distortion, low noise and low drift with wide bandwidth, making it outstanding as an input amplifier for flash A/D converters.

AD844—SPECIFICATIONS (@ T_A=+25°C and V_S=±15V dc, unless otherwise noted)

Model	Conditions	AD844J/A Min	AD844J/A Typ	AD844J/A Max	AD844B Min	AD844B Typ	AD844B Max	AD844S Min	AD844S Typ	AD844S Max	Units
INPUT OFFSET VOLTAGE[1]			50	300		50	150		50	300	μV
T_{min}–T_{max}			75	500		75	200		125	500	μV
vs. Temperature			1			1	5		1	5	μV/°C
vs. Supply	5V–18V										
Initial			4	20		4	10		4	20	μV/V
T_{min}–T_{max}			4			4	10		4	20	μV/V
vs. Common Mode	V_{CM}=±10V										
Initial			10	35		10	20		10	35	μV/V
T_{min}–T_{max}			10			10	20		10	35	μV/V
INPUT BIAS CURRENT											
−Input Bias Current[1]			200	450		150	250		200	450	nA
T_{min}–T_{max}			800	1500		750	1100		1900	2500	nA
vs. Temperature			9			9	15		20	30	nA/°C
vs. Supply	5V–18V										
Initial			175	250		175	200		175	250	nA/V
T_{min}–T_{max}			220			220	240		220	300	nA/V
vs. Common Mode	V_{CM}=±10V										
Initial			90	160		90	110		90	160	nA/V
T_{min}–T_{max}			110			110	150		120	200	nA/V
+Input Bias Current[1]			150	400		100	200		100	400	nA
T_{min}–T_{max}			350	700		300	500		800	1300	nA
vs. Temperature			3			3	7		7	15	nA/°C
vs. Supply	5V–18V										
Initial			80	150		80	100		80	150	nA/V
T_{min}–T_{max}			100			100	120		120	200	nA/V
vs. Common Mode	V_{CM}=±10V										
Initial			90	150		90	120		90	150	nA/V
T_{min}–T_{max}			130			130	190		140	200	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
−Input			50	65		50	65		50	65	Ω
+Input		7	10		7	10		7	10		MΩ
Input Capacitance											
−Input			2			2			2		pF
+Input			2			2			2		pF
Input Voltage Range											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	f≥1kHz		2			2			2		nV/√Hz
INPUT CURRENT NOISE											
−Input	f≥1kHz		10			10			10		pA/√Hz
+Input	f≥1kHz		12			12			12		pA/√Hz
OPEN LOOP TRANSRESISTANCE	V_{OUT}=±10V										
	R_{LOAD}=500Ω	2.2	3.0		2.8	3.0		2.2	3.0		MΩ
T_{min}–T_{max}		1.3	2.0		1.6	2.0		1.3	1.6		MΩ
Transcapacitance			4.5			4.5			4.5		pF
DIFFERENTIAL GAIN ERROR[2]	f=4.4MHz		0.03			0.03			0.03		%
DIFFERENTIAL PHASE ERROR[2]	f=4.4MHz		0.15			0.15			0.15		Degree
FREQUENCY RESPONSE											
Small Signal Bandwidth											
[3]Gain=−1			60			60			60		MHz
[4]Gain=−10			33			33			33		MHz
TOTAL HARMOMIC DISTORTION	f=100kHz, 2V rms[5]		0.005			0.005			0.005		%
SETTLING TIME											
10V Output Step	±15V Supplies										
Gain=−1, to 0.1%[5]			100			100			100		ns
Gain=−10, to 0.1%[6]			100			100			100		ns
2V Output Step	±5V Supplies										
Gain=−1, to 0.1%[5]			110			110			110		ns
Gain=−10, to 0.1%[6]			100			100			100		ns

Model	Conditions	AD844J/A Min	AD844J/A Typ	AD844J/A Max	AD844B Min	AD844B Typ	AD844B Max	AD844S Min	AD844S Typ	AD844S Max	Units
OUTPUT SLEW RATE	Overdriven Input	1200	2000		1200	2000		1200	2000		V/μs
FULL POWER BANDWIDTH											
V_{OUT}=20V p-p[5]	V_S=±15V		20			20			20		MHz
V_{OUT}=2V p-p[5]	V_S=±5V THD=3%		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}=500Ω	**10**	11		**10**	11		**10**	11		±V
Short Circuit Current			80			80			80		mA
T_{min}–T_{max}			60			60			60		mA
Output Resistance	Open Loop		15			15			15		Ω
POWER SUPPLY											
Operating Range		±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current			6.5	7.5		6.5	7.5		6.5	7.5	mA
T_{min}–T_{max}			7.5	8.5		7.5	8.5		8.5	9.5	mA

NOTES
[1]Rated performance after a 5 minute warmup at T_A=25°C.
[2]Input signal 285mV p-p carrier (40 IRE) riding on 0 to 642mV (90 IRE) ramp. R_L=100Ω; R1, R2=300Ω.
[3]Input signal 0dBm, C_L=10pF, R_L=500Ω, R1=500Ω, R2=500Ω in Figure 26.
[4]Input signal 0dBm, C_L=10pF, R_L=500Ω, R1=500Ω, R2=50Ω in Figure 26.
[5]C_L=10pF, R_L=500Ω, R1=1kΩ, R2=1kΩ in Figure 26.
[6]C_L=10pF, R_L=500Ω, R1=500Ω, R2=50Ω in Figure 26.

Specifications subject to change without notice. All min and max specifications are guaranteed.
Specifications shown in **boldface** are tested on all production units at final electrical test.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Power Dissipation[2] 1.1W
Output Short Circuit Duration . . . . . Indefinite
Common Mode Input Voltage . . . . . ±V_S
Differential Input Voltage 6V
Inverting Input Current
  Continuous 5mA
  Transient 10mA
Storage Temperature Range (Q) . . . . . −65°C to +150°C
  (N, R) . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C
ESD Rating . . . . . 1000 V

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA}=100°C/Watt
8-Pin Cerdip Package: θ_{JA}=110°C/Watt
16-Pin SOIC Package: θ_{JA}=100°C/Watt

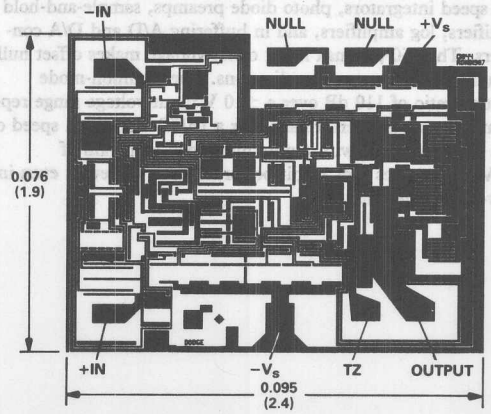
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD844JR	0°C to +70°C	R-16
AD844JR-REEL	0°C to +70°C	Tape and Reel
AD844AN	−40°C to +85°C	N-8
AD844AQ	−40°C to +85°C	Q-8
AD844BQ	−40°C to +85°C	Q-8
AD844SQ	−55°C to +125°C	Q-8
AD844SQ/883B	−55°C to +125°C	Q-8
5962-8964401PA	−55°C to +125°C	Q-8
AD844A Chips	−40°C to +85°C	Die
AD844S Chips	−55°C to +125°C	Die

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



SUBTRATE CONNECTED TO +V_S

Precision, 16 MHz CBFET Op Amp

AD845

FEATURES

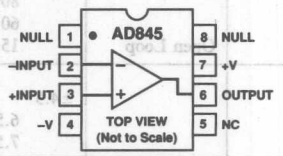
Replaces Hybrid Amplifiers in Many Applications

AC PERFORMANCE:
- Settles to 0.01% in 350 ns
- 100 V/μs Slew Rate
- 12.8 MHz min Unity-Gain Bandwidth
- 1.75 MHz Full-Power Bandwidth at 20 V p–p

DC PERFORMANCE:
- 0.25 mV max Input Offset Voltage
- 5 μV/°C max Offset Voltage Drift
- 0.5 nA Input Bias Current
- 250 V/mV min Open-Loop Gain
- 4 μV p–p max Voltage Noise, 0.1 Hz to 10 Hz
- 94 dB min CMRR
- Available in Plastic Mini-DIP, Hermetic Cerdip and SOIC Packages. Also Available in Tape and Reel in Accordance with EIA-481A Standard

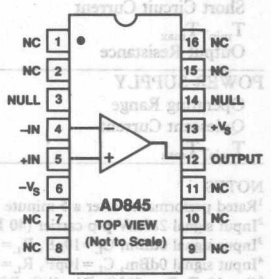
CONNECTION DIAGRAMS

Plastic Mini-DIP (N) Package and Cerdip (Q) Package



NC = NO CONNECT

16-Pin SOIC (R-16) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD845 is a fast, precise, N channel JFET input, monolithic operational amplifier. It is fabricated using Analog Devices' complementary bipolar (CB) process. Advanced laser-wafer trimming technology enables the very low input offset voltage and offset voltage drift performance to be realized. This precision, when coupled with a slew rate of 100 V/μs, a stable unity-gain bandwidth of 16 MHz, and a settling time of 350 ns 0.01%—while driving a parallel load of 100 pF and 500 Ω—represents a combination of features unmatched by any FET input IC amplifier. The AD845 can easily be used to upgrade many existing designs which use BiFET or FET input hybrid amplifiers and, in some cases, those which use bipolar input op amps.

The AD845 is ideal for use in applications such as active filters, high speed integrators, photo diode preamps, sample-and-hold amplifiers, log amplifiers, and in buffering A/D and D/A converters. The 250 μV max input offset voltage makes offset nulling unnecessary in many applications. The common-mode rejection ratio of 110 dB over a ±10 V input voltage range represents exceptional performance for a JFET input high speed op amp. This, together with a minimum open-loop gain of 250 V/mV ensures that 12-bit performance is achieved, even in unity-gain buffer circuits.

The AD845 conforms to the standard op amp pinout except that offset nulling is to V+. The AD845J and AD845K grade devices are available specified to operate over the commercial 0 to +70°C temperature range. AD845A and AD845B devices are specified for operation over the −40°C to +85°C industrial temperature range. The AD845S is specified to operate over the full military temperature range of −55°C to +125°C. Both the industrial and military versions are available in 8-pin cerdip packages. The commercial version is available in an 8-pin plastic mini-DIP and 16-pin SOIC; "J" and "S" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time, and dc precision of the AD845 make it ideal for high speed applications requiring 12-bit accuracy.
2. The performance of circuits using the LF400, HA2520/2/5, HA2620/2/5, 3550, OPA605, and LH0062 can be upgraded in most cases.
3. The AD845 is unity-gain stable and internally compensated.
4. The AD845 is specified while driving 100 pF/500 Ω loads.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD845J/A Min	AD845J/A Typ	AD845J/A Max	AD845K/B Min	AD845K/B Typ	AD845K/B Max	AD845S Min	AD845S Typ	AD845S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.7	**1.5**		0.1	**0.25**		0.25	**1.0**	mV
	T_{min}–T_{max}			2.5			**0.4**			2.0	mV
Offset Drift				20		1.5	**5.0**			**10**	μV/°C
INPUT BIAS CURRENT[2]											
Initial	V_{CM} = 0 V		0.75	**2**		0.5	**1**		0.75	**2**	nA
	T_{min}–T_{max}			45/75			**18/38**			**500**	nA
INPUT OFFSET CURRENT											
Initial	V_{CM} = 0 V		25	**300**		15	**100**		25	**300**	pA
	T_{min}–T_{max}			3/6.5			**1.2/2.6**			**20**	nA
INPUT CHARACTERISTICS											
Input Resistance			10^{11}			10^{11}			10^{11}		kΩ
Input Capacitance			4.0			4.0			4.0		pF
INPUT VOLTAGE RANGE											
Differential			±20			±20			±20		V
Common Mode		**±10**	+ 10.5/−13		**±10**	+10.5/−13		**±10**	+10.5/−13		V
Common-Mode Rejection	V_{CM} = ±10 V	**86**	110		**94**	113		**86**	110		dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		4			4			4		μV p–p
	f = 10 Hz		80			80			80		nV/√Hz
	f = 100 Hz		60			60			60		nV/√Hz
	f = 1 kHz		25			25			25		nV/√Hz
	f = 10 kHz		18			18			18		nV/√Hz
	f = 100 kHz		12			12			12		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.1			0.1			0.1		pA/√Hz
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥2 kΩ	**200**	500		**250**	500		**200**	500		V/mV
	R_{LOAD}≥500 Ω	**100**	250		**125**	250		**100**	250		V/mV
	T_{min}–T_{max}	70			75			50			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	**±12.5**			**±12.5**			**±12.5**			V
Current	Short Circuit		50			50			50		mA
Output Resistance	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Small Signal	Unity Gain	12.8	16		13.6	16		13.6	16		MHz
Full Power Bandwidth[3]	V_O = ±10 V										
	R_{LOAD} = 500 Ω		1.75			1.75			1.75		MHz
Rise Time			20			20			20		ns
Overshoot			20			20			20		%
Slew Rate		**80**	100		**94**	100		**94**	100		V/μs
Settling Time	10 V Step										
	C_{LOAD} = 100 pF										ns
	R_{LOAD} = 500 Ω										ns
	to 0.01%		350			350	500		350	500	ns
	to 0.1%		250			250			250		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.04			0.04			0.04		%
DIFFERENTIAL PHASE	f = 4.4 MHz		0.02			0.02			0.02		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±4.75		**±18**	±4.75		**±18**	±4.75		**±18**	V
Rejection Ratio	V_S = ±5 to ±15 V	**88**	110		**95**	113		**88**	110		dB
Quiescent Current	T_{min} to T_{max}		10	12		10	**12**		10	**12**	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C.

[3]FPBW=slew rate/2π V peak.

[4]"S" grade T_{min}-T_{max} are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

9

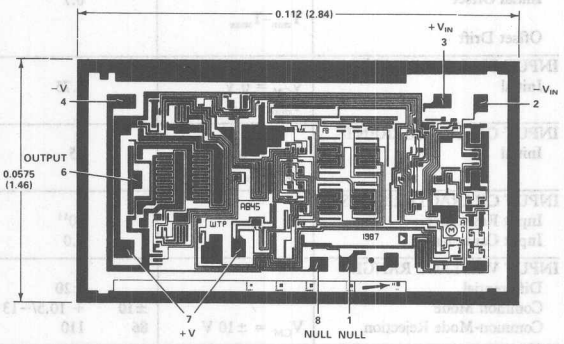
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic Mini-DIP . . . . . 1.6 Watts
Cerdip . . . . . 1.4 Watts
16-Pin SOIC . . . . . 1.5 Watts
Input Voltage . . . . . $\pm V_S$
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range
Q . . . . . −65°C to +150°C
N, R . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Mini-DIP package: θ_{JA} = 100°C/W; cerdip package: θ_{JA} = 110°C/W; SOIC package: θ_{JA} = 100°C/W.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



SUBSTRATE CONNECTED TO $+V_S$

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD845JN	0°C to +70°C	8-Pin Plastic Mini-DIP	N-8
AD845KN	0°C to +70°C	8-Pin Plastic Mini-DIP	N-8
AD845JR	0°C to +70°C	16-Pin SOIC	R-16
AD845AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD845BQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD845SQ	−55°C to +125°C	8-Pin Cerdip	Q-8
AD845SQ/883B	−55°C to +125°C	8-Pin Cerdip	Q-8
5962-8964501PA	−55°C to +125°C	8-Pin Cerdip	Q-8
AD845J Chips	0°C to +70°C	Die	
AD845S Chips	−55°C to +125°C	Die	
AD845JR-Reel	0°C to +70°C	Tape & Reel	

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

450 V/μs, Precision, Current-Feedback Op Amp

AD846

FEATURES

AC PERFORMANCE
- Small Signal Bandwidth: 80 MHz ($A_V = -1$)
- Slew Rate: 450 V/μs
- Full Power Bandwidth: 6.8 MHz at 20 V p-p, $R_L = 500\ \Omega$
- Fast Settling: for 10 V Step: 110 ns to 0.01%, 80 ns to 0.1%
- Differential Gain: <0.01% @ 4.4 MHz
- Differential Phase: <0.028° @ 4.4 MHz
- Total Harmonic Distortion (THD): 0.0005% @ 100 kHz
- Open-Loop Transimpedance: 200 MΩ
- Input Voltage Noise: 2 nV/√Hz

DC PERFORMANCE
- Input Offset Voltage: 75 μV max (B Grade)
- Input Offset Drift: 3.5 μV/°C max (B Grade)
- Quiescent Supply Current: 6.5 mA max

APPLICATIONS
- High Speed DAC Buffers
- Multiflash ADC Error Amplifiers
- Flash ADC Buffers
- Coaxial Cable Drivers
- High Performance Audio Circuitry
- Available in Plastic Mini-DIP, Hermetic Cerdip, and Hermetic Metal Can Packages
- MIL-STD-883B Parts Available

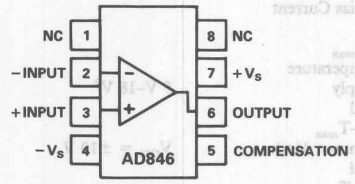
PRODUCT DESCRIPTION

The AD846 is a monolithic, very high speed operational amplifier offering high performance. Although technically classed as a current-feedback or transimpedance amplifier, it may be used in much the same way as traditional op amps while providing significant performance benefits. Employing Analog Devices' junction isolated complementary bipolar (CB) process, the AD846 achieves true "12-bit" (0.01%) precision on critical ac and dc parameters, a level of performance unmatched by amplifiers fabricated using either the dielectrically isolated (DI) or other bipolar processes.

The AD846 offers significant advantages over conventional high speed operational amplifiers. It maintains a nearly constant bandwidth and settling time to 0.01% over a wide range of closed-loop gains. This makes the AD846 ideal for amplifying the residue in multiple-pass analog-to-digital converters.

CONNECTION DIAGRAM

Plastic Mini-DIP (N) Package
and
Cerdip (Q) Package



NC = NO CONNECT
TOP VIEW

Other advantages include: low input errors and high open-loop transresistance (200 MΩ) into a 500 Ω load, ensuring true 12-bit dc accuracy for closed-loop gains from −1 to gains greater than −100. This combination of ac and dc performance makes the AD846 an excellent choice for buffering precision high speed DACs and flash ADCs.

The AD846 is available in three performance grades. The AD846A and AD846B are rated over the industrial temperature range of −40°C to +85°C. The AD846S is rated over the full military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev C.

Extended reliability PLUS screening is available specified over the commercial temperature range. PLUS screening includes 168 hour burn-in as well as other environmental and physical tests. The AD846 is available in two types of 8-pin package: plastic mini-DIP and hermetic cerdip. "A" and "S" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The AD846 achieves settling times of 110 ns to 0.01% for gains of −1 to −10, with a 450 V/μs slew rate, while consuming only 5 mA of supply current.
2. For closed-loop gains of −1 to −100, the high speed performance of the AD846 is achieved without sacrificing full 12-bit dc precision.
3. The AD846 is well suited to line driver and video buffer applications where the properties of low distortion and high slew rate are required.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD846—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD846A Min	AD846A Typ	AD846A Max	AD846B Min	AD846B Typ	AD846B Max	AD846S Min	AD846S Typ	AD846S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial			25	200		25	75		25	200	μV
T_{min}–T_{max}			50	350		50	125		100	350	μV
vs. Temperature			0.8	5		0.8	3.5		1	5.5	μV/°C
vs. Supply (PSRR)	5 V–18 V[2]										
Initial		110	125		120	125		110	125		dB
T_{min}–T_{max}		110	120		116	120		94	116		dB
vs. Common Mode (CMRR)	V_{CM} = ±10 V										
Initial		110	125		120	125		110	125		dB
T_{min}–T_{max}		110	120		116	120		94	116		dB
INPUT BIAS CURRENT[3]											
–Input Bias Current											
Initial			150	450		100	250		150	450	nA
T_{min}–T_{max}			450	1200		400	750		1000	1500	nA
vs. Temperature			6	20		6	17		9	20	nA/°C
vs. Supply	5 V–18 V[2]										
Initial			9	15		9	10		9	15	nA/V
T_{min}–T_{max}			11	20		11	15		11	25	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	10		3	5		5	10	nA/V
T_{min}–T_{max}			5	15		3	7		5	20	nA/V
+Input Bias Current											
Initial			3	15		3	5		3	15	μA
T_{min}–T_{max}			4	20		4	7		5	20	μA
vs. Temperature			15	80		15	45		15	80	nA/°C
vs. Supply	5 V–18 V[2]										
Initial			5	15		5	10		5	15	nA/V
T_{min}–T_{max}			5	20		5	15		5	20	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	15		3	10		5	15	nA/V
T_{min}–T_{max}			5	15		3	10		5	20	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
–Input			50			50			50		Ω
+Input			10			10			10		kΩ
Input Capacitance											
–Input			2			2			2		pF
+Input			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	F = 1 kHz		2			2			2		nV/√Hz
Input Current Noise											
–Input	1 kHz		20			20			20		pA/√Hz
+Input	1 kHz		6			6			6		pA/√Hz
OPEN LOOP TRANSRESISTANCE	V_{OUT} = ±10 V										
	R_{LOAD} = 500 Ω	100	200		150	200		100	200		MΩ
	T_{min}–T_{max}	50			75			50			MΩ
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} = 500 Ω	±10			±10			±10			V
Current	Short Circuit		65			65			65		mA
Output Resistance	Open Loop		16			16			16		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	A_V = –1 R_F = 1k		80			80			80		MHz
(–3dB)	A_V = –10 R_F = 875 Ω		31			31			31		MHz
	A_V = –30 R_F = 875 Ω		15			15			15		MHz
Full Power Bandwidth[4]	V_{OUT} = 20 V p–p R_L = 500 Ω		6.8			6.8			6.8		MHz
Rise Time	A_V = –1		10			10			10		ns
Overshoot	A_V = –1		20			20			20		%
Slew Rate	A_V = –1		450			450			450		V/μs
Settling Time											
10 V Step, A_V = –1	to 0.1%		80			80			80		ns
	to 0.01%		110			110			110		ns
TOTAL HARMONIC DISTORTION[5]	F = 100 kHz		0.0005			0.0005			0.0005		%

Model	Conditions	AD846A Min	AD846A Typ	AD846A Max	AD846B Min	AD846B Typ	AD846B Max	AD846S Min	AD846S Typ	AD846S Max	Units
DIFFERENTIAL GAIN	F = 4.4 MHz, R_L = 100 Ω		0.01			0.01			0.01		%
DIFFERENTIAL PHASE	F = 4.4 MHz, R_L = 100 Ω		0.028			0.028			0.028		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	V
Quiescent Current	T_{min}–T_{max}		5	6.5		5	6.5		5	7	mA
TRANSISTOR COUNT			72			72			72		

NOTES
[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Test Conditions: $+V_S$ = 15 V, $-V_S$ = 5 V to 18 V and $+V_S$ = 5 V to 18 V, $-V_S$ = 15 V.
[3]Bias Current Specifications are guaranteed maximum after 5 minutes at T_A = +25°C.
[4]FPBW = Slew Rate/2 π V_{PEAK}.
[5]Total Harmonic Distortion.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic Package . . . . . 1.5 W
  Cerdip Package . . . . . 1.3 W
Common-Mode Input Voltage, Max Safe . . . . . $|V_S|$ −3 V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . ±1 V
Continuous Input Current
  Inverting or Noninverting . . . . . 2.0 mA
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N) . . . . . −65°C to +125°C
Operating Temperature Range
  AD846A/B . . . . . −40°C to +85°C
  AD846S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C
ESD Rating . . . . . 3500 V

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C, derate cerdip (Q) package at 8.7 mW/°C and plastic (N) package at 10 mW/°C.
Plastic Package: θ_{JA} = 100°C/Watt, θ_{JC} =33°C/W.
Cerdip Package: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/W.

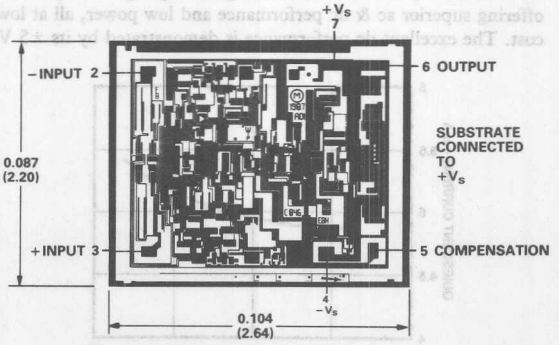
ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD846AN	−40°C to +85°C	N-8
AD846BN	−40°C to +85°C	N-8
AD846AQ	−40°C to +85°C	Q-8
AD846BQ	−40°C to +85°C	Q-8
AD846SQ	−55°C to +125°C	Q-8
AD846SQ/883B	−55°C to +125°C	Q-8
5962-8964601PA	−55°C to +125°C	Q-8

NOTES
[1]"A" and "S" grade chips are also available.
[2]N = Plastic DIP Package; Q = Cerdip Package. For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Consult factory for latest dimensions.



High Speed, Low Power Monolithic Op Amp

AD847

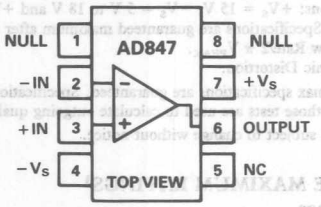
FEATURES

Superior Performance
- High Unity Gain BW: 50 MHz
- Low Supply Current: 5.3 mA
- High Slew Rate: 300 V/μs
- Excellent Video Specifications
  - 0.04% Differential Gain (NTSC and PAL)
  - 0.19° Differential Phase (NTSC and PAL)
- Drives Any Capacitive Load
- Fast Settling Time to 0.1% (10 V Step): 65 ns
- Excellent DC Performance
  - High Open-Loop Gain 5.5 V/mV (R_{LOAD} = 1 kΩ)
  - Low Input Offset Voltage: 0.5 mV
- Specified for ±5 V and ±15 V Operation
- Available in a Wide Variety of Options
  - Plastic DIP and SOIC Packages
  - Cerdip Package
  - Die Form
  - MIL-STD-883B Processing
  - Tape & Reel (EIA-481A Standard)
- Dual Version Available: AD827 (8 Lead)
- Enhanced Replacement for LM6361
- Replacement for HA2544, HA2520/2/5 and EL2020

APPLICATIONS
- Video Instrumentation
- Imaging Equipment
- Copiers, Fax, Scanners, Cameras
- High Speed Cable Driver
- High Speed DAC and Flash ADC Buffers

CONNECTION DIAGRAM

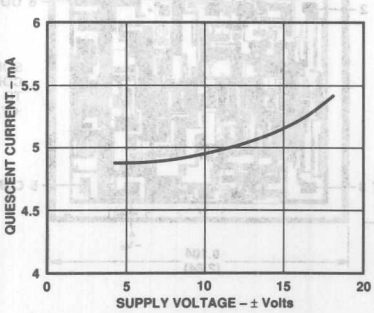
Plastic DIP (N),
Small Outline (R) and
Cerdip (Q) Packages



NC = NO CONNECT

PRODUCT DESCRIPTION

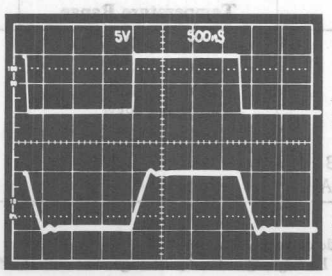
The AD847 represents a breakthrough in high speed amplifiers offering superior ac & dc performance and low power, all at low cost. The excellent dc performance is demonstrated by its ±5 V specifications which include an open-loop gain of 3500 V/V (500 Ω load) and low input offset voltage of 0.5 mV. Common-mode rejection is a minimum of 78 dB. Output voltage swing is ±3 V into loads as low as 150 Ω. Analog Devices also offers over 30 other high speed amplifiers from the low noise AD829 (1.7 nV/√Hz) to the ultimate video amplifier, the AD811, which features 0.01% differential gain and 0.01° differential phase.



Quiescent Current vs. Supply Voltage

APPLICATION HIGHLIGHTS

1. As a buffer the AD847 offers a full-power bandwidth of 12.7 MHz (5 V p–p with ±5 V supplies) making it outstanding as an input buffer for flash A/D converters.
2. The low power and small outline package of the AD847 make it very well suited for high density applications such as multiple pole active filters.
3. The AD847 is internally compensated for unity gain operation and remains stable when driving any capacitive load.



AD847 Driving Capacitive Loads

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD847J Min	AD847J Typ	AD847J Max	AD847AR Min	AD847AR Typ	AD847AR Max	Units
INPUT OFFSET VOLTAGE[1]		±5 V		0.5	**1**		0.5	**1**	mV
	T_{MIN} to T_{MAX}				3.5			4	mV
Offset Drift				15			15		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	**6.6**		3.3	**6.6**	µA
	T_{MIN} to T_{MAX}				7.2			10	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	**300**		50	**300**	nA
	T_{MIN} to T_{MAX}				400			500	nA
Offset Current Drift				0.3			0.3		nA/°C
OPEN-LOOP GAIN	V_{OUT} = ±2.5 V	±5 V							
	R_{LOAD}= 500 Ω		**2**	3.5		**2**	3.5		V/mV
	T_{MIN} to T_{MAX}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		**3**	5.5		**3**	5.5		V/mV
	T_{MIN} to T_{MAX}		1.5			1.5			V/mV
DYNAMIC PERFORMANCE									
Unity Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_{OUT} = 5 V p-p								
	R_{LOAD} = 500 Ω,	±5 V		12.7			12.7		MHz
	V_{OUT} = 20 V p-p,								
	R_{LOAD} = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 1 kΩ	±5 V		200			200		V/µs
		±15 V	225	300		225	300		V/µs
Settling Time									
to 0.1%, R_{LOAD} = 250 Ω	−2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step, A_V = −1	±15 V		65			65		ns
to 0.01%, R_{LOAD} = 250 Ω	−2.5 V to +2.5 V	±5 V		140			140		ns
	10 V Step, A_V = −1	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			50			50		Degree
Differential Gain	f ≈ 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.04			0.04		%
Differential Phase	f ≈ 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.19			0.19		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	**78**	95		**78**	95		dB
	V_{CM} = ±12 V	±15 V	**78**	95		**78**	95		dB
	T_{MIN} to T_{MAX}		75			75			dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		**75**	86		**75**	86		dB
	T_{MIN} to T_{MAX}		72			72			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		15			15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15 V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 1 kΩ	±15 V	**12**			**12**			±V
	R_{LOAD} = 500 Ω	±15 V	**10**			**10**			±V
Short-Circuit Current		±15 V		32			32		mA
INPUT RESISTANCE				300			300		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			± 4.5		**±18**	±4.5		**±18**	V
Quiescent Current		±5 V		4.8	**6.0**		4.8	**6.0**	mA
	T_{MIN} to T_{MAX}				7.3			7.3	mA
		±15 V		5.3	**6.3**		5.3	**6.3**	mA
	T_{MIN} to T_{MAX}				7.6			7.6	mA

NOTES

[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]Full Power Bandwidth = Slew Rate/2π V_{PEAK}.

[3]Slew Rate is measured on rising edge.

All min and max specifications are guaranteed. Specifications in **boldface** are 100% tested at final electrical test.

Specifications subject to change without notice.

	T_{MIN} to T_{MAX}				4			4	mV
Offset Drift				15			15		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	5		3.3	5	µA
	T_{MIN} to T_{MAX}				7.5			7.5	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	300		50	300	nA
	T_{MIN} to T_{MAX}				400			400	nA
Offset Current Drift				0.3			0.3		nA/°C
OPEN LOOP GAIN	V_{OUT} = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		2	3.5		2	3.5		V/mV
	T_{MIN} to T_{MAX}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		3	5.5		3	5.5		V/mV
	T_{MIN} to T_{MAX}		1.5			1.5			V/mV
DYNAMIC PERFORMANCE									
Unity Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_{OUT} = 5 V p-p								
	R_{LOAD} = 500 Ω,	±5 V		12.7			12.7		MHz
	V_{OUT} = 20 V p-p,								
	R_{LOAD} = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 1 kΩ	±5 V		200			200		V/µs
		±15 V	225	300		225	300		V/µs
Settling Time									
to 0.1%, R_{LOAD} = 250 Ω	−2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step, A_V = −1	±15 V		65			65		ns
to 0.01%, R_{LOAD} = 250 Ω	−2.5 V to +2.5 V	±5 V		140			140		ns
	10 V Step, A_V = −1	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			50			50		Degree
Differential Gain	f ≈ 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.04			0.04		%
Differential Phase	f ≈ 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.19			0.19		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	80	95		80	95		dB
	V_{CM} = ±12 V	±15 V	80	95		80	95		dB
	T_{MIN} to T_{MAX}		75			75			dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		75	86		75	86		dB
	T_{MIN} to T_{MAX}		72			72			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		15			15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE									
VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15 V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3		2.5	3		±V
	R_{LOAD} = 1 kΩ	±15 V	12			12			±V
	R_{LOAD} = 500 Ω	±15 V	10			10			±V
Short-Circuit Current		±15 V		32			32		mA
INPUT RESISTANCE				300			300		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			± 4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		4.8	5.7		4.8	5.7	mA
	T_{MIN} to T_{MAX}				7.0			7.8	mA
		±15 V		5.3	6.3		5.3	6.3	mA
	T_{MIN} to T_{MAX}				7.6			8.4	mA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Internal Power Dissipation[2]	
Plastic (N)	1.2 Watts
Small Outline (R)	0.8 Watts
Cerdip (Q)	1.1 Watts
Input Voltage	$\pm V_S$
Differential Input Voltage	±6 V
Storage Temperature Range (Q)	−65°C to +150°C
(N, R)	−65°C to +125°C
Junction Temperature	175°C
Lead Temperature Range (Soldering 60 sec)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

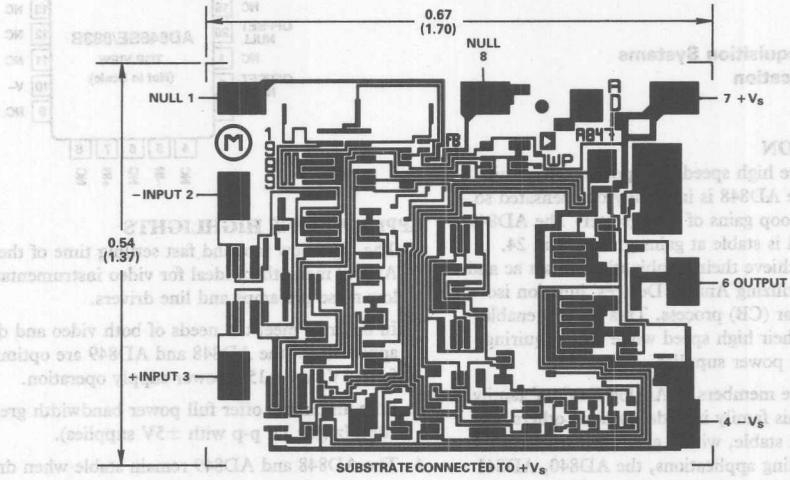
[2]Mini-DIP Package: θ_{JA} = 100°C/Watt; θ_{JC} = 33°C/Watt
Cerdip Package: θ_{JA} = 110°C/Watt; θ_{JC} = 30°C/Watt
Small Outline Package: θ_{JA} = 155°C/Watt; θ_{JC} = 33°C/Watt

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD847 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



ORDERING GUIDE

Model[1]	Temperature Range – °C	Package Description	Package Option[2]
AD847JN	0 to +70	Plastic	N-8
AD847JR	0 to +70	SOIC	R-8
AD847AQ	−40 to +85	Cerdip	Q-8
AD847AR	−40 to +85	SOIC	R-8
AD847SQ	−55 to +125	Cerdip	Q-8
AD847SQ/883B	−55 to +125	Cerdip	Q-8
5962-8964701PA	−55 to +125	Cerdip	Q-8

NOTES

[1]AD847 also available in J and S grade chips, and AD847JR and AD847AR are available in tape and reel.

[2]For outline information see Package Information section.

High Speed, Low Power Monolithic Op Amps

AD848/AD849

FEATURES

725MHz Gain Bandwidth – AD849
175MHz Gain Bandwidth – AD848
4.8mA Supply Current
300V/µs Slew Rate
80ns Settling Time to 0.1% for a 10V Step – AD849
Differential Gain: AD848 = 0.07%, AD849 = 0.08%
Differential Phase: AD848 = 0.08°, AD849 = 0.04°
Drives Capacitive Loads

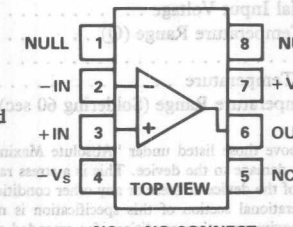
DC PERFORMANCE

3nV/$\sqrt{Hz}$ Input Voltage Noise – AD849
85V/mV Open Loop Gain into a 1kΩ Load – AD849
1mV max Input Offset Voltage
Performance Specified for ±5V and ±15V Operation
Available in Plastic, Hermetic Cerdip and Small Outline Packages. Chips and MIL-STD-883B Parts Available.
Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

Cable Drivers
8- and 10-Bit Data Acquisition Systems
Video and R_F Amplification
Signal Generators

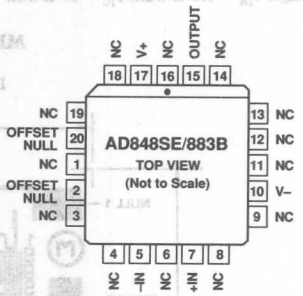
CONNECTION DIAGRAMS



Plastic (N), Small Outline (R) and Cerdip (Q) Packages

NC = NO CONNECT

20-Terminal LCC Pinout



PRODUCT DESCRIPTION

The AD848 and AD849 are high speed, low power monolithic operational amplifiers. The AD848 is internally compensated so that it is stable for closed loop gains of 5 or greater. The AD849 is fully decompensated and is stable at gains greater than 24. The AD848 and AD849 achieve their combination of fast ac and good dc performance by utilizing Analog Devices' junction isolated complementary bipolar (CB) process. This process enables these op amps to achieve their high speed while only requiring 4.8mA of current from the power supplies.

The AD848 and AD849 are members of Analog Devices' family of high speed op amps. This family includes, among others, the AD847 which is unity gain stable, with a gain bandwidth of 50MHz. For more demanding applications, the AD840, AD841 and AD842 offer even greater precision and greater output current drive.

The AD848 and AD849 have good dc performance. When operating with ±5V supplies, they offer open loop gains of 13V/mV (AD848 with a 500Ω load) and low input offset voltage of 1mV maximum. Common-mode rejection is a minimum of 92dB. Output voltage swing is ±3V even into loads as low as 150Ω.

APPLICATIONS HIGHLIGHTS

1. The high slew rate and fast settling time of the AD848 and AD849 make them ideal for video instrumentation circuitry, low noise pre-amps and line drivers.
2. In order to meet the needs of both video and data acquisition applications, the AD848 and AD849 are optimized and tested for ±5V and ±15V power supply operation.
3. Both amplifiers offer full power bandwidth greater than 20MHz (for 2V p-p with ±5V supplies).
4. The AD848 and AD849 remain stable when driving any capacitive load.
5. Laser wafer trimming reduces the input offset voltage to 1mV maximum on all grades, thus eliminating the need for external offset nulling in many applications.
6. The AD848 is an enhanced replacement for the LM6164 series and can function as a pin-for-pin replacement for many high speed amplifiers such as the HA2520/2/5 and EL2020 in applications where the gain is 5 or greater.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@T_A = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD848J Min	AD848J Typ	AD848J Max	AD848A/S Min	AD848A/S Typ	AD848A/S Max	Units
INPUT OFFSET VOLTAGE[1]		±5V		0.2	1		0.2	1	mV
		±15V		0.5	2.3		0.5	2.3	mV
	T_{min} to T_{max}	±5V			1.5			2	mV
		±15V			3.0			3.5	mV
Offset Drift		±5V, ±15V		7			7		µV/°C
INPUT BIAS CURRENT		±5V, ±15V		3.3	6.6		3.3	6.6/5	µA
	T_{min} to T_{max}	±5V, ±15V			7.2			7.5	µA
INPUT OFFSET CURRENT		±5V, ±15V		50	300		50	300	nA
	T_{min} to T_{max}	±5V, ±15V			400			400	nA
Offset Current Drift		±5V, ±15V		0.3			0.3		nA/°C
OPEN LOOP GAIN	V_O = ±2.5V	±5V							
	R_{LOAD} = 500Ω		9	13		9	13		V/mV
	T_{min} to T_{max}		7			7/5			V/mV
	R_{LOAD} = 150Ω			8			8		V/mV
	V_{OUT} = ±10V	±15V							
	R_{LOAD} = 1kΩ		12	20		12	20		V/mV
	T_{min} to T_{max}		8			8/6			V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth	A_{VCL}≥5	±5V		125			125		MHz
		±15V		175			175		MHz
Full Power Bandwidth[2]	V_O = 2V p-p,								
	R_L = 500Ω	±5V		24			24		MHz
	V_O = 20V p-p,								
	R_L = 1kΩ	±15V		4.7			4.7		MHz
Slew Rate		±5V		200			200		V/µs
	R_{LOAD} = 1kΩ	±15V	225	300		225	300		V/µs
Settling Time to 0.1%	−2.5V to +2.5V	±5V		65			65		ns
	10V Step, A_V = −4	±15V		100			100		ns
Phase Margin	C_{LOAD} = 10pF	±15V							
	R_{LOAD} = 1kΩ			60			60		Degrees
DIFFERENTIAL GAIN	f = 4.4MHz	±15V		0.07			0.07		%
DIFFERENTIAL PHASE	f = 4.4MHz	±15V		0.08			0.08		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5V	±5V	92	105		92	105		dB
	V_{CM} = ±12V	±15V	92	105		92	105		dB
	T_{min} to T_{max}		88			88			dB
POWER SUPPLY REJECTION	V_S = ±4.5V to ±18V		85	98		85	98		dB
	T_{min} to T_{max}		80			80			dB
INPUT VOLTAGE NOISE	f = 10kHz	±15V		5			5		nV/√Hz
INPUT CURRENT NOISE	f = 10kHz	±15V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500Ω	±5V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150Ω	±5V	2.5	3		2.5	3		±V
	R_{LOAD} = 50Ω	±5V		1.4			1.4		±V
	R_{LOAD} = 1kΩ	±15V	12			12			±V
	R_{LOAD} = 500Ω	±15V	10			10			±V
SHORT CIRCUIT CURRENT		±15V		32			32		mA
INPUT RESISTANCE				70			70		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5V		4.8	6.0		4.8	6.0	mA
	T_{min} to T_{max}				7.4			7.4/8.3	mA
		±15V		5.1	6.8		5.1	6.8	mA
	T_{min} to T_{max}				8.0			8.0/9.0	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]Full power bandwidth = slew rate/2π V_{PEAK}. Refer to Figure 1.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. All others are guaranteed but not necessarily tested.

Specifications subject to change without notice.

INPUT OFFSET VOLTAGE[1]		±5V		0.3	1		0.1	0.75	mV
		±15V		0.3	1		0.1	0.75	mV
	T_{min} to T_{max}	±5V			1.3			1.0	mV
		±15V			1.3			1.0	mV
Offset Drift		±5V, ±15V		2			2		µV/°C
INPUT BIAS CURRENT		±5V, ±15V		3.3	6.6		3.3	6.6/5	µA
	T_{min} to T_{max}	±5V, ±15V			7.2			7.5	µA
INPUT OFFSET CURRENT		±5V, ±15V		50	300		50	300	nA
	T_{min} to T_{max}	±5V, ±15V			400			400	nA
Offset Current Drift		±5V, ±15V		0.3			0.3		nA/°C
OPEN LOOP GAIN	V_O = ±2.5V	±5V							
	R_{LOAD} = 500Ω		30	50		30	50		V/mV
	T_{min} to T_{max}		20			20/15			V/mV
	R_{LOAD} = 150Ω			32			32		V/mV
	V_{OUT} = ±10V	±15V							
	R_{LOAD} = 1kΩ		45	85		45	85		V/mV
	T_{min} to T_{max}		30			30/25			V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth	A_{VCL}≥25	±5V		520			520		MHz
		±15V		725			725		MHz
Full Power Bandwidth[2]	V_O = 2V p-p,								
	R_L = 500Ω	±5V		20			20		MHz
	V_O = 20V p-p,								
	R_L = 1kΩ	±15V		4.7			4.7		MHz
Slew Rate		±5V		200			200		V/µs
	R_{LOAD} = 1kΩ	±15V	225	300		225	300		V/µs
Settling Time to 0.1%	−2.5V to +2.5V	±5V		65			65		ns
	10V Step, A_V = −24	±15V		80			80		ns
Phase Margin	C_{LOAD} = 10pF	±15V							
	R_{LOAD} = 1kΩ			60			60		Degrees
DIFFERENTIAL GAIN	f = 4.4MHz	±15V		0.08			0.08		%
DIFFERENTIAL PHASE	f = 4.4MHz	±15V		0.04			0.04		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5V	±5V	100	115		100	115		dB
	V_{CM} = ±12V	±15V	100	115		100	115		dB
	T_{min} to T_{max}		96			96			dB
POWER SUPPLY REJECTION	V_S = ±4.5V to ±18V		98	120		98	120		dB
	T_{min} to T_{max}		94			94			dB
INPUT VOLTAGE NOISE	f = 10kHz	±15V		3			3		nV/√Hz
INPUT CURRENT NOISE	f = 10kHz	±15V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500Ω	±5V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150Ω	±5V	2.5	3		2.5	3		±V
	R_{LOAD} = 50Ω	±5V		1.4			1.4		±V
	R_{LOAD} = 1kΩ	±15V	12			12			±V
	R_{LOAD} = 500Ω	±15V	10			10			±V
SHORT CIRCUIT CURRENT		±15V		32			32		mA
INPUT RESISTANCE				25			25		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5V		4.8	6.0		4.8	6.0	mA
	T_{min} to T_{max}				7.4			7.4/8.3	mA
		±15V		5.1	6.8		5.1	6.8	mA
	T_{min} to T_{max}				8.0			8.0/9.0	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]Full power bandwidth = slew rate/2π V_{PEAK}. Refer to Figure 1.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. All others are guaranteed but not necessarily tested.

Specifications subject to change without notice.

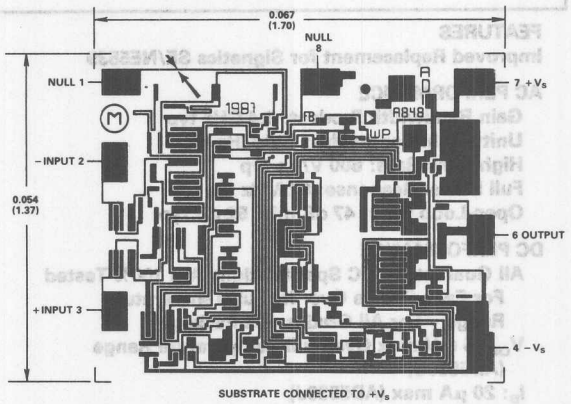
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.1 Watts
Small Outline (R) . . . . . 0.9 Watts
Cerdip (Q) . . . . . 1.1 Watts
LCC (E) . . . . . 0.8 Watts
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6V
Storage Temperature Range (Q) . . . . . −65°C to +150°C
(N, R) . . . . . −65°C to +125°C
Junction Temperature . . . . . +175°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]LCC: θ_{JA} = 150°C/Watt
Mini-DIP Package: θ_{JA} = 110°C/Watt
Cerdip Package: θ_{JA} = 110°C/Watt
Small Outline Package: θ_{JA} = 155°C/Watt.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions. (AD848 and AD849 are identical except for the part number in the upper right.)
Dimensions shown in inches and (mm).



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ORDERING GUIDE

Model	Gain Bandwidth MHz	Min Stable Gain	Max Offset Voltage mV	Temperature Range – °C	Package Option[1]
AD848JN	175	5	1	0 to +70	N-8
AD848JR[2]	175	5	1	0 to +70	R-8
AD848JCHIPS	175	5	1	0 to +70	Die Form
AD848AQ	175	5	1	−40 to +85	Q-8
AD848SQ	175	5	1	−55 to +125	Q-8
AD848SQ/883B	175	5	1	−55 to +125	Q-8
AD848SE/883B	175	5	1	−55 to +125	E-20A
AD849JN	725	25	1	0 to +70	N-8
AD849JR[2]	725	25	1	0 to +70	R-8
AD849AQ	725	25	0.75	−40 to +85	Q-8
AD849SQ	725	25	0.75	−55 to +125	Q-8
AD849SQ/883B	725	25	0.75	−55 to +125	Q-8
AD847J/A/S	50	1	1	See AD847 Data Sheet	

NOTES
[1]E = LCC; N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[2]Plastic SOIC (R) available in tape and reel. AD848 available in S grade chips. AD849 available in J and S grade chips.

Ultrahigh Frequency Operational Amplifier

AD5539

FEATURES

Improved Replacement for Signetics SE/NE5539

AC PERFORMANCE

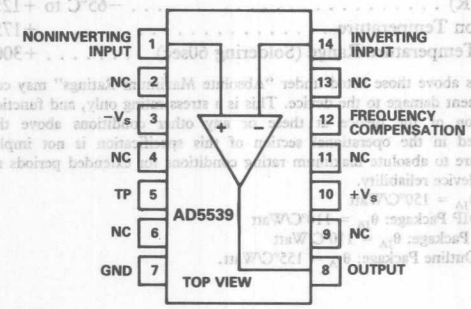
- Gain Bandwidth Product: 1.4 GHz typ
- Unity Gain Bandwidth: 220 MHz typ
- High Slew Rate: 600 V/μs typ
- Full Power Response: 82 MHz typ
- Open-Loop Gain: 47 dB min, 52 dB typ

DC PERFORMANCE

- All Guaranteed DC Specifications Are 100% Tested For Each Device Over Its Full Temperature Range – For All Grades and Packages
- V_{OS}: 5 mV max Over Full Temperature Range (AD5539S)
- I_B: 20 μA max (AD5539J)
- CMRR: 70 dB min, 85 dB typ
- PSRR: 100 μV/V typ
- MIL-STD-883B Parts Available

CONNECTION DIAGRAM

Plastic DIP (N) Package
or Cerdip (Q) Package



PRODUCT DESCRIPTION

The AD5539 is an ultrahigh frequency operational amplifier designed specifically for use in video circuits and RF amplifiers. Requiring no external compensation for gains greater than 5, it may be operated at lower gains with the addition of external compensation.

As a superior replacement for the Signetics NE/SE5539, each AD5539 is 100% dc tested to meet all of its guaranteed dc specifications over the full temperature range of the device.

The high slew rate and wide bandwidth of the AD5539 provide low cost solutions to many otherwise complex and expensive high frequency circuit design problems.

The AD5539 is available specified to operate over either the commercial (AD5539JN/JQ) or military (AD5539SQ) temperature range. The commercial grade is available either in 14-pin plastic or cerdip packages. The military version is supplied in the cerdip package. Chip versions are also available.

PRODUCT HIGHLIGHTS

1. All guaranteed dc specifications are 100% tested.
2. The AD5539 drives 50 Ω and 75 Ω loads directly.
3. Input voltage noise is less than 4 $nV\sqrt{Hz}$.
4. Low cost RF and video speed performance.
5. ±2 volt output range into a 150 Ω load.
6. Low cost.
7. Chips available.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C and V_S = ±8 V dc, unless otherwise noted)

Parameter	AD5539J Min	AD5539J Typ	AD5539J Max	AD5539S Min	AD5539S Typ	AD5539S Max	Units
INPUT OFFSET VOLTAGE							
Initial Offset[1]		2	5		2	3	mV
T_{min} to T_{max}			6			5	mV
INPUT OFFSET CURRENT							
Initial Offset[2]		0.1	2		0.1	1	µA
T_{min} to T_{max}			5			3	µA
INPUT BIAS CURRENT							
Initial[2]							
V_{CM} = 0		6	20		6	13	µA
Either Input							
T_{min} to T_{max}			40			25	µA
FREQUENCY RESPONSE							
R_L = 150 Ω[3]							
Small Signal Bandwidth		220			220		MHz
A_{CL} = 2[4]							
Gain Bandwidth Product		1400			1400		MHz
A_{CL} = 26 dB							
Full Power Response							
A_{CL} = 2[4]		68			68		MHz
A_{CL} = 7		82			82		MHz
A_{CL} = 20		65			65		MHz
Settling Time (1%)		12			12		ns
Slew Rate		600			600		V/µs
Large Signal Propagation Delay		4			4		ns
Total Harmonic Distortion							
R_L = ∞		0.010			0.010		%
R_L = 100 Ω[3]		0.016			0.016		%
V_{OUT} = 2 V p–p							
A_{CL} = 7, f = 1 kHz							
INPUT IMPEDANCE		100			100		kΩ
OUTPUT IMPEDANCE (f <10 MHz)		2			2		Ω
INPUT VOLTAGE RANGE							
Differential[5]							
(Max Nondestructive)		250			250		mV
Common-Mode Voltage							
(Max Nondestructive)		2.5			2.5		V
Common-Mode Rejection Ratio							
ΔV_{CM} = 1.7 V							
R_S = 100 Ω	70	85		70	85		dB
T_{min} to T_{max}	60			60			dB
INPUT VOLTAGE NOISE							
Wideband RMS Noise (RTI)		5			5		µV
BW = 5 MHz; R_S = 50 Ω							
Spot Noise		4			4		nV√Hz
F = 1 kHz; R_S = 50 Ω							
OPEN-LOOP GAIN							
V_O = +2.3 V, −1.7 V							
R_L = 150 Ω[3]	47	52	58	47	52	58	dB
R_L = 2 kΩ	47		58	48		57	dB
T_{min} to T_{max} $-R_L$ = 2 kΩ	43		63	46		60	dB

OUTPUT CHARACTERISTICS							
Positive Output Swing							
R_L = 150 Ω[3]	+2.3	+2.8		+2.3	+2.8		V
R_L = 2 kΩ	+2.3	+3.3		+2.5	+3.3		V
T_{min} to T_{max} with R_L = 2 kΩ	+2.3			+2.3			V
Negative Output Swing							
R_L = 150 Ω[3]		−2.2	**−1.7**		−2.2	**−1.7**	V
R_L = 2 kΩ		−2.9	**−1.7**		−2.9	**−2.0**	V
T_{min} to T_{max} with R_L = 2 kΩ			**−1.5**			**−1.5**	V
POWER SUPPLY (No Load, No Resistor to $-V_S$)							
Rated Performance		±8			±8		V
Operating Range	**±4.5**		**±10**	**±4.5**		**±10**	V
Quiescent Current							
Initial I_{CC}+		14	**18**		14	**17**	mA
T_{min} to T_{max}			**20**			**18**	mA
Initial I_{CC}−		11	**15**		11	**14**	mA
T_{min} to T_{max}			**17**			**15**	mA
PSRR							
Initial		100	**1000**		100	**1000**	μV/V
T_{min} to T_{max}			**2000**			**2000**	μV/V
TEMPERATURE RANGE							
Operating,							
Rated Performance							
Commercial (0 to +70°C)	AD5539JN, AD5539JQ						
Military (−55°C to +125°C)					AD5539SQ		
PACKAGE OPTIONS[6]							
Plastic (N-14)	AD5539JN						
Cerdip (Q-14)	AD5539JQ			AD5539SQ, AD5539SQ/883B			

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C.
[3]R_X = 470 Ω to $-V_S$.
[4]Externally compensated.
[5]Defined as voltage between inputs, such that neither exceeds +2.5 V, −5.0 V from ground.
[6]For outline information see Package Information section.

Specifications subject to change without notice.

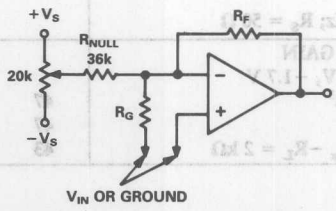
Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±10 V
Internal Power Dissipation	550 mW
Input Voltage	+2.5 V, −5.0 V
Differential Input Voltage	0.25 V
Storage Temperature Range (Q)	−65°C to +150°C
Storage Temperature Range (N)	−65°C to +125°C
Operating Temperature Range	
AD5539JN	0 to +70°C
AD5539JQ	0 to +70°C
AD5539SQ	−55°C to +125°C
Lead Temperature Range (Soldering 60 Seconds)	300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OFFSET NULL CONFIGURATION



OUTPUT NULL RANGE ≅ $+V_S\left(\frac{R_F}{R_{NULL}}\right)$ TO $-V_S\left(\frac{R_F}{R_{NULL}}\right)$

OFFSET NULL CONFIGURATION

800 MHz, 50 mW Current Feedback Amplifier

AD8001

FEATURES

Excellent Video Specifications (R_L = 150 Ω, G = +2)
- Gain Flatness 0.1 dB to 100 MHz
- 0.01% Differential Gain Error
- 0.025° Differential Phase Error

Low Power
- 5.5 mA max Power Supply Current (55 mW)

High Speed and Fast Settling
- 880 MHz, –3 dB Bandwidth (G = +1)
- 440 MHz, –3 dB Bandwidth (G = +2)
- 1200 V/μs Slew Rate
- 10 ns Settling Time to 0.1%

Low Distortion
- –65 dBc THD, f_C = 5 MHz
- 33 dBm 3rd Order Intercept, F_1 = 10 MHz
- –66 dB SFDR, f = 5 MHz

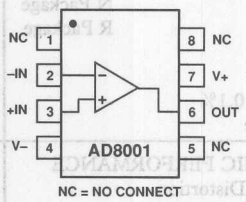
High Output Drive
- 70 mA Output Current
- Drives Up to 4 Back-Terminated Loads (75 Ω Each) While Maintaining Good Differential Gain/Phase Performance (0.05%/0.25°)

APPLICATIONS

- A-to-D Driver
- Video Line Driver
- Professional Cameras
- Video Switchers
- Special Effects
- RF Receivers

FUNCTIONAL BLOCK DIAGRAM

8-Pin Plastic Mini-DIP and SOIC



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD8001 is a low power, high speed amplifier designed to operate on ±5 V supplies. The AD8001 features unique transimpedance linearization circuitry. This allows it to drive video loads with excellent differential gain and phase performance on only 50 mW of power. The AD8001 is a current feedback amplifier and features gain flatness of 0.1 dB to 100 MHz while offering differential gain and phase error of 0.01% and 0.025°. This makes the AD8001 ideal for professional video electronics such as cameras and video switchers. Additionally, the AD8001's low distortion and fast settling make it ideal for buffer high speed A-to-D converters.

The AD8001 offers low power of 5.5 mA max (V_S = ±5 V) and can run on a single +12 V power supply, while being capable of delivering up to 70 mA of load current. All this is offered in a small 8-pin DIP or 8-pin SOIC package. These features make this amplifier ideal for portable and battery powered applications where size and power is critical.

The outstanding bandwidth of 800 MHz along with 1200 V/μs of slew rate make the AD8001 useful in many general purpose high speed applications where dual power supplies of up to ±6 V and single supplies from 6 V to 12 V are needed. The AD8001 is available in the industrial temperature range of –40°C to +85°C.

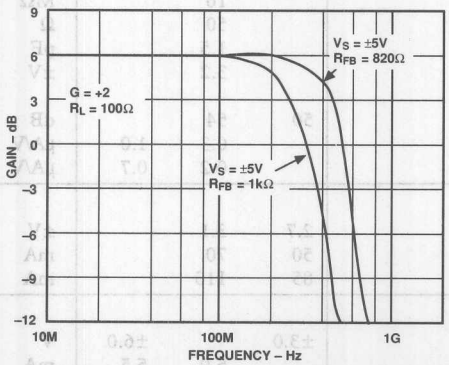


Figure 1. Frequency Response of AD8001

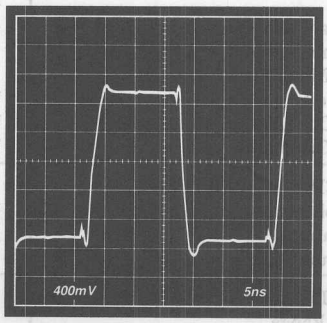


Figure 2. Transient Response of AD8001; 2 V Step, G = +2

AD8001–SPECIFICATIONS (@ T_A = + 25°C, V_S = ±5 V, R_L = 100 Ω, unless otherwise noted)

Model	Conditions	AD8001A Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, N Package	G = +2, < 0.1 dB Peaking, R_F = 750 Ω	350	440		MHz
	G = +1, < 1 dB Peaking, R_F = 1 kΩ	650	880		MHz
R Package	G = +2, < 0.1 dB Peaking, R_F = 681 Ω	350	440		MHz
	G = +1, < 0.1 dB Peaking, R_F = 845 Ω	575	715		MHz
Bandwidth for 0.1 dB Flatness					
N Package	G = +2, R_F = 750 Ω	85	110		MHz
R Package	G = +2, R_F = 681 Ω	100	125		MHz
Slew Rate	G = +2, V_O = 2 V Step	800	1000		V/µs
	G = –1, V_O = 2 V Step	960	1200		V/µs
Settling Time to 0.1%	G = –1, V_O = 2 V Step		10		ns
Rise & Fall Time	G = –1, V_O = 2 V Step, R_F = 649 Ω		1.4		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p		–65		dBc
	G = +2, R_L = 100 Ω				
Input Voltage Noise	f = 10 kHz		2.0		n V/√Hz
Input Current Noise	f = 10 kHz, +In		2.0		pA/√Hz
	–In		18		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.01	0.025	%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.025	0.04	Degree
Third Order Intercept	f = 10 MHz		33		dBm
1 dB Gain Compression	f = 10 MHz		14		dBm
SFDR	f = 5 MHz		–66		dB
DC PERFORMANCE					
Input Offset Voltage			2.0	5.5	mV
	T_{MIN}–T_{MAX}		2.0	9.0	mV
Offset Drift			10		µV/°C
–Input Bias Current			5.0	25	±µA
	T_{MIN}–T_{MAX}			35	±µA
+Input Bias Current			3.0	6.0	±µA
	T_{MIN}–T_{MAX}			10	±µA
Open Loop Transresistance	V_O = ±2.5 V	250	900		kΩ
	T_{MIN}–T_{MAX}	175			kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		10		MΩ
	–Input		50		Ω
Input Capacitance	+Input		1.5		pF
Input Common-Mode Voltage Range			3.2		±V
Common-Mode Rejection Ratio					
Offset Voltage	V_{CM} = ±2.5 V	50	54		dB
–Input Current	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		0.3	1.0	µA/V
+Input Current	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		0.2	0.7	µA/V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω	2.7	3.1		±V
Output Current	R_L = 37.5 Ω	50	70		mA
Short Circuit Current		85	110		mA
POWER SUPPLY					
Operating Range		±3.0		±6.0	V
Quiescent Current	T_{MIN}–T_{MAX}		5.0	5.5	mA
Power Supply Rejection Ratio	$+V_S$ = +4 V to +6V, $-V_S$ = –5 V	60	75		dB
	$-V_S$ = –4 V to –6 V, $+V_S$ = +5 V	50	56		dB
–Input Current	T_{MIN}–T_{MAX}		0.5	2.5	µA/V
+Input Current	T_{MIN}–T_{MAX}		0.1	0.5	µA/V

Specifications subject to change without notice.

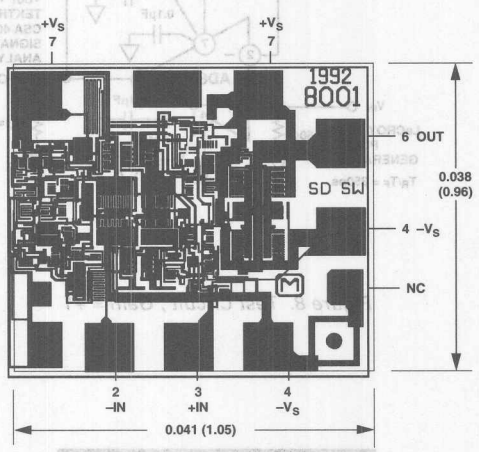
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Internal Power Dissipation[2]
Plastic Package (N) . . . . . 1.3 Watts
Small Outline Package (R) . . . . . 0.9 Watts
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±1.2 V
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range N, R . . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin Plastic Package: θ_{JA} = 90°C/Watt
8-Pin SOIC Package: θ_{JA} = 140°C/Watt

METALLIZATION PHOTO

Dimensions shown in inches and (mm).
Connect Substrate to $-V_S$.



MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8001 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8001 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

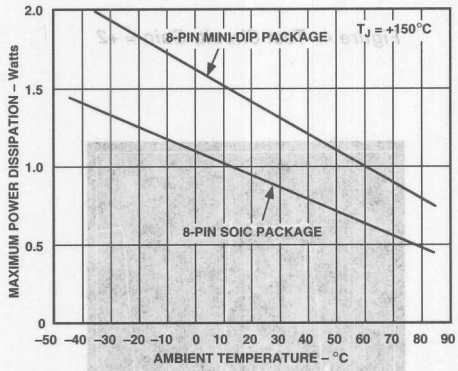


Figure 3. Plot of Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD8001AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD8001AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD8001ACHIPS	–40°C to +85°C	Die Form	
AD8001SMD[2]	–55°C to +125°C	8-Pin Cerdip	Q-8
AD8001R-EB+2[3]		SOIC Eval Board, G = +2	

NOTES
[1]For outline information see Package Information section.
[2]Standard Military Drawing Device. Ordering Number TBD. Contact our local sales office, representative or distributor for availability.
[3]Refer to Evaluation Board section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8001 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

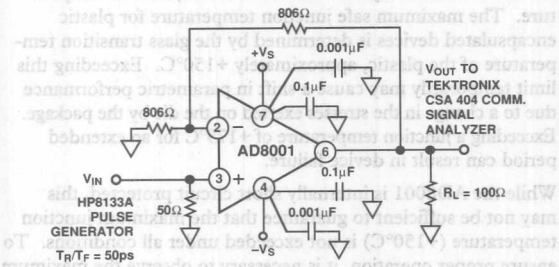


Figure 4. Test Circuit, Gain = +2

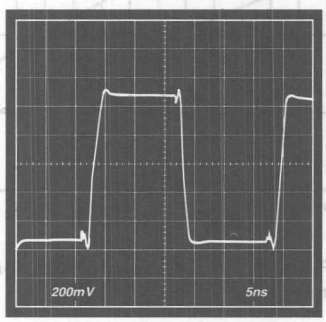


Figure 5. 1 V Step Response, G = +2

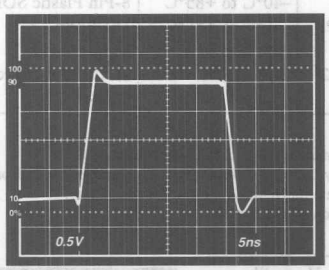


Figure 6. 2 V Step Response, G = +1

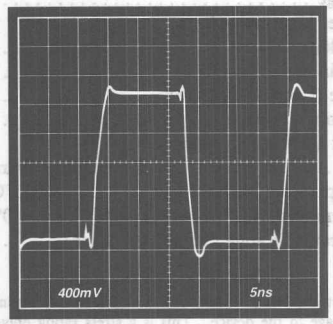


Figure 7. 2 V Step Response, G = +2

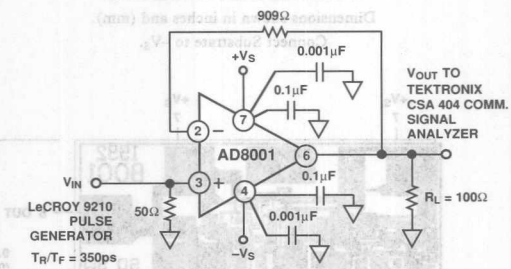


Figure 8. Test Circuit , Gain = +1

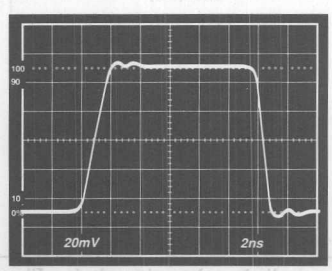


Figure 9. 100 mV Step Response, G = +1

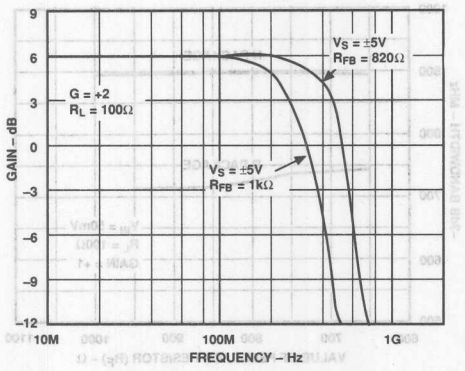


Figure 10. Frequency Response, G = +2

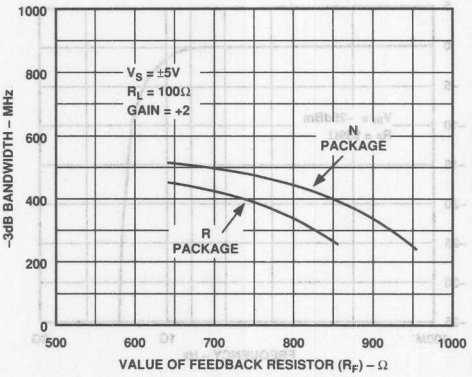


Figure 13. –3 dB Bandwidth vs. R_F

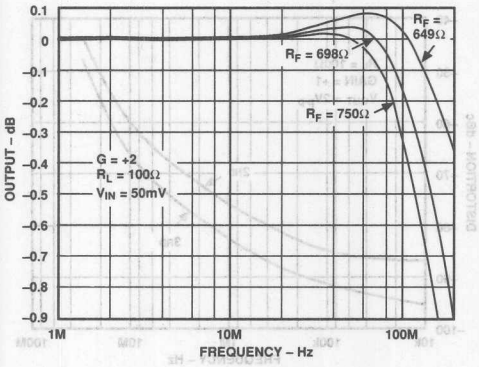


Figure 11. 0.1 dB Flatness, R Package (for N Package add 50 Ω to R_F)

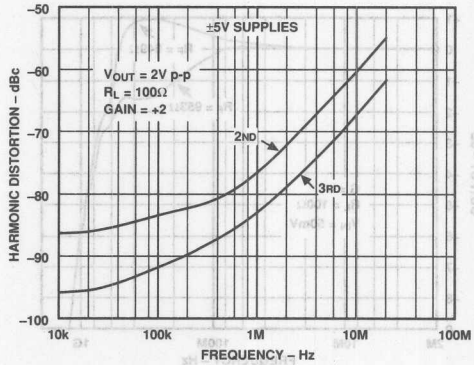


Figure 14. Distortion vs. Frequency, R_L = 100 Ω

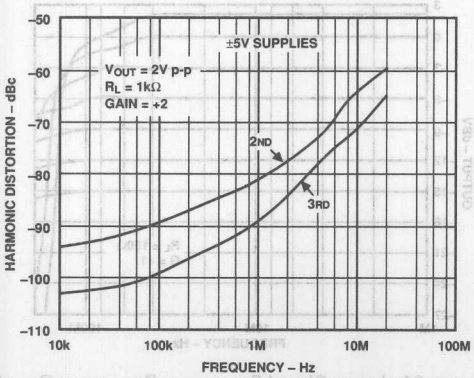


Figure 12. Distortion vs. Frequency, R_L = 1 kΩ

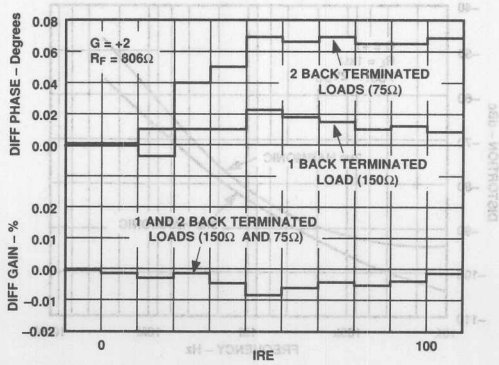


Figure 15. Differential Gain and Differential Phase

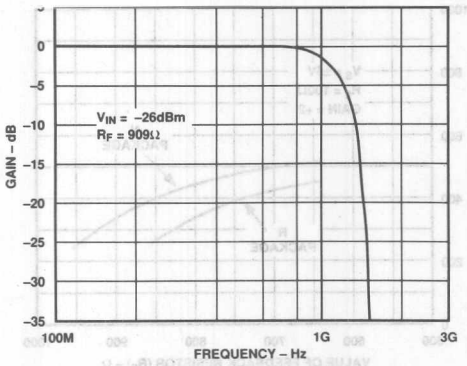


Figure16. Frequency Response, G = +1

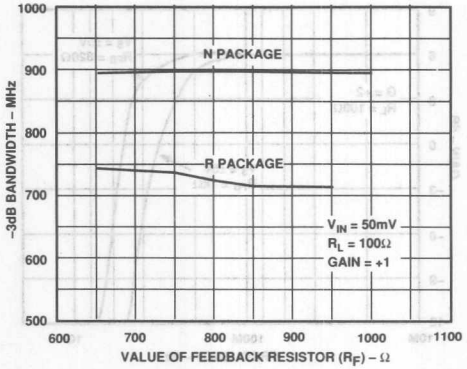


Figure 19. –3 dB Bandwidth vs. R_F, G = +1

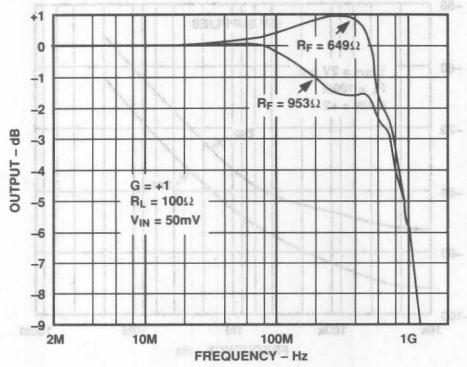


Figure 17. Flatness, R Package, G = +1 (for N Package Add 100 Ω to R_F)

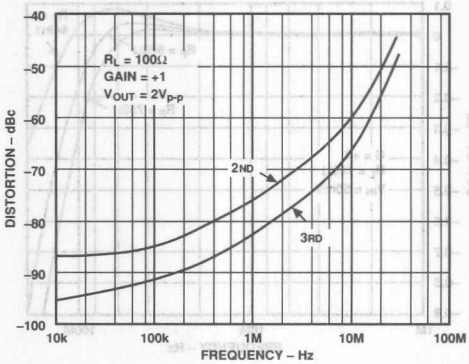


Figure 20. Distortion vs. Frequency, R_L = 100Ω

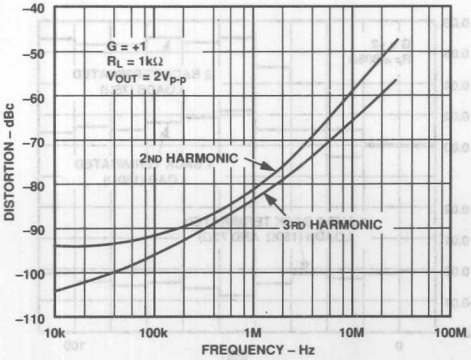


Figure 18. Distortion vs. Frequency, R_L = 1 kΩ

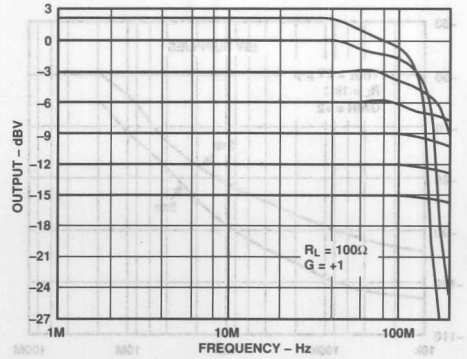


Figure 21. Large Signal Frequency Response, G = +1

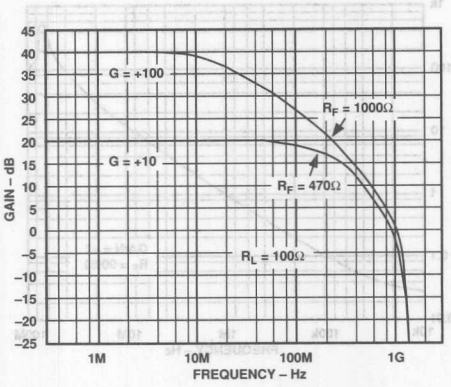


Figure 22. Frequency Response, G = +10, G = +100

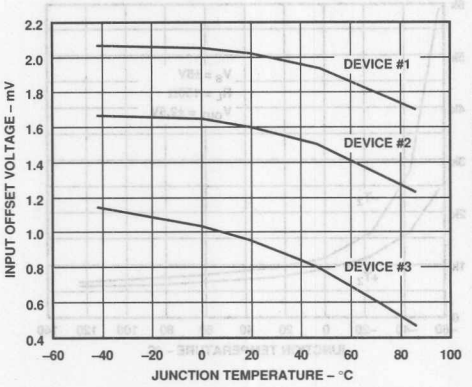


Figure 25. Input Offset vs. Temperature

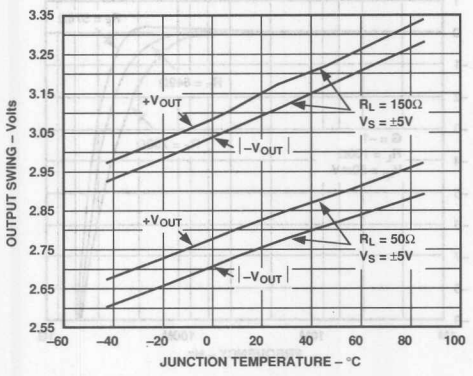


Figure 23. Output Swing vs.Temperature

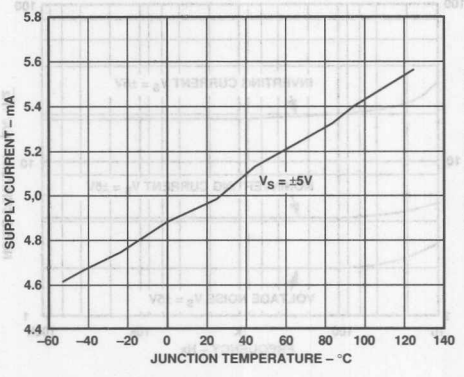


Figure 26. Supply Current vs. Temperature

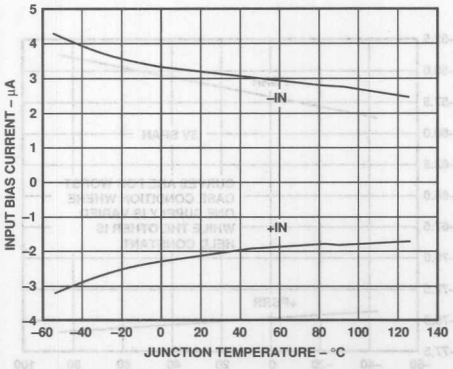


Figure 24. Input Bias Current vs. Temperature

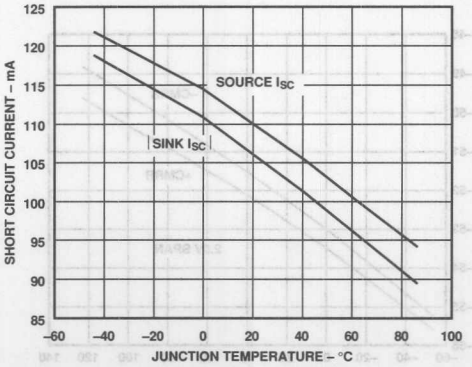


Figure 27. Short Circuit Current vs. Temperature

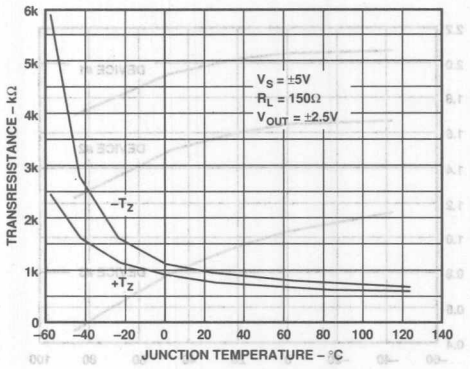


Figure 28. Transresistance vs. Temperature

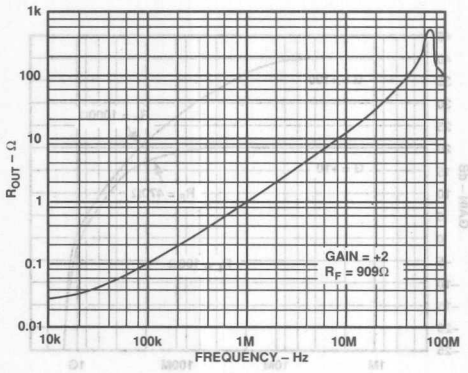


Figure 31. Output Resistance vs. Frequency

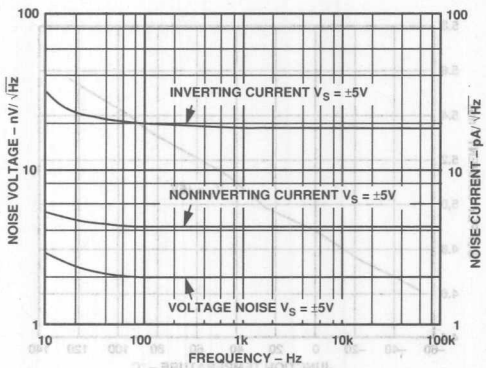


Figure 29. Noise vs. Frequency

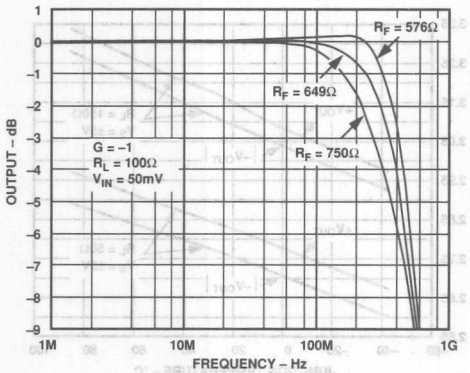


Figure 32. –3 dB Bandwidth vs. Frequency, G = –1

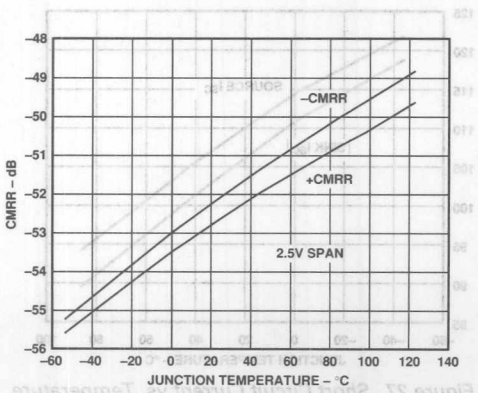


Figure 30. CMRR vs. Temperature

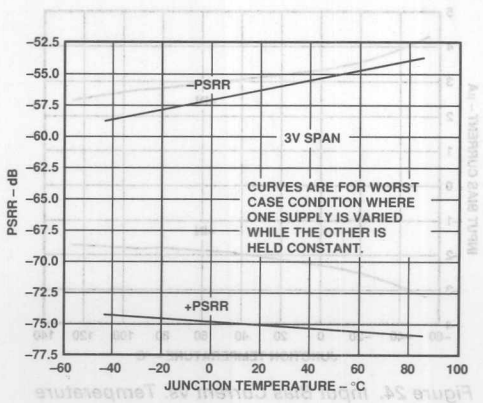


Figure 33. PSRR vs. Temperature

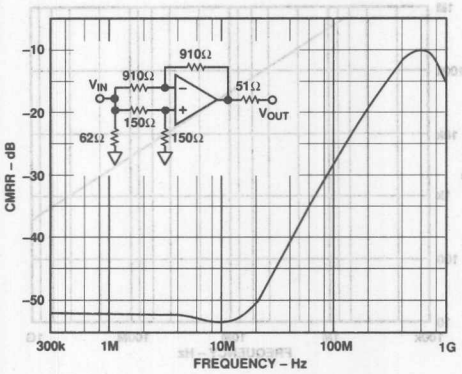


Figure 34. CMRR vs. Frequency

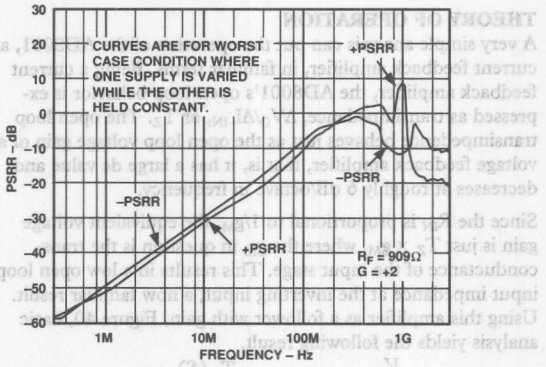


Figure 37. PSRR vs. Frequency

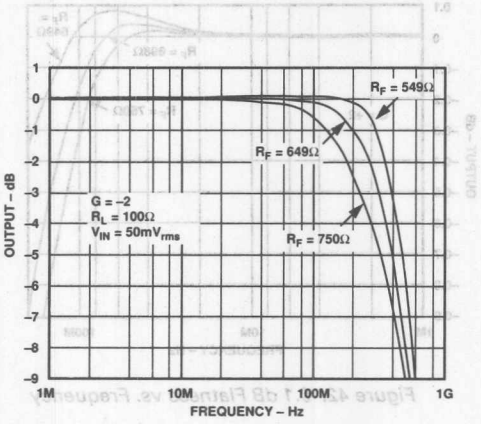


Figure 35. –3 dB Bandwidth vs. Frequency, G = –2

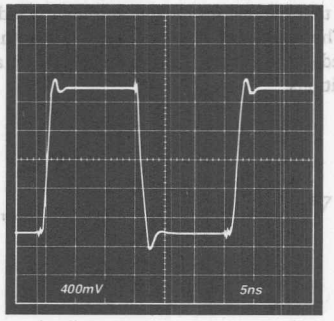


Figure 38. 2 V Step Response, G = –1

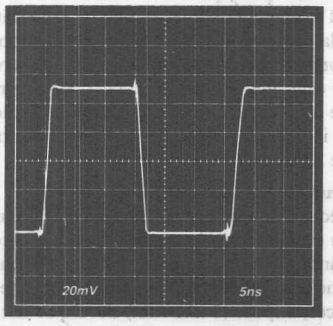


Figure 36. 100 mV Step Response, G = –1

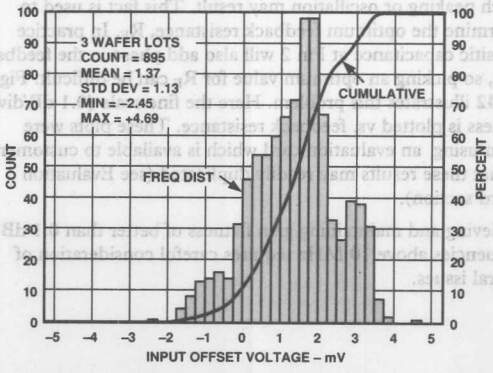


Figure 39. Input Offset Voltage Distribution

...amplifier, the AD8001's open-loop behavior is expressed as transimpedance, $\Delta V_O/\Delta I_{-IN}$, or T_Z. The open loop transimpedance behaves just as the open loop voltage gain of a voltage feedback amplifier, that is, it has a large dc value and decreases at roughly 6 dB/octave in frequency.

Since the R_{IN} is proportional to $1/g_M$, the equivalent voltage gain is just $T_Z \times g_M$, where the g_M in question is the transconductance of the input stage. This results in a low open loop input impedance at the inverting input, a now familiar result. Using this amplifier as a follower with gain, Figure 40, basic analysis yields the following result.

$$\frac{V_O}{V_{IN}} = G \times \frac{T_z(S)}{T_z(S) + G \times R_{IN} + R_1}$$

$$G = 1 + \frac{R_1}{R_2} \qquad R_{IN} = 1/g_M \approx 50\ \Omega$$

Recognizing that $G \times R_{IN} << R_1$ for low gains, it can be seen to the first order that bandwidth for this amplifier is independent of gain (G). This simple analysis in conjunction with Figure 41 in fact can predict the behavior of the AD8001 over a wide range of conditions.

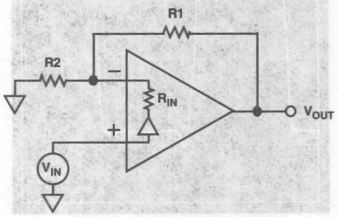


Figure 40.

Considering that additional poles contribute excess phase at high frequencies there is a minimum feedback resistance below which peaking or oscillation may result. This fact is used to determine the optimum feedback resistance, R_F. In practice parasitic capacitance at Pin 2 will also add phase in the feedback loop, so picking an optimum value for R_F can be difficult. Figure 42 illustrates this problem. Here the fine scale (0.1 dB/div) flatness is plotted vs. feedback resistance. These plots were taken using an evaluation card which is available to customers so that these results may readily duplicated (see Evaluation Board section).

Achieving and maintaining gain flatness of better than 0.1 dB at frequencies above 10 MHz requires careful consideration of several issues.

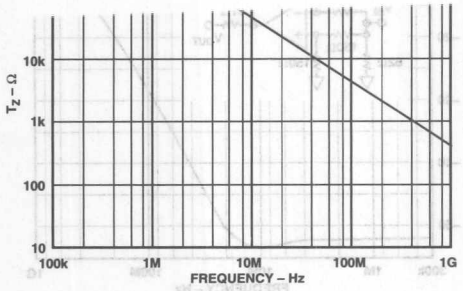


Figure 41. Transimpedance vs. Frequency

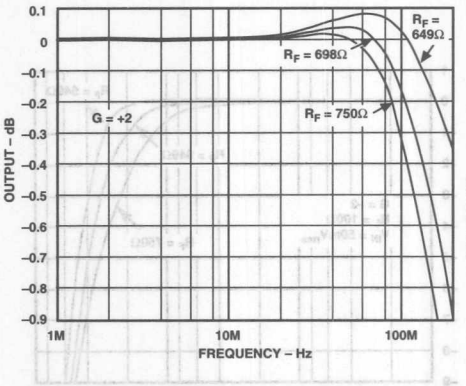


Figure 42. 0.1 dB Flatness vs. Frequency

Choice of Feedback and Gain Resistors

Because of the above mentioned relationship between the bandwidth and the feedback resistor, the fine scale gain flatness will, to some extent, vary with feedback resistance. It, therefore, is recommended that once optimum resistor values have been determined, 1% tolerance values should be used if it is desired to maintain flatness over a wide range of production lots. In addition, resistors of different construction have different associated parasitic capacitance and inductance. Surface mount resistors were used for the bulk of the characterization for this data sheet. It is not recommended that leaded components be used with the AD8001.

Printed Circuit Board Layout Considerations

As to be expected for a wideband amplifier, PC board parasitics can affect the overall closed loop performance. Of concern are stray capacitances at the output and the inverting input nodes. If a ground plane is to be used on the same side of the board as the signal traces, a space (5 mm min) should be left around the signal lines to minimize coupling. Additionally, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths on the order of less than 5 mm are recommended. If long runs of coaxial cable are being driven, dispersion and loss must be considered.

ing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 µF) will be required to provide the best settling time and lowest distortion. A parallel combination at least 4.7 µF and between 0.1 µF and 0.01 µF is recommended. Some brands of electrolyic capacitors will require a small series damping resistor ≈4.7 Ω for optimum results.

DC Errors and Noise

There are three major noise and offset terms to consider in a current feedback amplifier. For offset errors refer to the equation below. For noise error the terms are root-sum-squared to give a net output error. In the circuit below (Figure 43) they are input offset (V_{IO}) which appears at the output multiplied by the noise gain of the circuit ($1 + R_F/R_I$), Noninverting input current ($I_{BN} \times R_N$) also multiplied by the noise gain, and the inverting input current, which when divided between R_F and R_I and subsequently multiplied by the noise gain always appears at the output as $I_{BN} \times R_F$. The input voltage noise of the AD8001 is a low 2 nV/√Hz. At low gains though the inverting input current noise times R_F is the dominant noise source. Careful layout and device matching contribute to better offset and drift specifications for the AD8001 compared to many other current feedback amplifiers. The typical performance curves in conjunction with the equations below can be used to predict the performance of the AD8001 in any application.

$$V_{OUT} = V_{IO} \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{BN} \times R_N \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{BI} \times R_F$$

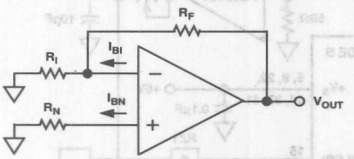


Figure 43. Output Offset Voltage

Driving Capacitive Loads

The AD8001 was designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, best frequency response is obtained by the addition of a small series resistance as shown in Figure 44. The accompanying graph shows the optimum value for R_{SERIES} vs. capacitive load. It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of R_{SERIES} and C_L.

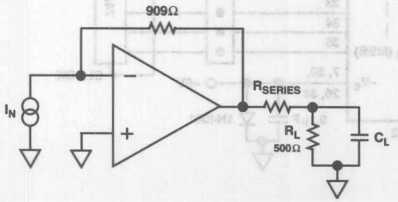


Figure 44. Driving Capacitive Loads

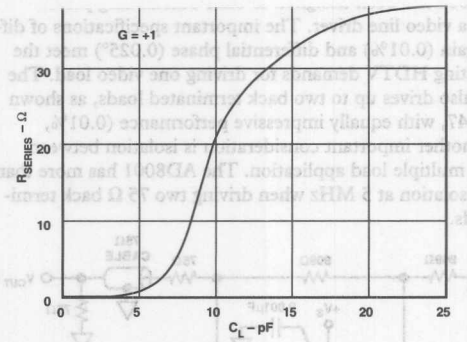


Figure 45. Recommended R_{SERIES} vs. Capacitive Load

Communications

Distortion is a key specification in communications applications. Intermodulation distortion (IMD) is a measure of the ability of an amplifier to pass complex signals without the generation of spurious harmonics. The third order products are usually the most problematic since several of them fall near the fundamentals and do not lend themselves to filtering. Theory predicts that the third order harmonic distortion components increase in power at three times the rate of the fundamental tones. The specification of third order intercept as the virtual point where fundamental and harmonic power are equal is one standard measure of distortion performance. Op amps used in closed-loop applications do not always obey this simple theory. At a gain of two the AD8001 has performance summarized in Figure 46. Here the worst third order products are plotted vs. input power. The third order intercept of the AD8001 is +33 dBm at 10 MHz.

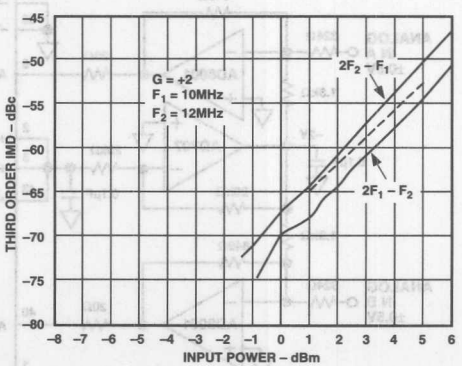


Figure 46. Third Order IMD; F_1 = 10 MHz, F_2 = 12 MHz

Operation as a Video Line Driver

The AD8001 has been designed to offer outstanding performance as a video line driver. The important specifications of differential gain (0.01%) and differential phase (0.025°) meet the most exacting HDTV demands for driving one video load. The AD8001 also drives up to two back terminated loads, as shown in Figure 47, with equally impressive performance (0.01%, 0.07°). Another important consideration is isolation between loads in a multiple load application. The AD8001 has more than 40 dB of isolation at 5 MHz when driving two 75 Ω back terminated loads.

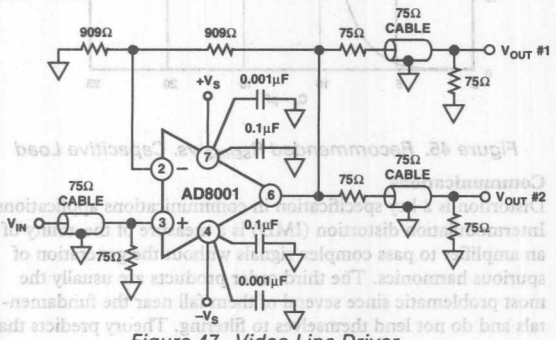


Figure 47. Video Line Driver

Driving A-to-D Converters

The AD8001 is well suited for driving high speed analog-to-digital converters such as the AD9058. The AD9058 is a dual 8-bit 50 Msps ADC. In the circuit below two AD8001s are shown driving the inputs of the AD9058 which are configured for 0 V to +2 V ranges. Bipolar input signals are buffered, amplified (–2×), and offset (by +1.0 V) into the proper input range of the ADC. Using the AD9058's internal +2 V reference connected to both ADCs as shown in Figure 48 reduces the number of external components required to create a complete data acquisition system. The 20 Ω resistors in series with ADC input are used to help the AD8001s drive the 10 pF ADC input capacitance. The two AD8001s only add 100 mW to the power consumption while not limiting the performance of the circuit

Layout Considerations

The specified high speed performance of the AD8001 requires careful attention to board layout and component selection. Proper RF design techniques and low parasitic component selection are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

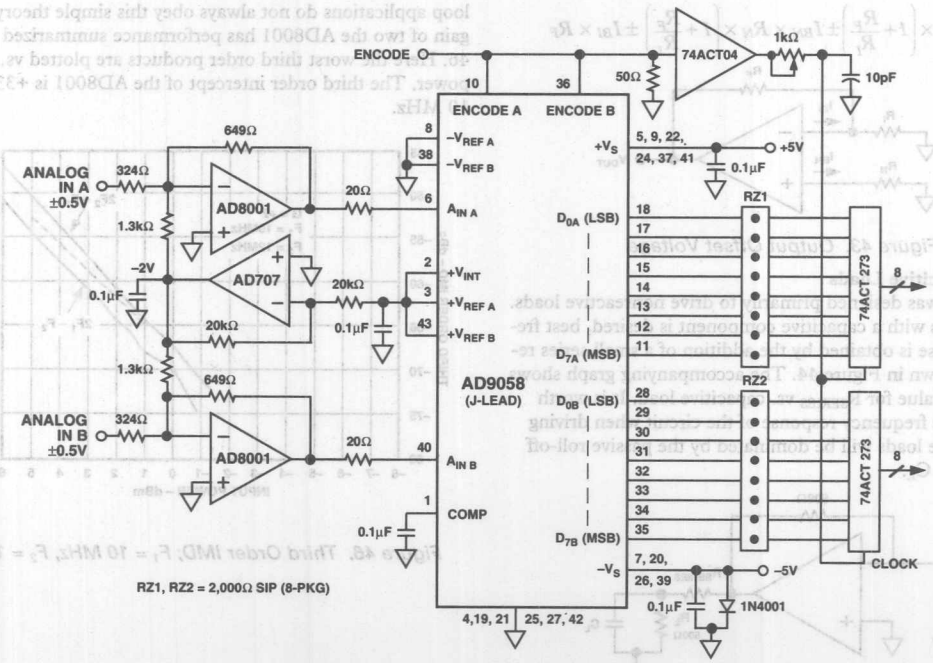


Figure 48. AD8001 Driving a Dual A-to-D Converter

Chip capacitors should be used for supply bypassing (see Figure 49). One end should be connected to the ground plane and the other within 1/8 in. of each power pin. An additional large (4.7 µF–10 µF) tantalum electrolytic capacitor should be connected in parallel, but not necessarily so close, to supply current for fast, large-signal changes at the output.

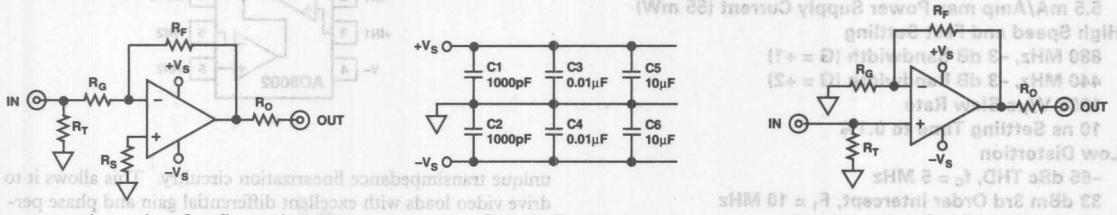
The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than about 1 in.). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

Evaluation Board

An evaluation board for the AD8001 is available that has been carefully laid-out and tested to demonstrate that the specified high speed performance of the device can be realized. For ordering information, please refer to the Ordering Guide.

The layout of the evaluation board can be used as shown or serve as a guide for a board layout.

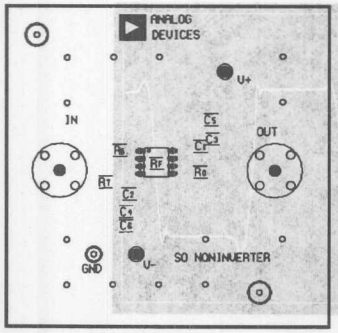


Inverting Configuration *Supply Bypassing* *Noninverting Configuration*

Figure 49. Inverting and Noninverting Configurations for Evaluation Boards

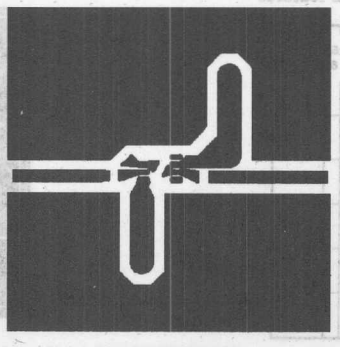
Table I. Recommended Component Values

	AD8001AN (DIP) Gain					AD8001AR (SOIC) Gain				
Component	**–1**	**+1**	**+2**	**+10**	**+100**	**–1**	**+1**	**+2**	**+10**	**+100**
R_F	649 Ω	1050 Ω	750 Ω	470 Ω	1000 Ω	604 Ω	953 Ω	681 Ω	470 Ω	1000 Ω
R_G	649 Ω	–	750 Ω	51 Ω	10Ω	604 Ω	–	681 Ω	51 Ω	10 Ω
R_O (Nominal)	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω
R_S	0 Ω	–	–	–	–	0 Ω	–	–	–	–
R_T (Nominal)	54.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	54.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω
Small Signal BW (MHz)	340	880	460	260	20	370	710	440	260	20
0.1 dB Flatness (MHz)	105	70	105	–	–	130	100	120	–	–



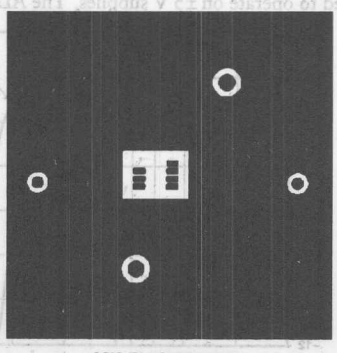
SOIC (R) NONINVERTER

Figure 50. Evaluation Board Silkscreen (Top)



SOIC (R) NONINVERTER

Figure 51. Evaluation Board Layout (Solder Side)



SOIC (R) NONINVERTER

Figure 52. Evaluation Board Layout (Component Side)

FEATURES

Excellent Video Specifications (R_L = 150 Ω, G = +2)
- Gain Flatness 0.1 dB to 100 MHz
- 0.01% Differential Gain Error
- 0.025° Differential Phase Error

Low Power
- 5.5 mA/Amp max Power Supply Current (55 mW)

High Speed and Fast Settling
- 880 MHz, –3 dB Bandwidth (G = +1)
- 440 MHz, –3 dB Bandwidth (G = +2)
- 1200 V/μs Slew Rate
- 10 ns Settling Time to 0.1%

Low Distortion
- –65 dBc THD, f_C = 5 MHz
- 33 dBm 3rd Order Intercept, F_1 = 10 MHz
- –66 dB SFDR, f = 5 MHz
- –60 dB Crosstalk, f = 5 MHz

High Output Drive
- 70 mA Output Current
- Drives Up to 8 Back-Terminated Loads (75 Ω Each) While Maintaining Good Differential Gain/Phase Performance (0.05%/0.25°)

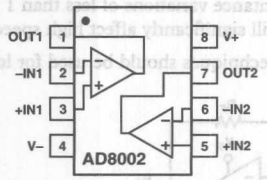
Available in Small 8-Pin PDIP or SOIC

APPLICATIONS

A-to-D Driver
Video Line Driver
Professional Cameras
Video Switchers
Special Effects
RF Receivers

FUNCTIONAL BLOCK DIAGRAM

8-Pin Plastic Mini-DIP and SOIC



PRODUCT DESCRIPTION

The AD8002 is a dual, low power, high speed amplifier designed to operate on ±5 V supplies. The AD8002 features unique transimpedance linearization circuitry. This allows it to drive video loads with excellent differential gain and phase performance on only 50 mW of power per amplifier. The AD8002 is a current feedback amplifier and features gain flatness of 0.1 dB to 100 MHz while offering differential gain and phase error of 0.01% and 0.025°. This makes the AD8002 ideal for professional video electronics such as cameras and video switchers. Additionally, the AD8002's low distortion and fast settling make it ideal for buffer high speed A-to-D converters.

The AD8002 offers low power of 5.5 mA/amplifier max (V_S = ±5 V) and can run on a single +12 V power supply, while being capable of delivering up to 70 mA of load current. All this is offered in a small 8-pin DIP or 8-pin SOIC package. These features make this amplifier ideal for portable and battery powered applications where size and power is critical.

The outstanding bandwidth of 800 MHz along with 1200 V/μs of slew rate make the AD8002 useful in many general purpose high speed applications where dual power supplies of up to ±6 V and single supplies from 6 V to 12 V are needed. The AD8002 is available in the industrial temperature range of –40°C to +85°C.

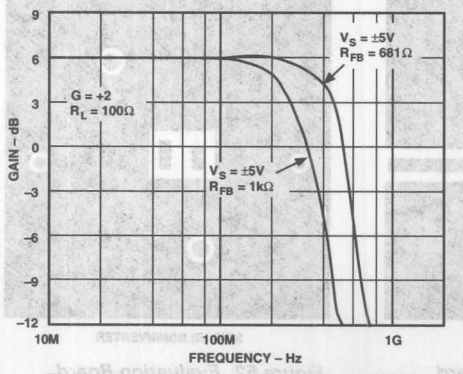


Figure 1. Frequency Response of AD8002

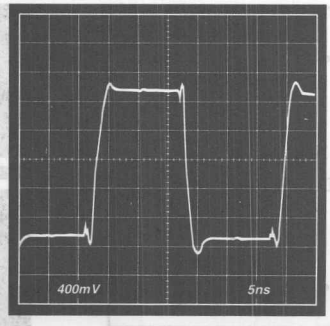


Figure 2. Transient Response of AD8002; 2 V Step, G = +2

PRELIMINARY TECHNICAL DATA

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SPECIFICATIONS (@ T_A = + 25°C, V_S = ±5 V, R_L = 100 Ω, unless otherwise noted)

Model	Conditions	AD8002A Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, N Package	G = +2, < 0.1 dB Peaking, R_F = 681 Ω		440		MHz
	G = +1, < 1 dB Peaking, R_F = 1.2 kΩ		880		MHz
R Package	G = +2, < 0.1 dB Peaking, R_F = 681 Ω		440		MHz
	G = +1, < 0.1 dB Peaking, R_F = 845 Ω		715		MHz
Bandwidth for 0.1 dB Flatness					
N Package	G = +2, R_F = 681 Ω		110		MHz
R Package	G = +2, R_F = 681 Ω		125		MHz
Slew Rate	G = +2, V_O = 2 V Step		1000		V/µs
	G = –1, V_O = 2 V Step		1200		V/µs
Settling Time to 0.1%	G = –1, V_O = 2 V Step		10		ns
Rise & Fall Time	G = –1, V_O = 2 V Step, R_F = 649 Ω		1.4		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p G = +2, R_L = 100 Ω		–65		dBc
Crosstalk	f = 5 MHz		–60		dB
Input Voltage Noise	f = 10 kHz		2.0		nV/√Hz
Input Current Noise	f = 10 kHz, +In		2.0		pA/√Hz
	–In		18		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.01		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.025		Degree
Third Order Intercept	f = 10 MHz		33		dBm
1 dB Gain Compression	f = 10 MHz		14		dBm
SFDR	f = 5 MHz		–66		dB
DC PERFORMANCE					
Input Offset Voltage			2.0	5.5	mV
	T_{MIN}–T_{MAX}		2.0		mV
Offset Drift			10		µV/°C
–Input Bias Current			5.0	25	±µA
	T_{MIN}–T_{MAX}			35	±µA
+Input Bias Current			3.0	6.0	±µA
	T_{MIN}–T_{MAX}			10	±µA
Open Loop Transresistance	V_O = ±2.5 V	250	900		kΩ
	T_{MIN}–T_{MAX}	175			kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		10		MΩ
	–Input		50		Ω
Input Capacitance	+Input		1.5		pF
Input Common-Mode Voltage Range			3.2		±V
Common-Mode Rejection Ratio					
Offset Voltage	V_{CM} = ±2.5 V	50	54		dB
–Input Current	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		0.3	1.0	µA/V
+Input Current	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		0.2	0.7	µA/V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω	2.7	3.1		±V
Output Current[1]	R_L = 37.5 Ω	50	70		mA
Short Circuit Current[1]		85	110		mA
POWER SUPPLY					
Operating Range		±3.0		±6.0	V
Quiescent Current/Both Amplifiers	T_{MIN}–T_{MAX}		10.0	11.0	mA
Power Supply Rejection Ratio	$+V_S$ = +4 V to +6 V, $-V_S$ = –5 V	60	75		dB
	$-V_S$ = – 4 V to –6 V, $+V_S$ = +5 V	50	56		dB
–Input Current	T_{MIN}–T_{MAX}		0.5	2.5	µA/V
+Input Current	T_{MIN}–T_{MAX}		0.1	0.5	µA/V

NOTES

[1]Output current is limited by the maximum power dissipation in the package. See the power derating curves.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... 12.6 V
Internal Power Dissipation[2]
Plastic Package (N) ..... 1.3 Watts
Small Outline Package (R) ..... 0.9 Watts
Input Voltage (Common Mode) ..... $\pm V_S$
Differential Input Voltage ..... ±1.2 V
Output Short Circuit Duration
..... Observe Power Derating Curves
Storage Temperature Range N, R .....–65°C to +125°C
Operating Temperature Range (A Grade) ... –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) ..... +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Pin Plastic Package: θ_{JA} = 90°C/Watt
8-Pin SOIC Package: θ_{JA} = 140°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD8002AN	–40°C to +85°C	8-Pin Plastic DIP
AD8002AR	–40°C to +85°C	8-Pin Plastic SOIC

*For outline information see Package Information section.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8002 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8002 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

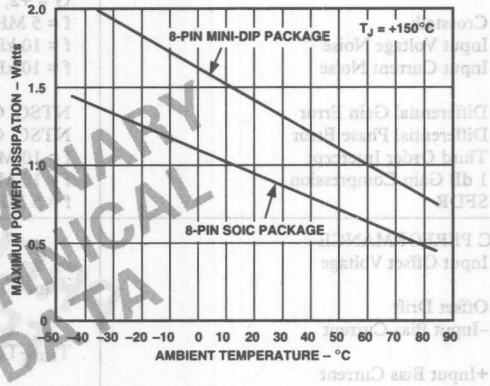

Figure 3. Plot of Maximum Power Dissipation vs. Temperature

PRELIMINARY TECHNICAL DATA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8002 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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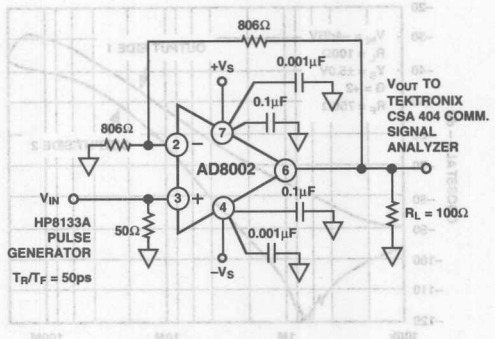

Figure 4. Test Circuit, Gain = +2

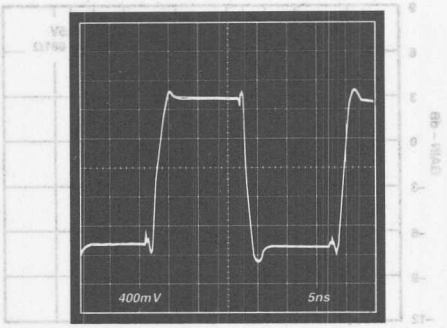

Figure 7. 2 V Step Response, G = +2

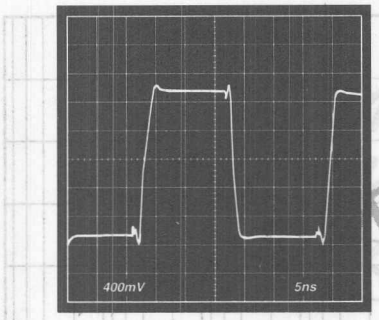

Figure 5. 1 V Step Response, G = +2

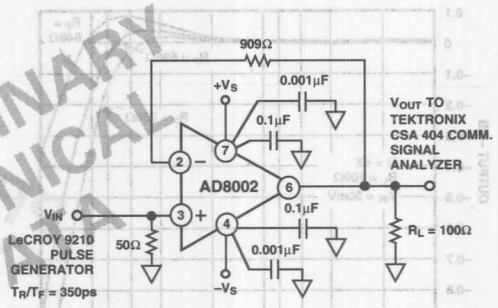

Figure 8. Test Circuit , Gain = +1

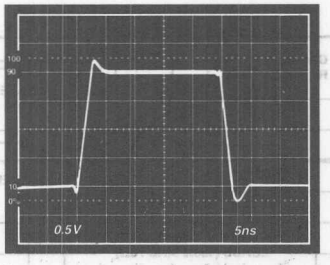

Figure 6. 2 V Step Response, G = +1

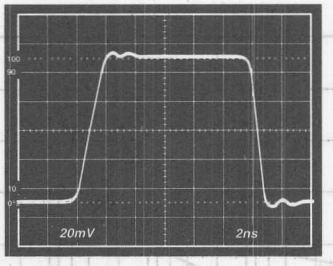

Figure 9. 100 mV Step Response, G = +1

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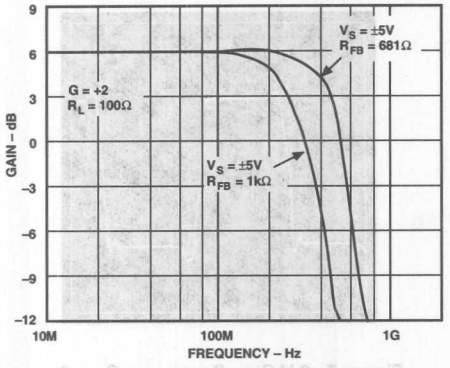

Figure 10. Frequency Response, G = +2

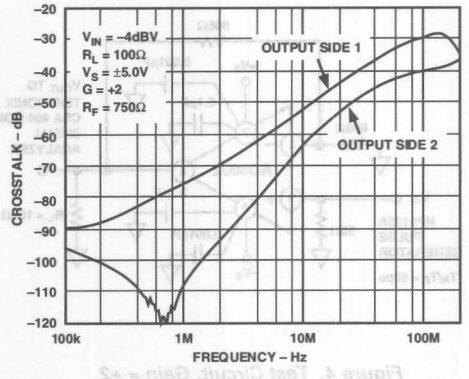

Figure 13. Crosstalk (Output-to-Output) vs. Frequency

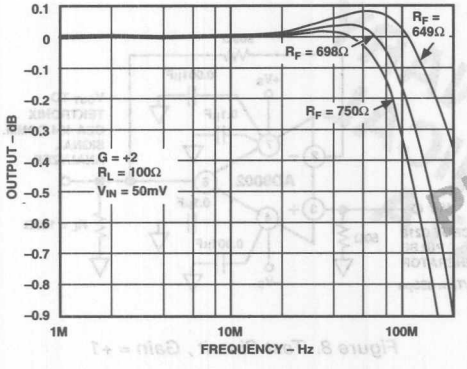

Figure 11. 0.1 dB Flatness, R Package (for N Package Add 50 Ω to R_F)

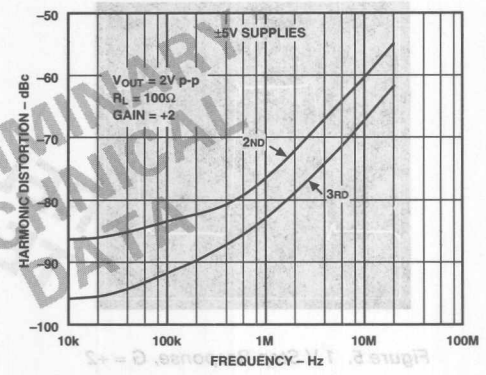

Figure 14. Distortion vs. Frequency, R_L = 100 Ω

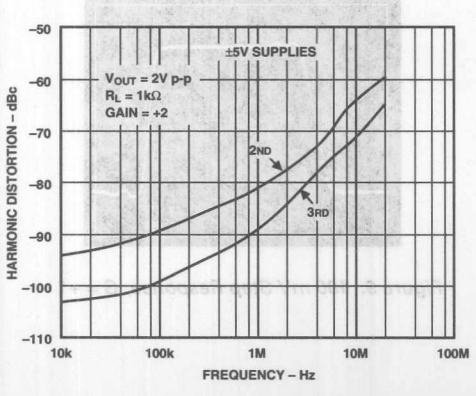

Figure 12. Distortion vs. Frequency, R_L = 1 kΩ

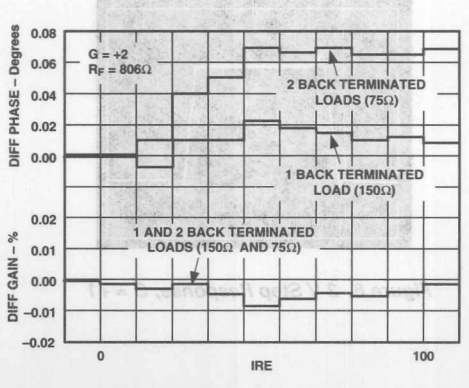

Figure 15. Differential Gain and Differential Phase

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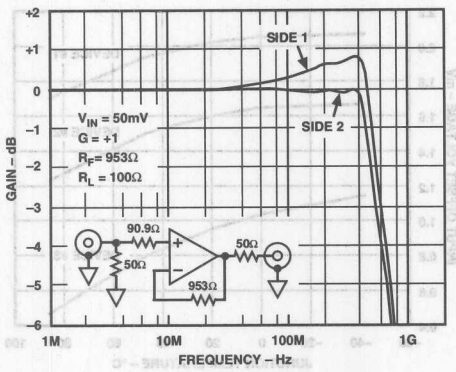

Figure 16. Frequency Response, G = +1

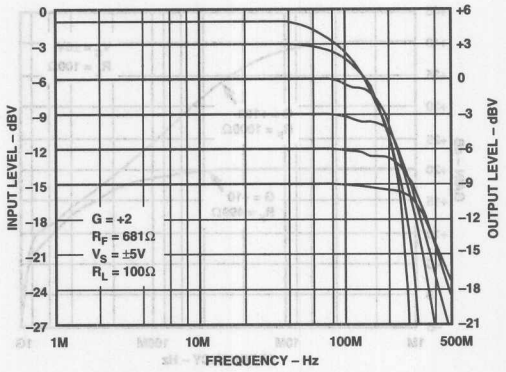

Figure 19. Large Signal Frequency Response, G = +2

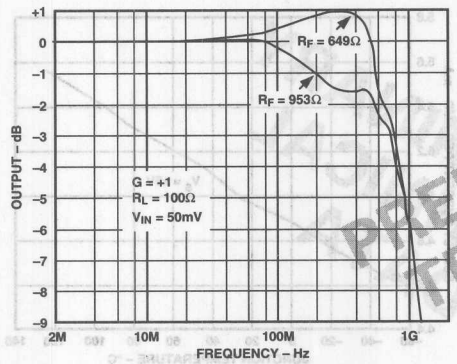

Figure 17. Flatness, R Package, G = +1 (for N Package Add 100 Ω to R_F)

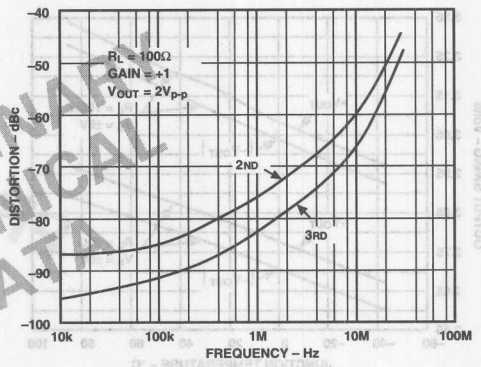

Figure 20. Distortion vs. Frequency, R_L = 100Ω

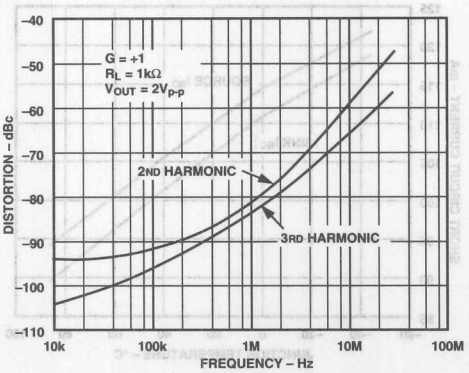

Figure 18. Distortion vs. Frequency, R_L = 1 kΩ

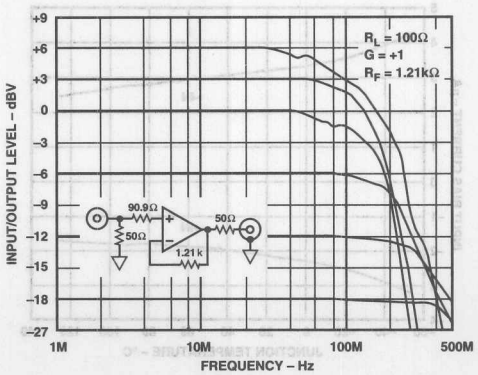

Figure 21. Large Signal Frequency Response, G = +1

PRELIMINARY TECHNICAL DATA

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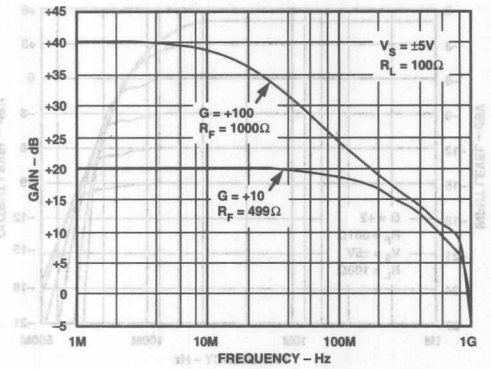

Figure 22. Frequency Response, G = +10, G = +100

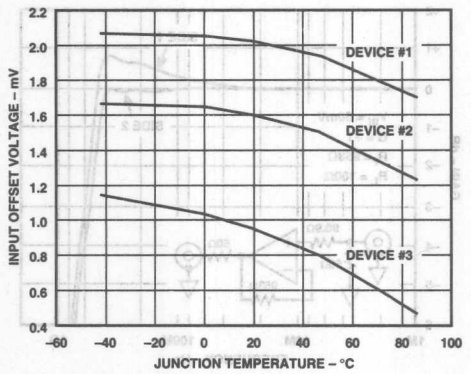

Figure 25. Input Offset vs. Temperature

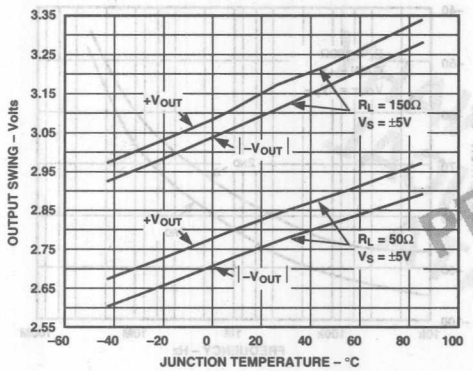

Figure 23. Output Swing vs. Temperature

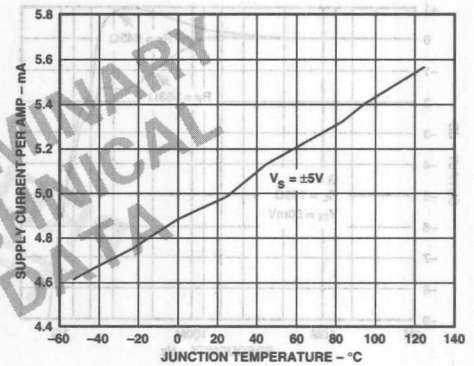

Figure 26. Supply Current vs. Temperature

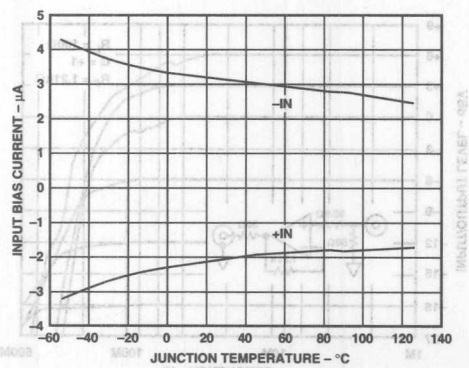

Figure 24. Input Bias Current vs. Temperature

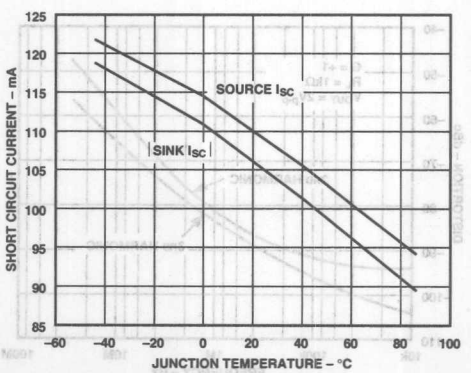

Figure 27. Short Circuit Current vs. Temperature

PRELIMINARY TECHNICAL DATA

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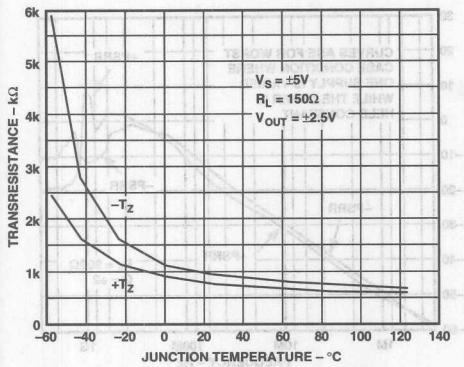

Figure 28. Transresistance vs. Temperature

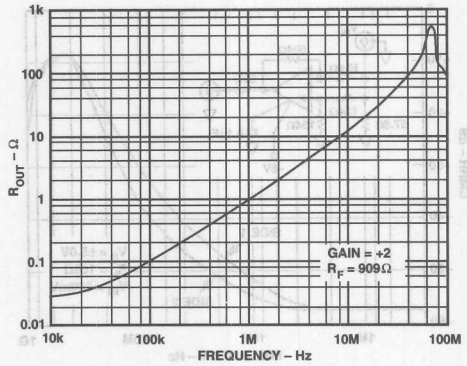

Figure 31. Output Resistance vs. Frequency

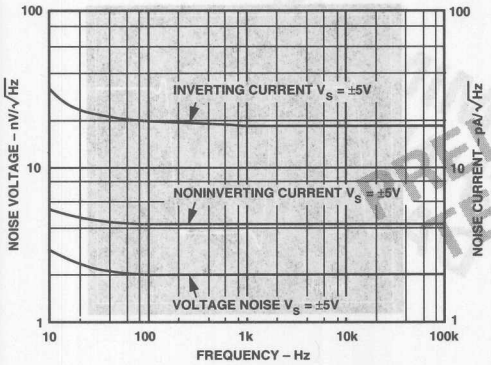

Figure 29. Noise vs. Frequency

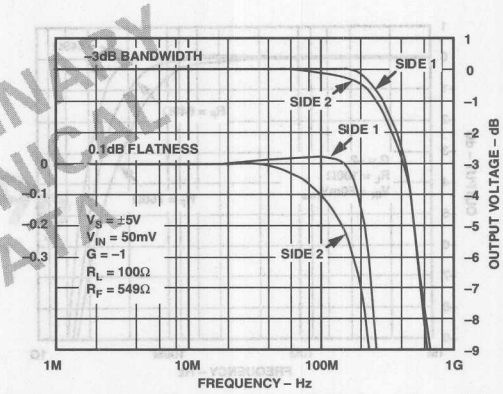

Figure 32. –3 dB Bandwidth vs. Frequency, G = –1

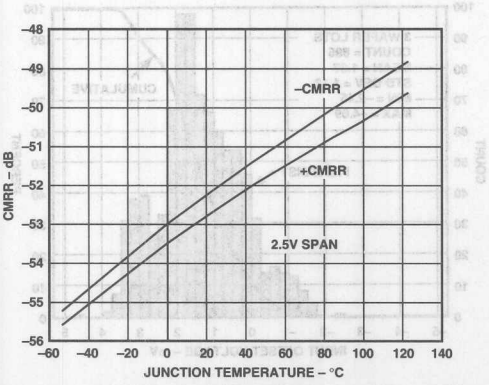

Figure 30. CMRR vs. Temperature

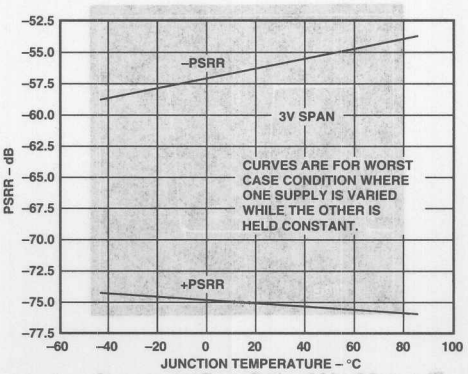

Figure 33. PSRR vs. Temperature

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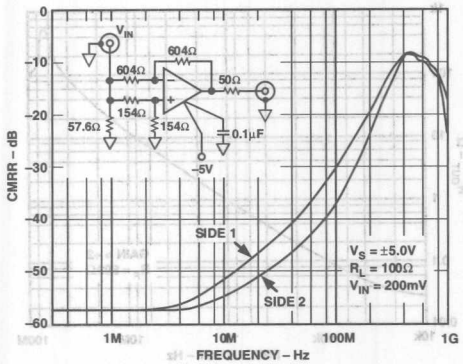

Figure 34. CMRR vs. Frequency

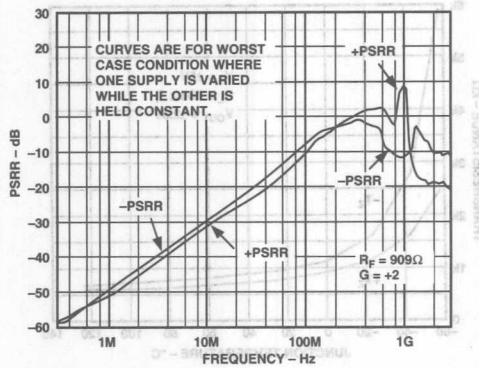

Figure 37. PSRR vs. Frequency

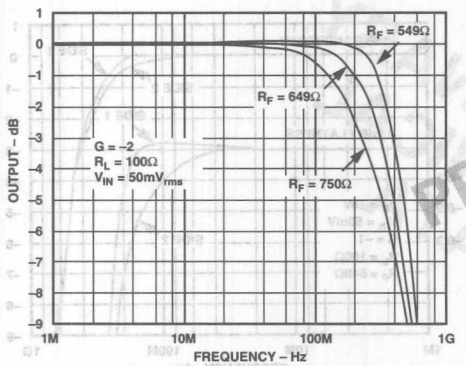

Figure 35. –3 dB Bandwidth vs. Frequency, G = –2

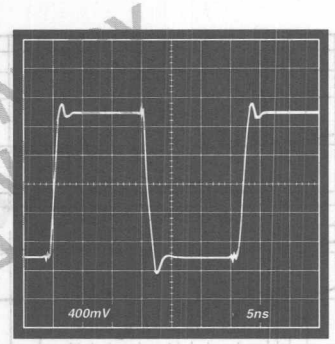

Figure 38. 2 V Step Response, G = –1

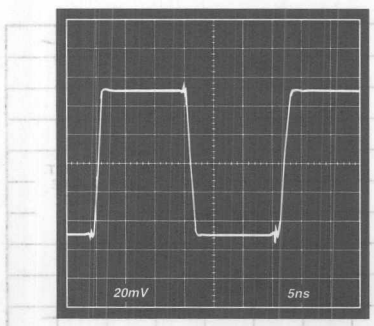

Figure 36. 100 mV Step Response, G = –1

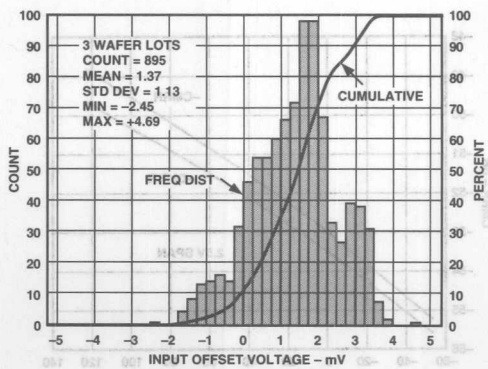

Figure 39. Input Offset Voltage Distribution

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THEORY OF OPERATION

A very simple analysis can put the operation of the AD8002, a current feedback amplifier, in familiar terms. Being a current feedback amplifier, the AD8002's open-loop behavior is expressed as transimpedance, $\Delta V_O/\Delta I_{-IN}$, or T_Z. The open loop transimpedance behaves just as the open loop voltage gain of a voltage feedback amplifier, that is, it has a large dc value and decreases at roughly 6 dB/octave in frequency.

Since the R_{IN} is proportional to $1/g_M$, the equivalent voltage gain is just $T_Z \times g_M$, where the g_M in question is the transconductance of the input stage. This results in a low open loop input impedance at the inverting input, a now familiar result. Using this amplifier as a follower with gain, Figure 40, basic analysis yields the following result.

$$\frac{V_O}{V_{IN}} = G \times \frac{T_Z(S)}{T_Z(S) + G \times R_{IN} + R_1}$$

$$G = 1 + \frac{R_1}{R_2} \qquad R_{IN} = 1/g_M \approx 50\ \Omega$$

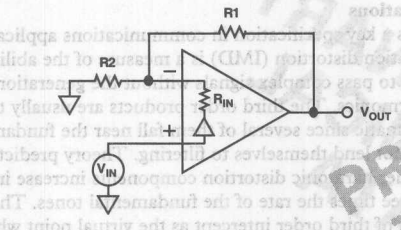

Figure 40.

Recognizing that $G \times R_{IN} << R_1$ for low gains, it can be seen to the first order that bandwidth for this amplifier is independent of gain (G). This simple analysis in conjunction with Figure 41 in fact can predict the behavior of the AD8002 over a wide range of conditions.

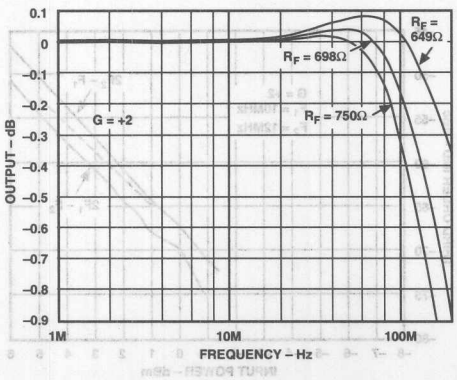

Figure 41. Frequency Response, G = +2

Considering that additional poles contribute excess phase at high frequencies there is a minimum feedback resistance below which peaking or oscillation may result. This fact is used to determine the optimum feedback resistance, R_F. In practice parasitic capacitance at Pin 2 will also add phase in the feedback loop, so picking an optimum value for R_F can be difficult. Figure 42 illustrates this problem. Here the fine scale (0.1 dB/div) flatness is plotted vs. feedback resistance.

Achieving and maintaining gain flatness of better than 0.1 dB at frequencies above 10 MHz requires careful consideration of several issues.

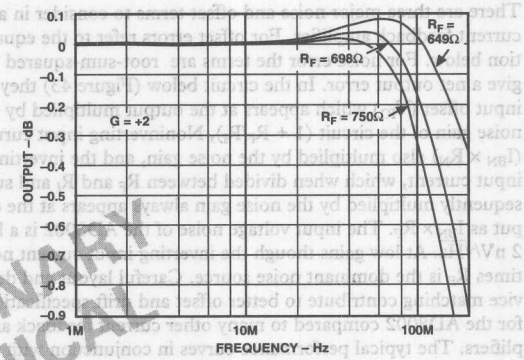

Figure 42. 0.1 dB Flatness vs. Frequency, G = +2

Choice of Feedback and Gain Resistors

Because of the above mentioned relationship between the bandwidth and the feedback resistor, the fine scale gain flatness will, to some extent, vary with feedback resistance. It, therefore, is recommended that once optimum resistor values have been determined, 1% tolerance values should be used if it is desired to maintain flatness over a wide range of production lots. In addition, resistors of different construction have different associated parasitic capacitance and inductance. Surface mount resistors were used for the bulk of the characterization for this data sheet. It is not recommended that leaded components be used with the AD8002.

Printed Circuit Board Layout Considerations

As to be expected for a wideband amplifier, PC board parasitics can affect the overall closed loop performance. Of concern are stray capacitances at the output and the inverting input nodes. If a ground plane is to be used on the same side of the board as the signal traces, a space (5 mm min) should be left around the signal lines to minimize coupling. Additionally, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths on the order of less than 5 mm are recommended. If long runs of coaxial cable are being driven, dispersion and loss must be considered.

PRELIMINARY TECHNICAL DATA

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ing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 µF) will be required to provide the best settling time and lowest distortion. A parallel combination at least 4.7 µF and between 0.1 µF and 0.01 µF is recommended. Some brands of electrolyic capacitors will require a small series damping resistor ≈4.7 Ω for optimum results.

DC Errors and Noise

There are three major noise and offset terms to consider in a current feedback amplifier. For offset errors refer to the equation below. For noise error the terms are root-sum-squared to give a net output error. In the circuit below (Figure 43) they are input offset (V_{IO}) which appears at the output multiplied by the noise gain of the circuit ($1 + R_F/R_I$), Noninverting input current ($I_{BN} \times R_N$) also multiplied by the noise gain, and the inverting input current, which when divided between R_F and R_I and subsequently multiplied by the noise gain always appears at the output as $I_{BN} \times R_F$. The input voltage noise of the AD8002 is a low 2 nV/√Hz. At low gains though the inverting input current noise times R_F is the dominant noise source. Careful layout and device matching contribute to better offset and drift specifications for the AD8002 compared to many other current feedback amplifiers. The typical performance curves in conjunction with the equations below can be used to predict the performance of the AD8002 in any application.

$$V_{OUT} = V_{IO} \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{BN} \times R_N \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{BI} \times R_F$$

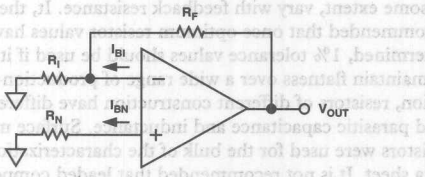

Figure 43. Output Offset Voltage

Driving Capacitive Loads

The AD8002 was designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, best frequency response is obtained by the addition of a small series resistance as shown in Figure 44. The accompanying graph

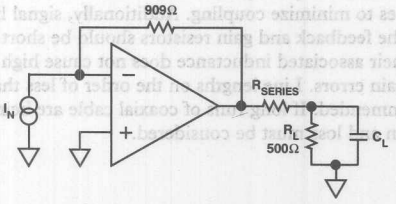

Figure 44. Driving Capacitive Loads

shows the optimum value for R_{SERIES} vs. capacitive load. It is

ron-off of R_{SERIES} and C_L

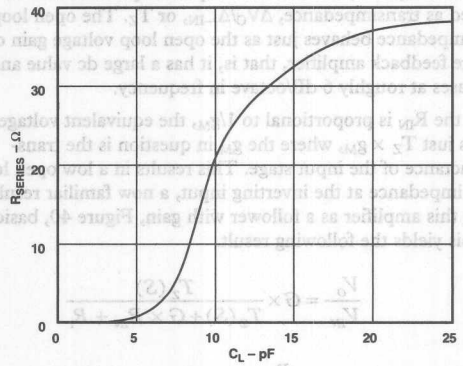

Figure 45. Recommended R_{SERIES} vs. Capacitive Load

Communications

Distortion is a key specification in communications applications. Intermodulation distortion (IMD) is a measure of the ability of an amplifier to pass complex signals without the generation of spurious harmonics. The third order products are usually the most problematic since several of them fall near the fundamentals and do not lend themselves to filtering. Theory predicts that the third order harmonic distortion components increase in power at three times the rate of the fundamental tones. The specification of third order intercept as the virtual point where fundamental and harmonic power are equal is one standard measure of distortion performance. Op amps used in closed-loop applications do not always obey this simple theory. At a gain of two, the AD8002 has performance summarized in Figure 46. Here the worst third order products are plotted vs. input power. The third order intercept of the AD8002 is +33 dBm at 10 MHz.

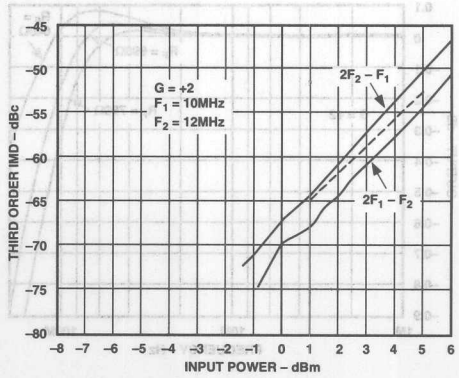

Figure 46. Third Order IMD; F_1 = 10 MHz, F_2 = 12 MHz

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Operation as a Video Line Driver

The AD8002 has been designed to offer outstanding performance as a video line driver. The important specifications of differential gain (0.01%) and differential phase (0.025°) meet the most exacting HDTV demands for driving one video load with each amplifier. The AD8002 also drives up to four back terminated loads, as shown in Figure 47, with equally impressive performance. Another important consideration is isolation between loads in a multiple load application. The AD8002 has more than 40 dB of isolation at 5 MHz when driving two 75 Ω back terminated loads.

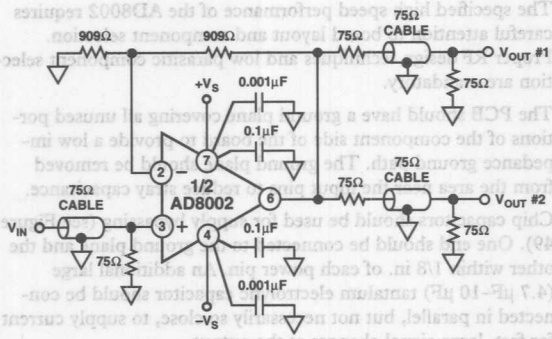

Figure 47. Video Line Driver

Driving A-to-D Converters

The AD8002 is well suited for driving high speed analog-to-digital converters such as the AD9058. The AD9058 is a dual 8-bit 50 Msps ADC. In the circuit below the AD8002 is shown driving the inputs of the AD9058 which are configured for 0 V to +2 V ranges. Bipolar input signals are buffered, amplified (–2×), and offset (by +1.0 V) into the proper input range of the ADC. Using the AD9058's internal +2 V reference connected to both ADCs as shown in Figure 48 reduces the number of external components required to create a complete data acquisition system. The 20 Ω resistors in series with ADC inputs are used to help the AD8002s drive the 10 pF ADC input capacitance. The two AD8002s only add 100 mW to the power consumption while not limiting the performance of the circuit.

PRELIMINARY TECHNICAL DATA

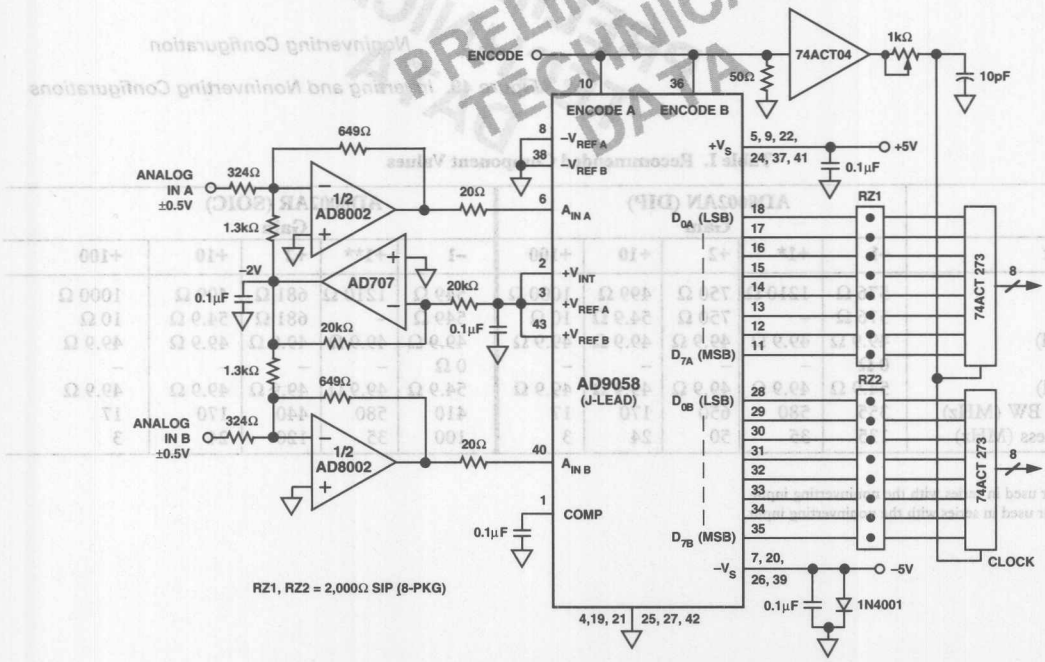

Figure 48. AD8002 Driving a Dual A-to-D Converter

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Layout Considerations

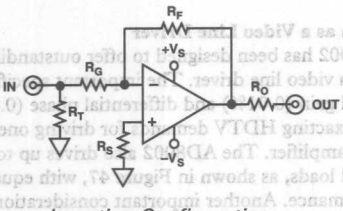
The specified high speed performance of the AD8002 requires careful attention to board layout and component selection. Proper RF design techniques and low parasitic component selection are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

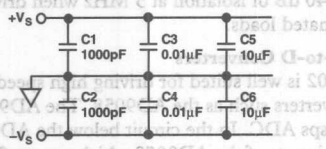
Chip capacitors should be used for supply bypassing (see Figure 49). One end should be connected to the ground plane and the other within 1/8 in. of each power pin. An additional large (4.7 µF–10 µF) tantalum electrolytic capacitor should be connected in parallel, but not necessarily so close, to supply current for fast, large-signal changes at the output.

The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

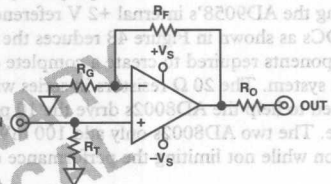
Stripline design techniques should be used for long signal traces (greater than about 1 in.). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.



Inverting Configuration



Supply Bypassing



Noninverting Configuration

Figure 49. Inverting and Noninverting Configurations

Table I. Recommended Component Values

	AD8002AN (DIP) Gain					AD8002AR (SOIC) Gain				
Component	**–1**	**+1***	**+2**	**+10**	**+100**	**–1**	**+1****	**+2**	**+10**	**+100**
R_F	576 Ω	1210 Ω	750 Ω	499 Ω	1000 Ω	549 Ω	1210 Ω	681 Ω	499 Ω	1000 Ω
R_G	576 Ω	–	750 Ω	54.9 Ω	10 Ω	549 Ω	–	681 Ω	54.9 Ω	10 Ω
R_O (Nominal)	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω
R_S	0 Ω	–	–	–	–	0 Ω	–	–	–	–
R_T (Nominal)	54.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	54.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω
Small Signal BW (MHz)	355	580	650	170	17	410	580	440	170	17
0.1 dB Flatness (MHz)	135	35	50	24	3	100	35	120	24	3

NOTES
*100 Ω resistor used in series with the noninverting input.
**90.9 Ω resistor used in series with the noninverting input.

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Quad 3000 V/μs, 35 mW Current Feedback Amplifier

AD8004

FEATURES

High Speed
- 400 MHz –3 dB Bandwidth (G = +1)
- 3000 V/μs Slew Rate
- 10 ns Settling Time to 0.1%
- 0.9 ns Rise Time for 2 V Step

Low Power
- 3.5 mA/Amp Power Supply Current (35 mW/Amp)

Single Supply Operation
- Fully Specified for +5 V Supply

Great Video Specifications (R_L = 150 Ω, G = +2)
- Gain Flatness 0.1 dB to 30 MHz
- 0.05% Differential Gain Error
- 0.05° Differential Phase Error

Low Distortion
- –65 dBc THD at 10 MHz
- 33 dBm Third Order Intercept, f = 10 MHz
- –65 dB SFDR, f = 20 MHz

High Output Current of 50 mA

Available in a Small 14-Pin PDIP and SOIC

APPLICATIONS

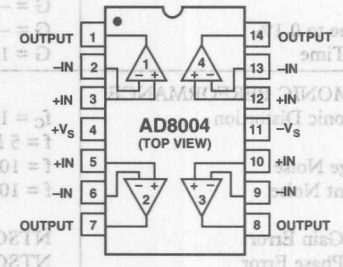
Image Scanners

Active Filters

Video Switchers

Special Effects

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

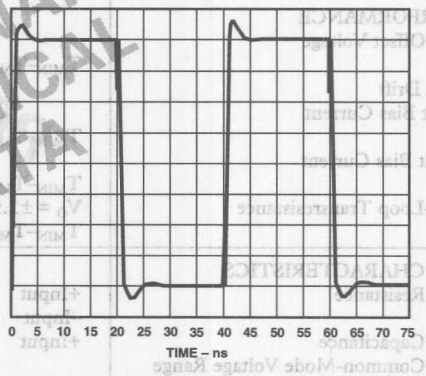


Figure 1. 4 V Step Response of AD8004

PRODUCT DESCRIPTION

The AD8004 is a quad, low power, high speed amplifier designed to operate on +5 V or ±5 V supplies. It utilizes a current feedback architecture and features high slew rate of 3000 V/μs making the AD8004 ideal for handling large amplitude pulses. Additionally, the AD8004 provides gain flatness of 0.1 dB to 30 MHz while offering differential gain and phase error of 0.05% and 0.05°. This makes the AD8004 suitable for professional video electronics such as cameras and video switchers.

The AD8004 offers low power of 3.5 mA/amplifier and can run on a single +5 V or +12 V power supply, while being capable of delivering up to 50 mA of load current. All this is offered in a small 14-pin DIP or 14-pin SOIC package. These features make this amplifier ideal for portable and battery powered applications where size and power is critical.

The outstanding bandwidth of 400 MHz along with 3000 V/μs of slew rate make the AD8004 useful in many general purpose high speed applications where dual power supplies of up to ±6 V and single supplies from 5 V to 12 V are needed. The AD8004 is available in the industrial temperature range of –40°C to +85°C.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

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Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +2, < 0.1 dB Peaking		250		MHz
	G = +1		400		MHz
Bandwidth for 0.1 dB Flatness	G = +2		30		MHz
Slew Rate	G = +2		3000		V/µs
	G = –1		TBD		V/µs
Settling Time to 0.1%	G = –1, V_O = 2 V Step		10		ns
Rise & Fall Time	G = 1, V_O = 2 V Step		0.9		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 10 MHz, V_O = 2 V p-p		–65		dBc
Crosstalk	f = 5 MHz		–60		dB
Input Voltage Noise	f = 10 kHz		3.0		nV/√Hz
Input Current Noise	f = 10 kHz, +In		2.0		pA/√Hz
	–In		18		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.05		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.05		Degree
Third Order Intercept	f = 10 MHz		33		dBm
SFDR	f = 20 MHz		–65		dB
1 dB Gain Compression	f = 10 MHz		16		dBm
DC PERFORMANCE					
Input Offset Voltage			5.0	15	mV
	T_{MIN}–T_{MAX}		TBD	TBD	mV
Offset Drift			30		µV/°C
–Input Bias Current			5.0	25	±µA
	T_{MIN}–T_{MAX}			TBD	±µA
+Input Bias Current			5.0	15	±µA
	T_{MIN}–T_{MAX}			TBD	±µA
Open-Loop Transresistance	V_O = ±2.5 V		300		kΩ
	T_{MIN}–T_{MAX}		TBD		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		2		MΩ
	–Input		50		Ω
Input Capacitance	+Input		1.5		pF
Input Common-Mode Voltage Range			3.2		±V
Common-Mode Rejection Ratio					
Offset Voltage	V_{CM} = ±2.5 V	50	54		dB
–Input Current	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		TBD	TBD	µA/V
+Input Current	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		TBD	TBD	µA/V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω		1.1 to 3.9		±V
Output Current			50		mA
Short Circuit Current			TBD		mA
POWER SUPPLY					
Operating Range		±2.5		±6.0	V
Quiescent Current	T_{MIN}–T_{MAX}		3.5		mA
Power Supply Rejection Ratio	V_S = ±1.75 V to ±6 V		60		dB
–Input Current	T_{MIN}–T_{MAX}		TBD	TBD	µA/V
+Input Current	T_{MIN}–T_{MAX}		TBD	TBD	µA/V

Specifications subject to change without notice.

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($@T_A$ = +25°C, V_S = +5 V, R_L = 100 Ω, R_F = 500 Ω unless otherwise noted)

Parameter	Conditions	AD8004A Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +2, < 0.1 dB Peaking		250		MHz
	G = +1		400		MHz
Bandwidth for 0.1 dB Flatness	G = +2		30		MHz
Slew Rate	G = +2		3000		V/µs
	G = –1		TBD		V/µs
Settling Time to 0.1%	G = –1, V_O = 2 V Step		10		ns
Rise & Fall Time	G = 1, V_O = 2 V Step		0.9		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 10 MHz, V_O = 2 V p-p		–65		dBc
Crosstalk	f = 5 MHz		–60		dB
Input Voltage Noise	f = 10 kHz		3.0		nV/√Hz
Input Current Noise	f = 10 kHz, +In		2.0		pA/√Hz
	–In		18		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.07		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.07		Degree
Third Order Intercept	f = 10 MHz		33		dBm
SFDR	f = 20 MHz		–65		dB
1 dB Gain Compression	f = 10 MHz		14		dBm
DC PERFORMANCE					
Input Offset Voltage			5.0	15	mV
	T_{MIN}–T_{MAX}		TBD	TBD	mV
Offset Drift			30		µV/°C
–Input Bias Current			5.0	25	±µA
	T_{MIN}–T_{MAX}			TBD	±µA
+Input Bias Current			5.0	15	±µA
	T_{MIN}–T_{MAX}			TBD	±µA
Open Loop Transresistance	V_O = +1 V to +3.9 V		300		kΩ
	T_{MIN}–T_{MAX}		TBD		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		2		MΩ
	–Input		50		Ω
Input Capacitance	+Input		1.5		pF
Input Common-Mode Voltage Range			3.2		V
Common-Mode Rejection Ratio					
Offset Voltage	V_{CM} = +1 V to +3 V	50	54		dB
–Input Current	V_{CM} = +1 V to +3 V, T_{MIN}–T_{MAX}		TBD	TBD	µA/V
+Input Current	V_{CM} = +1 V to +3 V, T_{MIN}–T_{MAX}		TBD	TBD	µA/V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_C = 150 Ω		1.1 to 3.9		V
Output Current			50		mA
Short Circuit Current			TBD		mA
POWER SUPPLY					
Operating Range		0, +5		+12	V
Quiescent Current	T_{MIN}–T_{MAX}		3.5		mA
Power Supply Rejection Ratio	V_S = +3.5 V to +12 V		60		dB
–Input Current	T_{MIN}–T_{MAX}		TBD	TBD	µA/V
+Input Current	T_{MIN}–T_{MAX}		TBD	TBD	µA/V

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Internal Power Dissipation[2]
Plastic Package (N) . . . . . 1.6 Watts
Small Outline Package (R) . . . . . 1.0 Watts
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±1.2 V
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range (N, R) . . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
14-Pin plastic DIP package: θ_{JA} = 75°C/W
14-pin SOIC package: θ_{JA} = 120°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD8004AN	–40°C to +85°C	14-Pin Plastic DIP	N-14
AD8004AR	–40°C to +85°C	14-Pin Plastic SOIC	R-14

*For outline information see Package Information section.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8004 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8004 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curve below.

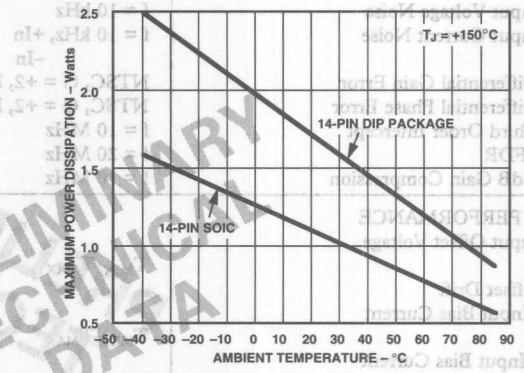


Figure 2. Maximum Power Dissipation vs. Ambient Temperature

PRELIMINARY TECHNICAL DATA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8004 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Low Distortion, Wide Bandwidth Voltage Feedback Clamp Amps

AD8036/AD8037

FEATURES

Superb Clamping Characteristics
- <25 mV Clamp Accuracy
- 3 ns Overdrive Recovery
- Minimized Nonlinear Clamping Region

Wide Bandwidth — AD8036 / AD8037
- Small Signal — 350 MHz / 240 MHz
- Large Signal (4 V p-p) — 200 MHz / 150 MHz

Good DC Characteristics
- 2 mV Offset
- 10 μV/°C Drift

Ultralow Distortion, Low Noise
- –90 dBc typ @ 5 MHz
- –64 dBc typ @ 20 MHz
- 5.6 nV/√Hz Spectral Noise Density

High Speed
- Slew Rate 1600 V/μs
- Settling 11 ns to 0.1%, 16 ns to 0.01%

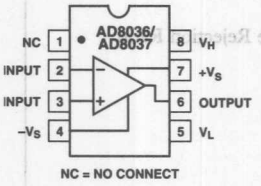
±3 V to ± 5 V Supply Operation

APPLICATIONS

- ADC Buffer
- IF/RF Signal Processing
- High Quality Imaging
- Broadcast Video Systems
- Video Amplifier

FUNCTIONAL BLOCK DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q), and SO (R) Packages



NC = NO CONNECT

PRELIMINARY TECHNICAL DATA

9

PRODUCT DESCRIPTION

The AD8036 and AD8037 are very high speed and wide bandwidth input clamping amplifiers. The AD8036 is unity-gain stable. The AD8037 is stable at a gain of two. Utilizing proprietary input clamping architecture, the AD8036 and AD8037 offer unparalleled clamp amp performance. Also, utilizing a voltage feedback architecture, their exceptional settling time, bandwidth, and low distortion performance meet the requirements of many applications that previously depended on current feedback amplifiers. Their classical op amp structure works much more predictably in many designs. This product can be used as a classical op amp or a clamp amp where a high and low output voltage is specified.

A proprietary design architecture has produced an amplifier that combines many of the best characteristics of both current feedback and voltage feedback amplifiers. The AD8036 and AD8037 exhibit exceptionally fast and accurate pulse response (16 ns to 0.01%) as well as extremely wide small signal and large signal bandwidth and ultralow distortion. The AD8036 achieves –68 dBc at 20 MHz with 350 MHz small signal and 200 MHz large signal bandwidths. The AD8036 and AD8037's clamp accuracy is 25 mV or less and it recovers from overdrive within 2 ns.

These characteristics position the AD8036/AD8037 ideally for driving as well as buffering flash and high resolution ADCs. Additionally, nonlinear functions with high speed and wide bandwidth are made possible by the balanced high impedance inputs of the voltage feedback architecture.

The AD8036 is offered in industrial (–40°C to +85°C) and military (–55°C to +125°C) temperature ranges and the AD8037 in industrial. Industrial versions are available in plastic DIP and SOIC; MIL versions are packaged in cerdip.

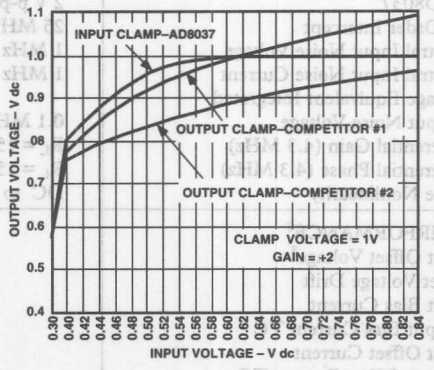


Figure 1. Clamp Accuracy

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	Conditions	Temp.	Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
Bandwidth (–3 dB)						
Small Signal AD8036	$V_{OUT} \leq 0.4$ V p-p	Full		350		MHz
AD8037	$V_{OUT} \leq 0.4$ V p-p	Full		240		MHz
Large Signal AD8036	$V_{OUT} = 4$ V p-p	Full		200		MHz
AD8037	$V_{OUT} = 4$ V p-p	Full		150		MHz
Amplitude of Peaking	Full Spectrum	Full		0.1		dB
Flatness	40 MHz	Full		0.1		dB
Common-Mode Rejection Ratio	@ 20 MHz	+25°C		+28		dB
Slew Rate	$V_{OUT} = 4$ V Step	Full		1600		V/µs
Rise/Fall Time	$V_{OUT} = 0.5$ V Step	+25°C		1.5		ns
	$V_{OUT} = 4$ V Step	Full		3.6		ns
Overshoot	$V_{OUT} = 2$ V Step	Full		0		%
Settling Time						
To 0.1%	$V_{OUT} = 2$ V Step	+25°C		11		ns
To 0.01%	$V_{OUT} = 2$ V Step	Full		16		ns
To 0.1%	$V_{OUT} = 4$ V Step	+25°C				ns
To 0.02%	$V_{OUT} = 4$ V Step	+25°C				ns
CLAMP PERFORMANCE						
Clamp Voltage Range	V_H or V_L	Full	±3.3	±3.5		V
Clamp Accuracy	2× Overdrive	Full		±25	±50	mV
Clamp Nonlinearity Range[1]	2× Overdrive	Full				
Bias Current (V_H or V_L)		+25°C		50	100	µA
Clamp Input Bandwidth (–3 dB)	V_H or V_L = 2 V p-p	Full	100	250		MHz
Clamp Overshoot	2× Overdrive	+25°C		4	5	%
Overdrive Recovery	2× Overdrive	+25°C		1	10	ns
HARMONIC/NOISE PERFORMANCE						
2nd Harmonic Distortion						
AD8036	2 V p-p; 20 MHz	Full		–68		dBc
AD8037	2 V p-p; 20 MHz	Full		–60		dBc
3rd Harmonic Distortion						
AD8036	2 V p-p; 20 MHz	Full		–77		dBc
AD8037	2 V p-p; 20 MHz	Full		–70		dBc
3rd Order Intercept	25 MHz	Full		+40		dBm
Spectral Input Noise Voltage	1 MHz to 200 MHz	+25°C		5.6		nV/√Hz
Spectral Input Noise Current	1 MHz to 200 MHz	+25°C		3.6		pA/√Hz
Average Equivalent Integrated Input Noise Voltage	0.1 MHz to 200 MHz	+25°C		80		µV rms
Differential Gain (4.3 MHz)	$R_L = 150\ \Omega$	+25°C		0.01	0.05	%
Differential Phase (4.3 MHz)	$R_L = 150\ \Omega$	+25°C		0.01	0.05	Degrees
Phase Nonlinearity	DC to 100 MHz	+25°C		1.1		Degrees
DC PERFORMANCE[2]						
Input Offset Voltage[3]		+25°C		±2		mV
Offset Voltage Drift		Full		±10		µV/°C
Input Bias Current		+25°C		7		µA
Input Bias Current TC		Full		35		nA/°C
Input Offset Current		+25°C		3		µA
Input Offset Current TC		Full		2.5		nA/°C
Common-Mode Rejection Ratio	$\Delta V_{CM} = 1$ V	+25°C		60		dB
Open Loop Gain	$V_{OUT} = \pm 2$ V p-p	+25°C		56		dB

PRELIMINARY TECHNICAL DATA

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Parameter	Conditions	Temp.	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Input Resistance		+25°C		500		kΩ
Input Capacitance		+25°C		1.2		pF
Common-Mode Input Range		Full		±3.4		V
OUTPUT CHARACTERISTICS						
Output Voltage Range		Full		±3.4		V
Output Current		Full		70		mA
Output Resistance		+25°C		0.3		Ω
POWER SUPPLY						
Supply Voltage ($\pm V_S$)		Full	3.0	5.0	5.5	V
Quiescent Current		Full		17	20	mA
Power Supply Rejection Ratio		+25°C		66		dB

NOTES
[1]Nonlinearity is defined as signal distortion as the output approaches the clamping levels.
[2]Measured at $A_V = 20$.
[3]Measured with respect to the inverting input.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±6.5 V
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 6 V
Continuous Output Current[2] . . . . . 90 mA
Operating Temperature Ranges
AN, AR . . . . . –40°C to +85°C
SQ/883B . . . . . –55°C to +125°C
Storage Temperature (Ceramic) . . . . . –65°C to +150°C
Storage Temperature (Plastic) . . . . . –65°C to +125°C
Junction Temperature (Ceramic)[3] . . . . . +175°C
Junction Temperature (Plastic)[3] . . . . . +150°C
Lead Soldering Temperature (1 Minute)[4] . . . . . +220°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Output is short-circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.
[3]Typical thermal impedances (part soldered onto board; no air flow):
Ceramic DIP: $\theta_{JA} = 110°C/W$; $\theta_{JC} = 20°C/W$
Plastic SOIC: $\theta_{JA} = 150°C/W$; $\theta_{JC} = 30°C/W$
Plastic DIP: $\theta_{JA} = 140°C/W$; $\theta_{JC} = 30°C/W$.
[4]Temperature shown is for surface mount devices, mounted by vapor phase soldering. Through-hole devices (ceramic and plastic DIPs) can be soldered at +300°C for 10 seconds.

PRELIMINARY TECHNICAL DATA

9

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD8036AN	–40°C to +85°C	Plastic DIP	N-8
AD8036AR	–40°C to +85°C	SOIC	R-8
AD8036SQ/883B	–55°C to +125°C	Cerdip	Q-8
AD8036-EB		Evaluation Board	
AD8037AN	–40°C to +85°C	Plastic DIP	N-8
AD8037AR	–40°C to +85°C	SOIC	R-8

*N = Plastic DIP; Q = Cerdip; R = SOIC (Small Outline Integrated Circuit.) For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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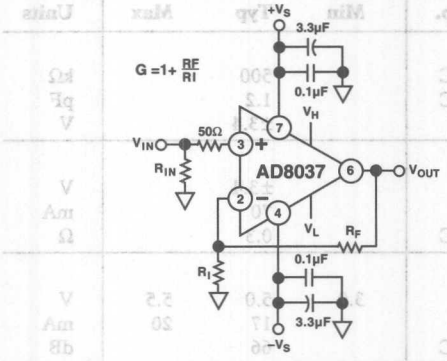

Figure 2. Noninverting Operation

Clamp Operation

The AD8036/AD8037 have built-in input clamps that can be used to protect sensitive devices connected to the amplifier output. Clamp operation can only be performed in the noninverting configuration. By utilizing input clamps, the maximum linear range is achieved in conjunction with the highest clamp accuracy.

The clamp voltages (high and low) are connected to pins V_{HIGH} (input) and V_{LOW} (input) accordingly. These are high *impedance* nodes with minimal current drawn. These input clamp voltages multiplied by the amplifier gain sets the limited output swing range. V_H (output) = V_H (input) × A_V and V_L (output) = V_L (input) × A_V. The chart on the cover page shows the characteristics of the AD8036/AD8037 in clamped operation versus competitors who use output clamping techniques. The improved accuracy and hard clamping characteristics of the AD8036/AD8037 allow clamps to be used in applications where output clamps cannot be used. Also, the recovery from overdrive will be 1 ns typical.

The proprietary input clamp architecture has also been designed to minimize signal distortion as you approach the clamp voltages. This characteristic is fundamental to the signal integrity in the clamp region and allows for maximum useful amplifier range. Figure 3 shows the distortion of the AD8037 as you approach a high clamp voltage value of 1 V versus the competitors.

In addition, the clamp voltage range is only limited by the output voltage range (±3.4 V), and the clamp voltages can be set to any value between the ±3.4 V swing. Of course, the clamps can be set beyond the output voltage swing, but then the output will not be limited by the clamp voltages, but by the swing range. Output clamps typically have limited clamp voltage settings and cannot be set to any voltage between $\pm V_{CC}$. For example, it is typical that a low clamp voltage can be set only as high as +2 V, and the high clamp voltage as low as –2 V. This can be a limiting feature in many applications.

The AD8036/AD8037 have been designed with internal ties from the clamp voltage pins to $\pm V_{CC}$, and if the clamp pins are left floating, the low clamp voltage (V_L) will be set to $-V_{CC}$ and the high clamp voltage (V_H) will be set to $+V_{CC}$. In this configuration, the AD8036/AD8037 will perform as a standard operational amplifier and will not clamp the output.

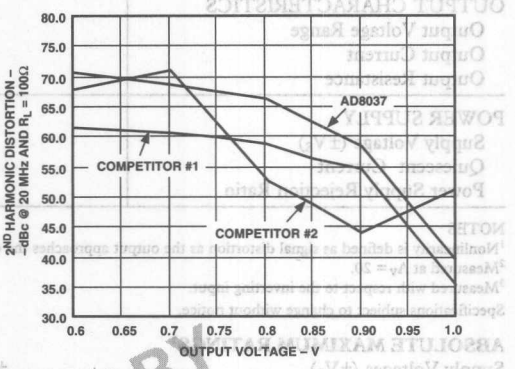

Figure 3. Distortion Near Clamp Values

Layout Considerations

The specified high speed performance of the AD8036/AD8037 requires careful attention to board layout and component selection. Proper RF design techniques and low-pass parasitic component selection are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path. The ground plane should be removed from the area near the input pins to reduce the stray capacitance.

Chip capacitors should be used for the supply bypassing (see Figure 2). One end should be connected to the ground plane and the other within 1/8 inch of each power pin. An additional large (0.47 µF–10 µF) tantalum electrolytic capacitor should be connected in parallel, but not necessarily so close, to supply current for fast, large signal changes at the output.

The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

Evaluation Board

An evaluation board for the AD8036 is available that has been carefully laid-out and tested to demonstrate that the specified high speed performance of the device can be realized. For ordering information, please refer to the ordering guide.

The layout of the evaluation board can be used as shown or serve as a guide for a board layout.

PRELIMINARY TECHNICAL DATA

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Table I.

Component	AD8036AN (DIP) Gain –1	+1	+2	+10	+100	AD8036AR (SOIC) Gain –1	+1	+2	+10	+100
R_F	270 Ω	140 Ω	270 Ω	470 Ω	100 Ω	320 Ω	190 Ω	320 Ω	470 Ω	100 Ω
R_G	270 Ω		270 Ω	51 Ω	10 Ω	320 Ω		320 Ω	51 Ω	10 Ω
R_O (Nominal)	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	100 Ω	100 Ω	100 Ω	49.9 Ω	49.9 Ω
R_S	100 Ω	130 Ω	100 Ω	100 Ω	100 Ω	150 Ω	180 Ω	150 Ω	100 Ω	100 Ω
R_T (Nominal)	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	100 Ω	100 Ω	100 Ω	49.9 Ω	49.9 Ω

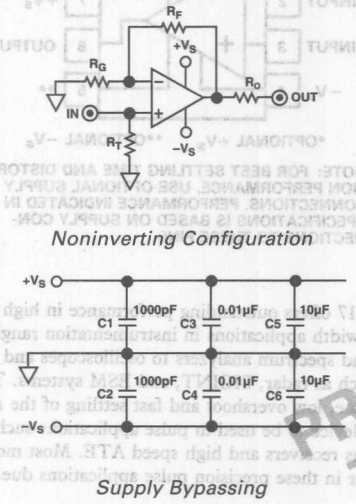

Figure 4. Noninverting Configuration for Evaluation Boards

A Diodeless, High Speed, Full-Wave Rectifier

A high speed, full-wave rectifier (or absolute-value amplifier) circuit using high speed, clamping amplifiers is shown in Figure 5. This circuit topology provides both speed and performance enhancements over the traditional diode-based topologies that contain diodes in the amplifier feedback path. These diode-based topologies have performance limitations at both lower signal input levels and higher bandwidths. One limitation is due to the increase in dynamic resistance of the diode that reduces the amount of feedback at lower signal levels. Another limitation is due to the reduction of the amplifier's open-loop gain at higher frequencies which is required to over come the forward-bias voltage drop of the diode. These limitations are most visible at the zero crossings of the input signal when the diodes must change states.

This circuit in Figure 5 consists of three high speed, clamping amplifiers (U1–U3: AD8037) along with 1% metal-film resistors used for gain control and input bias current compensation. The high speed, clamp accuracy and large signal bandwidth of the AD8037 make this application feasible. They can accurately clamp the input signal within 5 ns to a user defined level. Since the internal clamping circuitry of these amplifiers is located within their input stages, these amplifiers can clamp only in the noninverting mode. In this circuit, only U2 is configured as a clamping amplifier while U1 and U3 function as a buffer and difference amplifier, respectively.

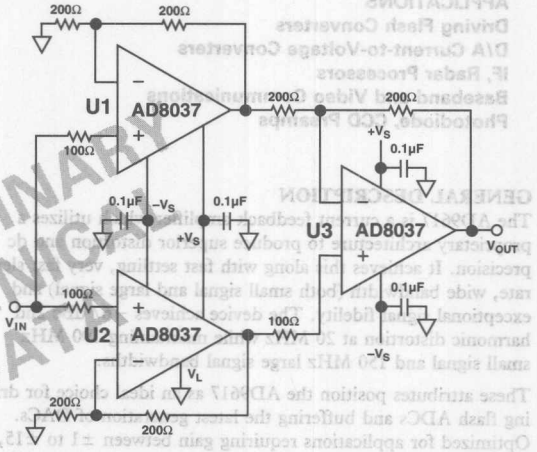

Figure 5.

The circuit is configured for positive full-wave rectification by configuring U2 as a gain-of-two, positive half-wave rectifier. This is accomplished by setting the positive clamping threshold level (Pin 8 of U2) to the positive supply (hence, outside the input voltage range of the amplifiers input) and the negative clamping threshold level (Pin 5 of U2) to ground. For negative full-wave rectification, U2 must be configured as a gain-of-two, negative half-wave rectifier by setting the positive clamping threshold level to ground and the negative clamping threshold level to the negative supply. U1 is simply configured as a gain of two buffer and is required to buffer the input signal source, V_{IN}, from the dynamic input impedance presented by U3 as well as match the signal delay of U2. U3 subtracts the output of the half-wave rectifier (U2) from the buffer output (U1) to produce the desired gain-of-two full-wave rectification. An optional trim network consisting of a potentiometer can be used to trim out any clamping offset error of U2. Precision 1% resistors for the gain controlling elements of U1 and U2 will typically maintain under 2% gain accuracy while values under 250 Ω will not degrade the phase margin of these high speed amplifiers.

PRELIMINARY TECHNICAL DATA

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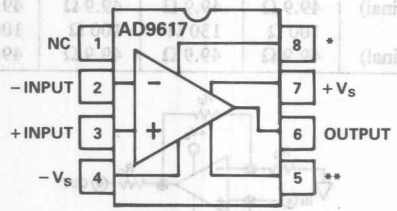
FEATURES

Usable Closed-Loop Gain Range: ±1 to ±40
Low Distortion: −67 dBc (2nd) at 20 MHz
Small Signal Bandwidth: 190 MHz (A_V = +3)
Large Signal Bandwidth: 150 MHz at 4 V p-p
Settling Time: 10 ns to 0.1%; 14 ns to 0.02%
Overdrive and Output Short Circuit Protected
Fast Overdrive Recovery
DC Nonlinearity 10 ppm

APPLICATIONS

Driving Flash Converters
D/A Current-to-Voltage Converters
IF, Radar Processors
Baseband and Video Communications
Photodiode, CCD Preamps

PIN CONFIGURATION



*OPTIONAL $+V_S$ **OPTIONAL $-V_S$

NOTE: FOR BEST SETTLING TIME AND DISTORTION PERFORMANCE, USE OPTIONAL SUPPLY CONNECTIONS. PERFORMANCE INDICATED IN SPECIFICATIONS IS BASED ON SUPPLY CONNECTIONS TO THESE PINS.

GENERAL DESCRIPTION

The AD9617 is a current feedback amplifier which utilizes a proprietary architecture to produce superior distortion and dc precision. It achieves this along with fast settling, very fast slew rate, wide bandwidth (both small signal and large signal) and exceptional signal fidelity. The device achieves −67 dBc 2nd harmonic distortion at 20 MHz while maintaining 190 MHz small signal and 150 MHz large signal bandwidths.

These attributes position the AD9617 as an ideal choice for driving flash ADCs and buffering the latest generation of DACs. Optimized for applications requiring gain between ±1 to ±15, the AD9617 is unity gain stable without external compensation.

Additional benefits of the AD9617B and T grades include input offset voltage of 500 μV and temperature coefficient (TC) of 3 μV/°C. These accuracy performance levels make the AD9617 an excellent choice for driving emerging high resolution (12–16 bits), high speed analog-to-digital converters and flash converters.

***Patent pending.**

The AD9617 offers outstanding performance in high fidelity, wide bandwidth applications in instrumentation ranging from network and spectrum analyzers to oscilloscopes and in military systems such as radar, SIGINT, and ESM systems. The superior slew rate, low overshoot and fast settling of the AD9617 allow the device to be used in pulse applications such as communications receivers and high speed ATE. Most monolithic op amps suffer in these precision pulse applications due to slew rate limiting.

The AD9617J operates over the range of 0 to +70°C and is available in either an 8-pin plastic mini-DIP or an 8-lead plastic small outline package (SOIC). The AD9617A and B versions are rated over the industrial temperature range of −40°C to +85°C. The AD9617S and T versions are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±7 V
Common Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 3 V
Continuous Output Current[2] . . . . . 70 mA
Operating Temperature Ranges
AD9617JN/JR . . . . . 0 to +70°C
AD9617AQ/BQ . . . . . −40°C to +85°C
AD9617SQ/TQ . . . . . −55°C to +125°C
Storage Temperature
AD9617JN/JR . . . . . −65°C to +125°C
AD9617AQ/BQ/SQ/TQ . . . . . −65°C to +150°C
Junction Temperature[3]
AD9617JN/JR . . . . . +150°C
AD9617AQ/BQ/SQ/TQ . . . . . +175°C
Lead Soldering Temperature (10 Seconds) . . . . . +300°C

DC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $A_V = +3$; $\pm V_S = \pm 5$ V; $R_F = 400\ \Omega$; $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9617JN/JR Min	AD9617JN/JR Typ	AD9617JN/JR Max	AD9617AQ/SQ Min	AD9617AQ/SQ Typ	AD9617AQ/SQ Max	AD9617BQ/TQ Min	AD9617BQ/TQ Typ	AD9617BQ/TQ Max	Units
Input Offset Voltage[4, 5]		+25°C	I	−1.1	+0.5	+2.2	−1.1	+0.5	+2.2	+0.0	+0.5	+1.1	mV
Input Offset Voltage TC[5]		Full	IV	−4	+3	+25	−4	+3	+25	−4	+3	+25	µV/°C
Input Bias Current[5]													
Inverting		+25°C	I	−50	0	+50	−50	0	+50	−25	0	+25	µA
Noninverting		+25°C	I	−25	+5	+35	−25	+5	+35	−15	+5	+20	µA
Input Bias Current TC[5]													
Noninverting		Full	IV	−50	+30	+125	−50	+30	+125	−50	+30	+125	nA/°C
Inverting		Full	IV	−50	+50	+150	−50	+50	+150	−50	+50	+150	nA/°C
Input Resistance													
Noninverting		+25°C	V		60			60			60		kΩ
Input Capacitance													
Noninverting		+25°C	V		1.5			1.5			1.5		pF
Common-Mode Input Range[6]	$T = T_{max}$	←	II	±1.4	±1.5		±1.4	±1.5		±1.4	±1.5		V
	$T = T_{min}$ to +25°C	←	II	±1.7	±1.8		±1.7	±1.8		±1.7	±1.8		V
Common-Mode Rejection Ratio[7]	$T = T_{max}$	←	II	44	48		44	48		44	48		dB
	$T = T_{min}$ to +25°C	←	II	50	53		50	53		50	53		dB
Power Supply Rejection Ratio	$\Delta V_S = \pm 5\%$	Full	II	50	60		50	60		50	60		dB
Open Loop Gain													
T_O	At dc	+25°C	V		500			500			500		kΩ
Nonlinearity	At dc	+25°C	IV		10			10			10		ppm
Output Voltage Range		+25°C	II	±3.4	±3.8		±3.4	±3.8		±3.4	±3.8		V
Output Impedance	At dc	+25°C	V		0.07			0.07			0.07		Ω
Output Current (50 Ω Load)	$T = +25°C$ to T_{max}	←	II	60			60			60			mA
	$T = T_{min}$	←	II	50			50			50			mA

AC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $A_V = +3$; $\pm V_S = \pm 5$ V; $R_F = 400\ \Omega$; $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9617JN/JR Min	AD9617JN/JR Typ	AD9617JN/JR Max	AD9617AQ/SQ Min	AD9617AQ/SQ Typ	AD9617AQ/SQ Max	AD9617BQ/TQ Min	AD9617BQ/TQ Typ	AD9617BQ/TQ Max	Units
FREQUENCY DOMAIN													
Bandwidth (−3 dB)													
Small Signal	$V_{OUT} \leq 2$ V p-p	Full	II	145	190		145	190		145	190		MHz
Large Signal	$V_{OUT} = 4$ V p-p	Full	IV		150		115	150		115	150		MHz
Bandwidth Variation vs. A_V	$A_V = -1$ to ±15	+25°C	V		40			40			40		MHz
Amplitude of Peaking (<50 MHz)	$T = T_{min}$ to +25°C	←	II		0			0	0.3		0	0.3	dB
	$T = T_{max}$	←	II		0			0	0.6		0	0.6	dB
Amplitude of Peaking (>50 MHz)	$T = T_{min}$ to +25°C	←	II		0			0	0.8		0	0.8	dB
	$T = T_{max}$	←	II		0			0	1.0		0	1.0	dB
Amplitude of Roll-Off (<75 MHz)		Full	II		0.1			0.1	0.6		0.1	0.6	dB
Phase Nonlinearity	dc to 75 MHz	+25°C	V		0.5			0.5			0.5		Degree
2nd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV		−86	−78		−86	−78		−86	−78	dBc
	2 V p-p; 20 MHz	Full	IV		−67	−59		−67	−59		−67	−59	dBc
	2 V p-p; 60 MHz	Full	II		−51	−43		−51	−43		−51	−43	dBc
3rd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV		−83	−75		−83	−75		−83	−75	dBc
	2 V p-p; 20 MHz	Full	IV		−69	−61		−69	−61		−69	−61	dBc
	2 V p-p; 60 MHz	Full	II		−54	−46		−54	−46		−54	−46	dBc
Input Noise Voltage	10 MHz	+25°C	V		1.2			1.2			1.2		nV/√(Hz)
Inverting Input Noise Current	10 MHz	+25°C	V		29			29			29		pA/√(Hz)
Average Equivalent Integrated Input Noise Voltage	0.1 to 200 MHz	+25°C	V		55			55			55		µV, rms

Parameter	Conditions	Temp	Test Level	AD9617JN/JR Min	Typ	Max	AD9617AQ/SQ Min	Typ	Max	AD9617BQ/TQ Min	Typ	Max	Units
TIME DOMAIN													
Slew Rate	V_{OUT} = 4 V Step	Full	IV		1400		1100	1400		1100	1400		V/μs
Rise/Fall Time													
V_{OUT} = 2 V Step		Full	IV		2.0			2.0	2.5		2.0	2.5	ns
V_{OUT} = 4 V Step	T = +25°C to T_{max}	←	IV		2.4			2.4	3.3		2.4	3.3	ns
V_{OUT} = 4 V Step	T = T_{min}	←	IV		2.4			2.4	3.5		2.4	3.5	ns
Overshoot	V_{OUT} = 2 V Step	Full	IV		3			3	14		3	14	%
Settling Time													
To 0.1%	V_{OUT} = 2 V Step	Full	IV		10			10	15		10	15	ns
To 0.02%	V_{OUT} = 2 V Step	Full	IV		14			14	23		14	23	ns
To 0.1%	V_{OUT} = 4 V Step	Full	IV		11			11	16		11	16	ns
To 0.02%	V_{OUT} = 4 V Step	Full	IV		16			16	24		16	24	ns
2×Overdrive Recovery to ±2 mV of Final Value	V_{IN} = 1.7 V Step	+25°C	V		50			50			50		ns
Propagation Delay		+25°C	V		2			2			2		ns
Differential Gain[8]		Full	V		<0.01			<0.01			<0.01		%
Differential Phase[8]		Full	V		0.01			0.01			0.01		Degree
POWER SUPPLY REQUIREMENTS													
Quiescent Current													
$+I_S$		Full	II		34	48		34	48		34	48	mA
$-I_S$		Full	II		34	48		34	48		34	48	mA

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Output is short circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.

[3]Typical thermal impedances (part soldered onto board):
Mini-DIP: θ_{JA} = 140°C/W; θ_{JC} = 30°C/W. Side Brazed/Cerdip: θ_{JA} = 110°C/W; θ_{JC} = 20°C/W. SOIC Package: θ_{JA} = 150°C/W; θ_{JC} = 30°C/W.

[4]Measured with respect to the inverting input.

[5]Typical is defined as the mean of the distribution.

[6]Measured in voltage follower configuration.

[7]Measured with V_{IN} = ±0.25 V.

[8]Frequency = 4.3 MHz; R_L = 150 Ω; A_V = +3.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C and sample tested at specified temperatures. AC testing of J grade devices done on sample basis.

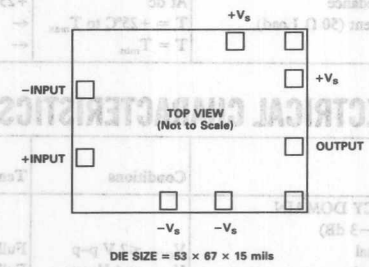
III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

Die Connections



DIE SIZE = 53 × 67 × 15 mils

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9617JN	0 to +70°C	Plastic DIP	N-8
AD9617JR	0 to +70°C	SOIC	R-8
AD9617AQ	−40°C to +85°C	Cerdip	Q-8
AD9617BQ	−40°C to +85°C	Cerdip	Q-8
AD9617SQ	−55°C to +125°C	Cerdip	Q-8
AD9617TQ	−55°C to +125°C	Cerdip	Q-8

*For outline information see Package Information section.

ANALOG DEVICES

Low Distortion, Precision, Wide Bandwidth Op Amp

AD9618*

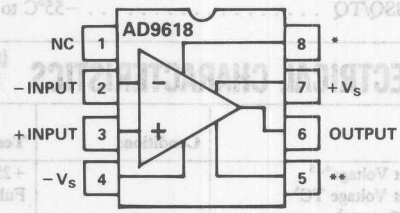
FEATURES

Usable Closed-Loop Gain Range: +5/−1 to ±100
Low Distortion: −63 dBc (2nd) at 20 MHz
Small Signal Bandwidth: 160 MHz (A_V = +10)
Large Signal Bandwidth: 150 MHz at 5 V p–p
Settling Time: 10 ns to 0.1%; 14 ns to 0.02%
Overdrive and Output Short Circuit Protected
Fast Overdrive Recovery
DC Nonlinearity 5 ppm

APPLICATIONS

Driving Flash Converters
D/A Current to Voltage Converters
IF, Radar Processors
Baseband and Video Communications
Photodiode, CCD Preamps

PIN CONFIGURATION



*OPTIONAL $+V_S$ **OPTIONAL $-V_S$

NOTE: FOR BEST SETTLING TIME AND DISTORTION PERFORMANCE, USE OPTIONAL SUPPLY CONNECTIONS. PERFORMANCE INDICATED IN SPECIFICATIONS IS BASED ON SUPPLY CONNECTIONS TO THESE PINS.

9

GENERAL DESCRIPTION

The AD9618 is a current feedback amplifier which utilizes a proprietary architecture to produce superior distortion and dc precision. It achieves this along with fast settling, very fast slew rate, wide bandwidth (both small signal and large signal), and exceptional signal fidelity. The device achieves −63 dBc 2nd harmonic distortion at 20 MHz while maintaining 160 MHz small signal and 150 MHz large signal bandwidths.

These attributes position the AD9618 as an ideal choice for driving flash ADCs and buffering the latest generation of DACs. Optimized for applications requiring gain between +5/−1 to ±40, the AD9618 is unity gain stable without external compensation.

Additional benefits of the AD9618B and T grades include input offset voltage of 500 μV and temperature coefficient (TC) of 3 μV/°C. These accuracy performance levels make the AD9618 an excellent choice for driving emerging high resolution (12–16 bits), high speed analog to digital converters and flash converters.

The AD9618 offers outstanding performance in high fidelity, wide bandwidth applications in instrumentation ranging from network and spectrum analyzers to oscilloscopes, and in military systems such as radar, SIGINT, and ESM systems. The superior slew rate, low overshoot, and fast settling of the AD9618 allow the device to be used in pulse applications such as communications receivers and high speed ATE. Most monolithic op amps suffer in these precision pulse applications due to slew rate limiting.

*Patent pending.

The AD9618J operates over the range of 0 to +70°C and is available in either an 8-pin plastic mini-DIP or an 8 lead plastic small outline package (SOIC). The AD9618A and B versions are rated over the industrial temperature range of −40°C to +85°C. The AD9618S and T versions are rated over the military temperature range of −55°C to +125°C; and are available processed to MIL-STD-883B.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9618—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±7 V
Common Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 3 V
Continuous Output Current[2] . . . . . 70 mA
Operating Temperature Ranges
AD9618JN/JR . . . . . 0 to +70°C
AD9618AQ/BQ . . . . . −40°C to +85°C
AD9618SQ/TQ . . . . . −55°C to +125°C
Storage Temperature
AD9618JN/JR . . . . . −65°C to +125°C
AD9618AQ/BQ/SQ/TQ . . . . . −65°C to +150°C
Junction Temperature[3]
AD9618JN/JR . . . . . 150°C
AD9618AQ/BQ/SQ/TQ . . . . . 175°C
Lead Soldering Temperature (10 Seconds) . . . . . +300°C

DC ELECTRICAL CHARACTERISTICS

(unless otherwise noted, $A_V = +10$; $\pm V_S = \pm 5$ V; $R_F = 1000\ \Omega$; $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9618JN/JR Min	AD9618JN/JR Typ	AD9618JN/JR Max	AD9618AQ/SQ Min	AD9618AQ/SQ Typ	AD9618AQ/SQ Max	AD9618BQ/TQ Min	AD9618BQ/TQ Typ	AD9618BQ/TQ Max	Units
Input Offset Voltage[4, 5]		+25°C	I	−1.1	+0.5	+2.2	−1.1	+0.5	+2.2	0.0	+0.5	+1.1	mV
Input Offset Voltage TC[5]		Full	IV	−4	+3	+25	−4	+3	+25	−4	+3	+25	µV/°C
Input Bias Current[5]													
Inverting		+25°C	I	−45	0	+45	−45	0	+45	−20	0	+20	µA
Noninverting		+25°C	I	−25	+5	+35	−25	+5	+35	−13	+5	+18	µA
Input Bias Current TC[5]													
Noninverting		Full	IV	−50	+30	+125	−50	+30	+125	−50	+30	+125	nA/°C
Inverting		Full	IV	−50	+40	+130	−50	+40	+130	−50	+40	+130	nA/°C
Input Resistance													
Noninverting		+25°C	V		75			75			75		kΩ
Input Capacitance													
Noninverting		+25°C	V		1.5			1.5			1.5		pF
Common Mode Input Range[6]	$T = T_{max}$	←	II	±1.0	±1.2		±1.0	±1.2		±1.0	±1.2		V
	$T = T_{min}$ to +25°C	←	II	±1.4	±1.5		±1.4	±1.5		±1.4	±1.5		V
Common Mode Rejection Ratio[7]	$T = T_{max}$	←	II	44	48		44	48		44	48		dB
	T = +25°C	←	II	48	52		48	52		48	52		dB
	$T = T_{min}$	←	II	50	54		50	54		50	54		dB
Power Supply Rejection Ratio	$\Delta V_S = \pm 5\%$	Full	II	50	60		50	60		50	60		dB
Open Loop Gain													
T_O	At dc	+25°C	V		3			3			3		MΩ
Nonlinearity	At dc	+25°C	V		5			5			5		ppm
Output Voltage Range		+25°C	II	±3.3	±3.7		±3.3	±3.7		±3.3	±3.7		V
Output Impedance	At dc	+25°C	V		0.08			0.08			0.08		Ω
Output Current (50 Ω Load)	$T = +25°C$ to T_{max}	←	II	60			60			60			mA
	$T = T_{min}$	←	II	50			50			50			mA

AC ELECTRICAL CHARACTERISTICS

(unless otherwise noted, $A_V = +10$; $\pm V_S = \pm 5$ V; $R_F = 1$ kΩ; $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9618JN/JR Min	AD9618JN/JR Typ	AD9618JN/JR Max	AD9618AQ/SQ Min	AD9618AQ/SQ Typ	AD9618AQ/SQ Max	AD9618BQ/TQ Min	AD9618BQ/TQ Typ	AD9618BQ/TQ Max	Units
FREQUENCY DOMAIN													
Bandwidth (−3 dB)													
Small Signal	$V_{OUT} \le 2$ V p–p	Full	II	130	160		130	160		130	160		MHz
Large Signal	$V_{OUT} \le 5$ V p–p	Full	IV		150		120	150		120	150		MHz
Bandwidth Variation vs. A_V	$A_V = -1$ to ±40	+25°C	V		35			35			35		MHz
Amplitude of Peaking (<50 MHz)	$T = T_{min}$ to +25°C	←	II		0			0	0.4		0	0.4	dB
	$T = T_{max}$	←	II		0			0	0.7		0	0.7	dB
Amplitude of Peaking (>50 MHz)	$T = T_{min}$ to +25°C	←	II		0			0	0.6		0	0.6	dB
	$T = T_{max}$	←	II		0			0	1.2		0	1.2	dB
Amplitude of Roll-Off (<75 MHz)		Full	II		0.5			0.5	1.2		0.5	1.2	dB
Phase Nonlinearity	dc to 75 MHz	+25°C	V		0.5			0.5			0.5		Degree
2nd Harmonic Distortion	2 V p–p; 4.3 MHz	Full	IV		−83	−75		−83	−75		−83	−75	dBc
	2 V p–p; 20 MHz	Full	IV		−63	−55		−63	−55		−63	−55	dBc
	2 V p–p; 60 MHz	Full	II		−51	−43		−51	−43		−51	−43	dBc
3rd Harmonic Distortion	2 V p–p; 4.3 MHz	Full	IV		−85	−77		−85	−77		−85	−77	dBc
	2 V p–p; 20 MHz	Full	IV		−70	−62		−70	−62		−70	−62	dBc
	2 V p–p; 60 MHz	Full	II		−62	−54		−62	−54		−62	−54	dBc
Input Noise Voltage	10 MHz	+25°C	V		1.2			1.2			1.2		nV/√(Hz)
Inverting Input Noise Current	10 MHz	+25°C	V		24			24			24		pA/√(Hz)

Parameter	Conditions	Temp	Test Level	AD9618JN/JR Min	Typ	Max	AD9618AQ/SQ Min	Typ	Max	AD9618BQ/TQ Min	Typ	Max	Units
Average Equivalent Integrated Input Noise Voltage	0.1 to 200 MHz	+25°C	V		38			38			38		μV, rms
TIME DOMAIN													
Slew Rate	V_{OUT} = 4 V Step	Full	IV		1800		1400	1800		1400	1800		V/μs
Rise/Fall Time													
V_{OUT} = 2 V Step		Full	IV		2.2			2.2	2.6		2.2	2.6	ns
V_{OUT} = 5 V Step	T = +25°C to	←	IV		2.3			2.3	2.8		2.3	2.8	ns
	$T = T_{min}$	←	IV		2.3			2.3	3.1		2.3	3.1	ns
Overshoot	V_{OUT} = 2 V Step	Full	IV		2			2	10		2	10	%
Settling Time													
To 0.1%	V_{OUT} = 2 V Step	Full	IV		9			9	15		9	15	ns
To 0.02%	V_{OUT} = 2 V Step	Full	IV		14			14	23		14	23	ns
To 0.1%	V_{OUT} = 4 V Step	Full	IV		10			10	16		10	16	ns
To 0.02%	V_{OUT} = 4 V Step	Full	IV		16			16	24		16	24	ns
2×Overdrive Recovery to ±2 mV of Final Value	V_{IN} = 0.6 V Step	+25°C	V		50			50			50		ns
Propagation Delay		+25°C	V		2			2			2		ns
Differential Gain[8]		Full	V		0.01			0.01			0.01		%
Differential Phase[8]		Full	V		0.02			0.02			0.02		Degree
POWER SUPPLY REQUIREMENTS													
Quiescent Current													
$+I_S$		Full	II		31	43		31	43		31	43	mA
$-I_S$		Full	II		31	43		31	43		31	43	mA

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Output is short circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.

[3]Typical thermal impedances (part soldered onto board):
Mini-DIP: θ_{JA} = 140°C/W; θ_{JC} = 30°C/W.
Side Brazed/Cerdip: θ_{JA} = 110°C/W; θ_{JC} = 20°C/W.
SOIC Package: θ_{JA} = 150°C/W; θ_{JC} = 30°C/W.

[4]Measured with respect to the inverting input.

[5]Typical is defined as the mean of the distribution.

[6]Measured in voltage follower configuration.

[7]Measured with V_{IN} = ±0.25 V.

[8]Frequency = 4.3 MHz; R_L = 150 Ω; A_V = +10.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C and sample tested at specified temperatures. AC testing of J grade devices done on sample basis.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

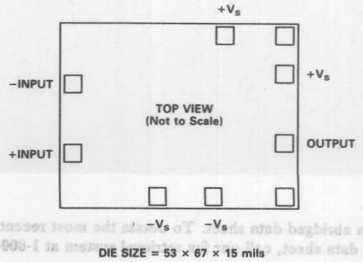
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9618JN	0 to +70°C	Plastic DIP	N-8
AD9618JR	0 to +70°C	SOIC	R-8
AD9618AQ	−40°C to +85°C	Cerdip	Q-8
AD9618BQ	−40°C to +85°C	Cerdip	Q-8
AD9618SQ	−55°C to +125°C	Cerdip	Q-8
AD9618TQ	−55°C to +125°C	Cerdip	Q-8

*For outline information see Package Information section.

DIE CONNECTIONS



DIE SIZE = 53 × 67 × 15 mils

Ultralow Distortion, 600 MHz Buffer

AD9620*

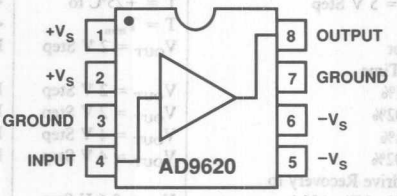
FEATURES

Excellent Gain Accuracy: 0.994 V/V
Wide Bandwidth: 600 MHz
Slew Rate: 2200 V/μs
Ultralow Distortion:
−73 dBc @ 20 MHz
−91 dBc @ 2.3 MHz
Fast Settling Time: 8 ns to 0.02%
Low Noise: 2.0 nV/√Hz

APPLICATIONS

IF/Communications
Impedance Transformations
Drives Flash ADCs
Line Driving

DIP CONFIGURATION



NC = NO CONNECT

GENERAL DESCRIPTION

The AD9620 is a monolithic, unity gain buffer amplifier that sets new standards in gain accuracy, wide bandwidth and low distortion. Its large signal bandwidth, ultralow distortion over frequency, and drive capabilities of the AD9620 make this buffer an ideal driver for flash ADCs. Other applications which require increased current drive at unity voltage gain, such as cable driving, also benefit from the AD9620's performance.

In addition to innovative (patent pending) feedback architecture, special packaging techniques improve dynamic performance by minimizing the reactive effects associated with standard packages. The result is −73 dBc harmonic suppression at 20 MHz, and −91 dBc at 2.3 MHz. The AD9620 also outperforms other amplifiers, including its predecessor AD9630, in terms of small-signal pulse response and dc linearity. These features make the AD9620 the premier driver for high speed, high resolution ADCs.

Available in side-brazed ceramic DIP packages, the "A" suffix unit is guaranteed for −40°C to +85°C operating temperatures; the "S" suffix device is guaranteed from −55°C to +125°C. AD9620 die are dc tested at +25°C.

*Patent(s) Pending.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±7 V
Input Voltage Range . . . . . $\pm V_S$
Continuous Output Current[2] . . . . . 70 mA
Operating Temperature Ranges
AD9620AD . . . . . −40°C to +85°C
AD9620SD . . . . . −55°C to +125°C
Storage Temperature
AD9620AD . . . . . −65°C to +150°C
AD9620SD . . . . . −65°C to +150°C
Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10 seconds)[4] . . . . . +300°C

DC ELECTRICAL CHARACTERISTICS (unless otherwise noted, $\pm V_S = \pm 5$ V; $R_{IN} = 50\ \Omega$, $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9620AD Min	AD9620AD Typ	AD9620AD Max	AD9620SD Min	AD9620SD Typ	AD9620SD Max	Units
DC SPECIFICATIONS										
Output Offset Voltage		+25°C	I	−8	±2	+8	−8	±2	+8	mV
Offset Voltage TC		Full	IV	−25	±5	+25	−25	±5	+25	µV/°C
Input Bias Current		+25°C	I	−35	±6	+35	−35	±6	+35	µA
Bias Current TC		Full	IV	−150	±50	+150	−150	±50	+150	nA/°C
Input Resistance		+25°C to T_{max}	VI	400	800		400	800		kΩ
Input Resistance		T_{min}	VI	190			190			kΩ
Input Capacitance		+25°C	V		1.0			1.0		pF
Gain	V_{OUT} = 2 V p–p	Full	VI	0.989	0.994		0.989	0.994		V/V
Output Voltage Range		Full	VI	+2.8		−2.8	+2.8		−2.8	V
Output Current (50 Ω Load)		Full	VI	40			40			mA
Output Impedance	At DC	+25°C	V		0.4			0.4		Ω
Power Supply Rejection Ratio	$\Delta V_S = \pm 5\%$	Full	VI	52	60		52	60		dB
DC Nonlinearity	±2 V Full Scale	+25°C	VI		0.005			0.005		%
FREQUENCY DOMAIN										
Bandwidth (−3 dB)										
Small Signal	V_{OUT} = ≤0.7 V p–p	T_{min} to +25°C	II	320	600		320	600		MHz
Small Signal	V_{OUT} = ≤0.7 V p–p	T_{max}	II	260			260			MHz
Large Signal	V_{OUT} = 4 V p–p	T_{min} to +25°C	IV	60	80		60	80		MHz
Large Signal	V_{OUT} = 4 V p–p	T_{max}	IV	45			45			MHz
Amplitude of Peaking	≤150 MHz	T_{min} to +25°C	II		0.8	1.5		0.8	1.5	dB
Amplitude of Peaking	≤150 MHz	T_{max}	II		1.5	2.2		1.5	2.2	dB
Amplitude of Rolloff	≤150 MHz	Full	II		0	0.3		0	0.3	dB
Group Delay	DC to 150 MHz	+25°C	V		0.75			0.75		ns
Phase Nonlinearity	DC to 150 MHz	+25°C	V		1.4			1.4		Degrees
2nd Harmonic Distortion	2 V p–p; 2.3 MHz	+25°C to T_{max}	IV		−91	−82		−91	−82	dBc
	2 V p–p; 2.3 MHz	T_{min}	IV		−81	−73		−81	−73	dBc
	2 V p–p; 20 MHz	Full	IV		−71	−63		−71	−63	dBc
	2 V p–p; 60 MHz	+25	I		−69	−60		−69	−60	dBc
	2 V p–p; 60 MHz	T_{min} and T_{max}	V		−62			−62		dBc
3rd Harmonic Distortion	2 V p–p; 2.3 MHz	Full	IV		−94	−86		−94	−86	dBc
	2 V p–p; 20 MHz	Full	IV		−81	−71		−81	−71	dBc
	2 V p–p; 60 MHz	+25°C	I		−60	−52		−60	−52	dBc
Spectral Input Noise Voltage	10 MHz	+25°C	V		2.0			2.0		nV/√Hz
Average Equivalent Integrated Output Noise Voltage	0.1 to 200 MHz	+25°C	V		28			28		µV
TIME DOMAIN										
Slew Rate	V_{OUT} = 4 V Step	+25°C	IV	1500	2200		1500	2200		V/µs
Rise/Fall Time	V_{OUT} = 1 V Step	T_{min} to +25°C	IV		0.8	1.2		0.8	1.2	ns
	V_{OUT} = 1 V Step	T_{max}	IV		1.1	1.5		1.1	1.5	ns
	V_{OUT} = 4 V Step	T_{min} to +25°C	IV		1.7	2.5		1.7	2.5	ns
	V_{OUT} = 4 V Step	T_{max}	IV		2.3	3.4		2.3	3.4	ns
Overshoot	V_{OUT} = 2 V Step	Full	IV		3	12		3	12	%
Settling Time										
To 0.1%	V_{OUT} = 2 V Step	Full	IV		6	10		6	10	ns
To 0.02%	V_{OUT} = 2 V Step	Full	IV		8	16		8	16	ns
Differential Gain	4.4 MHz	+25°C	V		0.02			0.02		%
Differential Phase	4.4 MHz	+25°C	V		0.02			0.02		Degrees

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Parameter	Conditions	Temp	Test Level	AD9620AD Min	AD9620AD Typ	AD9620AD Max	AD9620SD Min	AD9620SD Typ	AD9620SD Max	Units
POWER SUPPLY REQUIREMENTS										
Quiescent Current										
$+I_S$	$+V_S = +5$ V	Full	VI		40	48		40	48	mA
$-I_S$	$-V_S = -5$ V	Full	VI		40	48		40	48	mA

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Output is short-circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.

[3]Typical side-brazed thermal impedances (part soldered onto board): $\theta_{JA} = 110°C/W$; $\theta_{JC} = 20°C/W$.

[4]External capacitor of AD9620 is attached with 62 Sn/36 Pb/2 Ag solder. Board attachment temperatures should be reviewed to insure the capacitor does not reflow during board mounting.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

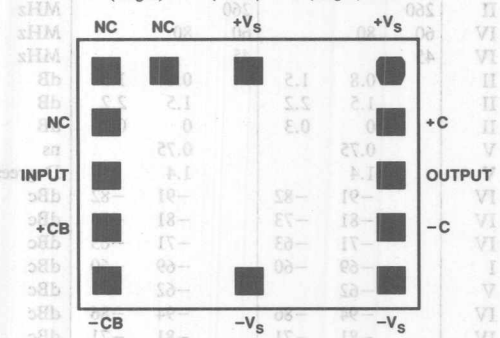
ORDERING GUIDE

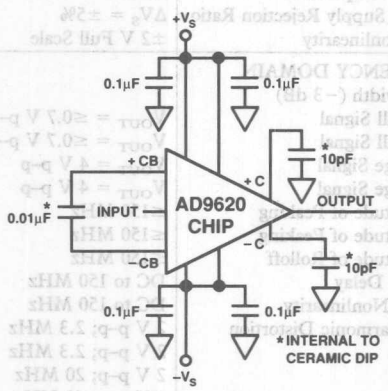
Model	Temperature Range	Package Description	Package Option*
AD9620AD	−40°C to +85°C	8-Pin DIP	D-8
AD9620SD	−55°C to +125°C	8-Pin DIP	D-8
AD9620 Chips	+25°C	Dice	

*For outline information see Package Information section.

AD9620 DIE LAYOUT

60 (length) × 50 (width) × 15 (height) mils





AD9620 Bonding Diagram

THEORY OF OPERATION

The AD9620 is a wide bandwidth, unity gain buffer amplifier that utilizes innovative (patent pending) voltage feedback architecture. Large loop gain and high slew rate significantly improve dc linearity and large signal bandwidth when compared with that achieved with more conventional designs.

Its large-signal bandwidth compares favorably with competitive devices of open-loop design without their limitations. Open-loop devices often sacrifice dc linearity and introduce frequency distortion when driving low load impedances; the AD9620 does not. Its design yields low distortion products that are relatively constant for any resistive load greater than 50 ohms.

The AD9620 will satisfy any high performance analog signal processing application requiring isolation or current boosting between the signal source and load. Its combination of high input resistance and low capacitance, dc precision, and exceptional dynamic characteristics sets a new standard in performance that has no equal.

Excessive peaking may occur when using the AD9620 to directly drive loads with more than 3 pF of capacitance. To prevent this, a small value of resistance (R_S) should be placed in series with the buffer output.

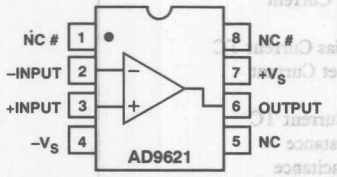
Wideband Voltage Feedback Amplifier

AD9621*

FEATURES
350 MHz Small Signal Bandwidth
130 MHz Large Signal BW (4 V p-p)
High Slew Rate: 1200 V/μs
Fast Settling: 11 ns to 0.01%/7 ns to 0.1%
±3 V Supply Operation

APPLICATIONS
ADC Input Driver
Differential Amplifiers
IF/RF Amplifiers
Pulse Amplifiers
Professional Video
DAC Current-to-Voltage
Baseband and Video Communications
Pin Diode Receivers
Active Filters/Integrators/Log Amps

CONNECTION DIAGRAM



 # OPTIONAL CAPACITOR CB CONNECTED HERE DECREASES SETTLING TIME

GENERAL DESCRIPTION

The AD9621 is one of a family of very high speed and wide bandwidth amplifiers utilizing a voltage feedback architecture. These amplifiers define a new level of performance for voltage feedback amplifiers, especially in the categories of large signal bandwidth, slew rate, settling, and low noise.

Proprietary design architectures have resulted in an amplifier family that combines the most attractive attributes of both current feedback and voltage feedback amplifiers. The AD9621 exhibits extraordinarily accurate and fast pulse response characteristics (7 ns settling to 0.1%) as well as extremely wide small and large signal bandwidth previously found only in current feedback amplifiers. When combined with balanced high impedance inputs and low input noise current more common to voltage feedback architectures, the AD9621 offers performance not previously available in a monolithic operational amplifier.

***Protected by U.S. Patent 5,150,074 and others pending.**

Other members of the AD962X amplifier family are the AD9622 (G = +2), AD9623 (G = +4), and the AD9624 (G = +6). A separate data sheet is available from Analog Devices for each model. Each generic device has been designed for a different minimum stable gain setting, allowing users flexibility in optimizing system performance. Dynamic performance specifications such as slew rate, settling time, and distortion vary from model to model. The table below summarizes key performance attributes for the AD962X family and can be used as a selection guide.

The AD9621 is offered in industrial and military temperature ranges. Industrial versions are available in plastic DIP, SOIC, and cerdip; MIL versions are packaged in cerdips.

PRODUCT HIGHLIGHTS

1. Wide Large Signal Bandwidth
2. High Slew Rate
3. Fast Settling
4. Output Short-Circuit Protected

Parameter	AD9621	AD9622	AD9623	AD9624	Units
Minimum Stable Gain	+1	+2	+4	+6	V/V
Harmonic Distortion (20 MHz)	−52	−66	−64	−66	dB
Large Signal Bandwidth (4 V p-p)	130	160	190	200	MHz
SSBW (0.5 V p-p)	350	220	270	300	MHz
Slew Rate	1200	1500	2100	2200	V/μs
Rise/Fall Time (0.5 V Step)	2.4	1.7	1.6	1.5	ns
Settling Time (to 0.1%/0.01%)	7/11	8/14	8/14	8/14	ns
Input Noise (0.1 MHz – 200 MHz)	80	49	36	32	μV rms

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9621—SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5$ V, $R_{LOAD} = 100\ \Omega$; $A_V = 1$, unless otherwise noted)

Parameter	Conditions	Temp	Test Level	AD9621AN/AQ/AR Min	AD9621AN/AQ/AR Typ	AD9621AN/AQ/AR Max	AD9621SQ Min	AD9621SQ Typ	AD9621SQ Max	Units
DC SPECIFICATIONS[1]										
Input Offset Voltage		+25°C	I	−12	±2	+12	−12	±2	+12	mV
		Full	VI	−15		+15	−15		+15	mV
Input Bias Current		+25°C	I		7	16		7	16	μA
		Full	VI	−20		+20	−20		+20	μA
Input Bias Current TC		Full	V		35			35		nA/°C
Input Offset Current		+25°C	I	−2.0	±0.3	+2.0	−2.0		+2.0	μA
		Full	VI	−3.0		+3.0	−3.0		+3.0	μA
Offset Current TC		Full	V		2.5			2.5		nA/°C
Input Resistance		+25°C	V		500			500		kΩ
Input Capacitance		+25°C	V		1.2			1.2		pF
Common-Mode Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Common-Mode Rejection Ratio	$\Delta V_{CM} = 1$ V	+25°C	I	46	49		46	49		dB
Open Loop Gain	$V_{OUT} = \pm 2$ V p-p	+25°C	V		56			56		dB
Output Voltage Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Output Current		Full	VI	60	70		60	70		mA
Output Resistance		+25°C	V		0.3			0.3		Ω
FREQUENCY DOMAIN										
Bandwidth (−3 dB)										
Small Signal	$V_{OUT} \leq 0.4$ V p-p	Full	II	230	350		230	350		MHz
Large Signal	$V_{OUT} \leq 4.0$ V p-p	Full	V		130			130		MHz
Amplitude of Peaking	Full Spectrum	Full	II		0.1	1.2		0.1	1.2	dB
Amplitude of Roll-off	≤ 100 MHz	Full	II		0	0.6		0	0.6	dB
Phase Nonlinearity	dc to 100 MHz	+25°C	V		1.1			1.1		Degree
2nd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		−55	−44		−55	−44	dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		−52	−43		−52	−43	dBc
Common-Mode Rejection Mode	@ 20 MHz	+25°C	V		+28			+28		dB
Spectral Input Noise Voltage	1 to 200 MHz	+25°C	V		5.6			5.6		$nV/\sqrt{Hz}$
Spectral Input Noise Current	1 to 200 MHz	+25°C	V		3.6			3.6		$pA/\sqrt{Hz}$
Average Equivalent Integrated Input Noise Voltage	0.1 to 200 MHz	+25°C	V		80			80		μV rms
TIME DOMAIN										
Slew Rate	$V_{OUT} = 5$ V Step	Full	IV	850	1200		850	1200		V/μs
Rise/Fall Time	$V_{OUT} = 0.5$ V Step	+25°C	V		2.4			2.4		ns
	$V_{OUT} = 5$ V Step	Full	IV		4.8	7		4.8	7	ns
Overshoot	$V_{OUT} = 2$ V Step	Full	IV		0	15		0	15	%
Settling Time										
To 0.1%	$V_{OUT} = 2$ V Step	+25°C	V		7			7		ns
To 0.01%	$V_{OUT} = 2$ V Step	Full	IV		11	15		11	15	ns
To 0.1%[2]	$V_{OUT} = 4$ V Step	+25°C	V		9			9		ns
To 0.01[2]	$V_{OUT} = 4$ V Step	+25°C	V		13			13		ns
Overdrive Recovery	1.5x to ±2 mV	+25°C	V		50			50		ns
Differential Gain (4.3 MHz)	$R_L = 150\ \Omega$	+25°C	V		0.01			0.01		%
Differential Phase (4.3 MHz)	$R_L = 150\ \Omega$	+25°C	V		<0.01			<0.01		Degree
POWER SUPPLY REQUIREMENTS[1]										
Supply Voltage ($\pm V_S$)		Full	IV	3.0	5.0	5.5	3.0	5.0	5.5	V
Quiescent Current										
$+I_S$	$+V_S = +5$ V	Full	VI		23	29		23	29	mA
$-I_S$	$-V_S = -5$ V	Full	VI		23	29		23	29	mA
Power Supply Rejection Ratio	$\Delta V_S = 0.5$ V	+25°C	I	54	66		54	66		dB

NOTES

[1]Measured at $A_V = 21$.

[2]Measured with a 0.001 μF C_B capacitor connected across Pins 1 and 8.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±6 V
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 6 V
Continuous Output Current[2] . . . . . 90 mA
Operating Temperature Ranges
AN, AQ, AR . . . . . −40°C to +85°C
SQ . . . . . −55°C to +125°C
Storage Temperature
Ceramic . . . . . −65°C to +150°C
Plastic . . . . . −65°C to +125°C
Junction Temperature
Ceramic[3] . . . . . +175°C
Plastic[3] . . . . . +150°C
Lead Soldering Temperature (1 minute)[4] . . . . . +220°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Output is short-circuit protected; for maximum reliability, 90 mA continuous current should not be exceeded.
[3]Typical thermal impedances (part soldered onto board; no air flow):
Ceramic DIP: θ_{JA} = 100°C/W; θ_{JC} = 30°C/W
Plastic SOIC: θ_{JA} = 125°C/W; θ_{JC} = 45°C/W
Plastic DIP θ_{JA} = 90°C/W; θ_{JC} = 45°C/W
[4]Temperature shown is for surface mount devices, mounted by vapor phase soldering. Throughhole devices (ceramic and plastic DIPs) can be soldered at +300°C for 10 seconds.

ORDERING GUIDE

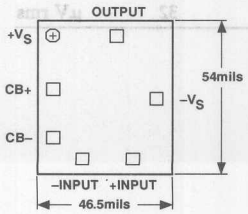
Model	Temperature Range	Package Description	Package Option*
AD9621AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD9621AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD9621AR	−40°C to +85°C	8-Pin SOIC	R-8
AD9621SQ	−55°C to +125°C	8-Pin Cerdip	Q-8

*For outline information see Package Information section.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing of "A" grade devices done on sample basis.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



Chip Layout

THEORY OF OPERATION

The AD9621 is a wide bandwidth, unity gain stable voltage feedback amplifier. Since its open-loop frequency response follows the conventional 6 dB/octave roll-off, its gain bandwidth product is basically constant. Increasing its closed-loop gain results in a corresponding decrease in small signal bandwidth. The AD9621 typically maintains a 55 degree unity loop gain phase margin. This high margin minimizes the effects of signal and noise peaking.

Feedback Resistor Choice

At minimum stable gain (+1), the AD9621 provides optimum dynamic performance with $R_F \cong 51\ \Omega$. This resistor acts only as a parasitic suppressor against damped R_F oscillations that can occur due to lead (input, feedback) inductance and parasitic capacitance. For settling accuracy to 0.1% or less, this resistor should not be required if layout guidelines are closely followed. This value for R_F provides the best combination of wide bandwidth, low parasitic peaking, and fast settling time.

When the AD9621 is used in the transimpedance (I-to-V) mode, such as for photo-diode detection, the value for R_F and diode capacitance (C_I) are usually known. See Figure 1. Generally, the value of R_F selected will be in the kΩ range, and a shunt capacitor (C_F) across R_F will be required to maintain good amplifier stability. The value of C_F required to maintain <1 dB of peaking can be estimated as:

$$C_F \cong [(2\omega_o C_I R_F - 1)/\omega_O{}^2 R_F{}^2]^{1/2} \quad \Big| \quad R_F \geq 1k\Omega$$

where ω_O is equal to the unity gain bandwidth product of the amplifier in RAD/sec, and C_I is the equivalent total input capacitance at the inverting input. Typically ω_O is 700 × 10^6 RAD/sec (See Open Loop Frequency Response curve).

As an example, choosing R_F of 10 kΩ and C_I of 5 pF, requires C_F to be 1.1 pF (Note: C_I includes both the source and parasitic circuit capacitance). The bandwidth of the amplifier can be estimated using the C_F calculated as:

$$f_3\,dB \cong \frac{1.6}{2\,\pi\,R_F\,C_F}$$

For general voltage gain applications, the amplifier bandwidth can be estimated as:

$$f_3\,dB \cong \frac{\omega_O}{1 + \left(\frac{R_F}{R_G}\right)}$$

This estimation loses accuracy for gains approaching +2/−1 or lower due to the amplifier's damping factor. For these "low gain" cases, the bandwidth will actually extend beyond the calculated value. See Closed Loop BW plots.

As a rule of thumb, capacitor C_F will not be required if:

$$(R_F \| R_G)\,C_I \leq \frac{NG}{4\,\omega_O}$$

where NG is the Noise Gain (1 + R_F/R_G) of the circuit. For most voltage gain applications, this should be the case.

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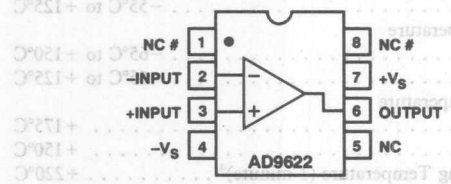
Wideband Voltage Feedback Amplifier

AD9622*

FEATURES
220 MHz Small Signal Bandwidth
160 MHz Large Signal BW (4 V p-p)
High Slew Rate: 1500 V/μs
Low Distortion: −66 dB @ 20 MHz
Fast Settling: 14 ns to 0.01%
3.5 nV/√Hz Spectral Noise Density
±3 V Supply Operation

APPLICATIONS
ADC Input Signal Amplifier
Differential Amplifiers
IF/RF Amplifiers
Pulse Amplifiers
Professional Video
DAC Current-to-Voltage
Baseband and Video Communications
Active Filters/Integrators/Log Amps

CONNECTION DIAGRAM



 # OPTIONAL CAPACITOR CB CONNECTED HERE DECREASES SETTLING TIME (SEE TEXT).

GENERAL DESCRIPTION

The AD9622 is one of a family of very high speed and wide bandwidth amplifiers utilizing a voltage feedback architecture. These amplifiers define a new level of performance for voltage feedback amplifiers, especially in the categories of large signal bandwidth, slew rate, settling, low distortion, and low noise.

Proprietary design architectures have resulted in an amplifier family that combines the most attractive attributes of both current feedback and voltage feedback amplifiers. The AD9622 exhibits extraordinarily accurate and fast pulse response characteristics (8 ns settling to 0.1%) as well as extremely wide small and large signal bandwidth previously found only in current feedback amplifiers. When combined with balanced high impedance inputs and low input noise more common to voltage feedback architectures, the AD9622 offers performance not previously available in a monolithic operational amplifier.

***Protected by U.S. Patent 5,150,074 and others pending.**

Other members of the AD962X amplifier family are the AD9621 (G = +1), AD9623 (G = +4), and the AD9624 (G = +6). A separate data sheet is available from Analog Devices for each model. Each generic device has been designed for a different minimum stable gain setting, allowing users flexibility in optimizing system performance. Dynamic performance specifications such as slew rate, settling time, and distortion vary from model to model. The table below summarizes key performance attributes for the AD962X family and can be used as a selection guide.

The AD9622 is offered in industrial and military temperature ranges. Industrial versions are available in plastic DIP, SOIC, and cerdip; MIL versions are packaged in cerdips.

PRODUCT HIGHLIGHTS

1. Wide Large Signal Bandwidth
2. High Slew Rate
3. Fast Settling
4. Low Distortion
5. Output Short-Circuit Protected
6. Low Intermodulation Distortion of High Frequencies

Parameter	AD9621	AD9622	AD9623	AD9624	Units
Minimum Stable Gain	+1	+2	+4	+6	V/V
Harmonic Distortion (20 MHz)	−52	−66	−64	−66	dB
Large Signal Bandwidth (4 V p-p)	130	160	190	200	MHz
SSBW (0.5 V p-p)	350	220	270	300	MHz
Slew Rate	1200	1500	2100	2200	V/μs
Rise/Fall Time (0.5 V Step)	2.4	1.7	1.6	1.5	ns
Settling Time (to 0.1%/0.01%)	7/11	8/14	8/14	8/14	ns
Input Noise (0.1 MHz–200 MHz)	80	49	36	32	μV rms

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $\pm V_S = \pm 5$ V; $R_{LOAD} = 100\ \Omega$; $A_V = 2$; $R_F = 270\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9622AN/AQ/AR Min	AD9622AN/AQ/AR Typ	AD9622AN/AQ/AR Max	AD9622SQ Min	AD9622SQ Typ	AD9622SQ Max	Units
DC SPECIFICATIONS[1]										
Input Offset Voltage		+25°C	I	−10	±2	+10	−10	±2	+10	mV
		Full	VI	−12		+12	−12		+12	mV
Input Bias Current		+25°C	I		7	14		7	14	μA
		Full	VI			18			18	μA
Bias Current TC		Full	V		35			35		nA/°C
Input Offset Current		+25°C	I	−2	±0.3	+2	−2	±0.3	+2	μA
		Full	VI	−3		+3	−3		+3	μA
Offset Current TC		Full	V		2.5			2.5		nA/°C
Input Resistance		+25°C	V		500			500		kΩ
Input Capacitance		+25°C	V		1.2			1.2		pF
Common-Mode Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Common-Mode Rejection Ratio	$\Delta V_{CM} = 1$ V	+25°C	I	47	57		47	57		dB
Open-Loop Gain	$V_{OUT} = \pm 2$ V p-p	+25°C	V		60			60		dB
Output Voltage Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Output Current		Full	VI	60	70		60	70		mA
Output Resistance		+25°C	V		0.3			0.3		Ω
FREQUENCY DOMAIN										
Bandwidth (−3 dB)										
Small Signal	$V_{OUT} \le 0.4$ V p-p	Full	II	160	220		160	220		MHz
Large Signal[2]	$V_{OUT} = 4$ V p-p	+25°C	V		160			160		MHz
Amplitude of Peaking	Full Spectrum	Full	II		0.2	1.2		0.2	1.2	dB
Amplitude of Roll-off	DC to 100 MHz	Full	II		0	0.8		0	0.8	dB
Phase Nonlinearity	0.3 MHz to 100 MHz	+25°C	V		1.3			1.3		degree
2nd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		−66	−56		−66	−56	dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		−68	−56		−68	−56	dBc
Common-Mode Rejection Ratio	@ 20 MHz	+25°C	V		+23			+23		dB
Spectral Input Noise Voltage	1 MHz to 200 MHz	+25°C	V		3.5			3.5		$nV/\sqrt{Hz}$
Spectral Input Noise Current	1 MHz to 200 MHz	+25°C	V		3.2			3.2		$pA/\sqrt{Hz}$
Average Equivalent Integrated Input Noise Voltage	0.1 MHz to 200 MHz	+25°C	V		49			49		μV rms
TIME DOMAIN										
Slew Rate	$V_{OUT} = 5$ V Step	Full	IV	1150	1500		1150	1500		V/μs
Rise/Fall Time	$V_{OUT} = 0.5$ V Step	+25°C	V		1.7			1.7		ns
	$V_{OUT} = 5$ V Step	Full	IV		3.1	4.2		3.1	4.2	ns
Overshoot	$V_{OUT} = 2$ V Step	Full	IV		3	15		3	15	%
Settling Time										
To 0.1%	$V_{OUT} = 2$ V Step	+25°C	V		8			8		ns
To 0.01%	$V_{OUT} = 2$ V Step	Full	IV		14	19		14	19	ns
To 0.1%[3]	$V_{OUT} = 4$ V Step	+25°C	V		10			10		ns
To 0.01%[3]	$V_{OUT} = 4$ V Step	+25°C	V		17			17		ns
Overdrive Recovery	2× to ±2 mV	+25°C	V		150			150		ns
Differential Gain (4.3 MHz)	$R_L = 150\ \Omega$	+25°C	V		0.01			0.01		%
Differential Phase (4.3 MHz)	$R_L = 150\ \Omega$	+25°C	V		<0.01			<0.01		degree
POWER SUPPLY REQUIREMENTS[1]										
Supply Voltage ($\pm V_S$)		Full	IV	3.0	5.0	5.5	3.0	5.0	5.5	V
Quiescent Current										
$+I_S$	$+V_S = 5$ V	Full	VI		23	29		23	29	mA
$-I_S$	$-V_S = -5$ V	Full	VI		23	29		23	29	mA
Power Supply Rejection Ratio	$\Delta V_S = 0.5$ V	+25°C	I	54	63		54	63		dB

NOTES
[1]Measured at $A_V = 21$.
[2]Effective large signal bandwidth; the device should not be stressed above 250 V × MHz (V_{OUT} p-p × Frequency) to ensure long term reliability.
[3]Measured with a 0.001 μF CB capacitor connected across Pins 1 and 8.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±6 V
Common-Mode Input Voltage . . . . . $\pm V_S$
Voltage Swing × Bandwidth Product . . . . . 250 V × MHz
Differential Input Voltage . . . . . 6 V
Continuous Output Current[2] . . . . . 90 mA
Operating Temperature Ranges
AN, AQ, AR . . . . . −40°C to +85°C
SQ . . . . . −55°C to +125°C
Storage Temperature
Ceramic . . . . . −65°C to +150°C
Plastic . . . . . −65°C to +125°C
Junction Temperature
Ceramic[3] . . . . . +175°C
Plastic[3] . . . . . +150°C
Lead Soldering Temperature (1 minute)[4] . . . . . +220°C

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Output is short-circuit protected; for maximum reliability, 90 mA continuous current should not be exceeded.

[3]Typical thermal impedances (part soldered onto board; no air flow):
Ceramic DIP: θ_{JA} = 100°C/W; θ_{JC} = 30°C/W
Plastic SOIC: θ_{JA} = 125°C/W; θ_{JC} = 45°C/W
Plastic DIP: θ_{JA} = 90°C/W; θ_{JC} = 45°C/W

[4]Temperature shown is for surface mount devices, mounted by vapor phase soldering. Through-hole devices (Ceramic and Plastic DIPs) can be soldered at +300°C for 10 seconds.

ORDERING GUIDE

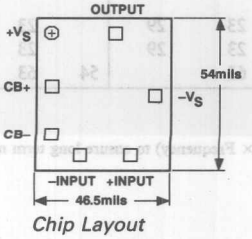
Model	Temperature Range	Package Description	Package Option*
AD9622AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD9622AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD9622AR	−40°C to +85°C	8-Pin SOIC	R-8
AD9622SQ	−55°C to +125°C	8-Pin Cerdip	Q-8

*For outline information see Package Information section.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing of "A" grade devices done on sample basis.
III– Sample tested only.
IV– Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI– All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



Chip Layout

THEORY OF OPERATION

The AD9622 is a wide bandwidth voltage feedback amplifier that is guaranteed for minimum gain stability of +2. Since its open loop frequency response follows the conventional 6 dB/octave roll-off, its gain bandwidth product is basically constant. Increasing its closed-loop gain results in a corresponding decrease in small signal bandwidth. The AD9622 typically maintains a 60 degree unity loop gain phase margin with $R_F \cong 270\ \Omega$. This high margin minimizes the effects of signal and noise peaking.

Feedback Resistor Choice

At minimum stable gain (+2), the AD9622 provides optimum dynamic performance with $R_F = 270\ \Omega$. When using this value and following the high speed layout guidelines, a shunt capacitor (C_F) should not be required. This value for R_F provides the best combination of wide bandwidth, low peaking, and distortion.

However, if improved gain flatness is desired, a shunt capacitor (C_F) will provide extra phase margin. This reduces both overshoot and peaking with only a slight reduction of bandwidth.

As an example, if the amplifier exhibits (worst case) peaking of 1 dB with $R_G \| R_F = 135\ \Omega$ ($A_V = 2$), then using a C_F of ≈ 1.5 pF across R_F will reduce this peaking to 0 dB. In addition, overshoot, noise, and settling time (0.01%) will also improve. This comes at the expense of slightly decreased closed-loop bandwidth due to the $R_F \times C_F$ time constant created.

If the equivalent input capacitance greatly exceeds 2 pF (due to source drive or long input traces to the amplifier), then added shunt capacitance (C_F) will be necessary to maintain stability.

Likewise, if larger R_G/R_F minimum-gain setting resistors are used, C_F will be necessary. As a rule of thumb, if the product of $R_F \| R_G \times C_I \leq 270 \times 10^{-12}$ seconds, then C_F is not required (for maximum bandwidth applications) and the amplifier's phase margin will maintain about 60°.

For $R_F \| R_G > 150\ \Omega$, use a C_F equal to $C_I \times R_G/R_F$. As the value of $R_F \| R_G$ increases, the bandwidth of the amplifier will begin to be controlled by the $R_F \times C_F$ time constant. Increasing C_F much beyond these guidelines will also cause amplifier instability.

Pulse Response

Unlike a traditional voltage feedback amplifier in which slew speed is usually dictated by its front end dc quiescent current and gain bandwidth product, the AD9622 provides "on demand" transconductance current that increases proportionally to the input "step" signal amplitude. This results in slew speeds (1500 V/μs) comparable to wideband current feedback designs. This, combined with relatively low input noise current (3.2 pA/$\sqrt{\text{Hz}}$), gives the AD9622 the best attributes of both voltage and current feedback amplifiers.

Bootstrap Capacitor (C_B)

In most applications, the C_B capacitor should not be required. Under certain conditions, it can be used to further enhance settling time performance.

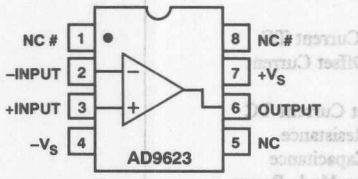
Wideband Voltage Feedback Amplifier

AD9623*

FEATURES
- 270 MHz Small Signal Bandwidth
- 190 MHz Large Signal BW (4 V p-p)
- High Slew Rate: 2100 V/μs
- Low Distortion: −64 dB @ 20 MHz
- Fast Settling: 15 ns to 0.01
- 2.6 nV/√Hz Spectral Noise Density
- ±3 V Supply Operation

APPLICATIONS
- ADC Input Driver
- Differential Amplifiers
- IF/RF Amplifiers
- Pulse Amplifiers
- Professional Video
- DAC Current-to-Voltage
- Baseband and Video Communications
- Active Filters/Integrators/Log Amps

CONNECTION DIAGRAM



 # OPTIONAL CAPACITOR CB CONNECTED HERE DECREASES SETTLING TIME (SEE TEXT).

GENERAL DESCRIPTION

The AD9623 is one of a family of very high speed and wide bandwidth amplifiers utilizing a voltage feedback architecture. These amplifiers define a new level of performance for voltage feedback amplifiers, especially in the categories of large signal bandwidth, slew rate, settling, low distortion, and low noise.

Proprietary design architectures have resulted in an amplifier family that combines the most attractive attributes of both current feedback and voltage feedback amplifiers. The AD9623 exhibits extraordinarily accurate and fast pulse response characteristics (8 ns settling to 0.1%) as well as extremely wide small and large signal bandwidth previously found only in current feedback amplifiers. When combined with balanced high impedance inputs and low input noise current more common to voltage feedback architectures, the AD9623 offers performance not previously available in a monolithic operational amplifier.

Other members of the AD962X amplifier family are the AD9621 (G = +1), AD9622 (G = +2), and the AD9624 (G = +6). A separate data sheet is available from Analog Devices for each model. Each generic device has been designed for a different minimum stable gain setting, allowing users flexibility in optimizing system performance. Dynamic performance specifications such as slew rate, settling time, and distortion vary from model to model. The table below summarizes key performance attributes for the AD962X family and can be used as a selection guide.

The AD9623 is offered in industrial and military temperature ranges. Industrial versions are available in plastic DIP, SOIC, and cerdip; MIL versions are packaged in cerdips.

PRODUCT HIGHLIGHTS

1. Wide Large Signal Bandwidth
2. High Slew Rate
3. Fast Settling
4. Low Distortion
5. Output Short-Circuit Protected
6. Low Intermodulation Distortion at High Frequencies

***Protected by U.S. Patent 5,150,074 and others pending.**

Parameter	AD9621	AD9622	AD9623	AD9624	Units
Minimum Stable Gain	+1	+2	+4	+6	V/V
Harmonic Distortion (20 MHz)	−52	−66	−64	−66	dB
Large Signal Bandwidth (4 V p-p)	130	160	190	200	MHz
SSBW (0.5 V p-p)	350	220	270	300	MHz
Slew Rate	1200	1500	2100	2200	V/μs
Rise/Fall Time (0.5 V Step)	2.4	1.7	1.6	1.5	ns
Settling Time (to 0.1%/0.01%)	7/11	8/14	8/14	8/14	ns
Input Noise (0.1 MHz–200 MHz)	80	49	36	32	μV rms

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter	Conditions	Temp	Level	AD9623AN/AQ/AR Min	AD9623AN/AQ/AR Typ	AD9623AN/AQ/AR Max	AD9623SQ Min	AD9623SQ Typ	AD9623SQ Max	Units
DC SPECIFICATIONS[1]										
Input Offset Voltage		+25°C	I	−8	±2	+8	−8	±2	+8	mV
		Full	VI	−10		+10	−10		+10	mV
Input Bias Current		+25°C	I		6	12		6	12	μA
		Full	VI			16			16	μA
Bias Current TC		Full	V		30			30		nA/°C
Input Offset Current		+25°C	I	−2	±0.3	+2	−2	±0.3	+2	μA
		Full	VI	−3		+3	−3		+3	μA
Offset Current TC		Full	V		2.0			2.0		nA/°C
Input Resistance		+25°C	V		600			600		kΩ
Input Capacitance		+25°C	V		1.2			1.2		pF
Common-Mode Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Common-Mode Rejection Ratio	ΔV_{CM} = 1 V	+25°C	I	52	63		52	63		dB
Open Loop Gain	V_{OUT} = ±2 V p-p	+25°C	V		69			69		dB
Output Voltage Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Output Current		Full	VI	60	70		60	70		mA
Output Resistance		+25°C	V		0.3			0.3		Ω
FREQUENCY DOMAIN										
Bandwidth (−3 dB)										
Small Signal	V_{OUT} = 0.4 V p-p	Full	II	190	270		190	270		MHz
Large Signal	V_{OUT} = 4 V p-p	+25°C	V		190			190		MHz
Amplitude of Peaking	Full Spectrum	Full	II		0.1	1.2		0.1	1.2	dB
Amplitude of Roll-off	DC to 100 MHz	Full	II		0	0.7		0	0.7	dB
Phase Nonlinearity	0.3 MHz to 100 MHz	+25°C	V		1.0			1.0		Degree
2nd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		−64	−56		−64	−56	dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		−72	−65		−72	−65	dBc
Common-Mode Rejection Ratio	@ 20 MHz	+25°C	V		+21			+21		dB
Spectral Input Noise Voltage	1 MHz to 200 MHz	+25°C	V		2.6			2.6		$nV/\sqrt{Hz}$
Spectral Input Noise Current	1 MHz to 200 MHz	+25°C	V		2.5			2.5		$pA/\sqrt{Hz}$
Average Equivalent Integrated Input Noise Voltage	0.1 MHz to 200 MHz	+25°C	V		36			36		μV rms
TIME DOMAIN										
Slew Rate	V_{OUT} = 5 V Step	Full	IV	1500	2100		1500	2100		V/μs
Rise/Fall Time	V_{OUT} = 0.5 V Step	+25°C	V		1.6			1.6		ns
	V_{OUT} = 5 V Step	Full	VI		2.4	3.1		2.4	3.1	ns
Overshoot	V_{OUT} = 2 V Step	Full	IV		3	15		3	15	%
Settling Time										
To 0.1%	V_{OUT} = 2 V Step	+25°C	V		8			8		ns
To 0.01%	V_{OUT} = 2 V Step	Full	IV		15	20		15	20	ns
To 0.1%[2]	V_{OUT} = 4 V Step	+25°C	V		9			9		ns
To 0.01%[2]	V_{OUT} = 4 V Step	+25°C	V		17			17		ns
Overdrive Recovery	2× to ±2 mV	+25°C	V		150			150		ns
Differential Gain (4.3 MHz)	R_L = 150 Ω	+25°C	V		0.01			0.01		%
Differential Phase (4.3 MHz)	R_L = 150 Ω	+25°C	V		<0.01			<0.01		Degree
POWER SUPPLY REQUIREMENTS[1]										
Supply Voltage (±V_S)		Full	IV	3.0	5.0	5.5	3.0	5.0	5.5	V
Quiescent Current										
$+I_S$	$+V_S$ = 5 V	Full	VI		23	29		23	29	mA
$-I_S$	$-V_S$ = −5 V	Full	VI		23	29		23	29	mA
Power Supply Rejection Ratio	ΔV_S = 1 V	+25°C	I	60	71		60	71		dB

NOTES
[1]Measured at A_V = 21.
[2]Measured with a 0.001 μF CB capacitor connected across Pins 1 and 8.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±6 V
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 6 V
Continuous Output Current[2] . . . . . 90 mA
Operating Temperature Ranges
AN, AQ, AR . . . . . −40°C to +85°C
SQ . . . . . −55°C to +125°C
Storage Temperature
Ceramic . . . . . −65°C to +150°C
Plastic . . . . . −65°C to +125°C
Junction Temperature
Ceramic[3] . . . . . +175°C
Plastic[3] . . . . . +150°C
Lead Soldering Temperature (1 minute)[4] . . . . . +220°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Output is short-circuit protected; for maximum reliability, 90 mA continuous current should not be exceeded.
[3]Typical thermal impedances (part soldered onto board; no air flow):
Ceramic DIP: θ_{JA} = 100°C/W; θ_{JC} = 30°C/W
Plastic SOIC: θ_{JA} = 125°C/W; θ_{JC} = 45°C/W
Plastic DIP: θ_{JA} = 90°C/W; θ_{JC} = 45°C/W
[4]Temperature shown is for surface mount devices, mounted by vapor phase soldering. Throughhole devices (Ceramic and Plastic DIPs) can be soldered at +300°C for 10 seconds.

ORDERING GUIDE

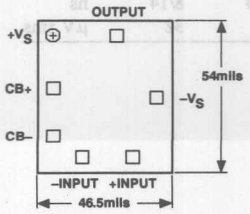
Model	Temperature Range	Package Description	Package Option*
AD9623AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD9623AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD9623AR	−40°C to +85°C	8-Pin SOIC	R-8
AD9623SQ	−55°C to +125°C	8-Pin Cerdip	Q-8

*For outline information see Package Information section.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing of A-grade devices done on sample basis.
III– Sample tested only.
IV– Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI– All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



Chip Layout

THEORY OF OPERATION

The AD9623 is a wide bandwidth voltage feedback amplifier that is guaranteed for minimum gain stability of +4. Since its open-loop frequency response follows the conventional 6 dB/octave roll-off, its gain bandwidth product is basically constant. Increasing its closed-loop gain results in a corresponding decrease in small signal bandwidth. The AD9623 typically maintains a 60 degree unity loop gain phase margin. This high margin minimizes the effects of signal and noise peaking.

Feedback Resistor Choice

At minimum stable gain (+4), the AD9623 provides optimum dynamic performance with $R_F \cong 390\ \Omega$. When using this value and following the high speed layout guidelines, a shunt capacitor (C_F) should not be required. This value R_F provides the best combination of wide bandwidth, low peaking, and distortion.

However, if improved gain flatness is desired, a shunt capacitor (C_F) will provide extra phase margin. This reduces both overshoot and peaking with only a slight reduction of bandwidth. See Figure 1.

As an example, if the amplifier exhibits (worst case) peaking of 1 dB with $R_G \| R_F = 98\ \Omega$ ($A_V = 4$), then using an effective C_F of ≈ 0.5–1 pF across R_F will reduce this peaking to 0 dB. In addition, overshoot, noise, and settling time (0.01%) will also improve. This comes at the expense of slightly decreased closed-loop bandwidth due to the $R_F \times C_F$ time constant created.

If total input capacitance greatly exceeds 3 pF (due to source drive or long input traces to the amplifier), then added shunt capacitance (C_F) will be necessary to maintain stability for minimum gain.

Likewise, if larger R_G/R_F minimum-gain setting resistors are used, C_F will be necessary. As a rule of thumb, if the product of $R_F \| R_G \times C_I \leq 300 \times 10^{-12}$ seconds, then C_F is not required (for maximum bandwidth at minimum gain) and the amplifier's phase margin will maintain about 60°.

For $R_F \| R_G > 150\ \Omega$, use a C_F equal to $C_I \times R_G/R_F$. For C_I (total) @ 2 pF, requires C_F to be 0.5 pF. This can be achieved by two 1 pF capacitors in series, or by using a resistor divider network at the amplifier's output in conjunction with a larger capacitor. Increasing C_F much beyond these guidelines will also cause amplifier instability.

Pulse Response

Unlike a traditional voltage feedback amplifier in which slew speed is usually dictated by its front end dc quiescent current and gain bandwidth product, the AD9623 provides "on demand" transconductance current that increases proportionally to the input "step" signal amplitude. This results in slew speeds (2100 V/μs) comparable to wideband current feedback designs. This, combined with relatively low input noise current (2.5 pA/$\sqrt{\text{Hz}}$), gives the AD9623 the best attributes of both voltage and current feedback amplifiers.

Bootstrap Capacitor (C_B)

In most applications, the C_B capacitor will not be required. Under certain conditions, it can be used to further enhance settling time performance.

9

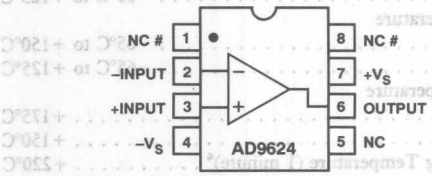
Wideband Voltage Feedback Amplifier

AD9624*

FEATURES
300 MHz Small Signal Bandwidth
200 MHz Large Signal BW (4 V p-p)
High Slew Rate: 2200 V/μs
Low Distortion: −60 dB @ 20 MHz
Fast Settling: 15 ns to 0.01%
2.2 nV/√Hz Spectral Noise Density
±3 V Supply Operation

APPLICATIONS
ADC Input Driver
Differential Amplifiers
IF/RF Amplifiers
Pulse Amplifiers
Professional Video
DAC Current-to-Voltage
Baseband and Video Communications
Active Filters/Integrators/Log Amps

CONNECTION DIAGRAM



 # OPTIONALCAPACITOR CB CONNECTED HERE DECREASES SETTLING TIME (SEE TEXT).

GENERAL DESCRIPTION

The AD9624 is one of a family of very high speed and wide bandwidth amplifiers utilizing a voltage feedback architecture. These amplifiers define a new level of performance for voltage feedback amplifiers, especially in the categories of large signal bandwidth, slew rate, settling, low distortion, and low noise.

Proprietary design architectures have resulted in an amplifier family that combines the most attractive attributes of both current feedback and voltage feedback amplifiers. The AD9624 exhibits extraordinarily accurate and fast pulse response characteristics (8 ns settling to 0.1%) as well as extremely wide small and large signal bandwidth previously found only in current feedback amplifiers. When combined with balanced high impedance inputs and low input noise current more common to voltage feedback architectures, the AD9624 offers performance not previously available in a monolithic operational amplifier.

***Protected by U.S. Patent 5,150,074 and others pending.**

Other members of the AD962X amplifier family are the AD9621 (G = +1), AD9622 (G = +2), and the AD9623 (G = +4). A separate data sheet is available from Analog Devices for each model. Each generic device has been designed for a different minimum stable gain setting, allowing users flexibility in optimizing system performance. Dynamic performance specifications such as slew rate, settling time, and distortion vary from model to model. The table below summarizes key performance attributes for the AD962X family and can be used as a selection guide.

The AD9624 is offered in industrial and military temperature ranges. Industrial versions are available in plastic DIP, SOIC, and cerdip; MIL versions are packaged in cerdips.

PRODUCT HIGHLIGHTS

1. Wide Large Signal Bandwidth
2. High Slew Rate
3. Fast Settling
4. Low Distortion
5. Output Short-Circuit Protected
6. Low Intermodulation Distortion at High Frequencies

Parameter	AD9621	AD9622	AD9623	AD9624	Units
Minimum Stable Gain	+1	+2	+4	+6	V/V
Harmonic Distortion (20 MHz)	−52	−66	−64	−66	dB
Large Signal Bandwidth (4 V p-p)	130	160	190	200	MHz
SSBW (0.5 V p-p)	350	220	270	300	MHz
Slew Rate	1200	1500	2100	2200	V/μs
Rise/Fall Time (0.5 V Step)	2.4	1.7	1.6	1.5	ns
Settling Time (to 0.1%/0.01%)	7/11	8/14	8/14	8/14	ns
Input Noise (0.1 MHz–200 MHz)	80	49	36	32	μV rms

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $\pm V_S = \pm 5$ V; $R_{LOAD} = 100\ \Omega$; $A_V = +8$; $R_F = 510\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9624AN/AQ/AR Min	AD9624AN/AQ/AR Typ	AD9624AN/AQ/AR Max	AD9624SQ Min	AD9624SQ Typ	AD9624SQ Max	Units
DC SPECIFICATIONS[1]										
Input Offset Voltage		+25°C	I	−8	±2	+8	−8	±2	+8	mV
		Full	VI	−10		+10	−10		+10	mV
Input Bias Current		+25°C	I		7	12		7	12	μA
		Full	VI			16			16	μA
Bias Current TC		Full	V		35			35		nA/°C
Input Offset Current		+25°C	I	−2	±0.3	+2	−2	±0.3	+2	μA
		Full	VI	−3		+3	−3		+3	μA
Offset Current TC		Full	V		2.5			2.5		nA/°C
Input Resistance		+25°C	V		500			500		kΩ
Input Capacitance		+25°C	V		1.2			1.2		pF
Common-Mode Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Common-Mode Rejection Ratio	$\Delta V_{CM} = 1$ V	+25°C	I	52	63		52	63		dB
Open-Loop Gain	$V_{OUT} = \pm 2$ V p-p	+25°C	V		74			74		dB
Output Voltage Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Output Current		Full	II	60	70		60	70		mA
Output Resistance		+25°C	V		0.3			0.3		Ω
FREQUENCY DOMAIN										
Small Signal Bandwidth										
$A_V = 6$	$V_{OUT} = 0.4$ V p-p	Full	IV	200	300		200	300		MHz
$A_V = 8$	$V_{OUT} = 0.4$ V p-p	Full	II	130	190		130	190		MHz
Large Signal Bandwidth	$V_{OUT} = 4$ V p-p	+25°C	V		170			170		MHz
Amplitude of Peaking	Full Spectrum	Full	II		0	0.4		0	0.4	dB
Amplitude of Peaking ($A_V = 6$)	Full Spectrum	+25°C	IV		0.2	1.2		0.2	1.2	dB
Amplitude of Roll-off	DC to 100 MHz	Full	II		0.6	1.6		0.6	1.6	dB
Phase Nonlinearity	0.3 MHz to 100 MHz	+25°C	V		0.7			0.7		Degree
2nd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		−60	−52		−60	−52	dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		−72	−64		−72	−64	dBc
Common-Mode Rejection Ratio	@ 20 MHz	+25°C	V		+30			+30		dB
Spectral Input Noise Voltage	1 MHz to 200 MHz	+25°C	V		2.2			2.2		nV/√Hz
Spectral Input Noise Current	1 MHz to 200 MHz	+25°C	V		2.5			2.5		pA/√Hz
Average Equivalent Integrated Input Noise Voltage	0.1 MHz to 200 MHz	+25°C	V		32			32		μV rms
TIME DOMAIN										
Slew Rate	$V_{OUT} = 5$ V Step	Full	IV	1400	2000		1400	2000		V/μs
Rise/Fall Time	$V_{OUT} = 0.5$ V Step	+25°C	V		1.8			1.8		ns
	$V_{OUT} = 5$ V Step	Full	IV		2.6	3.2		2.6	3.2	ns
Overshoot	$V_{OUT} = 2$ V Step	Full	IV		0	7		0	7	%
Settling Time										
To 0.1%	$V_{OUT} = 2$ V Step	+25°C	V		8			8		ns
To 0.01%	$V_{OUT} = 2$ V Step	Full	IV		15	20		15	20	ns
To 0.1%[2]	$V_{OUT} = 4$ V Step	+25°C	V		9			9		ns
To 0.01%[2]	$V_{OUT} = 4$ V Step	+25°C	V		17			17		ns
Overdrive Recovery	2× to ±2 mV	+25°C	V		130			130		ns
Differential Gain (4.3 MHz)	$R_L = 150\ \Omega$	+25°C	V		0.015			0.015		%
Differential Phase (4.3 MHz)	$R_L = 150\ \Omega$	+25°C	V		<0.01			<0.01		Degree
POWER SUPPLY REQUIREMENTS[1]										
Supply Voltage ($\pm V_S$)		Full	IV	3.0	5.0	5.5	3.0	5.0	5.5	V
Quiescent Current										
$+I_S$	$+V_S = 5$ V	Full	VI		23	29		23	29	mA
$-I_S$	$-V_S = -5$ V	Full	VI		23	29		23	29	mA
Power Supply Rejection Ratio	$\Delta V_S = 1$ V	+25°C	I	60	70		60	70		dB

NOTES
[1]Measured at $A_V = 21$.
[2]Measured with a 0.001 μF CB capacitor connected across Pins 1 and 8.
Specifications subject to change without notice.

Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	6 V
Continuous Output Current[2]	90 mA
Operating Temperature Ranges	
AN, AQ, AR	−40°C to +85°C
SQ	−55°C to +125°C
Storage Temperature	
Ceramic	−65°C to +150°C
Plastic	−65°C to +125°C
Junction Temperature	
Ceramic[3]	+175°C
Plastic[3]	+150°C
Lead Soldering Temperature (1 minute)[4]	+220°C

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Output is short-circuit protected; for maximum reliability, 90 mA continuous current should not be exceeded.

[3]Typical thermal impedances (part soldered onto board; no air flow):
Ceramic DIP: θ_{JA} = 100°C/W; θ_{JC} = 30°C/W
Plastic SOIC: θ_{JA} = 125°C/W; θ_{JC} = 45°C/W
Plastic DIP: θ_{JA} = 90°C/W; θ_{JC} = 45°C/W

[4]Temperature shown is for surface mount devices, mounted by vapor phase soldering. Through-hole devices (ceramic and plastic DIPs) can be soldered at +300°C for 10 seconds.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9624AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD9624AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD9624AR	−40°C to +85°C	8-Pin SOIC	R-8
AD9624SQ	−55°C to +125°C	8-Pin Cerdip	Q-8

*For outline information see Package Information section.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

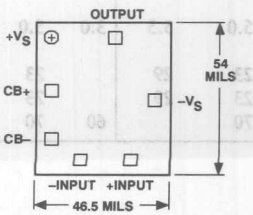
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing of A-grade devices done on sample basis.

III– Sample tested only.

IV– Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI– All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



Chip Layout

that is guaranteed for minimum gain stability of +6. Since its open loop frequency response follows the conventional 6 dB/octave roll-off, its gain bandwidth product is basically constant. Increasing its closed-loop gain results in a corresponding decrease in small signal bandwidth. The AD9624 typically maintains a 60 degree unity loop gain phase margin with $R_F \cong 510\ \Omega$. This high margin minimizes the effects of signal and noise peaking.

Feedback Resistor Choice

At minimum stable gain (+6), the AD9624 provides optimum dynamic performance with $R_F = 510\ \Omega$. When using this value and following the high speed layout guidelines, a shunt capacitor (C_F) should not be required. This value for R_F provides the best combination of wide bandwidth, low peaking, and distortion.

However, if improved gain flatness is desired, a shunt capacitor (C_F) will provide extra phase margin. This reduces both overshoot and peaking with only a slight reduction of bandwidth.

As an example, if the amplifier exhibits (worst case) peaking of 1.2 dB with $R_G \| R_F = 85\ \Omega$ ($A_V = 6$), then using a C_F of ≈ 0.5 pF (two 1 pF capacitors in series) across R_F will reduce this peaking to 0 dB. In addition, overshoot, noise, and settling time (<0.01%) will also improve. This comes at the expense of slightly decreased closed-loop bandwidth due to the $R_F \times C_F$ time constant created.

If the equivalent input capacitance greatly exceeds 4 pF (due to source drive or long input traces to the amplifier), then added shunt capacitance (C_F) will be necessary to maintain stability at minimum gain.

As a rule of thumb, if the product of $R_F \| R_G \times C_I \leq 300 \times 10^{-12}$ seconds, then C_F is not required (for maximum bandwidth applications) and the amplifier's phase margin will maintain about 60°. Generally, this should be the case.

Pulse Response

Unlike a traditional voltage feedback amplifier in which slew speed is usually dictated by its front end dc quiescent current and gain bandwidth product, the AD9624 provides "on demand" transconductance current that increases proportionally to the input "step" signal amplitude. This results in slew speeds (2000 V/μs) comparable to wideband current feedback designs. This, combined with relatively low input noise current (2.5 pA/$\sqrt{\text{Hz}}$), gives the AD9624 the best attributes of both voltage and current feedback amplifiers.

Low Distortion, 750 MHz Closed-Loop Buffer Amp

AD9630*

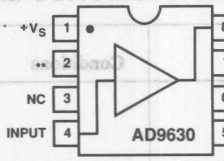
FEATURES

Excellent Gain Accuracy: 0.99 V/V
Wide Bandwidth: 750 MHz
Slew Rate: 1200 V/μs
Low Distortion
−65 dBc @ 20 MHz
−80 dBc @ 4.3 MHz
Settling Time
6 ns to 0.1%
8 ns to 0.02%
Low Noise: 2.4 nV/√Hz
Improved Source for CLC-110

APPLICATIONS

IF/Communications
Impedance Transformations
Drives Flash ADCs
Line Driving

PIN CONFIGURATION



**OPTIONAL +VS ***OPTIONAL −VS
NC = NO CONNECT

NOTE: FOR BEST SETTLING TIME PERFORMANCE USE OPTIONAL POWER SUPPLIES. ALL SPECIFICATIONS ARE BASED ON USING SINGLE ±VS CONNECTIONS EXCEPT FOR SETTLING TIME TO 0.02% AND SMALL SIGNAL S21. CONSULT THE FACTORY FOR VERSIONS WITH OPTIONAL POWER SUPPLY PINS DISCONNECTED INTERNAL TO THE PACKAGE.

9

General Description

The AD9630 is a monolithic buffer amplifier that utilizes innovative (patent pending) closed-loop design techniques to achieve exceptional gain accuracy, wide bandwidth, and low distortion. Slew rate limiting has been overcome as indicated by the 1200 V/μs slew rate; this improvement allows the user greater flexibility in wideband and pulse applications. The second harmonic distortion terms for an analog input tone of 4.3 MHz and 20 MHz are −80 dBc and −66 dBc, respectively. Clearly, the AD9630 establishes a new standard by combining in one part outstanding dc and dynamic performance.

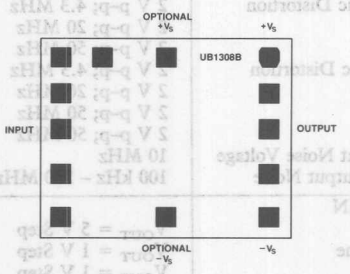
The large signal bandwidth, low distortion over frequency, and drive capabilities of the AD9630 make the buffer an ideal flash ADC driver. The AD9630 provides better signal fidelity than many of the flash ADCs that it has been designed to drive.

Other applications which require increased current drive at unity voltage gain such as cable driving benefit from the AD9630's performance.

The AD9630 is available in Plastic DIP (N), Ceramic DIP (Q), and SOIC (R). Consult with the factory concerning availability of MIL-STD-883 parts. Die are dc tested at +25°C.

DIE LAYOUT

Die Dimensions 60×50×15 mils



*Patent(s) Pending

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9630—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±7 V
Continuous Output Current[2] . . . . . 70 mA
Temperature Range over Which Specifications Apply
AD9630AN/AR/AQ . . . . . −40°C to +85°C
Lead Soldering Temperature (10 sec) . . . . . +300°C
Storage Temperature
AD9630AN/AR/AQ . . . . . −65°C to +150°C
Junction Temperature[3]
AD9630AN/AR/AQ . . . . . +150°C

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $\pm V_S = \pm 5$ V; $R_{IN} = 50\ \Omega$, $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9630AN/AR/AQ Min	Typ	Max	Units
DC SPECIFICATIONS							
Output Offset Voltage		+25°C	I	−8	±3	+8	mV
Offset Voltage TC		Full	IV	−40	±8	+40	µV/°C
Input Bias Current		+25°C	I	−25	±2	+25	µA
Bias Current TC		Full	IV	−100	±20	+100	nA/°C
Input Resistance		+25 to T_{max}	II	300	450		kΩ
Input Resistance		T_{min}	VI	150	250		kΩ
Input Capacitance		+25°C	V		1.0		pF
Gain	V_{OUT} = 2 V p-p	+25 to T_{max}	II	0.983	0.990		V/V
Gain	V_{OUT} = 2 V p-p	T_{min}	VI	0.980	0.985		V/V
Output Voltage Range		Full	VI	+3.2	±3.6	−3.2	V
Output Current (50 Ω Load)		+25 to T_{max}	II	50			mA
Output Current (50 Ω Load)		T_{min}	VI	40			mA
Output Impedance	At dc	+25°C	V		0.6		Ω
PSRR	$\Delta V_S = \pm 5\%$	Full	VI	44	55		dB
DC Nonlinearity	±2 V Full Scale	+25°C	V		0.03		%
FREQUENCY DOMAIN							
Bandwidth (−3 dB)							
Small Signal	$V_O \leq 0.7$ V p-p	T_{min} to 25	II	400	750		MHz
Small Signal	$V_O \leq 0.7$ V p-p	T_{max}	II	330	550		MHz
Large Signal	V_O = 5 V p-p	T_{min} to 25	V		120		MHz
Large Signal	V_O = 5 V p-p	T_{max}	V		105		MHz
Output Peaking	≤200 MHz	Full	II		0.4	1.2	dB
Output Rolloff	≤200 MHz	Full	II		0	0.3	dB
Group Delay	dc to 150 MHz	+25°C	V		0.7		ns
Linear Phase Deviation	dc to 150 MHz	+25°C	V		0.7		Degrees
2nd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV		−80	−73	dBc
	2 V p-p; 20 MHz	Full	IV		−66	−58	dBc
	2 V p-p; 50 MHz	Full	II		−52	−43	dBc
3rd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV		−86	−79	dBc
	2 V p-p; 20 MHz	Full	IV		−75	−68	dBc
	2 V p-p; 50 MHz	T_{min} to +25	II		−47	−41	dBc
	2 V p-p; 50 MHz	T_{max}	II		−46	−40	dBc
Spectral Input Noise Voltage	10 MHz	+25°C	V		2.4		nV/√Hz
Integrated Output Noise	100 kHz – 200 MHz	+25°C	V		32		µV
TIME DOMAIN							
Slew Rate	V_{OUT} = 5 V Step	+25°C	IV	700	1200		V/µs
Rise/Fall Time	V_{OUT} = 1 V Step	+25°C	IV		1.1	1.7	ns
	V_{OUT} = 1 V Step	T_{min} to T_{max}	IV		1.3	1.9	ns
	V_{OUT} = 5 V Step	+25°C	IV		4.2	5.7	ns
	V_{OUT} = 5 V Step	T_{min} to T_{max}	IV		5.0	6.5	ns
Overshoot Amplitude	V_{OUT} = 2 V Step	Full	IV		2	12	%
Settling Time							
To 0.1%	V_{OUT} = 2 V Step	T_{min} to +25	IV		6	10	ns
To 0.1%	V_{OUT} = 2 V Step	T_{max}	IV		7	12	ns
To 0.02%[4]	V_{OUT} = 2 V Step	T_{min} to +25	V		8		ns
To 0.02%[4]	V_{OUT} = 2 V Step	T_{max}	V		12		ns
Differential Gain	4.4 MHz	+25°C	V		0.015		%
Differential Phase	4.4 MHz	+25°C	V		0.025		Degree
SUPPLY CURRENTS							
V_{CC} ($+I_S$)	V_{CC} = +5 V	Full	II		19	26	mA
V_{EE} ($-I_S$)	V_{EE} = −5 V	Full	II		19	26	mA

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Output is short-circuit protected to ground, but not to supplies. Prolonged short circuit to ground may affect device reliability.
[3]Typical thermal impedances (part soldered onto board): Mini-DIP (N): θ_{JA} = 110°C/W; θ_{JC} = 30°C/W; SOIC (R): θ_{JA} = 150°C/W; θ_{JC} = 50°C/W; Cerdip (Q): θ_{JA} = 110°C/W; θ_{JC} = 20°C/W.
[4]Short-term settling with 50 Ω source impedance.

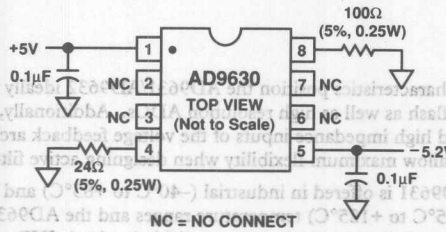
EXPLANATION OF TEST LEVELS

Test Level
- I 100% Production tested.
- II 100% Production tested at +25°C and sample tested at specified temperatures. AC testing of AN and AR grades done on sample basis only.
- III Sample tested only.
- IV Parameter is guaranteed by design and characterization testing.
- V Typical value.
- VI S versions are 100% production tested at temperature extremes. Other grades are sample tested at extremes.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9630AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD9630AR	−40°C to +85°C	8-Pin SOIC	R-8
AD9630AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD9630 Chips	+25°C	Dice	

*For outline information see Package Information section.



AD9630 Burn-In Circuit

THEORY OF OPERATION

The AD9630 is a wide-bandwidth, closed-loop, unity-gain buffer which makes use of a new voltage-feedback architecture (Patent Pending). This architecture brings together wide bandwidth and high slew rate along with exceptional dc linearity. Most previous wide bandwidth buffers achieved their bandwidth by utilizing an open-loop topology which sacrificed both dc linearity and frequency distortion when driven into low load impedances. The design's high loop correction factor radically improves dc linearity and distortion characteristics without diminishing bandwidth. This, in combination with high slew rate, results in exceptionally low distortion over a wide frequency range.

The AD9630 is an excellent choice to drive high speed and high resolution analog-to-digital Converters. Its output stage is designed to drive high speed flash converters with minimal or no series resistance. A current booster built into the output driver helps to maintain low distortion.

Parasitic or load capacitance (>7 pF) connected directly to the AD9630 output will result in frequency peaking. A small series resistor (R_S) connected between the buffer output and capacitive load will negate this effect. Figure 1 shows the optimal value of R_S as a function of C_L to obtain the flattest frequency response. Figure 2 illustrates frequency response for various capacitive loads utilizing the recommended R_S.

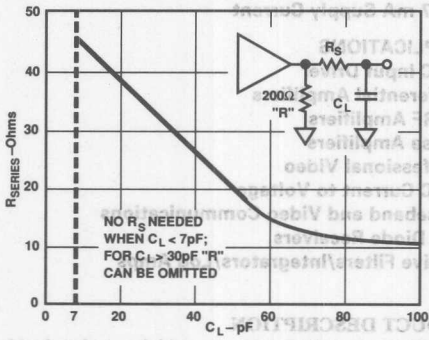


Figure 1. Recommended R_S vs. C_L

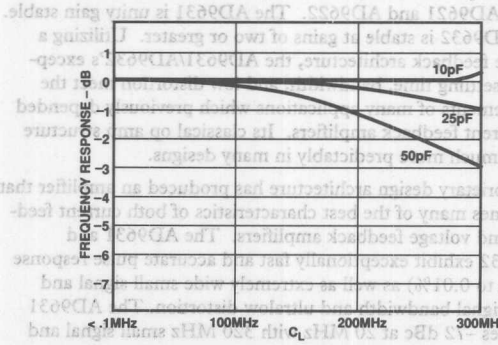


Figure 2. Frequency Response vs. C_L with Recommended R_S

In pulse mode applications, with R_S equal to approximately 12 ohms, capacitive loads of up to 50 pF can be driven with minimal settling time degradation.

FEATURES

Wide Bandwidth	**AD9631, G = +1**	**AD9632, G = +2**
Small Signal	**320 MHz**	**250 MHz**
Large Signal (4 V p-p)	**175 MHz**	**180 MHz**

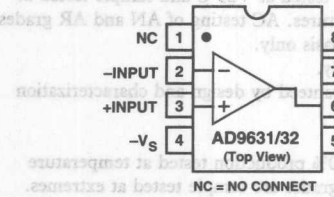
Ultralow Distortion (SFDR), Low Noise
–113 dBc typ @ 1 MHz
–95 dBc typ @ 5 MHz
–72 dBc typ @ 20 MHz
+46 dBc 3rd Order Intercept @ 25 MHz
7.0 nV/√Hz Spectral Noise Density
High Speed
Slew Rate 1300 V/μs
Settling 16 ns to 0.01%, 2 V Step
±3 V to ±5 V Supply Operation
17 mA Supply Current

APPLICATIONS

ADC Input Driver
Differential Amplifiers
IF/RF Amplifiers
Pulse Amplifiers
Professional Video
DAC Current to Voltage
Baseband and Video Communications
Pin Diode Receivers
Active Filters/Integrators/Log Amps

FUNCTIONAL BLOCK DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q), and SO (R) Packages



PRODUCT DESCRIPTION

The AD9631 and AD9632 are very high speed and wide bandwidth amplifiers. They are an improved performance alternative to the AD9621 and AD9622. The AD9631 is unity gain stable. The AD9632 is stable at gains of two or greater. Utilizing a voltage feedback architecture, the AD9631/AD9632's exceptional settling time, bandwidth, and low distortion meet the requirements of many applications which previously depended on current feedback amplifiers. Its classical op amp structure works much more predictably in many designs.

A proprietary design architecture has produced an amplifier that combines many of the best characteristics of both current feedback and voltage feedback amplifiers. The AD9631 and AD9632 exhibit exceptionally fast and accurate pulse response (16 ns to 0.01%) as well as extremely wide small signal and large signal bandwidth and ultralow distortion. The AD9631 achieves –72 dBc at 20 MHz with 320 MHz small signal and 175 MHz large signal bandwidths.

These characteristics position the AD9631/AD9632 ideally for driving flash as well as high resolution ADCs. Additionally, the balanced high impedance inputs of the voltage feedback architecture allow maximum flexibility when designing active filters.

The AD9631 is offered in industrial (–40°C to +85°C) and military (–55°C to +125°C) temperature ranges and the AD9632 in industrial. Industrial versions are available in plastic DIP and SOIC; MIL versions are packaged in cerdip.

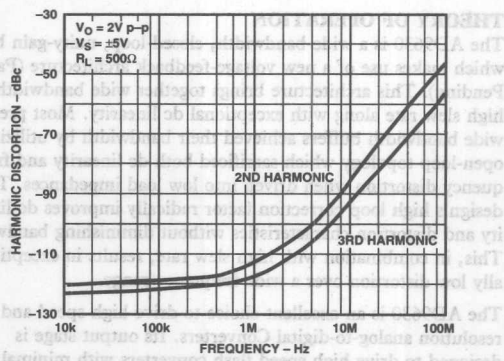


Figure 1. AD9631 Harmonic Distortion vs. Frequency, G = +1

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5$ V; $R_{LOAD} = 100\ \Omega$; $A_V = 1$ (AD9631); $A_V = 2$ (AD9632), unless otherwise noted)

Parameter	Conditions	AD9631A Min	AD9631A Typ	AD9631A Max	AD9632A Min	AD9632A Typ	AD9632A Max	Units
DYNAMIC PERFORMANCE								
Bandwidth (–3 dB)								
Small Signal	$V_{OUT} \le 0.4$ V p-p	220	320		180	250		MHz
Large Signal[1]	$V_{OUT} = 4$ V p-p	150	175		155	180		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT} = 300$ mV p-p							
	9631, $R_F = 140\ \Omega$; 9632, $R_F = 425\ \Omega$		130			130		MHz
Slew Rate, Average +/–	$V_{OUT} = 4$ V Step	1000	1300		1200	1500		V/µs
Rise/Fall Time	$V_{OUT} = 0.5$ V Step		1.2			1.4		ns
	$V_{OUT} = 4$ V Step		2.5			2.1		ns
Settling Time								
To 0.1%	$V_{OUT} = 2$ V Step		11			11		ns
To 0.01%	$V_{OUT} = 2$ V Step		16			16		ns
HARMONIC/NOISE PERFORMANCE								
2nd Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		–64	–57		–54	–47	dBc
	$R_L = 500\ \Omega$		–72	–65		–72	–65	dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		–76	–69		–74	–67	dBc
	$R_L = 500\ \Omega$		–81	–74		–81	–74	dBc
3rd Order Intercept	25 MHz		+46			+41		dBm
Noise Figure	$R_S = 50\ \Omega$		18			14		dB
Input Voltage Noise	1 MHz to 200 MHz		7.0			4.3		$nV\sqrt{Hz}$
Input Current Noise	1 MHz to 200 MHz		2.5			2.0		$pA\sqrt{Hz}$
Average Equivalent Integrated								
Input Noise Voltage	0.1 MHz to 200 MHz		100			60		µV rms
Differential Gain Error (3.58 MHz)	$R_L = 150\ \Omega$		0.03	0.06		0.02	0.04	%
Differential Phase Error (3.58 MHz)	$R_L = 150\ \Omega$		0.02	0.04		0.02	0.04	Degree
Phase Nonlinearity	dc to 100 MHz		1.1			1.1		Degree
DC PERFORMANCE[2], $R_L = 150\ \Omega$								
Input Offset Voltage[3]			3	10		2	5	mV
	T_{MIN}–T_{MAX}			13			8	mV
Offset Voltage Drift			±10			±10		µV/°C
Input Bias Current			2	7		2	7	µA
	T_{MIN}–T_{MAX}			10			10	µA
Input Offset Current			0.1	3		0.1	3	µA
	T_{MIN}–T_{MAX}			5			5	µA
Common-Mode Rejection Ratio	$V_{CM} = \pm 2.5$ V	70	90		70	90		dB
Open-Loop Gain	$V_{OUT} = \pm 2.5$ V	46	52		46	52		dB
	T_{MIN}–T_{MAX}	40			40			dB
INPUT CHARACTERISTICS								
Input Resistance			500			500		kΩ
Input Capacitance			1.2			1.2		pF
Input Common-Mode Voltage Range			±3.4			±3.4		V
OUTPUT CHARACTERISTICS								
Output Voltage Range, $R_L = 150\ \Omega$		±3.2	±3.9		±3.2	±3.9		V
Output Current			70			70		mA
Output Resistance			0.3			0.3		Ω
Short Circuit Current			240			240		mA
POWER SUPPLY								
Operating Range		±3.0	±5.0	±6.0	±3.0	±5.0	±6.0	V
Quiescent Current			17	18		16	17	mA
	T_{MIN}–T_{MAX}			21			20	mA
Power Supply Rejection Ratio	T_{MIN}–T_{MAX}	50	60		56	66		dB

NOTES
[1]See Max Ratings and Theory of Operation sections of data sheet.
[2]Measured at $A_V = 50$.
[3]Measured with respect to the inverting input.
Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	12.6 V
Voltage Swing × Bandwidth Product	550 V × MHz
Internal Power Dissipation[2]	
Plastic Package (N)	1.3 Watts
Small Outline Package (R)	0.9 Watts
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	±1.2 V
Output Short Circuit Duration	Observe Power Derating Curves
Storage Temperature Range N, R	–65°C to +125°C
Operating Temperature Range (A Grade)	–40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	+300°C

NOTES

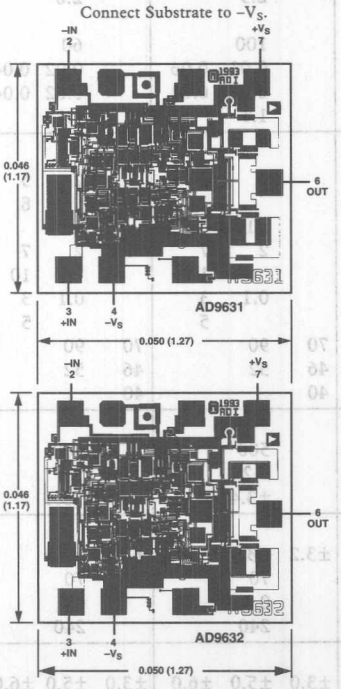
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Pin Plastic Package: θ_{JA} = 90°C/Watt
8-Pin SOIC Package: θ_{JA} = 140°C/Watt

METALIZATION PHOTO

Dimensions shown in inches and (mm).

Connect Substrate to $-V_S$.



MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by these devices is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD9631 and AD9632 are internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

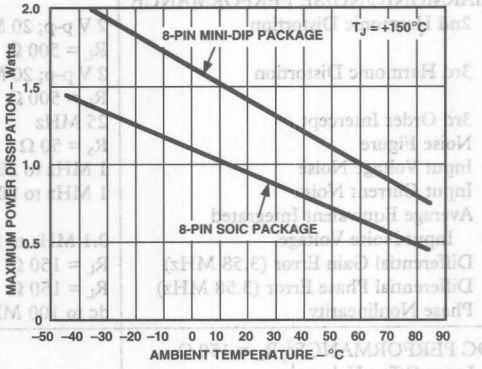


Figure 2. Plot of Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9631AN	–40C to +85°C	Plastic DIP	N-8
AD9631AR	–40°C to +85°C	SOIC	R-8
AD9631(SMD)	–55°C to +125°C	Cerdip	Q-8
AD9631-EB		Evaluation Board	
AD9632AN	–40°C to +85°C	Plastic DIP	N-8
AD9632AR	–40°C to +85°C	SOIC	R-8
AD9632-EB		Evaluation Board	

*N = Plastic DIP; Q = Cerdip; R= SOIC (Small Outline Integrated Circuit). For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

THEORY OF OPERATION

General

The AD9631 and AD9632 are wide bandwidth, voltage feedback amplifiers. Since their open-loop frequency response follows the conventional 6 dB/octave roll-off, their gain bandwidth product is basically constant. Increasing their closed-loop gain results in a corresponding decrease in small signal bandwidth. This can be observed by noting the bandwidth specification between the AD9631 (gain of 1) and AD9632 (gain of 2). The AD9631/AD9632 typically maintain 65 degrees of phase margin. This high margin minimizes the effects of signal and noise peaking.

Feedback Resistor Choice

The value of the feedback resistor is critical for optimum performance on the AD9631 (gain +1) and less critical as the gain increases. Therefore, this section is specifically targeted at the AD9631.

At minimum stable gain (+1), the AD9631 provides optimum dynamic performance with R_F = 140 Ω. This resistor acts only as a parasitic suppressor against damped RF oscillations that can occur due to lead (input, feedback) inductance and parasitic capacitance. This value of R_F provides the best combination of wide bandwidth, low parasitic peaking, and fast settling time.

In fact, for the same reasons, a 100–130 Ω resistor should be placed in series with the positive input for other AD9631 noninverting and all AD9631 inverting configurations. The correct connection is shown in Figures 57 and 58.

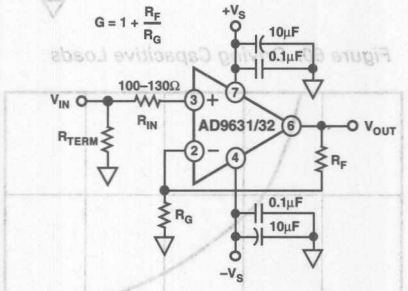


Figure 57. Noninverting Operation

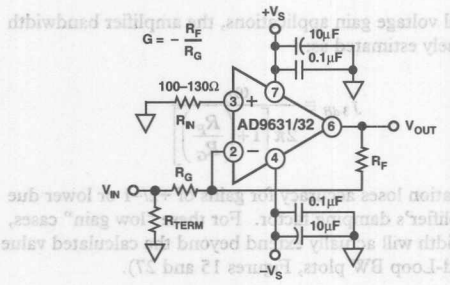


Figure 58. Inverting Operation

When the AD9631 is used in the transimpedance (I to V) mode, such as in photodiode detection, the value of R_F and diode capacitance (C_I) are usually known. Generally, the value of R_F selected will be in the kΩ range, and a shunt capacitor (C_F) across R_F will be required to maintain good amplifier stability. The value of C_F required to maintain optimal flatness (<1 dB Peaking) and settling time can be estimated as:

$$C_F \cong \left[(2\,\omega_O C_I R_F - 1)/\omega_O{}^2 R_F{}^2\right]^{1/2}$$

where ω_O is equal to the unity gain bandwidth product of the amplifier in rad/sec, and C_I is the equivalent total input capacitance at the inverting input. Typically $\omega_O = 800 \times 10^6$ rad/sec (see Open-Loop Frequency Response curve (Figure 17).

As an example, choosing R_F = 10 kΩ and C_I = 5 pF, requires C_F to be 1.1 pF (Note: C_I includes both source and parasitic circuit capacitance). The bandwidth of the amplifier can be estimated using the C_F calculated as:

$$f_{3\,dB} \cong \frac{1.6}{2\pi R_F C_F}$$

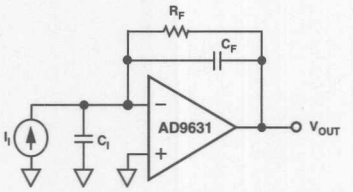


Figure 59. Transimpedance Configuration

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$$f_{3\,dB} \cong \frac{\omega_O}{2\pi\left[1+\left(\frac{R_F}{R_G}\right)\right]}$$

This estimation loses accuracy for gains of +2/–1 or lower due to the amplifier's damping factor. For these "low gain" cases, the bandwidth will actually extend beyond the calculated value (see Closed-Loop BW plots, Figures 15 and 27).

As a rule of thumb, capacitor C_F will not be required if:

$$(R_F \| R_G) \times C_I \leq \frac{NG}{4\,\omega_O}$$

where *NG* is the Noise Gain ($1 + R_F/R_G$) of the circuit. For most voltage gain applications, this should be the case.

Pulse Response

Unlike a traditional voltage feedback amplifier, where the slew speed is dictated by its front end dc quiescent current and gain bandwidth product, the AD9631 and AD9632 provide "on demand" current that increases proportionally to the input "step" signal amplitude. This results in slew rates (1300 V/µs) comparable to wideband current feedback designs. This, combined with relatively low input noise current (2.0 pA/$\sqrt{\text{Hz}}$), gives the AD9631 and AD9632 the best attributes of both voltage and current feedback amplifiers.

Large Signal Performance

The outstanding large signal operation of the AD9631 and AD9632 is due to a unique, proprietary design architecture. In order to maintain this level of performance, the maximum 550 V-MHz product must be observed, (e.g., @ 100 MHz, $V_O \leq 5.5$ V p-p).

the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 µF) will be required to provide the best settling time and lowest distortion. A parallel combination of at least 4.7 µF, and between 0.1 µF and 0.01 µF, is recommended. Some brands of electrolytic capacitors will require a small series damping resistor ≈4.7 Ω for optimum results.

Driving Capacitive Loads

The AD9631 and AD9632 were designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, the best frequency response is obtained by the addition of a small series resistance as shown in Figure 60. The accompanying graph shows the optimum value for R_{SERIES} vs. capacitive load. It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of R_{SERIES} and C_L.

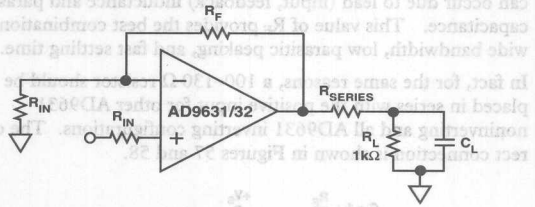


Figure 60. Driving Capacitive Loads

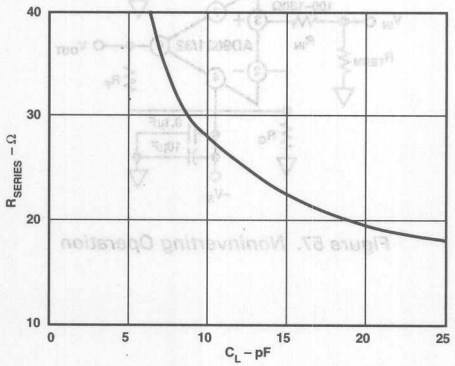


Figure 61. Recommended R_{SERIES} vs. Capacitive Load

Improved Second Source to the EL2020

ADEL2020

FEATURES

Ideal for Video Applications
- 0.02% Differential Gain
- 0.04° Differential Phase
- 0.1 dB Bandwidth to 25 MHz (G = +2)

High Speed
- 90 MHz Bandwidth (−3 dB)
- 500 V/µs Slew Rate
- 60 ns Settling Time to 0.1% (V_O = 10 V Step)

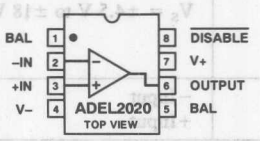
Low Noise
- 2.9 nV/√Hz Input Voltage Noise

Low Power
- 6.8 mA Supply Current
- 2.1 mA Supply Current (Power-Down Mode)

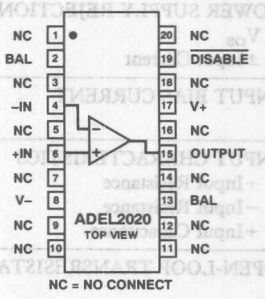
High Performance Disable Function
- Turn-Off Time of 100 ns
- Input to Output Isolation of 54 dB (Off State)

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N)



20-Pin Small Outline Package



NC = NO CONNECT

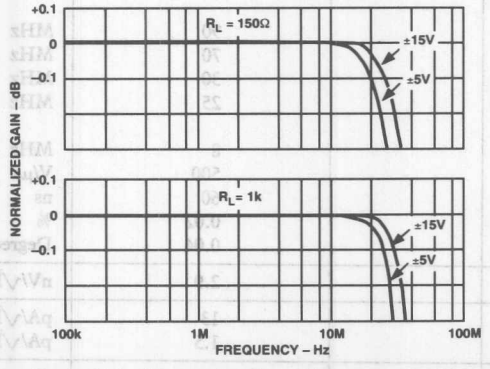
9

PRODUCT DESCRIPTION

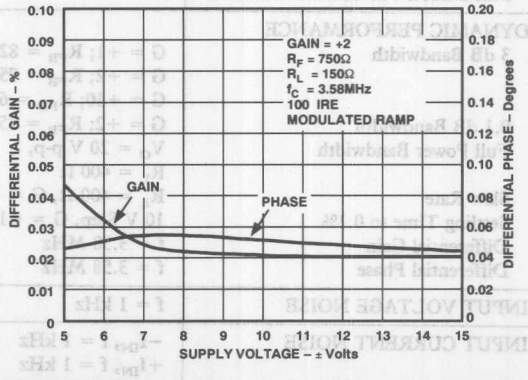
The ADEL2020 is an improved second source to the EL2020. This op amp improves on all the key dynamic specifications while offering lower power and lower cost. The ADEL2020 offers 50% more bandwidth and gain flatness of 0.1 dB to beyond 25 MHz. In addition, differential gain and phase are less than 0.05% and 0.05° while driving one back terminated cable (150 Ω).

The ADEL2020 offers other significant improvements. The most important of these is lower power supply current, 33% less than the competition while offering higher output drive. Important specs like voltage noise and offset voltage are less than half of those for the EL2020.

The ADEL2020 also features an improved disable feature. The disable time (to high output impedance) is 100 ns with guaranteed break before make. Finally the ADEL2020 is offered in the industrial temperature range of −40°C to +85°C in both plastic DIP and SOIC package.



Fine-Scale Gain (Normalized) vs. Frequency for Various Supply Voltages. R_F = 750 Ω, Gain = +2



Differential Gain and Phase vs. Supply Voltage

ADEL2020—SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, R_L = 150 Ω unless otherwise noted)

Parameter	Conditions	Temperature	ADEL2020A Min	Typ	Max	Units
INPUT OFFSET VOLTAGE				1.5	7.5	mV
		T_{MIN}–T_{MAX}		2.0	10.0	mV
Offset Voltage Drift				7		µV/°C
COMMON-MODE REJECTION	V_{CM} = ±10 V					
V_{OS}		T_{MIN}–T_{MAX}	50	64		dB
±Input Current		T_{MIN}–T_{MAX}		0.1	1.0	µA/V
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V					
V_{OS}		T_{MIN}–T_{MAX}	65	72		dB
±Input Current		T_{MIN}–T_{MAX}		0.05	0.5	µA/V
INPUT BIAS CURRENT	−Input	T_{MIN}–T_{MAX}		0.5	7.5	µA
	+Input	T_{MIN}–T_{MAX}		1	15	µA
INPUT CHARACTERISTICS						
+Input Resistance			1	10		MΩ
−Input Resistance				40		Ω
+Input Capacitance				2		pF
OPEN-LOOP TRANSRESISTANCE	V_O = ±10 V					
	R_L = 400 Ω	T_{MIN}–T_{MAX}	1	3.5		MΩ
OPEN-LOOP DC VOLTAGE GAIN	R_L = 400 Ω, V_{OUT} = ±10 V	T_{MIN}–T_{MAX}	80	100		dB
	R_L = 100 Ω, V_{OUT} = ±2.5 V	T_{MIN}–T_{MAX}	76	88		dB
OUTPUT VOLTAGE SWING	R_L = 400 Ω	T_{MIN}–T_{MAX}	±12.0	±13.0		V
Short-Circuit Current				150		mA
Output Current		T_{MIN}–T_{MAX}	30	60		mA
POWER SUPPLY						
Operating Range			±3.0		±18	V
Quiescent Current		T_{MIN}–T_{MAX}		6.8	10.0	mA
Power-Down Current		T_{MIN}–T_{MAX}		2.1	3.0	mA
Disable Pin Current	Disable Pin = 0 V	T_{MIN}–T_{MAX}		290	400	µA
Min Disable Pin Current to Disable		T_{MIN}–T_{MAX}		30		µA
DYNAMIC PERFORMANCE						
3 dB Bandwidth	G = +1; R_{FB} = 820			90		MHz
	G = +2; R_{FB} = 750			70		MHz
	G = +10; R_{FB} = 680			30		MHz
0.1 dB Bandwidth	G = +2; R_{FB} = 750			25		MHz
Full Power Bandwidth	V_O = 20 V p-p, R_L = 400 Ω			8		MHz
Slew Rate	R_L = 400 Ω, G = +1			500		V/µs
Settling Time to 0.1%	10 V Step, G = −1			60		ns
Differential Gain	f = 3.58 MHz			0.02		%
Differential Phase	f = 3.58 MHz			0.04		Degree
INPUT VOLTAGE NOISE	f = 1 kHz			2.9		nV/√Hz
INPUT CURRENT NOISE	$-I_{IN}$, f = 1 kHz			13		pA/√Hz
	$+I_{IN}$, f = 1 kHz			1.5		pA/√Hz
OUTPUT RESISTANCE	Open Loop (5 MHz)			15		Ω

Specifications subject to change without notice.

Internal Power Dissipation[2] . . . . . Observe Derating Curves
Output Short Circuit Duration . . . . . Observe Derating Curves
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
Plastic DIP and SOIC . . . . . −65°C to +125°C
Operating Temperature Range . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

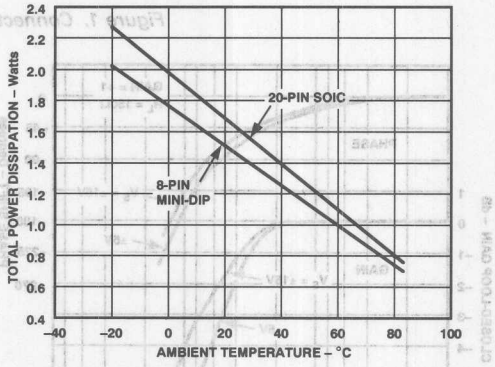
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 90°C/Watt
20-Pin SOIC Package: θ_{JA} = 150°C/Watt

ESD SUSCEPTIBILITY

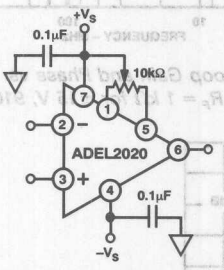
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the ADEL2020 features ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

ADEL2020 is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 145°C. If the maximum is exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the "overheated" condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves below.

While the ADEL2020 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions.



Maximum Power Dissipation vs. Temperature



Offset Null Configuration

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
ADEL2020AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
ADEL2020AR-20	−40°C to +85°C	20-Pin Plastic SOIC	R-20
ADEL2020AR-20-REEL	−40°C to +85°C	20-Pin Plastic SOIC	R-20

*For outline information see Package Information section.

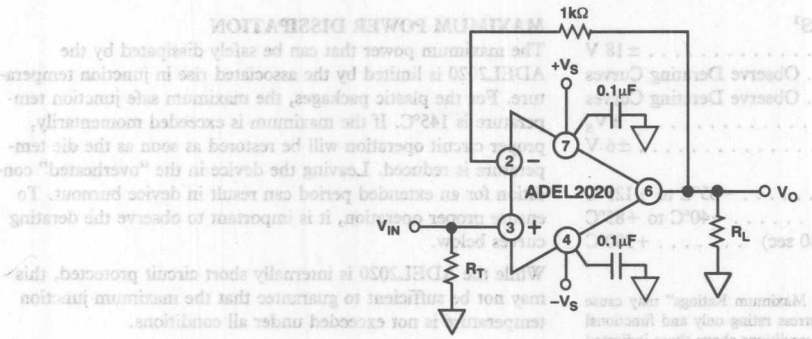


Figure 1. Connection Diagram for A_{VCL} = +1

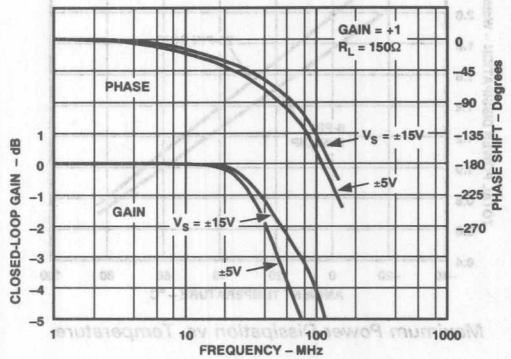


Figure 2. Closed-Loop Gain and Phase vs. Frequency, G = +1, R_L = 150 Ω, R_F = 1 kΩ for ±15 V, 910 Ω for ±5 V

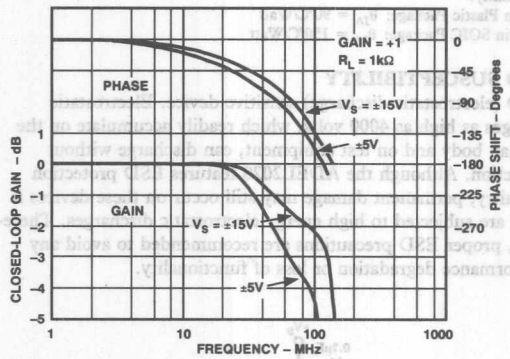


Figure 3. Closed-Loop Gain and Phase vs. Frequency, G = +1, R_L = 1 kΩ, R_F = 1 kΩ for ±15 V, 910 Ω for ±5 V

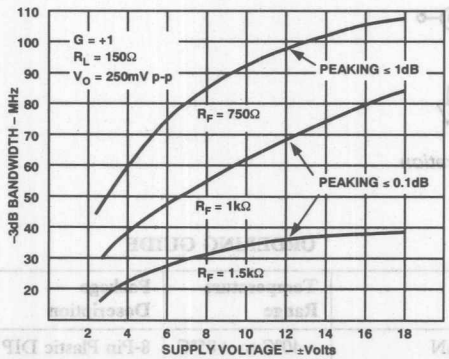


Figure 4. –3 dB Bandwidth vs. Supply Voltage, Gain = +1, R_L = 150 Ω

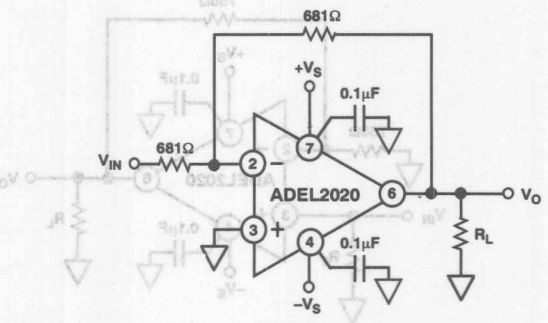


Figure 5. Connection Diagram for $A_{VCL} = -1$

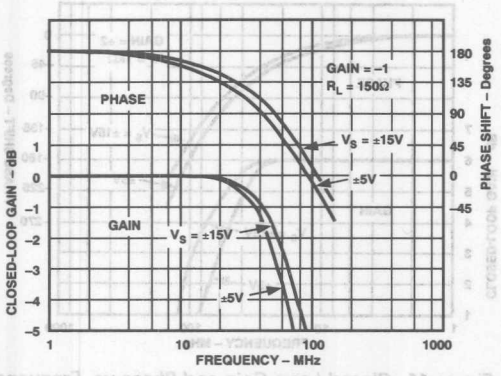


Figure 6. Closed-Loop Gain and Phase vs. Frequency, $G = -1$, $R_L = 150\ \Omega$, $R_F = 680\ \Omega$ for ±15 V, 620 Ω for ±5 V

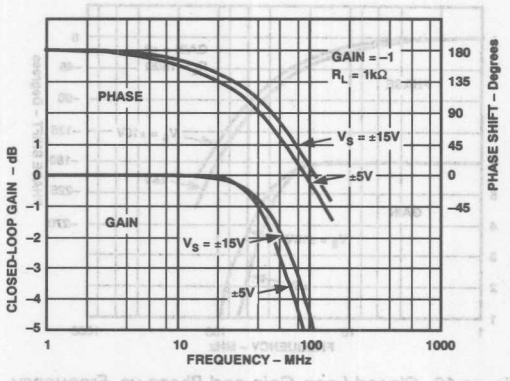


Figure 7. Closed-Loop Gain and Phase vs. Frequency, $G = -1$, $R_L = 1\ k\Omega$, $R_F = 680\ \Omega$ for $V_S = \pm 15$ V, 620 Ω for ±5 V

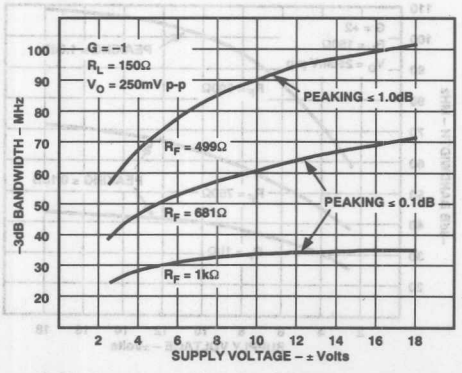


Figure 8. –3 dB Bandwidth vs. Supply Voltage, Gain = –1, $R_L = 150\ \Omega$

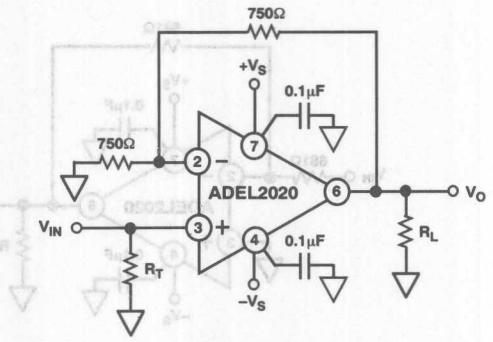


Figure 9. Connection Diagram for A_{VCL} = +2

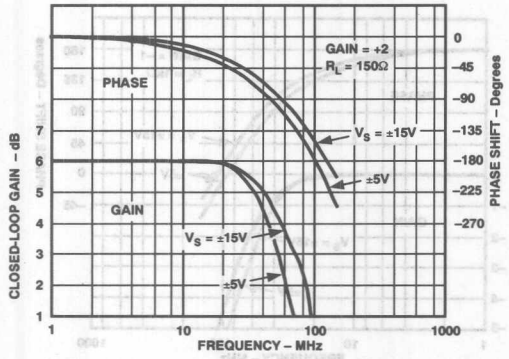


Figure 10. Closed-Loop Gain and Phase vs. Frequency, G = +2, R_L = 150 Ω, R_F = 750 Ω for ±15 V, 715 Ω for ±5 V

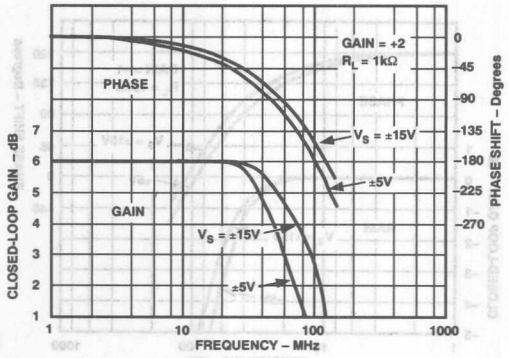


Figure 11. Closed-Loop Gain and Phase vs. Frequency, G = +2, R_L = 1 kΩ, R_F = 750 Ω for ±15 V, 715 Ω for ±5 V

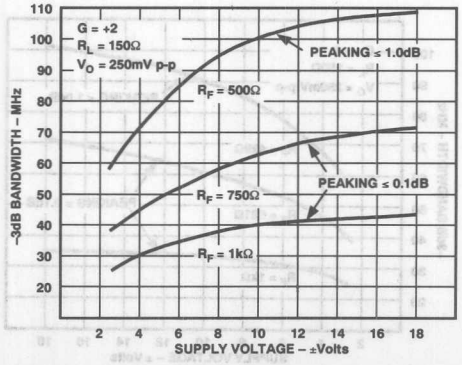


Figure 12. –3 dB Bandwidth vs. Supply Voltage, Gain = +2, R_L = 150 Ω

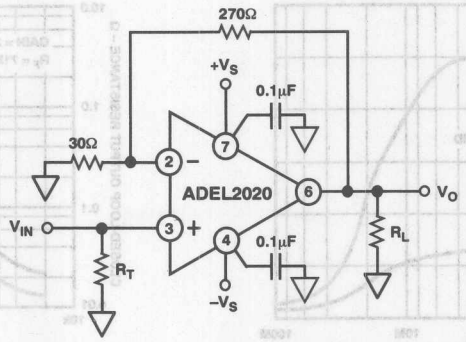


Figure 13. Connection Diagram for A_{VCL} = +10

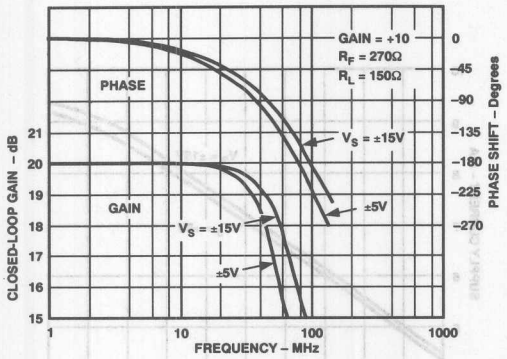


Figure 14. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 150 kΩ

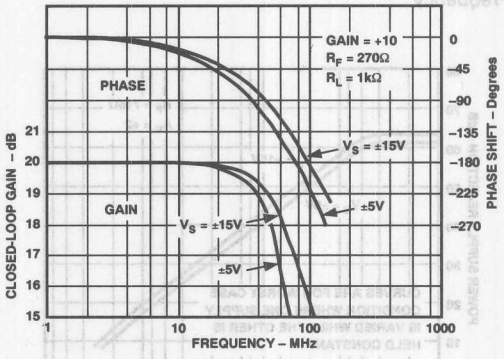


Figure 15. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 1 kΩ

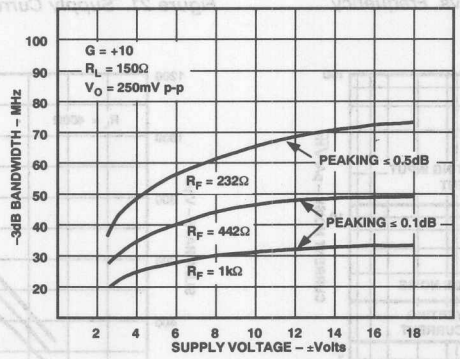


Figure 16. –3 dB Bandwidth vs. Supply Voltage, Gain = +10, R_L = 150 Ω

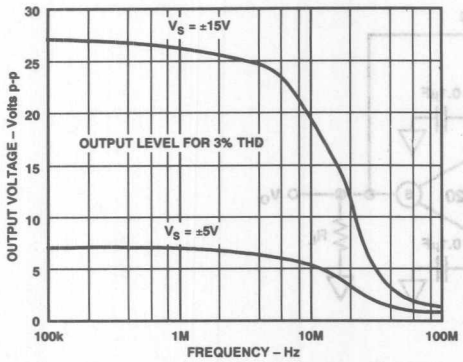


Figure 17. Maximum Undistorted Output Voltage vs. Frequency

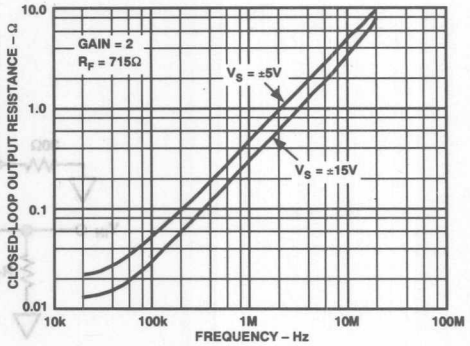


Figure 20. Closed-Loop Output Resistance vs. Frequency

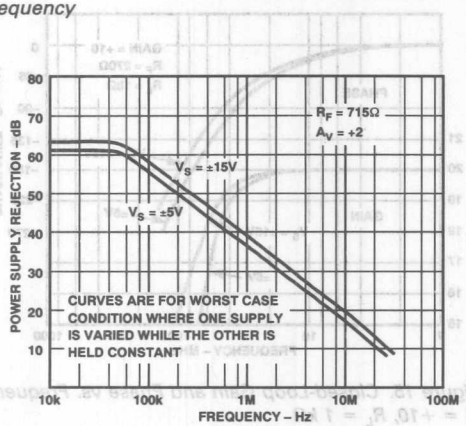


Figure 18. Power Supply Rejection vs. Frequency

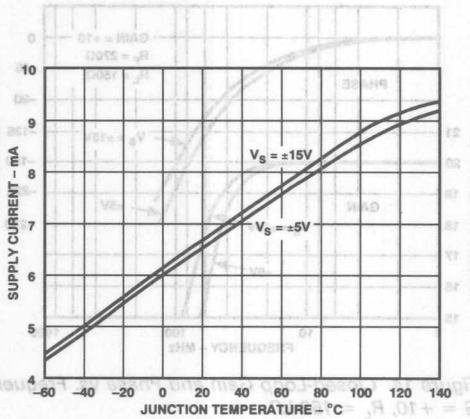


Figure 21. Supply Current vs. Junction Temperature

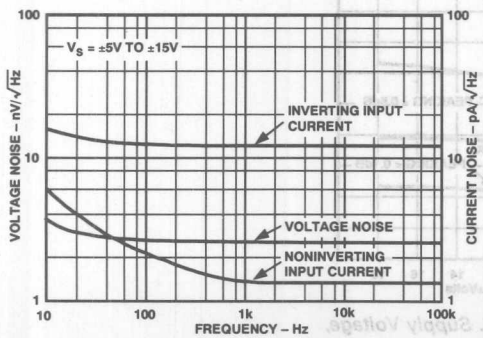


Figure 19. Input Voltage and Current Noise vs. Frequency

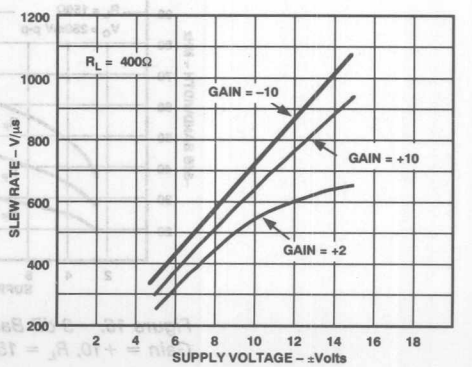


Figure 22. Slew Rate vs. Supply Voltage

GENERAL DESIGN CONSIDERATIONS

The ADEL2020 is a current feedback amplifier optimized for use in high performance video and data acquisition systems. Since it uses a current feedback architecture, its closed-loop bandwidth depends on the value of the feedback resistor. The −3 dB bandwidth is also somewhat dependent on the power supply voltage. Lowering the supplies increases the values of internal capacitances, reducing the bandwidth. To compensate for this, smaller values of feedback resistor are used at lower supply voltages.

POWER SUPPLY BYPASSING

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can contribute to resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 μF) will be required to provide the best settling time and lowest distortion. Although the recommended 0.1 μF power supply bypass capacitors will be sufficient in most applications, more elaborate bypassing (such as using two paralleled capacitors) may be required in some cases.

CAPACITIVE LOADS

When used with the appropriate feedback resistor, the ADEL2020 can drive capacitive loads exceeding 1000 pF directly without oscillation. Another method of compensating for large load capacitance is to insert a resistor in series with the loop output. In most cases, less than 50 Ω is all that is needed to achieve an extremely flat gain response.

OFFSET NULLING

A 10 kΩ pot connected between Pins 1 and 5, with its wiper connected to V+, can be used to trim out the inverting input current (with about ±20 μA of range). For closed-loop gains above about 5, this may not be sufficient to trim the output offset voltage to zero. Tie the pot's wiper to ground through a large value resistor (50 kΩ for ±5 V supplies, 150 kΩ for ±15 V supplies) to trim the output to zero at high closed-loop gains.

OPERATION AS A VIDEO LINE DRIVER

The ADEL2020 is designed to offer outstanding performance at closed-loop gains of one or greater. At a gain of 2, the ADEL2020 makes an excellent video line driver. The low differential gain and phase errors and wide −0.1 dB bandwidth are nearly independent of supply voltage and load. For applications requiring widest 0.1 dB bandwidth, it is recommended to use 715 Ω feedback and gain resistors. This will result in about 0.05 dB of peaking and a −0.1 dB bandwidth of 30 MHz on ±15 V supplies.

DISABLE MODE

By pulling the voltage on Pin 8 to common (0 V), the ADEL2020 can be put into a disabled state. In this condition, the supply current drops to less than 2.8 mA, the output becomes a high impedance, and there is a high level of isolation from input to output. In the case of a line driver for example, the output impedance will be about the same as for a 1.5 kΩ resistor (the feedback plus gain resistors) in parallel with a 13 pF capacitor (due to the output) and the input to output isolation will be better than 50 dB at 10 MHz.

Leaving the disable pin disconnected (floating) will leave the part in the enabled state.

In cases where the amplifier is driving a high impedance load, the input to output isolation will decrease significantly if the input signal is greater than about 1.2 V peak to peak. The isolation can be restored to the 50 dB level by adding a dummy load (say 150 Ω) at the amplifier output. This will attenuate the feedthrough signal. (This is not an issue for multiplexer applications where the outputs of multiple ADEL2020s are tied together as long as at least one channel is in the ON state.) The input impedance of the disable pin is about 35 kΩ in parallel with a few pF. When grounded, about 50 μA flows out of the disable pin for ±5 V supplies.

Break before make operation is guaranteed by design. If driven by standard CMOS logic, the disable time (until the output is high impedance), is about 100 ns and the enable time (to low impedance output) is about 160 ns. Since it has an internal pull-up resistor of about 35 kΩ, the ADEL2020 can be used with open drain logic as well. In this case, the enable time is increased to about 1 μs.

If there is a nonzero voltage present on the amplifier's output at the time it is switched to the disabled state, some additional decay time will be required for the output voltage to relax to zero. The total time for the output to go to zero will generally be about 250 ns and is somewhat dependent on the load impedance.

Closed-Loop High Speed Buffer

BUF04*

FEATURES

Bandwidth – 110 MHz
Slew Rate – 3000 V/μs
Low Offset Voltage – < 1 mV
Very Low Noise – < 4 nV/√Hz
Low Supply Current – 8.5 mA Max
Wide Supply Range – ±5 to ±15 V
Drives Capacitive Loads
Pin Compatible with BUF03

APPLICATIONS

Instrumentation Buffer
RF Buffer
Line Driver
High Speed Current Source
Op Amp Output Current Booster
High Performance Audio
High Speed AD/DA

GENERAL DESCRIPTION

The BUF04 is a wideband, closed-loop buffer that combines state of the art dynamic performance with excellent dc performance. This combination enables designers to maximize system performance without any speed versus dc accuracy compromises.

Built on a high speed Complementary Bipolar (CB) process for better power performance ratio, the BUF04 consumes less than 8.5 mA operating from ±5 V or ±15 V supplies. With a 2000 V/μs min slew rate, and 100 MHz gain bandwidth product, the BUF04 is ideally suited for use in high speed applications where low power dissipation is critical.

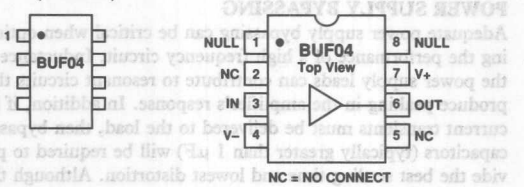
Full ±10 V output swing over the extended temperature range along with outstanding ac performance and high loop gain accuracy makes the device useful in high speed data acquisition systems.

*Patent pending.

FUNCTIONAL BLOCK DIAGRAM

8-Lead Narrow-Body SO
(S Suffix)

Plastic DIP
8-Lead and Cerdip
(P, Z Suffix)



High slew rate and very low noise and THD, coupled with wide input and output dynamic range, make the BUF04 an excellent choice for video and high performance audio circuits.

The BUF04's inherent ability to drive capacitive loads over a wide voltage and temperature range makes it extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The BUF04 is specified over the extended industrial (−40°C to +85°C) and military (−55°C to +125°C) temperature range. BUF04s are available in plastic and ceramic DIP plus SO-8 surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 , T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.3	1	mV
		−40°C ≤ T_A ≤ +85°C		1.3	4	mV
Input Bias Current	I_B	V_{CM} = 0		0.7	5	µA
		−40°C ≤ T_A ≤ +85°C		2.2	10	µA
Input Voltage Range	V_{CM}			±13		V
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			30		µV/°C
Offset Null Range				±25		mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 150 Ω,	±10.5	±11.1		V
		−40°C ≤ T_A ≤ +85°C	±10	±11		V
		R_L = 2 kΩ,	±13	±13.5		V
		−40°C ≤ T_A ≤ +85°C	±13	±13.15		V
Output Current − Continuous	I_{OUT}		±50	±65		mA
Peak Output Current	I_{OUTP}	Note 2		±80		mA
TRANSFER CHARACTERISTICS						
Gain	A_{VCL}	R_L = 2 kΩ	0.995	0.9985	1.005	V/V
		−40°C ≤ T_A ≤ +85°C	0.995	0.9980	1.005	V/V
Gain Linearity	NL	R_L = 1 kΩ, V_O = ±10 V		0.005		%
		R_L = 150 kΩ		0.008		%
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	76	93		dB
		−40°C ≤ T_A ≤ +85°C	76	93		dB
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞		6.9	8.5	mA
		−40°C ≤ T_A ≤ +85°C		6.9	8.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 70 pF	2000	3000		V/µs
Bandwidth	BW	−3 dB, C_L = 20 pF, R_L = ∞		110		MHz
Bandwidth	BW	−3 dB, C_L = 20 pF, R_L = 1 kΩ		110		MHz
Bandwidth	BW	−3 dB, C_L = 20 pF, R_L = 150 Ω		110		MHz
Settling Time		V_{IN} = ±10 V Step to 0.1%		60		ns
Differential Phase		f = 3.58 MHz, R_L = 150 Ω		0.02		Degrees
		f = 4.43 MHz, R_L = 150 Ω		0.03		Degrees
Differential Gain		f = 3.58 MHz, R_L = 150 Ω		0.014		%
		f = 4.43 MHz, R_L = 150 Ω		0.008		%
Input Capacitance				3		pF
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		4		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		2		pA/√Hz

NOTE

[1]Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125°C, with an LTPD of 1.3.

Specifications subject to change without notice.

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ELECTRICAL CHARACTERISTICS (@ V_S = ±5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.8	2.0	mV
		$-40°C \le T_A \le +85°C$		1.0	4	mV
Input Bias Current	I_B	V_{CM} = 0 V		0.15	5	µA
		$-40°C \le T_A \le +85°C$		1.6	10	µA
Input Voltage Range	V_{CM}			±3.0		V
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			30		µV/°C
Offset Null Range				±25		mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 150 Ω,	±3.0			V
		$-40°C \le T_A \le +85°C$	±2.75	±3.00		V
		R_L = 2 kΩ,	±3.0	±3.6		V
		$-40°C \le T_A \le +85°C$	±3.0	±3.35		V
Output Current – Continuous	I_{OUT}		±40			mA
Peak Output Current	I_{OUTP}	Note 2		±75		mA
TRANSFER CHARACTERISTICS						
Gain	A_{VCL}	R_L = 2 kΩ,	0.995	0.9977	1.005	V/V
		$-40°C \le T_A \le +85°C$	0.995		1.005	V/V
Gain Linearity	NL	R_L = 1 kΩ		0.005		%
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	76	93		dB
		$-40°C \le T_A \le +85°C$	76	93		dB
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞		6.60	8	mA
		$-40°C \le T_A \le +85°C$		6.70	8	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 70 pF		2000		V/µs
Bandwidth	BW	−3 dB, C_L = 20 pF, R_L = ∞		100		MHz
Bandwidth	BW	−3 dB, C_L = 20 pF, R_L = 1 kΩ		100		MHz
Bandwidth	BW	−3 dB, C_L = 20 pF, R_L = 150 Ω		100		MHz
Differential Phase		f = 3.58 MHz, R_L = 150 Ω		0.13		Degrees
		f = 4.43 MHz, R_L = 150 Ω		0.15		Degrees
Differential Gain		f = 3.58 MHz, R_L = 150 Ω		0.04		%
		f = 4.43 MHz, R_L = 150 Ω		0.06		%
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		4		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		2		pA/√Hz

NOTE

[1]Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125°C, with an LTPD of 1.3.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}	V_S = ±15 V	1	mV max
	V_{OS}	V_S = ±5 V	2	mV max
Input Bias Current	I_B	V_{CM} = 0 V	5	µA max
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	76	dB
Output Voltage Range	V_O	R_L = 150 Ω	±10.5	V min
Supply Current	I_{SY}	V_O = 0 V, R_L = 2 kΩ	8.5	mA max
Gain	AV_{CL}	V_O = ±10 V, R_L = 2 kΩ	1 ± 0.005	V/V

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage . . . . . ±18 V
Maximum Power Dissipation . . . . . See Figure 16
Storage Temperature Range
Z Package . . . . . −65°C to +175°C
P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
BUF04Z . . . . . −55°C to +125°C
BUF04S, P . . . . . −40°C to +85°C
Junction Temperature Range
Z Package . . . . . −65°C to +150°C
P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

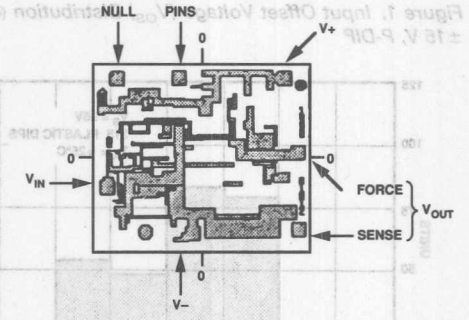
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

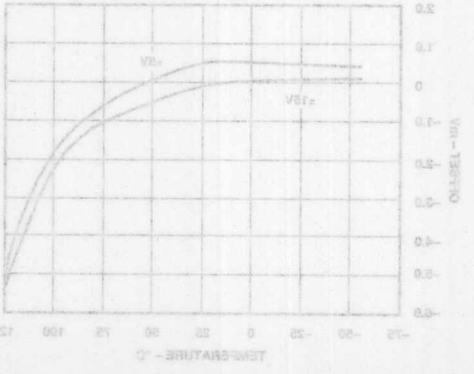
Model	Temperature Range	Package Description	Package Option*
BUF04AZ/883	−55°C to +125°C	Cerdip	Q-8
BUF04GP	−40°C to +85°C	Plastic DIP	N-8
BUF04GS	−40°C to +85°C	SO	SO-8
BUF04GBC	+25°C	DICE	DICE

*For outline information see Package Information section.

DICE CHARACTERISTICS



BUF04 Die Size 0.075 × 0.064 inch, 5,280 Sq. Mils
Substrate (Die Backside) Is Connected to V+
Transistor Count 45.



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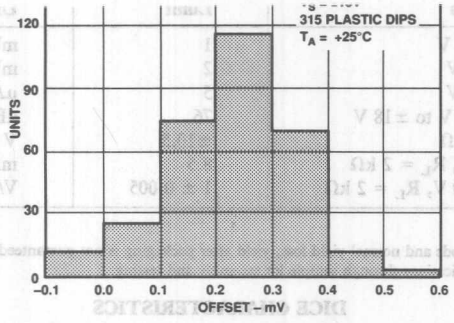


Figure 1. Input Offset Voltage (V_{OS}) Distribution @ ±15 V, P-DIP

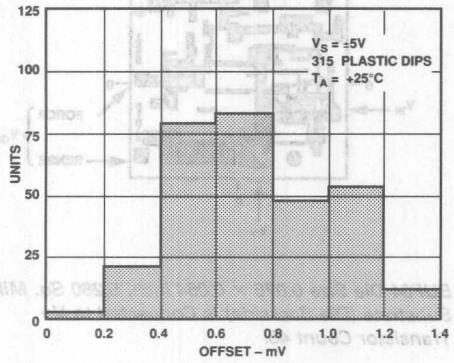


Figure 2. Input Offset Voltage (V_{OS}) Distribution @ ±5 V, P-DIP

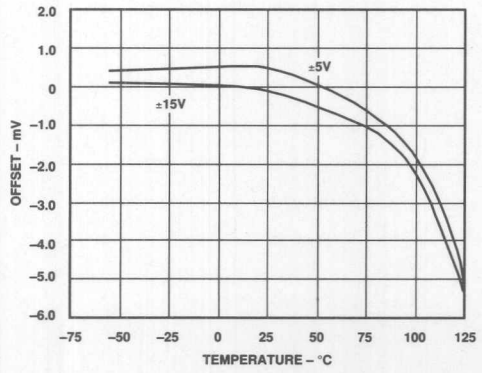


Figure 3. Input Offset Voltage (V_{OS}) vs. Temperature

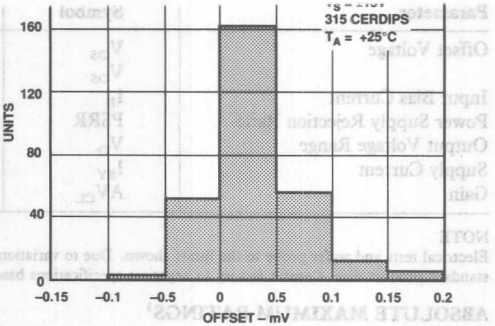


Figure 4. Input Offset Voltage (V_{OS}) Distribution @ ±15 V, Cerdip

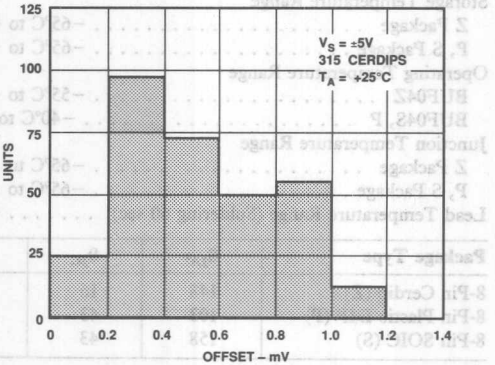


Figure 5. Input Offset Voltage (V_{OS}) Distribution @ ±5 V, Cerdip

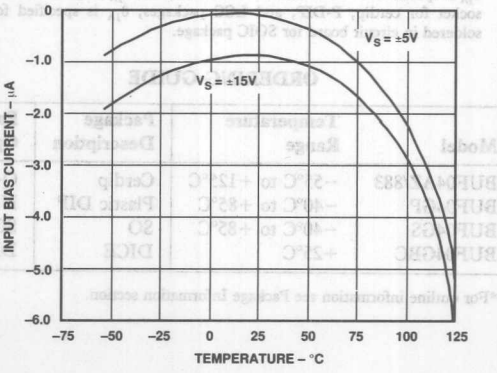


Figure 6. Input Bias Current vs. Temperature

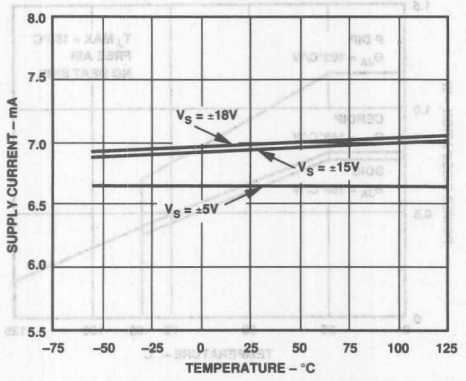


Figure 7. Supply Current vs. Temperature

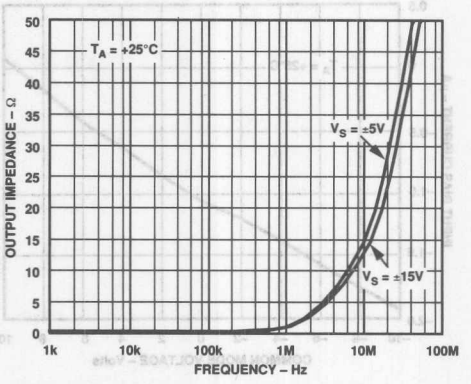


Figure 10. Output Impedance vs. Frequency

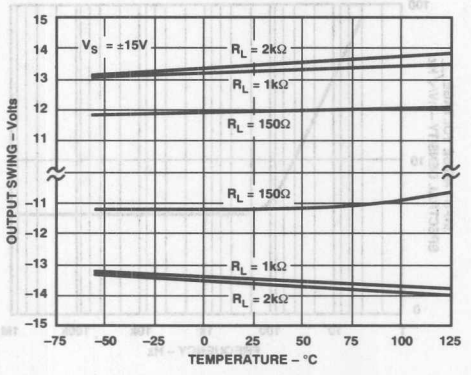


Figure 8. Output Voltage Swing vs. Temperature @ ±15 V

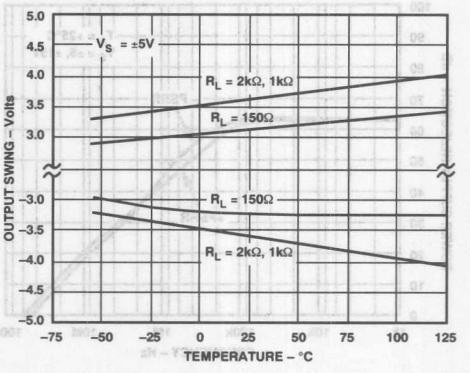


Figure 11. Output Voltage Swing vs. Temperature @ ±5 V

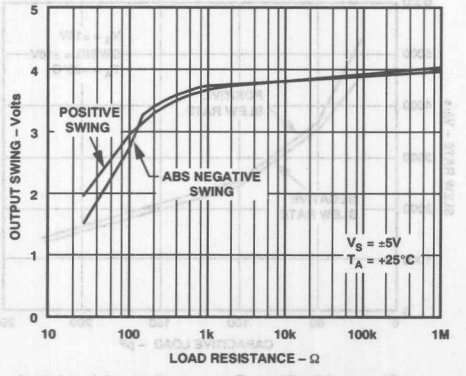


Figure 9. Maximum V_{OUT} Swing vs. Load @ ±5 V

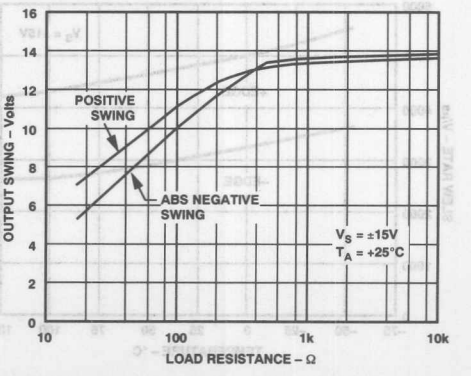


Figure 12. Maximum V_{OUT} Swing vs. Load @ ±15 V

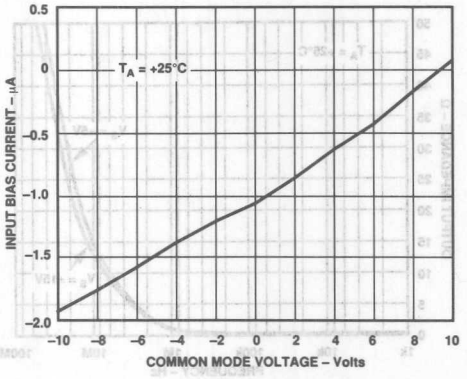


Figure 13. Bias Current vs. Input Voltage

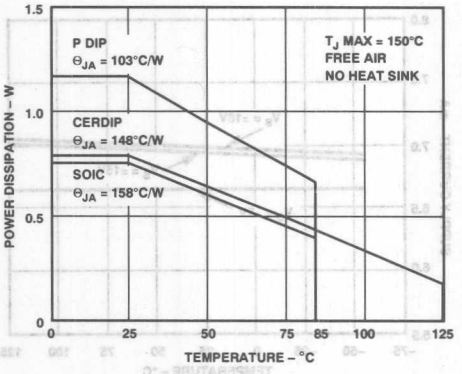


Figure 16. Maximum Power Dissipation vs. Ambient Temperature

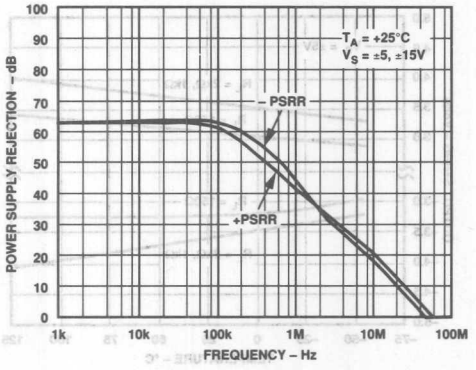


Figure 14. Power Supply Rejection vs. Frequency

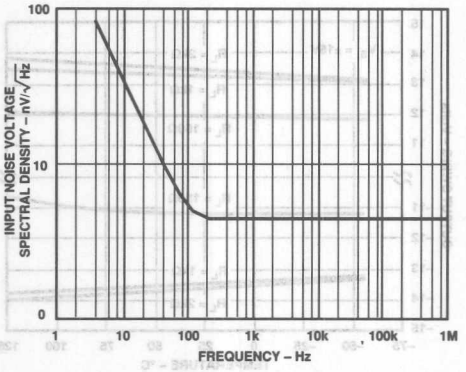


Figure 17. Input Noise Voltage vs. Frequency

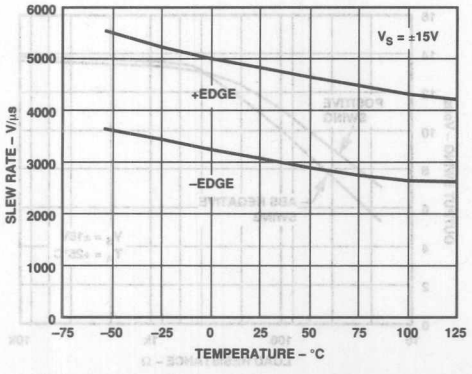


Figure 15. Slew Rate vs. Temperature

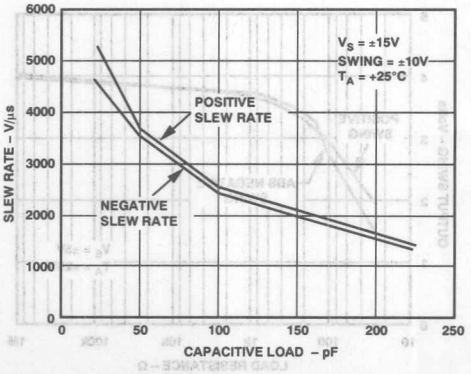


Figure 18. Slew Rate vs. Capacitive Loads

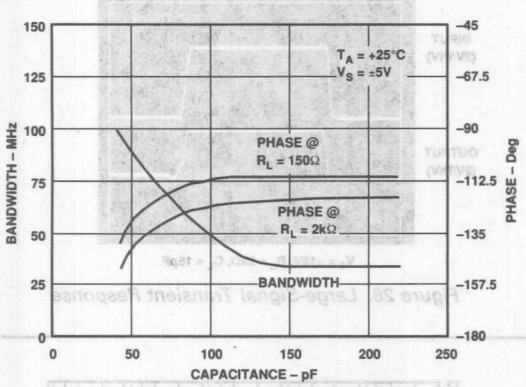


Figure 19. Bandwidth and Phase vs. Capacitive Loads @ ±5 V

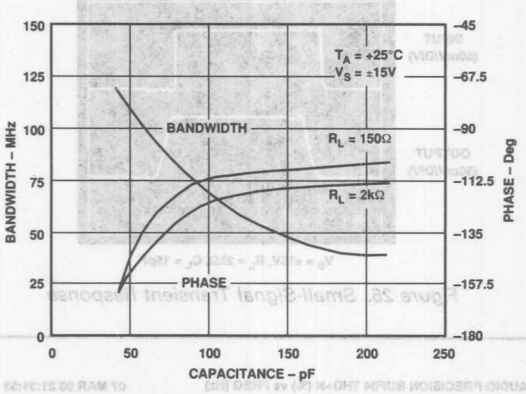


Figure 22. Bandwidth & Phase vs. Capacitive Loads @± 15 V

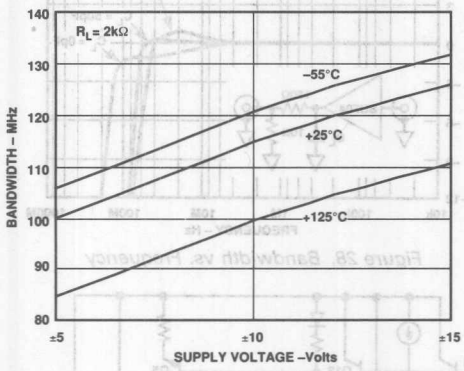


Figure 20. Bandwidth vs. Supply Voltage and Temperature

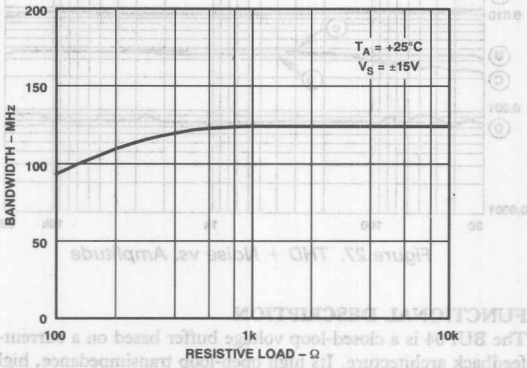


Figure 23. Bandwidth vs. Loads

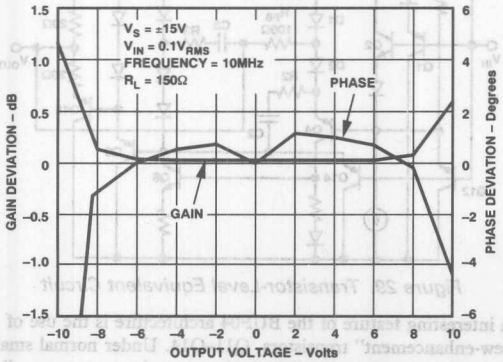


Figure 21. Gain and Phase Deviation, R_L = 150 Ω

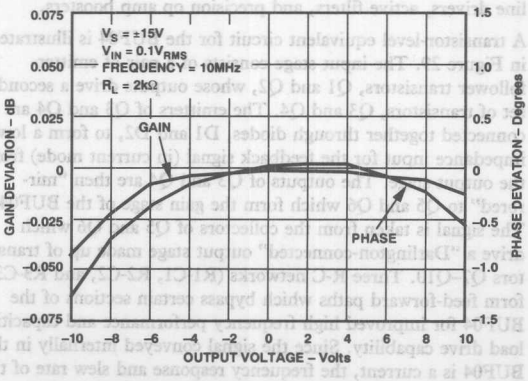
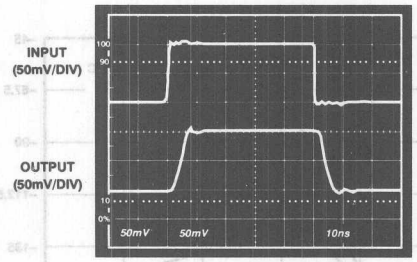
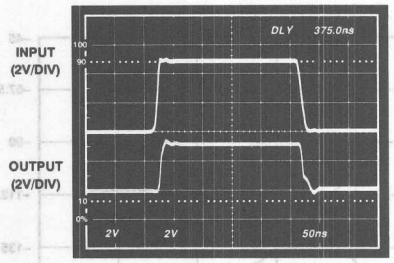


Figure 24. Gain and Phase Deviation, R_L = 2 kΩ



V_S = ±15V, R_L = 2kΩ, C_L = 15pF

Figure 25. Small-Signal Transient Response



V_S = ±15V, R_L = 2kΩ, C_L = 15pF

Figure 26. Large-Signal Transient Response

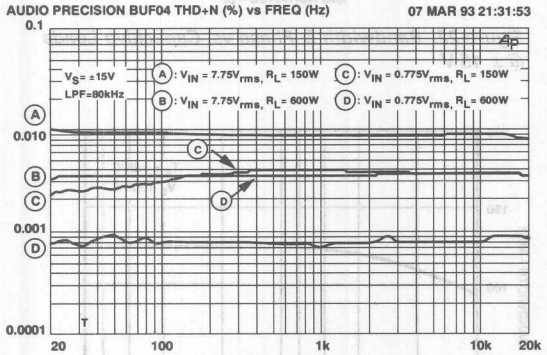


Figure 27. THD + Noise vs. Amplitude

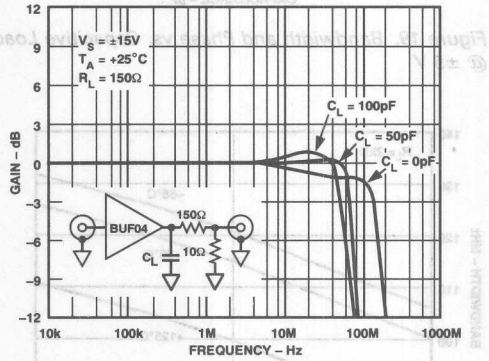


Figure 28. Bandwidth vs. Frequency

FUNCTIONAL DESCRIPTION

The BUF04 is a closed-loop voltage buffer based on a current-feedback architecture. Its high open-loop transimpedance, high output current drive capability, and its low input offset voltage makes it useful in a variety of applications, such as buffering the inputs of sampling and flash A/D converters, audio and video line drivers, active filters, and precision op amp boosters.

A transistor-level equivalent circuit for the BUF04 is illustrated in Figure 29. The input stage consists of a pair of emitter-follower transistors, Q1 and Q2, whose outputs drive a second set of transistors, Q3 and Q4. The emitters of Q3 and Q4 are connected together through diodes, D1 and D2, to form a low-impedance input for the feedback signal (in current mode) from the output stage. The outputs of Q3 and Q4 are then "mirrored" to Q5 and Q6 which form the gain stage of the BUF04. The signal is taken from the collectors of Q5 and Q6 which drive a "Darlington-connected" output stage made up of transistors Q7–Q10. Three R-C networks (R1-C1, R2-C2, and R3-C3) form feed-forward paths which bypass certain sections of the BUF04 for improved high frequency performance and capacitive load drive capability. Since the signal conveyed internally in the BUF04 is a current, the frequency response and slew rate of the BUF04 are insensitive to supply voltage variations.

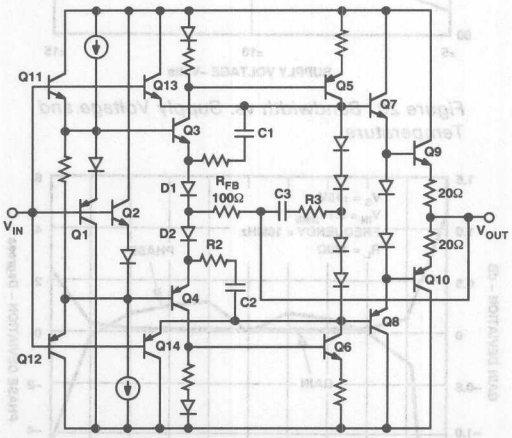


Figure 29. Transistor-Level Equivalent Circuit

An interesting feature of the BUF04 architecture is the use of "slew-enhancement" transistors, Q11–Q14. Under normal small-signal ($V_{IN} < 2\ V_{be}$s) conditions, these transistors are normally "OFF." In large signals, high speed transient applications where the input signal is $> 2\ V_{be}$s, these transistors turn on and literally "brute-force" the output to follow the input. When the input signal drops below $2\ V_{be}$s, the transistors return to their normally "OFF" state.

A two-terminal equivalent circuit of the BUF04 is shown in Figure 30 where the transistor-level equivalent circuit is reduced to its essential elements. The input stage develops a signal current, I_{IN}, that is replicated by an internal current conveyor so as to flow through R_t, the transimpedance of the BUF04. The voltage developed across R_t is buffered by a unity-gain output voltage follower. With an open-loop R_t of 400 kΩ and an R_{IN} of 30 Ω, the voltage gain of the BUF04, given by the ratio R_t/R_{IN} is approximately 13,000—accurate to approximately 13.5 bits. The BUF04's open-loop ac transimpedance response is determined by the open-loop pole formed by R_t and C_t. Since C_t is typically 8 pF, the open-loop pole occurs at approximately 50 kHz.

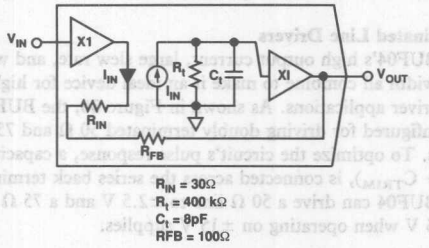


Figure 30. Current-Feedback Functional Equivalent Circuit of the BUF04

Grounding and Bypassing Considerations

To take full advantage of the BUF04's very wide bandwidth, high slew rates, and dynamic range capabilities requires due diligence with regard to supply bypassing. In high speed circuits, the supply bypassing network must provide a very low-impedance return path for currents flowing to and from the load network. As with any high speed application, multiple bypassing is always recommended. A 10 μF tantalum electrolytic in parallel with a 0.1 μF ceramic capacitor is sufficient for most applications. For those high speed applications where output load currents approach 50 mA, small-valued resistors (1.1 Ω to 4.7 Ω) in series with the tantalum capacitors may improve circuit transient response by damping out the capacitor's self-inductance. Figure 31 illustrates bypassing recommendations.

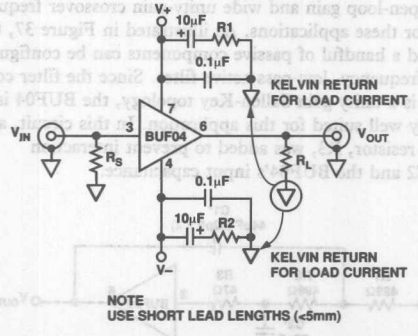


Figure 31. Recommended Power-Supply Bypassing

To minimize the effects of high-frequency coupling, circuits must be built with short interconnect leads, and large ground planes should be used whenever possible to provide a low resistance, low-inductance circuit path. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth and stability. If sockets are necessary, individual pin sockets (oftentimes called "cage jacks," AMP Part No. 5-330808-3 or 5-330808-6) should be used. They contribute far less stray reactance than molded socket assemblies.

Offset Voltage Nulling

Although the offset voltage of the BUF04 is very low (1 mV, maximum) for such a high speed buffer, the circuit shown in Figure 32 can be used if additional offset voltage nulling is required. A potentiometer ranging from 1k to 10k can be used for V_{OS} nulling; with a 10 kΩ potentiometer, the trim range is ±30 mV.

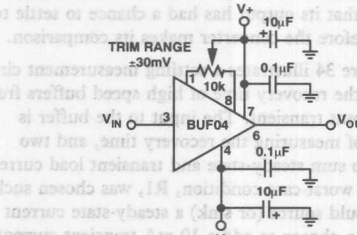


Figure 32. Optional Offset Voltage Nulling Scheme

APPLICATIONS

Output Short-Circuit Protection

To optimize the transient response and output voltage swing of the BUF04, internal output short-circuit current limiting was omitted. Although the BUF04 can provide continuous output currents of 50 mA without protection, direct connection of the BUF04's output to ground or to the supplies will destroy the device. An active current limit technique, illustrated in Figure 33, provides the necessary short-circuit protection while retaining full dc output voltage swing to the load.

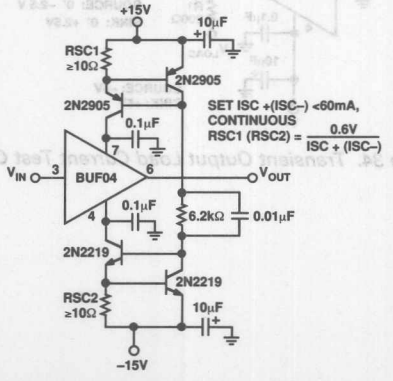


Figure 33. Short-Circuit Current Limiting Using Current Sources

Output Current Transient Recovery

Settling characteristics of high speed buffers also include the buffer's ability to recover, i.e., settle, from a transient output current load condition. When driving the input of an A/D converter, especially the successive-approximation converter types, the buffer must maintain a constant output voltage under dynamically changing load current conditions. In these types of converters, the comparison point is usually diode-clamped, but it may deviate several hundred millivolts resulting in high frequency modulation of the A/D input current. Open-loop and closed-loop buffers (also, op amps configured as followers) that exhibit high closed-loop output impedances and/or low unity-gain crossover frequencies recover very slowly from output load current transients. This slow recovery leads to linearity errors or missing codes because of errors in the instantaneous input voltage. Therefore, the buffer (or op amp) chosen for this type of application should exhibit low output impedance and high unity-gain bandwidth so that its output has had a chance to settle to its nominal value before the converter makes its comparison.

The circuit in Figure 34 illustrates a settling measurement circuit for evaluating the recovery time of high speed buffers from an output load current transient. The input to the buffer is grounded for ease of measuring the recovery time, and two resistors are used to sum steady-state and transient load currents at the output. As a worst-case condition, R1, was chosen such that the BUF04 would source (or sink) a steady-state current of 25 mA. R2 was then chosen to add a 10 mA transient current upon the steady-state value. To set accurately the nodal voltages internal to the BUF04, the supply voltages were offset by the voltage applied to R1. Because of its high transimpedance, wide bandwidth, and low output impedance, the BUF04 exhibits an extremely fast recovery time of 60 ns to 0.01%, as shown in Figure 34. Results were identical regardless whether the BUF04 was sourcing or sinking current.

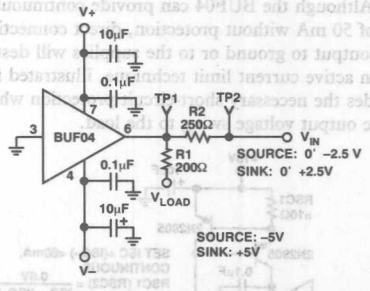


Figure 34. Transient Output Load Current Test Circuit

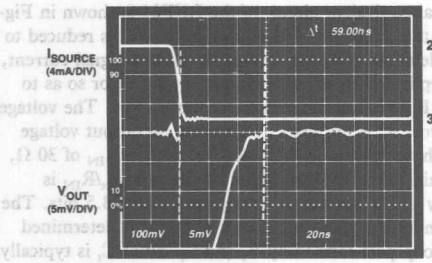
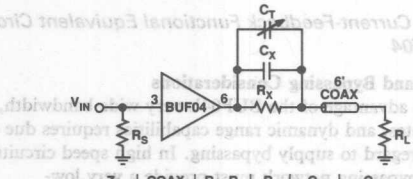


Figure 35. BUF04's Output Load Current Recovery Time

Terminated Line Drivers

The BUF04's high output current, large slew rate, and wide bandwidth all combine to make it an ideal device for high speed line driver applications. As shown in Figure 36, the BUF04 can be configured for driving doubly terminated 50 Ω and 75 Ω cables. To optimize the circuit's pulse response, a capacitor, C_T (C_X + C_{TRIM}), is connected across the series back termination. The BUF04 can drive a 50 Ω line to ±2.5 V and a 75 Ω line to ±3.75 V when operating on ±15 V supplies.



Z_O	COAX	R_S, R_L	R_X	C_X	C_T
50Ω	RG-58	50Ω	50	91pF	3–15pF
75Ω	RG-59	75Ω	75	62pF	3–15pF

Figure 36. Line Driver Configuration

Low-Pass Active Filter

In many signal-conditioning applications, filters are required to band-limit noise or altogether eliminate other unwanted signals prior to conversion. Often, high frequency filters are needed for these applications; however, there are few op amps that exhibit the high open-loop gain and wide unity-gain crossover frequency required for these applications. As illustrated in Figure 37, the BUF04 and a handful of passive components can be configured as a high frequency, low-pass active filter. Since the filter configuration is a unity-gain Sallen-Key topology, the BUF04 is particularly well suited for this application. In this circuit, an additional resistor, R3, was added to prevent interaction between C2 and the BUF04's input capacitance.

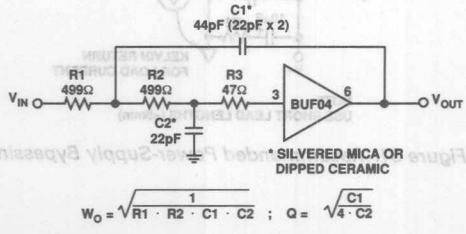


Figure 37. A 10 MHz Low-Pass Active Filter

Operation Within an Op Amp Feedback Loop

The BUF04 is well suited as a current booster or isolation buffer within the closed loop of precision op amps such as the OP177, the OP97, the OP27, or the OP77. Since the BUF04 is a closed-loop voltage buffer, no interstage coupling resistor between the op amp and the buffer's input is required for circuit stability. The wide bandwidth and high slew rate of the BUF04 assure that the loop has the characteristics of the op amp; hence, no additional rolloff is required.

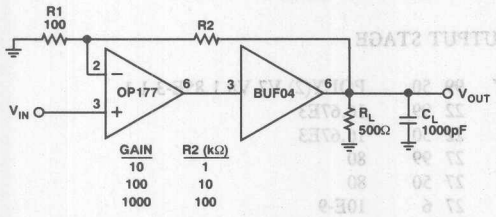


Figure 38. BUF04 as Booster Stage for a Precision Op Amp

Paralleling BUF04s for Increased Load Drive Capability

In applications where continuous output currents greater than 50 mA are required or where heat management is an issue, a number of BUF04s can be connected in parallel to reduce the drive requirement of any one buffer. An example of one such application is illustrated in Figure 39. In this circuit, the BUF04s are required to drive a doubly terminated 50 Ω line to ±5 V. This type of a load for a single BUF04 would certainly cause a power dissipation problem. Parallel operation results in lower input and output impedances and increased bias currents; on the other hand, input equivalent noise voltage is reduced and input offset voltage remains unchanged.

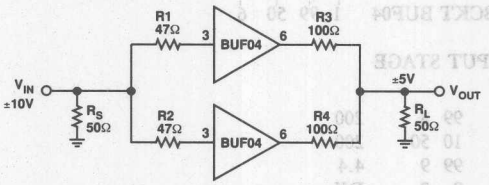


Figure 39. Paralleling BUF04s for High Output Currents

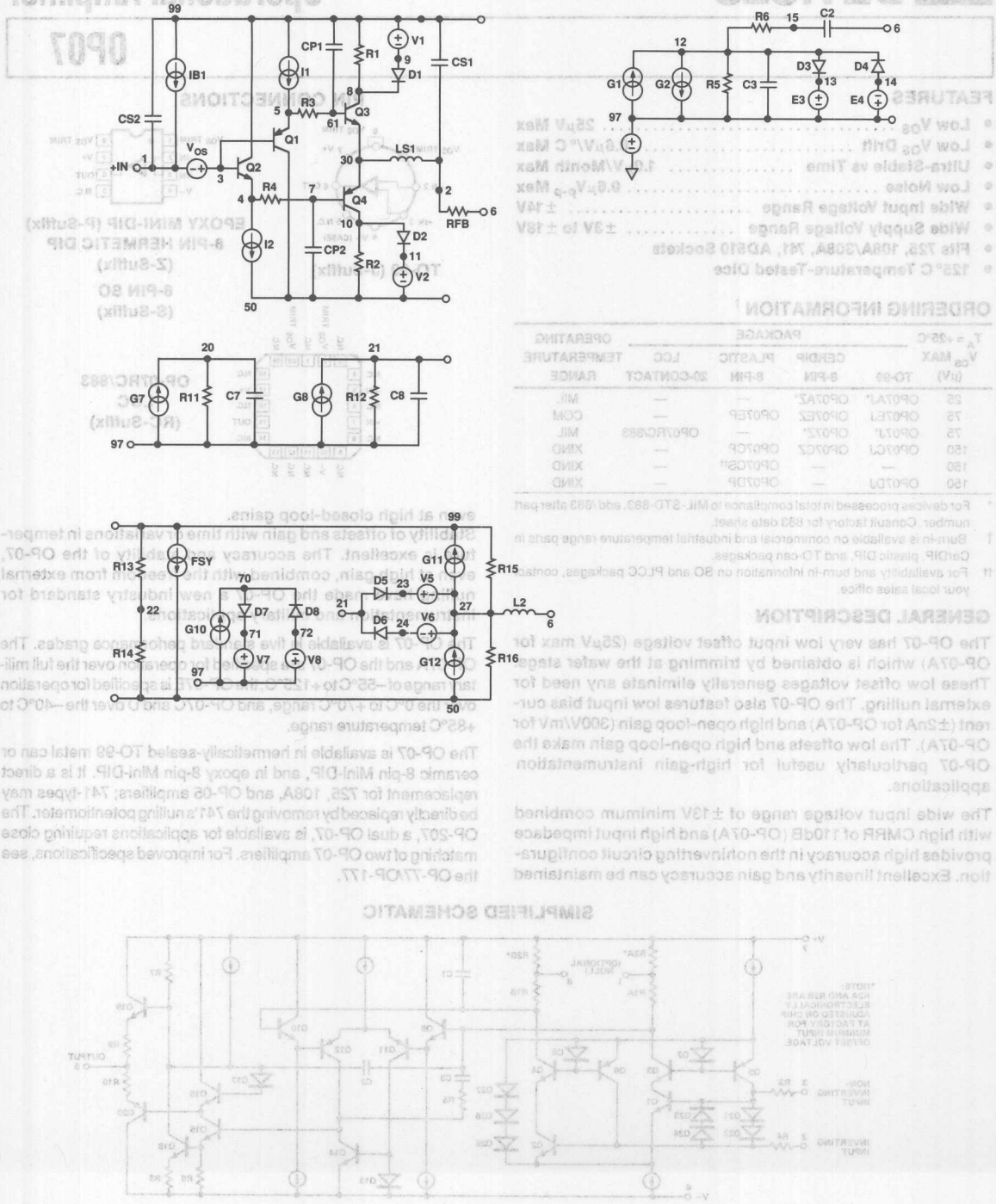
Overdrive Recovery and Phase Reversal

In applications where the inputs could be driven to the supply rails, the BUF04 recovers in 10 ns from positive or negative overdrive. The BUF04 does not exhibit any output voltage phase reversal when the input signal exceeds its input voltage range.

BUF04

```
* BUF04 SPICE Macro-model                    7/93, Rev. A
*                                           JCB / PMI
*
* Copyright 1993 by Analog Devices, Inc.
*
*
* Node assignments
*                    noninverting input
*                    |  positive supply
*                    |  |  negative supply
*                    |  |  |  output
*                    |  |  |  |
*                    |  |  |  |
.SUBCKT BUF04        1  99 50 6
*
* INPUT STAGE
*
R1      99  8        200
R2      10  50       200
V1      99  9        4.4
D1      9   8        DX
V2      11  50       4.4
D2      10  11       DX
I1      99  5        1.8E-3
I2      4   50       1.8E-3
Q1      50  3   5    QP
Q2      99  3   4    QN
Q3      8   61  30   QN
Q4      10  7   30   QP
R3      5   61       50E3
R4      4   7        50E3
CP1     61  99       14E-15
CP2     7   50       14E-15
RFB     6   2        100
*
* INPUT ERROR SOURCES
*
IB1     99  1        0.7E-6
VOS     3   1        0.3E-3
LS1     30  2        1E-9
CS1     99  2        2.0E-12
CS2     99  1        3.0E-12
*
EREF    97  0        22 0 1
*
* TRANSCONDUCTANCE STAGE
*
R5      12  97       365E3
C3      12  97       8E-12
G1      97  12       99 8 5E-3
G2      12  97       10 50 5E-3
E3      13  97       POLY(1)   99  97 -2.5  1.1
E4      97  14       POLY(1)   97  50 -2.5  1.1
D3      12  13       DX
D4      14  12       DX
R6      12  15       200
C2      15  6        20E-12
*
* POLE AT 200 MHz
*
R11     20  97       1E6
C7      20  97       0.759E-15
G7      97  20       12  22  1E-6
*
* POLE AT 200 MHz
*
R12     21  97       1E6
C8      21  97       0.759E-15
G8      97  21       20  22  1E-6
*
* OUTPUT STAGE
*
FSY     99  50       POLY(2) V7 V8 1.85E-3 1 1
R13     22  99       16.67E3
R14     22  50       16.67E3
R15     27  99       80
R16     27  50       80
L2      27  6        10E-9
G11     27  99       99 21 12.5E-3
G12     50  27       21 50 12.5E-3
V5      23  27       3.3
V6      27  24       3.3
D5      21  23       DX
D6      24  21       DX
G10     97  70       27 21 12.5E-3
D7      70  71       DX
D8      72  70       DX
V7      71  97       DC 0
V8      97  72       DC 0
*
* MODELS USED
*
.MODEL QN NPN(BF=1000  IS=1E-15)
.MODEL QP PNP(BF=1000  IS=1E-15)
.MODEL DX D(IS=1E-15)
.ENDS BUF04
```

BUF04 SPICE



9

FEATURES

- Low V_{OS} ..... 25μV Max
- Low V_{OS} Drift ..... 0.6μV/°C Max
- Ultra-Stable vs Time ..... 1.0μV/Month Max
- Low Noise ..... 0.6μV_{p-p} Max
- Wide Input Voltage Range ..... ±14V
- Wide Supply Voltage Range ..... ±3V to ±18V
- Fits 725, 108A/308A, 741, AD510 Sockets
- 125° C Temperature-Tested Dice

ORDERING INFORMATION †

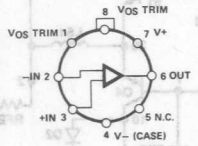
T_A = +25°C V_{OS} MAX (μV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
25	OP07AJ*	OP07AZ*	—	—	MIL
75	OP07EJ	OP07EZ	OP07EP	—	COM
75	OP07J*	OP07Z*	—	OP07RC/883	MIL
150	OP07CJ	OP07CZ	OP07CP	—	XIND
150	—	—	OP07CS††	—	XIND
150	OP07DJ	—	OP07DP	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

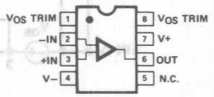
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

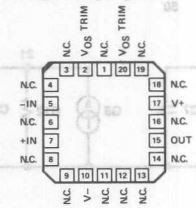
PIN CONNECTIONS



TO-99 (J-Suffix)



EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP
(Z-Suffix)
8-PIN SO
(S-Suffix)



OP-07RC/883
LCC
(RC-Suffix)

GENERAL DESCRIPTION

The OP-07 has very low input offset voltage (25μV max for OP-07A) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current (±2nA for OP-07A) and high open-loop gain (300V/mV for OP-07A). The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain instrumentation applications.

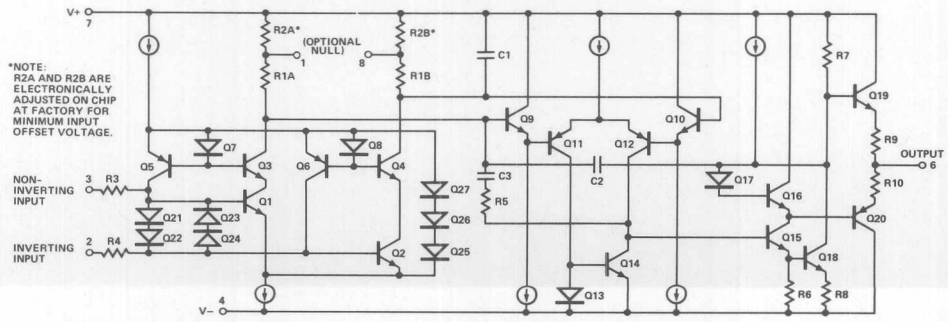
The wide input voltage range of ±13V minimum combined with high CMRR of 110dB (OP-07A) and high input impedace provides high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Stability of offsets and gain with time or variations in temperture is excellent. The accuracy and stability of the OP-07, even at high gain, combined with the freedom from external nulling have made the OP-07 a new industry standard for instrumentation and military applications.

The OP-07 is available in five standard performance grades. The OP-07A and the OP-07 are specified for operation over the full military range of –55°C to +125°C; the OP-07E is specified for operation over the 0°C to +70°C range, and OP-07C and D over the –40°C to +85°C temperature range.

The OP-07 is available in hermetically-sealed TO-99 metal can or ceramic 8-pin Mini-DIP, and in epoxy 8-pin Mini-DIP. It is a direct replacement for 725, 108A, and OP-05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer. The OP-207, a dual OP-07, is available for applications requiring close matching of two OP-07 amplifiers. For improved specifications, see the OP-77/OP-177.

SIMPLIFIED SCHEMATIC



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
  J, RC and Z Packages ..... –65°C to +150°C
  P Package ..... –65°C to +125°C
Operating Temperature Range
  OP-07A, OP-07, OP-07RC ..... –55°C to +125°C
  OP-07E ..... 0°C to +70°C
  OP-07C, OP-07D ..... –40°C to +85°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_j) ..... +150°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	30	75	μV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 2)	—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I_{OS}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I_B		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{Hz}$
		f_O = 100Hz (Note 3)	—	10.0	13.0	—	10.0	13.0	
		f_O = 1000Hz (Note 3)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz (Note 3)	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{Hz}$
		f_O = 100Hz (Note 3)	—	0.14	0.23	—	0.14	0.23	
		f_O = 1000Hz (Note 3)	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	30	80	—	20	60	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to ±18V	—	4	10	—	4	10	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	300	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 4)	150	400	—	150	400	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	±10.5	±12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 3)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	75	120	—	75	120	mW
		$V_S = \pm 3V$, No Load	—	4	6	—	4	6	
Offset Adjustment Range		$R_P = 20k\Omega$	—	±4	—	—	±4	—	mV

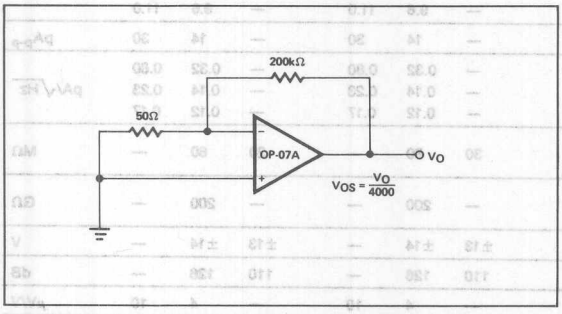
NOTES:
1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves. Parameter is sample tested.
3. Sample tested.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

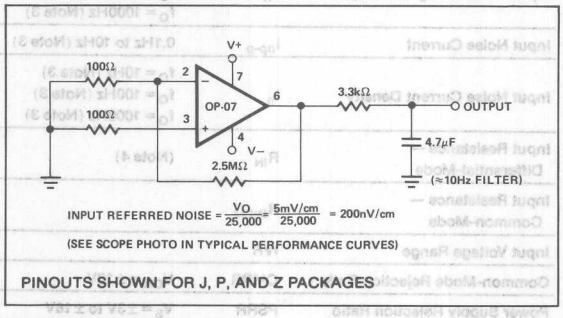
PARAMETER	SYMBOL	CONDITIONS	OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	25	60	—	60	200	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.2	0.6	—	0.3	1.3	μV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.6	—	0.3	1.3	μV/°C
Input Offset Current	I_{OS}		—	0.8	4	—	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1	±4	—	±2	±6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	13	50	pA/°C
Input Voltage Range	IVR		±13	±13.5	—	±13	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±12.6	—	±12	±12.6	—	V

NOTES:
1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

TYPICAL OFFSET VOLTAGE TEST CIRCUIT

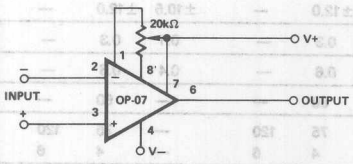


TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT



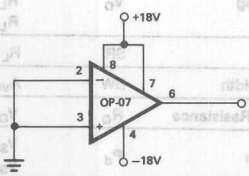
PINOUTS SHOWN FOR J, P, AND Z PACKAGES

OPTIONAL OFFSET NULLING CIRCUIT



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

BURN-IN CIRCUIT



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-07E			OP-07C			OP-07D			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	(Note 1)	—	30	75	—	60	150	—	60	150	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 2)	—	0.3	1.5	—	0.4	2.0	—	0.5	3.0	μV/Mo
Input Offset Current	I_{OS}		—	0.5	3.8	—	0.8	6.0	—	0.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	—	±2.0	±12	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		f_O = 100Hz (Note 3)	—	10.0	13.0	—	10.2	13.5	—	10.3	13.5	
		f_O = 1000Hz	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{Hz}$
		f_O = 100Hz (Note 3)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		f_O = 1000Hz	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	15	50	—	8	33	—	7	31	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	160	—	—	120	—	—	120	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	106	123	—	100	120	—	94	110	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	—	5	20	—	7	32	—	7	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	200	500	—	120	400	—	120	400	—	V/mV
		$R_L \geq 500\Omega$ V_O = ±0.5V V_S = ±3V (Note 4)	150	400	—	100	400	—	—	400	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.0	±13.0	—	±12.0	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±11.5	±12.8	—	±11.5	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	—	±12.0	—	—	±12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 5)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0	—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	V_S = ±15V, No Load	—	75	120	—	80	150	—	80	150	mW
		V_S = ±3V, No Load	—	4	6	—	4	8	—	4	8	
Offset Adjustment Range		R_P = 20kΩ	—	±4	—	—	±4	—	—	±4	—	mV

NOTES:
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves. Parameter is sample tested.
3. Sample tested.
4. Guaranteed by design.
5. Guaranteed but not tested.

OP07

			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	45	130	—	85	250	—	85	250	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 3)	—	0.3	1.3	—	0.5	1.8	—	0.7	2.5	μV/°C
With External Trim	TCV_{OSn}	R_P = 20kΩ (Note 3)	—	0.3	1.3	—	0.4	1.6	—	0.7	2.5	μV/°C
Input Offset Current	I_{OS}		—	0.9	5.3	—	1.6	8.0	—	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	—	12	50	pA/°C
Input Bias Current	I_B		—	±1.5	±5.5	—	±2.2	±9.0	—	±3.0	±14	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	—	18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	103	123	—	97	120	—	94	106	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	—	7	32	—	10	51	—	10	51	μV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ V_O = ±10V	180	450	—	100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±12.6	—	±11	±12.6	—	±11	±12.6	—	V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

ANALOG DEVICES

Low Noise, Precision Operational Amplifier

OP27

FEATURES

- **Low Noise** ..... $80nV_{p-p}$ (0.1Hz to 10Hz)
  ..... $3nV/\sqrt{Hz}$
- **Low Drift** ..... $0.2\mu V/°C$
- **High Speed** ..... 2.8V/μs Slew Rate
  ..... 8MHz Gain Bandwidth
- **Low V_{OS}** 10μV
- **Excellent CMRR** ..... 126dB at V_{CM} of ±11V
- **High Open-Loop Gain** ..... 1.8 Million
- **Fits 725, OP-07, OP-05, AD510, AD517, 5534A sockets**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
25	OP27AJ*	OP27AZ*	–	–	MIL
25	OP27EJ	OP27EZ	OP27EP	–	IND/COM
60	OP27BJ*	OP27BZ*	–	OP27BR/883	MIL
60	OP27FJ	OP27FZ	OP27FP	–	IND/COM
100	OP27CJ	OP27CZ	–	–	MIL
100	OP27GJ	OP27GZ	OP27GP	–	XIND
100	–	–	OP27GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

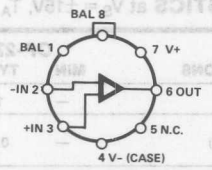
The OP-27 precision operational amplifier combines the low offset and drift of the OP-07 with both high speed and low noise. Offsets down to 25μV and drift of 0.6μV/°C maximum make the OP-27 ideal for precision instrumentation applications. Exceptionally low noise, $e_n = 3.5nV/\sqrt{Hz}$, at 10Hz, a low 1/f noise corner frequency of 2.7Hz, and high gain (1.8 million), allow accurate high-gain amplification of low-level signals. A gain-bandwidth product of 8MHz and a 2.8V/μsec slew rate provides excellent dynamic accuracy in high-speed data-acquisition systems.

A low input bias current of ±10nA is achieved by use of a bias-current-cancellation circuit. Over the military temperature range, this circuit typically holds I_B and I_{OS} to ±20nA and 15nA respectively.

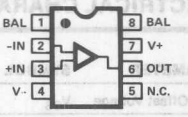
The output stage has good load driving capability. A guaranteed swing of ±10V into 600Ω and low output distortion make the OP-27 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

PIN CONNECTIONS



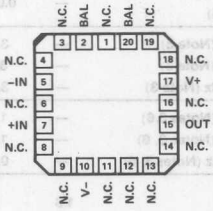
TO-99
(J-Suffix)



8-PIN HERMETIC DIP
(Z-Suffix)

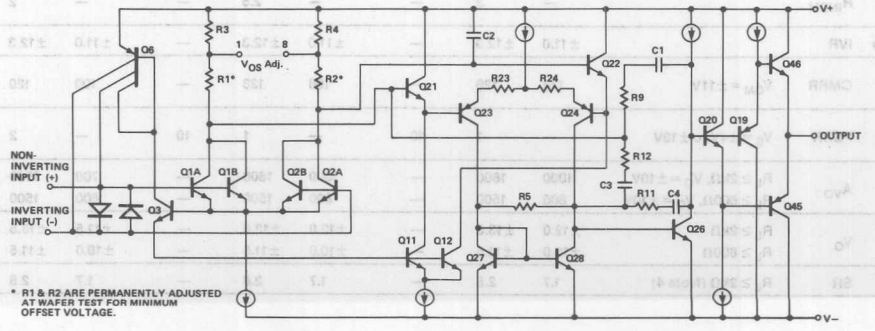
EPOXY MINI-DIP
(P-Suffix)

8-PIN SO
(S-Suffix)



OP-27BRC/883
LCC PACKAGE
(RC-Suffix)

SIMPLIFIED SCHEMATIC



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OP27

Low cost, high-volume production of OP-27 is achieved by using an on-chip zener-zap trimming network. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-27 provides excellent performance in low-noise high-accuracy amplification of low-level signals. Applications include stable integrators, precision summing amplifiers, precision voltage-threshold detectors, comparators, and professional audio circuits such as tape-head and microphone preamplifiers.

The OP-27 is a direct replacement for 725, OP-06, OP-07 and OP-05 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage ..... ±22V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-27A, OP-27B, OP-27C (J, Z, RC)..... –55°C to +125°C
OP-27E, OP-27F (J, Z) ..... –25°C to +85°C
OP-27E, OP-27F (P) ..... 0°C to +70°C
OP-27G (P, S, J, Z) ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. The OP-27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SO package.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27A/E MIN	OP-27A/E TYP	OP-27A/E MAX	OP-27B/F MIN	OP-27B/F TYP	OP-27B/F MAX	OP-27C/G MIN	OP-27C/G TYP	OP-27C/G MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 3)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	nV/√Hz
		f_O = 30Hz (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		f_O = 1000Hz (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	f_O = 10Hz (Notes 3,6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	pA/√Hz
		f_O = 30Hz (Notes 3, 6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		f_O = 1000Hz (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11V	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4V to ±18V	—	1	10	—	1	10	—	2	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 600\Omega$, V_O = ±10V	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-27A/E MIN	OP-27A/E TYP	OP-27A/E MAX	OP-27B/F MIN	OP-27B/F TYP	OP-27B/F MAX	OP-27C/G MIN	OP-27C/G TYP	OP-27C/G MAX	UNITS
Gain Bandwidth Prod.	GBW	(Note 4)	5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	V_O	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	±4.0	—	—	±4.0	—	—	±4.0	—	mV

NOTES:
1. Input offset voltage measurements are performed ~ 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.
7. Guaranteed by input bias current.

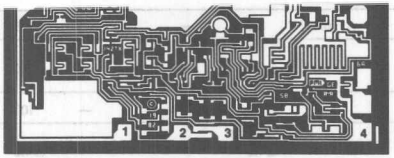
ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27A MIN	OP-27A TYP	OP-27A MAX	OP-27B MIN	OP-27B TYP	OP-27B MAX	OP-27C MIN	OP-27C TYP	OP-27C MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-27J and OP-27Z, $0°C \le T_A \le +70°C$ for OP-27EP, FP and $-40°C \le T_A \le +85°C$ for OP-27GP, GS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27E MIN	OP-27E TYP	OP-27E MAX	OP-27F MIN	OP-27F TYP	OP-27F MAX	OP-27G MIN	OP-27G TYP	OP-27G MAX	UNITS
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$. TCV_{OS} is 100% tested for A/E grades, sample tested for B/C/F/G grades.
3. Guaranteed by design.



DIE SIZE 0.109 × 0.055 inch, 5995 sq. mils
(2.77 × 1.40mm, 3.88 sq. mm)

2. (–) INPUT
3. (+) INPUT
4. V–
6. OUTPUT
7. V+
8. NULL

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-27N, OP-27G, and OP-27GR devices; $T_A = 125°C$ for OP-27NT and OP-27GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27NT LIMIT	OP-27N LIMIT	OP-27GT LIMIT	OP-27G LIMIT	OP-27GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	60	35	200	60	100	μV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		±60	±40	±95	±55	±80	nA MAX
Input Voltage Range	IVR		±10.3	±11	±10.3	±11	±11	V MIN
Common-Mode Rejection Ratio	CMRR	V_{CM} = IVR	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	10	—	10	20	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	600	1000	500	1000	700	V/mV MIN
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	—	800	—	800	600	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11.5	±12.0	±11.0	±12.0	±11.5	V MIN
		$R_L \geq 600\Omega$	—	±10.0	—	±10.0	±10.0	
Power Consumption	P_d	$V_O = 0$	—	140	—	140	170	mW MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27N TYPICAL	OP-27G TYPICAL	OP-27GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nulled or Unnulled $R_P = 8k\Omega$ to $20k\Omega$	0.2	0.3	0.4	μV/°C
Average Input Offset Current Drift	TCI_{OS}		80	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	160	200	pA/°C
Input Noise Voltage Density	e_n	f_O = 10Hz	3.5	3.5	3.8	nV/$\sqrt{Hz}$
		f_O = 30Hz	3.1	3.1	3.3	
		f_O = 1000Hz	3.0	3.0	3.2	
Input Noise Current Density	i_n	f_O = 10Hz	1.7	1.7	1.7	pA/$\sqrt{Hz}$
		f_O = 30Hz	1.0	1.0	1.0	
		f_O = 1000Hz	0.4	0.4	0.4	
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.09	μVp-p
Slew Rate	SR	$R_L \geq 2k\Omega$	2.8	2.8	2.8	V/μs
Gain Bandwidth Product	GBW		8	8	8	MHz

NOTE:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

ANALOG DEVICES

Low Noise, Precision, High Speed Operational Amplifier ($A_{VCL} \geq 5$)

OP37

FEATURES

- **Low Noise** ..... 80nV p-p (0.1Hz to 10Hz)
  ..... 3nV/$\sqrt{Hz}$ at 1kHz
- **Low Drift** ..... 0.2μV/°C
- **High Speed** ..... 17V/μs Slew Rate
  ..... 63MHz Gain Bandwidth
- **Low Input Offset Voltage** 10μV
- **Excellent CMRR** ... 126dB (Common-Voltage of ±11V)
- **High Open-Loop Gain** ..... 1.8 Million
- **Replaces 725, OP-05, OP-06, OP-07, AD510, AD517, SE5534 in Gains >5**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (µV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
25	OP37AJ*	OP37AZ*	–	–	MIL
25	OP37EJ	OP37EZ	OP37EP	–	IND/COM
60	OP37BJ*	OP37BZ*	–	OP37BRC/883	MIL
60	OP37FJ	OP37FZ	OP37FP	–	IND/COM
100	OP37CJ*	OP37CZ	–	–	MIL
100	OP37GJ	OP37GZ	OP37GP	–	XIND
100	–	–	OP37GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

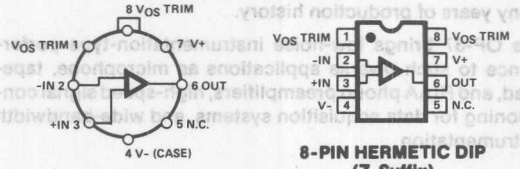
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO package, contact your local sales office.

GENERAL DESCRIPTION

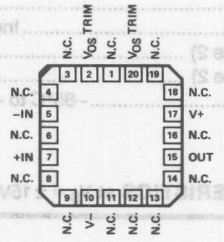
The OP-37 provides the same high performance as the OP-27, but the design is optimized for circuits with gains greater than five. This design change increases slew rate to 17V/μsec and gain-bandwidth product to 63MHz.

PIN CONNECTIONS



TO-99 (J-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)
EPOXY MINI-DIP (P-Suffix)
8-PIN SO (S-Suffix)



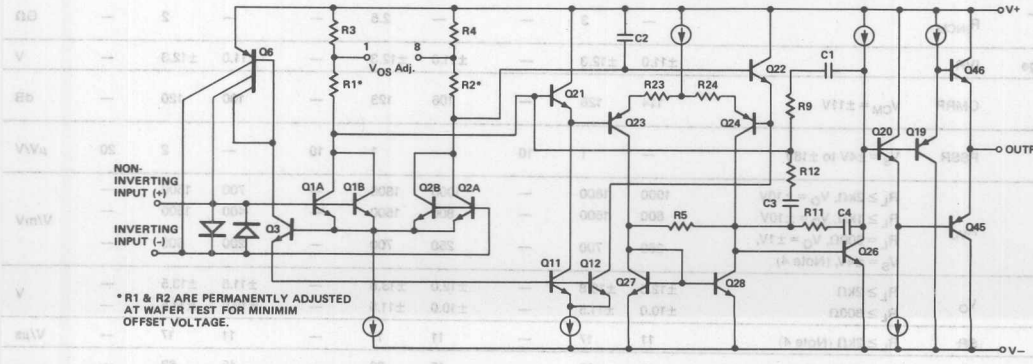
OP-37BRC/883 LCC PACKAGE (RC-Suffix)

The OP-37 provides the low offset and drift of the OP-07 plus higher speed and lower noise. Offsets down to 25μV and drift of 0.6μV/°C maximum make the OP-37 ideal for precision instrumentation applications. Exceptionally low noise (e_n=3.5nV/$\sqrt{Hz}$ at 10Hz), a low 1/f noise corner frequency of 2.7Hz, and the high gain of 1.8 million, allow accurate high-gain amplification of low-level signals.

The low input bias current of ±10nA and offset current of 7nA are achieved by using a bias-current-cancellation circuit. Over the military temperature range this typically holds I_B and I_{OS} to ±20nA and 15nA respectively.

The output stage has good load driving capability. A guaranteed swing of ±10V into 600Ω and low output distortion make the OP-37 an excellent choice for professional audio applications.

SIMPLIFIED SCHEMATIC



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PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low-cost, high-volume production of the OP-37 is achieved by using on-chip zener-zap trimming. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-37 brings low-noise instrumentation-type performance to such diverse applications as microphone, tape-head, and RIAA phono preamplifiers, high-speed signal conditioning for data acquisition systems, and wide-bandwidth instrumentation.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage ..... ±22V
Internal Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... –65°C to +150°C

Operating Temperature Range
OP-37A, OP-37B, OP-37C (J, Z, RC) ..... –55°C to +125°C
OP-37E, OP-37F (J, Z) ..... –25°C to +85°C
OP-37E, OP-37F (P) ..... 0°C to +70°C
OP-37G (P, S, J, Z) ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC, TC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. The OP-37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-37A/E			OP-37B/F			OP-37C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 3)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	$nV/\sqrt{Hz}$
		f_O = 30Hz (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		f_O = 1000Hz (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	f_O = 10Hz (Notes 3, 6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	$pA/\sqrt{Hz}$
		f_O = 30Hz (Notes 3, 6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		f_O = 1000Hz (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11V	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSSR	V_S = ±4V to ±18V	—	1	10	—	1	10	—	2	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 1k\Omega$, V_O = ±10V	800	1500	—	800	1500	—	400	1500	—	
		$R_L = 600\Omega$, V_O = ±1V, V_S = ±4V, (Note 4)	250	700	—	250	700	—	200	500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	11	17	—	11	17	—	11	17	—	V/μs
Gain Bandwidth Prod.	GBW	f_O = 10kHz (Note 4)	45	63	—	45	63	—	45	63	—	MHz
		f_O = 1MHz	—	40	—	—	40	—	—	40	—	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-37A/E MIN	OP-37A/E TYP	OP-37A/E MAX	OP-37B/F MIN	OP-37B/F TYP	OP-37B/F MAX	OP-37C/G MIN	OP-37C/G TYP	OP-37C/G MAX	UNITS
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	$V_O = 0$	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	±4.0	—	—	±4.0	—	—	±4.0	—	mV

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
2. Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.
7. Guaranteed by input bias current.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37A MIN	OP-37A TYP	OP-37A MAX	OP-37B MIN	OP-37B TYP	OP-37B MAX	OP-37C MIN	OP-37C TYP	OP-37C MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

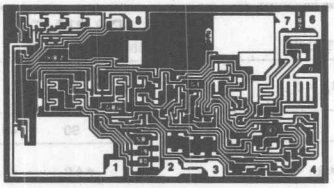
ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-37EJ/FJ and OP-37EZ/FZ, $0°C \le T_A \le +70°C$ for OP-37EP/FP and $-40°C \le T_A \le +85°$ for OP-37GP/GS/GJ/GZ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37E MIN	OP-37E TYP	OP-37E MAX	OP-37F MIN	OP-37F TYP	OP-37F MAX	OP-37G MIN	OP-37G TYP	OP-37G MAX	UNITS
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$. TCV_{OS} is 100% tested for A/E grades, sample tested for B/C/F/G grades.
3. Guaranteed by design.

DICE CHARACTERISTICS

DIE SIZE 0.098 × 0.056 inch, 5488 sq. mils
(2.49 × 1.42 mm, 3.54 sq. mm)



1. NULL
2. (–) INPUT
3. (+) INPUT
4. V–
6. OUTPUT
7. V+
8. NULL

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-37N, OP-37G and OP-37GR devices; $T_A = 125°C$ for OP-37NT and OP-37GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37NT LIMIT	OP-37N LIMIT	OP-37GT LIMIT	OP-37G LIMIT	OP-37GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	60	35	200	60	100	μV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		±60	±40	±95	±55	±80	nA MAX
Input Voltage Range	IVR		±10.3	±11	±10.3	±11	±11	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$T_A = 25°C$, $V_S = \pm 4V$ to $\pm 18V$	10	10	10	10	20	μV/V MAX
		$T_A = 125°C$, $V_S = \pm 4.5V$ to $\pm 18V$	16	—	20	—	—	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	600	1000	500	1000	700	V/mV MIN
		$R_L \geq 1k\Omega$, $V_O = \pm 10V$	—	800	—	800	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11.5	±12.0	±11.0	±12.0	±11.5	V MIN
		$R_L \geq 600\Omega$	—	±10.0	—	±10.0	±10.0	
Power Consumption	P_d	$V_O = 0$	—	140	—	140	170	mW MAX

NOTES:
For 25°C characteristics of OP-37NT and OP-37GT devices, see OP-37N and OP-37G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot asembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37NT TYPICAL	OP-37N TYPICAL	OP-37GT TYPICAL	OP-37G TYPICAL	OP-37GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nulled or Unnulled $R_P = 8k\Omega$ to $20k\Omega$	0.2	0.2	0.3	0.3	0.4	μV/°C
Average Input Offset Current Drift	TCI_{OS}		80	80	130	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	100	160	160	200	pA/°C
Input Noise Voltage Density	e_n	$f_O = 10Hz$	3.5	3.5	3.5	3.5	3.8	$nV/\sqrt{Hz}$
		$f_O = 30Hz$	3.1	3.1	3.1	3.1	3.3	
		$f_O = 1000Hz$	3.0	3.0	3.0	3.0	3.2	
Input Noise Current Density	i_n	$f_O = 10Hz$	1.7	1.7	1.7	1.7	1.7	$pA/\sqrt{Hz}$
		$f_O = 30Hz$	1.0	1.0	1.0	1.0	1.0	
		$f_O = 1000Hz$	0.4	0.4	0.4	0.4	0.4	
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.08	0.08	0.09	μV_{P-P}
Slew Rate	SR	$R_L \geq 2k\Omega$	17	17	17	17	17	V/μs
Gain Bandwidth Product	GBW	$f_O = 10kHz$	63	63	63	63	63	MHz

NOTE:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

ANALOG DEVICES

High Speed, Fast Settling Precision Operational Amplifier

OP42

FEATURES

Fast

- Slew Rate ..... 50V/μs Min
- Settling-Time (0.01%) ..... 1μs Max
- Gain-Bandwidth Product ..... 10MHz Typ

Precise

- Common-Mode Rejection ..... 88dB Min
- Open-Loop Gain ..... 500V/mV Min
- Offset Voltage ..... 750μV Max
- Bias Current ..... 200pA Max

Excellent Radiation Hardness
Available in Die Form

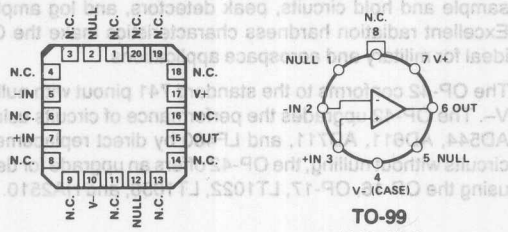
ORDERING INFORMATION †

T_A = 25°C V_{OS} MAX (mV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	SO 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
1.0	OP42AJ*	OP42AZ*	–	–	OP42ARC/883	MIL
0.75	OP42EJ	OP42EZ	–	–	–	IND
1.5	OP42FJ	OP42FZ	–	–	–	IND
5.0	–	–	OP42GP	OP42GS	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

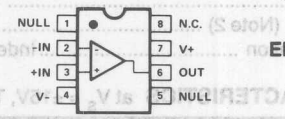
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages.

PIN CONNECTIONS



TO-99
(J-Suffix)

20-CONTACT LCC
(RC-Suffix)



8-PIN CERDIP
(Z Suffix)

EPOXY MINI-DIP
(P-Suffix)

8-PIN SO
(S-Suffix)

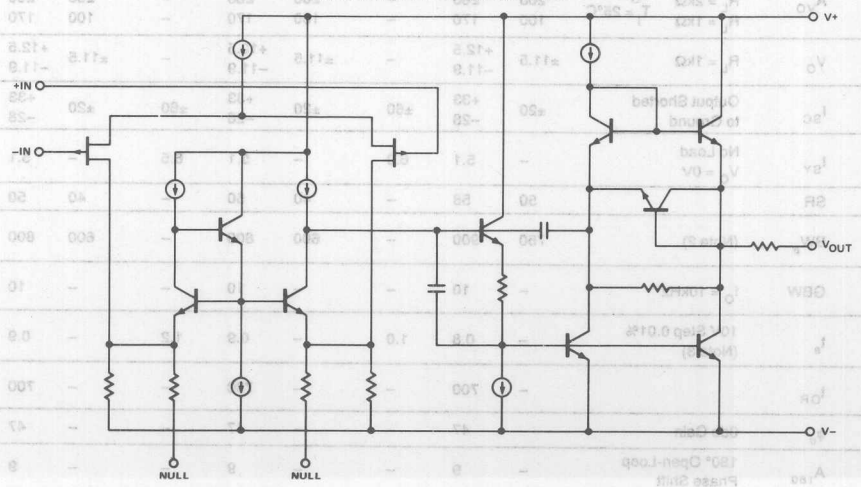
GENERAL DESCRIPTION

The OP-42 is a fast precision JFET-input operational amplifier. Similar in speed to the OP-17, the OP-42 offers a symmetric 58V/μs slew rate and is internally compensated for unity-gain operation. OP-42 speed is achieved with a supply current of less than 6mA. Unity-gain stability, a wide full-power bandwidth of 900kHz, and a fast settling-time of 800ns to 0.01% make the OP-42 an ideal output amplifier for fast digital-to-analog converters.

Equal attention was given to both speed and precision in the OP-42 design. Its tight 750μV maximum input offset voltage combined with well-controlled drift of less than 10μV/°C eliminates the need for external nulling in many circuits. The OP-42's

Continued

SIMPLIFIED SCHEMATIC



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

CMR combined with a minimum 500V/mV gain into 10kΩ load ensure excellent linearity in both noninverting and inverting gain configurations. The low input bias and offset currents provided by the JFET input stage suit the OP-42 for use in high-speed sample and hold circuits, peak detectors, and log amplifiers. Excellent radiation hardness characteristics make the OP-42 ideal for military and aerospace applications.

The OP-42 conforms to the standard 741 pinout with nulling to V–. The OP-42 upgrades the performance of circuits using the AD544, AD611, AD711, and LF400 by direct replacement. In circuits without nulling, the OP-42 offers an upgrade for designs using the OP-16, OP-17, LT1022, LT1056, and HA2510.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Input Voltage (Note 2) ..... ±20V
Differential Input Voltage (Note 2) 40V
Output Short-Circuit Duration ..... Indefined
OP42E, F (J, Z) ..... –25°C to +85°C
OP42G ..... –40°C to +85°C
Junction Temperature ..... –65°C to +175°C
Lead Temperature Range (Soldering, 60 sec.) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC,TC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CERDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-42E			OP-42F			OP-42G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}		–	0.3	0.75	–	0.4	1.5	–	1.5	5.0	mV
Input Bias Current	I_B	V_{CM} = 0V T_j = 25°C	–	80	200	–	130	250	–	130	250	pA
Input Offset Current	I_{OS}	V_{CM} = 0V T_j = 25°C	–	4	40	–	6	50	–	6	50	pA
Input Voltage Range	IVR	(Note 1)	±11	+12.5 –12.0	–	±11	+12.5 –12.0	–	±11	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	88	98	–	80	92	–	80	92	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	–	9	40	–	12	50	–	12	50	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ V_O = ±10V R_L = 2kΩ T_j = 25°C R_L = 1kΩ	500 200 100	900 260 170	– – –	500 200 100	900 260 170	– – –	500 200 100	900 260 170	– – –	V/mV
Output Voltage Swing	V_O	R_L = 1kΩ	±11.5	+12.5 –11.9	–	±11.5	+12.5 –11.9	–	±11.5	+12.5 –11.9	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+33 –28	±60	±20	+33 –28	±60	±20	+33 –28	±60	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.1	6.0	–	5.1	6.5	–	5.1	6.5	mA
Slew Rate	SR		50	58	–	40	50	–	40	50	–	V/µs
Full-Power Bandwidth	BW_p	(Note 2)	750	900	–	600	800	–	600	800	–	kHz
Gain-Bandwidth Product	GBW	f_O = 10kHz	–	10	–	–	10	–	–	10	–	MHz
Settling -Time	t_s	10V Step 0.01% (Note 3)	–	0.8	1.0	–	0.9	1.2	–	0.9	1.2	µs
Overload Recovery Time	t_{OR}		–	700	–	–	700	–	–	700	–	ns
Phase Margin	ϕ_o	0db Gain	–	47	–	–	47	–	–	47	–	degrees
Gain Margin	A_{180}	180° Open-Loop Phase Shift	–	9	–	–	9	–	–	9	–	dB
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 4)	100	300	–	100	300	–	100	300	–	pF

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-42E MIN	OP-42E TYP	OP-42E MAX	OP-42F MIN	OP-42F TYP	OP-42F MAX	OP-42G MIN	OP-42G TYP	OP-42G MAX	UNITS
Differential Input Impedance	Z_{IN}		–	10^{12}||6	–	–	10^{12}||6	–	–	10^{12}||6	–	Ω||pF
Open-Loop Output Resistance	R_O		–	50	–	–	50	–	–	50	–	Ω
Voltage Noise	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	–	2	–	–	2	–	–	2	–	$\mu V_{p\text{-}p}$
Voltage Noise Density	e_n	f_O = 10Hz	–	38	–	–	38	–	–	38	–	nV/√Hz
		f_O = 100Hz	–	16	–	–	16	–	–	16	–	
		f_O = 1kHz	–	13	–	–	13	–	–	13	–	
		f_O = 10kHz	–	12	–	–	12	–	–	12	–	
Current Noise Density	i_n	f_O = 1kHz	–	0.007	–	–	0.007	–	–	0.007	–	pA/√Hz
External V_{OS} Trim Range		R_{pot} = 20kΩ	–	4	–	–	4	–	–	4	–	mV
Long-Term V_{OS} Drift			–	5	–	–	5	–	–	5	–	µV/month
Supply Voltage Range	V_S		±8	±15	±20	±8	±15	±20	±8	±15	±20	V

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.
3. Settling-time is sample tested for A and E grades. Test circuit is shown in Figure 4. Settling-time for F grade is guaranteed but not tested.
4. Guaranteed but not tested.

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ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-42A MIN	OP-42A TYP	OP-42A MAX	UNITS
Offset Voltage	V_{OS}		–	0.3	1.0	mV
Input Bias Current	I_B	V_{CM} = 0V T_J = 25°C	–	80	200	pA
Input Offset Current	I_{OS}	V_{CM} = 0V T_J = 25°C	–	4	40	pA
Input Voltage Range	IVR	(Note 1)	±11	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	86	96	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	–	9	40	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ, V_O = ±10V, T_J = 25°C	500	900	–	V/mV
		R_L = 2kΩ, V_O = ±10V, T_J = 25°C	200	260	–	
		R_L = 1kΩ, V_O = ±10V, T_J = 25°C	100	170	–	
Output Voltage Swing	V_O	R_L = 1kΩ	±11.5	+12.5 –11.9	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+33 –28	±60	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.1	6.0	mA
Slew Rate	SR		45	52	–	V/µs
Full-Power Bandwidth	BW_p	(Note 2)	700	850	–	kHz
Gain-Bandwidth Product	GBW	f_O = 10kHz	–	10	–	MHz
Settling -Time	t_s	10V Step 0.01% (Note 3)	–	0.8	1.0	µs
Overload Recovery Time	t_{OR}		–	700	–	ns
Phase Margin	ϕ_o	0db Gain	–	47	–	degrees

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-42A MIN	OP-42A TYP	OP-42A MAX	UNITS
Gain Margin	A_{180}	180° Open-Loop Phase Shift	–	9	–	dB
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 4)	100	300	–	pF
Differential Input Impedance	Z_{IN}		–	10^{12}‖6	–	Ω‖pF
Open-Loop Output Resistance	R_O		–	50	–	Ω
Voltage Noise	$e_{n\ p-p}$	0.1Hz to 10Hz	–	2	–	μV_{p-p}
Voltage Noise Density	e_n	f_O = 10Hz	–	38	–	nV/√Hz
		f_O = 100Hz	–	16	–	
		f_O = 1kHz	–	13	–	
		f_O = 10kHz	–	12	–	
Current Noise Density	i_n	f_O = 1kHz	–	0.007	–	pA/√Hz
External V_{OS} Trim Range		R_{pot} = 20kΩ	–	4	–	mV
Long-Term V_{OS} Drift			–	5	–	µV/month
Supply Voltage Range	V_S		±8	±15	±20	V

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.
3. Settling-time is sample tested for A and E grades. Test circuit is shown in Figure 4. Settling-time for F grade is guaranteed but not tested.
4. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –25°C ≤ T_A ≤ 85°C for E/F grades, and –40°C ≤ T_A ≤ +85°C for G grade, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-42E MIN	OP-42E TYP	OP-42E MAX	OP-42F MIN	OP-42F TYP	OP-42F MAX	OP-42G MIN	OP-42G TYP	OP-42G MAX	UNITS
Offset Voltage	V_{OS}		–	0.4	1.2	–	0.6	2.5	–	2.0	6.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	4	10	–	8	–	–	8	–	µV/°C
Input Bias Current	I_B	(Note 1)	–	0.5	1.2	–	0.6	2.0	–	0.6	2.0	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.05	0.2	–	0.06	0.4	–	0.06	0.4	nA
Input Voltage Range	IVR	(Note 2)	±11	+12.5 –12.0	–	±11	+12.5 –12.0	–	±11	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	86	96	–	80	94	–	80	94	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	–	2	40	–	6	50	–	6	50	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ (Note 1)	200	500	–	200	500	–	200	500	–	V/mV
		R_L = 2kΩ V_O = ±10V	100	160	–	100	160	–	100	160	–	
Output Voltage Swing	V_O	R_L = 2kΩ	±11.0	+12.3 –11.8	–	±11.0	+12.3 –11.8	–	±11.0	+12.3 –11.8	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±8	–	±60	±8	–	±60	±8	–	±60	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.1	6.0	–	5.1	6.5	–	5.1	6.5	mA
Slew Rate	SR	R_L = 2kΩ	45	57	–	40	50	–	40	50	–	V/µs
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 3)	100	250	–	100	250	–	100	250	–	pF

NOTES:
1. T_j = 85°C for E/F/G Grades; T_j = 125°C for A grade.
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A ≤ 125°C for A grade, unless otherwise noted.

			OP-42A			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}		–	0.5	2.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	4	10	µV/°C
Input Bias Current	I_B	(Note 1)	–	6	20	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.2	1.0	nA
Input Voltage Range	IVR	(Note 2)	±11	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	80	94	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	–	10	50	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ (Note 1) R_L = 2kΩ V_O = ±10V	160 80	350 110	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±11.0	+12.3 –11.8	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±8	–	±60	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.1	6.0	mA
Slew Rate	SR	R_L = 2kΩ	40	52	–	V/µs
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 3)	100	250	–	pF

NOTES:
1. T_J = 85°C for E/F Grades; T_J = 125°C for A grade.
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

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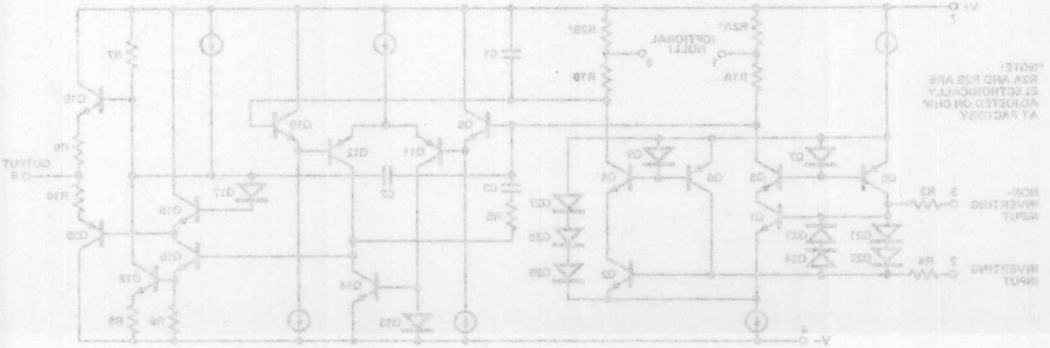


FEATURES

- Outstanding Gain Linearity
- Ultra High Gain ..... 5000V/mV Min
- Low V_{OS} Over Temperature ..... 60µV Max
- Excellent TCV_{OS} ..... 0.3µV/°C Max
- High PSRR ..... 3µV/V Max
- Low Power Consumption ..... 60mW Max
- Fits OP-07, 725, 108A/308A, 741 Sockets
- Available in Die Form

ORDERING INFORMATION †

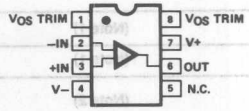
PACKAGE				OPERATING TEMPERATURE RANGE
TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-PIN	
OP77AJ*	OP77AZ*	–	–	MIL
OP77EJ	OP77EZ	–	–	IND
–	–	OP77EP	–	COM
OP77BJ*	OP77BZ*	–	OP77BRC/883	MIL
OP77FJ	OP77FZ	–	–	IND
–	–	OP77FP	–	COM
–	–	OP77GP	–	COM
–	–	OP77GS††	–	COM
–	–	OP77HP	–	XIND
–	–	OP77HS††	–	XIND

* For devices processed in total compliance to MIL-SDT-883, add /883 after part number. Consult factory for 883 data sheet.

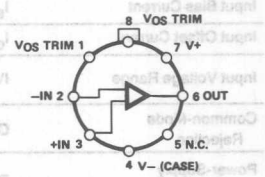
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS

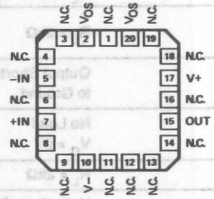


EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP
(Z-Suffix)



TO-99 (J-Suffix)

8-PIN SO
(S-Suffix)



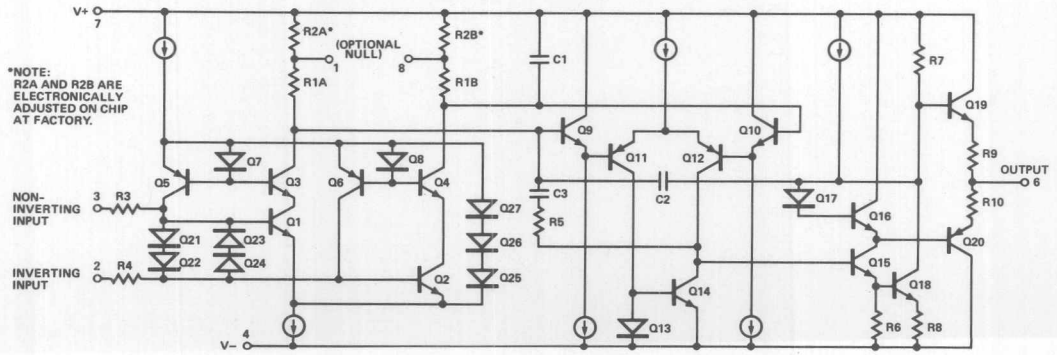
OP-77BRC/883
LCC
(RC-Suffix)

GENERAL DESCRIPTION

The OP-77 significantly advances the state-of-the-art in precision op amps. The OP-77's outstanding gain of 10,000,000 or more is maintained over the full ±10V output range. This exceptional gain-linearity eliminates incorrectable system nonlinearities common in previous monolithic op amps, and provides superior performance in high closed-loop-gain applications. Low initial V_{OS} drift and rapid stabilization time, combined with only 50mW power consumption, are significant improvements over previous designs. These characteristics, plus the exceptional TCV_{OS} of 0.3µV/°C maximum and the low V_{OS} of 25µV maximum, eliminates the need for V_{OS} adjustment and increases system accuracy over temperature.

PSRR of 3µV/V (110dB) and CMRR of 1.0µV/V maximum virtually eliminiate errors caused by power supply drifts and common-mode signals. This combination of outstanding characteristics makes the OP-77 ideally suited for high-resolution instrumentation and other tight error budget systems. *Continued*

SIMPLIFIED SCHEMATIC



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This product is available in six standard grades and five standard packages: the TO-99 can, the 8-pin mini-DIP in ceramic, SO or epoxy, and the 20-contact LCC.

The OP-77 is a direct or upgrade replacement for the OP-07, 05, 725, or 108A op amps. 741-types can be replaced by eliminating the V_{OS} adjust pot. For higher precision performance refer to OP-177.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
J, Z, and RC Packages ..... –65°C to +150°C
P Package ..... –65°C to +125°C
Operating Temperature Range
OP-77A, OP-77B (J, Z, RC) ..... –55°C to +125°C
OP-77E, OPP-77F (J, Z) ..... –25°C to +85°C
OP-77E, OP-77F, OP-77G (P, S) ..... 0°C to 70°
OP-77H (P, S) ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC, TC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77A MIN	OP-77A TYP	OP-77A MAX	OP-77B MIN	OP-77B TYP	OP-77B MAX	UNITS
Input Offset Voltage	V_{OS}		–	10	25	–	20	60	µV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)	–	0.2	–	–	0.2	–	µV/Mo
Input Offset Current	I_{OS}		–	0.3	1.5	–	0.3	2.8	nA
Input Bias Current	I_B		–0.2	1.2	2.0	–0.2	1.2	2.8	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	–	0.35	0.6	–	0.35	0.6	µVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 2) f_O = 100Hz (Note 2) f_O = 1000Hz (Note 2)	– – –	10.3 10.0 9.6	18.0 13.0 11.0	– – –	10.3 10.0 9.6	18.0 13.0 11.0	V/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	–	14	30	–	14	30	pAp-p
Input Noise Current Density	i_n	f_O = 10Hz (Note 2) f_O = 100Hz (Note 2) f_O = 1000Hz (Note 2)	– – –	0.32 0.14 0.12	0.80 0.23 0.17	– – –	0.32 0.14 0.12	0.80 0.23 0.17	pA/√Hz
Input Resistance – Differential-Mode	R_{IN}	(Note 3)	26	45	–	18.5	45	–	MΩ
Input Resistance – Common-Mode	R_{INCM}		–	200	–	–	200	–	GΩ
Input Voltage Range	IVR		±13	±14	–	±13	±14	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	–	0.1	1.0	–	0.1	1.0	µV/V
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	–	0.7	3	–	0.7	3	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, VO = ±10V	5000	12000	–	2000	8000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ R_L ≥ 2kΩ R_L ≥ 1kΩ	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	– – –	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	– – –	V
Slew Rate	SR	R_L ≥ 2kΩ (Note 2)	0.1	0.3	–	0.1	0.3	–	V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 2)	0.4	0.6	–	0.4	0.6	–	MHz
Open-Loop Output Resistance	R_O		–	60	–	–	60	–	Ω
Power Consumption	P_d	V_S = ±15V, No Load V_S = ±3V, No Load	– –	50 3.5	60 4.5	– –	50 3.5	60 4.5	mW
Offset Adjustment Range		R_P = 20kΩ	–	±3	–	–	±3	–	mV

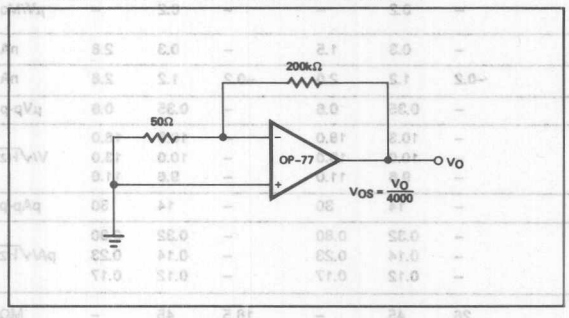
NOTES:
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV.
2. Sample tested.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

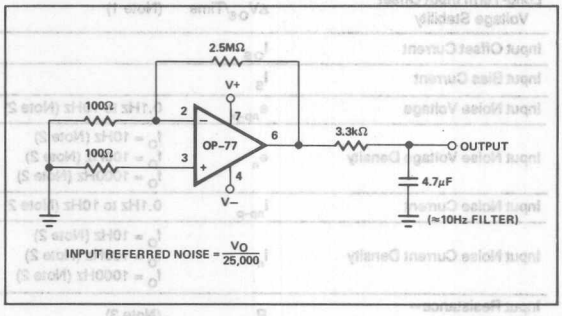
PARAMETER	SYMBOL	CONDITIONS	OP-77A MIN	OP-77A TYP	OP-77A MAX	OP-77B MIN	OP-77B TYP	OP-77B MAX	UNITS
Input Offset Voltage	V_{OS}		—	25	60	—	45	120	μV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	0.1	0.3	—	0.2	0.6	μV/°C
Input Offset Current	I_{OS}		—	0.5	2.2	—	0.5	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	1.5	25	—	1.5	50	pA/°C
Input Bias Current	I_B		−0.2	2.4	4	−0.2	2.4	6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	15	35	pA/°C
Input Voltage Range	IVR		±13	±13.5	—	±13	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	3	μV/V
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	1	3	—	1	5	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	2000	6000	—	1000	4000	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13.0	—	±12	±13.0	—	V
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	60	75	—	60	75	mW

NOTES:
1. OP-77A: TCV_{OS} is 100% tested.
2. Guaranteed by end-point limits.

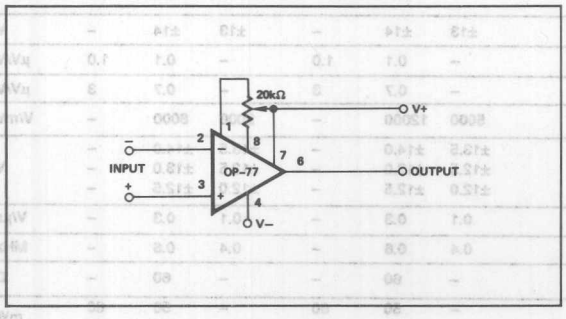
TYPICAL OFFSET VOLTAGE TEST CIRCUIT



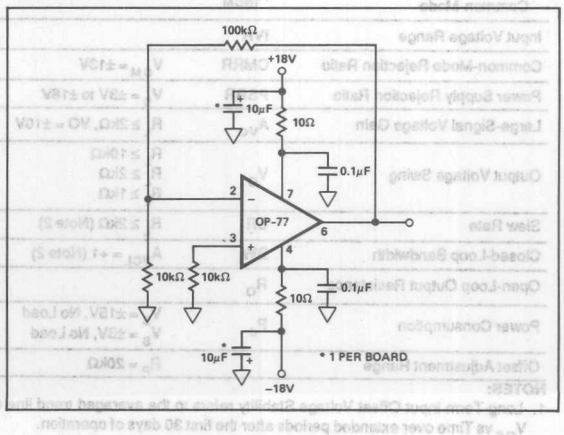
TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT



OPTIONAL OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

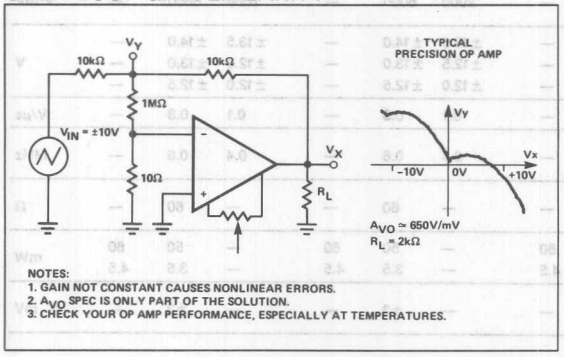
PARAMETER	SYMBOL	CONDITIONS	OP-77E MIN	OP-77E TYP	OP-77E MAX	OP-77F MIN	OP-77F TYP	OP-77F MAX	OP-77G/H MIN	OP-77G/H TYP	OP-77G/H MAX	UNITS
Input Offset Voltage	V_{OS}		—	10	25	—	20	60	—	50	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 1)	—	0.3	—	—	0.4	—	—	0.4	—	μV/Mo
Input Offset Current	I_{OS}		—	0.3	1.5	—	0.3	2.8	—	0.3	2.8	nA
Input Bias Current	I_B		−0.2	1.2	2.0	−0.2	1.2	2.8	−0.2	1.2	2.8	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		f_O = 100Hz (Note 2)	—	10.0	13.0	—	10.2	13.5	—	10.2	13.5	
		f_O = 1000Hz	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{Hz}$
		f_O = 100Hz (Note 2)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		f_O = 1000Hz	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	26	45	—	18.5	45	—	18.5	45	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	1.6	—	0.1	1.6	μV/V
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.7	3.0	—	0.7	3.0	—	0.7	3.0	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	5000	12000	—	2000	6000	—	2000	6000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±13.5	±14.0	—	±13.5	±14.0	—	±13.5	±14.0	—	V
		$R_L \geq 2k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	±12.5	±13.0	—	
		$R_L \geq 1k\Omega$	±12.0	±12.5	—	±12.0	±12.5	—	±12.0	±12.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 2)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O		—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	50	60	—	50	60	—	50	60	mW
		$V_S = \pm 3V$, No Load	—	3.5	4.5	—	3.5	4.5	—	3.5	4.5	
Offset Adjustment Range		$R_P = 20k\Omega$	—	±3	—	—	±3	—	—	±3	—	mV

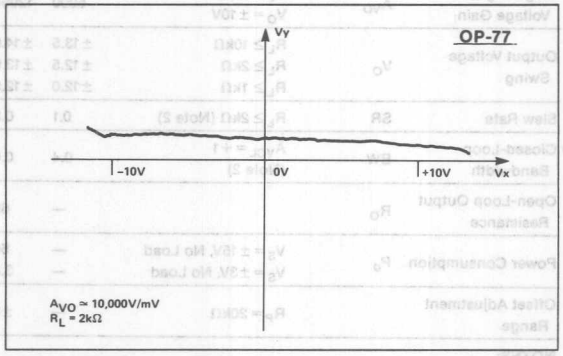
NOTES:
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. Sample tested.
3. Guaranteed by design.

Input Offset Voltage	V_{OS}	J, Z Packages		–	10	45	–	20	100	–	–	–	µV
		P Package		–	10	55	–	20	100	–	80	150	
Average Input Offset Voltage Drift	TCV_{OS}	J, Z Packages	(Note 1)	–	0.1	0.3	–	0.2	0.6	–	–	–	µV/°C
		P Package		–	0.3	0.6	–	0.4	1.0	–	0.7	1.2	
Input Offset Current	I_{OS}			–	0.5	2.2	–	0.5	4.5	–	0.5	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)		–	1.5	40	–	1.5	85	–	1.5	85	pA/°C
Input Bias Current	I_B	E, F, G Grades		–0.2	2.4	4.0	–0.2	2.4	6.0	–0.2	2.4	6.0	nA
		H Grade		–	–	–	–	–	–	–	2.4	±6.0	
Average Input Bias Current Drift	TCI_B	(Note 2)		–	8	40	–	15	60	–	15	60	pA/°C
Input Voltage Range	IVR			±13.0	±13.5	–	±13.0	±13.5	–	±13.0	±13.5	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V		–	0.1	1.0	–	0.1	3.0	–	0.1	3.0	µV/V
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V		–	1.0	3.0	–	1.0	5.0	–	1.0	5.0	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ V_O = ±10V		2000	6000	–	1000	4000	–	1000	4000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ		±12	±13.0	–	±12	±13.0	–	±12	±13.0	–	V
Power Consumption	P_d	V_S = ±15V, No Load		–	60	75	–	60	75	–	60	75	mW

NOTES:
1. OP-77E: TCV_{OS} is 100% tested on J and Z packages.
2. Guaranteed by end-point limits.

OPEN-LOOP GAIN LINEARITY





Actual open-loop voltage gain can vary greatly at various output voltages. All automated testers use end-point testing and therefore only show the average gain. This causes errors in high closed-loop gain circuits. Since this is so difficult for manufacturers to test, you should make your own evaluation. This simple test circuit makes it easy. An ideal op amp would show a horizontal scope trace.

This is the output gain linearity trace for the new OP-77. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. The average open-loop gain is truly impressive – approximately 10,000,000.

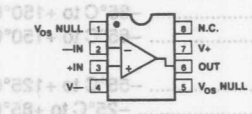
Precision, Low Voltage Micropower Operational Amplifier

OP90

FEATURES

- Single/Dual Supply Operation ..... +1.6V to +36V
  +0.8V to ±18V
- True Single-Supply Operation; Input and Output Voltage Ranges Include Ground
- Low Supply Current ..... 20μA Max
- High Output Drive ..... 5mA Min
- Low Input Offset Voltage ..... 150μV Max
- High Open-Loop Gain ..... 700V/mV Min
- Outstanding PSRR ..... 5.6μV/V Max
- Standard 741 Pinout with Nulling to V–
- Available in Die Form

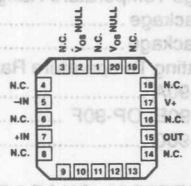
PIN CONNECTIONS



8-PIN HERMETIC DIP
(Z-Suffix)

8-PIN EPOXY MINI-DIP
(P-Suffix)

8-PIN SO (S-Suffix)



OP-90 ARC/883
LCC (RC-Suffix)

GENERAL DESCRIPTION

The OP-90 is a high performance micropower op amp that operates from a single supply of +1.6V to +36V or from dual supplies of ±0.8 to ±18V. Input voltage range includes the negative rail allowing the OP-90 to accommodate input signals down to ground in single supply operation. The OP-90's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

The OP-90 draws less than 20μA of quiescent supply current, while able to deliver over 5mA of output current to a load. Input offset voltage is below 150μV eliminating the need for external nulling. Gain exceeds 700,000 and common-mode rejection is better than 100dB. The power supply-rejection ratio of under 5.6μV/V minimizes offset voltage changes experienced in battery powered systems.

The low offset voltage and high gain offered by the OP-90 bring precision performance to micropower applications. The minimal voltage and current requirements of the OP-90 suit it for battery and solar powered applications, such as portable instruments, remote sensors, and satellites.

ORDERING INFORMATION †

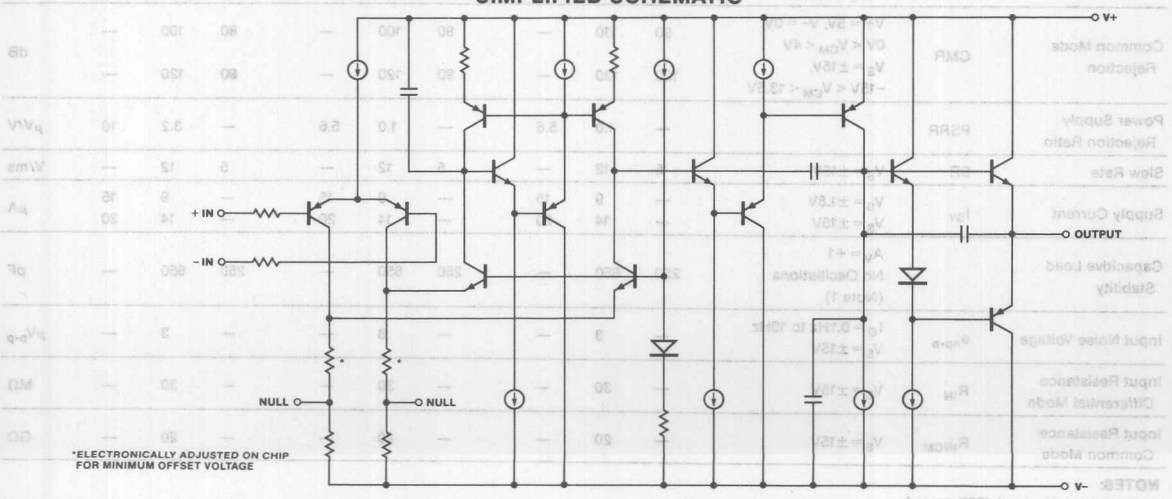
T_A = 25°C V_{OS} MAX (mV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
150	OP90AZ*	–	OP90ARC/883	MIL
150	OP90EZ	–	–	IND
250	OP90FZ	–	–	IND
450	–	OP90GP	–	XIND
450	–	OP90GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

SIMPLIFIED SCHEMATIC



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... [(V–) – 20V] to [(V+) + 20V]
Common-Mode Input Voltage
..... [(V–) – 20V] to [(V+) + 20V]
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
Z Package ..... –65°C to +150°C
P Package ..... –65°C to +150°C
Operating Temperature Range
OP-90A ..... –55°C to +125°C
OP-90E, OP-90F ..... –25°C to +85°C
OP-90G ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±1.5V to ±15V, T_A = +25°C, unless otherwise noted.

			OP-90A/E			OP-90F			OP-90G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	50	150	—	75	250	—	125	450	µV
Input Offset Current	I_{OS}	V_{CM} = 0V	—	0.4	3	—	0.4	5	—	0.4	5	nA
Input Bias Current	I_B	V_{CM} = 0V	—	4.0	15	—	4.0	20	—	4.0	25	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V										
		R_L = 100kΩ	700	1200	—	500	1000	—	400	800	—	
		R_L = 10kΩ	350	600	—	250	500	—	200	400	—	
		R_L = 2kΩ	125	250	—	100	200	—	100	200	—	V/mV
		V+ = 5V, V– = 0V, 1V < V_O < 4V										
		R_L = 100kΩ	200	400	—	125	300	—	100	250	—	
		R_L = 10kΩ	100	180	—	75	140	—	70	140	—	
Input Voltage Range	IVR	V+ = 5V, V– = 0V	0/4	—	—	0/4	—	—	0/4	—	—	V
		V_S = ±15V (Note 2)	–15/13.5	—	—	–15/13.5	—	—	–15/13.5	—	—	
	V_O	V_S = ±15V										
		R_L = 10kΩ	±14	±14.2	—	±14	±14.2	—	±14	±14.2	—	V
		R_L = 2kΩ	±11	±12	—	±11	±12	—	±11	±12	—	
Output Voltage Swing	V_{OH}	V+ = 5V, V– = 0V										
		R_L = 2kΩ	4.0	4.2	—	4.0	4.2	—	4.0	4.2	—	V
	V_{OL}	V+ = 5V, V– = 0V										
		R_L = 10kΩ	—	100	500	—	100	500	—	100	500	µV
Common Mode Rejection	CMR	V+ = 5V, V– = 0V, 0V < V_{CM} < 4V	90	110	—	80	100	—	80	100	—	dB
		V_S = ±15V, –15V < V_{CM} < 13.5V	100	130	—	90	120	—	90	120	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	1.0	5.6	—	3.2	10	µV/V
Slew Rate	SR	V_S = ±15V	5	12	—	5	12	—	5	12	—	V/ms
Supply Current	I_{SY}	V_S = ±1.5V	—	9	15	—	9	15	—	9	15	µA
		V_S = ±15V	—	14	20	—	14	20	—	14	20	
Capacitive Load Stability		A_V = +1 No Oscillations (Note 1)	250	650	—	250	650	—	250	650	—	pF
Input Noise Voltage	e_{np-p}	f_O = 0.1Hz to 10Hz, V_S = ±15V	—	3	—	—	3	—	—	3	—	μV_{p-p}
Input Resistance Differential Mode	R_{IN}	V_S = ±15V	—	30	—	—	30	—	—	30	—	MΩ
Input Resistance Common Mode	R_{INCM}	V_S = ±15V	—	20	—	—	20	—	—	20	—	GΩ

NOTES:
1. Guaranteed but not 100% tested.
2. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-90A MIN	OP-90A TYP	OP-90A MAX	UNITS
Input Offset Voltage	V_{OS}		—	80	400	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	2.5	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	1.5	5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.0	20	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_O = \pm10V$				V/mV
		$R_L = 100k\Omega$	225	400	—	
		$R_L = 10k\Omega$	125	240	—	
		$R_L = 2k\Omega$	50	110	—	
		$V+ = 5V$, $V- = 0V$, $1V < V_O < 4V$				
		$R_L = 100k\Omega$	100	200	—	
		$R_L = 10k\Omega$	50	110	—	
Input Voltage Range	IVR	$V+ = 5V$, $V- = 0V$ (Note 1)	0/3.5	—	—	V
		$V_S = \pm15V$	−15/13.5	—	—	
Output Voltage Swing	V_O	$V_S = \pm15V$				V
		$R_L = 10k\Omega$	±13.5	±13.7	—	
		$R_L = 2k\Omega$	±10.5	±11.5	—	
	V_{OH}	$V+ = 5V$, $V- = 0V$				V
		$R_L = 2k\Omega$	3.9	4.1	—	
	V_{OL}	$V+ = 5V$, $V- = 0V$				μV
		$R_L = 10k\Omega$	—	100	500	
Common Mode Rejection	CMR	$V+ = 5V$, $V- = 0V$, $0V < V_{CM} < 3.5V$	85	105	—	dB
		$V_S = \pm15V$, $-15V < V_{CM} < 13.5V$	95	115	—	
Power Supply Rejection Ratio	PSRR		—	3.2	10	μV/V
Supply Current	I_{SY}	$V_S = \pm1.5V$	—	15	25	μA
		$V_S = \pm15V$	—	19	30	

NOTE:
1. Guaranteed by CMR test.

9

PARAMETER	SYMBOL	CONDITIONS	OP-90E MIN	OP-90E TYP	OP-90E MAX	OP-90F MIN	OP-90F TYP	OP-90F MAX	OP-90G MIN	OP-90G TYP	OP-90G MAX	UNITS
Input Offset Voltage	V_{OS}		—	70	270	—	110	550	—	180	675	µV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	2	—	0.6	5	—	1.2	5	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	—	0.8	3	—	1.0	5	—	1.3	7	nA
Input Bias Current	I_B	V_{CM} = 0V	—	4.0	15	—	4.0	20	—	4.0	25	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V										
		R_L = 100kΩ	500	800	—	350	700	—	300	600	—	
		R_L = 10kΩ	250	400	—	175	350	—	150	250	—	
		R_L = 2kΩ	100	200	—	75	150	—	75	125	—	V/mV
		V+ = 5V, V− = 0V, 1V < V_O < 4V										
		R_L = 100kΩ	150	280	—	100	220	—	80	160	—	
		R_L = 10kΩ	75	140	—	50	110	—	40	90	—	
Input Voltage Range	IVR	V+ = 5V, V− = 0V	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	
		V_S = ±15V (Note 1)	−15/13.5	—	—	−15/13.5	—	—	−15/13.5	—	—	V
Output Voltage Swing	V_O	V_S = ±15V										
		R_L = 10kΩ	±13.5	±14	—	±13.5	±14	—	±13.5	±14	—	V
		R_L = 2kΩ	±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	
	V_{OH}	V+ = 5V, V− = 0V										
		R_L = 2kΩ	3.9	4.1	—	3.9	4.1	—	3.9	4.1	—	V
	V_{OL}	V+ = 5V, V− = 0V										
		R_L = 10kΩ	—	100	500	—	100	500	—	100	500	µV
Common Mode Rejection	CMR	V+ = 5V, V− = 0V, 0V < V_{CM} < 3.5V	90	110	—	80	100	—	80	100	—	
		V_S = ±15V, −15V < V_{CM} < 13.5V	100	120	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	3.2	10	—	5.6	17.8	µV/V
Supply Current	I_{SY}	V_S = ±1.5V	—	13	25	—	13	25	—	12	25	
		V_S = ±15V	—	17	30	—	17	30	—	16	30	µA

NOTE:
1. Guaranteed by CMR test.

FEATURES

- Low Supply Current ..... 600μA Max
- OP-07 Type Performance
  - Offset Voltage ..... 20μV Max
  - Offset Voltage Drift ..... 0.6μV/°C Max
- Very Low Bias Current
  - 25°C ..... 100pA Max
  - –55°C to +125°C ..... 250pA Max
- High Common-Mode Rejection ..... 114dB Min
- Extended Industrial Temp. Range ..... –40°C to +85°C
- Available in Die Form

ORDERING INFORMATION †

PACKAGE			OPERATING TEMPERATURE RANGE
TO-99	CERDIP	PLASTIC	
OP97AJ*	OP97AZ*	–	MIL
OP97EJ	OP97EZ	OP97EP	XIND
OP97FJ	OP97FZ	OP97FP	XIND
–	–	OP97FS††	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

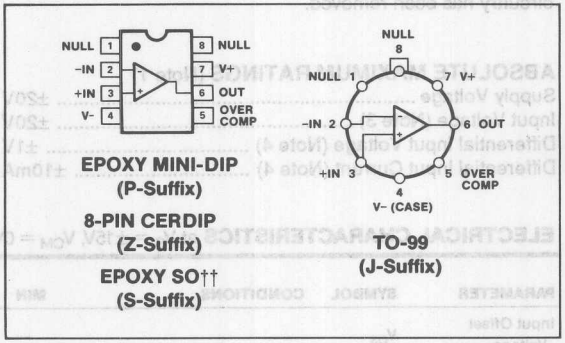
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-97 is a low-power alternative to the industry-standard OP-07 precision amplifier. The OP-97 maintains the standards of performance set by the OP-07 while utilizing only 600μA supply current, less than 1/6 that of an OP-07. Offset voltage is an ultra-low 25μV, and drift over temperature is below 0.6μV/°C. External offset trimming is not required in the majority of circuits.

PIN CONNECTIONS



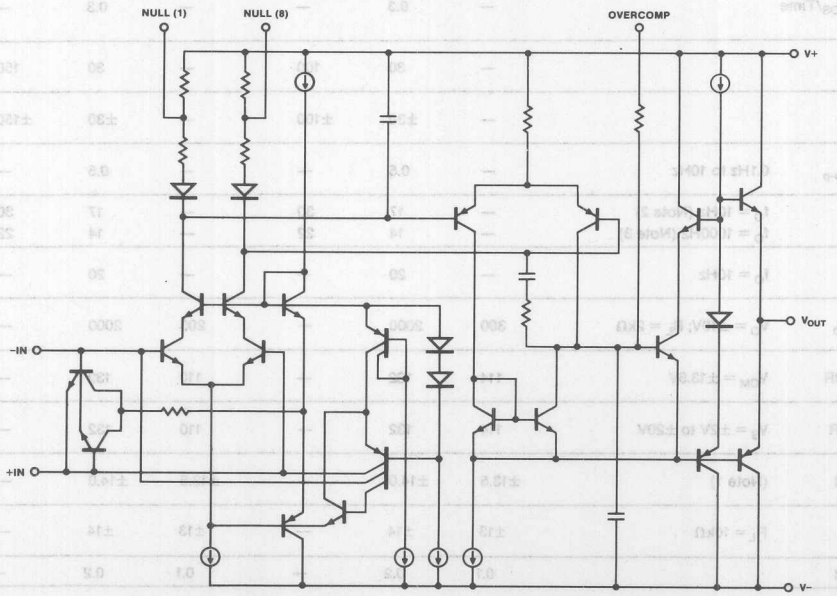
EPOXY MINI-DIP (P-Suffix)

8-PIN CERDIP (Z-Suffix)

EPOXY SO†† (S-Suffix)

TO-99 (J-Suffix)

SIMPLIFIED SCHEMATIC



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OP97

Improvements have been made over OP-07 specifications in several areas. Notable is bias current, which remains below 250pA over the full military temperature range. The OP-97 is ideal for use in precision long-term integrators or sample-and-hold circuits that must operate at elevated temperatures.

Common-mode rejection and power-supply rejection are also improved with the OP-97, at 114dB minimum over wider ranges of common-mode or supply voltage. Outstanding PSR, a supply range specified from ±2.25V to ±20V and the OP-97's minimal power requirements combine to make the OP-97 a preferred device for portable and battery-powered instruments.

The OP-97 conforms to the OP-07 pinout, with the null potentiometer connected between pins 1 and 8 with the wiper to V+. The OP-97 will upgrade circuit designs using 725, OP05, OP07, OP12, and 1012 type amplifiers. It may replace 741-type amplifiers in circuits without nulling or where the nulling circuitry has been removed.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Input Voltage (Note 3) ..... ±20V
Differential Input Voltage (Note 4) ..... ±1V
Differential Input Current (Note 4) ..... ±10mA
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
OP-97A (J, Z) ..... –55°C to +125°C
OP-97E, F (J, P, Z, S) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.
3. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
4. The OP-97's inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.

			OP-97A/E			OP-97F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	10	25	—	30	75	µV
Long-Term Offset Voltage Stability	ΔV_{OS}/Time		—	0.3	—	—	0.3	—	µV/Month
Input Offset Current	I_{OS}		—	30	100	—	30	150	pA
Input Bias Current	I_B		—	±30	±100	—	±30	±150	pA
Input Noise Voltage	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	$\mu V_{p\text{-}p}$
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 2) f_O = 1000Hz (Note 3)	— —	17 14	30 22	— —	17 14	30 22	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
Input Noise Current Density	i_N	f_O = 10Hz	—	20	—	—	20	—	$fA/\sqrt{Hz}$
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V; R_L = 2kΩ	300	2000	—	200	2000	—	V/mV
Common-Mode Rejection	CMR	V_{CM} = ±13.5V	114	132	—	110	132	—	dB
Power-Supply Rejection	PSR	V_S = ±2V to ±20V	114	132	—	110	132	—	dB
Input Voltage Range	IVR	(Note 1)	±13.5	±14.0	—	±13.5	±14.0	—	V
Output Voltage Swing	V_O	R_L = 10kΩ	±13	±14	—	±13	±14	—	V
Slew Rate	SR		0.1	0.2	—	0.1	0.2	—	V/µs

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted. (Continued.)

PARAMETER	SYMBOL	CONDITIONS	OP-97A/E MIN	OP-97A/E TYP	OP-97A/E MAX	OP-97F MIN	OP-97F TYP	OP-97F MAX	UNITS
Differential Input Resistance	R_{IN}	(Note 4)	30	—	—	30	—	—	MΩ
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.4	0.9	—	0.4	0.9	—	MHz
Supply Current	I_{SY}		—	380	600	—	380	600	μA
Supply Voltage	V_S	Operating Range	±2	±15	±20	±2	±15	±20	V

NOTES:
1. Guaranteed by CMR test.
2. 10Hz noise voltage density is sample tested. Devices 100% tested for noise are available on request.
3. Sample tested.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $-40°C \le T_A \le +85°C$ for the OP-97E/F and $-55°C \le T_A \le +125°C$ for the OP-97A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-97A/E MIN	OP-97A/E TYP	OP-97A/E MAX	OP-97F MIN	OP-97F TYP	OP-97F MAX	UNITS
Input Offset Voltage	V_{OS}		—	25	60	—	60	200	μV
Average Temperature Coefficient of V_{OS}	TCV_{OS}	S-Package	—	0.2	0.6	—	0.3	2.0	μV/°C
			—	—	—	—	0.3	—	
Input Offset Current	I_{OS}		—	60	250	—	80	750	pA
Average Temperature Coefficient of I_{OS}	TCI_{OS}		—	0.4	2.5	—	0.6	7.5	pA/°C
Input Bias Current	I_B		—	±60	±250	—	±80	±750	pA
Average Temperature Coefficient of I_B	TCI_B		—	0.4	2.5	—	0.6	7.5	pA/°C
Large-Signal Voltage Gain	A_{VO}	$V_O = +10V$; $R_L = 2k\Omega$	200	1000	—	150	1000	—	V/mV
Common-Mode Rejection	CMR	$V_{CM} = \pm13.5V$	108	128	—	108	128	—	dB
Power-Supply Rejection	PSR	$V_S = \pm2.5V$ to ±20V	108	126	—	108	128	—	dB
Input Voltage Range	IVR	(Note 1)	±13.5	±14.0	—	±13.5	±14.0	—	V
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±13	±14	—	±13	±14	—	V
Slew Rate	SR		0.05	0.15	—	0.05	0.15	—	V/μs
Supply Current	I_{SY}		—	400	800	—	400	800	μA
Supply Voltage	V_S	Operating Range	±2.5	±15	±20	±2.5	±15	±20	V

NOTES:
1. Guaranteed by CMR test.

Low Noise, Low Drift Single-Supply Operational Amplifiers

OP-113/OP-213/OP-413*

FEATURES

Single- or Dual-Supply Operation
Low Noise: 4.7 nV/$\sqrt{Hz}$ @ 1 kHz
Wide Bandwidth: 3.4 MHz
Low Offset Voltage: 100 μV
Very Low Drift: 0.2 μV/°C
Unity Gain Stable
No Phase Reversal

APPLICATIONS

Digital Scales
Multimedia
Strain Gages
Battery Powered Instrumentation
Temperature Transducer Amplifier

GENERAL DESCRIPTION

The OP-113 family dual operational amplifier features the lowest noise and drift of any single-supply amplifier. It has been designed for systems with internal calibration. Often these processor based systems are capable of calibrating corrections for offset and gain, but they cannot correct for temperature drifts and noise. Optimized for these parameters, the OP-113 family can be used to take advantage of superior analog performance combined with digital correction. Many systems using internal calibration operate from unipolar supplies, usually either +5 volts or +12 volts. The OP-113 family is designed to operate from single supplies from +4 volts to +36 volts, and to maintain its low noise and precision performance.

The OP-113 family is unity gain stable and has a typical gain bandwidth product of 3.4 MHz. Slew rate is in excess of 1 V/μs. Noise density is a very low 4.7 nV/$\sqrt{Hz}$, and noise in the 0.1 Hz to 10 Hz band is 120 nV p-p. Input offset voltage is guaranteed and offset drift is guaranteed to be less than 0.8 μV/°C. Input common-mode range includes the negative supply and to within 1 volt of the positive supply over the full supply range. Phase reversal protection is designed into the OP-113 family for cases where input voltage range is exceeded. Output voltage swings also include the negative supply and go to within 1 volt of the positive rail. The output is capable of sinking and sourcing current throughout its range and is specified with 600 Ω loads.

Digital scales and other strain gage applications benefit from the very low noise and low drift of the OP-113 family. Other applications include use as a buffer or amplifier for both A/D and D/A sigma-delta converters. Often these converters have high resolutions requiring the lowest noise amplifier to utilize their full potential. Many of these converters operate in either single-supply or low-supply voltage systems, and attaining the greater signal swing possible increases system performance. No other single supply amplifier provides better performance for these applications.

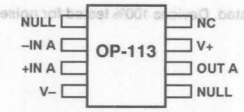
The OP-113 family is specified for single +5 volt and dual ±15 volt operation over the XIND—extended industrial (−40°C to +85°C) temperature range. They are available in plastic and ceramic 8-pin DIPs, plus SOIC-8 surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.

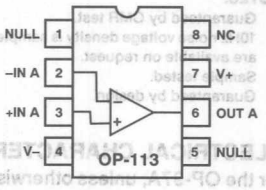
*Protected by U.S. Patent No. 5,146,181.

PIN CONNECTIONS

8-Lead Narrow-Body SO (S Suffix)

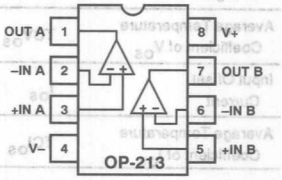


8-Lead Epoxy DIP (P Suffix)
8-Lead Ceramic DIP (Z Suffix)

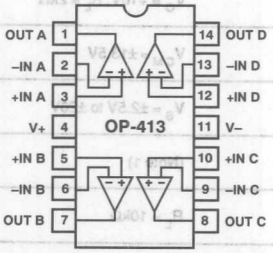


8-Lead Narrow-Body SO (S Suffix)

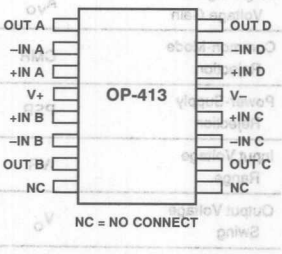
8-Lead Epoxy DIP (P Suffix)
8-Lead Ceramic DIP (Z Suffix)



14-Lead Epoxy DIP (P Suffix)
14-Lead Ceramic DIP (Y Suffix)



16-Lead Wide-Body SOL (S Suffix)



SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	OP-113E/OP-413E Min	Typ	Max	OP-113F/OP-413F Min	Typ	Max	Units
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP-113			75			150	µV
		−40°C ≤ T_A ≤ +85°C			125			225	µV
		OP-213			100			250	µV
		−40°C ≤ T_A ≤ +85°C			150			325	µV
		OP-413			125			275	µV
		−40°C ≤ T_A ≤ +85°C			175			350	µV
Input Bias Current	I_B	V_{CM} = 0 V,		240	600			600	nA
		−40°C ≤ T_A ≤ +85°C			700			700	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V							
		−40°C ≤ T_A ≤ +85°C			50			50	nA
Input Voltage Range	V_{CM}		−15		+14	−15		+14	V
Common-Mode Rejection	CMR	−15 V ≤ V_{CM} ≤ +14 V	100	116		96			dB
		−15 V ≤ V_{CM} ≤ +14 V,							
		−40°C ≤ T_A ≤ +85°C	97	116		94			dB
Large Signal Voltage Gain	A_{VO}	OP-113, OP-213, R_L = 600 Ω,							
		−40°C ≤ T_A ≤ +85°C	1	2.4		1			V/µV
		OP-413, R_L = 1 kΩ,							
		−40°C ≤ T_A ≤ +85°C	1	2.4		1			V/µV
		R_L = 2 kΩ,							
		−40°C ≤ T_A ≤ +85°C	2	8		2			V/µV
Long Term Offset Voltage[1]	V_{OS}	Note 1			150			300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 2		0.2	0.8			1.5	µV/°C
OUTPUT CHARACTERISTICS									
Output Voltage Swing High	V_{OH}	R_L = 2 kΩ	+14			+14			V
		R_L = 2 kΩ,							
		−40°C ≤ T_A ≤ +85°C	+13.9			+13.9			V
Output Voltage Swing Low	V_{OL}	R_L = 2 kΩ			−14.5			−14.5	V
		R_L = 2 kΩ,							
		−40°C ≤ T_A ≤ +85°C			−14.5			−14.5	V
Short Circuit Limit	I_{SC}			±40			±40		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = ±2 V to ±18 V	103	120		100			dB
		V_S = ±2 V to ±18 V							
		−40°C ≤ T_A ≤ +85°C	100	120		97			dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = 0 V, R_L = ∞,							
		V_S = ±18 V			2			2	mA
		−40°C ≤ T_A ≤ +85°C			2.5			2.5	mA
Supply Voltage Range	V_S		+4		±18	+4		±18	V
AUDIO PERFORMANCE									
THD + Noise		V_{IN} = 3 V rms, R_L = 2 kΩ							
		f = 1 kHz,		0.0009			0.0009		%
Voltage Noise Density	e_n	f = 10 Hz		9			9		nV/√Hz
		f = 1 kHz		4.7			4.7		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.4			0.4		pA/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		120			120		nV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ	0.8	1.2		0.8	1.2		V/µs
Gain Bandwidth Product	GBP			3.4			3.4		MHz
Channel Separation		V_{OUT} = 10 V p-p							
		R_L = 2 kΩ, f = 1 kHz		105			105		dB
Settling Time	t_S	to 0.01%, 0 to 10 V Step		9			9		µs

NOTES

[1]Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 120°C, with an LTPD of 1.3.

[2]Guaranteed specifications, based on characterization data.

Specifications subject to change without notice.

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Parameter	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Units
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP-113			125			175	μV
		$-40°C \le T_A \le +85°C$			175			250	μV
		OP-213			150			300	μV
		$-40°C \le T_A \le +85°C$			225			375	μV
		OP-413			175			325	μV
		$-40°C \le T_A \le +85°C$			250			400	μV
Input Bias Current	I_B	$V_{CM} = 0$ V, $V_{OUT} = 2$		300	650			650	nA
		$-40°C \le T_A \le +85°C$			750			750	nA
Input Offset Current	I_{OS}	$V_{CM} = 0$ V, $V_{OUT} = 2$							
		$-40°C \le T_A \le +85°C$			50			50	nA
Input Voltage Range	V_{CM}		0		+4			+4	V
Common-Mode Rejection	CMR	$0 \le V_{CM} \le 4$ V	93	106		90			dB
		$0 \le V_{CM} \le 4$ V							
		$-40°C \le T_A \le +85°C$	90			87			dB
Large Signal Voltage Gain	A_{VO}	OP-113, OP-213, $R_L = 600$, 2k							
		$0.01 \text{ V} \le V_{OUT} \le 3.9$ V	2			2			V/μV
		OP-413, $R_L = 600$, 2k							
		$0.01 \text{ V} \le V_{OUT} \le 3.9$ V	1			1			V/μV
Long Term Offset Voltage[1]	V_{OS}	Note 1			200			350	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 2		0.2	1.0			1.5	μV/°C
OUTPUT CHARACTERISTICS									
Output Voltage Swing High	V_{OH}	$R_L = 600\ \Omega$	4.0			4.0			V
		$R_L = 100$ kΩ, $-40°C \le T_A \le +85°C$	4.1			4.1			V
		$R_L = 600\ \Omega$, $-40°C \le T_A \le +85°C$	3.9			3.9			V
Output Voltage Swing Low	V_{OL}	$R_L = 600\ \Omega$			3.0			3.0	mV
		$R_L = 100$ kΩ			3.5			3.5	mV
		$R_L = 600\ \Omega$, $-40°C \le T_A \le +85°C$			4.0			4.0	mV
		$R_L = 100$ kΩ, $-40°C \le T_A \le +85°C$			5.0			5.0	mV
Short Circuit Limit	I_{SC}			±30			±30		mA
POWER SUPPLY									
Supply Current	I_{SY}	$V_{OUT} = 2.0$ V, No Load		1.35	1.75			1.75	mA
Supply Current	I_{SY}	$-40°C \le T_A \le +85°C$			2.0			2.0	mA
AUDIO PERFORMANCE									
THD + Noise		$V_{OUT} = 0$ dBu, f = 1 kHz		0.001			0.001		%
Voltage Noise Density	e_n	f = 10 Hz		9			9		$nV/\sqrt{Hz}$
Voltage Noise Density	e_n	f = 1 kHz		4.7			4.7		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		0.45			0.45		$pA/\sqrt{Hz}$
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		120			120		nV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	$R_L = 2$ kΩ	0.6	0.9		0.6			V/μs
Gain Bandwidth Product	GBP			3.5			3.5		MHz
Settling Time	t_S	to 0.1%, 2 V Step		5.8			5.8		μs

NOTES

[1]Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 120°C, with an LTPD of 1.3.

[2]Guaranteed specifications, based on characterization data.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = +5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}	V_S = ±15 V	±100	µV max
		V_{CM} = 0, V_{OUT} = 2 V	±150	µV max
Input Bias Current	I_B	V_{CM} = 0 V	650	nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	50	nA max
Input Voltage Range[1]			0 to 4	V min
Common-Mode Rejection	CMRR	0 ≤ V_{CM} ≤ 4 V	90	dB min
Power Supply Rejection Ratio	PSRR	V_S = ±2 V to ±18 V	100	µV/V
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_S = ±15 V	2	V/µV min
Output Voltage Swing High	V_{OH}	R_L = 600 Ω	4.0	V min
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞, V_S, V_S = ±18 V	2.0	mA max/amp

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.

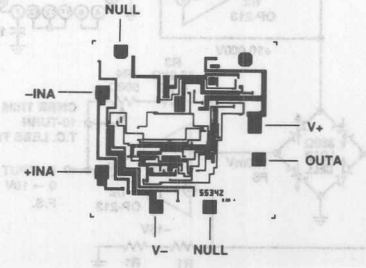
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage . . . . . ±18 V
Differential Input Voltage . . . . . ±10 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
Z, Y Package . . . . . −65°C to +175°C
P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
OP-113/OP-213/OP-413A, B . . . . . −55°C to +125°C
OP-113/OP-213/OP-413E, F . . . . . −40°C to +85°C
Junction Temperature Range
Z, Y Package . . . . . −65°C to +150°C
P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Cerdip (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

DICE CHARACTERISTICS



OP-113 Die Size 0.064 X 0.0627 inch, 3,968 sq. mils.
Substrate (Die Backside) Is Connected to V+.
Transistor Count, 66.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP113AZ/883	−55°C to +125°C	8-Pin Cerdip	Q-8
OP113BZ/883	−55°C to +125°C	8-Pin Cerdip	Q-8
OP113EZ	−40°C to +85°C	8-Pin Cerdip	Q-8
OP113EP	−40°C to +85°C	8-Pin Plastic DIP	N-8
OP113ES	−40°C to +85°C	8-Pin SOIC	SO-8
OP113FP	−40°C to +85°C	8-Pin Plastic DIP	N-8
OP113FS	−40°C to +85°C	8-Pin SOIC	SO-8
OP113GBC	+25°C	DICE	
OP213AZ/883	−55°C to +125°C	8-Pin Cerdip	Q-8
OP213BZ/883	−55°C to +125°C	8-Pin Cerdip	Q-8
OP213EZ	−40°C to +85°C	8-Pin Cerdip	Q-8
OP213EP	−40°C to +85°C	8-Pin Plastic DIP	N-8
OP213ES	−40°C to +85°C	8-Pin SOIC	SO-8
OP213FP	−40°C to +85°C	8-Pin Plastic DIP	N-8
OP213FS	−40°C to +85°C	8-Pin SOIC	SO-8
OP213GBC	+25°C	DICE	
OP413AY/883	−55°C to +125°C	14-Pin Cerdip	Q-14
OP413BY/883	−55°C to +125°C	14-Pin Cerdip	Q-14
OP413EY	−40°C to +85°C	14-Pin Cerdip	Q-14
OP413EP	−40°C to +85°C	14-Pin Plastic DIP	N-14
OP413ES	−40°C to +85°C	16-Pin SOL	SOL-16
OP413FP	−40°C to +85°C	14-Pin Plastic DIP	N-14
OP413FS	−40°C to +85°C	16-Pin SOL	SOL-16
OP413GBC	+25°C	DICE	

*For outline information see Package Information section.

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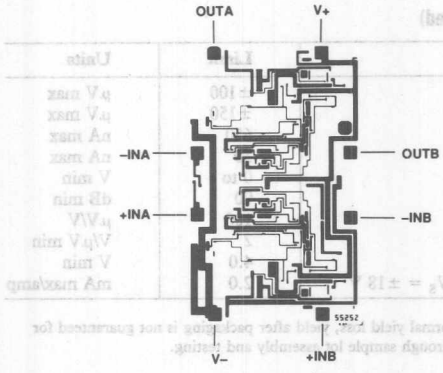
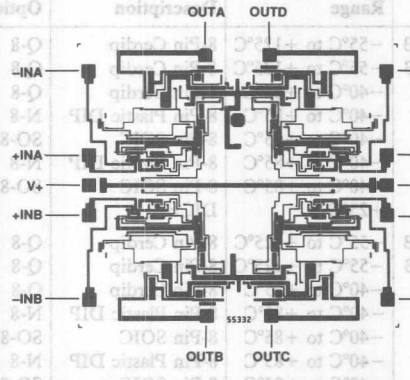


OP-213 Die Size 0.062 X 0.097 inch, 6,014 sq. mils. Substrate (Die Backside) Is Connected to V+. Transistor Count, 132.



OP-413 Die Size 0.106 X 0.106 inch, 10,176 sq. mils. Substrate (Die Backside) Is Connected to V+. Transistor Count, 256.

APPLICATIONS

The OP-113, OP-213 and OP-413 form a new family of high performance amplifiers that feature precision performance in standard dual supply configurations, and, more importantly, maintain precision performance when a single power supply is used. In addition to accurate dc specifications, it is the lowest noise single supply amplifier available with only 4.7 nV/$\sqrt{\text{Hz}}$ typical noise density.

Single supply applications have special requirements due to the generally reduced dynamic range of the output signal. Single supply applications are often operated at voltages of +5 volts or +12 volts, compared to dual supply applications with supplies of ±12 volts or ±15 volts. This results in reduced output swings. Where a dual supply application may often have 20 volts of signal output swing, single supply applications are limited to at most the supply range, and more commonly several volts below the supply. In order to attain the greatest swing the single supply output stage must swing closer to the supply rails than in dual supply applications.

The OP-113 family has a new patented output stage that allows the output to swing closer to ground, or the negative supply, than previous bipolar output stages. Previous op amps had outputs that could swing to within about ten millivolts of the negative supply in single supply applications. However the OP-113 family combines both a bipolar and a CMOS device in the output stage, enabling it to swing to within a few hundred microvolts of ground.

When operating with reduced supply voltages, the input range is also reduced. This reduction in signal range results in reduced signal-to-noise ratio, for any given amplifier. There are only two ways to improve this; increase the signal range or reduce the noise. The OP-113 family addresses both of these parameters. Input signal range is from the negative supply to within one volt of the positive supply over the full supply range. Competitive parts have input ranges that are a half a volt to five volts less than this. Noise has also been optimized in the OP-113 family. At 4.7 nV/$\sqrt{\text{Hz}}$, it is less than one fourth that of competitive devices.

Phase Reversal

The OP-113 family is protected against phase reversal as long as both of the inputs are within the supply ranges. However, if there is a possibility of either input going below the negative supply (or ground in the single supply case), then the inputs should be protected with a series resistor to limit input current to 2 mA.

OP-113 Offset Adjust

The OP-113 has the facility for external offset adjustment, using the industry standard arrangement. Pins 1 and 5 are used in conjunction with a potentiometer of 10 kΩ total resistance, connected with the wiper to V− (or ground in single supply applications). The total adjustment range is about ±2 mV using this configuration.

Adjusting the offset to zero has minimal effect on offset drift (assuming the potentiometer has a tempco of less than 1000 ppm/°C). Adjustment away from zero, however, (like all bipolar amplifiers) will result in a TCV_{OS} of approximately 3.3 μV/°C for every millivolt of induced offset.

It is, therefore, not generally recommended that this trim be used to compensate for system errors originating outside of the OP-113. The initial offset of the OP-113 is low enough that external trimming is almost never required, but if necessary, the 2 mV trim range may be somewhat excessive. Reducing the trimming potentiometer to a 2 kΩ value will give a more reasonable range of ±400 μV.

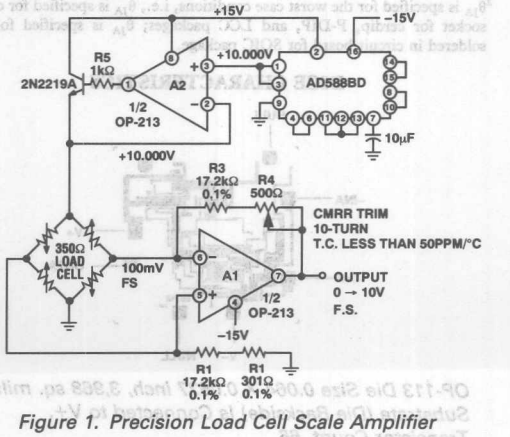


Figure 1. Precision Load Cell Scale Amplifier

APPLICATION CIRCUITS

A High Precision Industrial Load-Cell Scale Amplifier

The OP-113 family makes an excellent amplifier for conditioning a load-cell bridge. Its low noise greatly improves the signal resolution, allowing the load cell to operate with a smaller output range, thus reducing its nonlinearity. Figure 1 shows one half of the OP-113 family used to generate a very stable 10.000 V bridge excitation voltage while the second amplifier provides a differential gain. R4 should be trimmed for maximum common-mode rejection.

A Low Voltage Single Supply, Strain-Gage Amplifier

The true zero swing capability of the OP-113 family allows the amplifier in Figure 2 to amplify the strain-gage bridge accurately even with no signal input while being powered by a single +5 volt supply. A stable 4.000 V bridge voltage is made possible by the rail-to-rail OP-295 amplifier, whose output can swing to within a millivolt of either rail. This high voltage swing greatly increases the bridge output signal without a corresponding increase in bridge input.

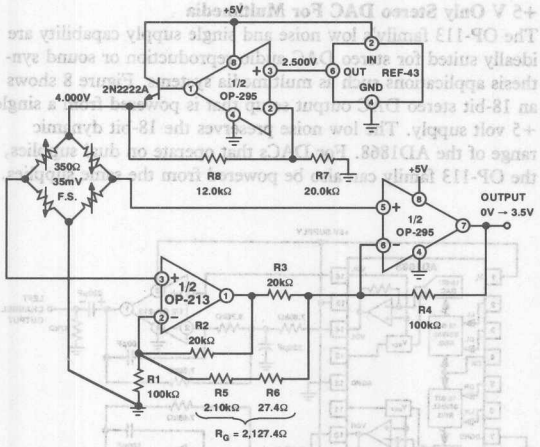


Figure 2. Single Supply Strain-Gage Amplifier

A High Accuracy Linearized RTD Thermometer Amplifier

Zero-suppressing the bridge facilitates simple linearization of the RTD by feeding back a small amount of the output signal to the RTD (Resistor Temperature Device). In Figure 3 the left leg of the bridge is servoed to a virtual ground voltage by amplifier A1, while the right leg of the bridge is also servoed to zero-volt by amplifier A2. This eliminates any error resulting from common-mode voltage change in the amplifier. A three-wire RTD is used to balance the wire resistance on both legs of the bridge, thereby reducing temperature mismatch errors. The 5.000 V bridge excitation is derived from the extremely stable AD588 reference device with 1.5 ppm/°C drift performance.

Linearization of the RTD is done by feeding a fraction of the output voltage back to the RTD in the form of a current. With just the right amount of positive feedback, the amplifier output will be linearly proportional to the temperature of the RTD.

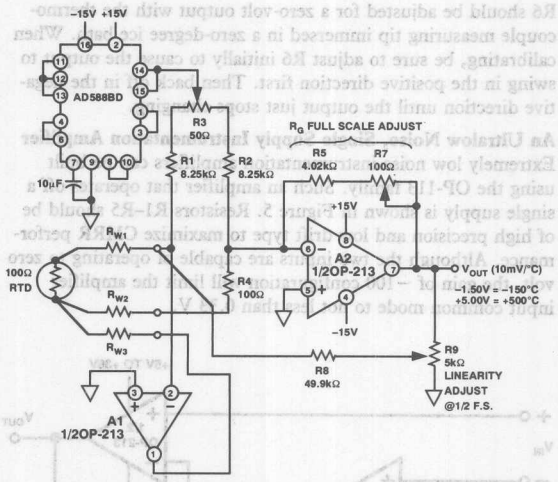


Figure 3. Ultraprecision RTD Amplifier

To calibrate the circuit, first immerse the RTD in a zero-degree ice bath or substitute an exact 100 Ω resistor in place of the RTD. Adjust the ZERO ADJUST potentiometer for a 0.000 V output, then set R9 LINEARITY ADJUST potentiometer to the middle of its adjustment range. Substitute a 280.9 Ω resistor (equivalent to 500°C) in place of the RTD, and adjust the FULL-SCALE ADJUST potentiometer for a full-scale voltage of 5.000 V.

To calibrate out the nonlinearity, substitute a 194.07 Ω resistor (equivalent to 250°C) in place of the RTD, then adjust the LINEARITY ADJUST potentiometer for a 2.500 V output. Check and readjust the full-scale and half-scale as needed.

Once calibrated, the amplifier outputs a 10 mV/°C temperature coefficient with an accuracy better than ±0.5°C over an RTD measurement range of −150°C to +500°C. Indeed the amplifier can be calibrated to a higher temperature range, up to 850°C.

A High Accuracy Thermocouple Amplifier

Figure 4 shows a popular K-type thermocouple amplifier with cold-junction compensation. Operating from a single +12 volt supply, the OP-113 family's low noise allows temperature measurement to better than 0.02°C resolution from 0°C to 1000°C range. The cold-junction error is corrected by using an inexpensive silicon diode as a temperature measuring device. It should be placed as close to the two terminating junctions as physically possible. An aluminum block might serve well as an isothermal system.

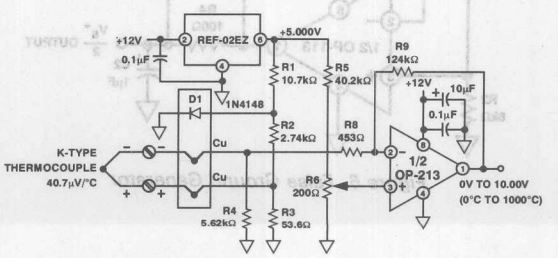


Figure 4. Accurate K-Type Thermocouple Amplifier

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calibrating, be sure to adjust R6 initially to cause the output to swing in the positive direction first. Then back off in the negative direction until the output just stops changing.

An Ultralow Noise, Single Supply Instrumentation Amplifier

Extremely low noise instrumentation amplifiers can be built using the OP-113 family. Such an amplifier that operates off a single supply is shown in Figure 5. Resistors R1–R5 should be of high precision and low drift type to maximize CMRR performance. Although the two inputs are capable of operating to zero volt, the gain of −100 configuration will limit the amplifier input common mode to not less than 0.33 V.

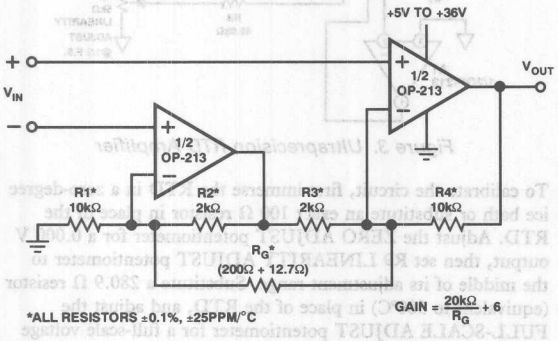

Figure 5. Ultralow Noise, Single Supply Instrumentation Amplifier

Supply Splitter Circuit

The OP-113 family has excellent frequency response characteristic that makes it an ideal pseudo-ground reference generator as shown in Figure 6. The OP-113 family serves as a voltage follower buffer. In addition, it drives a large capacitor that serves as a charge reservoir to minimize transient load changes, as well as a low impedance output device at high frequencies. The circuit easily supplies 25 mA load current with good settling characteristics.

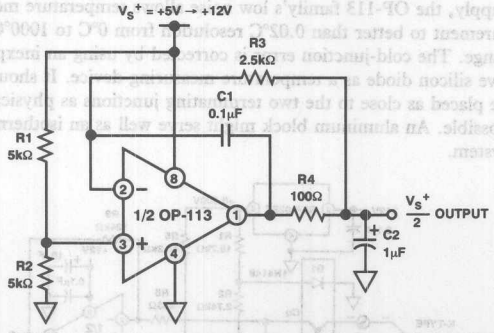

Figure 6. False Ground Generator

capabilities. Figure 7 shows the OP-113 family used as a two-pole active filter that band limits the noise of the 2.500 V reference. Total noise measures 3 µV p-p.

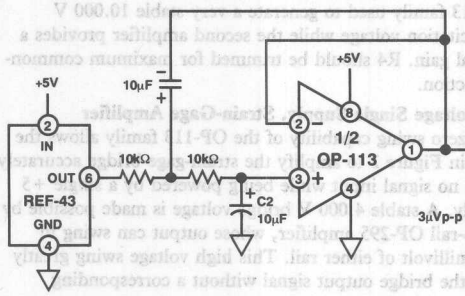

Figure 7. Low Noise Voltage Reference

+5 V Only Stereo DAC For Multimedia

The OP-113 family's low noise and single supply capability are ideally suited for stereo DAC audio reproduction or sound synthesis applications such as multimedia systems. Figure 8 shows an 18-bit stereo DAC output setup that is powered from a single +5 volt supply. The low noise preserves the 18-bit dynamic range of the AD1868. For DACs that operate on dual supplies, the OP-113 family can also be powered from the same supplies.

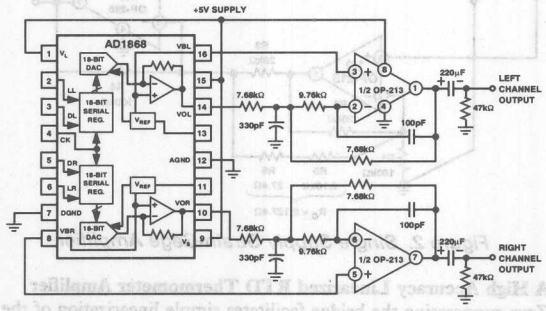

Figure 8. +5 V Only 18-Bit Stereo DAC

Low Voltage Headphone Amplifiers

Figure 9 shows a stereo headphone output amplifier for the AD1849 16-bit SoundPort® Stereo Codec device. The pseudo-reference voltage is derived from the common-mode voltage generated internally by the AD1849, thus providing a convenient bias for the headphone output amplifiers.

SoundPort is a registered trademark of Analog Devices, Inc.

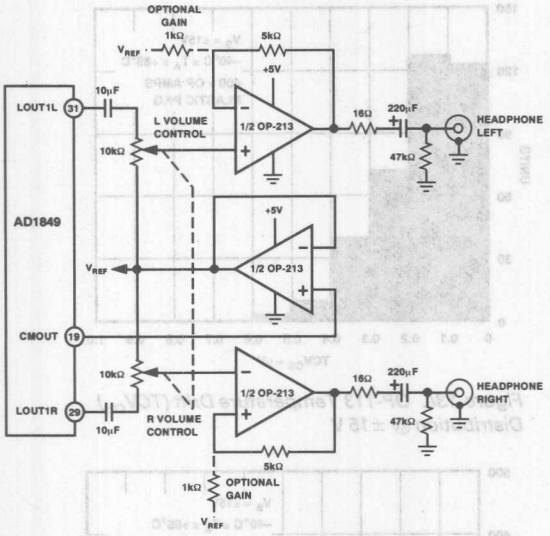

Figure 9. Headphone Output Amplifier for Multimedia Sound Codec

Low Noise Microphone Amplifier for Multimedia

The OP-113 family is ideally suited as a low noise microphone preamp for low voltage audio applications. Figure 10 shows a gain of 100 stereo preamp for the AD1849 16-bit SoundPort Stereo Codec chip. The common-mode output buffer serves as a "phantom power" driver for the microphones.

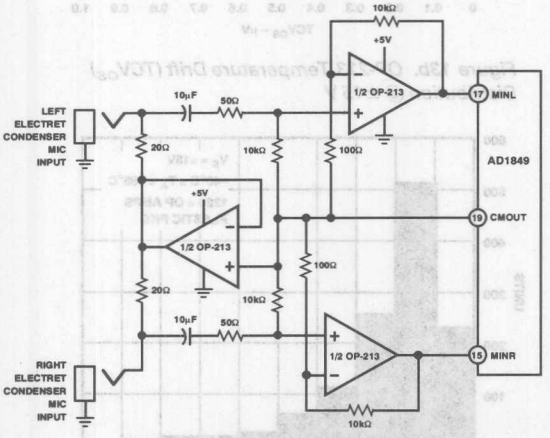

Figure 10. Low Noise Stereo Microphone Amplifier for Multimedia Sound Codec

Precision Voltage Comparator

With its PNP inputs and zero volt common-mode capability, the OP-113 family can make useful voltage comparators. There is only a slight penalty in speed in comparison to IC comparators. However, the significant advantage is its voltage accuracy. For example, V_{OS} can be a few hundred microvolts or less, combined with CMRR and PSRR exceeding 100 dB, while operating on 5 V supply. Standard comparators like the 111/311 family operate on 5 volts, but not with common-mode at ground, nor with offset below 3 mV. Indeed no commercially available single supply comparator has a V_{OS} less than 200 μV.

Figure 11 shows the OP-113 family response to a 10 mV overdrive signal when operating in open loop. The top trace shows the output rising edge has a 15 μs propagation delay, while the bottom trace shows a 7 μs delay on the output falling edge. This ac response is quite acceptable in many applications.

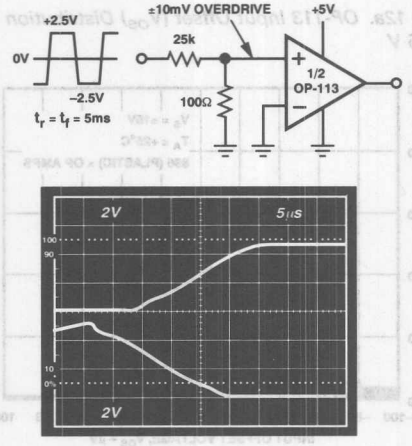

Figure 11. Precision Comparator

The low noise and 250 μV (maximum) offset voltage enhance the overall dc accuracy of this type of comparator. Note that zero crossing detectors and similar ground referred comparisons can be implemented even if the input swings to −0.3 volts below ground.

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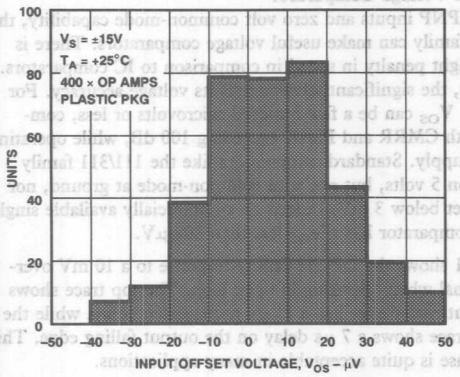

Figure 12a. OP-113 Input Offset (V_{OS}) Distribution @ ±15 V

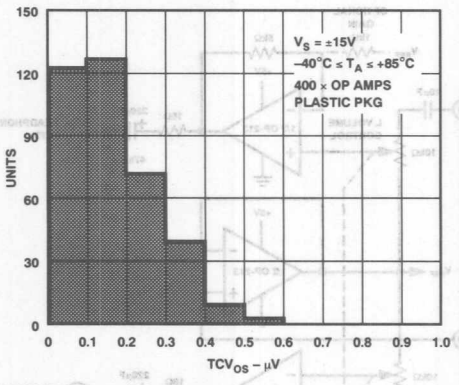

Figure 13a. OP-113 Temperature Drift (TCV_{OS}) Distribution @ ±15 V

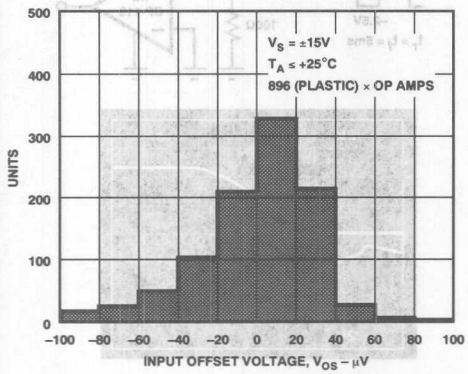

Figure 12b. OP-213 Input Offset (V_{OS}) Distribution @ ±15 V

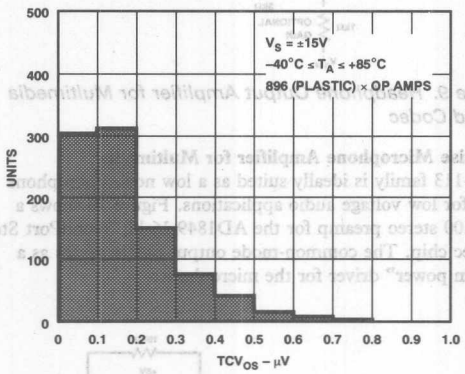

Figure 13b. OP-213 Temperature Drift (TCV_{OS}) Distribution @ ±15 V

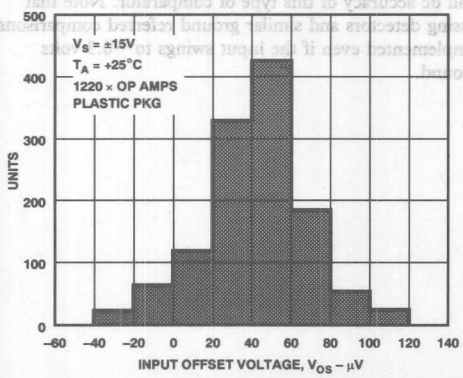

Figure 12c. OP-413 Input Offset (V_{OS}) Distribution @ ±15 V

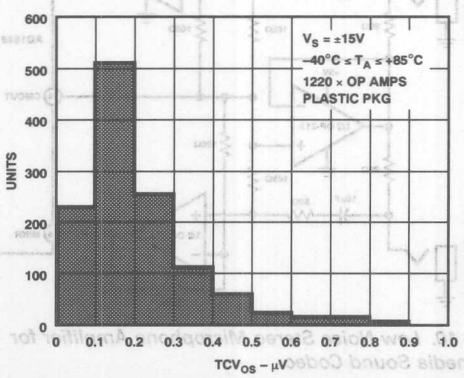

Figure 13c. OP-413 Temperature Drift (TCV_{OS}) Distribution @ ±15 V

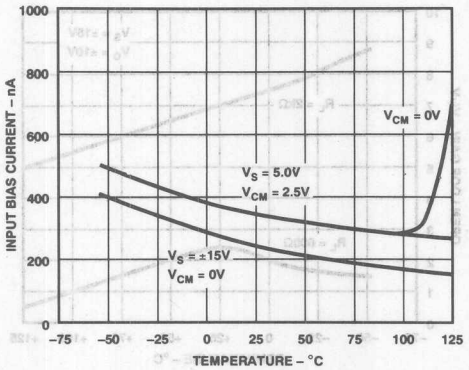

Figure 14. OP-113 Input Bias Current vs. Temperature

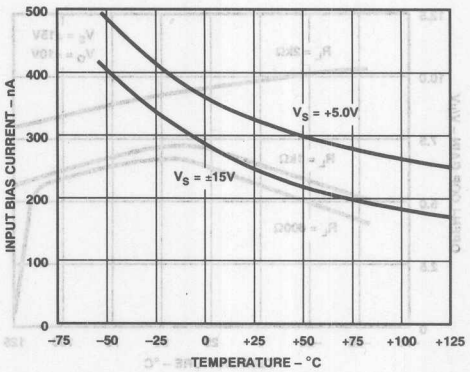

Figure 17. OP-213 Input Bias Current vs. Temperature

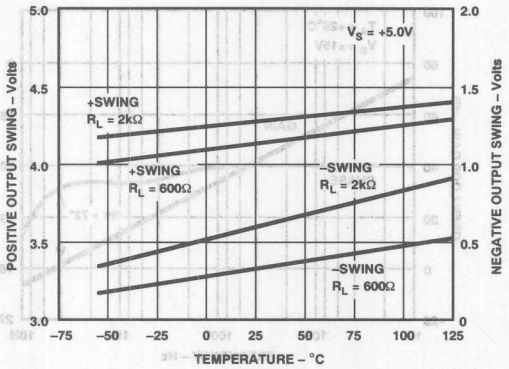

Figure 15. Output Swing vs. Temperature and R_L @ +5 V

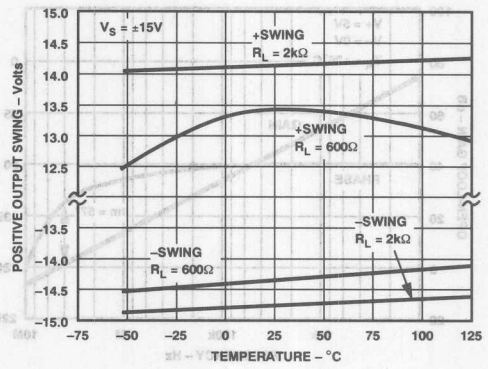

Figure 18. Output Swing vs. Temperature and R_L @ ±15 V

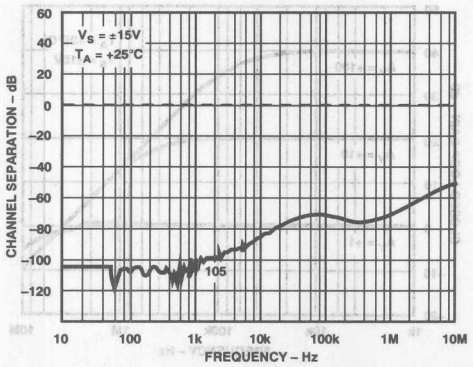

Figure 16. Channel Separation

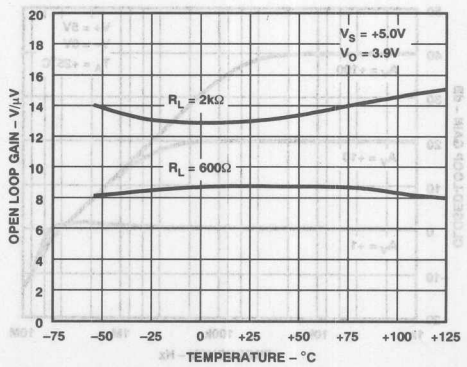

Figure 19. Open-Loop Gain vs. Temperature @ +5 V

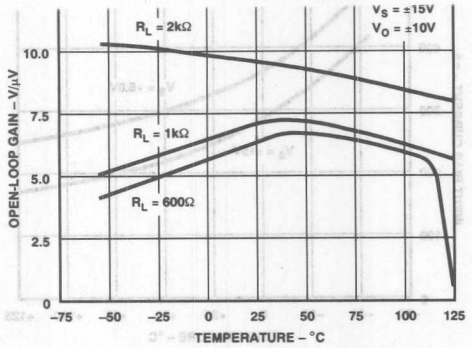

Figure 20. OP-413 Open-Loop Gain vs. Temperature

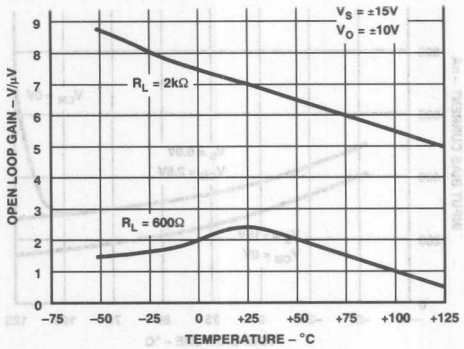

Figure 23. OP-213 Open-Loop Gain vs. Temperature

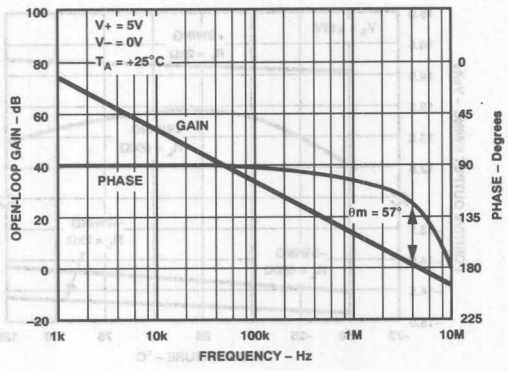

Figure 21. Open-Loop Gain, Phase vs. Frequency @ +5 V

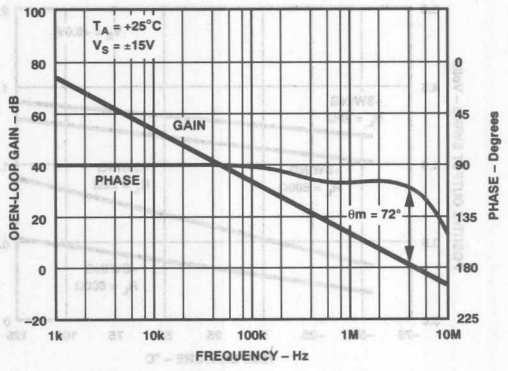

Figure 24. Open-Loop Gain Phase vs. Frequency @ ±15 V

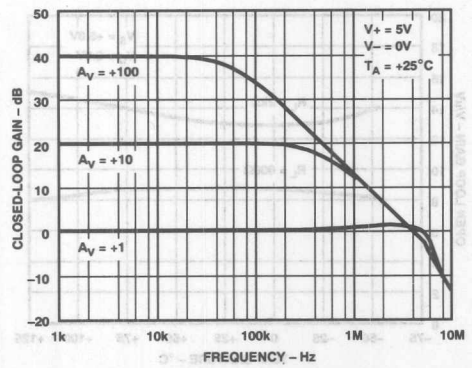

Figure 22. Closed-Loop Gain vs. Frequency @ +5 V

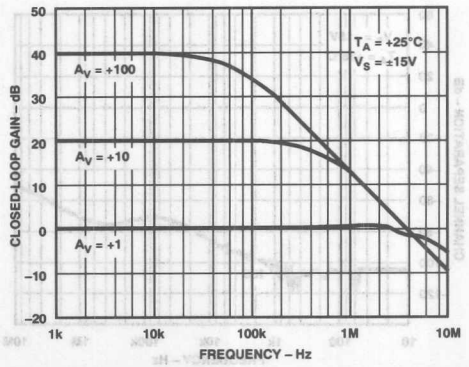

Figure 25. Closed-Loop Gain vs. Frequency @ ±15 V

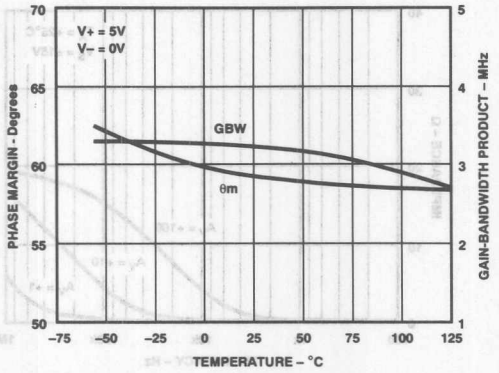

Figure 26. Gain Bandwidth Product and Phase Margin vs. Temperature @ +5 V

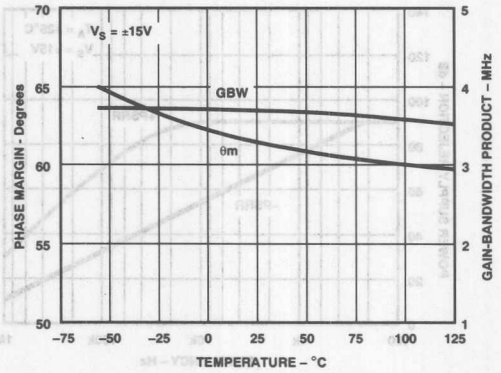

Figure 29. Gain Bandwidth Product and Phase Margin vs. Temperature @ ±15 V

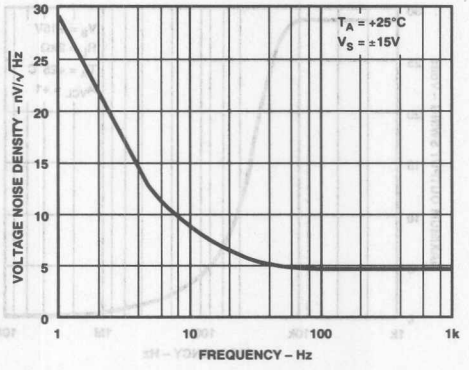

Figure 27. Voltage Noise Density vs. Frequency

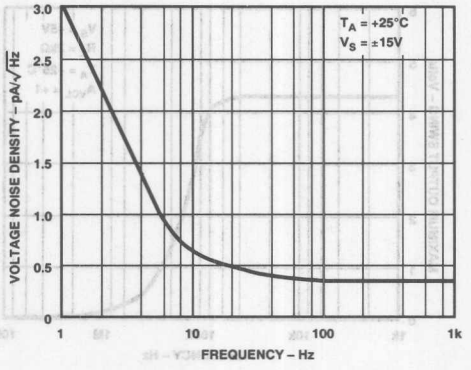

Figure 30. Current Noise Density vs. Frequency

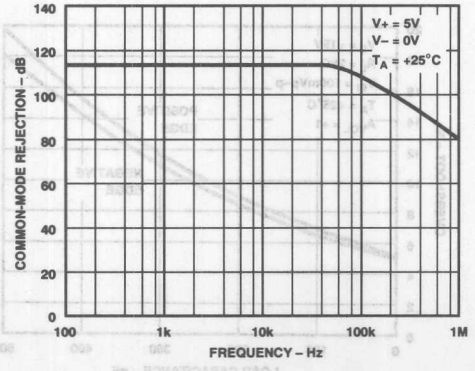

Figure 28. Common-Mode Rejection vs. Frequency @ +5 V

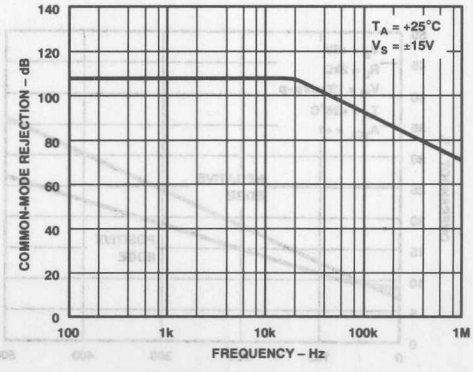

Figure 31. Common-Mode Rejection vs. Frequency @ ±15 V

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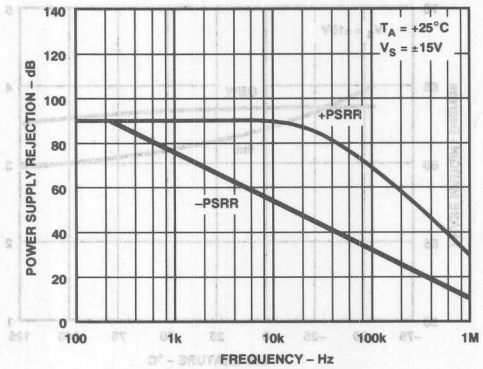


Figure 32. Power Supply Rejection vs. Frequency @ ±15 V

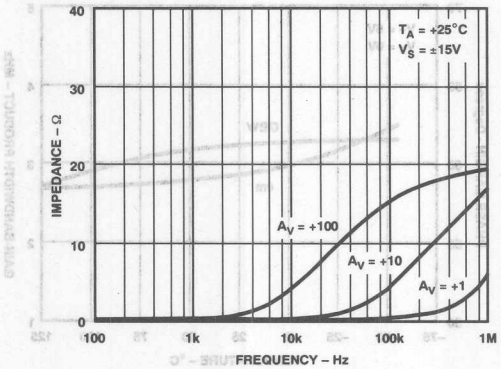


Figure 35. Closed-Loop Output Impedance vs. Frequency @ +15 V

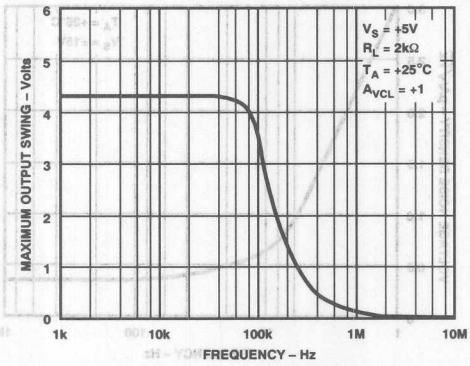


Figure 33. Maximum Output Swing vs. Frequency @ +5 V

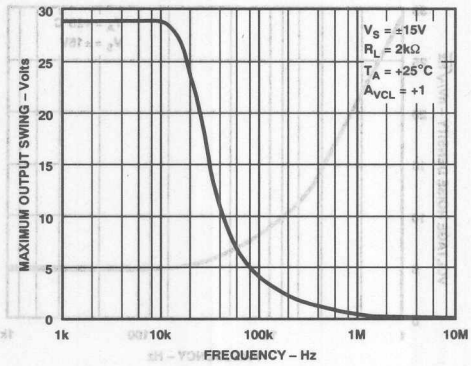


Figure 36. Maximum Output Swing vs. Frequency @ ±15 V

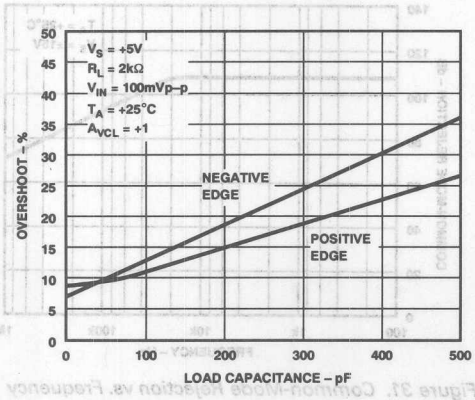


Figure 34. Small Signal Overshoot vs. Load Capacitance @ +5 V

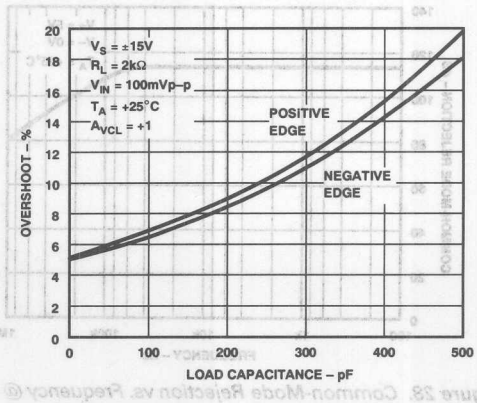


Figure 37. Small Signal Overshoot vs. Load Capacitance @ ±15 V

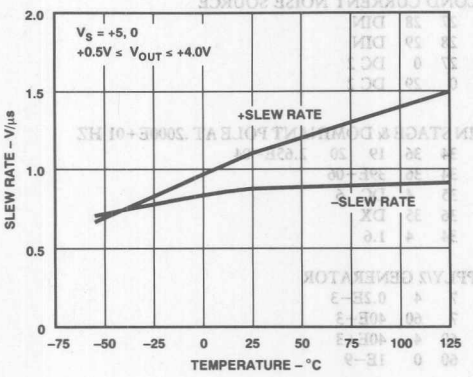


Figure 38. Slew Rate vs. Temperature @ +5 V (0.5 V ≤ V_{OUT} ≤ +4.0 V)

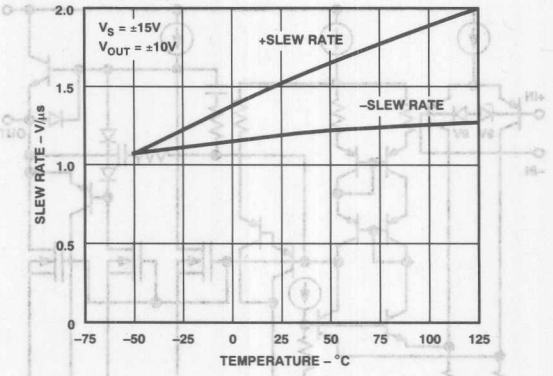


Figure 41. Slew Rate vs. Temperature @ ±15 V (−10 V ≤ V_{OUT} ≤ +10.0 V)

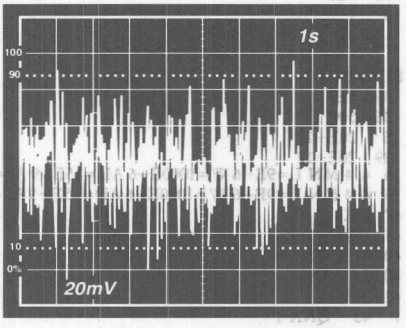


Figure 39. Input Voltage Noise @ ±15 V (20 nV/div)

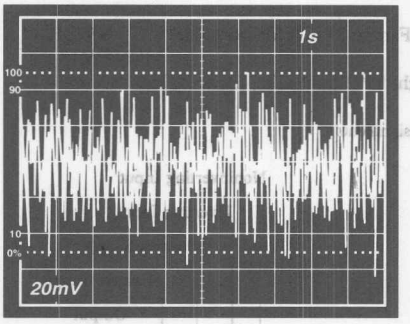


Figure 42. Input Voltage Noise @ +5 V (20 nV/div)

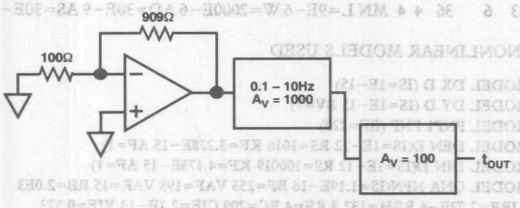


Figure 40. Noise Test Diagram

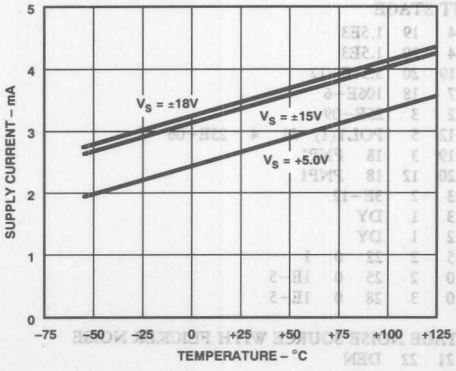


Figure 43. Supply Current vs. Temperature

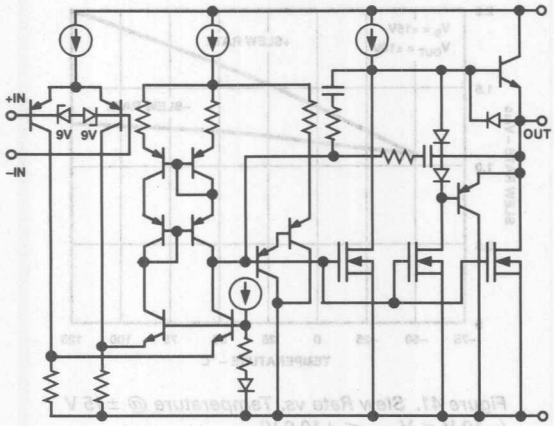


Figure 44. OP-213 Simplified Schematic

```
*OP113 Family SPICE Macro-Model          9/92, Rev. A
*                                        JCN/PMI
*Copyright 1992 by Analog Devices, Inc.
*
*Node Assignments
*
*                          Noninverting Input
*                          Inverting Input
*                          Positive Supply
*                          Negative Supply
*                          Output
*
.SUBCKT OP113 Family    3   2   7   4   6
*
* INPUT STAGE
R3      4    19   1.5E3
R4      4    20   1.5E3
C1      19   20   5.31E-12
I1      7    18   106E-6
IOS     2    3    25E-09
EOS     12   5    POLY(1)  51   4    25E-06   1
Q1      19   3    18   PNP1
Q2      20   12   18   PNP1
CIN     3    2    3E-12
D1      3    1    DY
D2      2    1    DY
EN      5    2    22   0    1
GN1     0    2    25   0    1E-5
GN2     0    3    28   0    1E-5
*
* VOLTAGE NOISE SOURCE WITH FLICKER NOISE
DN1     21   22   DEN
DN2     22   23   DEN
VN1     21   0    DC 2
VN2     0    23   DC 2
*
* CURRENT NOISE SOURCE WITH FLICKER NOISE
DN3     24   25   DIN
DN4     25   26   DIN
VN3     24   0    DC 2
VN4     0    26   DC 2
*
* SECOND CURRENT NOISE SOURCE
DN5     27   28   DIN
DN6     28   29   DIN
VN5     27   0    DC 2
VN6     0    29   DC 2
*
* GAIN STAGE & DOMINANT POLE AT .2000E+01 HZ
G2      34   36   19   20   2.65E-04
R7      34   36   39E+06
V3      35    4   DC   6
D4      36   35   DX
VB2     34    4   1.6
*
* SUPPLY/2 GENERATOR
ISY     7    4    0.2E-3
R10     7    60   40E+3
R11     60   4    40E+3
C3      60   0    1E-9
*
* CMRR STAGE & POLE AT 6 kHZ
ECM     50   4    POLY(2)  3   60   2   60   0   1.6   0   1.6
CCM     50   51   26.5E-12
RCM1    50   51   1E6
RCM2    51   4    1
*
*
OUTPUT STAGE
R12     37   36   1E3
R13     38   36   500
C4      37   6    20E-12
C5      38   39   20E-12
M1      39   36   4  4  MN  L=9E-6  W=1000E-6  AD=15E-9  AS=15E-9
M2      45   36   4  4  MN  L=9E-6  W=1000E-6  AD=15E-9  AS=15E-9
D5      39   47   DX
D6      47   45   DX
Q3      39   40   41   QPA 8
VB      7    40   DC   0.861
R14     7    41   375
Q4      41   7    43   QNA 1
R17     7    43   15
Q5      43   39   6    QNA 20
Q6      46   45   6    QPA 20
R18     46   4    15
Q7      36   46   4    QNA 1
M3      6    36   4  4  MN  L=9E-6  W=2000E-6  AD=30E-9  AS=30E-9
*
* NONLINEAR MODELS USED
*
.MODEL DX D (IS=1E-15)
.MODEL DY D (IS=1E-15 BV=7)
.MODEL PNP1 PNP (BF=220)
.MODEL DEN D(IS=1E-12 RS=1016 KF=3.278E-15 AF=1)
.MODEL DIN D(IS=1E-12 RS=100019 KF=4.173E-15 AF=1)
.MODEL QNA NPN(IS=1.19E-16 BF=253 VAF=193 VAR=15 RB=2.0E3
+ IRB=7.73E-6 RBM=132.8 RE=4 RC=209 CJE=2.1E-13 VJE=0.573
+ MJE=0.364 CJC=1.64E-13 VJC=0.534 MJC=0.5 CJS=1.37E-12
+ VJS=0.59 MJS=0.5 TF=0.43E-9 PTF=30)
.MODEL QPA PNP(IS=5.21E-17 BF=131 VAF=62 VAR=15 RB=1.52E3
+ IRB=1.67E-5 RBM=368.5 RE=6.31 RC=354.4 CJE=1.1E-13
+ VJE=0.745 MJE=0.33 CJC=2.37E-13 VJC=0.762 MJC=0.4
+ CJS=7.11E-13 VJS=0.45 MJS=0.412 TF=1.0E-9 PTF=30)
.MODEL MN NMOS(LEVEL=3 VTO=1.3 RS=0.3 RD=0.3 TOX=8.5E-8
+LD=1.48E-6 WD=1E-6 NSUB=1.53E16 UO=650 DELTA=10 VMAX=2E5
+ XJ=1.75E-6 KAPPA=0.8 ETA=0.066 THETA=0.01 TPG=1 CJ=2.9E-4
+ PB=0.837 MJ=0.407 CJSW=0.5E-9 MJSW=0.33)
*
.ENDS OP113 Family
```

Bipolar/JFET, Audio Operational Amplifier

OP176*

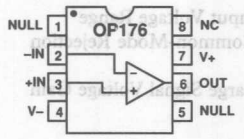
FEATURES
Low Noise: 6 nV/√Hz
High Slew Rate: 25 V/μs
Wide Bandwidth: 10 MHz
Low Supply Current: 2.5 mA
Low Offset Voltage: 1 mV
Unity Gain Stable
SO-8 Package

APPLICATIONS
Line Driver
Active Filters
Fast Amplifiers
Integrators

PIN CONNECTIONS

8-Lead Narrow-Body SO (S Suffix)

8-Lead Epoxy DIP (P Suffix)



GENERAL DESCRIPTION

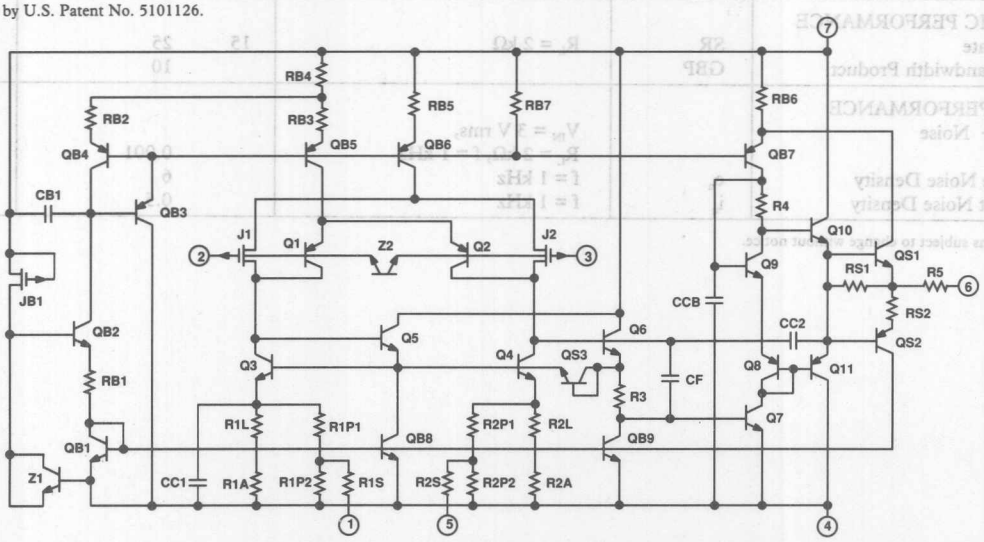
The OP176 is a low noise, high output drive op amp that features the Butler Amplifier front-end. This new front-end design combines both bipolar and JFET transistors to attain amplifiers with the accuracy and low noise performance of bipolar transistors, and the speed and sound quality of JFETs. Total Harmonic Distortion plus Noise equals previous audio amplifiers, but at much lower supply currents.

Improved dc performance is also provided with bias and offset currents greatly reduced over purely bipolar designs. Input offset voltage is guaranteed at 1 mV and is typically less than 200 μV. This allows the OP176 to be used in many dc coupled or summing applications without the need for special selections or the added noise of additional offset adjustment circuitry.

The output is capable of driving 600 Ω loads to 10 V rms while maintaining low distortion. THD + Noise at 3 V rms is a low 0.0006%.

The OP176 is specified over the extended industrial (–40°C to +85°C) temperature range. OP176s are available in both plastic DIP and SO-8 packages. SO-8 packages are available in 2500 piece reels. Many audio amplifiers are not offered in SO-8 surface mount packages for a variety of reasons, however, the OP176 was designed so that it would offer full performance in surface mount packaging.

*Protected by U.S. Patent No. 5101126.



Simplified Schematic

OP176–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				1	mV
Offset Voltage	V_{OS}	–40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 0 V			350	nA
		V_{CM} = 0 V, –40°C ≤ T_A ≤ +85°C			400	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V			±50	nA
		V_{CM} = 0 V, –40°C ≤ T_A ≤ +85°C			±100	nA
Input Voltage Range	V_{CM}		–10.5		+10.5	V
Common-Mode Rejection	CMRR	V_{CM} = ±10.5 V, –40°C ≤ T_A ≤ +85°C	80	106		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	250			V/mV
		R_L = 2 kΩ, –40°C ≤ T_A ≤ +85°C	175			V/mV
		R_L = 600 Ω		200		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ, –40°C ≤ T_A ≤ +85°C	–13.5		+13.5	V
		R_L = 600 Ω, V_S = ±18 V	–14.8		+14.8	V
Output Short Circuit Current	I_{SC}		±25	±50		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	86	108		dB
		–40°C ≤ T_A ≤ +85°C	80			dB
Supply Current	I_{SY}	V_S = ±4.5 V to ±18 V, V_O = 0 V, R_L = ∞, –40°C ≤ T_A ≤ +85°C			2.5	mA
Supply Current	I_{SY}	V_S = ±22 V, V_O = 0 V, R_L = ∞, –40°C ≤ T_A ≤ +85°C			2.75	mA
Supply Voltage Range	V_S		±4.5		±22	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	15	25		V/µs
Gain Bandwidth Product	GBP			10		MHz
AUDIO PERFORMANCE						
THD + Noise		V_{IN} = 3 V rms, R_L = 2 kΩ, f = 1 kHz		0.001		%
Voltage Noise Density	e_n	f = 1 kHz		6		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.5		pA/√Hz

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		1	mV max
Input Bias Current	I_B	V_{CM} = 0 V	350	nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	±50	nA max
Input Voltage Range[1]	V_{CM}		±10.5	V min
Common-Mode Rejection	CMRR	V_{CM} = ±10.5 V	80	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	86	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	250	V/mV min
Output Voltage Range	V_O	R_L = 2 kΩ	13.5	V min
		V_S = ±18.0 V, R_L = 600 Ω	14.8	V min
Supply Current	I_{SY}	V_S = ±22.0 V, V_O = 0 V, R_L = ∞	2.75	mA max
		V_S = ±4.5 V to ±18 V, V_O = 0 V, R_L = ∞	2.5	mA max

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.

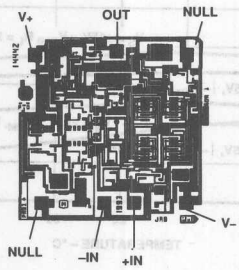
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±22 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±7.5 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
P, S Package . . . . . –65°C to +150°C
Operating Temperature Range
OP176G . . . . . –40°C to +85°C
Junction Temperature Range
P, S Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For input voltages greater than ±7.5 V limit input current to less than 5 mA.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

DICE CHARACTERISTICS



OP176 Die Size 0.069 × 0.067 Inch, 4,623 Sq. Mils. Substrate (Die Backside) Is Connected to V–. Transistor Count, 26.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP176GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP176GS	–40°C to +85°C	8-Pin SOIC	SO-8
OP176GSR	–40°C to +85°C	SO-8 Reel, 2500 Pieces	
OP176GBC	+25°C	DICE	

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP176 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OP176–Typical Characteristics

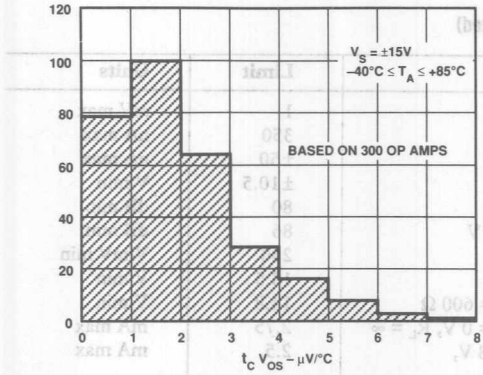


Figure 1. Input Offset Voltage Drift Distribution @ ±15 V

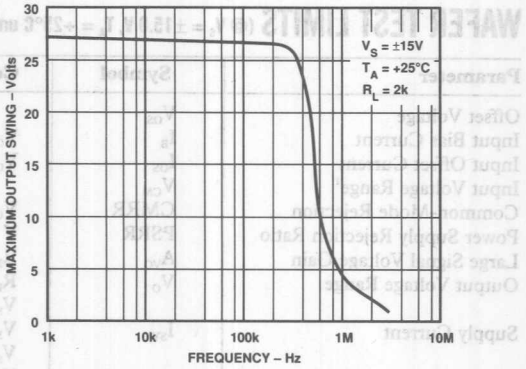


Figure 4. Maximum Output Swing vs. Frequency

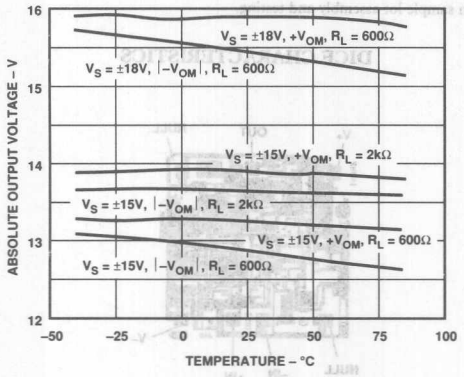


Figure 2. Output Swing vs. Temperature

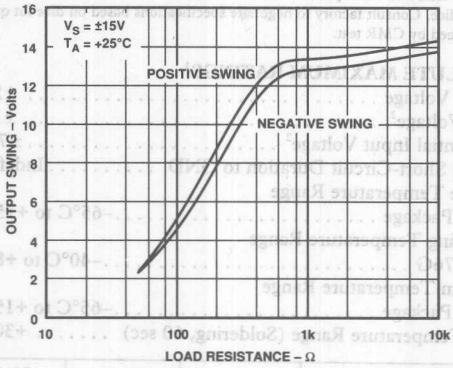


Figure 5. Maximum Output Swing vs. Load Resistance

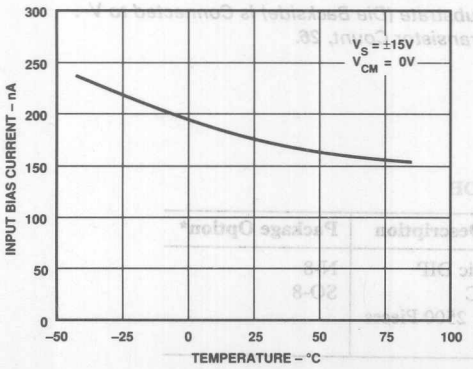


Figure 3. Input Bias Current vs. Temperature

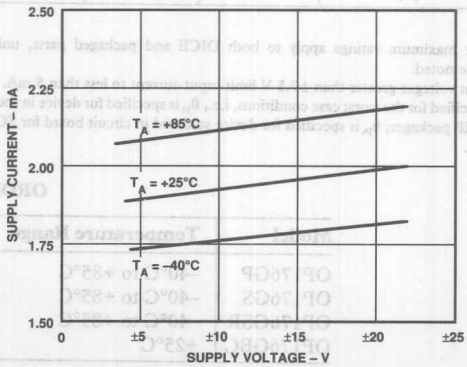


Figure 6. Supply Current per Amplifier vs. Supply Voltage

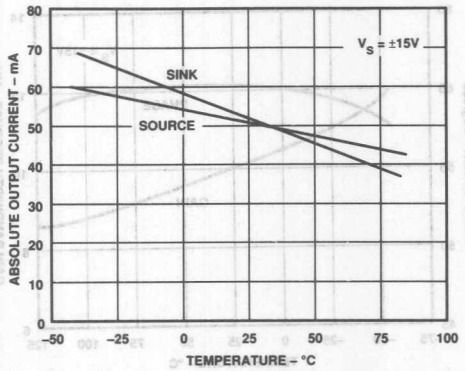


Figure 7. Short Circuit Current vs. Temperature @ ±15 V

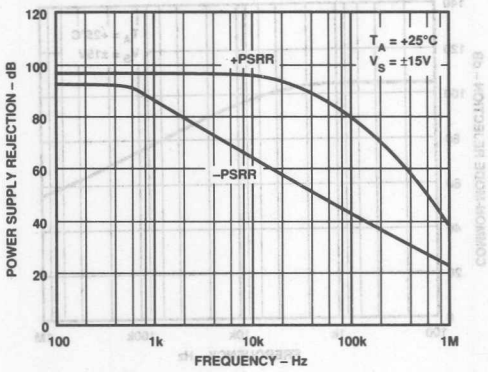


Figure 10. Power Supply Rejection vs. Frequency

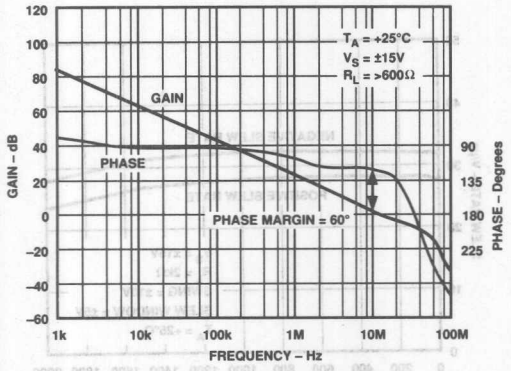


Figure 8. Open-Loop Gain & Phase vs. Frequency

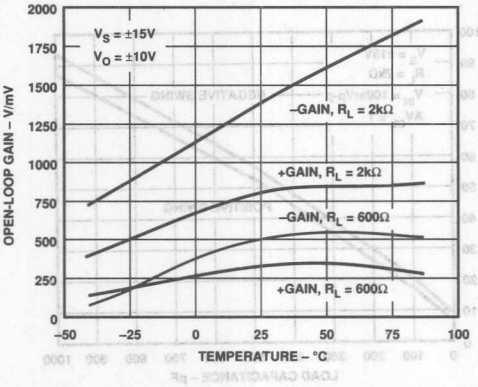


Figure 11. Open-Loop Gain vs. Temperature

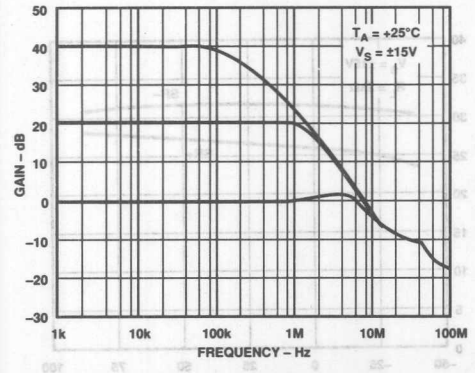


Figure 9. Closed-Loop Gain vs. Frequency

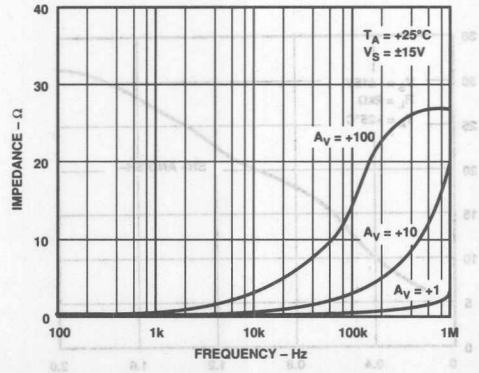


Figure 12. Closed-Loop Output Impedance vs. Frequency

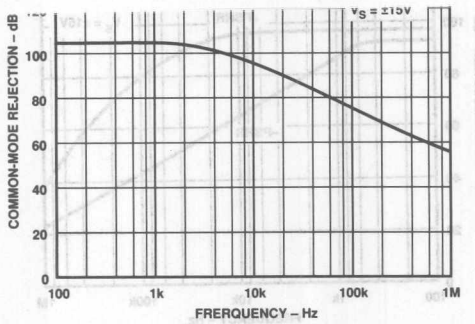


Figure 13. Common-Mode Rejection vs. Frequency

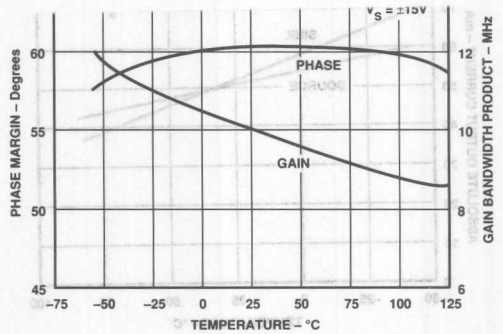


Figure 16. Gain Bandwidth Product & Phase Margin vs. Temperature

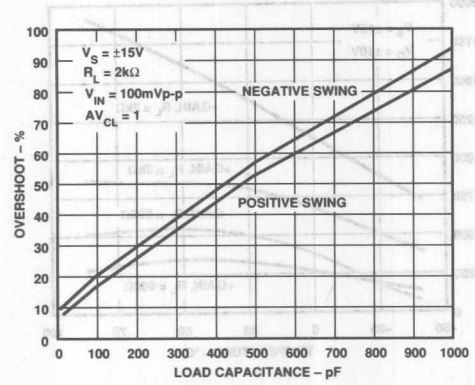


Figure 14. Small Signal Overshoot vs. Load Capacitance

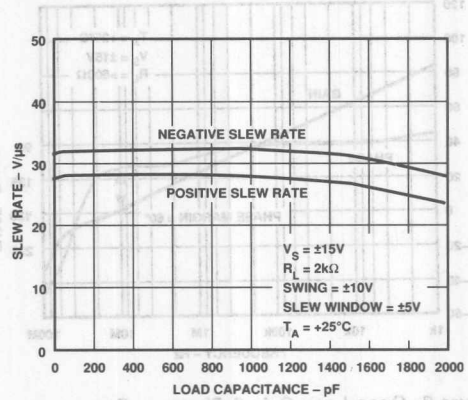


Figure 17. Slew Rate vs. Load Capacitance

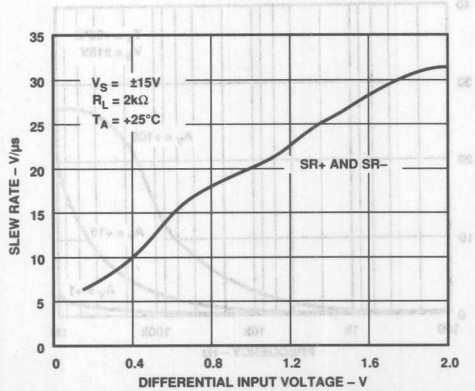


Figure 15. Slew Rate vs. Differential Input Voltage

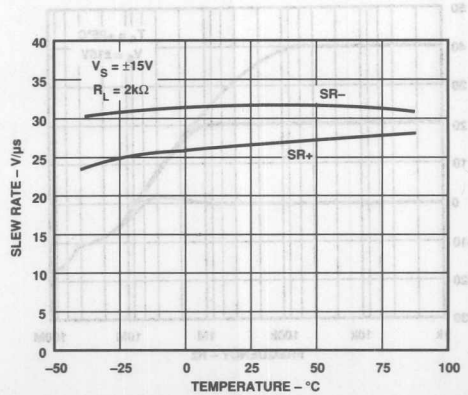


Figure 18. Slew Rate vs. Temperature

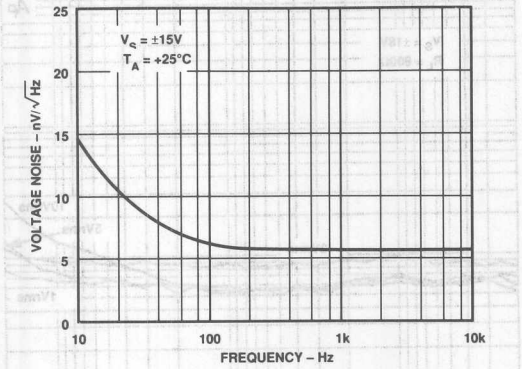


Figure 19. Voltage Noise Density vs. Frequency

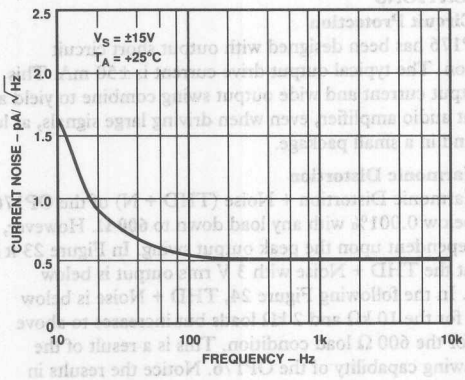


Figure 21. Current Noise Density vs. Frequency

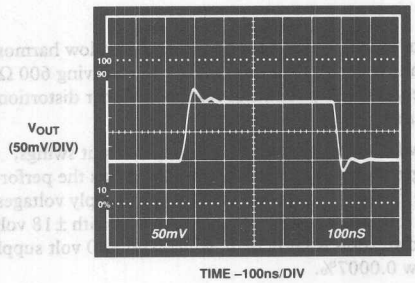


Figure 20. Small Signal Transient Response

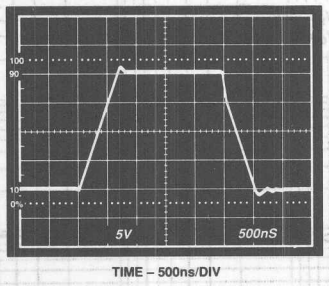


Figure 22. Large Signal Transient Response

9

APPLICATIONS

Short Circuit Protection

The OP176 has been designed with output short circuit protection. The typical output drive current is ±50 mA. This high output current and wide output swing combine to yield an excellent audio amplifier, even when driving large signals, at low power and in a small package.

Total Harmonic Distortion

Total Harmonic Distortion + Noise (THD + N) of the OP176 is well below 0.001% with any load down to 600 Ω. However, this is dependent upon the peak output swing. In Figure 23 it is seen that the THD + Noise with 3 V rms output is below 0.001%. In the following Figure 24, THD + Noise is below 0.001% for the 10 kΩ and 2 kΩ loads but increases to above 0.01% for the 600 Ω load condition. This is a result of the output swing capability of the OP176. Notice the results in Figure 25, showing THD vs. V_{IN} (V rms).

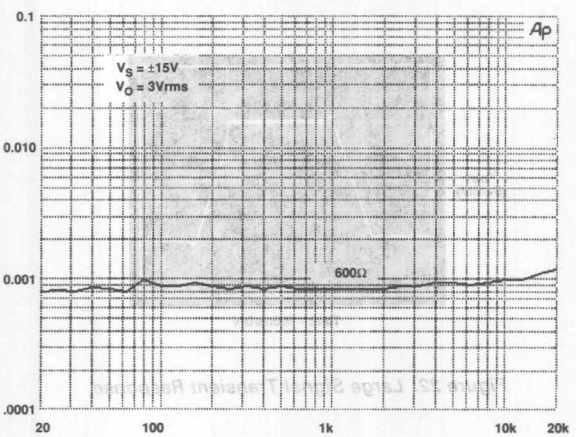


FIGURE 23. THD + Noise vs. Frequency

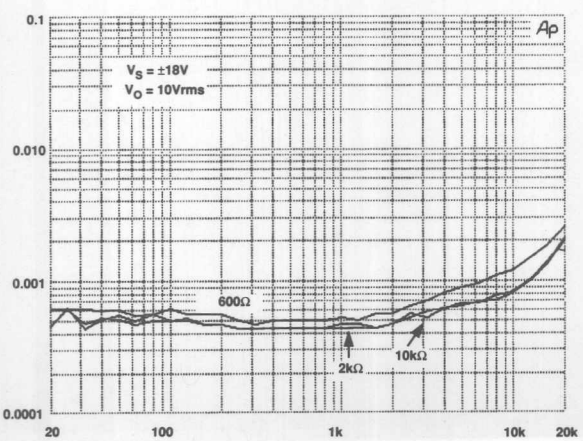


Figure 24. THD + Noise vs. R_{LOAD}

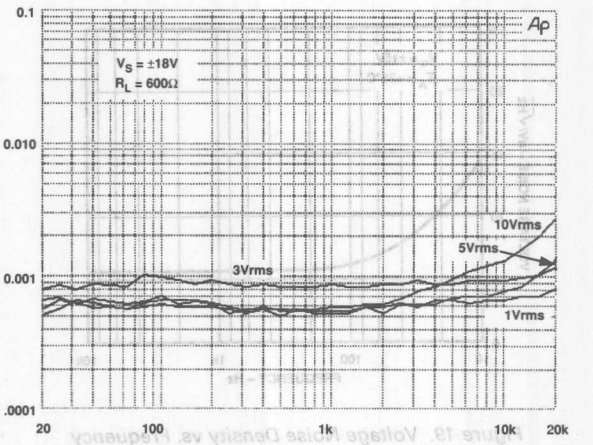


Figure 25. THD + Noise vs. Output Amplitude (V rms)

The output of the OP176 is designed to maintain low harmonic distortion while driving 600 Ω loads. However, driving 600 Ω loads with very high output swings results in higher distortion if clipping occurs.

To attain low harmonic distortion with large output swings, supply voltages may be increased. Figure 26 shows the performance of the OP176 driving 600 Ω loads with supply voltages varying from ±18 volts to ±20 volts. Notice that with ±18 volt supplies the distortion is fairly high, while with ±20 volt supplies it is a very low 0.0007%.

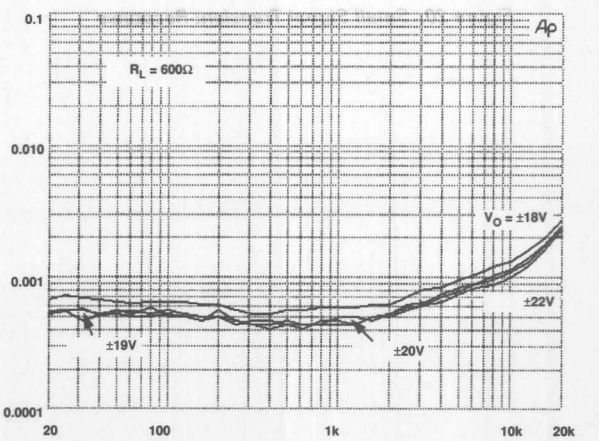


Figure 26. THD + Noise vs. Supply Voltage

Noise

The voltage noise density of the OP176 is below 6 nV/$\sqrt{Hz}$ from 30 Hz. This enables low noise designs to have good performance throughout the full audio range. Figure 27 shows a typical OP176 with a 1/f corner at 6 Hz.

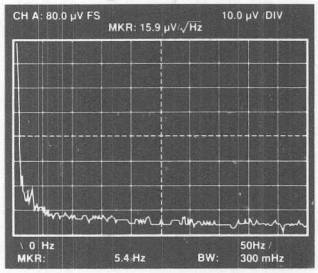


Figure 27. 1/f Noise Corner

Noise Testing

For audio applications the noise density is usually the most important noise parameter. For characterization the OP176 is tested using an Audio Precision, System One. The input signal to the Audio Precision must be amplified enough to measure accurately. For the OP176 the noise is gained by approximately 1020 using the circuit shown in Figure 28. Any readings on the Audio Precision must then be divided by the gain. In implementing this test fixture, good supply bypassing is essential.

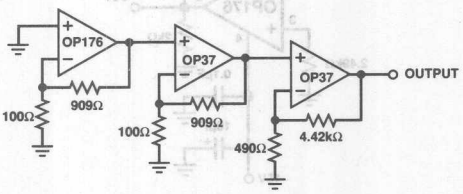


Figure 28. Noise Test

Upgrading "5534" Sockets

The OP176 is a superior amplifier for upgrading existing designs using the industry standard 5534. In most application circuits, the OP176 can directly replace the 5534 without any modifications to the surrounding circuitry. Like the 5534, the OP176 follows the industry standard, single op amp pinout. The difference between these two devices is the location of the null pins and the 5534's compensation capacitor.

The 5534 normally requires a 22 pF capacitor between Pins 5 and 8 for stable operation. Since the OP176 is internally compensated for unity gain operation, it does not require external compensation. Nevertheless, if the 5534 socket already includes a capacitor, the OP176 can be inserted without removing it. Since the OP176's Pin 8 is a "NO CONNECT" pin, there is no internal connection to that pin. Thus, the 22 pF capacitor would be electrically connected through Pin 5 to the internal nulling circuitry. With the other end left open, the capacitor should have no effect on the circuit. However, to avoid altogether any possibility for noise injection, it is recommended that the 22 pF capacitor be cut out of the circuit entirely.

If the original 5534 socket includes offset nulling circuitry, one would find a 10 kΩ to 100 kΩ potentiometer connected between Pins 1 and 8 with said potentiometer's wiper arm connected to V+. In order to upgrade the socket to the OP176, this circuit should be removed before inserting the OP176 for its offset nulling scheme uses Pins 1 and 5. Whereas the wiper arm of the 5534 trimming potentiometer is connected to the positive supply, the OP176's wiper arm is connected to the negative supply. Directly substituting the OP176 into the original socket would inject a large current imbalance into its input stage. In this case, the potentiometer should be removed altogether, or, if nulling is still required, the trimming potentiometer should be rewired to match the nulling circuit as illustrated in Figure 29.

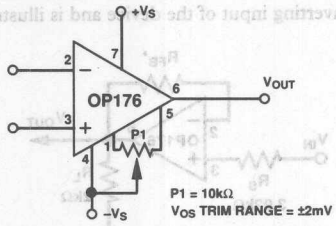


Figure 29. Offset Voltage Nulling Scheme

Input Overcurrent Protection

The maximum input differential voltage that can be applied to the OP176 is determined by a pair of internal Zener diodes connected across its inputs. They limit the maximum differential input voltage to ±7.5 V. This is to prevent emitter-base junction breakdown from occurring in the input stage of the OP176 when very large differential voltages are applied. However, in order to preserve the OP176's low input noise voltage, internal resistances in series with the inputs were not used to limit the current in the clamp diodes. In small signal applications, this is not an issue; however, in applications where large differential voltages can be inadvertently applied to the device, large transient currents can flow through these diodes. Although these diodes have been designed to carry a current of ±5 mA, external resistors as shown in Figure 30 should be used in the event that the OP176's differential voltage were to exceed ±7.5 V.

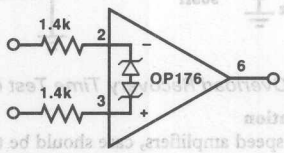


Figure 30. Input Overcurrent Protection

low noise and p-channel JFETs for high speed performance, the output voltage of the OP176 may exhibit phase reversal if either of its inputs exceeds the specified negative common-mode input voltage. This might occur in some applications where a transducer, or a system, fault might apply very large voltages upon the inputs of the OP176. Even though the input voltage range of the OP176 is ±10.5 V, an input voltage of approximately −13.5 V will cause output voltage phase reversal. In inverting amplifier configurations, the OP176's internal 7.5 V clamping diodes will prevent phase reversal; however, they will not prevent this effect from occurring in noninverting applications. For these applications, the fix is a 3.92 kΩ resistor in series with the noninverting input of the device and is illustrated in Figure 31.

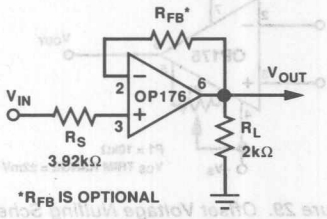


Figure 31. Output Voltage Phase Reversal Fix

Overdrive Recovery

The overdrive recovery time of an operational amplifier is the time required for the output voltage to recover to a rated output level from a saturated condition. This recovery time is important in applications where the amplifier must recover quickly after a large abnormal transient event. The circuit shown in Figure 32 was used to evaluate the OP176's overload recovery time. The OP176 takes approximately 1 µs to recover to V_{OUT} = +10 V and approximately 900 ns to recover to V_{OUT} = −10 V.

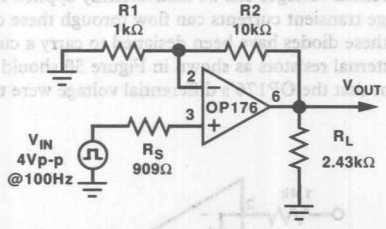


Figure 32. Overload Recovery Time Test Circuit

High Speed Operation

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress, and component placement. Recommended circuit configurations for inverting and noninverting applications are shown in Figure 33 and Figure 34.

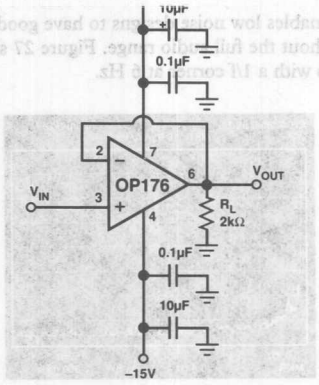


Figure 33. Unity Gain Follower

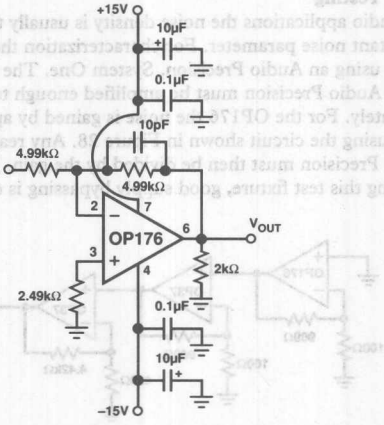


Figure 34. Unity Gain Inverter

In inverting and noninverting applications, the feedback resistance forms a pole with the source resistance and capacitance (R_S and C_S) and the OP176's input capacitance (C_{IN}), as shown in Figure 35. With R_S and R_F in the kΩ range, this pole can create excess phase shift and even oscillation. A small capacitor, C_{FB}, in parallel with R_{FB} eliminates this problem. By setting R_S (C_S + C_{IN}) = R_{FB} C_{FB}, the effect of the feedback pole is completely removed.

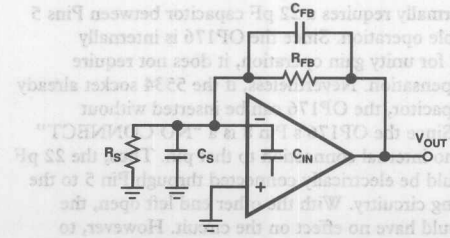


Figure 35. Compensating the Feedback Pole

Attention to Source Impedances Minimizes Distortion
Since the OP176 is a very low distortion amplifier, careful attention should be given to source impedances seen by both inputs. As with many FET-type amplifiers, the p-channel JFETs in the OP176's input stage exhibit a gate-to-source capacitance that varies with the applied input voltage. In an inverting configuration, the inverting input is held at a virtual ground and, as such, does not vary with input voltage. Thus, since the gate-to-source voltage is constant, there is no distortion due to input capacitance modulation. In noninverting applications, however, the gate-to-source voltage is not constant. The resulting capacitance modulation can cause distortion above 1 kHz if the input impedance is > 2 kΩ and unbalanced.

Figure 36 shows some guidelines for maximizing the distortion performance of the OP176 in noninverting applications. The best way to prevent unwanted distortion is to ensure that the parallel combination of the feedback and gain setting resistors (R_F and R_G) is less than 2 kΩ. Keeping the values of these resistors small has the added benefits of reducing the thermal noise of the circuit and dc offset errors. If the parallel combination of R_F and R_G is larger than 2 kΩ, then an additional resistor, R_S, should be used in series with the noninverting

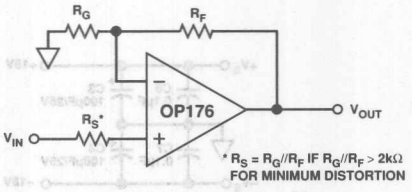


Figure 36. Balanced Input Impedance to Mininize Distortion in Noninverting Amplifier Circuits

input. The value of R_S is determined by the parallel combination of R_F and R_G to maintain the low distortion performance of the OP176. For a more generalized treatment on circuit impedances and their effects on circuit distortion, please review the section on Active Filters at the end of the Applications section.

Driving Capacitive Loads
As with any high speed amplifier, care must be taken when driving capacitive loads. The graph in Figure 14 shows the OP176's overshoot versus capacitive load. The test circuit is a standard noninverting voltage follower; it is this configuration that places the most demand on an amplifier's stability. For capacitive loads greater than 400 pF, overshoot exceeds 40% and is roughly equivalent to a 45° phase margin. If the application requires the OP176 to drive loads larger than 400 pF, then external compensation should be used.

Figure 37 shows a simple circuit which uses an in-the-loop compensation technique that allows the OP176 to drive any capacitive load. The equations in the figure allow optimization of the output resistor, R_X, and the feedback capacitor, C_F, for optimal circuit stability. One important note is that the circuit bandwidth is reduced by the feedback capacitor, C_F, and is given by:

$$BW = \frac{1}{2\pi R_F C_F}$$

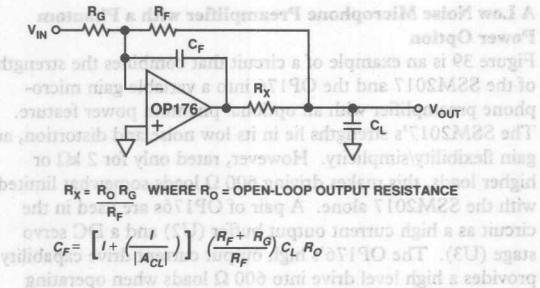


Figure 37. In-the-Loop Compensation Technique for Driving Capacitive Loads

APPLICATIONS USING THE OP176

A High Speed, Low Noise Differential Line Driver
The circuit of Figure 38 is a unique line driver widely used in many applications. With ±18 V supplies, this line driver can deliver a differential signal of 30 V p-p into a 2.5 kΩ load. The high slew rate and wide bandwidth of the OP176 combine to yield a full power bandwidth of 130 kHz while the low noise front end produces a referred-to-input noise voltage spectral density of 15 nV/√Hz. The circuit is capable of driving lower impedance loads as well. For example, with a reduced output level of 5 V rms (14 V p-p), the circuit exhibits a full-power bandwidth of 190 kHz while driving a differential load of 249 Ω! The design is a transformerless, balanced transmission system where output common-mode rejection of noise is of paramount importance. Like the transformer-based design, either output can be shorted to ground for unbalanced line driver applications without changing the circuit gain of 1. Other circuit gains can be set according to the equation in the diagram. This allows the design to be easily set for noninverting, inverting, or differential operation.

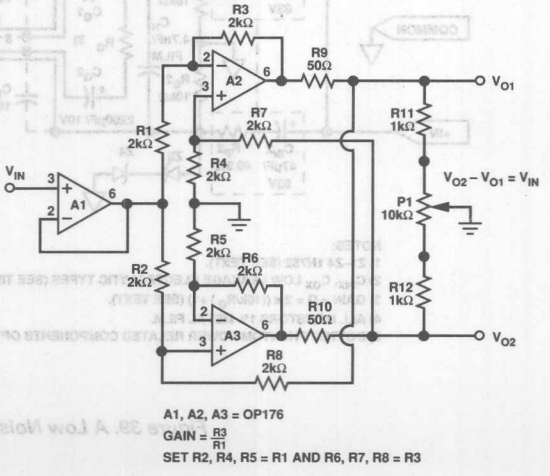


Figure 38. A High Speed, Low Noise Differential Line Driver

A Low Noise Microphone Preamplifier with a Phantom Power Option

Figure 39 is an example of a circuit that combines the strengths of the SSM2017 and the OP176 into a variable gain microphone preamplifier with an optional phantom power feature. The SSM2017's strengths lie in its low noise and distortion, and gain flexibility/simplicity. However, rated only for 2 kΩ or higher loads, this makes driving 600 Ω loads somewhat limited with the SSM2017 alone. A pair of OP176s are used in the circuit as a high current output buffer (U2) and a DC servo stage (U3). The OP176's high output current drive capability provides a high level drive into 600 Ω loads when operating from ±18 V supplies. For a complete treatment of the circuit design details, the interested reader should consult application note AN-242, available from Analog Devices.

This amplifier's performance is quite good over programmed gain ranges of 2 to 2000. For a typical audio load of 600 Ω, THD + N at various gains and an output level of 10 V rms is illustrated in Figure 40. For all but the very highest gain, the THD + N is consistent and well below 0.01%, while the gain of 2000 becomes more limited by noise. The noise performance of the circuit is exceptional with a referred-to-input noise voltage spectral density of 1 nV/√Hz at a circuit gain of 1000.

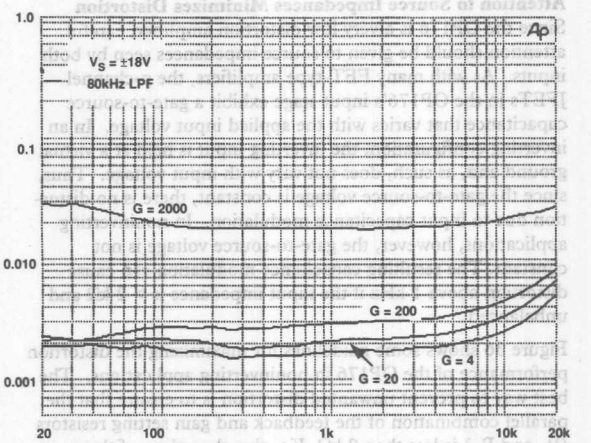


Figure 40. Low Noise Microphone Preamplifier THD + N Performance at Various Gains (V_{OUT} = 10 V rms and R_L = 600 Ω)

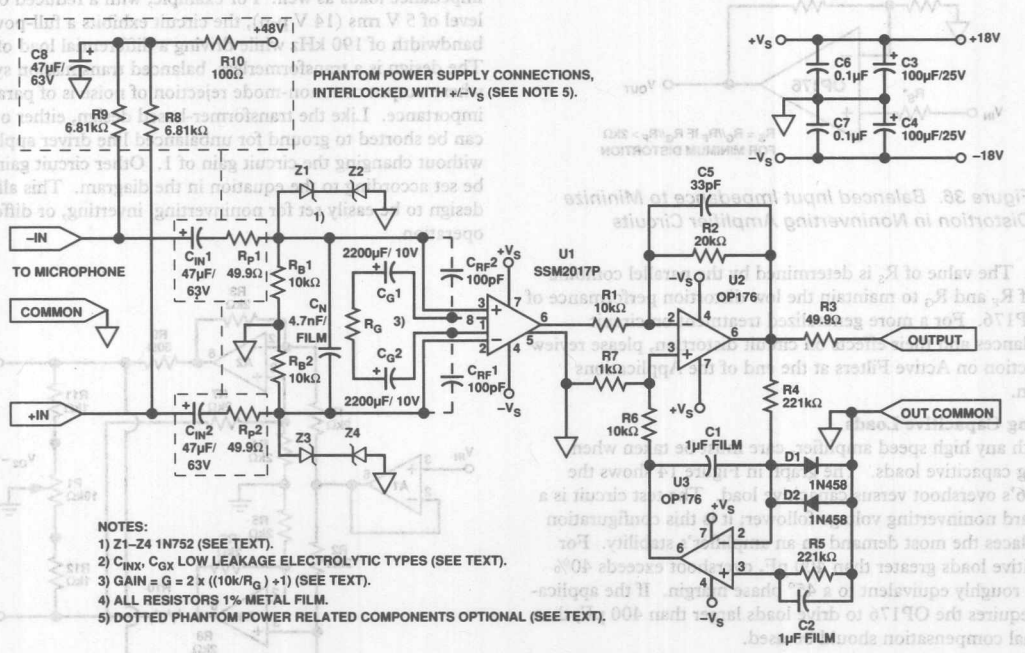


Figure 39. A Low Noise Microphone Preamplifier

A Low Noise, +5 V/+10 V Reference

In many high resolution applications, voltage reference noise can be a major contributor to overall system error. Monolithic voltage references often exhibit too much wide band noise to be used alone in these systems. Only through careful filtering and buffering of these monolithic references can one realize wide-band microvolt noise levels. The circuit illustrated in Figure 41 is an example of a low noise precision reference optimized for both ac and dc performance around the OP176. With a +10 V reference (the AD587), the circuit exhibits a 1 kHz spot output noise spectral density < 10 nV/$\sqrt{\text{Hz}}$. The reference output voltage is selectable between 5 V and 10 V, depending only on the selection of the monolithic reference. The output table illustrated in the figure provides a selection of monolithic references compatible with this circuit.

OUTPUT TABLE

V_{OUT}	U1	TOLERANCE (+/–mV)
10V	AD587	5 TO 10
10V	REF01	30 TO 100
10V	REF10	30 TO 50
10V	AD581	5 TO 30
5V	REF195	2 TO 10
5V	AD586	2.5 TO 20
5V	REF02	15 TO 50
5V	REF05	15 TO 25

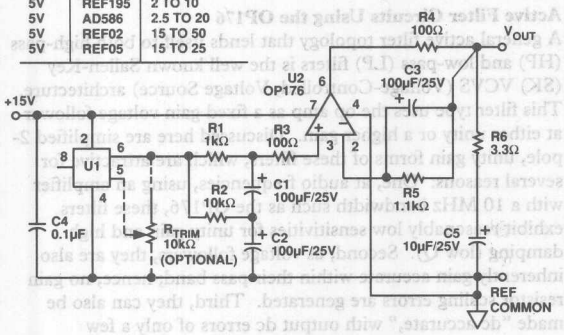


Figure 41. A Low Noise, +5 V/+10 V Reference

In operation, the basic reference voltage is set by U1, either a 5 V or 10 V 3-terminal reference chosen from the table. In this case, the reference used is a 10 V buried Zener reference, but all U1 IC types shown can plug into the pinout and can be optionally trimmed. The stable 10 V from the reference is then applied to the R1-C1-C2 noise filter, which uses electrolytic capacitors for a low corner frequency. When electrolytic capacitors are used for filtering, one must be cognizant of their dc leakage current errors. Here, however, a dc bootstrap of C1 is used, so this capacitor sees only the small R2 dc drop as bias, effectively lowering its leakage current to negligible levels. The resulting low noise, dc-accurate output of the filter is then buffered by a low noise, unity gain op amp using an OP176. With the OP176's low V_{OS} and control of the source resistances, the dc performance of this circuit is quite good and will not compromise voltage reference accuracy and/or drift. Also, the OP176 has a typical current limit of 50 mA, so it can provide higher output currents when compared to a typical IC reference alone.

A Differential ADC Driver

High performance audio sigma-delta ADCs, such as the stereo 16-bit AD1878 and the 18-bit AD1879, present challenging design problems with regards to input interfacing. Because of an internal switched capacitor input circuit, the ADC input structure presents a difficult dynamic load to the drive amplifier with fast transient input currents due to their 3 MHz ADC sampling rate. Also, these ADCs inputs are differential with a rated full-scale range of ±6.3 V, or about 4.4 V rms. Hence, the ADC interface circuit of Figure 42 is designed to accept a balanced input signal to drive the low dynamic impedances seen at the inputs of these ADCs. The circuit uses two OP176

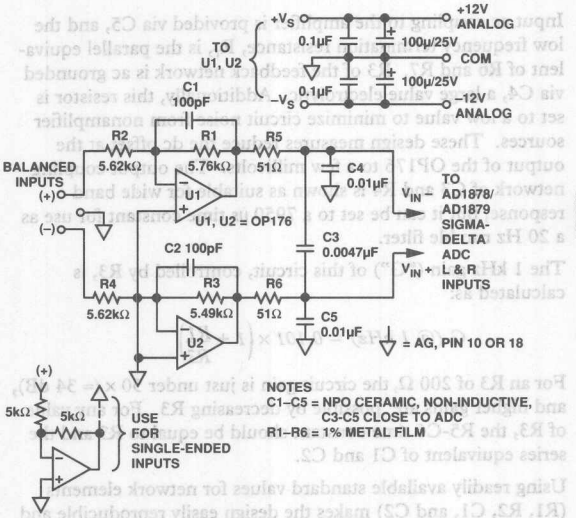


Figure 42. A Balanced Driver Circuit for Sigma-Delta ADCs

amplifiers as inverting low-pass filters for their speed and high output current drive. The outputs of the OP176s then drive the differential ADC inputs through an RC network. This RC network buffers the amplifiers against step changes at the ADC sampling inputs using one differential (C3) and two common-mode connected capacitors (C4 and C5). The 51 Ω series resistors isolate the OP176s from the heavily capacitive loads, while the capacitors absorb the transient currents. Operating on ±12 V supplies, this circuit exhibits a very low THD + N of 0.001% at 5 V rms outputs. For single-ended drive sources, a third op amp unity gain inverter can be added between R2's (+) input terminal and R4. For best results, short-lead, noninductive capacitors are suggested for C3, C4, and C5 (which are placed close to the ADC), and 1% metal-film types for R1 through R6. For surface mount PCBs, these components can be NPO ceramic chip capacitors and thin-film chip resistors.

An RIAA Phono Preamp

Figure 43 illustrates a simple phono preamplifier using RIAA equalization. The OP176 is used here to provide gain and is chosen for its low input voltage noise and high speed performance. The feedback equalization network (R1, R2, C1, and C2) forms a three time constant network, providing reasonably accurate equalization with standard component values. The input components terminate a moving magnet phono cartridge as recommended by the manufacturer, the element values shown being typical. When this ac coupled circuit is built with a low noise bipolar input device such as the OP176, amplifier bias current makes direct cartridge coupling difficult. This circuit uses input and output capacitor coupling to minimize biasing interactions.

Input ac coupling to the amplifier is provided via C5, and the low frequency termination resistance, R_T, is the parallel equivalent of R6 and R7. R3 of the feedback network is ac grounded via C4, a large value electrolytic. Additionally, this resistor is set to a low value to minimize circuit noise from nonamplifier sources. These design measures reduce the dc offset at the output of the OP176 to a few millivolts. The output coupling network of C3 and R4 is shown as suitable for wide band response, but it can be set to a 7950 µs time constant for use as a 20 Hz rumble filter.

The 1 kHz gain ("G") of this circuit, controlled by R3, is calculated as:

$$G\ (@\ 1\ kHz) = 0.101 \times \left(1 + \frac{R1}{R3}\right)$$

For an R3 of 200 Ω, the circuit gain is just under 50 × (≈ 34 dB), and higher gains are possible by decreasing R3. For any value of R3, the R5-C6 time constant should be equal to R3 and the series equivalent of C1 and C2.

Using readily available standard values for network elements (R1, R2, C1, and C2) makes the design easily reproducible and inexpensive. These components are ideally high quality precision types, for low equalization errors and minimum parasitics. One percent metal-film resistors and two percent film capacitors of polystyrene or polypropylene are recommended. Using the suggested values, the frequency response relative to the ideal RIAA characteristic is within ±0.2 dB over 20 Hz–20 kHz. Even tighter response can be achieved by using the alternate values, shown in brackets "[ ]," with the trade-off of a non off-the-shelf part.

As previously mentioned, the OP176 was chosen for three reasons: (1) For optimal circuit noise performance, the amplifier used should exhibit voltage and current noise densities of 5 nV/√Hz and 1 pA/√Hz, respectively. (2) For high gain accuracy, especially at high stage gains, the amplifier should exhibit a gain bandwidth product in excess of 5 MHz. (3) Equally important because of the 100% feedback through the network at high frequencies, the amplifier must be unity gain stable. With the OP176, the circuit exhibits low distortion over the entire range, generally well below 0.01% at outputs levels of 5 V rms using ±18 V supplies. To achieve maximum performance from this high gain, low level circuit, power supplies should be well regulated and noise free, and care should be taken with shielding and conductor layout.

Active Filter Circuits Using the OP176

A general active filter topology that lends itself to both high-pass (HP) and low-pass (LP) filters is the well known Sallen-Key (SK) VCVS (Voltage-Controlled, Voltage Source) architecture. This filter type uses the op amp as a fixed gain voltage follower at either unity or a higher gain. Discussed here are simplified 2-pole, unity gain forms of these filters, which are attractive for several reasons: One, at audio frequencies, using an amplifier with a 10 MHz bandwidth such as the OP176, these filters exhibit reasonably low sensitivities for unity gain and high damping (low Q). Second, as voltage followers, they are also inherently gain accurate within their pass band; hence, no gain resistor scaling errors are generated. Third, they can also be made "dc accurate," with output dc errors of only a few millivolts. The specific filter response in terms of HP, LP and damping is determined by the RC network around the op amp, as shown in Figure 44a.

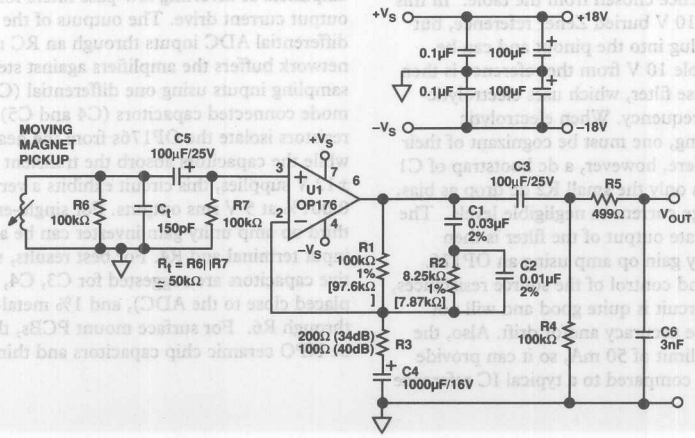


Figure 43. An RIAA Phono Preamplifier Circuit

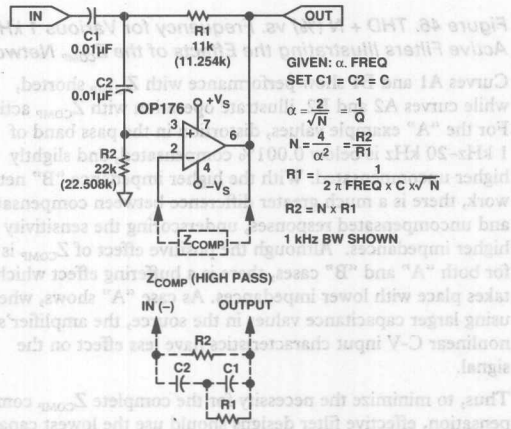
High Pass Sections

Figure 44a illustrates the high-pass form of a 2-pole SK filter using an OP176. For simplicity and practicality, capacitors C1 and C2 are set equal ("C"), and resistors R2 and R1 are adjusted to a ratio, N, which provides the filter damping coefficient, α, as per the design expressions. This high pass design is begun with selection of standard capacitor values for C1 and C2 and a calculation of N. The values for R1 and R2 are then determined from the following expressions:

$$R1 = \frac{1}{2\pi \times FREQ \times C \times \sqrt{N}}$$

and

$$R2 = N \times R1$$



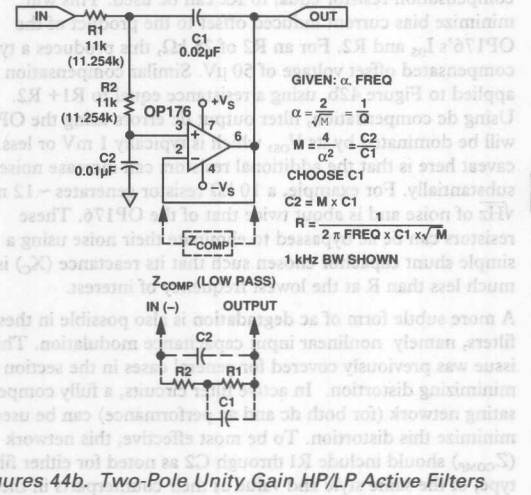
Figures 44a. Two-Pole Unity Gain HP/LP Active Filters

In this examples, circuit α (or 1/Q) is set equal to $\sqrt{2}$, providing a Butterworth (maximally flat) characteristic. The filter corner frequency is normalized to 1 kHz, with resistor values shown in both rounded and (exact) form. Various other 2-pole response shapes are possible with appropriate selection of α, and frequency can be easily scaled, using inversely proportional R or C values for a given α. The 22 V/µs slew rate of the OP176 will support 20 V p-p outputs above 100 kHz with low distortion. The frequency response resulting with this filter is shown as the dotted HP portion of Figure 45.

Low Pass Sections

In the LP SK arrangement of Figure 44b, the R and C elements are interchanged where the resistors are made equal. Here, the ratio of C2/C1 ("M") is used to set the filter α, as noted. Otherwise, this filter is similar to the HP section, and the resulting 1 kHz LP response is shown in Figure 45. The design begins with a choice of a standard capacitor value for C1 and a calculation of M. This then forces a value of "M × C1" for C2. Then, the value for R1 and R2 ("R") is calculated according to the following equation:

$$R = \frac{1}{2\pi \times FREQ \times C1 \times \sqrt{M}}$$



Figures 44b. Two-Pole Unity Gain HP/LP Active Filters

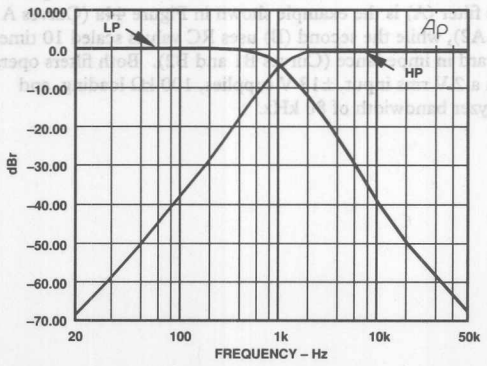


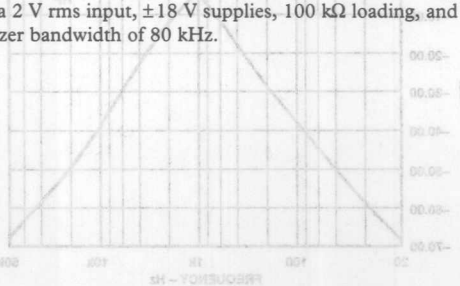
Figure 45. Relative Frequency Response of 2-Pole, 1 kHz Butterworth LP (Left) and HP (Right) Active Filters

or 2% film types preferably, such as polypropylene or polystyrene, or NPO (COG) ceramic for smaller values.

Active Filter Circuit Subtleties

In designing active filter circuits with the OP176, moderately low values (10 kΩ or less) for R1 and R2 can be used to minimize the effects of Johnson noise when critical. The practical tradeoff is, of course, capacitor size and expense. DC errors will result for larger values of resistance, unless compensation for amplifier input bias current is used. To add bias compensation in the HP filter section of Figure 42a, a feedback compensation resistor equal to R2 can be used. This will minimize bias current induced offset to the product of the OP176's I_{OS} and R2. For an R2 of 25 kΩ, this produces a typical compensated offset voltage of 50 µV. Similar compensation is applied to Figure 42b, using a resistance equal to R1+ R2. Using dc compensation, filter output dc errors using the OP176 will be dominated by its V_{OS}, which is typically 1 mV or less. A caveat here is that the additional resistors can increase noise substantially. For example, a 10 kΩ resistor generates ~ 12 nV/$\sqrt{Hz}$ of noise and is about twice that of the OP176. These resistors can be ac bypassed to eliminate their noise using a simple shunt capacitor chosen such that its reactance (X_C) is much less than R at the lowest frequency of interest.

A more subtle form of ac degradation is also possible in these filters, namely nonlinear input capacitance modulation. This issue was previously covered for general cases in the section on minimizing distortion. In active filter circuits, a fully compensating network (for both dc and ac performance) can be used to minimize this distortion. To be most effective, this network (Z_{COMP}) should include R1 through C2 as noted for either filter type, of the same style and value as their counterparts in the forward path. The effects of a Z_{COMP} network on the THD + N performance of two 1 kHz HP filters is illustrated in Figure 46. One filter (A) is the example shown in Figure 44a (Curves A1 and A2), while the second (B) uses RC values scaled 10 times upward in impedance (Curves B1 and B2). Both filters operate with a 2 V rms input, ±18 V supplies, 100 kΩ loading, and analyzer bandwidth of 80 kHz.



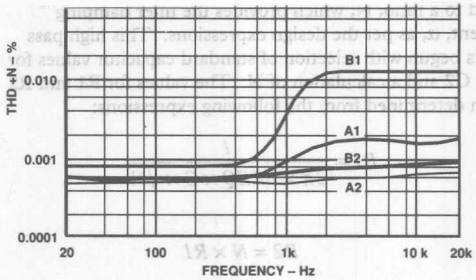


Figure 46. THD + N (%) vs. Frequency for Various 1 kHz HP Active Filters Illustrating the Effects of the Z_{COMP} Network

Curves A1 and B1 show performance with Z_{COMP} shorted, while curves A2 and B2 illustrate operation with Z_{COMP} active. For the "A" example values, distortion in the pass band of 1 kHz–20 kHz is below 0.001% compensated, and slightly higher uncompensated. With the higher impedance "B" network, there is a much greater difference between compensated and uncompensated responses, underscoring the sensitivity to higher impedances. Although the positive effect of Z_{COMP} is seen for both "A" and "B" cases, there is a buffering effect which takes place with lower impedances. As case "A" shows, when using larger capacitance values in the source, the amplifier's nonlinear C-V input characteristics have less effect on the signal.

Thus, to minimize the necessity for the complete Z_{COMP} compensation, effective filter designs should use the lowest capacitive impedances practical, with an 0.01 µF lower value limit as a goal for lowest distortion (while lower values can certainly be used, they may suffer higher distortion without the use of full compensation). Since most designs are likely to use low relative impedances for reasons of low noise and offset, the effects of CM distortion may or may not actually be apparent to a given application.

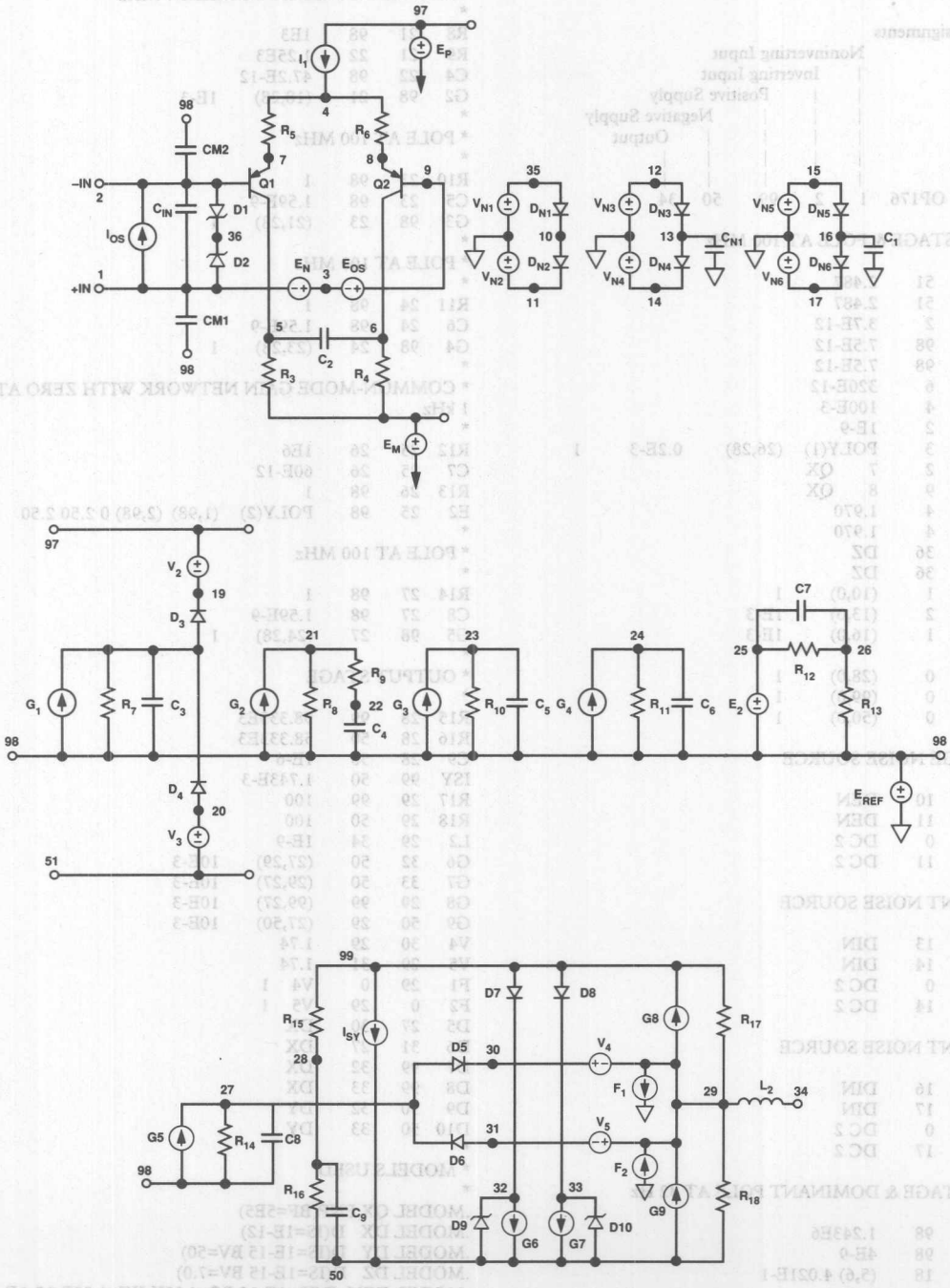


Figure 47. OP176 Spice Model Schematic

OP176 SPICE Model

```
*
* Node Assignments
*                    Noninverting Input
*                    |   Inverting Input
*                    |   |   Positive Supply
*                    |   |   |   Negative Supply
*                    |   |   |   |   Output
*                    |   |   |   |   |
.SUBCKT OP176        1   2   99  50  34
*
* INPUT STAGE & POLE AT 100 MHz
*
R3   5   51   2.487
R4   6   51   2.487
CIN  1   2    3.7E-12
CM1  1   98   7.5E-12
CM2  2   98   7.5E-12
C2   5   6    320E-12
I1   97  4    100E-3
IOS  1   2    1E-9
EOS  9   3    POLY(1)  (26,28)  0.2E-3  1
Q1   5   2    7   QX
Q2   6   9    8   QX
R5   7   4    1.970
R6   8   4    1.970
D1   2   36   DZ
D2   1   36   DZ
EN   3   1    (10,0)   1
GN1  0   2    (13,0)   1E-3
GN2  0   1    (16,0)   1E-3
*
EREF 98  0    (28,0)   1
EP   97  0    (99,0)   1
EM   51  0    (50,0)   1
*
* VOLTAGE NOISE SOURCE
*
DN1  35  10   DEN
DN2  10  11   DEN
VN1  35  0    DC 2
VN2  0   11   DC 2
*
* CURRENT NOISE SOURCE
*
DN3  12  13   DIN
DN4  13  14   DIN
VN3  12  0    DC 2
VN4  0   14   DC 2
*
* CURRENT NOISE SOURCE
*
DN5  15  16   DIN
DN6  16  17   DIN
VN5  15  0    DC 2
VN6  0   17   DC 2
*
* GAIN STAGE & DOMINANT POLE AT 32 Hz
*
R7   18  98   1.243E6
C3   18  98   4E-9
G1   98  18   (5,6) 4.021E-1
V2   97  19   1.35
V3   20  51   1.35
D3   18  19   DX
D4   20 18 DX
*
* POLE/ZERO PAIR AT 1.5 MHz/2.7 MHz
*
R8   21  98   1E3
R9   21  22   1.25E3
C4   22  98   47.2E-12
G2   98  21   (18,28)  1E-3
*
* POLE AT 100 MHz
*
R10  23  98   1
C5   23  98   1.59E-9
G3   98  23   (21,28)  1
*
* POLE AT 100 MHz
*
R11  24  98   1
C6   24  98   1.59E-9
G4   98  24   (23,28)  1
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT
1 kHz
*
R12  25  26   1E6
C7   25  26   60E-12
R13  26  98   1
E2   25  98   POLY(2)  (1,98)  (2,98) 0 2.50 2.50
*
* POLE AT 100 MHz
*
R14  27  98   1
C8   27  98   1.59E-9
G5   98  27   (24,28)  1
*
* OUTPUT STAGE
*
R15  28  99   58.333E3
R16  28  50   58.333E3
C9   28  50   1E-6
ISY  99  50   1.743E-3
R17  29  99   100
R18  29  50   100
L2   29  34   1E-9
G6   32  50   (27,29)  10E-3
G7   33  50   (29,27)  10E-3
G8   29  99   (99,27)  10E-3
G9   50  29   (27,50)  10E-3
V4   30  29   1.74
V5   29  31   1.74
F1   29  0    V4   1
F2   0   29   V5   1
D5   27  30   DX
D6   31  27   DX
D7   99  32   DX
D8   99  33   DX
D9   50  32   DY
D10  50  33   DY
*
* MODELS USED
*
.MODEL QX PNP(BF=5E5)
.MODEL DX  D(IS=1E-12)
.MODEL DY  D(IS=1E-15 BV=50)
.MODEL DZ  D(IS=1E-15 BV=7.0)
.MODEL DEN D(IS=1E-12 RS=4.35K KF=1.95E-15 AF=1)
.MODEL DIN D(IS=1E-12 RS=268 KF=1.08E-15 AF=1)
.ENDS OP176
```

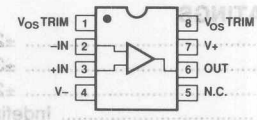
Ultra-Precision Operational Amplifier

OP177

FEATURES

- Ultra-Low Offset Voltage
  - T_A = 25°C ..... 10µV Max
  - –55°C ≤ T_A ≤ 125°C ..... 20µV Max
- Outstanding Offset Voltage Drift ..... 0.1µV/°C Max
- Excellent Open-Loop Gain and Gain Linearity ..... 12V/µV Typ
- CMRR ..... 130dB Min
- PSRR ..... 120dB Min
- Low Supply Current ..... 2.0 mA Max
- Fits Industry Standard Precision Op Amp Sockets (OP07/OP77)

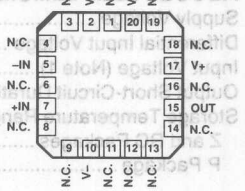
PIN CONNECTIONS



EPOXY MINI-DIP
(P-Suffix)

8-PIN HERMETIC DIP
(Z-Suffix)

8-PIN SO
(S-Suffix)



OP-177BRC/883
LCC
(RC-Suffix)

ORDERING INFORMATION †

PACKAGE				OPERATING
CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-PIN	SO 8-PIN	TEMPERATURE RANGE
OP177AZ*	–	–	–	MIL
OP177BZ*	–	OP177BRC/883	–	MIL
OP177EZ	–	–	–	XIND
OP177FZ	OP177FP	–	–	XIND
OP177GZ	OP177GP	–	OP177GS	XIND

MIL = –55°C to +125°C XIND = –40°C to +85°C

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerDIP, plastic DIP, and TO-can packages.

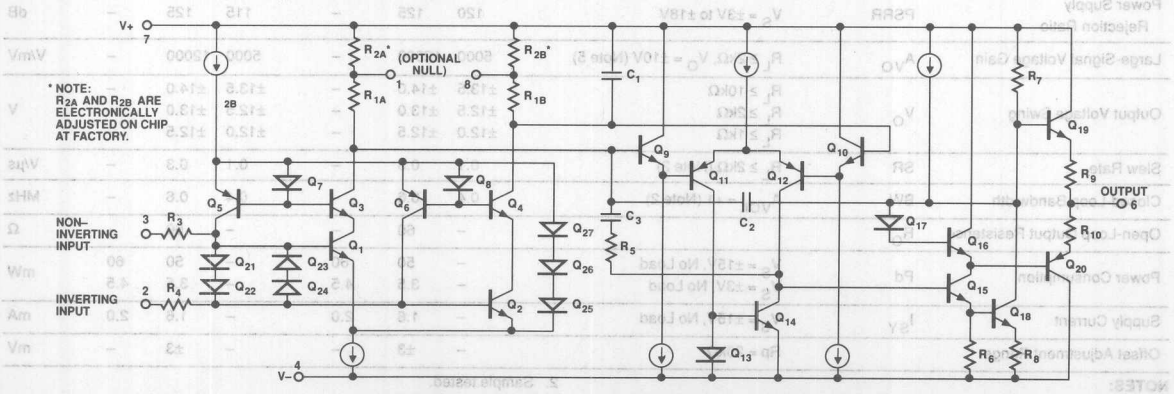
GENERAL DESCRIPTION

The OP-177 features the highest precision performance of any op amp currently available. Offset voltage of the OP-177 is only 10µV MAX at room temperature and 20µV MAX over the full military temperature range of –55°C to +125°C. The ultra-low V_{OS} of the OP-177, combines with its exceptional offset voltage drift (TCV_{OS}) of 0.1µV/°C MAX, to eliminate the need for external V_{OS} adjustment and increases system accuracy over temperature.

The OP-177's open-loop gain of 12V/µV is maintained over the full ±10V output range. CMRR of 130dB MIN, PSRR of 120dB MIN, and maximum supply current of 2mA are just a few examples of the excellent performance of this operational amplifier. The OP-177's combination of outstanding specifications insure accurate performance in high closed-loop gain applications.

This low noise bipolar input op amp is also a cost effective alternative to chopper-stabilized amplifiers. The OP-177 provides chopper-type performance without the usual problems of high noise, low frequency chopper spikes, large physical size, limited common-mode input voltage range, and bulky external storage capacitors.

Continued



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This product is available in 8-pin ceramic and epoxy DIPs, as well as the space saving 8-pin Small-Outline (SO) and the Leadless Chip Carrier (LCC) packages.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
Z and RC Packages ..... –65°C to +150°C
P Package ..... –65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177A MIN	OP-177A TYP	OP-177A MAX	OP-177B MIN	OP-177B TYP	OP-177B MAX	UNITS
Input Offset Voltage	V_{OS}		–	4	10	–	10	25	µV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)	–	0.2	–	–	0.2	–	µV/Mo
Input Offset Current	I_{OS}		–	0.3	1.0	–	0.3	1.5	nA
Input Bias Current	I_B		–0.2	–	1.5	–0.2	–	2.0	nA
Input Noise Voltage	e_n	f_o = 1Hz to 100Hz (Note 2)	–	118	150	–	118	150	nV_{RMS}
Input Noise Current	i_n	f_o = 1Hz to 100Hz (Note 2)	–	3	8	–	3	8	pA_{RMS}
Input Resistance Differential-Mode	R_{IN}	(Note 3)	26	45	–	26	45	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	200	–	–	200	–	GΩ
Input Voltage Range	IVR	(Note 4)	±13	±14	–	±13	±14	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	130	140	–	130	140	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	120	125	–	115	125	–	dB
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V (Note 5)	5000	12000	–	5000	12000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ R_L ≥ 2kΩ R_L ≥ 1kΩ	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	– – –	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	– – –	V
Slew Rate	SR	R_L ≥ 2kΩ (Note 2)	0.1	0.3	–	0.1	0.3	–	V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 2)	0.4	0.6	–	0.4	0.6	–	MHz
Open-Loop Output Resistance	R_O		–	60	–	–	60	–	Ω
Power Consumption	Pd	V_S = ±15V, No Load V_S = ±3V, No Load	– –	50 3.5	60 4.5	– –	50 3.5	60 4.5	mW
Supply Current	I_{SY}	V_S = ±15V, No Load	–	1.6	2.0	–	1.6	2.0	mA
Offset Adjustment Range		Rp = 20kΩ	–	±3	–	–	±3	–	mV

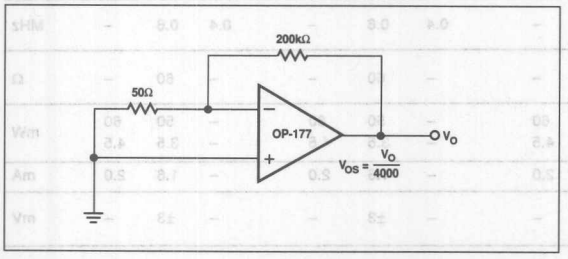
NOTES:
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2.0µV.
2. Sample tested.
3. Guaranteed by design.
4. Guaranteed by CMRR test condition.
5. To insure high open-loop gain throughout the ±10V output range, A_{VO} is tested at $-10V \le V_O \le 0V$, $0V \le V_O \le +10V$, and $-10V \le V_O \le +10V$.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.

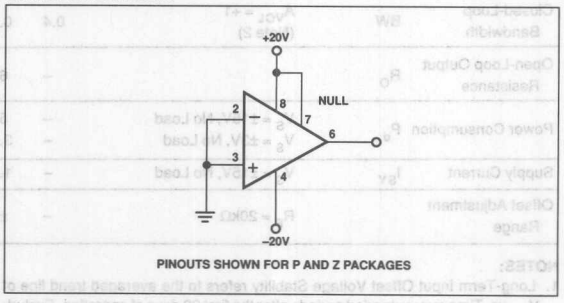
PARAMETER	SYMBOL	CONDITIONS	OP-177A MIN	OP-177A TYP	OP-177A MAX	OP-177B MIN	OP-177B TYP	OP-177B MAX	UNITS
Input Offset Voltage	V_{OS}		–	10	20	–	25	55	µV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	–	0.03	0.1	–	0.1	0.3	µV/°C
Input Offset Current	I_{OS}		–	0.5	1.5	–	0.5	2.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	–	1.5	25	–	1.5	25	pA/°C
Input Bias Current	I_B		–0.2	2.4	4	–0.2	2.4	4	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	–	8	25	–	8	25	pA/°C
Input Voltage Range	IVR	(Note 3)	±13	±13.5	–	±13	±13.5	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	120	140	–	120	140	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	120	125	–	110	120	–	dB
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V (Note 4)	2000	6000	–	2000	6000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13.0	–	±12	±13.0	–	V
Power Consumption	P_d	V_S = ±15V, No Load	–	60	75	–	60	75	mW
Supply Current	I_{SY}	V_S = ±15V, No Load	–	2.0	2.5	–	2.0	2.5	mA

NOTES:
1. TCV_{OS} is 100% tested.
2. Guaranteed by end-point limits.
3. Guaranteed by CMRR test condition.
4. To insure high open-loop gain throughout the ±10V output range, A_{VO} is tested at –10V ≤ V_O ≤ 0V, 0V ≤ V_O ≤ +10V, and –10V ≤ V_O ≤ +10V.

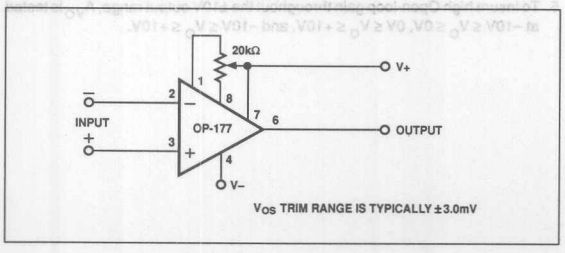
TYPICAL OFFSET VOLTAGE TEST CIRCUIT



BURN-IN CIRCUIT



OPTIONAL OFFSET NULLING CIRCUIT

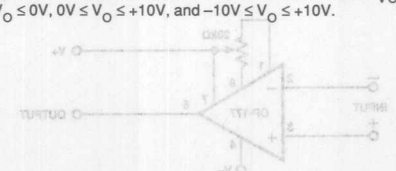


ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177E			OP-177F			OP-177G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		–	4	10	–	10	25	–	20	60	µV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 1)	–	0.2	–	–	0.3	–	–	0.4	–	µV/Mo
Input Offset Current	I_{OS}		–	0.3	1.0	–	0.3	1.5	–	0.3	2.8	nA
Input Bias Current	I_B		–0.2	1.0	1.5	–0.2	1.2	2.0	–0.2	1.2	2.8	nA
Input Noise Voltage	e_n	f_o = 1Hz to 100Hz (Note 2)	–	118	150	–	118	150	–	118	150	nV_{RMS}
Input Noise Current	i_n	f_o = 1Hz to 100Hz (Note 2)	–	3	8	–	3	8	–	3	8	pA_{RMS}
Input Resistance – Differential-Mode	R_{IN}	(Note 3)	26	45	–	26	45	–	18.5	45	–	MΩ
Input Resistance – Common-Mode	R_{INCM}		–	200	–	–	200	–	–	200	–	GΩ
Input Voltage Range	IVR	(Note 4)	±13	±14	–	±13	±14	–	±13	±14	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	130	140	–	130	140	–	115	140	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	120	125	–	115	125	–	110	120	–	dB
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V (Note 5)	5000	12000	–	5000	12000	–	2000	6000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ	±13.5	±14.0	–	±13.5	±14.0	–	±13.5	±14.0	–	V
		R_L ≥ 2kΩ	±12.5	±13.0	–	±12.5	±13.0	–	±12.5	±13.0	–	
		R_L ≥ 1kΩ	±12.0	±12.5	–	±12.0	±12.5	–	±12.0	±12.5	–	
Slew Rate	SR	R_L ≥ 2kΩ (Note 2)	0.1	0.3	–	0.1	0.3	–	0.1	0.3	–	V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 2)	0.4	0.6	–	0.4	0.6	–	0.4	0.6	–	MHz
Open-Loop Output Resistance	R_O		–	60	–	–	60	–	–	60	–	Ω
Power Consumption	P_d	V_S = ±15V, No Load	–	50	60	–	50	60	–	50	60	mW
		V_S = ±3V, No Load	–	3.5	4.5	–	3.5	4.5	–	3.5	4.5	
Supply Current	I_{SY}	V_S = ±15V, No Load	–	1.6	2.0	–	1.6	2.0	–	1.6	2.0	mA
Offset Adjustment Range		R_P = 20kΩ	–	±3	–	–	±3	–	–	±3	–	mV

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2.0µV.
2. Sample tested.
3. Guaranteed by design.
4. Guaranteed by CMRR test condition.
5. To insure high Open-loop gain throughout the ±10V output range, A_{VO} is tested at –10V ≤ V_O ≤ 0V, 0V ≤ V_O ≤ +10V, and –10V ≤ V_O ≤ +10V.



ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ ±85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177E			OP-177F			OP-177G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		–	10	20	–	15	40	–	20	100	µV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	–	0.03	0.1	–	0.1	0.3	–	0.7	1.2	µV/°C
Input Offset Current	I_{OS}		–	0.5	1.5	–	0.5	2.2	–	0.5	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	–	1.5	25	–	1.5	40	–	1.5	85	pA/°C
Input Bias Current	I_B		–0.2	2.4	4.0	–0.2	2.4	4.0	–	2.4	±6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	–	8	25	–	8	40	–	15	60	pA/°C
Input Voltage Range	IVR	(Note 3)	±13.0	±13.5	–	±13.0	±13.5	–	±13.0	±13.5	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	120	140	–	120	140	–	110	140	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	120	125	–	110	120	–	106	115	–	dB
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ V_O = ±10V	2000	6000	–	2000	6000	–	1000	4000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12.0	±13.0	–	±12.0	±13.0	–	±12.0	±13.0	–	V
Power Consumption	P_d	V_S = ±15V, No Load	–	60	75	–	60	75	–	60	75	mW
Supply Current	I_{SY}	V_S = ±15V, No Load	–	2.0	2.5	–	2.0	2.5	–	2.0	2.5	mA

NOTES:
1. OP177E and OP177F: TCV_{OS} is 100% tested.
2. Guaranteed by end-point limits.
3. Guaranteed by CMRR test condition.
4. To insure high open-loop gain throughout the ±10V output range, A_{VO} is tested at –10V ≤ V_O ≤ 0V, 0V ≤ V_O ≤ +10V, and –10V ≤ V_O ≤ +10V.

9

OP183/OP283

FEATURES

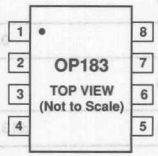
Single-Supply – +3 Volts to +36 Volts
Wide Bandwidth – 5 MHz
Low Offset Voltage – <1 mV
High Slew Rate – 10 V/μs
Low Noise – 10 nV/√Hz
Unity-Gain Stable
Input and Output Range Includes GND
No Phase Reversal

APPLICATIONS

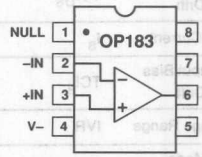
Multimedia
Telecom
ADC Buffers
Wide Band Filters
Microphone Preamplifiers

PIN CONNECTIONS

8-Lead Narrow-Body SO (S Suffix)

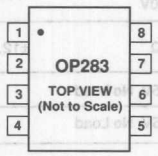


8-Lead Epoxy DIP (P Suffix)

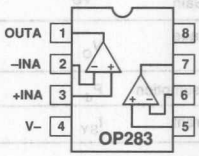


NC = NO CONNECT

8-Lead Narrow-Body SO (S Suffix)



8-Lead Epoxy DIP (P Suffix)



GENERAL DESCRIPTION

The OP183 is a single-supply, 5 MHz bandwidth amplifier with slew rates of 10 V/μs. The OP283 is a dual version. Both can operate from voltages as low as 3 volts and up to 36 volts. This combination of slew rate and bandwidth yields excellent single-supply ac performance making them ideally suited for telecom and multimedia audio applications.

In addition to its ac characteristics, the OP183 family provides good dc performance with guaranteed 1 mV offset. Noise is a respectable 10 nV/√Hz. Supply current is only 1.2 mA per amplifier.

These amplifiers are well suited for single-supply applications that require moderate bandwidths even when used in high gain configurations. This makes them useful in filters and instrumentation. Their output drive capability and very wide full power bandwidth make them a good choice for multimedia headphone drivers or microphone input amplifiers.

The OP183 and OP283 are available in 8-pin plastic DIP and SO-8 surface mount packages. They are specified over the extended industrial (–40°C to +85°C) temperature range.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 2.5 V, V_{OUT} = 2.5 V,		0.025	1.0	mV
		−40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 2.5 V, V_{OUT} = 2.5 V,		350	600	nA
		−40°C ≤ T_A ≤ +85°C		430	750	nA
Input Offset Current	I_{OS}	V_{CM} = 2.5 V, V_{OUT} = 2.5 V,				nA
		−40°C ≤ T_A ≤ +85°C		11	±50	nA
Input Voltage Range			0		+3.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 to 3.5 V				
		−40°C ≤ T_A ≤ +85°C	70	104		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.2 ≤ V_O ≤ 3.8 V	100			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			−1.6		nA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	+4.0	4.22		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND		50	75	mV
Short Circuit Limit	I_{SC}	Source		25		mA
		Sink		30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +4 V to +6 V,				
		−40°C ≤ T_A ≤ +85°C	70	104		dB
Supply Current/Amplifier	I_{SY}	V_O = 2.5 V,				
		−40°C ≤ T_A ≤ +85°C		1.2	1.5	mA
Supply Voltage Range	V_S		+3		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	5	10		V/µs
Full-Power Bandwidth	BWp	1% Distortion		>50		kHz
Settling Time	t_S	To 0.01%		1.5		µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	θo			46		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz, V_{CM} = 2.5 V		10		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

ELECTRICAL CHARACTERISTICS (@ V_S = +3.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 1.5 V, V_{OUT} = 1.5 V,		0.3	1.0	mV
		−40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 1.5 V, V_{OUT} = 1.5 V,		350	600	nA
		−40°C ≤ T_A ≤ +85°C			750	nA
Input Offset Current	I_{OS}	V_{CM} = 1.5 V, V_{OUT} = 1.5 V,				nA
		−40°C ≤ T_A ≤ +85°C		11	±50	nA
Input Voltage Range			0		+1.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 1.5 V,				
		−40°C ≤ T_A ≤ +85°C	70	103		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.2 ≤ V_O ≤ 1.8 V	100	260		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	+2.0	2.25		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND		90	125	mV
Short Circuit Limit	I_{SC}	Source		25		mA
		Sink		30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.5 V to +3.5 V,				
		−40°C ≤ T_A ≤ +85°C	60	113		dB
Supply Current/Amplifier	I_{SY}	−40°C ≤ T_A ≤ +85°C, V_O = 1.5 V		1.2	1.5	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP			5		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz, V_{CM} = 1.5 V		10		nV/√Hz

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ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.01	1.0	mV
		–40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B			300	600	nA
		–40°C ≤ T_A ≤ +85°C		400	750	nA
Input Offset Current	I_{OS}	–40 ≤ T_A ≤ +85°C		11	±50	nA
Input Voltage Range			–15		+13.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –15 V to +13.5 V, –40°C ≤ T_A ≤ +85°C	70	86		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	100	1000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			–1.6		nA/°C
Long Term Offset Voltage	V_{OS}	Note 1			1.5	mV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND, –40°C ≤ T_A ≤ +85°C	+13.9	14.1		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND, –40°C ≤ T_A ≤ +85°C		–14.05	–13.9	V
Short-Circuit Limit	I_{SC}	Source		30		mA
		Sink		50		mA
Open -Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		15		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V, –40°C ≤ T_A ≤ +85°C	70	25		dB
Supply Current/Amplifier	I_{SY}	V_S = ±18 V, V_O = 0 V, –40°C ≤ T_A ≤ +85°C		1.2	1.75	mA
Supply Voltage Range	V_S		+3		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	10	15		V/µs
Full-Power Bandwidth	BW_p	1% Distortion		50		kHz
Settling Time	t_S	To 0.01%		1.5		µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	Øo			56		degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		10		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

NOTES
[1]Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125 °C, with an LTPD of 1.3.
Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = +5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}	V_S = ±15 V, V_O = 0 V	1.0	mV max
Input Bias Current	I_B	V_{CM} = 2.5 V	±600	nA max
Input Offset Current	I_{OS}	V_{CM} = 2.5 V	±50	nA max
Common-Mode Rejection	CMRR	V_{CM} = 0 V to 3.5 V	70	dB min
Power Supply Rejection Ratio	PSRR	V = ±2.5 V to ±18 V	70	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.2 ≤ V_O ≤ 3.8 V	100	V/mV min
Output Voltage High	V_{OH}	R_L = 2 kΩ	4.0	V min
Output Voltage Low	V_{OL}	R_L = 2 kΩ	75	mV max
Supply Current/Amplifier	I_{SY}	V_S = ±15 V, V_O = 0 V, R_L = ∞	1.5	mA max

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Input Voltage ..... ±18 V
Differential Input Voltage[2] ..... ±7 V
Output Short-Circuit Duration to GND ..... Indefinite
Storage Temperature Range
P, S Package ..... –65°C to +150°C
Operating Temperature Range
OP183/OP283G ..... –40°C to +85°C
Junction Temperature Range
P, S Package ..... –65°C to +150°C
Lead Temperature Range (Soldering 60 Sec) ..... +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

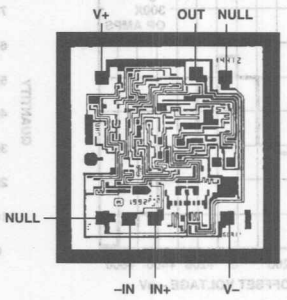
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±7 V, the absolute maximum input voltage is equal to the supply voltage. Maximum input current should not exceed 2 mA.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC packages.

ORDERING GUIDE

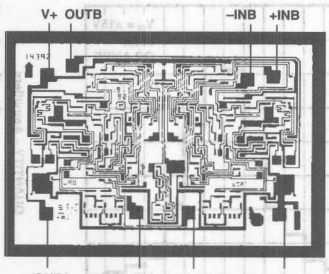
Model	Temperature Range	Package Description	Package Option*
OP183GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP183GS	–40°C to +85°C	8-Pin SOIC	SO-8
OP183GBC	+25°C	DICE	
OP283GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP283GS	–40°C to +85°C	8-Pin SOIC	SO-8
OP283GBC	+25°C	DICE	

*For outline information see Package Information section.

DICE CHARACTERISTICS



OP183 Die Size 0.058 X 0.063 Inch, 3,717 Sq. Mils Substrate (Die Backside) Is Connected to V–. Transistor Count, 30.



OP283 Die Size 0.063 X 0.092 Inch, 5,796 Sq. Mils Substrate (Die Backside) Is Connected to V–. Transistor Count, 55.

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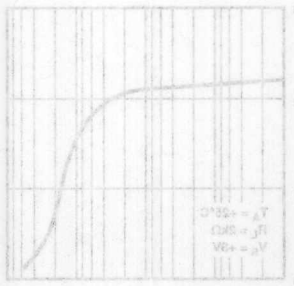
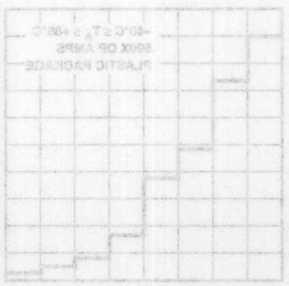
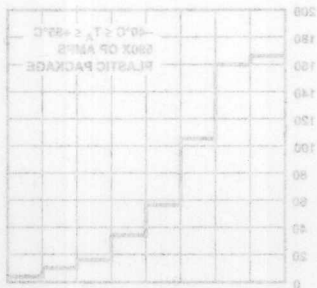






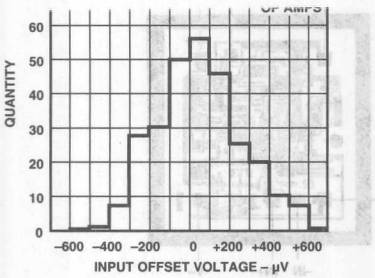


Figure 1. OP183 Input Offset Voltage Distribution @ +5 V

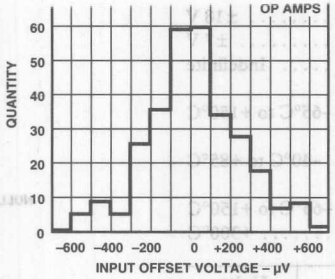


Figure 2. OP183 Input Offset Voltage Distribution @ ±15 V

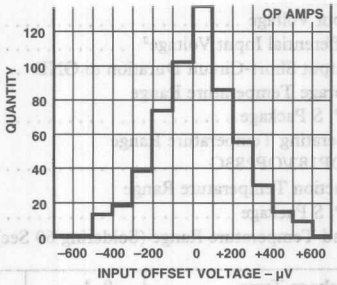


Figure 3. OP283 Input Offset Voltage Distribution @ +5 V

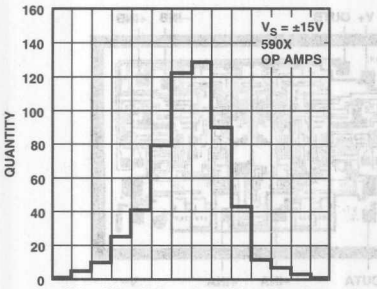


Figure 4. OP283 Input Offset Voltage Distribution @ ±15 V

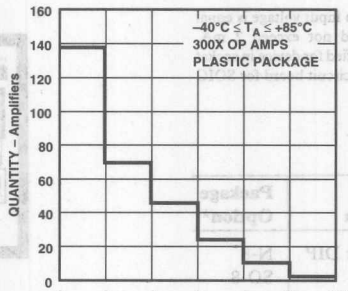


Figure 5. OP183 Input Offset Voltage Drift (TCV_{OS}) Distribution @ +5 V

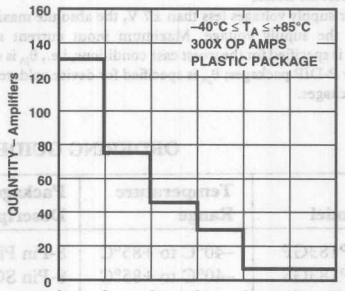


Figure 6. OP183 Input Offset Voltage Drift (TCV_{OS}) Distribution @ ±15 V

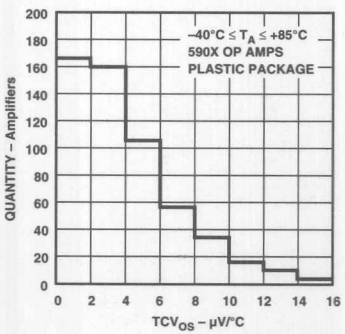


Figure 7. OP283 Input Offset Voltage Drift (TCV_{OS}) Distribution @ +5 V

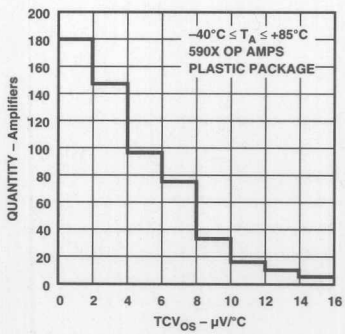


Figure 8. OP283 Input Offset Voltage Drift (TCV_{OS}) Distribution @ ±15 V

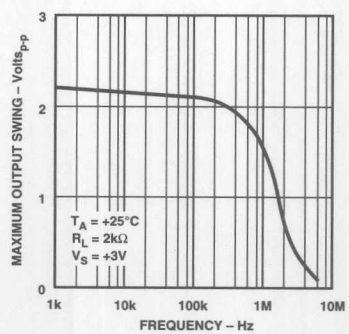


Figure 9. OP183/OP283 Maximum Output Swing vs. Frequency @ +3 V

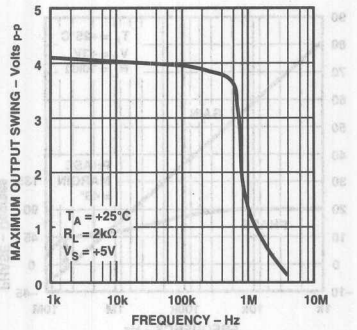


Figure 10. OP183/OP283 Maximum Output Swing vs. Frequency @ +5 V

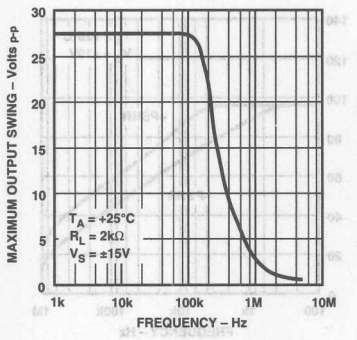


Figure 11. OP183/OP283 Maximum Output Swing vs. Frequency @ ±15 V

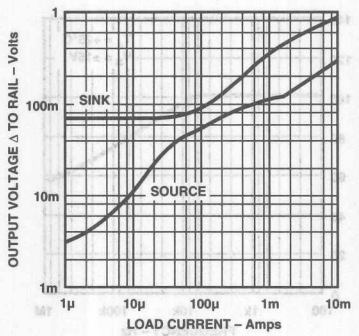


Figure 12. Output Voltage vs. Sink & Source Current

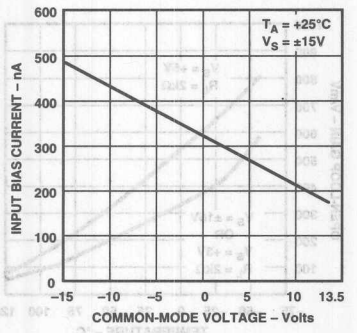


Figure 13. Input Bias Current vs. Common-Mode Voltage

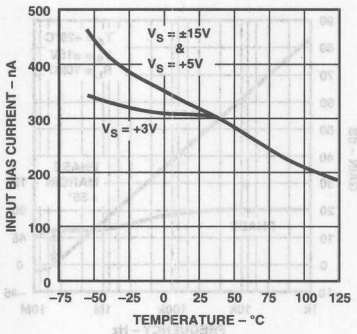


Figure 14. Input Bias Current vs. Temperature

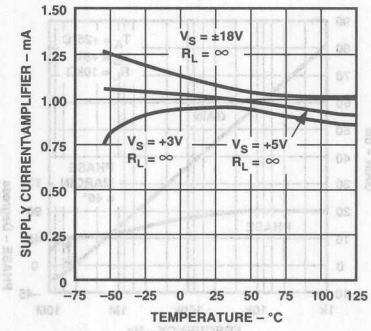


Figure 15. Supply Current per Amplifier vs. Temperature

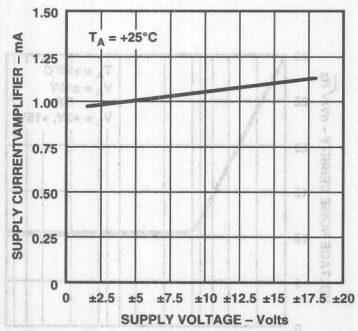


Figure 16. Supply Current per Amplifier vs. Supply Voltage

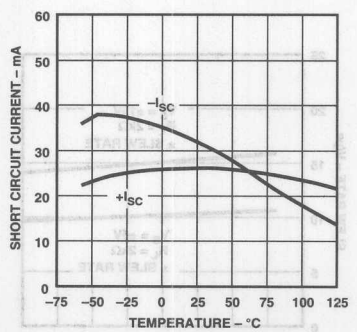


Figure 17. Short-Circuit Current vs. Temperature @ +5 V

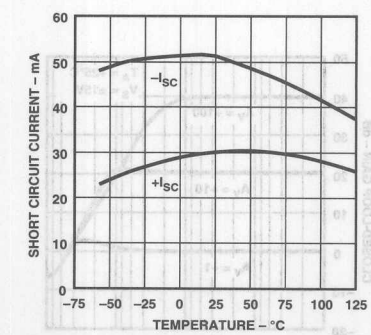


Figure 18. Short-Circuit Current vs. Temperature @ ±15 V

9

OP183/OP283–Typical Characteristics

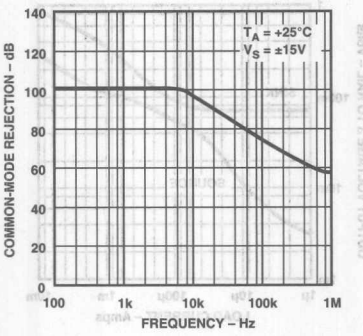


Figure 19. Common-Mode Rejection vs. Frequency

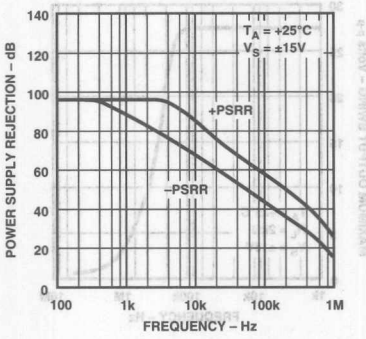


Figure 20. Power Supply Rejection vs. Frequency

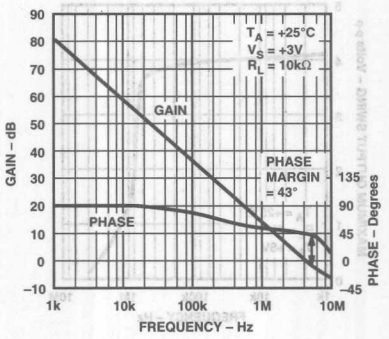


Figure 21. Open-Loop Gain and Phase vs. Frequency @ +3 V

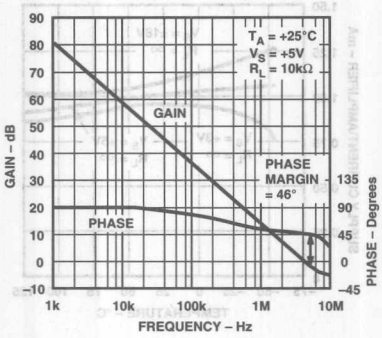


Figure 22. Open-Loop Gain and Phase vs. Frequency @ +5 V

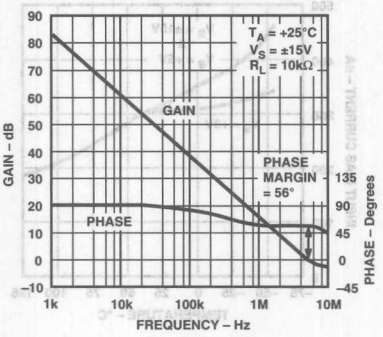


Figure 23. Open-Loop Gain and Phase vs. Frequency @ ±15 V

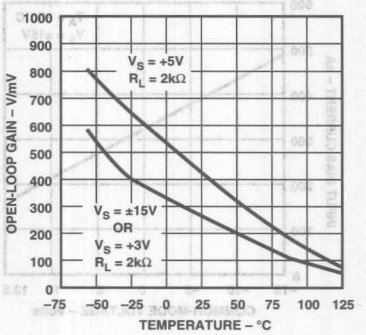


Figure 24. Open-Loop Gain vs. Temperature

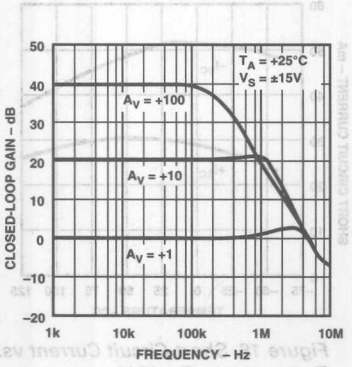


Figure 25. Closed-Loop Gain vs. Frequency

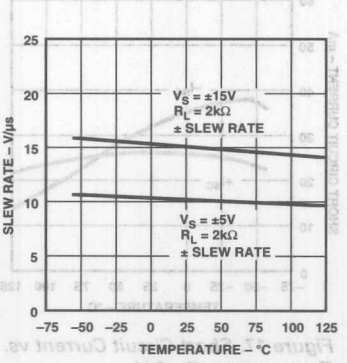


Figure 26. Slew Rate vs. Temperature

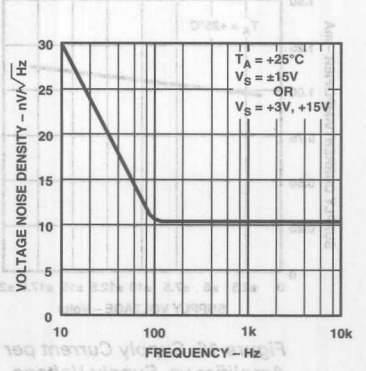


Figure 27. Voltage Noise Density vs. Frequency

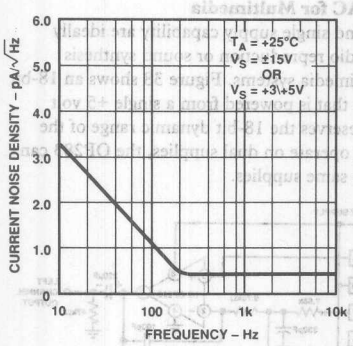


Figure 28. Current Noise Density vs. Frequency

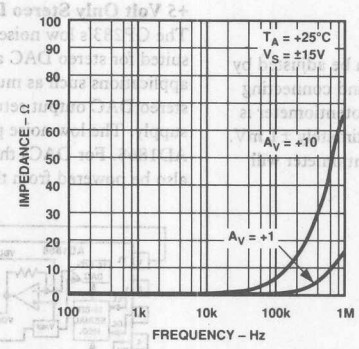


Figure 29. Closed-Loop Output Impedance vs. Frequency

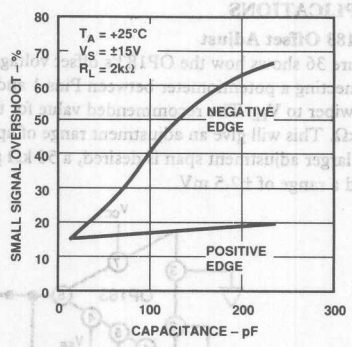


Figure 30. Small Signal Overshoot vs. Load Capacitance

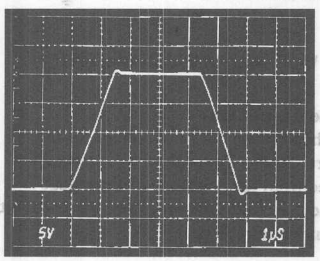


Figure 31. Large Signal Performance @ ±15 V

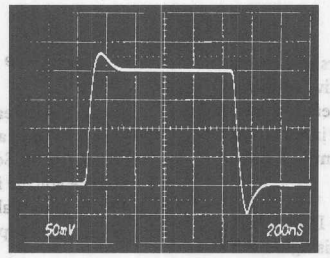


Figure 32. Small Signal Performance @ ±15 V

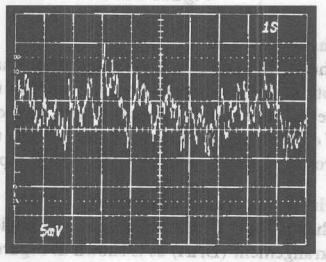


Figure 33. 0.1 Hz to 10 Hz Noise @ ± 2.5 V

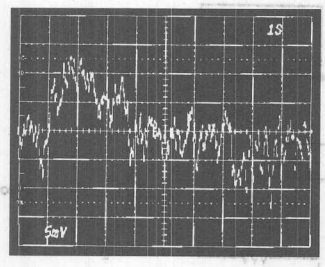


Figure 34. 0.1 Hz to 10 Hz Noise @ ±15 V

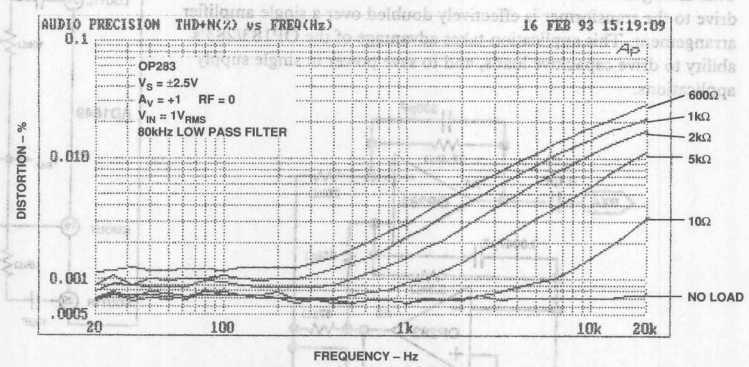


Figure 35. THD + Noise vs. Frequency for Various Loads

APPLICATIONS

OP183 Offset Adjust

Figure 36 shows how the OP183's offset voltage can be adjusted by connecting a potentiometer between Pins 1 and 5, and connecting the wiper to V_{EE}. The recommended value for the potentiometer is 10 kΩ. This will give an adjustment range of approximately ±1 mV. If a larger adjustment span is desired, a 50 kΩ potentiometer will yield a range of ±2.5 mV.

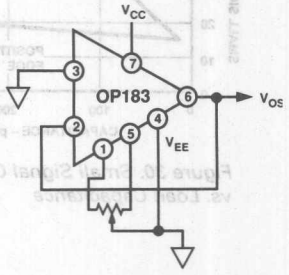


Figure 36. OP183 Offset Adjust

Phase Reversal

The OP183 family is protected against phase reversal as long as both of the inputs are within the range of the positive supply and the negative supply minus 0.6 volts. However if there is a possibility of either input going beyond these limits, then the inputs should be protected with a series resistor to limit input current to 2 mA.

Direct Access Arrangement

The OP183/OP283 can be used in a single supply Direct Access Arrangement (DAA) as is shown in Figure 37. This figure shows a portion of a typical DAA capable of operating from a single +5 volt supply and it should also work on +3 volt supplies with minor modifications. Amplifiers A2 and A3 are configured so that the transmit signal TXA is inverted by A2 and is not inverted by A3. This arrangement drives the transformer differentially so that the drive to the transformer is effectively doubled over a single amplifier arrangement. This application takes advantage of the OP183/283's ability to drive capacitive loads, and to save power in single supply applications.

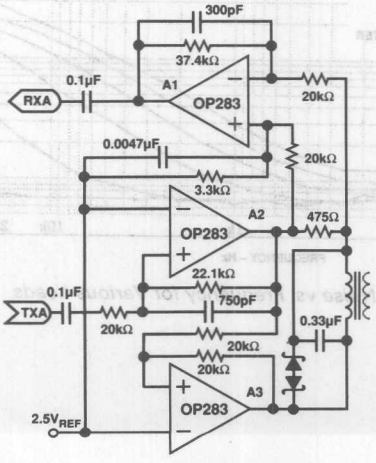


Figure 37. Direct Access Arrangement

+5 Volt Only Stereo DAC for Multimedia

The OP283's low noise and single supply capability are ideally suited for stereo DAC audio reproduction or sound synthesis applications such as multimedia systems. Figure 38 shows an 18-bit stereo DAC output setup that is powered from a single +5 volt supply. The low noise preserves the 18-bit dynamic range of the AD1868. For DACs that operate on dual supplies, the OP283 can also be powered from the same supplies.

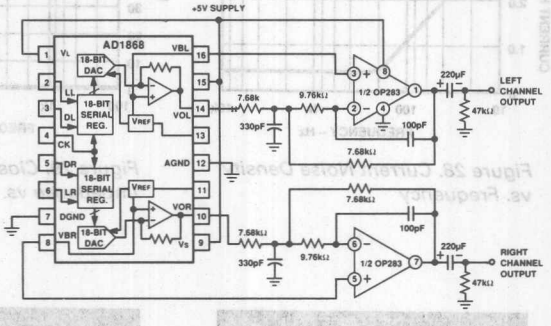


Figure 38. +5 Volt Only 18-Bit Stereo DAC

Low Voltage Headphone Amplifiers

Figure 39 shows a stereo headphone output amplifier for the AD1849 16-bit SoundPort® Stereo Codec device. The pseudo-reference voltage is derived from the common-mode voltage generated internally by the AD1849, thus providing a convenient bias for the headphone output amplifiers.

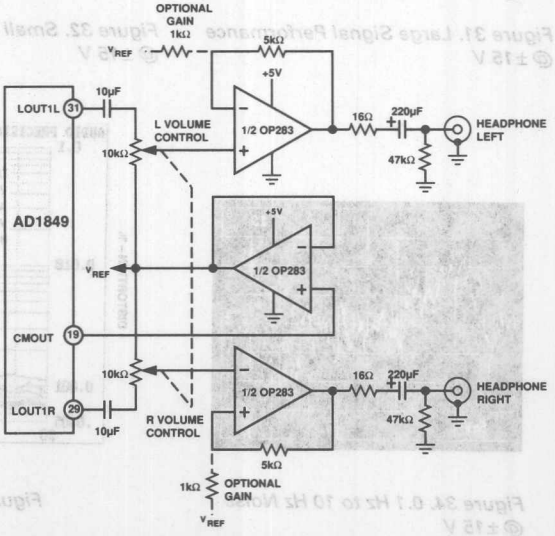


Figure 39. Headphone Output Amplifier for Multimedia Sound Codec

SoundPort is a registered trademark of Analog Devices Inc.

Low Noise Microphone Amplifier for Multimedia

The OP183 family is ideally suited as a low noise microphone preamp for low voltage audio applications. Figure 40 shows a gain of 100 stereo preamp for the AD1849 16-bit SoundPort Stereo Codec chip. The common-mode output buffer serves as a "phantom power" driver for the microphones.

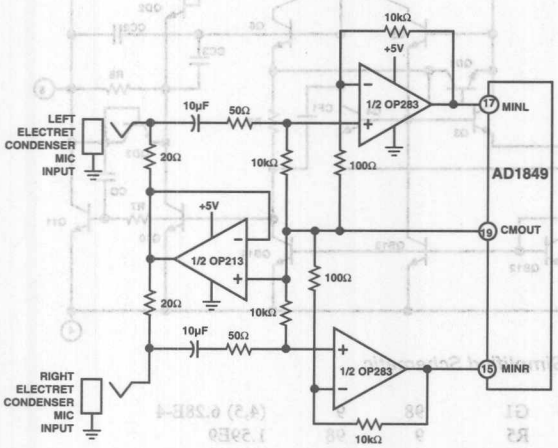


Figure 40. Low Noise Stereo Microphone Amplifier for Multimedia Sound CODEC

A +3 Volt 50 Hz/60 Hz Active Notch Filter with False Ground

To process ac signals, it may be easier to use a false-ground bias rather than the negative supply as a reference ground. This would reject the power-line frequency interference which oftentimes can obscure low frequency physiological signals, such as heart rates, blood pressures, EEGs, ECGs, et cetera.

Figure 41 shows a 50 Hz/60 Hz active notch filter for eliminating line noise in patient monitoring equipment. It has several kilohertz bandwidth and is not sensitive to false-ground perturbations. The simple false-ground circuit shown achieves good rejection of low frequency interference using standard off-the-shelf components.

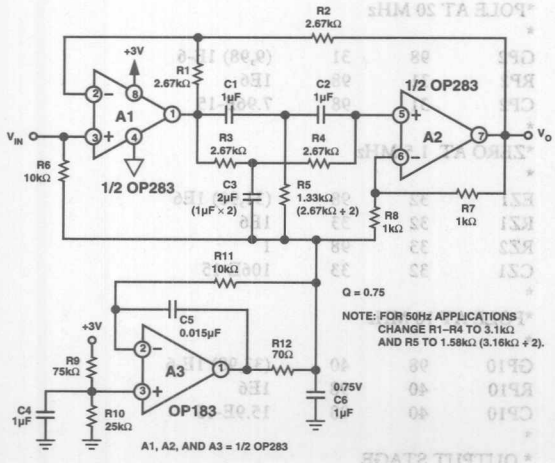


Figure 41. +3 Volt Supply 50 Hz/60 Hz Notch Filter with Pseudo Ground

Amplifier A3 biases A1 and A2 to the middle of their input common-mode range. When operating on a +3 V supply, the center of the OP283's common-mode range is 0.75 V. This notch filter effectively squelches 60 Hz pickup at a filter Q of 0.75. To reject 50 Hz interference, simply change the resistors in the twin-T section (R1 through R5) from 2.67 kΩ to 3.16 kΩ.

The filter section uses an OP283 dual op amp in a twin-T configuration whose frequency selectivity is very sensitive to the relative matching of the capacitors and resistors in the twin-T section. Mylar is the material of choice for the capacitors, and the relative matching of the capacitors and resistors determines the filter's pass band symmetry. Using 1% resistors and 5% capacitors produces satisfactory results.

A Low Voltage Frequency Synthesizer for Wireless Transceiver

The OP183's low noise and the low voltage operation capability serves well for the loop filter of a frequency synthesizer. Figure 42 shows a typical application in a radio transceiver. The phase noise performance of the synthesizer depends on low noise contribution from each component in the loop as the noise is amplified by the frequency division factor of the prescaler.

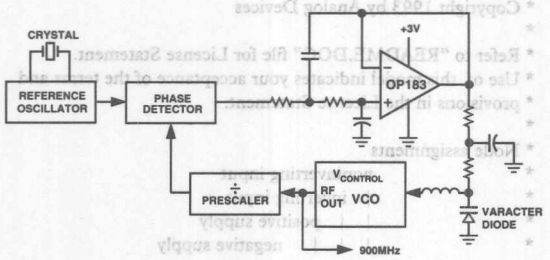


Figure 42. A Low Voltage Frequency Synthesizer for a Wireless Transceiver

The resistors used in the low-pass filter should be of low to moderate values to reduce noise contribution due to the input bias current as well as the resistors themselves. The filter cutoff frequency should be chosen to optimize the loop constant.

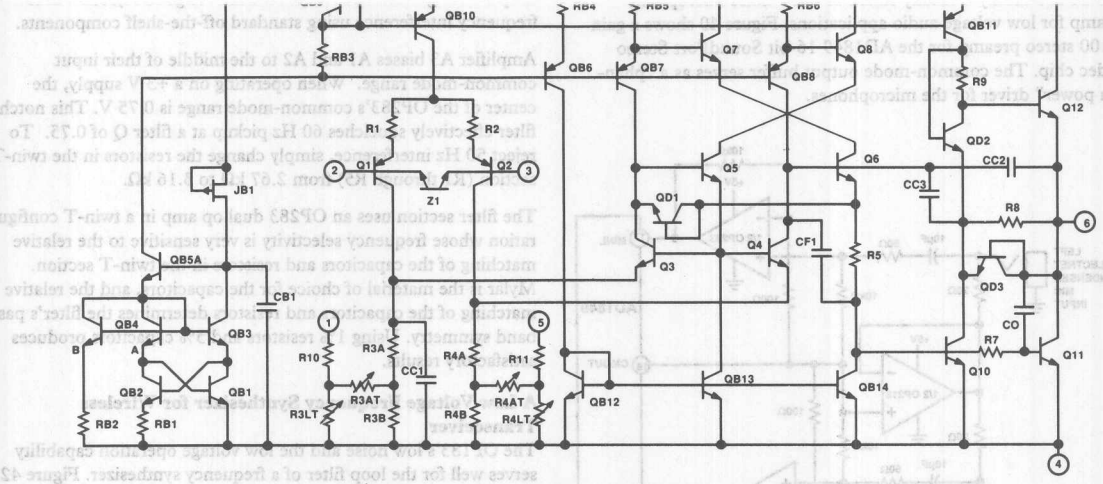
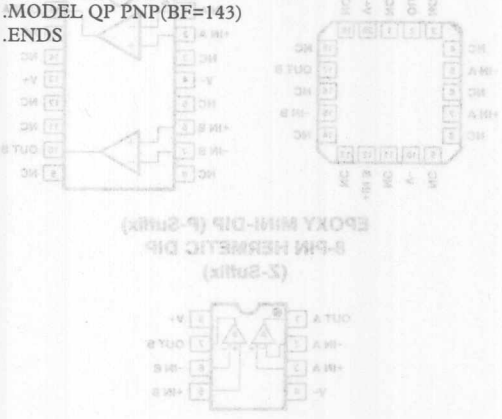


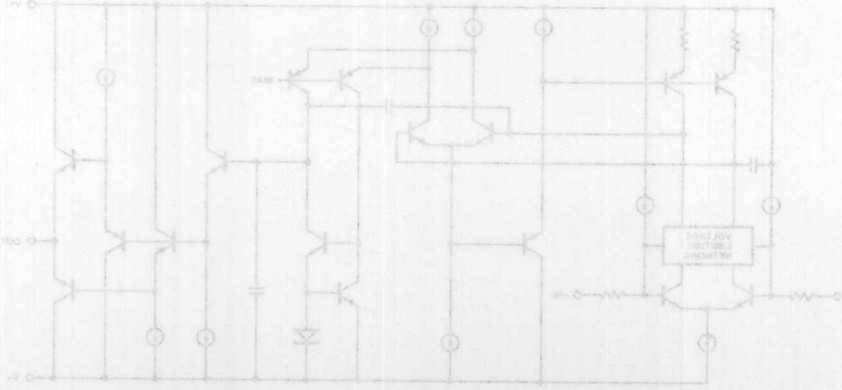
Figure 43. OP183 Simplified Schematic

```
* OP283 SPICE Macro-model                    Rev. A, 9/93
*                                            JCB/ADI
*
* Copyright 1993 by Analog Devices
*
* Refer to "README.DOC" file for License Statement.
* Use of  this model indicates your acceptance of the terms and
* provisions in the License Statement.
*
* Node assignments
*                    noninverting input
*                    | inverting input
*                    | | positive supply
*                    | | | negative supply
*                    | | | | output
*                    | | | | |
.SUBCKT OP283 2  1  99  50  45
*
* INPUT STAGE AND POLE AT 600 kHz
*
I1      99      8       1E-4
Q1      4       1       6       QP
Q2      5       3       7       QP
CIN     1       2       1.5PF
R1      50      4       1591
R2      50      5       1591
C1      4       5       83.4E-12
R3      6       8       1075
R4      7       8       1075
IOS     1       2       12.5E-9
EOS     3       2       POLY(1) (15,98) 25E-6 1
DC1     2       36      DZ
DC2     1       36      DZ
*
* GAIN STAGE AND DOMINANT POLE AT 10 Hz
*
EREF    98      0       POLY(2) (99,0) (50,0) 0 0.5 0.5
G1      98      9       (4,5) 6.28E-4
R5      9       98      1.59E9
C2      9       98      10E-12
D1      9       10      DX
D2      11      9       DX
E1      10      98      POLY(1)  99  98  -1.35  1.03
V2      50      11      -0.63
*
* COMMON MODE STAGE WITH ZERO AT 353 Hz
*
ECM     14      98      POLY(2) (1,98) (2,98) 0 3.5 3.5
R7      14      15      1E6
C4      14      15      3.75E-11
R8      15      98      1
*
*POLE AT 20 MHz
*
GP2     98      31      (9,98) 1E-6
RP2     31      98      1E6
CP2     31      98      7.96E-15
*
*ZERO AT  1.5 MHz
*
EZ1     32      98      (31,98) 1E6
RZ1     32      33      1E6
RZ2     33      98      1
CZ1     32      33      106E-15
*
*POLE AT 10 MHz
*
GP10    98      40      (33,98) 1E-6
RP10    40      98      1E6
CP10    40      98      15.9E-15
*
* OUTPUT STAGE
*
RO1     99      45      140
```

G8	50	45	(40,50)	7.14E-3
G9	98	60	(45,40)	7.14E-3
D7	60	61	DX	
D8	62	60	DX	
V7	61	98	DC 0	
V8	98	62	DC 0	
GSY	99	50	(99,50)5E-6	
FSY	99	50	POLY(2) V7 V8 1.075E-3 1 1	
D9	40	41	DX	
D10	42	40	DX	
V5	41	45	1.2	
V6	45	42	1.5	

```
*
* MODELS USED
*
.MODEL DX D
.MODEL DZ D(IS=1E-15 BV=7.0)
.MODEL QP PNP(BF=143)
.ENDS
```





Dual Low Offset, Low Power Operational Amplifier

OP200

FEATURES

- **Low Input Offset Voltage ..... 75μV Max**
- **Low Offset Voltage Drift, Over −55°C ≤ T_A ≤ +125°C ..... 0.5μV/°C Max**
- **Low Supply Current (Per Amplifier) ..... 725μA Max**
- **High Open-Loop Gain ..... 5000V/mV Min**
- **Low Input Bias Current ..... 2nA Max**
- **Low Noise Voltage Density ..... 11nV/$\sqrt{Hz}$ at 1kHz**
- **Stable With Large Capacitive Loads ..... 10nF Typ**
- **Pin Compatible to OP-14, OP-221, LM158, MC1458/1558, and LT1013 With Improved Performance**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
75	OP200AZ*	–	OP200ARC*	MIL
75	OP200EZ	–	–	XIND
150	OP200FZ	–	–	XIND
200	–	OP200GP	–	XIND
200	–	OP200GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

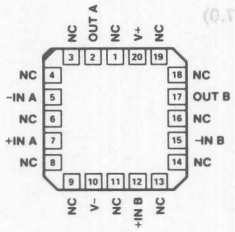
GENERAL DESCRIPTION

The OP-200 is the first monolithic dual operational amplifier to offer OP-77 type precision performance. Available in the industry standard 8-pin pinout, the OP-200 combines precision performance with the space and cost savings offered by a dual amplifier.

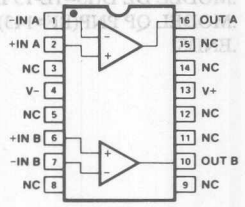
The OP-200 features an extremely low input offset voltage of less than 75μV with a drift below 0.5μV/°C, guaranteed over the

PIN CONNECTIONS

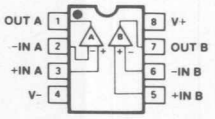
LCC (RC-Suffix)



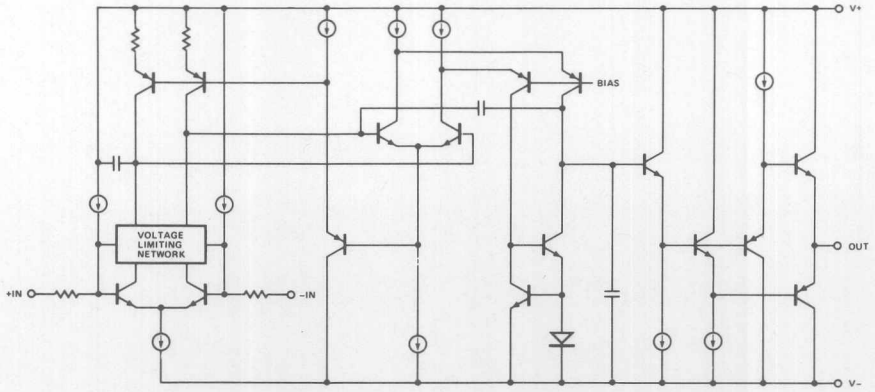
16-PIN SOL (S-Suffix)



EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP (Z-Suffix)



SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



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full military temperature range. Open-loop gain of the OP-200 exceeds 5,000,000 into a 10kΩ load; input bias current is under 2nA; CMR is over 120dB and PSRR below 1.8μV/V. On-chip zener-zap trimming is used to achieve the extremely low input offset voltage of the OP-200 and eliminates the need for offset nulling.

Power consumption of the OP-200 is very low, with each amplifier drawing less than 725μA of supply current. The total current drawn by the dual OP-200 is less than one-half that of a single OP-07, yet the OP-200 offers significant improvements over this industry standard op amp. The voltage noise density of the OP-200, 11nV/$\sqrt{Hz}$ at 1kHz, is half that of most competitive devices.

The OP-200 is pin compatible with the OP-14, OP-221, LM158, MC1458/1558, and LT1013 and can be used to upgrade systems using these devices. The OP-200 is an ideal choice for applications requiring multiple precision op amps and where low power consumption is critical.

For a quad precision op amp, see the OP-400.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, RC, S, Z-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP-200A ..... –55°C to +125°C
OP-200E, OP-200F ..... –40°C to +85°C
OP-200G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

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ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-200A/E			OP-200F			OP-200G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	25	75	—	50	150	—	80	200	μV
Long Term Input Voltage Stability			—	0.1	—	—	0.1	—	—	0.1	—	μV/mo
Input Offset Current	I_{OS}	V_{CM} = 0V	—	0.05	1.0	—	0.05	2.0	—	0.05	3.5	nA
Input Bias Current	I_B	V_{CM} = 0V	—	0.1	2.0	—	0.1	4.0	—	0.1	5.0	nA
Input Noise Voltage	$e_{n\ p-p}$	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	—	0.5	—	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 1)	—	22	36	—	22	36	—	22	—	nV/$\sqrt{Hz}$
		f_O = 1000Hz (Note 1)	—	11	18	—	11	18	—	11	—	
Input Noise Current	$i_{n\ p-p}$	0.1Hz to 10Hz	—	15	—	—	15	—	—	15	—	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz	—	0.4	—	—	0.4	—	—	0.4	—	pA/$\sqrt{Hz}$
Input Resistance Differential Mode	R_{IN}		—	10	—	—	10	—	—	10	—	MΩ
Input Resistance Common Mode	R_{INCM}		—	125	—	—	125	—	—	125	—	GΩ
Large Signal Voltage Gain	A_{VO}	V_O = ±10V										
		R_L = 10kΩ	5000	12000	—	3000	7000	—	3000	7000	—	V/mV
		R_L = 2kΩ	2000	3700	—	1500	3200	—	1500	3200	—	

PARAMETER	SYMBOL	CONDITIONS	OP-200A/E MIN	OP-200A/E TYP	OP-200A/E MAX	OP-200F MIN	OP-200F TYP	OP-200F MAX	OP-200G MIN	OP-200G TYP	OP-200G MAX	UNITS
Input Voltage Range	IVR	(Note 3)	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	V_{CM} = ±12V	120	135	—	115	135	—	110	130	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	—	0.4	1.8	—	0.4	3.2	—	0.6	5.6	μV/V
Output Voltage Swing	V_O	R_L = 10kΩ	±12	±12.6	—	±12	±12.6	—	±12	±12.6	—	V
		R_L = 2kΩ	±11	±12.2	—	±11	±12.2	—	±11	±12.2	—	
Supply Current Per Amplifier	I_{SY}	No Load	—	570	725	—	570	725	—	570	725	μA
Slew Rate	SR		0.1	0.15	—	0.1	0.15	—	0.1	0.15	—	V/μs
Gain Bandwidth Product	GBWP	A_V = +1	—	500	—	—	500	—	—	500	—	kHz
Channel Separation	CS	V_O = 20V_{p-p} f_O = 10Hz (Note 2)	123	145	—	123	145	—	123	145	—	dB
Input Capacitance	C_{IN}		—	3.2	—	—	3.2	—	—	3.2	—	pF
Capacitive Load Stability		A_V = +1 No Oscillations		10	—	—	10	—	—	10	—	nF

NOTES:
1. Sample tested.
2. Guaranteed but not 100% tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = +15V, −55°C ≤ T_A ≤ 125°C for OP-200A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-200A MIN	OP-200A TYP	OP-200A MAX	UNITS
Input Offset Voltage	V_{OS}		—	45	125	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.2	0.5	μV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	—	0.15	2.5	nA
Input Bias Current	I_B	V_{CM} = 0V	—	0.9	5.0	nA
Large Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10Ω	3000	9000	—	V/mV
		R_L = 2kΩ	1000	2700	—	
Input Voltage Range	IVR	(Note 1)	±12	±12.5	—	V
Common-Mode Rejection	CMR	V_{CM} = ±12V	115	130	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	—	0.2	3.2	μV/V
Output Voltage Swing	V_O	R_L = 10kΩ	±12	±12.4	—	V
		R_L = 2kΩ	±11	±12	—	
Supply Current Per Amplifier	I_{SY}	No Load	—	600	775	μA
Capacitive Load Stability		A_V = +1 No Oscillations	—	8	—	nF

NOTES:
1. Guaranteed by CMR test.

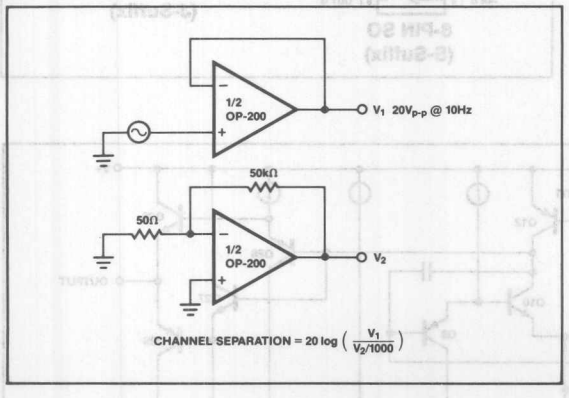
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40°C \le T_A \le +85°C$, unless otherwise noted.

			OP-200E			OP-200F			OP-200G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	35	100	—	80	250	—	110	300	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.2	0.5	—	0.5	1.5	—	0.6	2.0	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.08	2.5	—	0.08	3.5	—	0.1	6.0	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	0.3	5.0	—	0.3	7.0	—	0.5	10.0	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	3000 1500	10000 3200	—	2000 1000	5000 2500	—	2000 1000	5000 2500	—	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	—	±12	±12.5	—	±12	±12.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	130	—	110	130	—	105	130	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.15	3.2	—	0.15	5.6	—	0.3	10.0	μV/V
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	±12.4 ±12	—	±12 ±11	±12.4 ±12	—	±12 ±11	±12.4 ±12.2	—	V
Supply Current Per Amplifier	I_{SY}	No Load	—	600	775	—	600	775	—	600	775	μA
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	10	—	—	10	—	—	10	—	nF

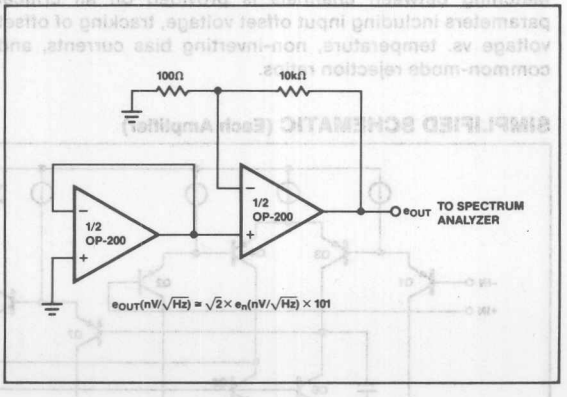
NOTES:
1. Guaranteed by CMR test.

9

CHANNEL SEPARATION TEST CIRCUIT



NOISE TEST SCHEMATIC



ANALOG DEVICES

Dual Micropower Operational Amplifier

OP220

FEATURES

- Excellent TCV_{OS} Match ..... 2μV/°C Max
- Low Input Offset Voltage ..... 150μV Max
- Low Supply Current 100μA
- Single-Supply Operation ..... +5V to +30V
- Low Input Offset Voltage Drift ..... 0.75μV/°C
- High Open-Loop Gain 2000V/mV
- High PSRR 3μV/V
- Low Input Bias Current 12nA
- Wide Common-Mode Voltage Range ..... V− to within 1.5V of V+
- Pin Compatible with 1458, LM158, LM2904
- Available in Die Form

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
150	OP220AJ*	OP220AZ	—	MIL
150	—	OP220EZ	—	IND
300	—	OP220FZ	—	IND
750	OP220CJ*	OP220CZ	—	MIL
750	OP220GJ	OP220GZ	OP220GP	XIND
750	—	—	OP220GS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

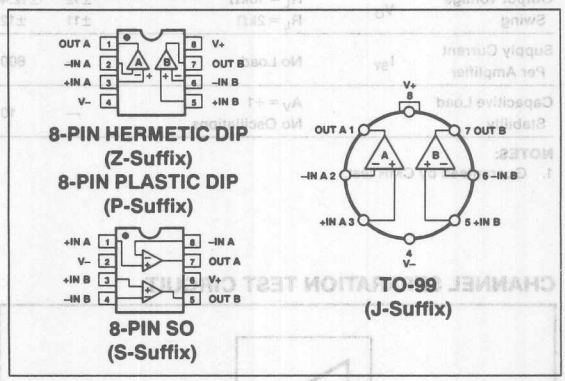
GENERAL DESCRIPTION

The OP-220 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The low offset voltage, and input offset voltage tracking as low as 1.0μV/°C, make this the first micropower precision dual operational amplifier.

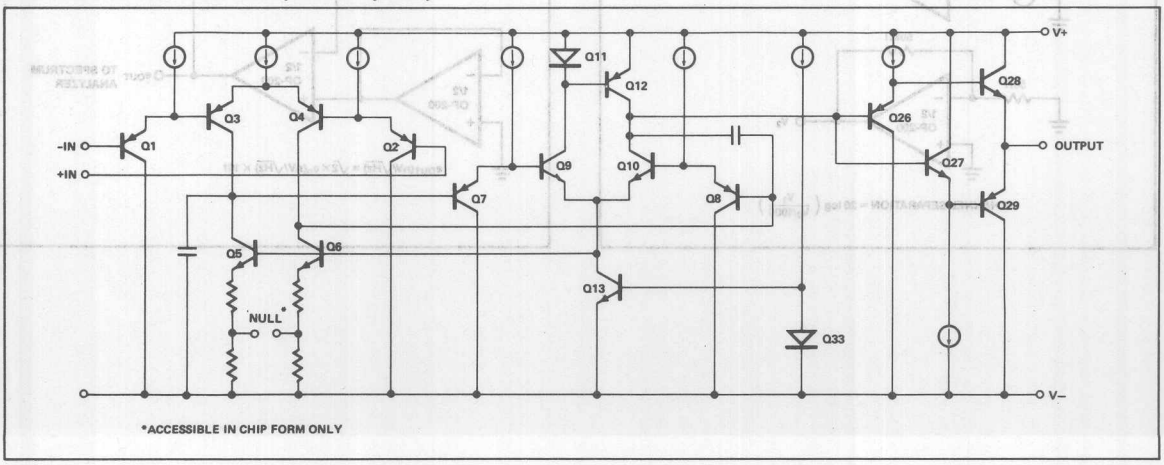
The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provides high performance in instrumentation amplifier designs. The individual amplifiers feature extremely low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection ratios.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (Each Amplifier)



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ELECTRICAL CHARACTERISTICS at V_S = ±2.5V to ±15V, –55°C ≤ T_A ≤ +125°C for OP-220A and C, –25°C ≤ T_A ≤ +85°C for OP-220E and F, –40°C ≤ T_A ≤ +85°C for OP-220G, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220F MIN	OP-220F TYP	OP-220F MAX	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	UNITS
Large-Signal Voltage Gain	A_{VO}	V_S = ±15V, R_L = 50kΩ V_O = ±10V	500	1000	—	500	800	—	400	500	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V– = 0V, R_L = 20kΩ	0.9/3.8	—	—	0.9/3.8	—	—	1/3.8	—	—	V
		V_S = ±15V, R_L = 50kΩ	±13.8	—	—	±13.8	—	—	±13.8	—	—	
Supply Current (Both Amplifiers)	I_{SY}	V_S = ±2.5V, No Load	—	135	170	—	155	185	—	170	210	µA
		V_S = ±15V, No Load	—	190	250	—	200	280	—	275	330	

NOTE: 1. Sample tested.

MATCHING CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220F MIN	OP-220F TYP	OP-220F MAX	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	150	300	—	250	500	—	300	600	µV
Average Noninverting Bias Current	I_B+	V_{CM} = 0	—	10	20	—	15	25	—	20	30	nA
Noninverting Offset Current	$I_{OS}+$	V_{CM} = 0	—	0.7	1.5	—	1	2	—	1.4	2.5	nA
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	V_{CM} = –15V to +13.5V	92	100	—	87	95	—	72	85	—	dB
Power Supply Rejection Ratio Match (Note 2)	ΔPSRR	V_S = ±2.5V to ±15V	—	6	14	—	18	44	—	57	140	µV/V

MATCHING CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A ≤ +125°C for OP-220A and C; –25°C ≤ T_A ≤ +85°C for OP-220E and F; –40°C ≤ T_A ≤ +85°C for OP-220G, unless otherwise noted. Grades E, F are sample tested.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220F MIN	OP-220F TYP	OP-220F MAX	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	250	500	—	400	800	—	800	1800	µV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	(Note 3)	—	1	2	—	1.5	3	—	1.5	5	µV/°C
Average Noninverting Bias Current	I_B+	V_{CM} = 0	—	10	25	—	15	30	—	22	40	nA
Average Drift of Noninverting Bias Current	TCI_B+	V_{CM} = 0 (Note 3)	—	15	25	—	15	30	—	30	50	pA/°C
Noninverting Offset Current	$I_{OS}+$	V_{CM} = 0	—	0.7	2	—	1	2.5	—	2.5	5	nA
Average Drift of Noninverting Offset Current	$TCI_{OS}+$	V_{CM} = 0 (Note 3)	—	7	15	—	12	22.5	—	15	30	pA/°C
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	V_{CM} = –15V to +13V	87	98	—	82	96	—	72	80	—	dB
Power Supply Rejection Ratio Match (Note 2)	ΔPSRR	V_S = ±2.5V to ±15V	—	10	26	—	30	78	—	57	250	µV/V

NOTES:

1. ΔCMRR is 20 $\log_{10} V_{CM}/\Delta CME$, where V_{CM} is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.
2. ΔPSRR is: $\frac{\text{Input-referred differential error}}{\Delta V_S}$
3. Sample tested.

Supply Voltage ..... ±18V
Differential Input Voltage ..... 30V or Supply Voltage
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-220A, C ..... –55°C to +125°C
OP-220E, F ..... –25°C to +85°C
OP-220G ..... –40°C to +85°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature (T) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = +25°C$, unless otherwise noted.

			OP-220A/E			OP-220F			OP-220C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	120	150	—	250	300	—	500	750	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.15	1.5	—	0.2	2	—	0.2	3.5	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	20	—	13	25	—	14	30	nA
Input Voltage Range	IVR	V+ = 5V, V– = 0V, $V_S = \pm 15V$	0/3.5 –15/13.5	—	—	0/3.5 –15/13.5	—	—	0/3.5 –15/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V– = 0V, $0V \le V_{CM} \le 3.5V$ $V_S = \pm 15V$, $-15V \le V_{CM} \le 13.5V$	90 95	100 100	—	85 90	90 95	—	75 80	85 90	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V– = 0V, V+ = 5V to 30V	—	3 6	10 18	—	10 18	32 57	—	32 57	100 180	µV/V
Large-Signal Voltage Gain	A_{VO}	V+ = 5V, V– = 0V, $R_L = 100k\Omega$ $1V \le V_O \le 3.5V$ $V_S = \pm 15V$, $R_L = 25k\Omega$ $V_O = \pm 10V$	500 1000	1000 2000	—	500 1000	800 2000	—	300 800	500 1600	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V– = 0V, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 25k\Omega$	0.7/4 ±14	—	—	0.7/4 ±14	—	—	0.8/4 ±14	—	—	V
Slew Rate	SR	$R_L = 25k\Omega$, (Note 1)	—	0.05	—	—	0.05	—	—	0.05	—	V/µs
Bandwidth	BW	$A_{VCL} = +1$, $R_L = 25k\Omega$	—	200	—	—	200	—	—	200	—	kHz
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	—	100 140	115 170	—	115 150	125 190	—	125 205	135 220	µA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-220A and C, $-25°C \le T_A \le +85°C$ for OP-220E and F, $-40°C \le T_A \le +85°C$ for OP-220G, unless otherwise noted.

			OP-220A/E			OP-220F			OP-220C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$V_S = \pm 15V$	—	0.75	1.5	—	1.2	2	—	2	3	µV/°C
Input Offset Voltage	V_{OS}		—	200	300	—	400	500	—	1000	1300	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.5	2	—	0.6	2.5	—	0.8	5	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	25	—	13	30	—	14	40	nA
Input Voltage Range	IVR	V+ = 5V, V– = 0V, $V_S = \pm 15V$	0/3.2 –15/13.2	—	—	0/3.2 –15/13.2	—	—	0/3.2 –15/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V– = 0V, $0V \le V_{CM} \le 3.2V$ $V_S = \pm 15V$ $-15V \le V_{CM} \le 13.2V$	85 90	90 95	—	80 85	85 90	—	70 75	80 85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V– = 0V, V+ = 5V to 30V	—	6 10	18 32	—	18 32	57 100	—	57 100	180 320	µV/V

Dual Low Power Operational Amplifier, Single or Dual Supply

OP221

FEATURES

- **Excellent TCV_{OS} Match ..... 2μV/°C Max**
- **Low Input Offset Voltage ..... 150μV Max**
- **Low Supply Current ..... 550μA Max**
- **Single Supply Operation ..... +5V to +30V**
- **Low Input Offset Voltage Drift ..... 0.75μV/°C**
- **High Open-Loop Gain ..... 1500V/mV Min**
- **High PSRR 3μV/V**
- **Wide Common-Mode Voltage Range ..... V− to within 1.5V of V+**
- **Pin Compatible with 1458, LM158, LM2904**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE TO-99	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
150	OP-221AJ/883	OP221AZ*	–	MIL
150	–	OP221EZ	–	IND
300	OP221BJ	–	–	MIL
500	OP221CJ	–	–	MIL
500	OP221GJ	OP221GZ	OP221GP	XIND
500	–	–	OP221GS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

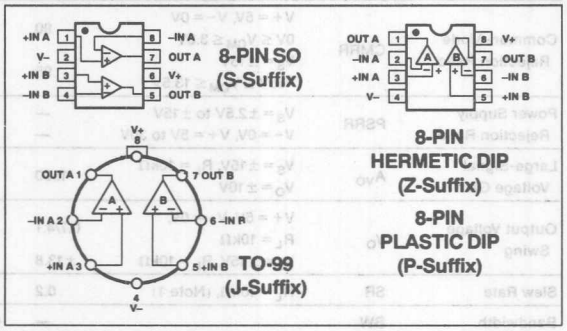
GENERAL DESCRIPTION

The OP-221 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The wide supply voltage range, wide input voltage range, and low supply current drain of the OP-221 make it well-suited for operation from batteries or unregulated power supplies.

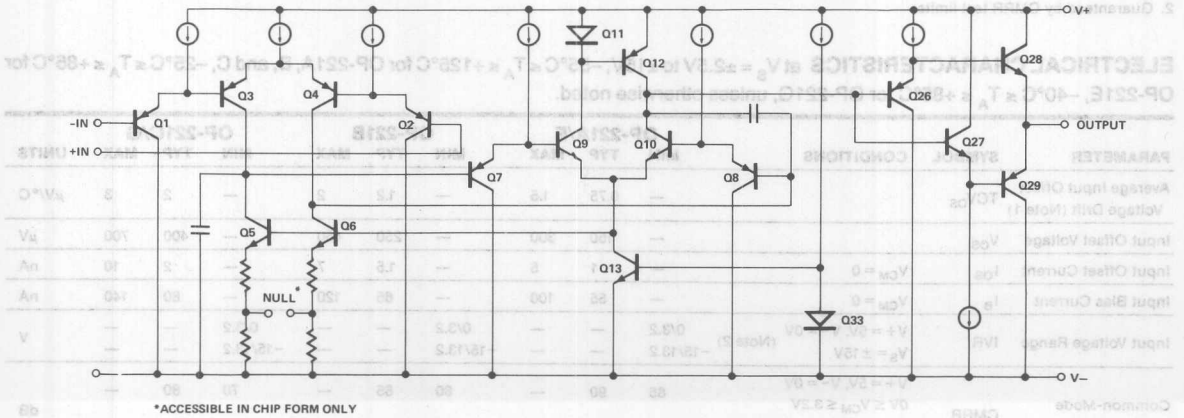
The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (Each Amplifier)



*ACCESSIBLE IN CHIP FORM ONLY

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... 30V or Supply Voltage
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-221A, B, C ..... –55°C to +125° C
OP-221E ..... –25°C to +85°C
OP-221G ..... –40°C to +85°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_J) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E MIN	OP-221A/E TYP	OP-221A/E MAX	OP-221B MIN	OP-221B TYP	OP-221B MAX	OP-221C/G MIN	OP-221C/G TYP	OP-221C/G MAX	UNITS
Input Offset Voltage	V_{OS}		—	75	150	—	150	300	—	250	500	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.5	3	—	1	5	—	1.5	7	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	50	80	—	60	100	—	70	120	nA
Input Voltage Range	IVR	V+ = 5V, V– = 0V (Note 2)	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	–15/13.5	—	—	–15/13.5	—	—	–15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V– = 0V $0V \le V_{CM} \le 3.5V$	90	100	—	85	90	—	75	85	—	dB
		$V_S = \pm 15V$ $-15V \le V_{CM} \le 13.5V$	95	100	—	90	95	—	80	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	3	10	—	10	32	—	32	100	µV/V
		V– = 0V, V+ = 5V to 30V	—	6	18	—	18	57	—	57	180	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_O = \pm 10V$	1500	—	—	1000	—	—	800	—	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V– = 0V, $R_L = 10k\Omega$	0.7/4.1	—	—	0.7/4.1	—	—	0.8/4	—	—	V
		$V_S = \pm 15V$, $R_L = 10k\Omega$	±13.8	—	—	±13.8	—	—	±13.5	—	—	
Slew Rate	SR	$R_L = 10k\Omega$, (Note 1)	0.2	0.3	—	0.2	0.3	—	0.2	0.3	—	V/µs
Bandwidth	BW		—	600	—	—	600	—	—	600	—	kHz
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	450	550	—	500	600	—	550	650	µA
		$V_S = \pm 15V$, No Load	—	600	800	—	800	850	—	850	900	

NOTES:
1. Sample tested.
2. Guaranteed by CMRR test limits.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-221A, B, and C, $-25°C \le T_A \le +85°C$ for OP-221E, $-40°C \le T_A \le +85°C$ for OP-221G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E MIN	OP-221A/E TYP	OP-221A/E MAX	OP-221B MIN	OP-221B TYP	OP-221B MAX	OP-221C/G MIN	OP-221C/G TYP	OP-221C/G MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}		—	0.75	1.5	—	1.2	2	—	2	3	µV/°C
Input Offset Voltage	V_{OS}		—	150	300	—	250	450	—	400	700	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	1	5	—	1.5	7	—	2	10	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	55	100	—	65	120	—	80	140	nA
Input Voltage Range	IVR	V+ = 5V, V– = 0V (Note 2)	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	–15/13.2	—	—	–15/13.2	—	—	–15/13.2	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V– = 0V $0V \le V_{CM} \le 3.2V$	85	90	—	80	85	—	70	80	—	dB
		$V_S = \pm 15V$ $-15V \le V_{CM} \le 13.2V$	90	95	—	85	90	—	75	85	—	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-221A, B, and C, $-25°C \le T_A \le +85°C$ for OP-221E, $-40°C \le T_A \le +85°C$ for OP-221G, unless otherwise noted. *(Continued)*

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E MIN	OP-221A/E TYP	OP-221A/E MAX	OP-221B MIN	OP-221B TYP	OP-221B MAX	OP-221C/G MIN	OP-221C/G TYP	OP-221C/G MAX	UNITS
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	6	18	—	18	57	—	57	180	µV/V
		$V- = 0V$, $V+ = 5V$ to $30V$	—	10	32	—	32	100	—	100	320	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$, $V_O = \pm 10V$	1000	—	—	800	—	—	600	—	—	V/mV
Output Voltage Swing	V_O	$V+ = 5V$, $V- = 0V$, $R_L = 10k\Omega$	0.8/3.8	—	—	0.8/3.8	—	—	0.9/3.7	—	—	V
		$V_S = \pm 15V$, $R_L = 10k\Omega$	±13.5	±14	—	±13.5	±14	—	±13.2	—	—	
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	500	650	—	550	700	—	600	750	µA
		$V_S = \pm 15V$, No Load	—	700	900	—	900	950	—	950	1000	

NOTES:
1. Sample tested.
2. Guaranteed by CMRR test limits.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E MIN	OP-221A/E TYP	OP-221A/E MAX	OP-221B MIN	OP-221B TYP	OP-221B MAX	OP-221C/G MIN	OP-221C/G TYP	OP-221C/G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	50	200	—	150	400	—	250	600	µV
Average Noninverting Bias Current	I_B+		—	—	80	—	—	100	—	—	120	nA
Noninverting Input Offset Current	$I_{OS}+$		—	2	5	—	2	5	—	4	10	nA
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	$V_{CM} = -15V$ to $+13.5V$	92	—	—	87	—	—	72	—	—	dB
Power Supply Rejection Ratio Match (Note 2)	ΔPSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	14	—	—	44	—	—	140	µV/V

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ for OP-221A, B, and C, $-25°C \le T_A \le +85°C$ for OP-221E, $-40°C \le T_A \le +85°C$ for OP-221G, unless otherwise noted. Grades E and G are sample tested.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E MIN	OP-221A/E TYP	OP-221A/E MAX	OP-221B MIN	OP-221B TYP	OP-221B MAX	OP-221C/G MIN	OP-221C/G TYP	OP-221C/G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	100	400	—	250	600	—	400	800	µV
Average Noninverting Bias Current	I_B+	$V_{CM} = 0$	—	—	100	—	—	120	—	—	140	nA
Input Offset Voltage Tracking	$TC\Delta V_{OS}$		—	1	2	—	1	3	—	3	5	µV/°C
Noninverting Input Offset Current	$I_{OS}+$	$V_{CM} = 0$	—	3	7	—	3	7	—	6	12	nA
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	$V_{CM} = -15V$ to $+13.2V$	87	90	—	82	85	—	72	80	—	dB
Power Supply Rejection Ratio Match (Note 2)	ΔPSRR		—	—	26	—	—	78	—	—	250	µV/V

NOTES:
1. ΔCMRR is $20 \log_{10} V_{CM}/\Delta CME$, where V_{CM} is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.
2. ΔPSRR is: $\frac{\text{Input-Referred Differential Error}}{\Delta V_S}$

FEATURES

- **Fast Slew Rate ..... 22V/µs Typ**
- **Settling Time (0.01%) ..... 1.2µs Max**
- **Offset Voltage ..... 300µV Max**
- **High Open-Loop Gain ..... 1000V/mV Min**
- **Low Total Harmonic Distortion ..... 0.002% Typ**
- **Improved Replacement for AD712, LT1057, OP-215, TL072, and MC34082**
- **Available in Die Form**

APPLICATIONS

- **Output Amplifier for Fast D/As**
- **Signal Processing**
- **Instrumentation Amplifiers**
- **Fast Sample/Holds**
- **Active Filters**
- **Low Distortion Audio Amplifiers**
- **Input Buffer for A/D Converters**
- **Servo Controllers**

GENERAL DESCRIPTION

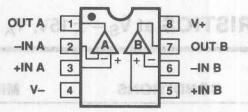
The OP-249 is a high-speed, precision dual JFET op amp, similar to the popular single op amp, the OP-42. The OP-249 outperforms available dual amplifiers by providing superior speed with excellent DC performance. Ultra-high open-loop gain (1kV/mV minimum), low offset voltage, and superb gain linearity, makes the OP-249 the industry's first true precision, dual high-speed amplifier.

With a slew rate of 22V/µs typical, and a fast settling time of less than 1.2µs maximum to 0.01%, the OP-249 is an ideal choice for high-speed bipolar D/A and A/D converter applications. The excellent DC performance of the OP-249 allows the full accuracy of high-resolution CMOS D/As to be realized.

Symmetrical slew rate, even when driving large loads, such as 600Ω, or 200pF of capacitance, and ultra-low distortion, make the OP-249 ideal for professional audio applications, active filters, high-speed integrators, servo systems, and buffer amplifiers.

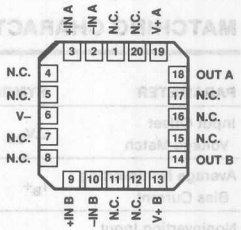
The OP-249 provides significant performance upgrades to the TL072, AD712, OP-215, MC34082 and the LT1057.

PIN CONNECTIONS

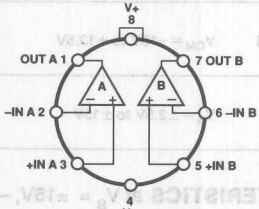


8-PIN CERDIP
(Z-Suffix)

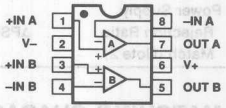
8-PIN EPOXY MINI-DIP
(P-Suffix)



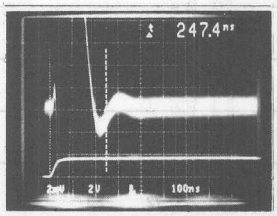
20-CONTACT LCC
(RC-Suffix)



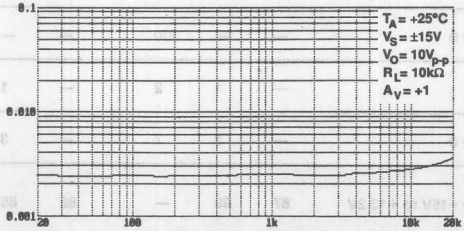
TO-99
(J-Suffix)



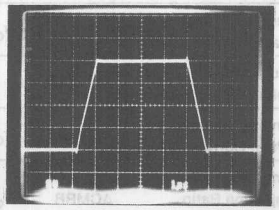
8-PIN SO
(S-Suffix)



FAST SETTLING
(0.01%)



LOW DISTORTION
A_V = +1, R_L = 10kΩ



EXCELLENT OUTPUT DRIVE
R_L = 600Ω

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ORDERING INFORMATION †

PACKAGE				OPERATING TEMPERATURE RANGE
TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	
OP249AJ*	OP249AZ*	–	OP249ARC/883	MIL
OP249EJ	–	–	–	XIND
OP249FJ	OP249FZ	–	–	XIND
–	–	OP249GP	–	XIND
–	–	OP249GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage (Note 2) ..... ±18V
Differential Input Voltage (Note 2) 36V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +175°C
Operating Temperature Range
OP-249A (J, Z, RC) ..... –55°C to +125°C
OP-249E,F (J, Z) ..... –40°C to +85°C
OP-249G (P, S) ..... –40°C to +85°C
Junction Temperature
OP-249 (J, Z, RC) ..... –65°C to +175°C
OP-249 (P, S) ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
TO-99 (J)	145	16	°C/W
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	150	41	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

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ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-249A			OP-249E			OP-249F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}		–	0.2	0.5	–	0.1	0.3	–	0.2	0.7	mV
Long Term Offset Voltage	V_{OS}	(Note 1)	–	–	0.8	–	–	0.6	–	–	1.0	mV
Offset Stability			–	1.5	–	–	1.5	–	–	1.5	–	µV/Month
Input Bias Current	I_B	V_{CM} = 0V, T_j = +25°C	–	30	75	–	20	50	–	30	75	pA
Input Offset Current	I_{OS}	V_{CM} = 0V, T_j = +25°C	–	6	25	–	4	15	–	6	25	pA
Input Voltage Range	IVR	(Note 2)	±11	+12.5 –12.5	–	±11	+12.5 –12.5	–	±11	+12.5 –12.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	80	90	–	86	95	–	80	90	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	12	31.6	–	9	31.6	–	12	50	µV/V
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 2kΩ	1000	1400	–	1000	1400	–	500	1200	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	+12.5 –12.5	–	±12.0	+12.5 –12.5	–	±12.0	+12.5 –12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+36 –33	±50	±20	+36 –33	±50	±20	+36 –33	±50	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.6	7.0	–	5.6	7.0	–	5.6	7.0	mA
Slew Rate	SR	R_L = 2kΩ, C_L = 50pF	18	22	–	18	22	–	18	22	–	V/µs
Gain-Bandwidth Product	GBW	(Note 4)	3.5	4.7	–	3.5	4.7	–	3.5	4.7	–	MHz
Settling Time	t_s	10V Step 0.01% (Note 3)	–	0.9	1.2	–	0.9	1.2	–	0.9	1.2	µs
Phase Margin	Θ_0	0dB Gain	–	55	–	–	55	–	–	55	–	Deg

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-249A MIN	OP-249A TYP	OP-249A MAX	OP-249E MIN	OP-249E TYP	OP-249E MAX	OP-249F MIN	OP-249F TYP	OP-249F MAX	UNITS
Differential Input Impedance	Z_{IN}		–	10^{12}||6	–	–	10^{12}||6	–	–	10^{12}||6	–	Ω||pF
Open-Loop Output Resistance	R_O		–	35	–	–	35	–	–	35	–	Ω
Voltage Noise	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	–	2	–	–	2	–	–	2	–	$\mu V_{p\text{-}p}$
Voltage Noise Density	e_n	f_O = 10Hz	–	75	–	–	75	–	–	75	–	nV/√Hz
		f_O = 100Hz	–	26	–	–	26	–	–	26	–	
		f_O = 1kHz	–	17	–	–	17	–	–	17	–	
		f_O = 10kHz	–	16	–	–	16	–	–	16	–	
Current Noise Density	i_n	f_O = 1kHz	–	0.003	–	–	0.003	–	–	0.003	–	pA/√Hz
Voltage Supply Range	V_S		±4.5	±15	±18	±4.5	±15	±18	±4.5	±15	±18	V

NOTES:
1 Long term offset voltage is guaranteed by a 1000 HR life test performed on 3 independent wafer lots at +125°C with a LTPD of 3.
2. Guaranteed by CMR test.
3. Settling-time is sample tested.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-249G MIN	OP-249G TYP	OP-249G MAX	UNITS
Offset Voltage	V_{OS}		–	0.4	2.0	mV
Input Bias Current	I_B	V_{CM} = 0V, T_j = +25°C	–	40	75	pA
Input Offset Current	I_{OS}	V_{CM} = 0V, T_j = +25°C	–	10	25	pA
Input Voltage Range	IVR	(Note 1)	±11	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	76	90	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	12	50	µV/V
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 2kΩ	500	1100	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	+12.5 –12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+36 –33	±50	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.6	7.0	mA
Slew Rate	SR	R_L = 2kΩ, C_L = 50pF	18	22	–	V/µs
Gain-Bandwidth Product	GBW	(Note 2)	–	4.7	–	MHz
Settling Time	t_s	10V Step 0.01%	–	0.9	1.2	µs
Phase Margin	Θ_0	0dB Gain	–	55	–	Deg

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-249G MIN	OP-249G TYP	OP-249G MAX	UNITS
Differential Input Impedance	Z_{IN}		–	$10^{12}\|\|6$	–	Ω||pF
Open-Loop Output Resistance	R_O		–	35	–	Ω
Voltage Noise	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	–	2	–	$\mu V_{p\text{-}p}$
Voltage Noise Density	e_n	f_O = 10Hz	–	75	–	$nV/\sqrt{Hz}$
		f_O = 100Hz	–	26	–	
		f_O = 1kHz	–	17	–	
		f_O = 10kHz	–	16	–	
Current Noise Density	i_n	f_O = 1kHz	–	0.003	–	$pA/\sqrt{Hz}$
Voltage Supply Range	V_S		±4.5	±15	±18	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-40°C \le T_A \le +85°C$ for E/F grades, and $-55°C \le T_A \le +125°C$ for A grade, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-249A MIN	OP-249A TYP	OP-249A MAX	OP-249E MIN	OP-249E TYP	OP-249E MAX	OP-249F MIN	OP-249F TYP	OP-249F MAX	UNITS
Offset Voltage	V_{OS}		–	0.12	1.0	–	0.1	0.5	–	0.5	1.1	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	1	5	–	1	3	–	1.2	6	µV/°C
Input Bias Current	I_B	(Note 1)	–	4	20	–	0.25	3.0	–	0.3	4.0	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.04	4	–	0.01	0.7	–	0.02	1.2	nA
Input Voltage Range	IVR	(Note 2)	±11	+12.5 −12.5	–	±11	+12.5 −12.5	–	±11	+12.5 −12.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	76	110	–	86	100	–	76	95	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	5	50	–	5	50	–	7	100	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ V_O = ±10V	500	1400	–	750	1400	–	250	1200	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	+12.5 −12.5	–	±12.0	+12.5 −12.5	–	±12.0	+12.5 −12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±10	–	±60	±18	–	±60	±18	–	±60	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.6	7.0	–	5.6	7.0	–	5.6	7.0	mA

NOTES:

1. $T_j = 85°C$ for E/F Grades; $T_j = 125°C$ for A Grade.
2. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-40°C \le T_A \le +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-249G MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}		–	1.0	3.6	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	6	25	µV/°C
Input Bias Current	I_B	(Note 1)	–	0.5	4.5	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.04	1.5	nA
Input Voltage Range	IVR	(Note 2)	±11.0	+12.5 –12.5	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm11V$	76	95	–	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm4.5V$ to $\pm18V$	–	10.0	100	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm10V$	250	1200	–	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12.0	+12.5 –12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±18	–	±60	mA
Supply Current	I_{SY}	No Load $V_O = 0V$	–	5.6	7.0	mA

NOTES:
1. $T_j = 85°C$.
2. Guaranteed by CMR test.

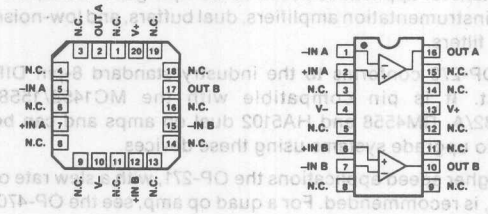
Dual Very Low Noise Precision Operational Amplifier

OP270

FEATURES

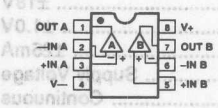
- Very Low Noise ..... 5nV/$\sqrt{Hz}$ @ 1kHz Max
- Excellent Input Offset Voltage ..... 75μV Max
- Low Offset Voltage Drift ..... 1μV/°C Max
- Very High Gain ..... 1500V/mV Min
- Outstanding CMR ..... 106dB Min
- Slew Rate ..... 2.4V/μs Typ
- Gain-Bandwidth Product ..... 5MHz Typ
- Industry Standard 8-Pin Dual Pinout
- Available In Die Form

PIN CONNECTIONS



LCC (RC-Suffix)

16-PIN SOL (S-Suffix)



EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP (Z-Suffix)

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
75	OP270AZ*	–	OP270ARC/883	MIL
75	OP270EZ	–	–	XIND
150	OP270FZ	–	–	XIND
250	–	OP270GP	–	XIND
250	–	OP270GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

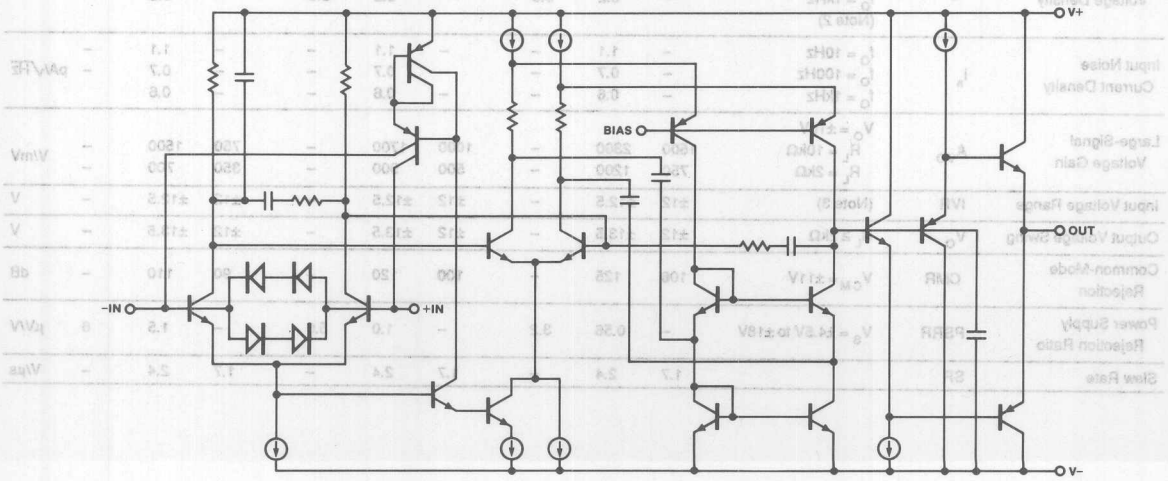
†† For availability and burn-in information on SO and PLCC packages, contact you local sales office.

GENERAL DESCRIPTION

The OP-270 is a high-performance monolithic dual operational amplifier with exceptionally low voltage noise, 5nV/$\sqrt{Hz}$ at 1kHz Max, offering comparable performance to PMI's industry standard OP-27.

The OP-270 features an input offset voltage below 75μV and an offset drift under 1μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP-270 is over 1,500,000 into a 10kΩ load insuring excellent gain accuracy and linearity, even in high-gain applications. Input bias current is under 20nA which reduces errors due to signal source resistance. The OP-270's CMR of over 106dB and PSRR of less than 3.2μV/V significantly reduce errors due to

SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

OP-27s, a significant advantage for power conscious applications. The OP-270 is unity-gain stable with a gain-bandwidth product of 5MHz and a slew rate of 2.4V/μs.

The OP-270 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, dual buffers, and low-noise active filters.

The OP-270 conforms to the industry standard 8-pin DIP pinout. It is pin compatible with the MC1458/1558, SE5532/A, RM4558 and HA5102 dual op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP-271, with a slew rate of 8V/μs, is recommended. For a quad op amp, see the OP-470.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP-270A ..... –55°C to +125°C
OP-270E, OP-270F, OP-270G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-270's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±10V, the input current should be limited to ±25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-270A/E			OP-270F			OP-270G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	–	–	10	75	–	20	150	–	50	250	μV
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1	10	–	3	15	–	5	20	nA
Input Bias Current	I_B	V_{CM} = 0V	–	5	20	–	10	40	–	15	60	nA
Input Noise Voltage	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz (Note 1)	–	80	200	–	80	200	–	80	–	nVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz	–	3.6	6.5	–	3.6	6.5	–	3.6	–	nV/√Hz
		f_O = 100Hz	–	3.2	5.5	–	3.2	5.5	–	3.2	–	
		f_O = 1kHz (Note 2)	–	3.2	5.0	–	3.2	5.0	–	3.2	–	
Input Noise Current Density	i_n	f_O = 10Hz	–	1.1	–	–	1.1	–	–	1.1	–	pA/√Hz
		f_O = 100Hz	–	0.7	–	–	0.7	–	–	0.7	–	
		f_O = 1kHz	–	0.6	–	–	0.6	–	–	0.6		
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10kΩ	1500	2300	–	1000	1700	–	750	1500	–	V/mV
		R_L = 2kΩ	750	1200	–	500	900	–	350	700	–	
Input Voltage Range	IVR	(Note 3)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13.5	–	±12	±13.5	–	±12	±13.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	106	125	–	100	120	–	90	110	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	0.56	3.2	–	1.0	5.6	–	1.5	6	μV/V
Slew Rate	SR		1.7	2.4	–	1.7	2.4	–	1.7	2.4	–	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-270A/E MIN	OP-270A/E TYP	OP-270A/E MAX	OP-270F MIN	OP-270F TYP	OP-270F MAX	OP-270G MIN	OP-270G TYP	OP-270G MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4	6.5	–	4	6.5	–	4	6.5	mA
Gain Bandwidth Product	GBW		–	5	–	–	5	–	–	5	–	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	175	–	125	175	–	–	175	–	dB
Input Capacitance	C_{IN}		–	3	–	–	3	–	–	3	–	pF
Input Resistance Differential-Mode	R_{IN}		–	0.4	–	–	0.4	–	–	0.4	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	20	–	–	20	–	–	20	–	GΩ
Settling Time	t_s	$A_V = +1$, 10V Step to 0.01%	–	5	–	–	5	–	–	5	–	µs

NOTES:
1. Guaranteed by not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

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ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-55°C \le T_A \le +125°C$ for OP-270A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-270A MIN	OP-270A TYP	OP-270A MAX	UNITS
Input Offset Voltage	V_{OS}		–	30	175	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.2	1	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	2	30	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	6	60	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 750 400	 1600 800	 – –	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm11V$	100	120	–	dB
Power Supply Rejection Ration	PSRR	$V_S = \pm4.5V$ to ±18V	–	1.0	5.6	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.5	7.5	mA

NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

			OP-270E			OP-270F			OP-270G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		–	25	150	–	45	275	–	100	400	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.2	1	–	0.4	2	–	0.7	3	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1.5	30	–	5	40	–	15	50	nA
Input Bias Current	I_B	V_{CM} = 0V	–	6	60	–	15	70	–	19	80	nA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10kΩ R_L = 2kΩ	1000 500	1800 900	– –	600 300	1400 700	– –	400 225	1250 670	– –	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13	–	±12	±13	–	±12	±13	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	100	120	–	94	115	–	90	100	–	dB
Power Supply Rejection Ration	PSRR	V_S = ±4.5V to ±18V	–	0.7	5.6	–	1.8	10	–	2.0	15	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.4	7.2	–	4.4	7.2	–	4.4	7.2	mA

NOTE:
1. Guaranteed by CMR test.

ANALOG DEVICES

High Speed, Dual Operational Amplifier

OP271

FEATURES

- Excellent Speed ..... 8.5V/μs Typ
- Fast Settling (0.01%) ..... 2μs Typ
- Unity-Gain Stable
- High Gain-Bandwidth ..... 5MHz Typ
- Low Input Offset Voltage ..... 200μV Max
- Low Offset Voltage Drift ..... 2μV/°C Max
- High Gain ..... 400V/mV Min
- Outstanding CMR ..... 106 dB Min
- Industry Standard 8-Pin Dual Pinout
- Available in Die Form

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP 8-PIN	PLASTIC	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
200	OP271AZ*	–	OP271ARC/883	MIL
200	OP271EZ	–	–	XND
300	OP271FZ	–	–	XND
400	–	OP271GP	–	XND
400	–	OP271GS††	–	XND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

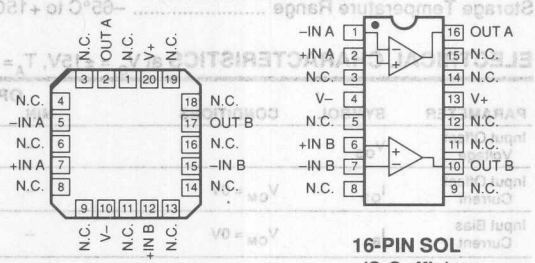
GENERAL DESCRIPTION

The OP-271 is a unity-gain stable monolithic dual op amp featuring excellent speed, 8.5V/μs typical, and fast settling time, 2μs typical to 0. 01%. The OP-271 has a gain-bandwidth of 5MHz with a high phase margin of 62°.

Input offset voltage of the OP-271 is under 200μV with input offset voltage drift below 2μV/°C, guaranteed over the full military temperature range. Open-loop gain exceeds 400,000 into a 10kΩ load ensuring outstanding gain accuracy and linearity. The input bias current is under 20nA limiting errors due to source resistance. The OP-271's outstanding CMR, over 106dB, and low PSRR, under 5.6μV/V, reduce errors caused by ground noise and power supply fluctuations. In addition, the OP-271 exhibits high CMR and PSRR over a wide frequency range, further improving system accuracy.

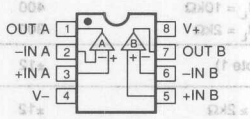
Continued

PIN CONNECTIONS



LCC (RC-Suffix)

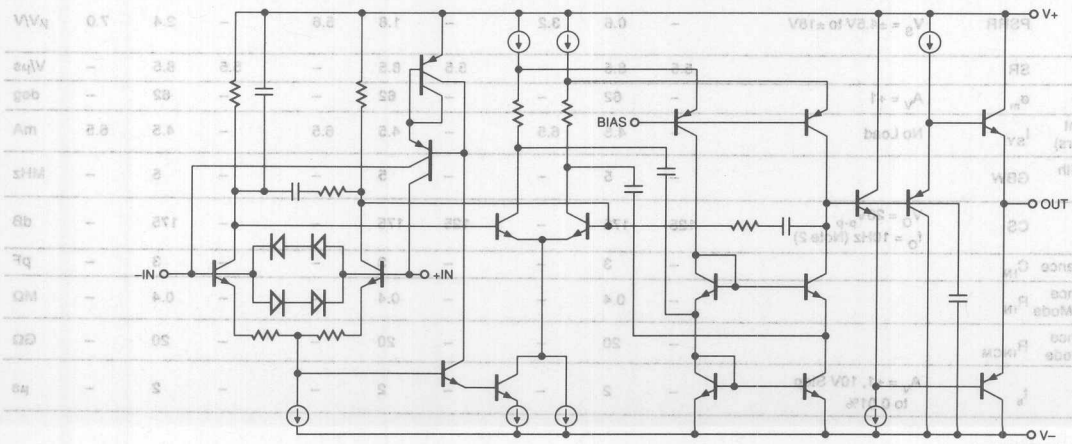
16-PIN SOL (S-Suffix)



EPOXY MINI-DIP (P-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC (One of the two amplifiers is shown.)



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

multiple gain blocks, high-speed instrumentation and amplifiers, buffers and active filters.

The OP-271 conforms to the industry standard 8-pin dual op amp pinout. It is pin compatible with the TL072, TL082, LF412, and 1458/1558 dual op amps and can be used to significantly improve systems using these devices.

For applications requiring lower voltage noise, see the OP-270. For a quad version of the OP-271, see the OP-471.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range ..... –65°C to +150°C

Operating Temperature Range
OP-271A ..... –55°C to +125°C
OP-271E, OP-271F, OP-271G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-271's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-271A/E			OP-271F			OP-271G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		–	75	200	–	150	300	–	200	400	µV
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1	10	–	4	15	–	7	20	nA
Input Bias Current	I_B	V_{CM} = 0V	–	4	20	–	6	40	–	12	60	nA
Input Noise Voltage Density	e_n	f_O = 1kHz	–	7.6	–	–	7.6	–	–	7.6	–	nV/ Hz
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10kΩ	400	650	–	300	500	–	250	400	–	V/mV
		R_L = 2kΩ	300	500	–	200	300	–	175	250	–	
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13	–	±12	±13	–	±12	±13	–	V
Common-Mode Rejection	CMR	V_{CM} = ±12V	106	120	–	100	115	–	90	105	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	0.6	3.2	–	1.8	5.6	–	2.4	7.0	µV/V
Slew Rate	SR		5.5	8.5	–	5.5	8.5	–	5.5	8.5	–	V/µs
Phase Margin	ϕ_m	A_V = +1	–	62	–	–	62	–	–	62	–	deg
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.5	6.5	–	4.5	6.5	–	4.5	6.5	mA
Gain Bandwidth Product	GBW		–	5	–	–	5	–	–	5	–	MHz
Channel Separation	CS	V_O = 20V_{p-p} f_O = 10Hz (Note 2)	125	175	–	125	175	–	–	175	–	dB
Input Capacitance	C_{IN}		–	3	–	–	3	–	–	3	–	pF
Input Resistance Differential-Mode	R_{IN}		–	0.4	–	–	0.4	–	–	0.4	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	20	–	–	20	–	–	20	–	GΩ
Settling Time	t_s	A_V = +1, 10V Step to 0.01%	–	2	–	–	2	–	–	2	–	µs

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed but not 100% tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$ for OP-271A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-271A MIN	OP-271A TYP	OP-271A MAX	UNITS
Input Offset Voltage	V_{OS}		—	115	400	µV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	1.5	30	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	7	60	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 300 200	 600 500	 — —	 V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	—	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	1.0	5.6	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	5.3	7.5	mA

NOTE:
1. Guaranteed by CMR test.

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ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40°C \le T_A \le +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-271A/E MIN	OP-271A/E TYP	OP-271A/E MAX	OP-271F MIN	OP-271F TYP	OP-271F MAX	OP-271G MIN	OP-271G TYP	OP-271G MAX	UNITS
Input Offset Voltage	V_{OS}		–	100	330	–	215	560	–	300	700	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.4	2	–	1	4	–	2.0	5	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	1	30	–	5	40	–	15	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	6	60	–	10	70	–	15	80	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 300 200	 600 500	 – –	 200 100	 500 400	 – –	 150 90	 400 300	 – –	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	100	120	–	94	115	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	–	0.7	5.6	–	51.8	10	–	2.0	15	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	–	5.2	7.2	–	5.2	7.2	–	5.2	7.2	mA

NOTE:
1. Guaranteed by CMR test.

Dual Bipolar/JFET, Audio Operational Amplifier

OP275*

FEATURES

Excellent Sonic Characteristics
Low Noise: 6 nV/√Hz
Low Distortion: 0.0006%
High Slew Rate: 22 V/μs
Wide Bandwidth: 9 MHz
Low Supply Current: 5 mA
Low Offset Voltage: 1 mV
Low Offset Current: 2 nA
Unity Gain Stable
SOIC-8 Package

APPLICATIONS

High Performance Audio
Active Filters
Fast Amplifiers
Integrators

GENERAL DESCRIPTION

The OP-275 is the first amplifier to feature the Butler Amplifier front-end. This new front-end design combines both bipolar and JFET transistors to attain amplifiers with the accuracy and low noise performance of bipolar transistors, and the speed and sound quality of JFETs. Total Harmonic Distortion plus Noise equals previous audio amplifiers, but at much lower supply currents.

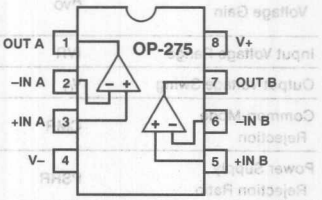
A very low 1/f corner of below 6 Hz maintains a flat noise density response. Whether noise is measured at either 30 Hz or 1 kHz, it is only 6 nV/√Hz. The JFET portion of the input stage gives the OP-275 its high slew rates to keep distortion low, even when large output swings are required, and the 22 V/μs slew rate of the OP-275 is the fastest of any standard audio amplifier. Best of all, this low noise and high speed are accomplished using less than 5 mA of supply current, lower than any standard audio amplifier.

*Patent pending.

PIN CONNECTIONS

8-Lead Narrow Body SOIC (S Suffix)

8-Lead Epoxy DIP (P Suffix)



Improved dc performance is also provided with bias and offset currents greatly reduced over purely bipolar designs. Input offset voltage is guaranteed at 1 mV and is typically less than 200 μV. This allows the OP-275 to be used in many dc coupled or summing applications without the need for special selections or the added noise of additional offset adjustment circuitry.

The output is capable of driving 600 Ω loads to 10 V rms while maintaining low distortion. THD + Noise at 3 V rms is a low 0.0006%.

The OP-275 is specified over the extended industrial (−40°C to +85°C) temperature range. OP-275s are available in both plastic DIP and SOIC-8 packages. SOIC-8 packages are available in 2500 piece reels. Many audio amplifiers are not offered in SOIC-8 surface mount packages for a variety of reasons, however the OP-275 was designed so that it would offer full performance in surface mount packaging.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
THD + Noise		V_{IN} = 3 V rms, R_L = 2 kΩ, f = 1 kHz		0.0006		%
Voltage Noise Density	e_n	f = 30 Hz		7		$nV/\sqrt{Hz}$
		f = 1 kHz		6		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		1.5		$pA/\sqrt{Hz}$
Headroom		THD + Noise ≤ 0.01%, R_L = 2 kΩ, V_S = ±18 V		>12.9		dBu
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				1	mV
		−40°C≤T_A≤+85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 0 V		100	350	nA
		V_{CM} = 0 V, −40°C≤T_A≤+85°C		100	400	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		2	±50	nA
		V_{CM} = 0 V, −40°C≤T_A≤+85°C		2	±100	nA
Input Voltage Range	V_{CM}		−10.5		+10.5	V
Common-Mode Rejection	CMR	V_{CM} = ±10.5 V, −40°C≤T_A≤+85°C	80	106		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	250			V/mV
		R_L = 2 kΩ, −40°C≤T_A≤+85°C	175			V/mV
		R_L = 600 Ω		200		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ	−13.5	±13.9	+13.5	V
		R_L = 2 kΩ, −40°C≤T_A≤+85°C	−13	±13.9	+13	V
		R_L = 600 Ω, V_S = ±18 V		±16		V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	85	111		dB
		V_S = ±4.5 V to ±18 V, −40°C≤T_A≤+85°C	80			dB
Supply Current	I_{SY}	V_S = ±4.5 V to ±18 V, V_O = 0 V, R_L = ∞, −40°C≤T_A≤+85°C		4	5	mA
		V_S = ±22 V, V_O = 0 V, R_L = ∞, −40°C≤T_A≤+85°C			5.5	mA
Supply Voltage Range	V_S		±4.5		±22	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	15	22		V/µs
Full-Power Bandwidth	BW_P					kHz
Gain Bandwidth Product	GBP			9		MHz
Phase Margin	∅o			62		Degrees
Overshoot Factor		V_{IN} = 100 mV, A_V = +1, R_L = 600 Ω, C_L = 100 pF		10		%

Specifications subject to change without notice.

9

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		1	mV max
Input Bias Current	I_B	V_{CM} = 0 V	350	nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	±50	nA max
Input Voltage Range[1]			±10.5	V min
Common-Mode Rejection	CMRR	V_{CM} = ±10.5 V	80	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	85	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	250	V/mV min
Output Voltage Range	V_O	R_L = 10 kΩ	±13.5	V min
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞	5	mA max

NOTES

Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

[1]Guaranteed by CMR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±22 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±7.5 V
Output Short-Circuit Duration to GND[3] . . . . . Indefinite
Storage Temperature Range
(P, S) Package . . . . . −65°C to +150°C
Operating Temperature Range
OP-275G . . . . . −40°C to +85°C
Junction Temperature Range
(P, S) Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[4]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES

[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

[2]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

[3]Shorts to either supply may destroy the device. See data sheet for full details.

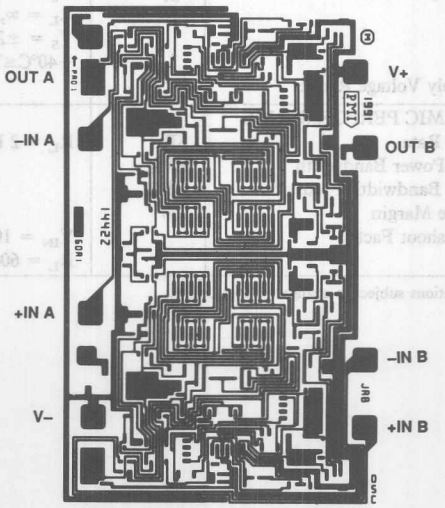
[4]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP275GP	−40°C to +85°C	8-Pin Plastic DIP	N-8
OP275GS	−40°C to +85°C	8-Pin SOIC	SO-8
OP275GSR	−40°C to +85°C	SOIC-8 Reel, 2500 pcs.	
OP275GBC	+25°C	DICE	

*For outline information see Package Information section.

DICE CHARACTERISTICS



OP-275 Die Size 0.070 × 0.108 in. (7,560 sq. mils)

The OP-275 has been designed with inherent output short circuit protection to ground.

However shorts to either supply may destroy the device when excessive voltages or currents are applied. For safe operation the output current of the OP-275 should be design limited to ±30 mA.

Total Harmonic Distortion

Total Harmonic Distortion + Noise (THD + N) of the OP-275 is well below 0.001% with any load down to 600 Ω. However, this is dependent upon the peak output swing. In Figure 1 it is seen that the THD + Noise with 3 V rms output is below 0.001%. In the following Figure 2, THD + Noise is below 0.001% for the 10 kΩ and 2 kΩ loads but increases to above 0.1% for the 600 Ω load condition. This is a result of the output swing capability of the OP-275. Notice the results in Figure 3, showing THD vs. V_{IN} (V rms). This figure shows that the THD + Noise remains very low until the output reaches 9.5 volts rms. This performance is similar to competitive products.

The output of the OP-275 is designed to maintain low harmonic distortion while driving 600 Ω loads. However, driving 600 Ω loads with very high output swings results in higher distortion if clipping occurs. A common example of this is in attempting to drive 10 V rms into any load with ±15 volt supplies. Clipping will occur and distortion will be very high.

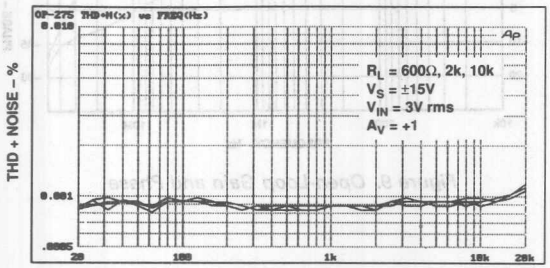


Figure 1. THD + Noise vs. Frequency vs. R_{LOAD}

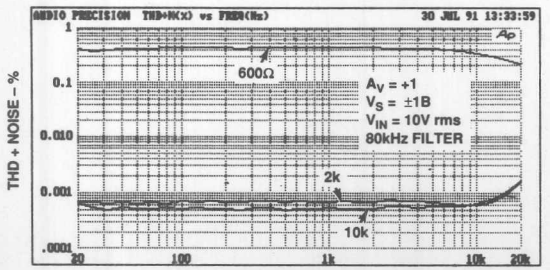


Figure 2. THD + Noise vs. R_{LOAD}; V_{IN} = 10 V rms, ±18 V Supplies

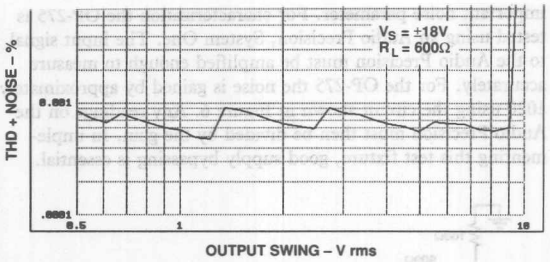


Figure 3. Headroom, THD + Noise vs. Output Amplitude (V rms); R_{LOAD} = 600 Ω, V_{SUP} = ±18 V

To attain low harmonic distortion with large output swings, supply voltages may be increased. Figure 4 shows the performance of the OP-275 driving 600 Ω loads with supply voltages varying from ±18 to ±20 volts. Notice that with ±18 volt supplies the distortion is fairly high, while with ±20 volt supplies it is a very low 0.0007%.

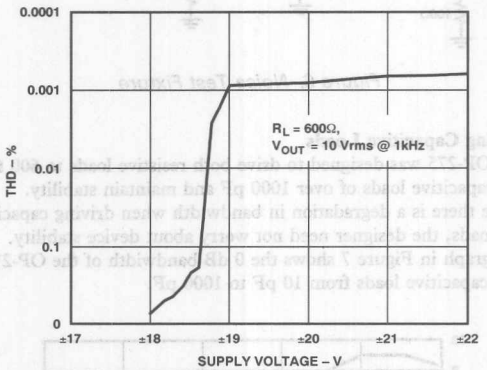


Figure 4. THD + Noise vs. Supply Voltage

Noise

The voltage noise density of the OP-275 is below 7 nV/$\sqrt{\text{Hz}}$ from 30 Hz. This enables low noise designs to have good performance throughout the full audio range. Figure 5 shows a typical OP-275 with a 1/f corner at 5.2 Hz.

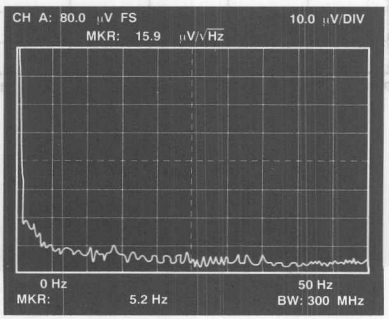


Figure 5. 1/f Noise Corner, V_s = ±15 V, A_V = 1000

Noise Testing

For audio applications the noise density is usually the most important noise parameter. For characterization the OP-275 is tested using an Audio Precision, System One. The input signal to the Audio Precision must be amplified enough to measure accurately. For the OP-275 the noise is gained by approximately 1020 using the circuit shown in Figure 6. Any readings on the Audio Precision must then be divided by the gain. In implementing this test fixture, good supply bypassing is essential.

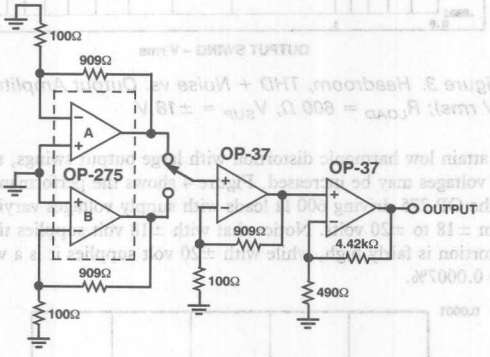


Figure 6. Noise Test Fixture

Driving Capacitive Loads

The OP-275 was designed to drive both resistive loads to 600 Ω and capacitive loads of over 1000 pF and maintain stability. While there is a degradation in bandwidth when driving capacitive loads, the designer need not worry about device stability. The graph in Figure 7 shows the 0 dB bandwidth of the OP-275 with capacitive loads from 10 pF to 1000 pF.

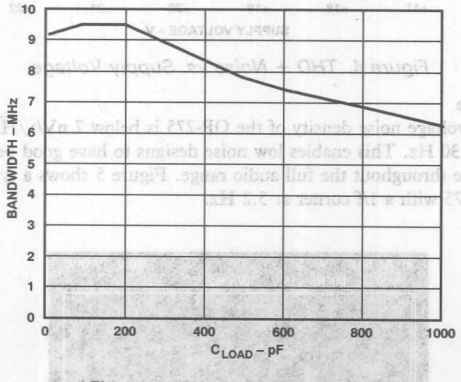


Figure 7. Bandwidth vs. C_{LOAD}

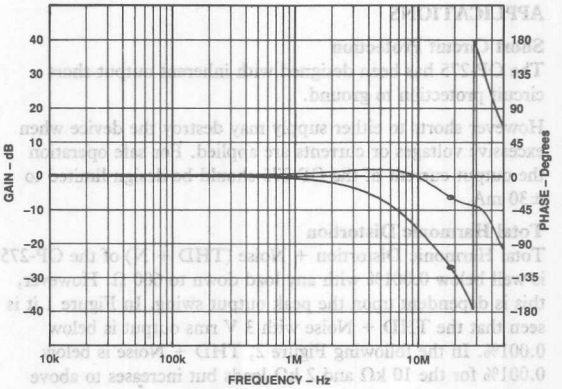


Figure 8. Closed-Loop Gain and Phase, $A_V = +1$

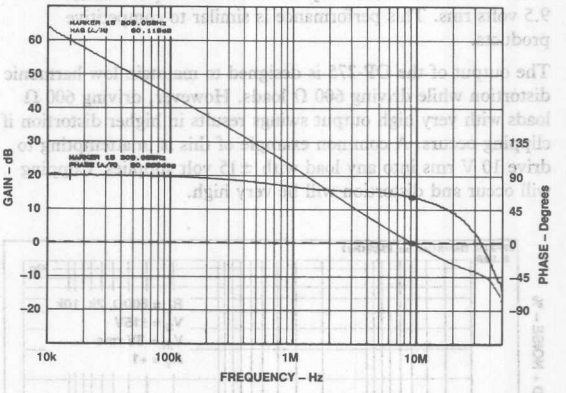


Figure 9. Open-Loop Gain and Phase

Rail-to-Rail Multimedia Operational Amplifier

OP279

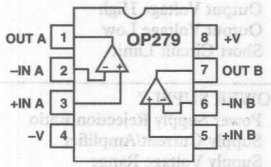
FEATURES
Rail-to-Rail Input and Output
High Output Current: 50 mA
Single-Supply: +5 V to +12 V
Wide Bandwidth: 2 MHz
High Slew Rate: 5 V/μs
Low Distortion: 0.01%
Unity Gain Stable
No Phase Reversal

APPLICATIONS
Multimedia
Telecom
DAA Transformer Driver
LCD Driver
Low Voltage Servo Control

FUNCTIONAL BLOCK DIAGRAMS

8-Lead Narrow-Body SO (S Suffix)

8-Lead Epoxy Dip (P Suffix)



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GENERAL DESCRIPTION

The OP279 is a dual, single-supply, high output current amplifier. It is designed for applications that require drive currents of up to 80 mA in low voltage applications.

Driving headphones directly or transformers or power transistors are applications that benefit from the OP279's high output current. The powerful output is combined with a unique input stage that maintains very low distortion with wide common-mode range even in single supply designs.

OP279s are useful amplifiers for buffering either ASICs or DACs when greater drive capability is needed than can usually be provided by CMOS outputs.

Bandwidth is 2 MHz and slew the rate is 5 V/μs, making these amplifiers well suited for single supply applications that require audio bandwidths when used in high gain configurations. Operation is guaranteed from voltages as low as 4.5 V, up to 12 V.

When using the OP279 in +5 V systems, very good audio performance can be attained. THD is below 0.01% with a 600 Ω load, and noise is a respectable 22 nV/√Hz. Supply current is less than 2 mA per amplifier.

The OP279 is available in 8-pin plastic DIP and SO-8 surface mount packages. They are specified over the extended industrial (–40°C to +85°C) temperature range.

PRELIMINARY TECHNICAL DATA

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

OP279–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, V_{CM} = 2.5 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{OUT} = 2.5 V			4	mV
Input Bias Current	I_B	V_{OUT} = 2.5 V		350	600	nA
Input Offset Current	I_{OS}	V_{OUT} = 2.5 V			±50	nA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V				
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.2 V ≤ V_O ≤ 3.8 V	100			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA Source	+4.9			V
Output Voltage Low	V_{OL}	I_L = 10 mA Sink		50	100	mV
Short Circuit Limit	I_{SC}	Source	50	80		mA
		Sink	50	80		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +4.75 V to +12 V	70	104		dB
Supply Current/Amplifier	I_{SY}	V_O = 2.5 V		2	2.5	mA
Supply Voltage Range	V_S		+4.75		±6	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		5		V/µs
Full-Power Bandwidth	BW_P	1% Distortion				kHz
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	ϕo			46		Degrees
AUDIO PERFORMANCE						
Total Harmonic Distortion	THD			0.01		%
Voltage Noise Density	e_n	f = 1 kHz		22		nV/√Hz

ELECTRICAL CHARACTERISTICS (@ V_S = ±5.0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				4	mV
Input Bias Current	I_B			400	600	nA
Input Offset Current	I_{OS}				±50	nA
Input Voltage Range			–5		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –5 V to +5 V	70	86		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	100	1000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			–1.6		nA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA Source	+4.9			V
Output Voltage Low	V_{OL}	I_L = 10 mA Sink			–4.9	V
Short Circuit Limit	I_{SC}	Source		80		mA
		Sink		80		mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		15		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±6 V, –40 ≤ T_A ≤ +85°C	70	25		dB
Supply Current/Amplifier	I_{SY}	V_S = ±6 V, V_O = 0 V		2	2.6	mA
Supply Voltage Range	V_S		+4.75		±6	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		5		V/µs
Full-Power Bandwidth	BW_P	1% Distortion				kHz
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	ϕo					Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		22		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Dual/Quad Low Power, High Speed JFET Operational Amplifiers

OP282/OP482

FEATURES

- High Slew Rate: 9 V/μs
- Wide Bandwidth: 4 MHz
- Low Supply Current: 250 μA/Amplifier
- Low Offset Voltage: 3 mV
- Low Bias Current: 100 pA
- Fast Settling Time
- Common-Mode Range Includes V+
- Unity Gain Stable

APPLICATIONS

- Active Filters
- Fast Amplifiers
- Integrators
- Supply Current Monitoring

GENERAL DESCRIPTION

The OP-282/OP-482 dual and quad operational amplifiers feature excellent speed at exceptionally low supply currents. Slew rate exceeds 7 V/μs with supply current under 250 μA per amplifier. These unity gain stable amplifiers have a typical gain-bandwidth of 4 MHz.

The JFET input stage of the OP-282/OP-482 insures bias current is typically a few picoamps and below 500 pA over the full temperature range. Offset voltage is under 3 mV for the dual and under 4 mV for the quad.

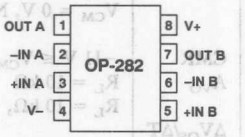
With a wide output swing, within 1.5 volts of each supply, low power consumption and high slew rate, the OP-282/OP-482 are ideal for battery-powered systems or power restricted applications. An input common-mode range that includes the positive supply makes the OP-282/OP-482 an excellent choice for high-side signal conditioning.

The OP-282/OP-482 are specified over the extended industrial temperature range. Both dual and quad amplifiers are available in plastic and ceramic DIP plus SOIC surface mount packages.

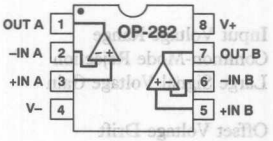
Contact your local sales office for MIL-STD-883 data sheet and availability.

PIN CONNECTIONS

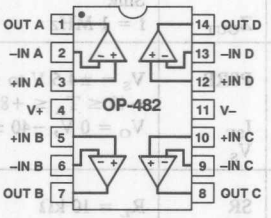
8-Lead Narrow-Body SOIC (S Suffix)



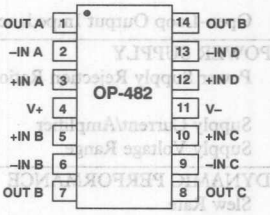
8-Lead Epoxy DIP (P Suffix)



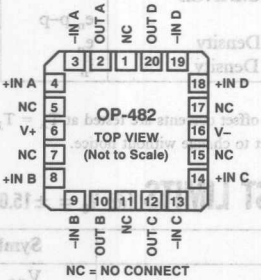
14-Lead Epoxy DIP (P Suffix)



14-Lead Narrow-Body SOIC (S Suffix)



20-Position Chip Carrier (RC Suffix)



NC = NO CONNECT

9

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP-282		0.2	3	mV
		OP-282, $-40 \le T_A \le +85°C$			4.5	mV
Offset Voltage	V_{OS}	OP-482		0.2	4	mV
		OP-482, $-40 \le T_A \le +85°C$			6	mV
Input Bias Current	I_B	$V_{CM} = 0$ V		3	100	pA
		$V_{CM} = 0$ V, Note 1			500	pA
Input Offset Current	I_{OS}	$V_{CM} = 0$ V		1	50	pA
		$V_{CM} = 0$ V, Note 1			250	pA
Input Voltage Range			−11		+15	V
Common-Mode Rejection	CMR	-11 V $\le V_{CM} \le +15$ V, $-40 \le T_A \le +85°C$	70	90		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10$ kΩ	20			V/mV
		$R_L = 10$ kΩ, $-40 \le T_A \le +85°C$	15			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		μV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			8		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	$R_L = 10$ kΩ	−13.5	±13.9	13.5	V
Short Circuit Limit	I_{SC}	Source	3	10		mA
		Sink	−8	−12		mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5$ V to ±18 V,				
		$-40 \le T_A \le +85°C$		25	316	μV/V
Supply Current/Amplifier	I_{SY}	$V_O = 0$ V, $-40 \le T_A \le +85°C$		210	250	μA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10$ kΩ	7	9		V/μs
Full-Power Bandwidth	BW_P	1% Distortion		125		kHz
Settling Time	t_S	To 0.01%		1.6		μs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	∅o			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p–p	0.1 Hz to 10 Hz		1.3		μVp–p
Voltage Noise Density	e_n	f = 1 kHz		36		nV/√Hz
Current Noise Density	i_n			0.01		pA/√Hz

NOTE

[1]The input bias and offset currents are tested at $T_A = T_J = +85°C$. Bias and offset currents are guaranteed but not tested at −40°C.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ $V_S = \pm15.0$ V, $T_A = +25°C$ unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}	OP-282	3	mV max
Offset Voltage	V_{OS}	OP-482	4	mV max
Input Bias Current	I_B	$V_{CM} = 0$ V	100	pA max
Input Offset Current	I_{OS}	$V_{CM} = 0$ V	50	pA max
Input Voltage Range[1]			−11, +15	V min/max
Common-Mode Rejection	CMRR	-11 V $\le V_{CM} \le +15$ V	70	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	316	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L = 10$ kΩ	20	V/mV min
Output Voltage Range	V_O	$R_L = 10$ kΩ	±13.5	V min
Supply Current/Amplifier	I_{SY}	$V_O = 0$ V, $R_L = \infty$	250	μA max

NOTES

Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

[1]Guaranteed by CMR test.

Specifications subject to change without notice.

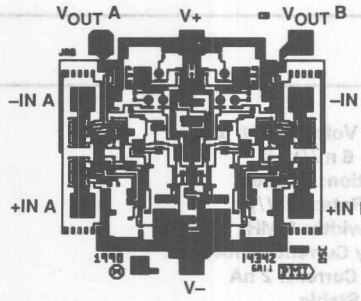
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . 36 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
  Y, Z, RC Packages . . . . . −65°C to +175°C
  P, S Packages . . . . . −65°C to +150°C
Operating Temperature Range
  OP-282A, OP-482A . . . . . −55°C to +125°C
  OP-282G, OP-482G . . . . . −40°C to +85°C
Junction Temperature Range
  Y, Z, RC Packages . . . . . −65°C to +125°C
  P, S Packages . . . . . −65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

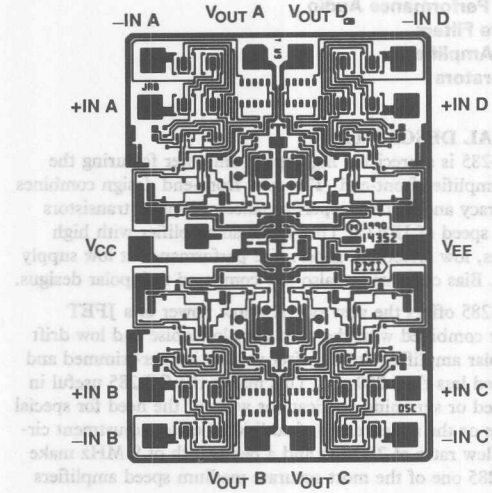
Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Cerdip (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SOIC (S)	120	36	°C/W
20-Contact LCC (RC)	98	38	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

DICE CHARACTERISTICS



OP-282 Die Size 0.063 × 0.060 Inch, 3,780 Sq. Mils



OP-482 Die Size 0.070 × 0.098 Inch, 6,860 Sq. Mils

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP282AZ/883	−55°C to +125°C	8-Pin Cerdip	Q-8
OP482AY/883	−55°C to +125°C	14-Pin Cerdip	Q-14
OP482ARC/883	−55°C to +125°C	20-Contact LCC	E-20A
OP282GP	−40°C to +85°C	8-Pin Plastic DIP	N-8
OP282GS	−40°C to +85°C	8-Pin SOIC	SO-8
OP482GP	−40°C to +85°C	14-Pin Plastic DIP	N-14
OP482GS	−40°C to +85°C	14-Pin SOIC	SO-14
OP282GBC	+25°C	DICE	
OP482GBC	+25°C	DICE	

*For outline information see Package Information section.

Dual, 9 MHz Precision Operational Amplifier

OP285*

FEATURES
Low Offset Voltage: 250 μV
Low Noise: 6 nV/√Hz
Low Distortion: 0.0006%
High Slew Rate: 22 V/μs
Wide Bandwidth: 9 MHz
Low Supply Current: 5 mA
Low Offset Current: 2 nA
Unity-Gain Stable
SO-8 Package

APPLICATIONS
High Performance Audio
Active Filters
Fast Amplifiers
Integrators

GENERAL DESCRIPTION

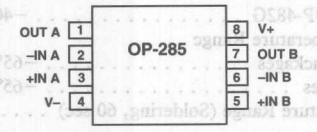
The OP-285 is a precision high speed amplifier featuring the Butler Amplifier front-end. This new front-end design combines the accuracy and low noise performance of bipolar transistors with the speed of JFETs. This yields an amplifier with high slew rates, low offset and good noise performance at low supply currents. Bias currents are also low compared to bipolar designs.

The OP-285 offers the slew rate and low power of a JFET amplifier combined with the precision, low noise and low drift of a bipolar amplifier. Input offset voltage is laser-trimmed and guaranteed less than 250 μV. This makes the OP-285 useful in dc coupled or summing applications without the need for special selections or the added noise of additional offset adjustment circuitry. Slew rates of 22 V/μs and a bandwidth of 9 MHz make the OP-285 one of the most accurate medium speed amplifiers available.

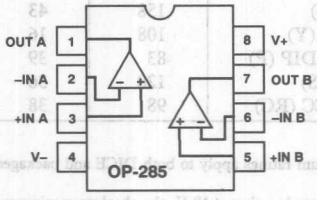
*Patents pending.

PIN CONNECTIONS

8-Lead Narrow-Body SO
(S Suffix)



8-Lead Epoxy DIP
(P Suffix)



The combination of low noise, speed and accuracy can be used to build high speed instrumentation systems. Circuits such as instrumentation amplifiers, ramp generators, bi-quad filters and dc coupled audio systems are all practical with the OP-285.

For applications that require long term stability, the OP-285 has a guaranteed maximum long term drift specification.

The OP-285 is specified over the XIND—extended industrial—(−40°C to +85°C) temperature range. OP-285s are available in 8-pin plastic DIP and SOIC-8 surface mount packages.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			35	250	μV
Offset Voltage	V_{OS}	−40°C ≤ T_A ≤ +85°C			600	μV
Input Bias Current	I_B	V_{CM} = 0 V		100	350	nA
Input Bias Current	I_B	V_{CM} = 0 V, −40°C ≤ T_A ≤ +85°C			400	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		2	±50	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V, −40°C ≤ T_A ≤ +85°C		2	±100	nA
Input Voltage Range	V_{CM}		−10.5		+10.5	V
Common-Mode Rejection	CMRR	V_{CM} = ±10.5 V, −40°C ≤ T_A ≤ +85°C	80	106		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	250			V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, −40°C ≤ T_A ≤ +85°C	175			V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 600 Ω		200		V/mV
Common-Mode Input Capacitance				7.5		pF
Differential Input Capacitance				3.7		pF
Long Term Offset Voltage	ΔV_{OS}	Note 1			300	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ	−13.5	±13.9	+13.5	V
Output Voltage Swing	V_O	R_L = 2 kΩ, −40°C ≤ T_A ≤ +85°C	−13	±13.9	+13	V
		R_L = 600 Ω, V_S = ±18 V		−16/+14		V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	85	111		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V, −40°C ≤ T_A ≤ +85°C	80			dB
Supply Current	I_{SY}	V_S = ±4.5 V to ±18 V, V_O = 0 V, R_L = ∞, −40°C ≤ T_A ≤ +85°C		4	5	mA
Supply Current	I_{SY}	V_S = ±22 V, V_O = 0 V, R_L = ∞, −40°C ≤ T_A ≤ +85°C			5.5	mA
Supply Voltage Range	VS		±4.5		±22	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	15	22		V/μs
Gain Bandwidth Product	GBP			9		MHz
Phase Margin	θo			62		Degrees
Settling Time	t_S	To 0.1%, 10 V Step		625		ns
Settling Time	t_S	To 0.01%, 10 V Step		750		ns
Distortion		A_V = +1, V_{OUT} = 8.5 V p-p, f = 1 kHz, R_L = 2 kΩ		−104		dB
Voltage Noise Density	e_n	f = 30 Hz		7		$nV/\sqrt{Hz}$
Voltage Noise Density	e_n	f = 1 kHz		6		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		0.9		$pA/\sqrt{Hz}$
Headroom		THD + Noise ≤ 0.01%, R_L = 2 kΩ, V_S = ±18 V		>12.9		dBu

NOTE

[1]Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent wafer lots at +125°C, with an LTPD of 1.3.

Specifications subject to change without notice.

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WAFER TEST LIMITS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		250	µV max
Input Bias Current	I_B	V_{CM} = 0 V	350	nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	±50	nA max
Input Voltage Range[1]	V_{CM}		±10.5	V min
Common-Mode Rejection	CMRR	V_{CM} = ±10.5 V	80	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	85	dB
Large Signal Voltage Gain	A_{V_O}	R_L = 2 kΩ	250	V/mV min
Output Voltage Range	V_O	R_L = 2 kΩ	13	V min
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞	5	mA max

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.

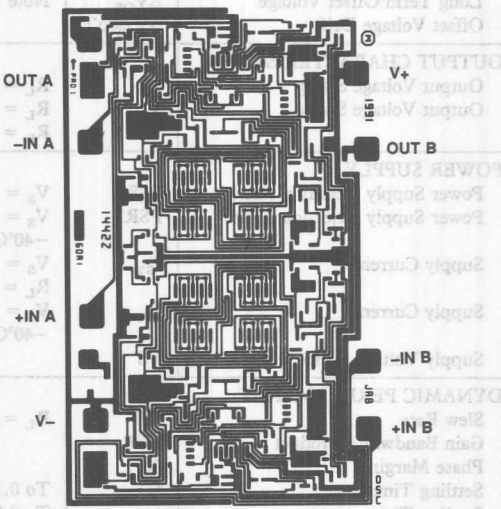
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±22 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±7.5 V
Output Short-Circuit Duration to Gnd[3] . . . . . Indefinite
Storage Temperature Range
P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
OP-285G . . . . . −40°C to +85°C
Junction Temperature Range
P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec) . . . . . +300°C

Package Type	θ_{JA}[4]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±7.5 V, the absolute maximum input voltage is equal to the supply voltage.
[3]Shorts to either supply may destroy the device. See data sheet for full details.
[4]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

DICE CHARACTERISTICS



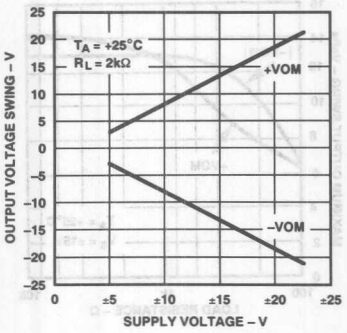
OP-285 Die Size 0.070 × 0.108 inch, 7,560 sq. mils

Substrate (Die Backside) Is Connected to V–
Transistor Count, 45

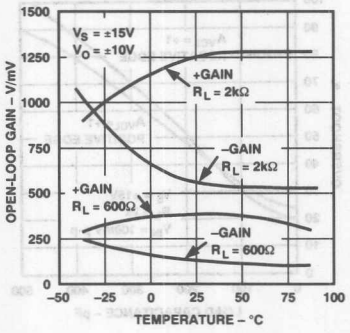
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP285GP	−40°C to +85°C	8-Pin Plastic DIP	N-8
OP285GS	−40°C to +85°C	8-Pin SOIC	SO-8
OP285GSR	−40°C to +85°C	SO-8 Reel, 2500 pcs.	
OP285GBC	+25°C	DICE	

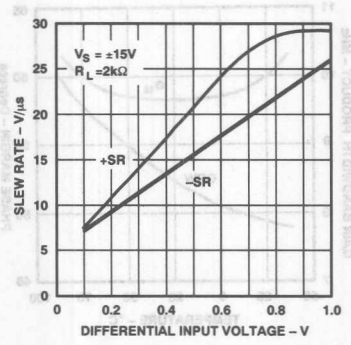
*For outline information see Package Information section.



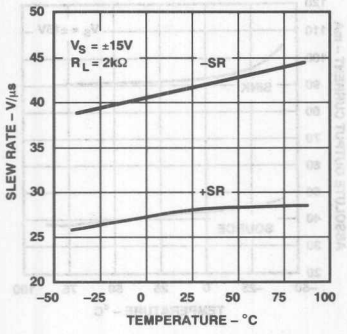
Output Voltage Swing vs. Supply Voltage



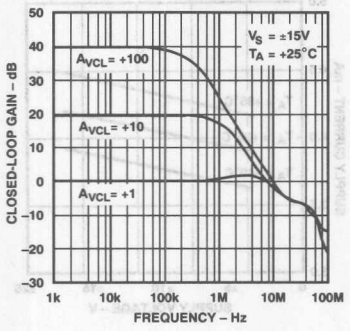
Open-Loop Gain vs. Temperature



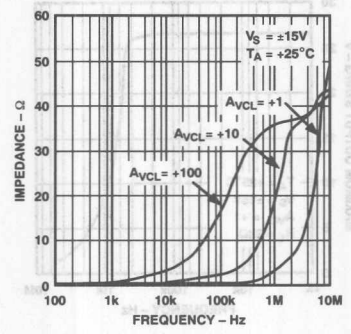
Slew Rate vs. Differential Input Voltage



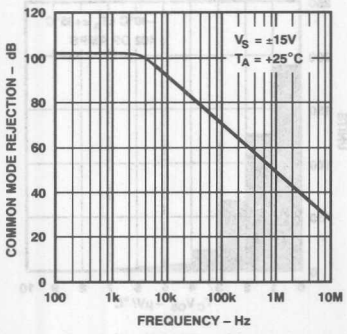
Slew Rate vs. Temperature



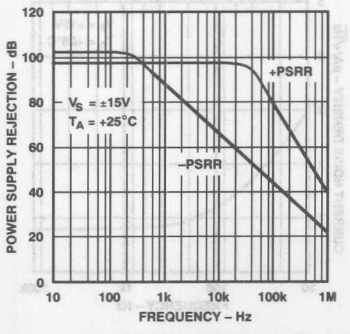
Closed-Loop Gain vs. Frequency



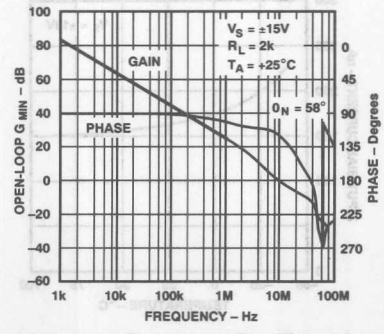
Closed-Loop Output Impedance vs. Frequency



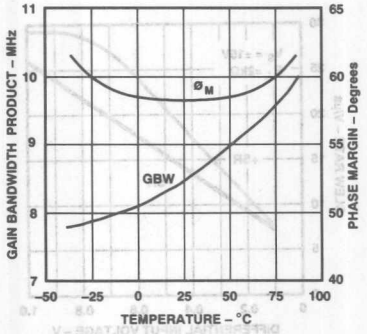
Common-Mode Rejection vs. Frequency



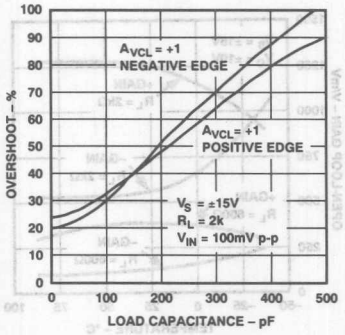
Power Supply Rejection vs. Frequency



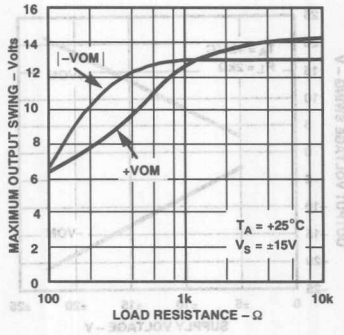
Open-Loop Gain, Phase vs. Frequency



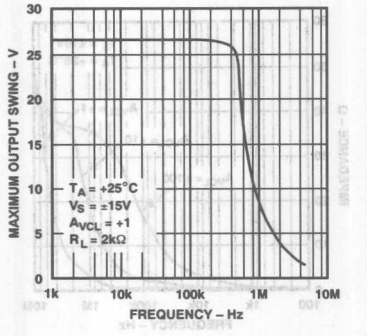
Gain Bandwidth Product, Phase Margin vs. Temperature



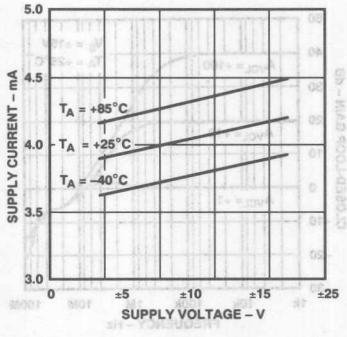
Small-Signal Overshoot vs. Load Capacitance



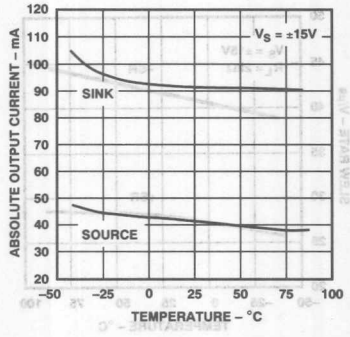
Maximum Output Voltage vs. Load Resistance



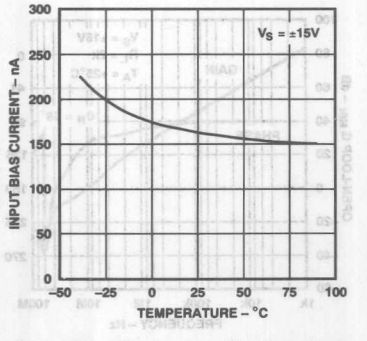
Maximum Output Swing vs. Frequency



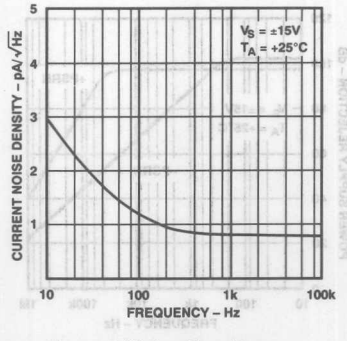
Supply Current vs. Supply Voltage



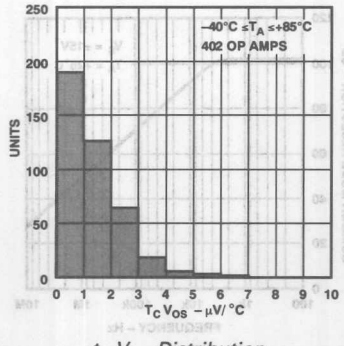
Short Circuit Current vs. Temperature



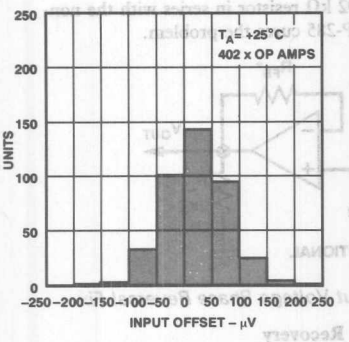
Input Bias Current vs. Temperature



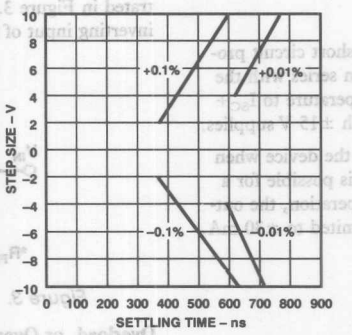
Current Noise Density vs. Frequency



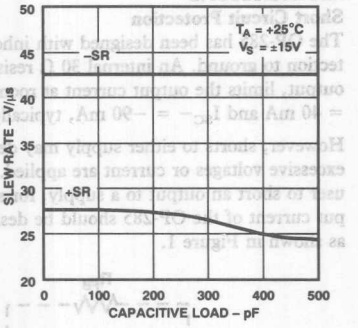
t_C V_{OS} Distribution



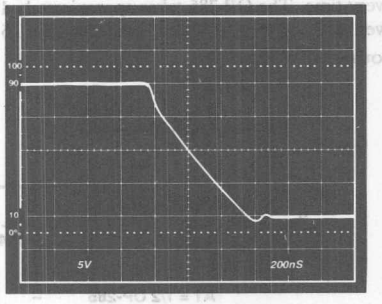
Input Offset (V_{OS}) Distribution



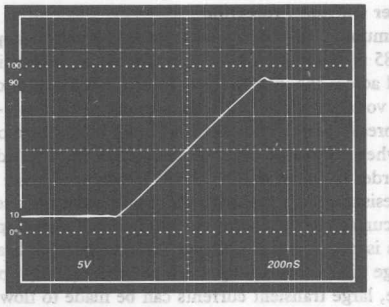
Settling Time vs. Step Size



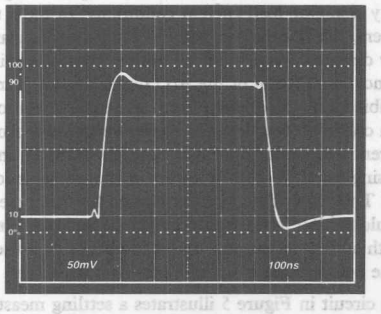
Slew Rate vs. Capacitive Load



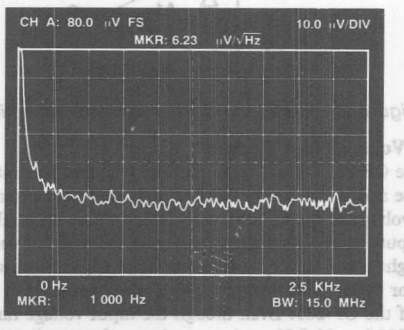
Negative Slew Rate
R_L = 2 kΩ, V_S = ±15 V, A_V = +1



Positive Slew Rate
R_L = 2 kΩ, V_S = ±15 V, A_V = +1



Small Signal Response
R_L = 2 kΩ, V_S = ±15 V, A_V = +1



OP-285 Voltage Noise Density vs. Frequency V_S = ±15 V, A_V = 1000

output, limits the output current at room temperature to $I_{SC}+$ = 40 mA and $I_{SC}-$ = −90 mA, typically, with ±15 V supplies.

However, shorts to either supply may destroy the device when excessive voltages or current are applied. If it is possible for a user to short an output to a supply, for safe operation, the output current of the OP-285 should be design-limited to ±30 mA, as shown in Figure 1.

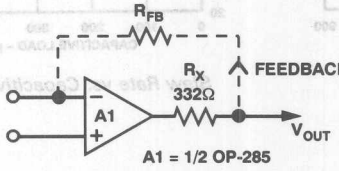


Figure 1. Recommended Output Short Circuit Protection

Input Over Current Protection

The maximum input differential voltage that can be applied to the OP-285 is determined by a pair of internal Zener diodes connected across the inputs. They limit the maximum differential input voltage to ±7.5 V. This is to prevent emitter-base junction breakdown from occurring in the input stage of the OP-285 when very large differential voltages are applied. However, in order to preserve the OP-285's low input noise voltage, internal resistance in series with the inputs were not used to limit the current in the clamp diodes. In small-signal applications, this is not an issue; however, in industrial applications, where large differential voltages can be inadvertently applied to the device, large transient currents can be made to flow through these diodes. The diodes have been designed to carry a current of ±8 mA; and, in applications where the OP-285's differential voltage were to exceed ±7.5 V, the resistor values shown in Figure 2 safely limit the diode current to ±8 mA.

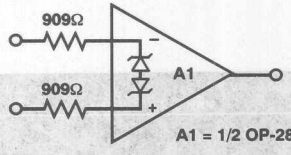


Figure 2. OP-285 Input Over Current Protection

Output Voltage Phase Reversal

Since the OP-285's input stage combines bipolar transistors for low noise and p-channel JFETs for high speed performance, the output voltage of the OP-285 may exhibit phase reversal if either of its inputs exceed its negative common-mode input voltage. This might occur in very severe industrial applications where a sensor, or system, fault might apply very large voltages on the inputs of the OP-285. Even though the input voltage range of the OP-285 is ±10.5 V, an input voltage of approximately −13.5 V will cause output voltage phase reversal. In inverting amplifier configurations, the OP-285's internal 7.5 V input clamping diodes will prevent phase reversal; however, they will not prevent this effect from occurring in noninverting applications. For these applications, the fix is a simple one and is illus-

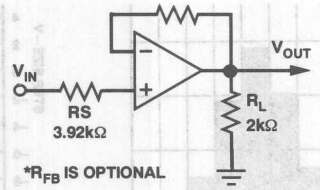


Figure 3. Output Voltage Phase Reversal Fix

Overload, or Overdrive, Recovery

Overload, or overdrive, recovery time of an operational amplifier is the time required for the output voltage to recover to a rated output voltage from a saturated condition. This recovery time is important in applications where the amplifier must recover quickly after a large abnormal transient event. The circuit shown in Figure 4 was used to evaluate the OP-285's overload recovery time. The OP-285 takes approximately 1.2 μs to recover to V_{OUT} = +10 V and approximately 1.5 μs to recover to V_{OUT} = −10 V.

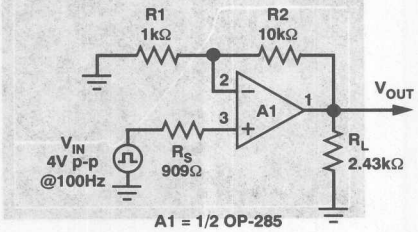


Figure 4. Overload Recovery Time Test Circuit

Driving the Analog Input of an A/D Converter

Settling characteristics of operational amplifiers also include the amplifier's ability to recover, i.e., settle, from a transient output current load condition. When driving the input of an A/D converter, especially successive-approximation converters, the amplifier must maintain a constant output voltage under dynamically changing load current conditions. In these types of converters, the comparison point is usually diode clamped, but it may deviate several hundred millivolts resulting in high frequency modulation of the A/D input current. Amplifiers that exhibit high closed-loop output impedances and/or low unity-gain crossover frequencies recover very slowly from output load current transients. This slow recovery leads to linearity errors or missing codes because of errors in the instantaneous input voltage. Therefore, the amplifier chosen for this type of application should exhibit low output impedance and high unity-gain bandwidth so that its output has had a chance to settle to its nominal value before the converter makes its comparison.

The circuit in Figure 5 illustrates a settling measurement circuit for evaluating the recovery time of an amplifier from an output load current transient. The amplifier is configured as a follower with a very high speed current generator connected to its output. In this test, a 1 mA transient current was used. As shown in Figure 6, the OP-285 exhibits an extremely fast recovery time of 139 ns to 0.01%. Because of its high gain-bandwidth product,

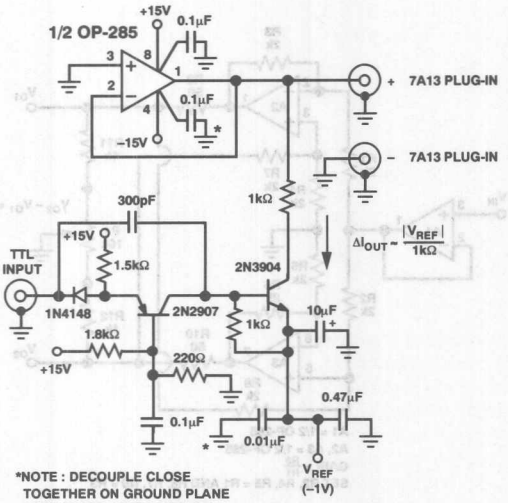


Figure 5. Transient Output Load Current Test Fixture

high open-loop gain, and low output impedance, the OP-285 is ideally suited to drive high speed A/D converters.

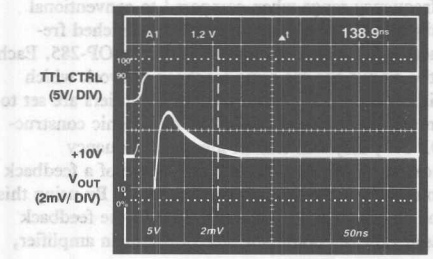


Figure 6. OP-285's Output Load Current Recovery Time

Measuring Settling Time

The design of OP-285 combines high slew rate and wide gain-bandwidth product to produce a fast-settling ($t_S < 1$ µs) amplifier for 8- and 12-bit applications. The test circuit designed to measure the settling time of the OP-285 is shown in Figure 7. This test method has advantages over false-sum node techniques in that the actual output of the amplifier is measured, instead of an error voltage at the sum node. Common-mode settling effects are exercised in this circuit in addition to the slew rate and bandwidth effects measured by the false-sum-node method. Of course, a reasonably flat-top pulse is required as the stimulus.

The output waveform of the OP-285 under test is clamped by Schottky diodes and buffered the JFET source follower. The signal is amplified by a factor of ten by the OP-260 and then Schottky-clamped at the output to prevent overloading the oscilloscope's input amplifier. The OP-41 is configured as a fast integrator which provides overall dc offset nulling.

High Speed Operation

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress, and component placement. Recommended circuit configurations for inverting and noninverting applications are shown in Figures 8 and Figure 9.

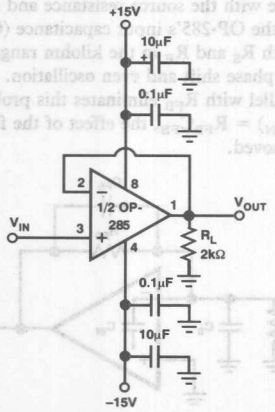


Figure 8. Unity Gain Follower

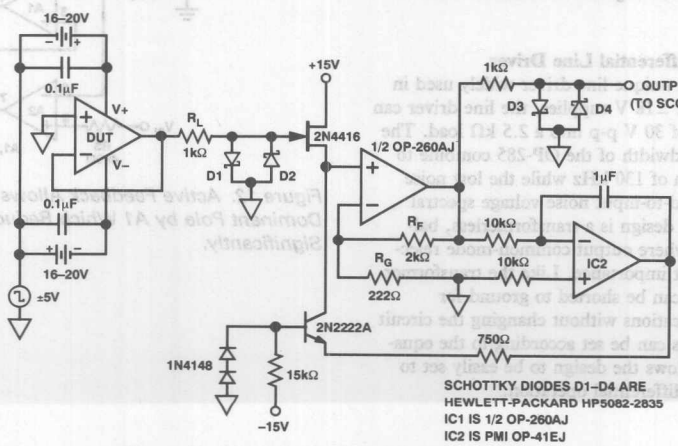


Figure 7. OP-285's Settling Time Test Fixture

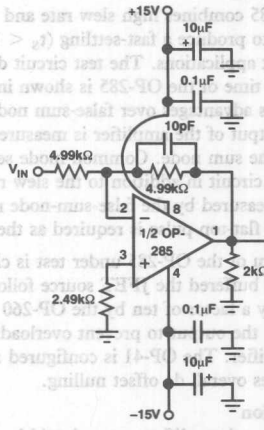


Figure 9. Unity Gain Inverter

In inverting and noninverting applications, the feedback resistance forms a pole with the source resistance and capacitance (R_S and C_S) and the OP-285's input capacitance (C_{IN}), as shown in Figure 10. With R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor, C_{FB}, in parallel with R_{FB} eliminates this problem. By setting R_S (C_S + C_{IN}) = $R_{FB}C_{FB}$, the effect of the feedback pole is completely removed.

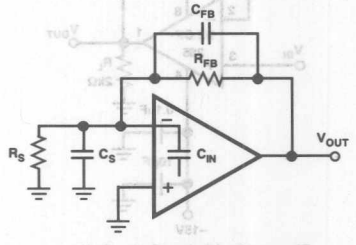


Figure 10. Compensating the Feedback Pole

High Speed, Low Noise Differential Line Driver

The circuit of Figure 11 is a unique line driver widely used in industrial applications. With ±18 V supplies, the line driver can deliver a differential signal of 30 V p-p into a 2.5 kΩ load. The high slew rate and wide bandwidth of the OP-285 combine to yield a full power bandwidth of 130 kHz while the low noise front end produces a referred-to-input noise voltage spectral density of 10 nV/$\sqrt{\text{Hz}}$. The design is a transformerless, balanced transmission system where output common-mode rejection of noise is of paramount importance. Like the transformer-based design, either output can be shorted to ground for unbalanced line driver applications without changing the circuit gain of 1. Other circuit gains can be set according to the equation in the diagram. This allows the design to be easily set to noninverting, inverting, or differential operation.

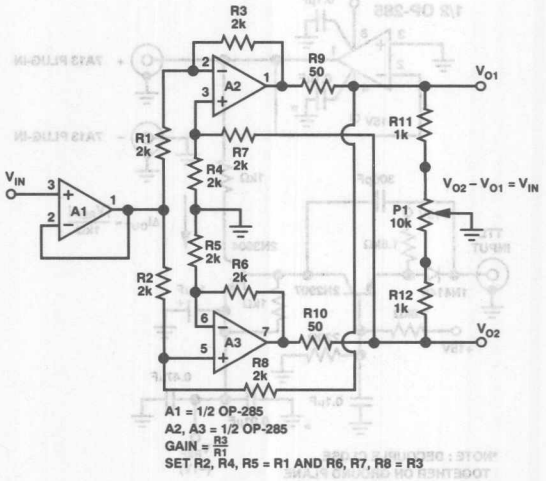


Figure 11. High Speed, Low Noise Differential Line Driver

Low Phase Error Amplifier

The simple amplifier configuration of Figure 12 utilizes the OP-285 and a few resistors to reduce phase error substantially over a wide frequency range when compared to conventional amplifier designs. This technique relies on the matched frequency characteristics of the two amplifiers in the OP-285. Each amplifier in the circuit has the same feedback network which produces a circuit gain of 10. Since the two amplifiers are set to the same gain and are matched due to the monolithic construction of the OP-285, they will exhibit identical frequency response. Recall from feedback theory that a pole of a feedback network becomes a zero in the loop gain response. By using this technique, the dominant pole of the amplifier in the feedback loop compensates for the dominant pole of the main amplifier,

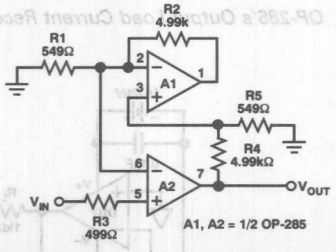


Figure 12. Active Feedback Allows Cancellation of A2's Dominant Pole by A1 Which Reduces the Phase Shift Significantly.

thereby reducing phase error dramatically. This is shown in Figure 13 where the 10× composite amplifier's phase response exhibits less than 1.5° phase shift through 500 kHz. On the other hand, the single gain stage amplifier exhibits 25 degrees of phase shift over the same frequency range. An additional benefit of the low phase error configuration is constant group delay, by virtue of constant phase shift at all frequencies below 500 kHz. Although this technique is valid for minimum circuit gains of 10, actual closed-loop magnitude response must be optimized for the amplifier chosen.

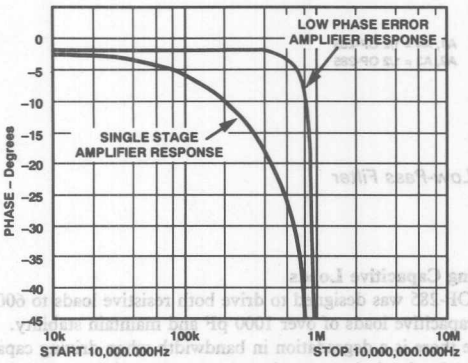


Figure 13. Phase Error Comparison

For a more detailed treatment on the design of low phase error amplifiers, please see Application Note AN-107.

Fast Current Pump

A fast, ±30 mA current source, illustrated in Figure 14, takes advantage of the OP-285's speed and high output current drive. This is a variation of the Howland current source where a second amplifier, A2, is used to increase load current accuracy and output voltage compliance. With supply voltages of ±15 V, the output voltage compliance of the current pump is ±8 V. To keep the output resistance in the MΩ range requires that 0.1% or better resistors be used in the circuit. The gain of the current pump can be easily changed according to the equations shown in the diagram.

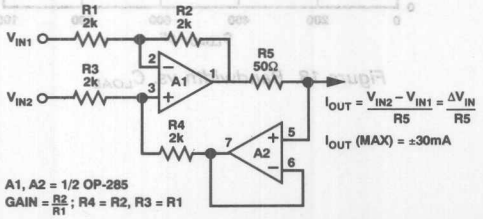


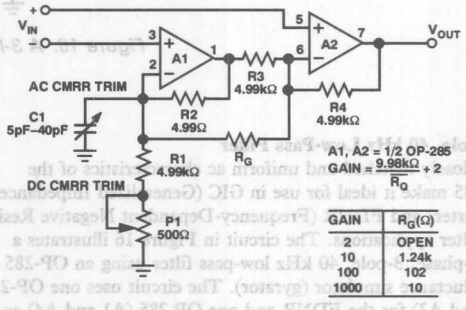
Figure 14. A Fast Current Pump

A Low Noise, High Speed Instrumentation Amplifier

A high speed, low noise instrumentation amplifier, constructed with a single OP-285, is illustrated in Figure 15. The circuit exhibits less than 1.2 μV p-p noise (RTI) in the 0.1 Hz to 10 Hz band and an input noise voltage spectral density of 9 nV/$\sqrt{Hz}$ (1 kHz) at a gain of 1000. The gain of the amplifier is easily set by R_G according to the formula:

$$\frac{V_{OUT}}{V_{IN}} = \frac{9.98\ k\Omega}{R_G} + 2$$

The advantages of a two op amp instrumentation amplifier based on a dual op amp is that the errors in the individual amplifiers tend to cancel one another. For example, the circuit's input offset voltage is determined by the input offset voltage matching of the OP-285, which is typically less than 250 μV.



GAIN	R_G(Ω)
2	OPEN
10	1.24k
100	102
1000	10

Figure 15. A High Speed Instrumentation Amplifier

Common-mode rejection of the circuit is limited by the matching of resistors R1 to R4. For good common-mode rejection, these resistors ought to be matched to better than 1%. The circuit was constructed with 1% resistors and included potentiometer P1 for trimming the DC CMRR and a capacitor C1 for trimming the AC CMRR. With these two trims, the circuit's common-mode rejection was better than 95 dB at 60 Hz and better than 65 dB at 10 kHz. For the best common-mode rejection performance, use a matched (better than 0.1%) thin-film resistor network for R1 through R4 and use the variable capacitor to optimize the circuit's AC CMR.

The instrumentation amplifier exhibits very wide small- and large-signal bandwidths regardless of the gain setting, as shown in the table. Because of its low noise, wide gain-bandwidth product, and high slew rate, the OP-285 is ideally suited for high speed signal conditioning applications.

Circuit Gain	R_G (Ω)	Circuit Bandwidth V_{OUT} = 100 mV p-p	Circuit Bandwidth V_{OUT} = 20 V p-p
2	Open	5 MHz	780 kHz
10	1.24 k	1 MHz	460 kHz
100	102	90 kHz	85 kHz
1000	10	10 kHz	10 kHz

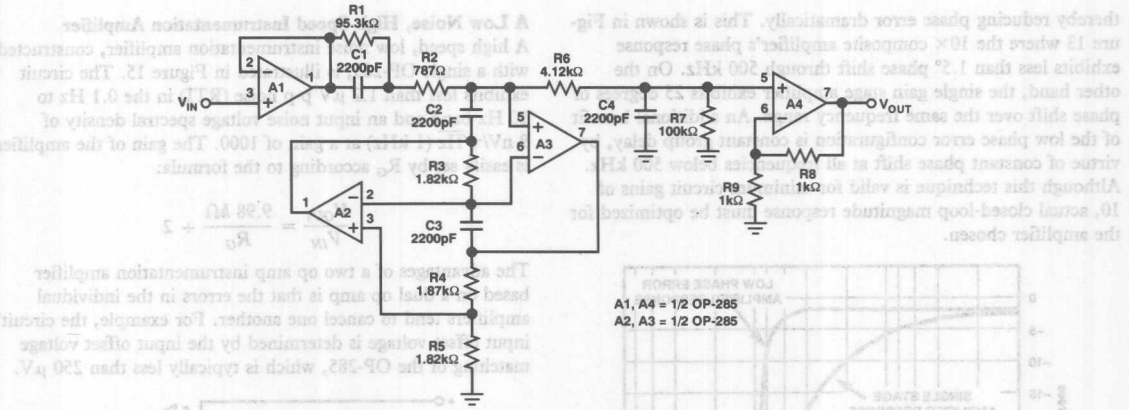


Figure 16. A 3-Pole, 40 kHz Low-Pass Filter

A 3-Pole, 40 kHz Low-Pass Filter

The closely matched and uniform ac characteristics of the OP-285 make it ideal for use in GIC (Generalized Impedance Converter) and FDNR (Frequency-Dependent Negative Resistor) filter applications. The circuit in Figure 16 illustrates a linear-phase, 3-pole, 40 kHz low-pass filter using an OP-285 as an inductance simulator (gyrator). The circuit uses one OP-285 (A2 and A3) for the FDNR and one OP-285 (A1 and A4) as an input buffer and bias current source for A3. Amplifier A4 is configured in a gain of 2 to set the pass band magnitude response to 0 dB. The benefits of this filter topology over classical approaches are that the op amp used in the FDNR is not in the signal path and that the filter's performance is relatively insensitive to component variations. Also, the configuration is such that large signal levels can be handled without overloading any of the filter's internal nodes. As shown in Figure 17, the OP-285's symmetric slew rate and low distortion produce a clean, well-behaved transient response.

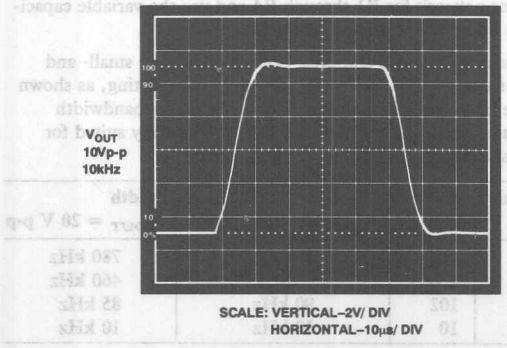


Figure 17. Low-Pass Filter Transient Response

Driving Capacitive Loads

The OP-285 was designed to drive both resistive loads to 600 Ω and capacitive loads of over 1000 pF and maintain stability. While there is a degradation in bandwidth when driving capacitive loads, the designer need not worry about device stability. The graph in Figure 18 shows the 0 dB bandwidth of the OP-285 with capacitive loads from 10 pF to 1000 pF.

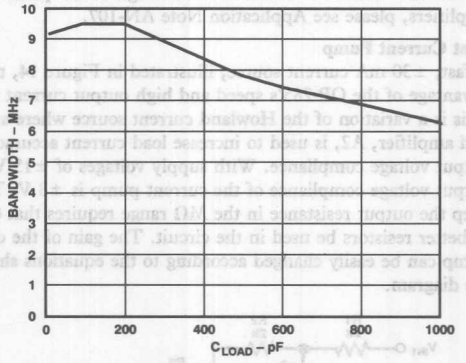
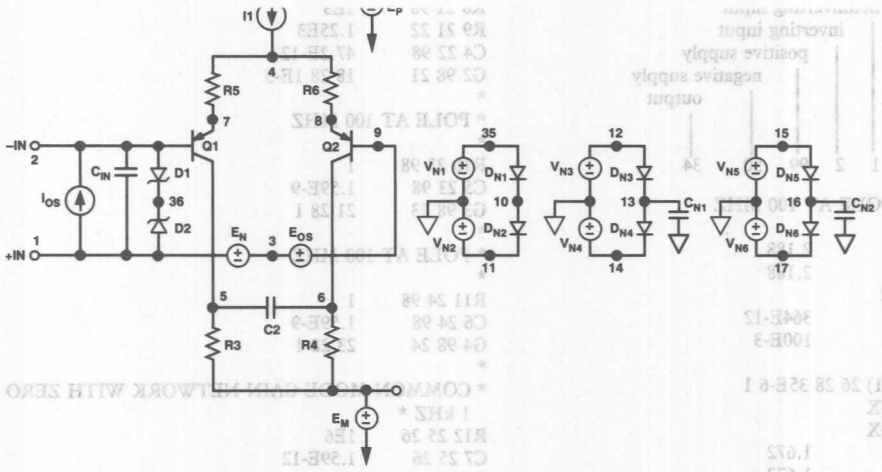


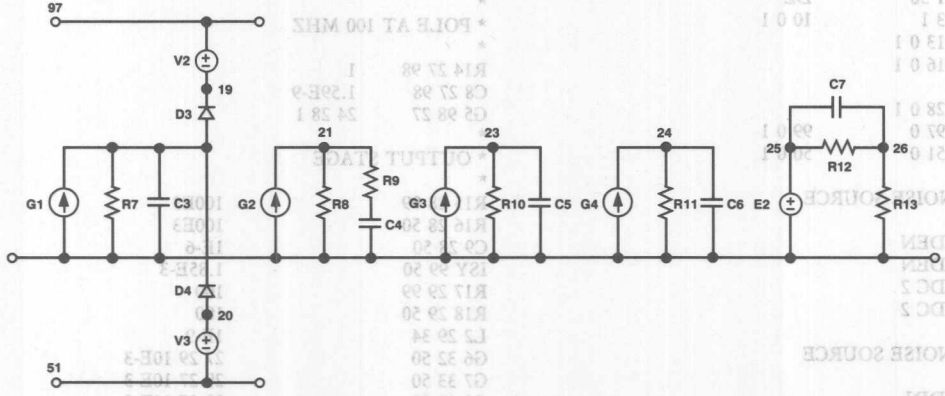
Figure 18. Bandwidth vs. C_{LOAD}

OP-285 SPICE Model

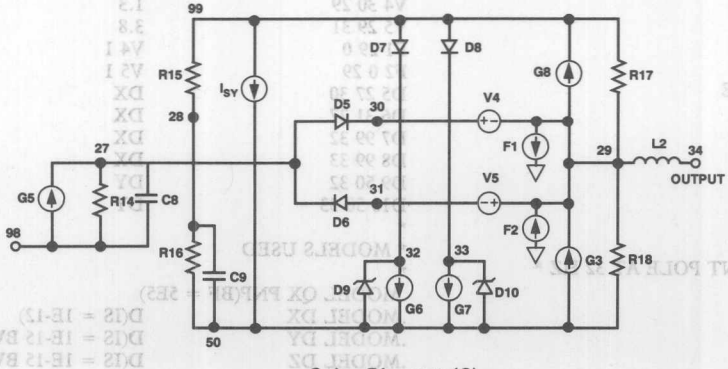
```
* Node assignments
*                        noninverting input
*                        |  inverting input
*                        |  |  positive supply
*                        |  |  |  negative supply
*                        |  |  |  |  output
*                        |  |  |  |  |
*                        |  |  |  |  |
.SUBCKT OP-285           1  2  99 50 34
*
* INPUT STAGE & POLE AT 100 MHZ
*
R3          5 51         2.188
R4          6 51         2.188
CIN 1 2     1.5E-12
C2          5 6          364E-12
I1          97 4         100E-3
IOS 1 2     1E-9
EOS 9 3     POLY(1) 26 28 35E-6 1
Q1          5 2 7 QX
Q2          6 9 8 QX
R5          7 4          1.672
R6          8 4          1.672
D1          2 36         DZ
D2          1 36         DZ
EN          3 1          10 0 1
GN1 0 2     13 0 1
GN2 0 1     16 0 1
*
EREF 98 0   28 0 1
EP          97 0         99 0 1
EM          51 0         50 0 1
*
* VOLTAGE NOISE SOURCE
*
DN1 35 10   DEN
DN2 10 11   DEN
VN1 35 0    DC 2
VN2 0 11    DC 2
*
* CURRENT NOISE SOURCE
*
DN3 12 13   DIN
DN4 13 14   DIN
VN3 12 0    DC 2
VN4 0 14    DC 2
CN1 13 0    7.53E-3
*
* CURRENT NOISE SOURCE
*
DN5 15 16   DIN
DN6 16 17   DIN
VN5 15 0    DC 2
VN6 0 17    DC 2
CN2 16 0    7.53E-3
*
* GAIN STAGE & DOMINANT POLE AT 32 HZ *
R7 18 98    1.09E6
C3 18 98    4.55E-9
G1 98 18    5 6 4.57E-1
V2 97 19    1.4
V3 20 51    1.4
D3 18 19    DX
D4 20 18    DX
*
* POLE/ZERO PAIR AT 1.5MHz/2.7MHz
*
R8 21 98    1E3
R9 21 22    1.25E3
C4 22 98    47.2E-12
G2 98 21    18 28 1E-3
*
* POLE AT 100 MHZ
*
R10 23 98   1
C5 23 98    1.59E-9
G3 98 23    21 28 1
*
* POLE AT 100 MHZ
*
R11 24 98   1
C6 24 98    1.59E-9
G4 98 24    23 28 1
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT
  1 kHZ *
R12 25 26   1E6
C7 25 26    1.59E-12
R13 26 98   1
E2 25 98    POLY(2) 1 98 2 98 0 2.506 2.506
*
* POLE AT 100 MHZ
*
R14 27 98   1
C8 27 98    1.59E-9
G5 98 27    24 28 1
*
* OUTPUT STAGE
*
R15 28 99           100E3
R16 28 50           100E3
C9 28 50            1E-6
ISY 99 50           1.85E-3
R17 29 99           100
R18 29 50           100
L2 29 34            1E-9
G6 32 50            27 29 10E-3
G7 33 50            29 27 10E-3
G8 29 99            99 27 10E-3
G9 50 29            27 50 10E-3
V4 30 29            1.3
V5 29 31            3.8
F1 29 0             V4 1
F2 0 29             V5 1
D5 27 30            DX
D6 31 27            DX
D7 99 32            DX
D8 99 33            DX
D9 50 32            DY
D10 50 33           DY
*
* MODELS USED
*
.MODEL QX PNP(BF = 5E5)
.MODEL DX           D(IS = 1E-12)
.MODEL DY           D(IS = 1E-15 BV = 50)
.MODEL DZ           D(IS = 1E-15 BV = 7.0)
.MODEL DEN D(IS = 1E-12 RS = 4.35K KF = 1.95E-15
AF = 1) .MODEL DIN D(IS = 1E-12 RS = 77.3E-6
KF = 3.38E-15 AF = 1) .ENDS OP-285
```



Spice Diagram (A)



Spice Diagram (B)



Spice Diagram (C)

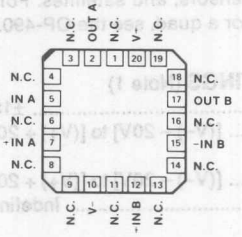
Precision, Low Power, Micropower Dual Operational Amplifier

OP290

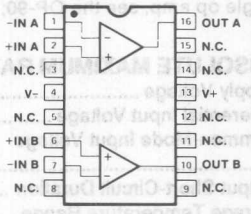
FEATURES

- Single/Dual Supply Operation ..... +1.6V to +36V
  ..... ±0.8V to ±18V
- True Single-Supply Operation; Input and Output Voltage Ranges Include Ground
- Low Supply Current (per amplifier) ..... 20μA Max
- High Output Drive ..... 5mA Min
- Low Input Offset Voltage ..... 200μV Max
- High Open-Loop Gain ..... 700V/mV Min
- Outstanding PSRR ..... 5.6μV/V Max
- Industry Standard 8-Pin Dual Pinout
- Available in Die Form

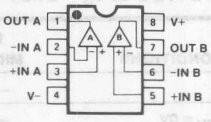
PIN CONNECTIONS



LCC
(RC-Suffix)



16-PIN SOL
(S-Suffix)



EPOXY MINI-DIP
(P-Suffix)

8-PIN HERMETIC DIP
(Z-Suffix)

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
200	OP290AZ*	–	OP290ARC/883	MIL
200	OP290EZ	–	–	XIND
300	OP290FZ	–	–	XIND
500	–	OP290GP	–	XIND
500	–	OP290GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

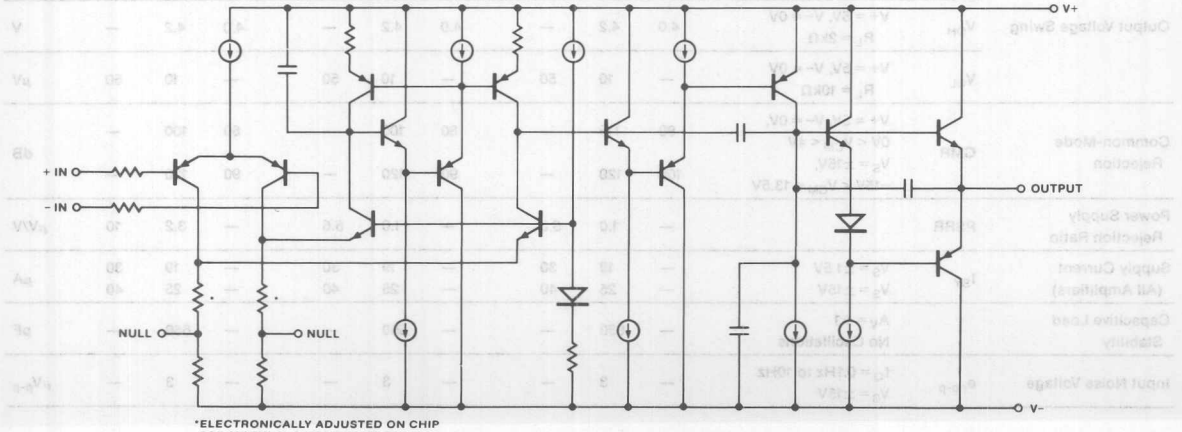
GENERAL DESCRIPTION

The OP-290 is a high performance micropower dual op amp that operates from a single supply of +1.6V to +36V or from dual supplies of ±0.8V to ±18V. Input voltage range includes the negative rail allowing the OP-290 to accommodate input signals down to ground in single supply operation. The OP-290's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

The OP-290 draws less than 20μA of quiescent supply current per amplifier, while able to deliver over 5mA of output current to a load. Input offset voltage is below 200μV eliminating the need for external nulling. Gain exceeds 700,000 and common-mode rejection is better than 100dB. The power

Continued

SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



*ELECTRONICALLY ADJUSTED ON CHIP FOR MINIMUM OFFSET VOLTAGE

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

GENERAL DESCRIPTION *Continued*

supply rejection ratio of under 5.6μV/V minimizes offset voltage changes experienced in battery powered systems.

The low offset voltage and high gain offered by the OP-290 bring precision performance to micropower applications. The minimal voltage and current requirements of the OP-290 suit it for battery and solar powered applications, such as portable instruments, remote sensors, and satellites. For a single op amp, see the OP-90; for a quad, see the OP-490.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... [(V–) – 20V] to [(V+) + 20V]
Common-Mode Input Voltage ..... [(V–) – 20V] to [(V+) + 20V]
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
P, RC, S, Z Package ..... –65°C to +150°C
Operating Temperature Range
OP-290A ..... –55°C to +125°C
OP-290E, OP-290F, OP-290G ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±1.5V to ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-290A/E MIN	OP-290A/E TYP	OP-290A/E MAX	OP-290F MIN	OP-290F TYP	OP-290F MAX	OP-290G MIN	OP-290G TYP	OP-290G MAX	UNITS
Input Offset Voltage	V_{OS}		—	50	200	—	75	300	—	125	500	μV
Input Offset Current	I_{OS}	V_{CM} = 0V	—	0.1	3	—	0.1	5	—	0.1	5	nA
Input Bias Current	I_B	V_{CM} = 0V	—	4.0	15	—	4.0	20	—	4.0	25	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V R_L = 100kΩ	700	1200	—	500	1000	—	400	800	—	V/mV
		R_L = 10kΩ	350	600	—	250	500	—	200	400	—	
		R_L = 2kΩ	125	250	—	100	200	—	100	200	—	
		V+ = 5V, V– = 0V, 1V < V_O < 4V R_L = 100kΩ	200	400	—	125	300	—	100	250	—	
		R_L = 10kΩ	100	180	—	75	140	—	70	140	—	
Input Voltage Range	IVR	V+ = 5V, V– = 0V	0/4	—	—	0/4	—	—	0/4	—	—	V
		V_S = ±15V (Note 1)	–15/13.5	—	—	–15/13.5	—	—	–15/13.5	—	—	
Output Voltage Swing	V_O	V_S = ±15V R_L = 10kΩ	±13.5	±14.2	—	±13.5	±14.2	—	±13.5	±14.2	—	V
		R_L = 2kΩ	±10.5	±11.5	—	±10.5	±11.5	—	±10.5	±11.5	—	
	V_{OH}	V+ = 5V, V– = 0V R_L = 2kΩ	4.0	4.2	—	4.0	4.2	—	4.0	4.2	—	V
	V_{OL}	V+ = 5V, V– = 0V R_L = 10kΩ	—	10	50	—	10	50	—	10	50	μV
Common-Mode Rejection	CMR	V+ = 5V, V– = 0V, 0V < V_{CM} < 4V	90	115	—	80	100	—	80	100	—	dB
		V_S = ±15V, –15V < V_{CM} < 13.5V	100	120	—	90	120	—	90	120	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	1.0	5.6	—	3.2	10	μV/V
Supply Current (All Amplifiers)	I_{SY}	V_S = ±1.5V	—	19	30	—	19	30	—	19	30	μA
		V_S = ±15V	—	25	40	—	25	40	—	25	40	
Capacitive Load Stability		A_V = +1 No Oscillations	—	650	—	—	650	—	—	650	—	pF
Input Noise Voltage	e_{np-p}	f_O = 0.1Hz to 10Hz V_S = ±15V	—	3	—	—	3	—	—	3	—	μV_{p-p}

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-290A/E MIN	OP-290A/E TYP	OP-290A/E MAX	OP-290F MIN	OP-290F TYP	OP-290F MAX	OP-290G MIN	OP-290G TYP	OP-290G MAX	UNITS
Input Resistance Differential-Mode	R_{IN}	$V_S = \pm 15V$	—	30	—	—	30	—	—	30	—	MΩ
Input Resistance Common-Mode	R_{INCM}	$V_S = \pm 15V$	—	20	—	—	20	—	—	20	—	GΩ
Slew Rate	SR	$A_V = +1$ $V_S = \pm 15V$	5	12	—	5	12	—	5	12	—	V/ms
Gain Bandwidth Product	GBWP	$A_V = +1$ $V_S = \pm 15V$	—	20	—	—	20	—	—	20	—	kHz
Channel Separation	CS	$f_O = 10Hz$ $V_O = 20V_{p-p}$ $V_S = \pm 15V$ (Note 2)	120	150	—	120	150	—	120	150	—	dB

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed but not 100% tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-290A MIN	OP-290A TYP	OP-290A MAX	UNITS
Input Offset Voltage	V_{OS}		—	80	500	μV
Average Input Offset Voltage Drift	TCV_{OS}	$V_S = \pm 15V$	—	0.3	3	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.1	5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.2	20	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$				V/mV
		$R_L = 100k\Omega$	225	400	—	
		$R_L = 10k\Omega$	125	240	—	
		$R_L = 2k\Omega$	50	110	—	
		$V+ = 5V$, $V- = 0V$, $1V < V_O < 4V$				
		$R_L = 100k\Omega$	100	200	—	
		$R_L = 10k\Omega$	50	110	—	
Input Voltage Range	IVR	$V+ = 5V$, $V- = 0V$ (Note 1)	0/3.5	—	—	V
		$V_S = \pm 15V$	−15/13.5	—	—	
Output Voltage Swing	V_O	$V_S = \pm 15V$				V
		$R_L = 10k\Omega$	±13	±14.1	—	
		$R_L = 2k\Omega$	±10	±11	—	
	V_{OH}	$V+ = 5V$, $V- = 0V$ $R_L = 2k\Omega$	3.9	4.1	—	V
	V_{OL}	$V+ = 5V$, $V- = 0V$ $R_L = 10k\Omega$	—	10	100	μV
Common-Mode Rejection	CMR	$V+ = 5V$, $V- = 0V$, $0V < V_{CM} < 3.5V$	80	105	—	dB
		$V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	90	115	—	
Power Supply Rejection Ratio	PSRR		—	3.2	10	μV/V
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 1.5V$	—	30	50	μA
		$V_S = \pm 15V$	—	38	60	

NOTE:
1. Guaranteed by CMR test.

9

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	70	400	—	115	600	—	200	750	μV
Average Input Offset Voltage Drift	TCV_{OS}	$V_S = \pm 15V$	—	0.3	3	—	0.6	5	—	1.2	—	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.1	3	—	0.1	5	—	0.1	7	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.2	15	—	4.2	20	—	4.2	25	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$										V/mV
		$R_L = 100k\Omega$	500	800	—	350	700	—	300	600	—	
		$R_L = 10k\Omega$	250	400	—	175	350	—	150	250	—	
		$R_L = 2k\Omega$	100	200	—	75	150	—	75	125	—	
		V+ = 5V, V− = 0V, $1V < V_O < 4V$										
		$R_L = 100k\Omega$	150	280	—	100	220	—	80	160	—	
		$R_L = 10k\Omega$	75	140	—	50	110	—	40	90	—	
Input Voltage Range	IVR	V+ = 5V, V− = 0V	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$ (Note 1)	−15/13.5	—	—	−15/13.5	—	—	−15/13.5	—	—	
	V_O	$V_S = \pm 15V$										V
		$R_L = 10k\Omega$	±13	±14	—	±13	±14	—	±13	±14	—	
		$R_L = 2k\Omega$	±10	±11	—	±10	±11	—	±10	±11	—	
Output Voltage Swing	V_{OH}	V+ = 5V, V− = 0V $R_L = 2k\Omega$	3.9	4.1	—	3.9	4.1	—	3.9	4.1	—	V
	V_{OL}	V+ = 5V, V− = 0V $R_L = 10k\Omega$	—	10	100	—	10	100	—	10	100	μV
Common-Mode Rejection	CMR	V+ = 5V, V− = 0V, $0V < V_{CM} < 3.5V$	85	105	—	80	100	—	80	100	—	dB
		$V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	95	115	—	90	110	—	90	110	—	
Power Supply Rejection Ratio	PSRR		—	3.2	7.5	—	5.6	10	—	5.6	15	μV/V
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 1.5V$	—	24	50	—	24	50	—	24	50	μA
		$V_S = \pm 15V$	—	31	60	—	31	60	—	31	60	

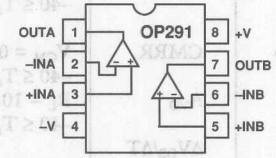
NOTE:
1. Guaranteed by CMR test.

FEATURES
Single-Supply Operation: 2.7 V to 12 V
Wide Input Voltage Range
Rail-to-Rail Output Swing
Low Supply Current: 300 μA/Amp
Wide Bandwidth: 3 MHz
Slew Rate: 0.5 V/μs
Low Offset Voltage: 700 μV
No Phase Reversal
Drives Capacitive Loads

APPLICATIONS
Industrial Process Control
Battery Powered Instrumentation
Power Supply Control and Protection
Telecom
Remote Sensors
Low Voltage Strain Gage Amplifiers
DAC Output Amplifier

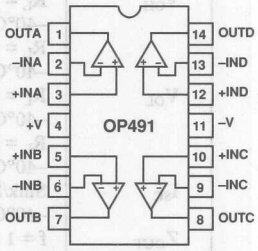
PIN CONFIGURATIONS

8-Lead Epoxy DIP (P Suffix)



8-Lead Narrow-Body SO (S Suffix)

14-Lead Epoxy DIP (P Suffix)



14-Lead Narrow-Body SO (S Suffix)

9

GENERAL DESCRIPTION

The OP291 and OP491 are dual and quad micropower single-supply, 3 MHz bandwidth amplifiers featuring rail-to-rail inputs and outputs. The OP291 and OP491 are guaranteed to operate from a 3 volt single supply as well as ±5 volt dual supplies.

Fabricated on Analog Devices' CBCMOS process, the OP291/OP491 have a unique input stage that allows the input voltage to safely extend 10 volts beyond either supply without any phase inversion or latch-up. The output voltage swings to within millivolts of the supplies and continues to sink or source current all the way to the supplies.

Applications for these amplifiers include portable telecom equipment, power supply control and protection, and interface for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezo electric, and resistive transducers.

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and maintain high signal-to-noise ratios.

The OP291/OP491 are specified over the extended industrial (–40°C to +125°C) temperature range. The OP291 dual amplifiers are available in 8-pin plastic DIPs and SO surface mount packages. The OP491 quad is available in 14-pin DIPs and 14-pin SO packages.

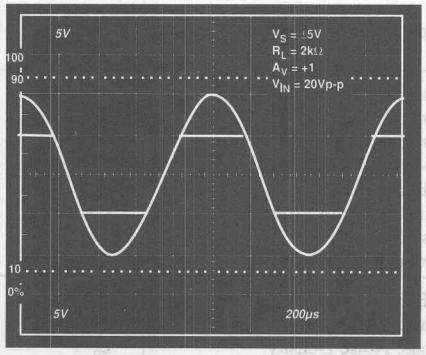


Figure 1. Input and Output with Inputs Overdriven by 5 V

OP291/OP491–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = +3.0 V, V_{CM} = 0.05 V, V_O = 1.4 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage OP291	V_{OS}			80	700	µV
		–40 ≤ T_A ≤ +125°C			1.5	mV
OP491	V_{OS}			80	700	µV
		–40 ≤ T_A ≤ +125°C			1.5	mV
Input Bias Current	I_B			30	50	nA
		–40 ≤ T_A ≤ +125°C			60	nA
Input Offset Current	I_{OS}			0.1	8	nA
		–40 ≤ T_A ≤ +125°C			16	nA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	70	90		dB
		–40 ≤ T_A ≤ +125°C	65	87		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ , V_O = 0.3 V to 2.7 V	25	70		V/mV
		–40 ≤ T_A ≤ +125°C		50		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1.1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			100		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		pA/°C
OUTPUT CHARACTERISTICS n						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	2.95	2.99		V
		–40°C to +125°C	2.90	2.98		V
		R_L = 2 kΩ to GND	2.8	2.9		V
		–40°C to +125°C	2.70	2.8		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		4.5	10	mV
		–40°C to +125°C			35	mV
		R_L = 2 kΩ to V+		40	55	mV
		–40°C to +125°C			100	mV
Short Circuit Limit	I_{SC}	Sink/Source	±9	±13.5		mA
		–40°C to +125°C	±6.5	±10.5		mA
Open Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V	80	110		dB
		–40°C ≤ T_A ≤ +125°C	75	110		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		200	350	µA
		–40°C ≤ T_A ≤ +125°C		330	480	µA
DYNAMIC PERFORMANCE						
Slew Rate	+SR	R_L = 10 kΩ		0.4		V/µs
Slew Rate	–SR	R_L = 10 kΩ		0.4		V/µs
Full-Power Bandwidth	BW_P	1% Distortion		1.2		kHz
Settling Time	t_S	To 0.01%		22		µs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	θ_O			45		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 10 kΩ		145		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		35		nV/√Hz
Current Noise Density	i_n			0.8		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V_S = +5.0 V, V_{CM} = 0.05 V, V_O = 1.4 V, T_A = +25°C unless otherwise noted)

Parameter		Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS							
Offset Voltage	OP291	V_{OS}			80	700	µV
			$-40 \le T_A \le +125°C$			1.5	mV
	OP491	V_{OS}			80	700	µV
			$-40 \le T_A \le +125°C$			1.5	mV
Input Bias Current		I_B			30	50	nA
			$-40 \le T_A \le +125°C$			60	nA
Input Offset Current		I_{OS}			0.1	8	nA
			$-40 \le T_A \le +125°C$			16	nA
Input Voltage Range				0		5	V
Common-Mode Rejection Ratio		CMRR	V_{CM} = 0 V to 5 V	70	93		dB
			$-40 \le T_A \le +125°C$	65	90		dB
Large Signal Voltage Gain		A_{VO}	R_L = 10 kΩ, V_O = 0.3 V to 4.7 V	25	70		V/mV
			$-40 \le T_A \le +125°C$		50		V/mV
Offset Voltage Drift		$\Delta V_{OS}/\Delta T$	$-40 \le T_A \le +125°C$		1.1		µV/°C
Bias Current Drift		$\Delta I_B/\Delta T$			100		pA/°C
Offset Current Drift		$\Delta I_{OS}/\Delta T$			20		pA/°C
OUTPUT CHARACTERISTICS							
Output Voltage High		V_{OH}	R_L = 100 kΩ to GND	4.95	4.99		V
			–40°C to +125°C	4.90	4.98		V
			R_L = 2 kΩ to GND	4.8	4.85		V
			–40°C to +125°C	4.65	4.75		V
Output Voltage Low		V_{OL}	R_L = 100 kΩ to V+		4.5	10	mV
			–40°C to +125°C			35	mV
			R_L = 2 kΩ to V+		40	55	mV
			–40°C to +125°C			155	mV
Short Circuit Limit		I_{SC}	Sink/Source	±9	±13.5		mA
			–40°C to +125°C	±6.5	±10.5		mA
Open Loop Impedance		Z_{OUT}	f = 1 MHz, A_V = 1		200		Ω
POWER SUPPLY							
Power Supply Rejection Ratio		PSRR	V_S = 2.7 V to 12 V	80	110		dB
			$-40 \le T_A \le +125°C$	75	110		dB
Supply Current/Amplifier		I_{SY}	V_O = 0 V		220	400	µA
			$-40 \le T_A \le +125°C$		350	500	µA
DYNAMIC PERFORMANCE							
Slew Rate		+SR	R_L = 10 kΩ		0.4		V/µs
Slew Rate		–SR	R_L = 10 kΩ		0.4		V/µs
Full-Power Bandwidth		BW_P	1% Distortion		1.2		kHz
Settling Time		t_S	To 0.01%		22		µs
Gain Bandwidth Product		GBP			3		MHz
Phase Margin		θ_O			45		Degrees
Channel Separation		CS	f = 1 kHz, R_L = 10 kΩ		145		dB
NOISE PERFORMANCE							
Voltage Noise		e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density		e_n	f = 1 kHz		35		nV/√Hz
Current Noise Density		i_n			0.8		pA/√Hz

NOTES
+5 V specifications are guaranteed by +3 V and ±5 V testing.
Specifications subject to change without notice.

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Parameter		Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS							
Offset Voltage	OP291	V_{OS}			80	700	µV
			$-40 \le T_A \le +125°C$			1.5	mV
	OP491	V_{OS}			80	700	µV
			$-40 \le T_A \le +125°C$			1.5	mV
Input Bias Current		I_B			30	50	nA
			$-40 \le T_A \le +125°C$			60	nA
Input Offset Current		I_{OS}			0.1	8	nA
			$-40 \le T_A \le +125°C$			16	nA
Input Voltage Range				–5		+5	V
Common-Mode Rejection		CMR	$V_{CM} = \pm 5$ V	75	100		dB
			$-40 \le T_A \le +125°C$	67	97		dB
Large Signal Voltage Gain		A_{VO}	$R_L = 10$ kΩ, $V_O = \pm 4.7$ V,	25	70		
			$-40 \le T_A \le +125°C$		50		V/mV
Offset Voltage Drift		$\Delta V_{OS}/\Delta T$			1.1		µV/°C
Bias Current Drift		$\Delta I_B/\Delta T$			100		pA/°C
Offset Current Drift		$\Delta I_{OS}/\Delta T$			20		pA/°C
OUTPUT CHARACTERISTICS							
Output Voltage Swing		V_O	$R_L = 100$ kΩ to GND	±4.93	±4.99		V
			–40°C to +125°C	±4.90	±4.98		V
			$R_L = 2$ kΩ to GND	±4.80	±4.95		V
			$-40 \le T_A \le +125°C$	±4.65	±4.75		V
Short Circuit Limit		I_{SC}	Sink/Source	±9	±16		mA
			–40°C to +125°C	±6	±13		mA
Open Loop Impedance		Z_{OUT}	f = 1 MHz, $A_V = 1$		200		Ω
POWER SUPPLY							
Power Supply Rejection Ratio		PSRR	$V_S = \pm 5$ V	80	110		dB
			$-40 \le T_A \le +125°C$	70	100		dB
Supply Current/Amplifier		I_{SY}	$V_O = 0$ V		260	420	µA
			$-40 \le T_A \le +125°C$		390	550	µA
DYNAMIC PERFORMANCE							
Slew Rate		±SR	$R_L = 10$ kΩ		0.5		V/µs
Full-Power Bandwidth		BW_P	1% Distortion		1.2		kHz
Settling Time		t_S	To 0.01%		22		µs
Gain Bandwidth Product		GBP			3		MHz
Phase Margin		θ_O			45		Degrees
Channel Separation		CS	f = 1 kHz		145		dB
NOISE PERFORMANCE							
Voltage Noise		e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density		e_n	f = 1 kHz		35		$nV/\sqrt{Hz}$
Current Noise Density		i_n			0.8		$pA/\sqrt{Hz}$

Specifications subject to change without notice.

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		±300	µV max
Input Bias Current	I_B		50	nA max
Input Offset Current	I_{OS}		8	nA
Input Voltage Range	V_{CM}		V– to V+	V min
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 10 V	70	dB min
Power Supply Rejection Ratio	PSRR	V = 2.7 V to +12 V	80	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	25	V/mV min
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	2.8	V min
Output Voltage Low	V_{OL}	R_L = 2 kΩ to V+	55	mV max
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞	350	µA max

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... +16 V
Input Voltage ..... V– to V+ 10 V
Differential Input Voltage ..... 7 V
Output Short-Circuit Duration to GND ..... Indefinite
Storage Temperature Range
P, S Packages ..... –65°C to +150°C
Operating Temperature Range
OP291/OP491G ..... –40°C to +125°C
Junction Temperature Range
P, S Packages ..... –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) ..... +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
14-Pin SOIC (S)	120	36	°C/W

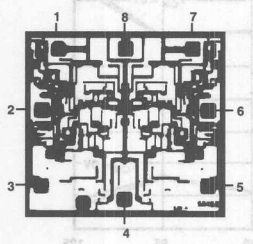
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for the worst case conditions; i.e., θ_{JA} is specified for device in socket for P-DIP packages, θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

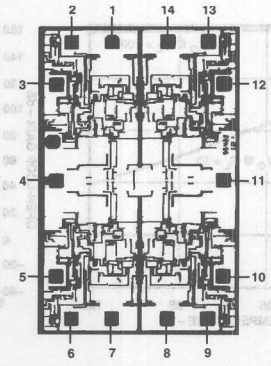
Model	Temperature Range	Package Description	Package Option*
OP291GP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP291GS	–40°C to +125°C	8-Pin SOIC	SO-8
OP291GBC	+25°C	DICE	
OP491GP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP491GS	–40°C to +125°C	14-Pin SOIC	SO-14
OP491GBC	+25°C	DICE	

*For outline information see Package Information section.

DICE CHARACTERISTICS



OP291 Die Size 0.070 × 0.070 Inch, 4,900 Sq. Mils. Substrate (Die Backside) Is Connected to V+. Transistor Count, 146.



OP491 Die Size 0.070 × 0.110 Inch, 7,700 Sq. Mils. Substrate (Die Backside) Is Connected to V+. Transistor Count, 290.

9

OP291/OP491–Typical Performance Characteristics

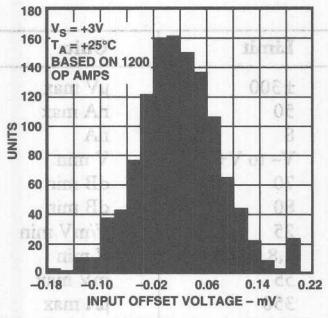


Figure 2. OP291 Input Offset Voltage Distribution, V_S = +3 V

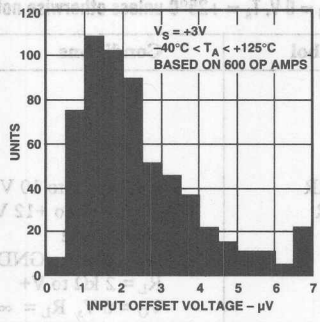


Figure 3. OP291 Input Offset Voltage Drift Distribution, V_S = +3 V

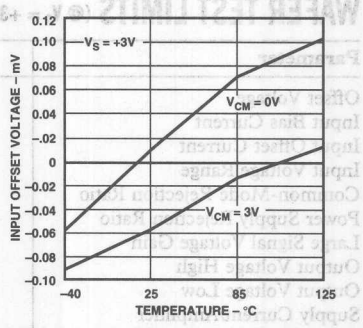


Figure 4. OP291/OP491 Input Offset Voltage vs. Temperature, V_S = +3 V

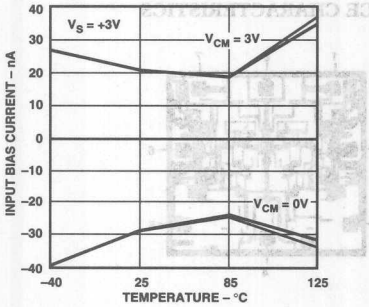


Figure 5. OP291/OP491 Input Bias Current vs. Temperature, V_S = +3 V

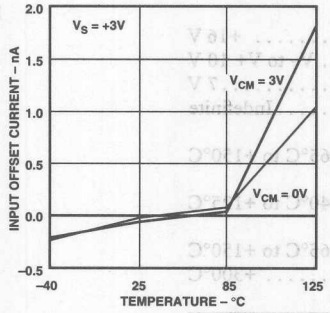


Figure 6. OP291/OP491 Input Offset Current vs.Temperature, V_S = +3 V

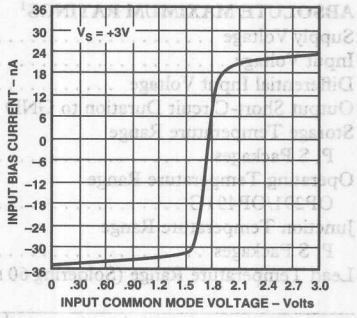


Figure 7. OP291/OP491 Input Bias Current vs. Common-Mode Voltage, V_S = +3 V

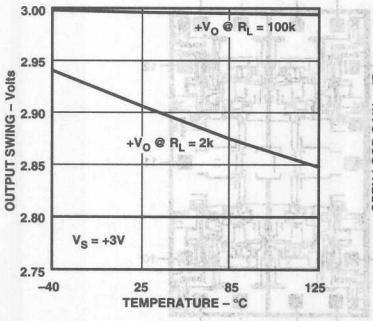


Figure 8. OP291/OP491 Output Voltage Swing vs. Temperature, V_S = +3 V

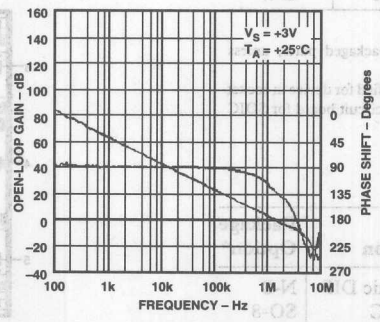


Figure 9. OP291/OP491 Open-Loop Gain & Phase vs. Frequency, V_S = +3 V

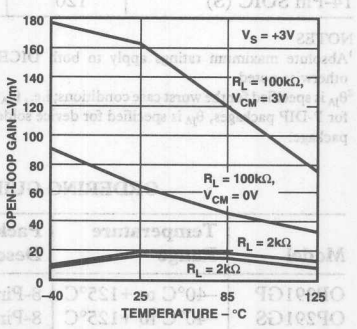


Figure 10. OP291/OP491 Open-Loop Gain vs. Temperature, V_S = +3 V

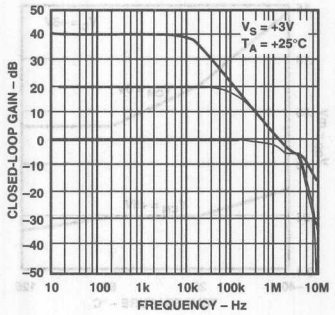


Figure 11. OP291/OP491 Closed-Loop Gain vs. Frequency, V_S = +3 V

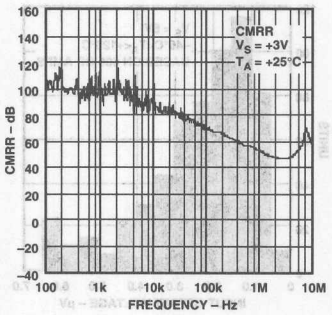


Figure 12. OP291/OP491 CMRR vs. Frequency, V_S = +3 V

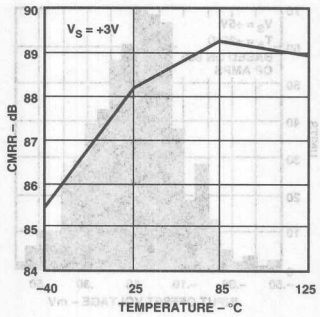


Figure 13. OP291/OP491 CMRR vs. Temperature, V_S = +3 V

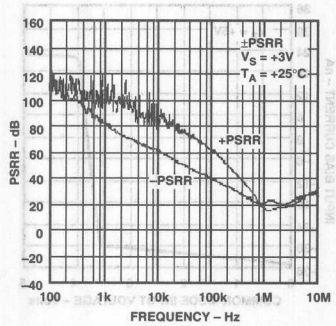


Figure 14. OP291/OP491 PSRR vs. Frequency, V_S = +3 V

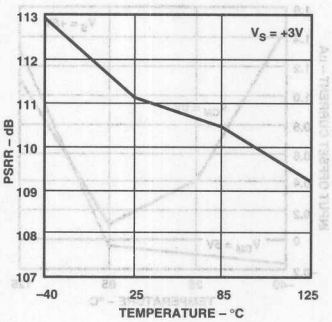


Figure 15. OP291/OP491 PSRR vs. Temperature, V_S = +3 V

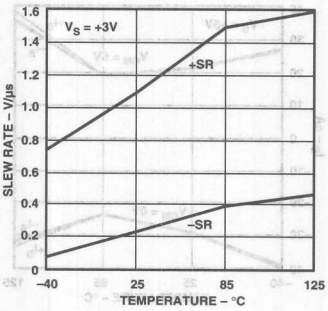


Figure 16. OP291/OP491 Slew Rate vs. Temperature, V_S = +3 V

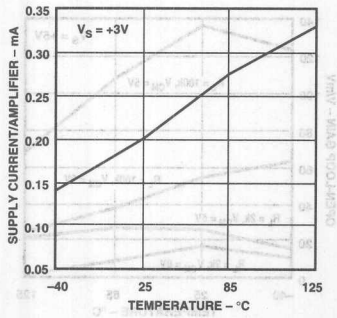


Figure 17. OP291/OP491 Supply Current vs. Temperature, V_S = +3 V, +5 V, ±5 V

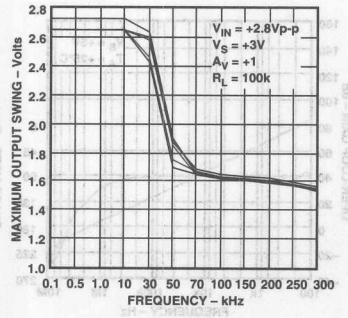


Figure 18. Maximum Output Swing vs. Frequency, V_S = +3 V

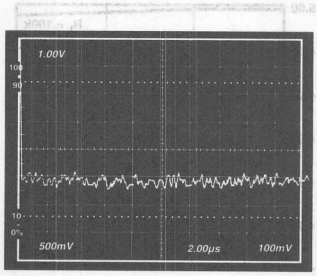


Figure 19. OP291/OP491 Voltage Noise Density

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OP291/OP491–Typical Performance Characteristics

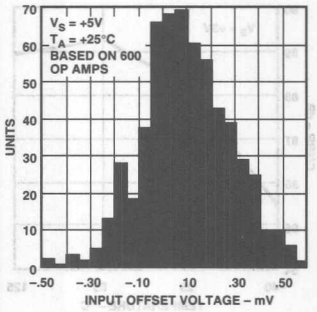

Figure 20. OP291 Input Offset Voltage Distribution, V_S = +5 V

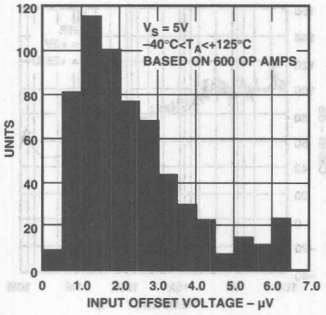

Figure 21. OP291 Input Offset Voltage Drift Distribution, V_S = +5 V

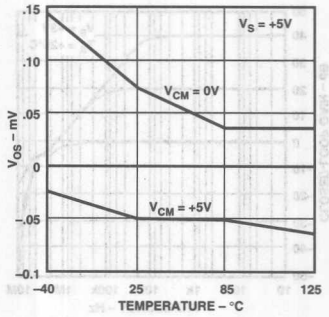

Figure 22. OP291/OP491 Input Offset Voltage vs. Temperature, V_S = +5 V

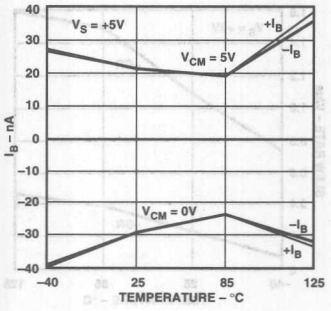

Figure 23. OP291/OP491 Input Bias Current vs. Temperature, V_S = +5 V

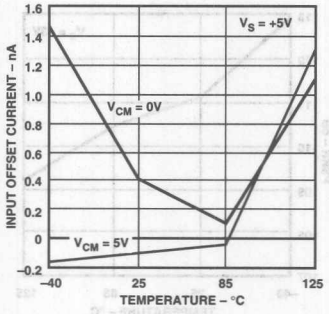

Figure 24. OP291/OP491 Input Offset Current vs. Temperature, V_S = +5 V

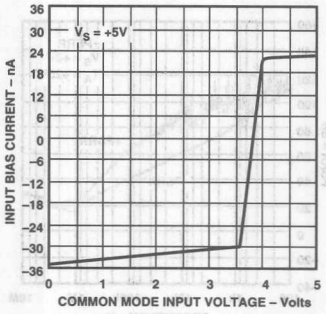

Figure 25. OP291/OP491 Input Bias Current vs. Common-Mode Voltage, V_S = +5 V

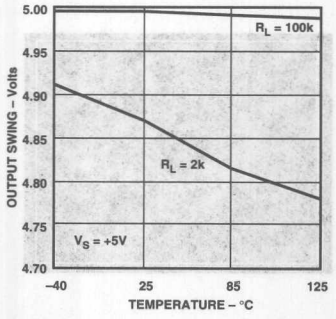

Figure 26. OP291/491 Output Voltage Swing vs. Temperature, V_S = +5 V

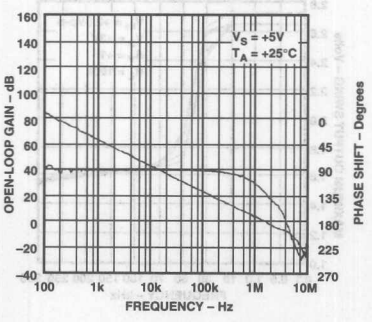

Figure 27. OP291/491 Open-Loop Gain & Phase vs. Frequency, V_S = +5 V

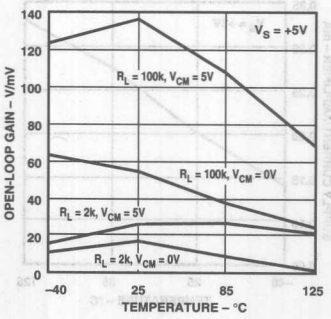

Figure 28. OP291/491 Open-Loop Gain vs. Temperature, V_S = +5 V

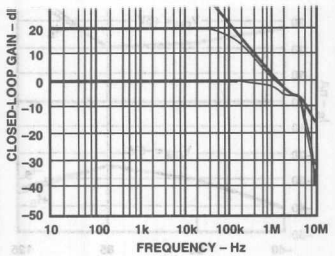

Figure 29. OP291/OP491 Closed-Loop Gain vs. Frequency, V_S = +5 V

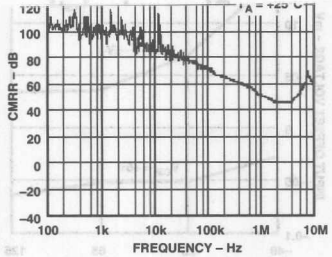

Figure 30. OP291/OP491 CMRR vs. Frequency, V_S = +5 V

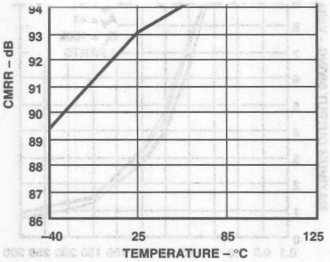

Figure 31. OP291/OP491 CMRR vs. Temperature, V_S = +5 V

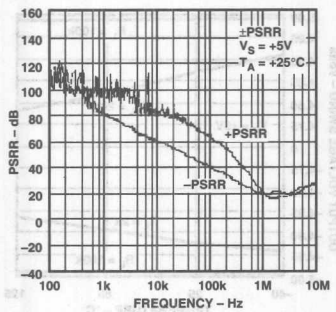

Figure 32. OP291/OP491 PSRR vs. Frequency, V_S = +5 V

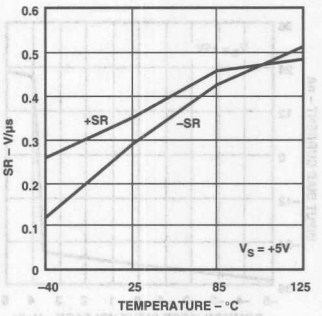

Figure 33. OP291 Slew Rate vs. Temperature, V_S = +5 V

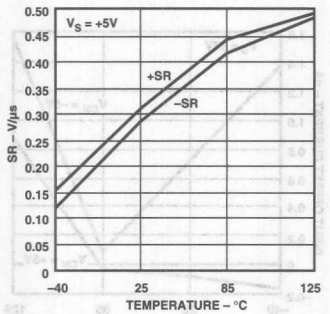

Figure 34. OP491 Slew Rate vs. Temperature, V_S = +5 V

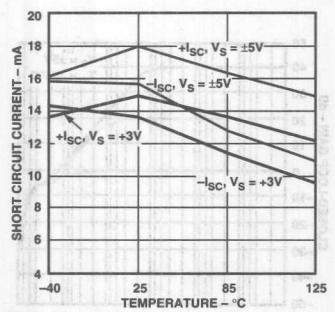

Figure 35. OP291/OP491 Short Circuit Current vs. Temperature, V_S = +3 V, +5 V, ±5 V

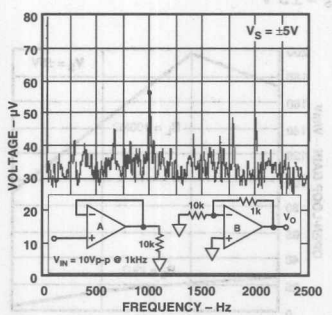

Figure 36. OP291/OP491 Channel Separation, V_S = ±5 V

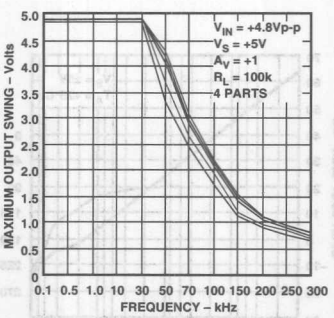

Figure 37. Maximum Output Swing vs. Frequency, V_S = ±5 V

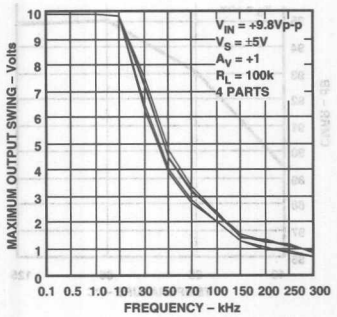

Figure 38. Maximum Output Swing vs. Frequency, $V_S = \pm 5$ V

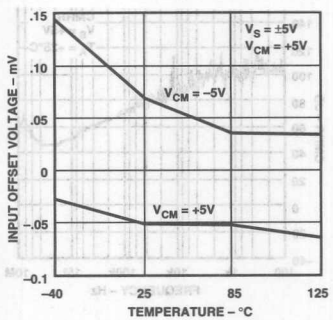

Figure 39. OP291/OP491 Input Offset Voltage vs. Temperature, $V_S = \pm 5$ V

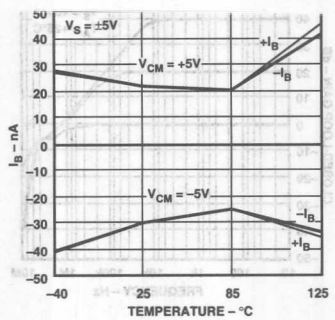

Figure 40. OP291/OP491 Input Bias Current vs. Temperature, $V_S = \pm 5$ V

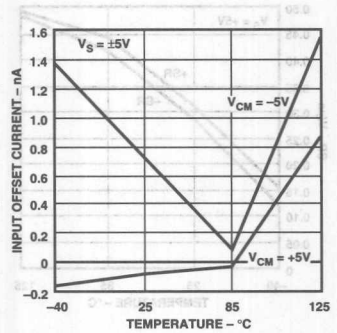

Figure 41. OP291/OP491 Input Offset Current vs. Temperature, $V_S = \pm 5$ V

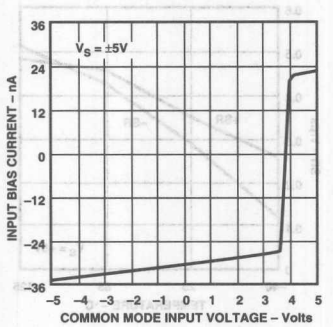

Figure 42. OP291/OP491 Input Bias Current vs. Common-Mode Voltage, $V_S = \pm 5$ V

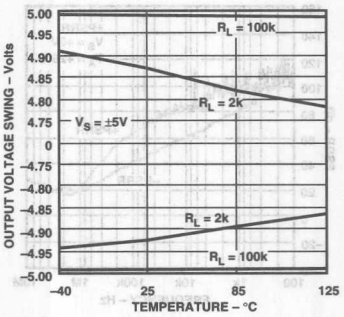

Figure 43. OP291/OP491 Output Voltage Swing vs. Temperature, $V_S = \pm 5$ V

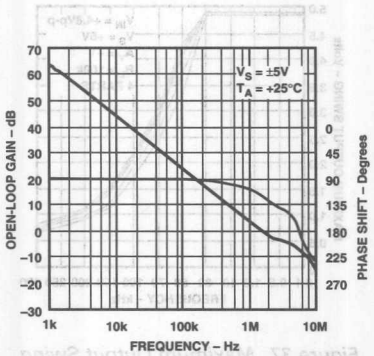

Figure 44. OP291/OP491 Open-Loop Gain & Phase vs. Frequency, $V_S = \pm 5$ V

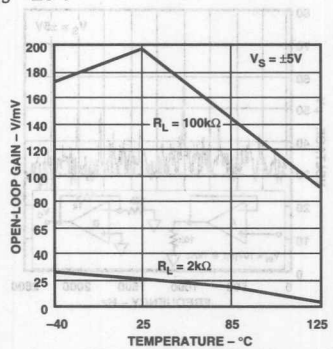

Figure 45. OP291/OP491 Open-Loop Gain vs. Temperature, $V_S = \pm 5$ V

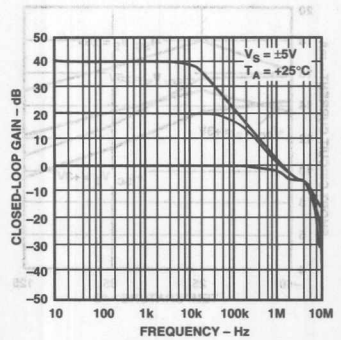

Figure 46. OP291/OP491 Closed-Loop Gain vs. Frequency, $V_S = \pm 5$ V

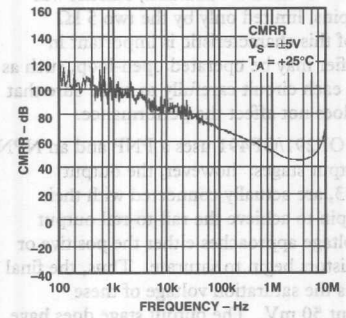

Figure 47. OP291/OP491 CMRR vs. Frequency, V_S = ±5 V

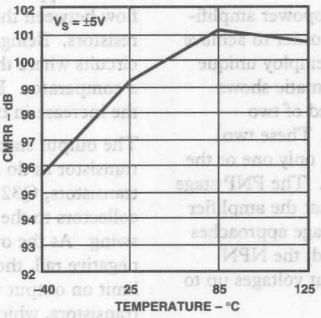

Figure 48. OP291/OP491 CMRR vs. Temperature, V_S = ±5 V

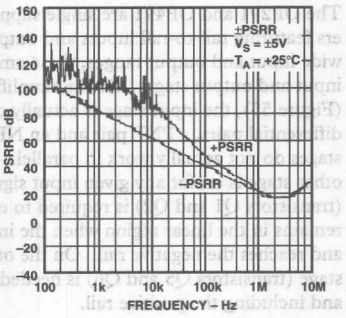

Figure 49. OP291/OP491 PSRR vs. Frequency, V_S = ±5 V

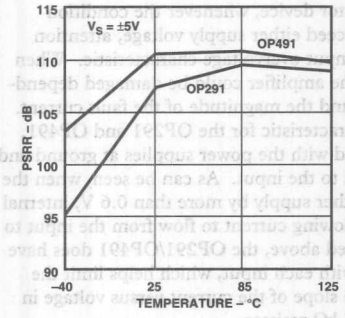

Figure 50. OP291/OP491 PSRR vs. Temperature, V_S = ±5 V

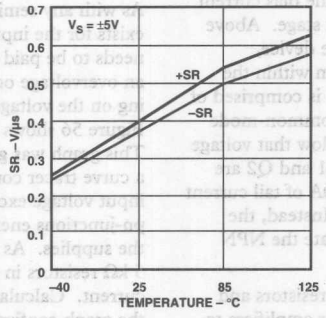

Figure 51. OP291/OP491 Slew Rate vs. Temperature, V_S = ±5 V

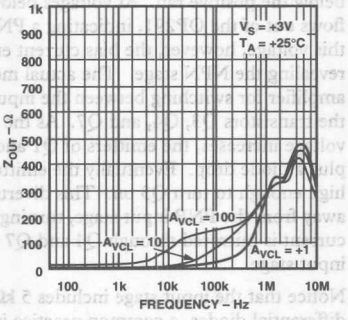

Figure 52. OP291/OP491 Output Impedance vs. Frequency

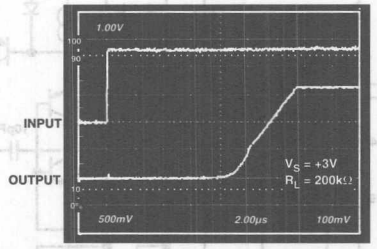

Figure 53. OP291/OP491 Large Signal Transient Response, V_S = +3 V

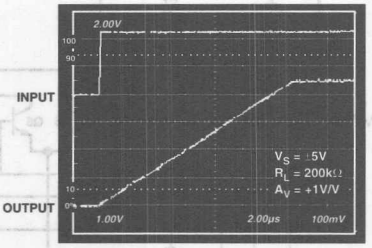

Figure 54. OP291/OP491 Large Signal Transient Response, V_S = ±5 V

FUNCTIONAL DESCRIPTION

The OP291 and OP491 are single supply, micropower amplifiers featuring rail-to-rail inputs and outputs. In order to achieve wide input and output ranges, these amplifiers employ unique input and output stages. As the simplified schematic shows (Figure 55), the input stage is actually comprised of two differential pairs, a PNP pair and an NPN pair. These two stages do not actually work in parallel. Instead, only one or the other stage is on for any given input signal level. The PNP stage (transistors Q1 and Q2) is required to ensure that the amplifier remains in the linear region when the input voltage approaches and reaches the negative rail. On the other hand, the NPN stage (transistors Q5 and Q6) is needed for input voltages up to and including the positive rail.

For the majority of the input common-mode range, the PNP stage is active, as is evidenced by examining the graph of Input Bias Current vs. Common-Mode Voltage. Notice that the bias current switches direction at approximately 1.2 volts to 1.3 volts below the positive rail. At voltages below this, the bias current flows out of the OP291, indicating a PNP input stage. Above this voltage, however, the bias current enters the device, revealing the NPN stage. The actual mechanism within the amplifier for switching between the input stages is comprised of the transistors Q3, Q4, and Q7. As the input common-mode voltage increases, the emitters of Q1 and Q2 follow that voltage plus a diode drop. Eventually the emitters of Q1 and Q2 are high enough to turn Q3 on. This diverts the 8 μA of tail current away from the PNP input stage, turning it off. Instead, the current is mirrored through Q4 and Q7 to activate the NPN input stage.

Notice that the input stage includes 5 kΩ series resistors and differential diodes, a common practice in bipolar amplifiers to protect the input transistors from large differential voltages. These diodes will turn on whenever the differential voltage exceeds approximately 0.6 V. In this condition, current will flow between the input pins, limited only by the two 5 kΩ resistors. Being aware of this characteristic is important in circuits where the amplifier may be operated open-loop, such as a comparator. Evaluate each circuit carefully to make sure that the increase in current does not affect the performance.

The output stage of the OP291/OP491 uses a PNP and an NPN transistor as do most output stages; however, the output transistors, Q32 and Q33, are actually connected with their collectors to the output pin to achieve the rail-to-rail output swing. As the output voltage approaches either the positive or negative rail, these transistors begin to saturate. Thus, the final limit on output voltage is the saturation voltage of these transistors, which is about 50 mV. The output stage does have inherent gain arising from the collectors and any external load impedance. Because of this, the open-loop gain of the amplifier is dependent on the load resistance.

Input Overvoltage Protection

As with any semiconductor device, whenever the condition exists for the input to exceed either supply voltage, attention needs to be paid to the input overvoltage characteristic. When an overvoltage occurs, the amplifier could be damaged depending on the voltage level and the magnitude of the fault current. Figure 56 shows the characteristic for the OP291 and OP491. This graph was generated with the power supplies at ground and a curve tracer connected to the input. As can be seen, when the input voltage exceeds either supply by more than 0.6 V, internal pn-junctions energize allowing current to flow from the input to the supplies. As described above, the OP291/OP491 does have 5 kΩ resistors in series with each input, which helps limit the current. Calculating the slope of the current versus voltage in the graph confirms the 5 kΩ resistor.

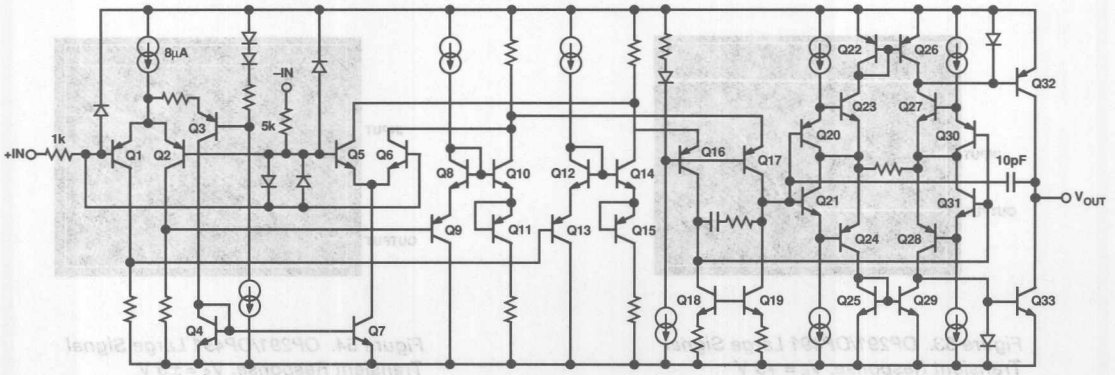

Figure 55. OP291/OP491 Simplified Schematic

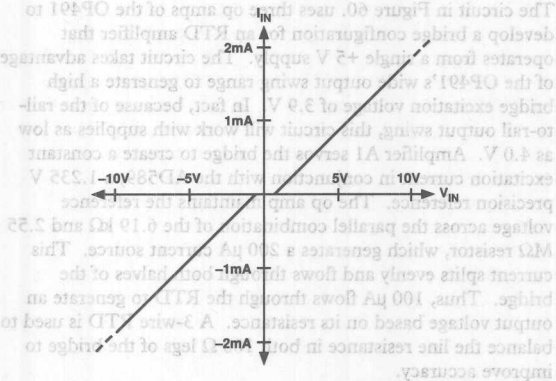

Figure 56. Input Overvoltage Characteristics

This input current is not inherently damaging to the device as long as it is limited to 5 mA or less. In the case shown, for an input of 10 V over the supply, the current is limited to 1.8 mA. If the voltage is large enough to cause more than 5 mA of current to flow, then an external series resistor should be added. The size of this resistor is calculated by dividing the maximum overvoltage by 5 mA and subtracting the internal 5 kΩ resistor. For example, if the input voltage could reach 100 V, the external resistor should be (100 V/5 mA) –5 k = 15 kΩ. This resistance should be placed in series with either or both inputs if they are subjected to the overvoltages. For more information on general overvoltage characteristics of amplifiers refer to the *1993 System Applications Guide*, available from the Analog Devices Literature Center.

Output Voltage Phase Reversal

Some operational amplifiers designed for single-supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. Typically for single-supply bipolar op amps, the negative supply determines the lower limit of their common-mode range. With these devices, external clamping diodes, with the anode connected to ground and the cathode to the inputs, prevent input signal excursions from exceeding the device's negative supply (i.e., GND), preventing a condition which could cause the output voltage to change phase. JFET-input amplifiers may also exhibit phase reversal, and, if so, a series input resistor is usually required to prevent it.

The OP291/OP491 is free from reasonable input voltage range restrictions due to its novel input structure. In fact, the input signal can exceed the supply voltage by a significant amount without causing damage to the device. As illustrated in Figure 57, the OP291/OP491 can safely handle a 20 V p-p input signal on ±5 V supplies without exhibiting any sign of output voltage phase reversal or other anomalous behavior. Thus no external clamping diodes are required.

Overdrive Recovery

The overdrive recovery time of an operational amplifier is the time required for the output voltage to recover to its linear region from a saturated condition. This recovery time is important in applications where the amplifier must recover quickly after a large transient event, such as a comparator. The circuit shown in Figure 58 was used to evaluate the OP291/OP491's overload recovery time. The OP291/OP491 takes approximately 8 µs to recover from positive saturation and approximately 6.5 µs to recover from negative saturation.

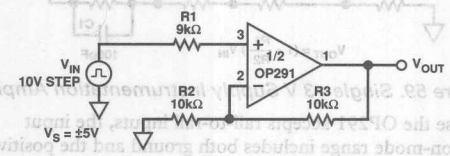

Figure 58. Overdrive Recovery Time Test Circuit

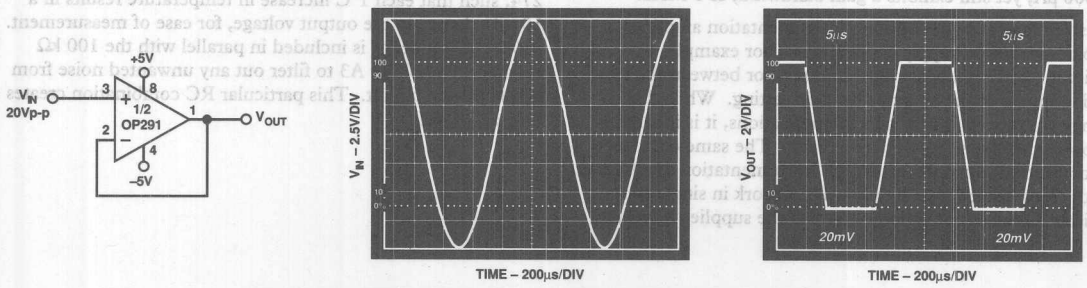

Figure 57. OP291/OP491 Output Voltage Phase Reversal Behavior

Single +3 V Supply, Instrumentation Amplifier

The OP291's low supply current and low voltage operation make it ideal for battery powered applications such as the instrumentation amplifier shown in Figure 59. The circuit utilizes the classic two op amp instrumentation amplifier topology, with four resistors to set the gain. The equation is simply that of a noninverting amplifier as shown in the figure. The two resistors labeled R1 should be closely matched to each other as well as both resistors labeled R2 to ensure good common-mode rejection performance. Resistor networks ensure the closest matching as well as matched drifts for good temperature stability. Capacitor C1 is included to limit the bandwidth and, therefore, the noise in sensitive applications. The value of this capacitor should be adjusted depending on the desired closed-loop bandwidth of the instrumentation amplifier. The RC combination creates a pole at a frequency equal to $1/(2\pi \times R1C1)$. If AC-CMRR is critical, than a matched capacitor to C1 should be included across the second resistor labeled R1.

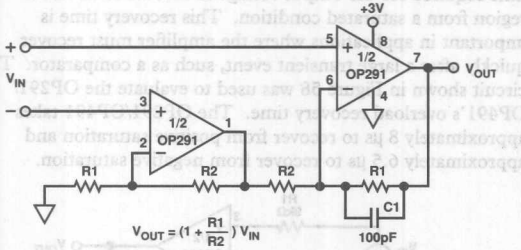

Figure 59. Single +3 V Supply Instrumentation Amplifier

Because the OP291 accepts rail-to-rail inputs, the input common-mode range includes both ground and the positive supply of 3 V. Furthermore, the rail-to-rail output range ensures the widest signal range possible and maximizes the dynamic range of the system. Also, with its low supply current of 300 µA/device, this circuit consumes a quiescent current of only 600 µA, yet still exhibits a gain bandwidth of 3 MHz.

A question may arise about other instrumentation amplifier topologies for single supply applications. For example, a variation on this topology adds a fifth resistor between the two inverting inputs of the op amps for gain setting. While that topology works well in dual supply applications, it is inherently not appropriate for single supply circuits. The same could be said for the traditional three op amp instrumentation amplifier. In both cases, the circuits simply will not work in single supply situations unless a false ground between the supplies is created.

The circuit in Figure 60. uses three op amps of the OP491 to develop a bridge configuration for an RTD amplifier that operates from a single +5 V supply. The circuit takes advantage of the OP491's wide output swing range to generate a high bridge excitation voltage of 3.9 V. In fact, because of the rail-to-rail output swing, this circuit will work with supplies as low as 4.0 V. Amplifier A1 servos the bridge to create a constant excitation current in conjunction with the AD589, a 1.235 V precision reference. The op amp maintains the reference voltage across the parallel combination of the 6.19 kΩ and 2.55 MΩ resistor, which generates a 200 µA current source. This current splits evenly and flows through both halves of the bridge. Thus, 100 µA flows through the RTD to generate an output voltage based on its resistance. A 3-wire RTD is used to balance the line resistance in both 100 Ω legs of the bridge to improve accuracy.

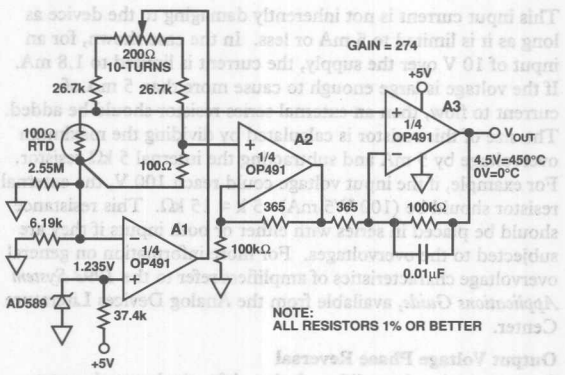

Figure 60. Single Supply RTD Amplifier

Amplifiers A2 and A3 are configured in the two op amp IA discussed above. Their resistors are chosen to produce a gain of 274, such that each 1°C increase in temperature results in a 10 mV change in the output voltage, for ease of measurement. A 0.01 µF capacitor is included in parallel with the 100 kΩ resistor on amplifier A3 to filter out any unwanted noise from this high gain circuit. This particular RC combination creates a pole at 1.6 kHz.

A +2.5 V Reference from a +3 V Supply

In many single-supply applications, the need for a 2.5 V reference often arises. Many commercially available monolithic 2.5 V references require at least a minimum operating supply voltage of 4 V. The problem is exacerbated when the minimum operating system supply voltage is + 3 V. The circuit illustrated in Figure 61 is an example of a +2.5 V that operates from a single +3 V supply. The circuit takes advantage of the OP291's rail-to-rail input and output voltage ranges to amplify an AD589's 1.235 V output to +2.5 V. The OP291's low TCV_{OS} of 1 µV/°C helps to maintain an output voltage temperature coefficient of less than 200 ppm/°C. The circuit's overall temperature coefficient is dominated by R2 and R3's temperature coefficient. Lower tempco resistors are recommended. The entire circuit draws less than 420 µA from a +3 V supply at 25°C.

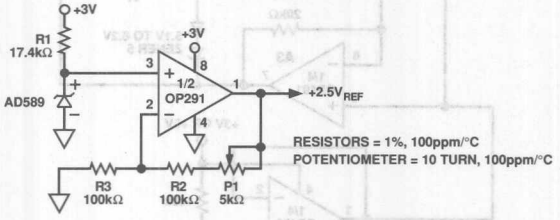

Figure 61. A +2.5 V Reference that Operates on a Single +3 V Supply

+5 V Only, 12-Bit DAC Swings Rail-to-Rail

The OP291 or OP491 are ideal for use with a CMOS DAC to generate a digitally controlled voltage with a wide output range. Figure 62 shows the DAC8043 used in conjunction with the AD589 to generate a voltage output from 0 V to 1.23 V. The DAC is actually operated in "voltage switching" mode where the reference is connected to the current output, I_{OUT}, and the output voltage is taken from the V_{REF} pin. This topology is inherently noninverting as opposed to the classic current output mode, which is inverting and, therefore, unsuitable for single supply.

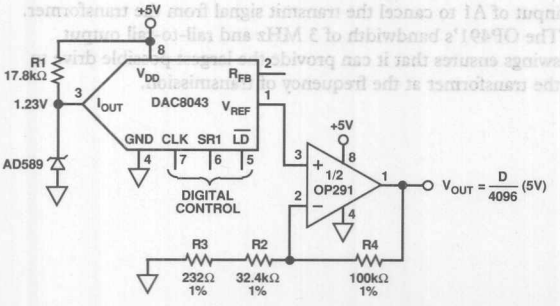

Figure 62. +5 V Only, 12-Bit DAC Swings Rail-to-Rail

The OP291 serves two functions. First, it is required to buffer the high output impedance of the DAC's V_{REF} pin, which is on the order of 10 kΩ. The op amp provides a low impedance output to drive any following circuitry. Secondly, the op amp amplifies the output signal to provide a rail-to-rail output swing. In this particular case, the gain is set to 4.1 to generate a 5.0 V output when the DAC is at full scale. If other output voltage ranges are needed, such as 0 to 4.095, the gain can easily be adjusted by altering the value of the resistors.

A High Side Current Monitor

In the design of power supply control circuits, a great deal of design effort is focused on ensuring a pass transistor's long-term reliability over a wide range of load current conditions. As a result, monitoring and limiting device power dissipation is of prime importance in these designs. The circuit illustrated in Figure 63 is an example of a +5 V, single-supply high side current monitor that can be incorporated into the design of a voltage regulator with fold-back current limiting or a high current power supply with crowbar protection. This design uses an OP291's rail-to-rail input voltage range to sense the voltage drop across a 0.1 Ω current shunt. A p-channel MOSFET used as the feedback element in the circuit converts the op amp's differential input voltage into a current. This current is then applied to R2 to generate a voltage that is a linear representation of the load current. The transfer equation for the current monitor is given by:

$$Monitor\ Output = R2 \times \left(\frac{R_{SENSE}}{R1}\right) \times I_L$$

For the element values shown, the Monitor Output's transfer characteristic is 2.5 V/A.

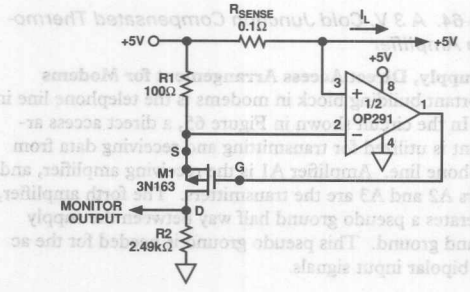

Figure 63. A High-Side Load Current Monitor

A +3 V, Cold Junction Compensated Thermocouple Amplifier
The OP291's low supply operation makes it ideal for +3 V battery powered applications such as the thermocouple amplifier shown in Figure 64. The K-type thermocouple terminates in an isothermal block where the junctions' ambient temperature is continuously monitored using a simple 1N914 diode. The diode corrects the thermal EMF generated in the junctions by feeding a small voltage, scaled by the 1.5 MΩ and 475 Ω resistors, to the op amp.

To calibrate this circuit, immerse the thermocouple measuring junction in a 0°C ice bath, and adjust the 500 Ω pot to zero volts out. Next, immerse the thermocouple in a 250°C temperature bath or oven and adjust the Scale Adjust pot for an output voltage of 2.50 V. Within this temperature range, the K-type thermocouple is accurate to within ±3°C without linearization.

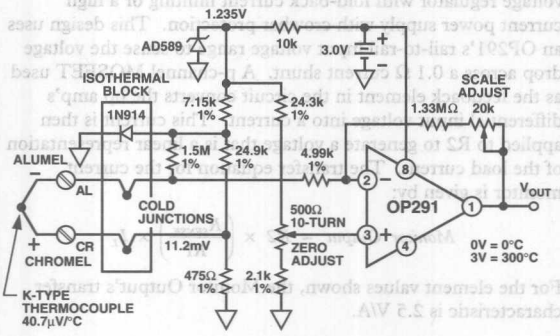

Figure 64. A 3 V, Cold Junction Compensated Thermocouple Amplifier

Single Supply, Direct Access Arrangement for Modems
An important building block in modems is the telephone line interface. In the circuit shown in Figure 65, a direct access arrangement is utilized for transmitting and receiving data from the telephone line. Amplifier A1 is the receiving amplifier, and amplifiers A2 and A3 are the transmitters. The forth amplifier, A4, generates a pseudo ground half way between the supply voltage and ground. This pseudo ground is needed for the ac coupled bipolar input signals.

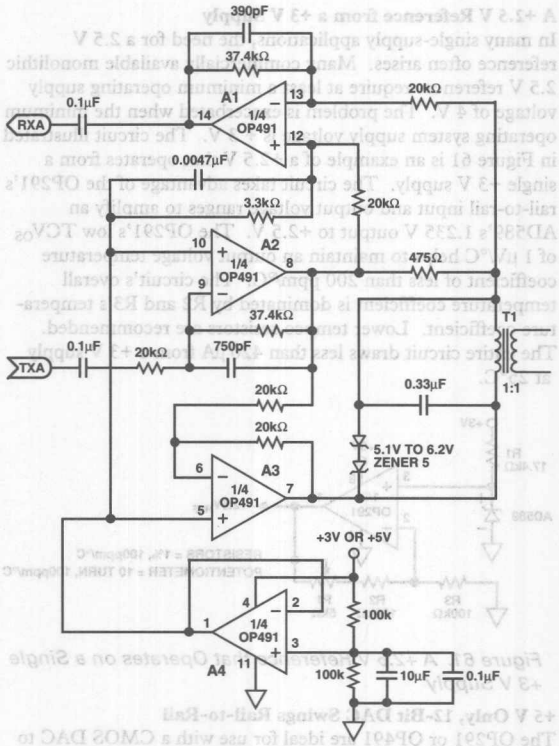

Figure 65. Single Supply Direct Access Arrangement for Modems

The transmit signal, TXA, is inverted by A2 and then re-inverted by A3 to provide a differential drive to the transformer, where each amplifier supplies half the drive signal. This is needed because of the smaller swings associated with a single supply as opposed to a dual supply. Amplifier A1 provides some gain for the received signal, and it also removes the transmit signal present at the transformer from the receive signal. To do this, the drive signal from A2 is also fed to the noninverting input of A1 to cancel the transmit signal from the transformer. The OP491's bandwidth of 3 MHz and rail-to-rail output swings ensures that it can provide the largest possible drive to the transformer at the frequency of transmission.

A +3 V, 50 Hz/60 Hz Active Notch Filter with False Ground

To process ac signals in a single-supply system, it is often best to use a false-ground biasing scheme. A circuit that uses this approach is illustrated in Figure 66. In this circuit, a false-ground circuit biases an active notch filter used to reject 50 Hz/60 Hz power line interference in portable patient monitoring equipment. Notch filters are quite commonly used to reject power line frequency interference which oftentimes obscures low frequency physiological signals, such as heart rates, blood pressure readings, EEGs, EKGs, et cetera. This notch filter effectively squelches 60 Hz pickup at a filter Q of 0.75. Substituting 3.16 kΩ resistors for the 2.67 kΩ resistors in the twin-T section (R1 through R5) configures the active filter to reject 50 Hz interference.

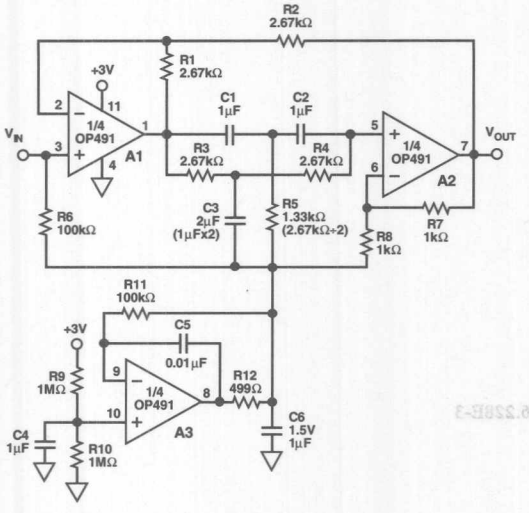

Figure 66. A +3 V Single-Supply, 50 Hz/60 Hz Active Notch Filter with False Ground

Amplifier A3 is the heart of the false-ground bias circuit. It simply buffers the voltage developed by R9 and R10 and is the reference for the active notch filter. Since the OP491 exhibits a rail-to-rail input common-mode range, R9 and R10 are chosen to split the +3 V supply symmetrically. An in-the-loop compensation scheme is used around the OP491 that allows the op amp to drive C6, a 1 µF capacitor, without oscillation. C6 maintains a low impedance ac ground over the operating frequency range of the filter.

The filter section uses a pair of OP491s in a twin-T configuration whose frequency selectivity is very sensitive to the relative matching of the capacitors and resistors in the twin-T section. Mylar is the material of choice for the capacitors, and the relative matching of the capacitors and resistors determines the filter's passband symmetry. Using 1% resistors and 5% capacitors produces satisfactory results.

Single-Supply Half-Wave and Full-Wave Rectifiers

An OP291/OP491 configured as a voltage follower operating on a single supply can be used as a simple half-wave rectifier in low-frequency (<2 kHz) applications. A full-wave rectifier can be configured with a pair of OP291s as illustrated in Figure 67. The circuit works in the following way: When the input signal is above 0 V, the output of amplifier A1 follows the input signal. Since the noninverting input of amplifier A2 is connected to A1's output, op amp loop control forces the A2's inverting input to the same potential. The result is that both terminals of R1 are equipotential; i.e., no current flows. Since there is no current flow in R1, the same condition exists upon R2; thus, the output of the circuit tracks the input signal. When the input signal is below 0 V, the output voltage of A1 is forced to 0 V. This condition now forces A2 to operate as an inverting voltage follower because the noninverting terminal of A2 is at 0 V as well. The output voltage at $V_{OUT}A$ is then a full-wave rectified version of the input signal. If needed, a buffered, half-wave rectified version of the input signal is available at $V_{OUT}B$.

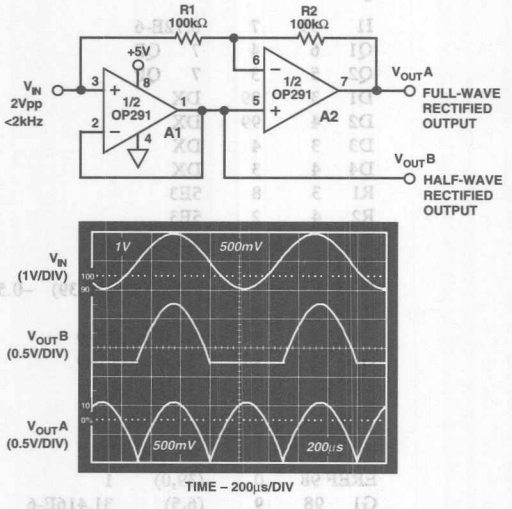

Figure 67. Single-Supply Half-Wave and Full-Wave Rectifiers Using an OP291

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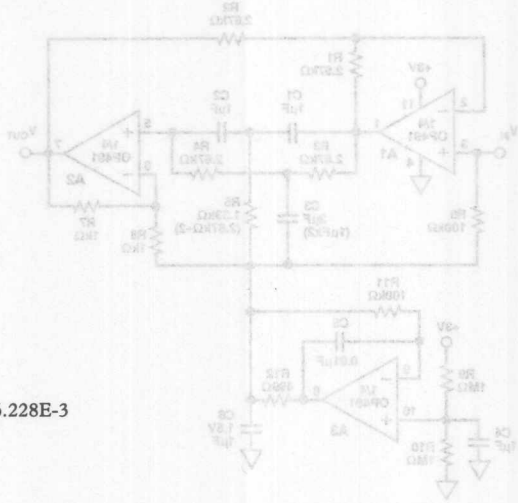
```
*
* Refer to "README.DOC" file for License Statement. Use of
* this model indicates your acceptance of the terms and pro-
* visions in the License Statement.
*
* Node assignments
*                  noninverting input
*                  |  inverting input
*                  |  |  positive supply
*                  |  |  |  negative supply
*                  |  |  |  |  output
*                  |  |  |  |  |
.SUBCKT OP491      1  2  99 50 45
*
* INPUT STAGE
*
I1    99   7    8.12E-6
Q1    6    4    7    QP
Q2    5    3    7    QP
D1    3    99   DX
D2    4    99   DX
D3    3    4    DX
D4    4    3    DX
R1    3    8    5E3
R2    4    2    5E3
R3    5    50   6.37E3
R4    6    50   6.37E3
EOS   8    1    POLY(1)  (16,39)   –0.5E-3   316.228E-3
IOS   3    4    10E-9
GB1   3    98   (21,98)  100E-9
GB2   4    98   (21,98)  100E-9
CIN   1    2    1E-12
*
* 1ST GAIN STAGE
*
EREF  98   0    (39,0)   1
G1    98   9    (6,5)    31.416E-6
R7    9    98   1E6
EC1   99   10   POLY(1)  (99,39)   –0.52   1
EC2   11   50   POLY(1)  (39,50)   –0.52   1
D5    9    10   DX
D6    11   9    DX
*
* 2ND GAIN STAGE AND DOMINANT POLE AT 1.25 Hz
*
G2    98   12   (9,39)    8.12E-6
R8    12   98   7.840E9
C2    12   98   16.24E-12
D7    12   13   DX
D8    14   12   DX
V1    99   13   0.58
V2    14   50   0.58
*
* COMMON-MODE STAGE
*
ECM   15   98   POLY(2) (1,39) (2,39) 0 0.5 0.5
R9    15   16   1E6
R10   16   98   10
```



```
*
* POLE AT 2.5 MHz
*
G3   98    18    (12,39) 1E-6
R11  18    98    1E6
C4   18    98    63.662E-15
*
* BIAS CURRENT-VS-COMMON-MODE VOLTAGE
*
EP   97    0     (99,0) 1
VB   99    17    1.3
RB   17    50    1E9
E3   19    0     (15,17) 16
D13  19    20    DX
R12  20    0     1E6
G4   98    21    (20,0) 1E-3
R13  21    98    5E3
D14  21    22    DY
E4   97    22    (POLY(1) (99,98) -0.765 1
*
* POLE AT 100 MHz
*
G6   98    40    (18,39) 1E-6
R20  40    98    1E6
C10  40    98    1.592E-15
*
* OUTPUT STAGE
*
RS1  99    39    109.375E3
RS2  39    50    109.375E3
RO1  99    45    41.667
RO2  45    50    41.667
G7   45    99    (99,40) 24E-3
G8   50    45    (40,50) 24E-3
G9   98    60    (45,40) 24E-3
D9   60    61    DX
D10  62    60    DX
V7   61    98    DC 0
V8   98    62    DC 0
FSY  99    50    POLY(2) V7 V8 0.247E-3  1  1
D11  41    45    DZ
D12  45    42    DZ
V5   40    41    0.131
V6   42    40    0.131
.MODEL DX D()
.MODEL DY D(IS=1E-9)
.MODEL DZ D(IS=1E-6)
.MODEL QP PNP(BF=66.667)
.ENDS
```

Dual/Quad Single Supply Operational Amplifiers

OP292/OP492

FEATURES

- Single Supply Operation: 4.5 V to 33 V
- Input Common Mode Includes Ground
- Output Swings to Ground
- High Slew Rate: 3 V/μs
- High Gain Bandwidth: 4 MHz
- Low Input Offset Voltage
- High Open-Loop Gain
- No Phase Inversion
- Low Cost

APPLICATIONS

- Disk Drives
- Mobile Phones
- Servo Controls
- Modems and Fax Machines
- Pagers
- Power Supply Monitors and Controls
- Battery Operated Instrumentation

GENERAL DESCRIPTION

The OP292/OP492 are low cost general purpose dual and quad operational amplifiers designed for single supply applications and are ideal for +5 volt systems.

Fabricated on Analog Devices' CBCMOS process, the OP292/OP492 series has a PNP input stage that allows the input voltage range to include ground. A BiCMOS output stage enables the output to swing to ground while sinking current.

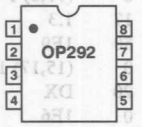
The OP292/OP492 series is unity-gain stable and features an outstanding combination of speed and performance for single or dual supply operation. The OP292/OP492 provide high slew rate, high bandwidth, with open-loop gain exceeding 40,000 and offset voltage under 800 μV (OP292) and 1 mV (OP492). With these combinations of features and low supply current, the OP292/OP492 series is an excellent choice for battery operated applications.

The OP292/OP492 series performance is specified for single or dual supply voltage operation over the extended industrial temperature range (−40°C to +125°C).

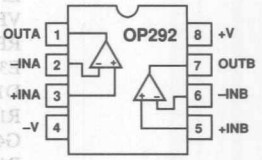
Package options for the OP292 and OP492 include plastic DIP, SO-8 (OP292) and SO-14.

PIN CONNECTIONS

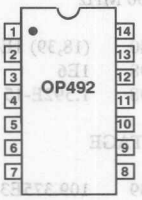
8-Lead Narrow-Body SO
(S Suffix)



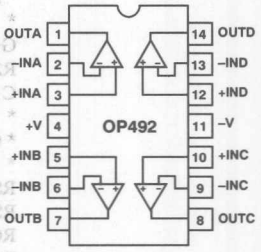
8-Lead Epoxy DIP
(P Suffix)



14-Lead Narrow-Body SO
(S Suffix)



14-Lead Epoxy DIP
(P Suffix)



SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5 V, V_{CM} = 0 V, V_O = +2 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
OP292				0.1	0.8	mV
		−40°C ≤ T_A ≤ +85°C		0.3	1.2	mV
		−40°C ≤ T_A ≤ +125°C		0.5	2.5	mV
OP492	V_{OS}			0.1	1	mV
		−40°C ≤ T_A ≤ +85°C		0.3	1.5	mV
		−40°C ≤ T_A ≤ +125°C		0.5	2.5	mV
Input Bias Current	I_B			450	700	nA
		−40°C ≤ T_A ≤ +85°C		0.75	2.5	µA
		−40°C ≤ T_A ≤ +125°C		3.0	5.0	µA
Input Offset Current	I_{OS}			7	50	nA
		−40°C ≤ T_A ≤ +85°C		100	700	nA
		−40°C ≤ T_A ≤ +125°C		0.4	1.2	µA
Input Voltage Range			0		4.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 4.0 V	75	95		dB
		−40°C ≤ T_A ≤ +85°C	70	93		dB
		−40°C ≤ T_A ≤ +125°C	65	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 4 V	25	200		V/mV
		−40°C ≤ T_A ≤ +85°C	10	100		V/mV
		−40°C ≤ T_A ≤ +125°C	5	50		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		2	10	µV/°C
Long Term V_{OS} Drift	$\Delta V_{OS}/\Delta t$	Note 1		1		µV/Month
Bias Current Drift	$\Delta I_B/\Delta T$	−40°C ≤ T_A ≤ +85°C		6		pA/°C
		−40°C ≤ T_A ≤ +125°C		400		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$	−40°C ≤ T_A ≤ +85°C		1.5		pA/°C
		−40°C ≤ T_A ≤ +125°C		2		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing						
High	V_{OUT}	R_L = 100 kΩ to GND				
		−40°C ≤ T_A ≤ +125°C	4.0	4.3		V
		R_L = 2 kΩ to GND	3.8	4.1		V
		−40°C ≤ T_A ≤ +125°C	3.7	3.9		V
Low	V_{OUT}	R_L = 100 kΩ to V+		8	20	mV
		−40°C ≤ T_A ≤ +125°C		12	20	mV
		R_L = 2 kΩ to V+		280	450	mV
		−40°C ≤ T_A ≤ +125°C		300	550	mV
Short Circuit Current Limit	I_{SC}		5	8		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4.5 V to +30 V, V_O = 2 V	75	95		dB
		−40°C ≤ T_A ≤ +125°C	70	90		dB
Supply Current Per Amp	I_{SY}	V_O = 2 V				
OP292, OP492				0.8	1.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		3		V/µs
		−40°C ≤ T_A ≤ +125°C	1	2		V/µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	ϕ_m			75		Degrees
Channel Separation	CS	f_O = 1 kHz		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		25		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		15		nV/√Hz
Current Noise Density	i_n			0.7		pA/√Hz

NOTES

[1]Long term offset voltage drift is guaranteed by 1000 hours life test performed on three independent wafer lots at +125°C with LTPD of 1.3.

Specifications subject to change without notice.

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ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
OP292				1.0	2.0	mV
		−40°C ≤ T_A ≤ +85°C		1.2	2.5	mV
		−40°C ≤ T_A ≤ +125°C		1.5	3	mV
OP492				1.4	2.5	mV
		−40°C ≤ T_A ≤ +85°C		1.7	2.8	mV
		−40°C ≤ T_A ≤ +125°C		2	3	mV
Input Bias Current	I_B			375	700	nA
		−40°C ≤ T_A ≤ +125°C		0.5	1	µA
Input Offset Current	I_{OS}			7	50	nA
		−40°C ≤ T_A ≤ +85°C		20	100	nA
		−40°C ≤ T_A ≤ +125°C		0.4	1.2	µA
Input Voltage Range		Note 1	−11		11	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11 V	78	100		dB
		−40°C ≤ T_A ≤ +125°C	75	95		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = ±10 V	25	120		V/mV
		−40°C ≤ T_A ≤ +85°C	10	75		V/mV
		−40°C ≤ T_A ≤ +125°C	5	60		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		4	10	µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$	−40°C ≤ T_A ≤ +125°C		3		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ to GND	±11	±12.2		V
		−40°C ≤ T_A ≤ +125°C	±10	±11		V
		R_L = 100 kΩ to GND	±13.8	±14.3		V
		−40°C ≤ T_A ≤ +125°C	±13.5	±14.0		mV
Short Circuit Current Limit	I_{SC}	Short Circuit to GND	8	10.5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.25 V to ±15 V	75	86		dB
		−40°C ≤ T_A ≤ +125°C	70	83		dB
Supply Current Per Amp	I_{SY}	V_O = 0 V				
OP292, OP492				1	1.4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ	2.5	4		V/µs
		−40°C ≤ T_A ≤ +125°C	2	3		V/µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	ϕ_m			75		Degrees
Channel Separation	CS	f_O = 1 kHz		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		25		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		15		nV/√Hz
Current Noise Density	i_n			0.7		pA/√Hz

NOTES

[1]Input voltage range is guaranteed by CMRR tests.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = +5.0 V, V_{CM} = 2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		±600	μV max
Input Bias Current	I_B		700	nA max
Input Offset Current	I_{OS}		50	nA max
Input Voltage Range[1]	V_{CM}		0/4	V min/V max
Common-Mode Rejection	CMRR	V_{CM} = 0 V to 4.0 V	75	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±15 V	75	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 4 V	25	V/mV min
Output Voltage	V_O	R_L = 2 kΩ	3.8	V min
Supply Current per Amp OP292, OP492	I_{SY}	V_O = 0 V, R_L = Open	1.2	mA max

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +33 V
Input Voltage[2] . . . . . −15 V to +14 V
Differential Input Voltage[2] V
Output Short-Circuit Duration . . . . . UNLIMITED
Storage Temperature Range
P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
OP292/OP492 P, S . . . . . −40°C to +125°C
Junction Temperature Range
P, S Package . . . . . −65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
8-Pin SO (S)	158	43	°C/W
14-Pin SO (S)	120	36	°C/W

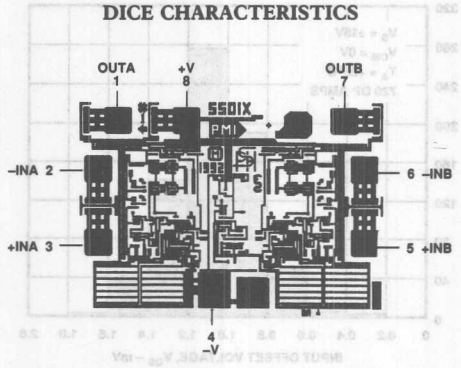
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than +36 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

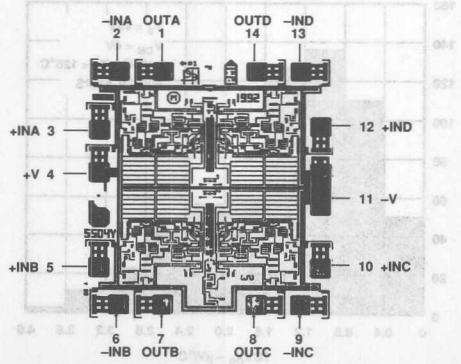
Model	Temperature Range	Package Option*
OP292GP	−40°C to +125°C	N-8
OP292GS	−40°C to +125°C	SO-8
OP492GP	−40°C to +125°C	N-14
OP492GS	−40°C to +125°C	SO-14
OP292/492GBC	+25°C	DICE

*For outline information see Package Information section.

DICE CHARACTERISTICS



OP292 Die Size 0.040 × 0.057 Inch, 2,280 Sq. Mils Substrate Connected to V+, Number of Transistors: Bipolar 47, MOSFET 5.



OP492 Die Size 0.057 × 0.068 Inch, 3,876 Sq. Mils Substrate Connected to V+, Number of Transistors: Bipolar 91, MOSFET 9.

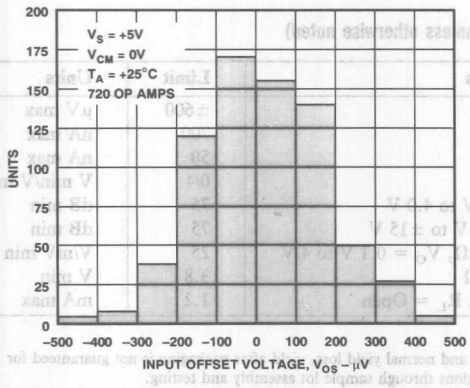


Figure 1. OP292 Input Offset Voltage Distribution @ +5 V

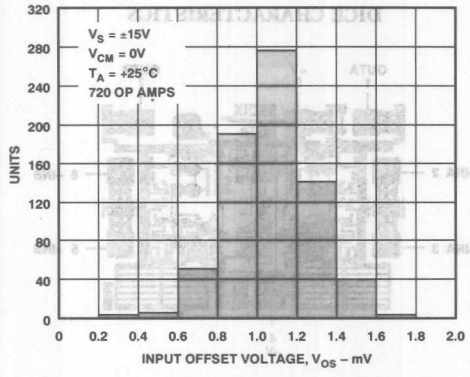


Figure 2. OP292 Input Offset Voltage Distribution @ ±15 V

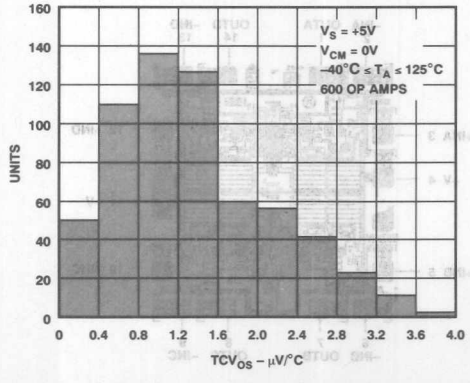


Figure 3. OP292 Temperature Drift (TCV_{OS}) Distribution @ +5 V

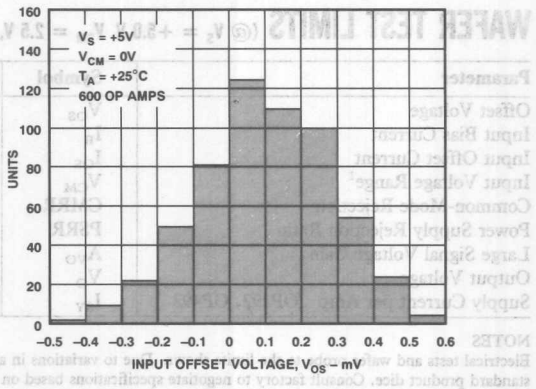


Figure 4. OP492 Input Offset Voltage Distribution @ +5 V

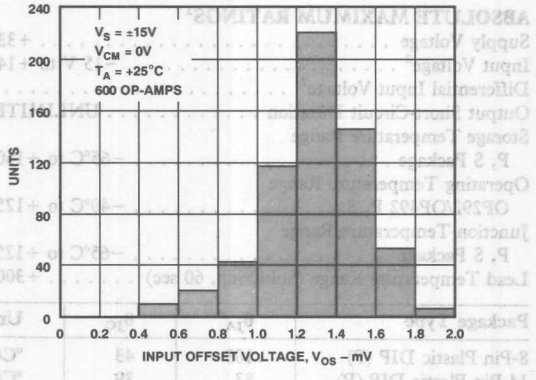


Figure 5. OP492 Input Offset Voltage Distribution @ ±15 V

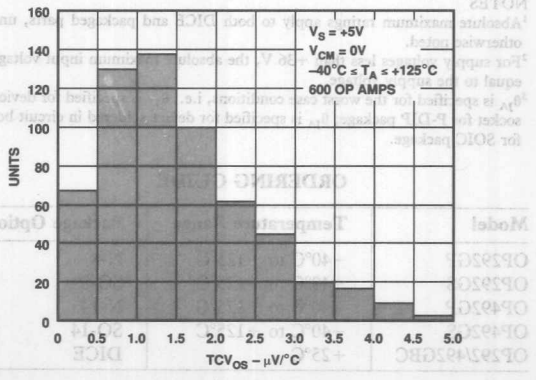


Figure 6. OP492 Temperature Drift (TCV_{OS}) Distribution @ +5 V

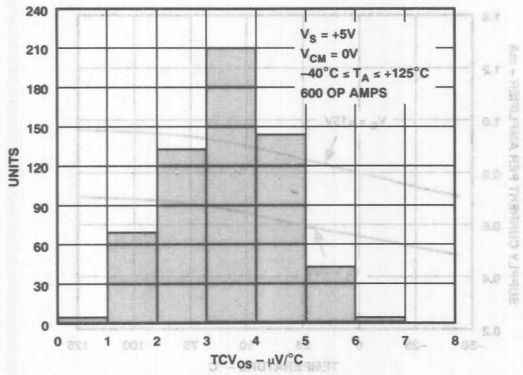


Figure 7. OP292 Temperature Drift (TCV_{OS}) Distribution @ ±15 V

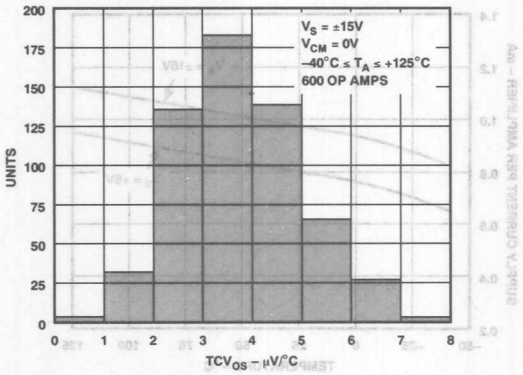


Figure 10. OP492 Temperature Drift (TCV_{OS}) Distribution @ ±15 V

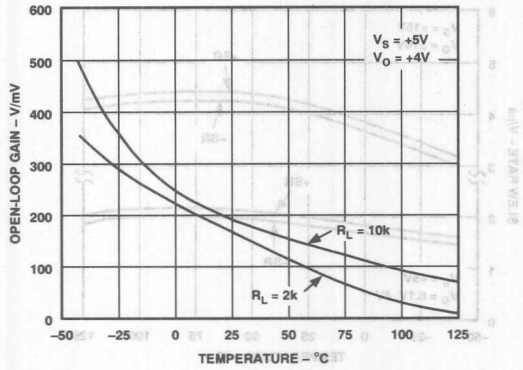


Figure 8. OP292 Open-Loop Gain vs. Temperature @ +5 V

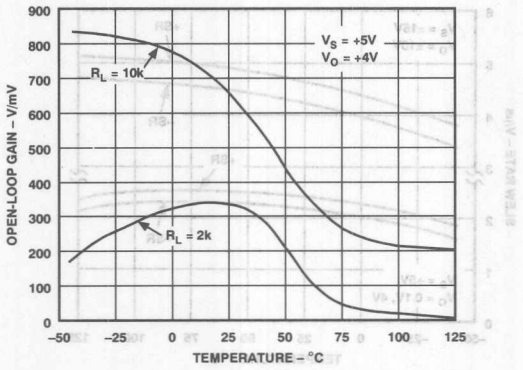


Figure 11. OP492 Open-Loop Gain vs. Temperature @ +5 V

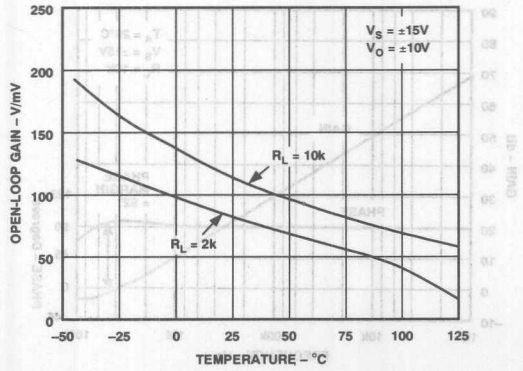


Figure 9. OP292 Open-Loop Gain vs. Temperature @ ±15 V

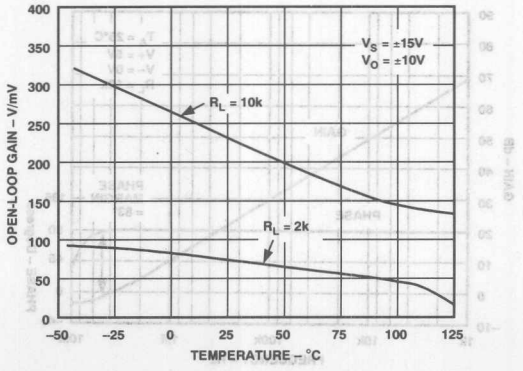


Figure 12. OP492 Open-Loop Gain vs. Temperature @ ±15 V

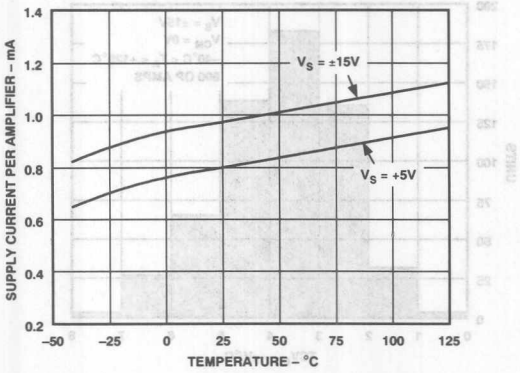


Figure 13. OP292 Supply Current per Amplifier vs. Temperature

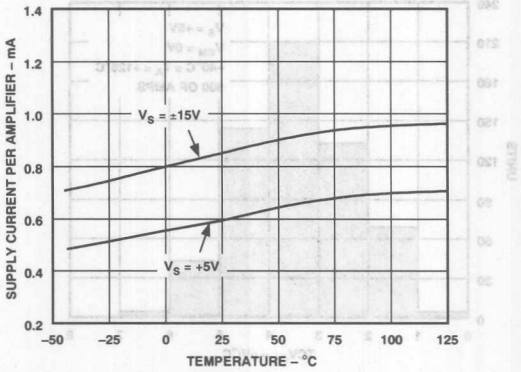


Figure 16. OP492 Supply Current per Amplifier vs. Temperature

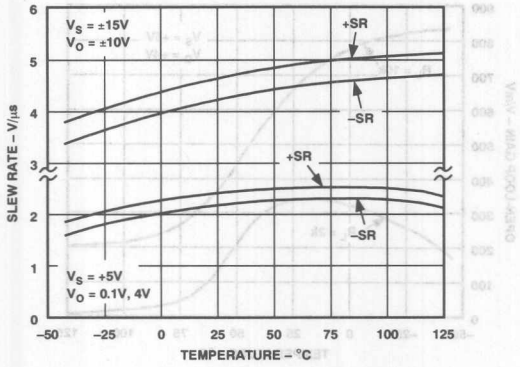


Figure 14. OP292 Slew-Rate vs. Temperature

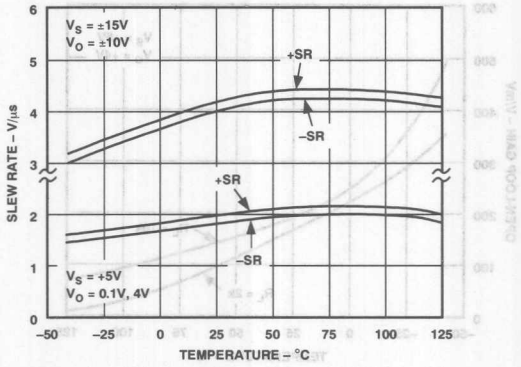


Figure 17. OP492 Slew-Rate vs. Temperature

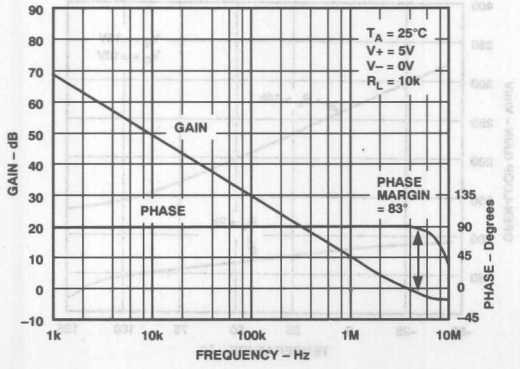


Figure 15. OP292/OP492 Open-Loop Gain and Phase vs. Frequency @ +5 V

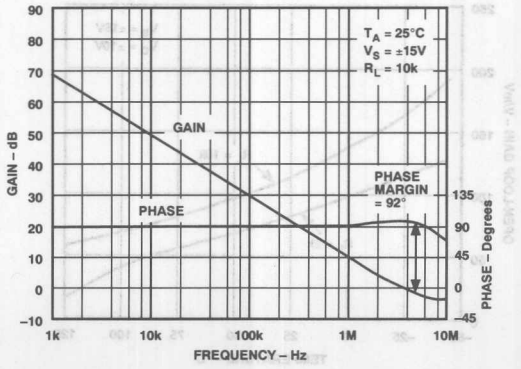


Figure 18. OP292/OP492 Open-Loop Gain/Phase vs. Frequency @ ±15 V

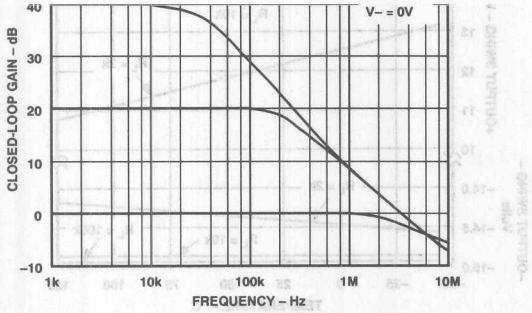


Figure 19. OP292/OP492 Closed-Loop Gain/Phase vs. Frequency @ +5 V

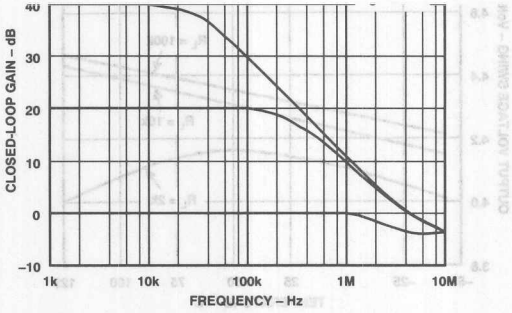


Figure 22. OP292/OP492 Closed-Loop Gain/Phase vs. Frequency @ ±15 V

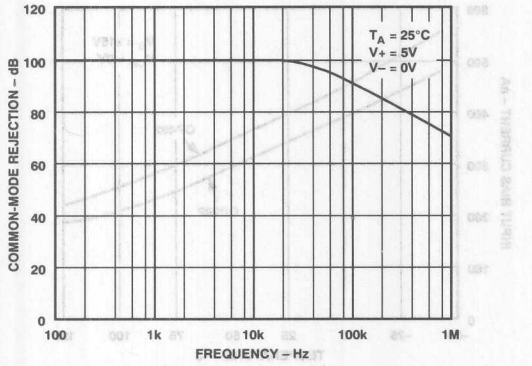


Figure 20. OP292/OP492 CMR vs. Frequency @ +5 V

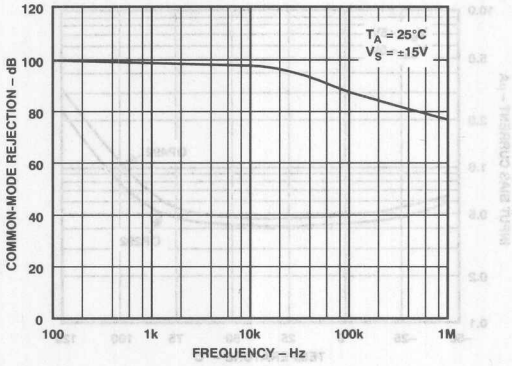


Figure 23. OP292/OP492 CMR vs. Frequency @ ±15 V

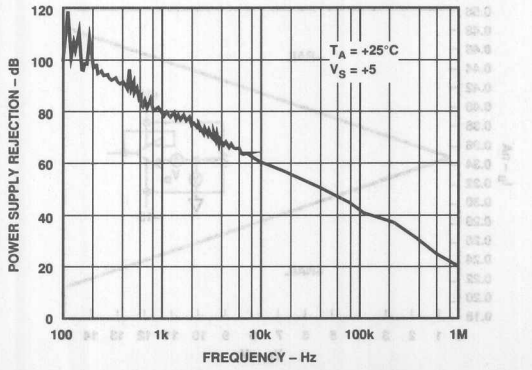


Figure 21. OP292/OP492 PSR vs. Frequency @ +5 V

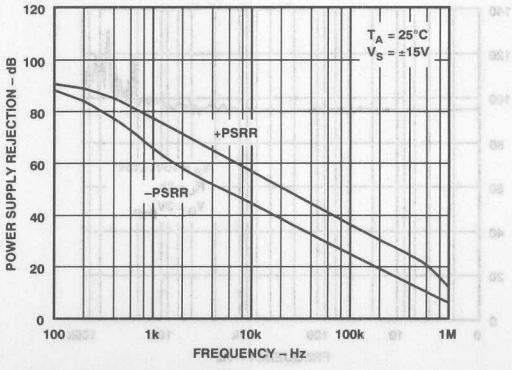


Figure 24. OP292/OP492 PSR vs. Frequency @ ±15 V

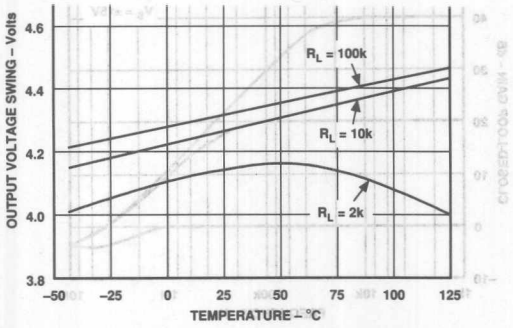


Figure 25. OP292/OP492 V_{OUT} Swing vs. Temperature @ +5 V

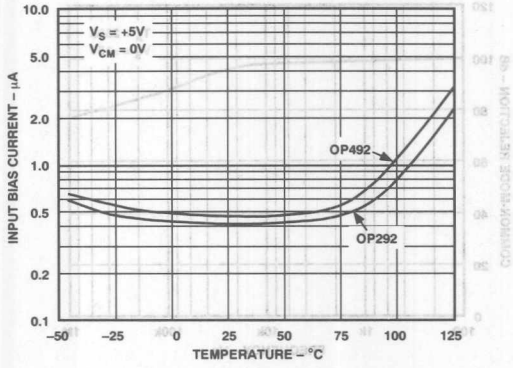


Figure 26. OP292/OP492 Input Bias Current vs. Temperature @ +5 V

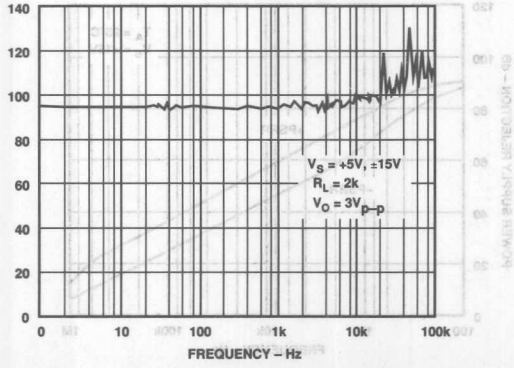


Figure 27. OP292/OP492 Channel Separation

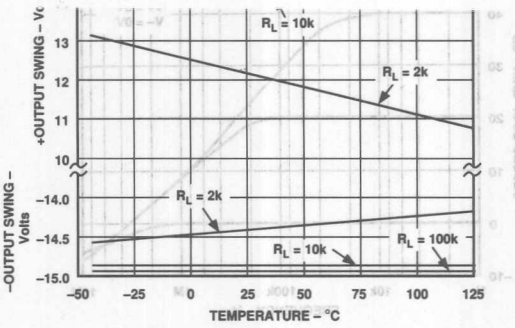


Figure 28. OP292/OP492 V_{OUT} Swing vs. Temperature @ ±15 V

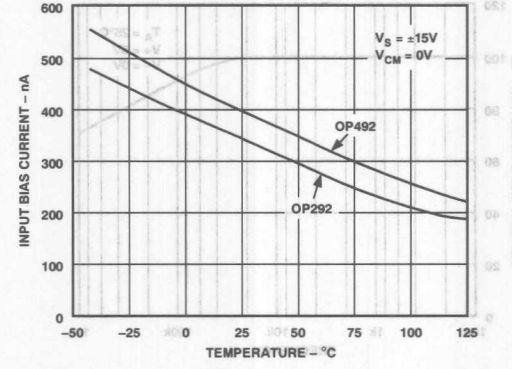


Figure 29. OP292/OP492 Input Bias Current vs. Temperature @ ±15 V

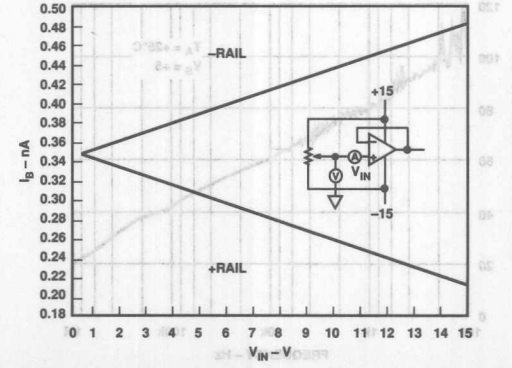


Figure 30. OP292/OP492 I_B Current vs. Common Mode Voltage

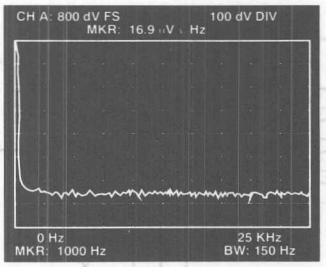


Figure 31. Voltage Noise Density

APPLICATION INFORMATION

PHASE REVERSAL

The OP492 has built-in protection against phase reversal when the input voltage goes to either supply rail. In fact it is safe for the input to exceed either supply rail by up to 0.6 V with no risk of phase reversal. However, the input should not go beyond the positive supply rail by more than 0.9 V, otherwise the output will reverse phase. If this condition can occur, the problem can be fixed by adding a 5 kΩ current limiting resistor in series with the input pin. With this addition, the input can go to more than 5 V beyond the positive rail without phase reversal.

An input voltage that is as much as 5 V below the negative rail will not result in phase reversal.

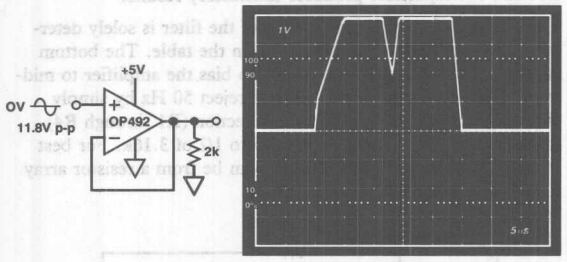


Figure 32. Output Can Reverse Phase If Input Exceeds the Positive Supply (V+) by More Than 0.9 V

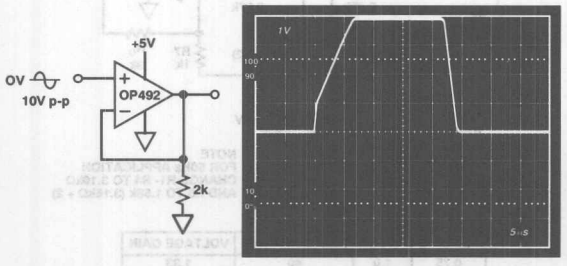


Figure 33. No Negative Rail Phase Reversal, Even with Input Signal at 5 V Below Ground

Power Supply Considerations

The OP292/OP492 are designed to operate equally well at single +5 V or ±15 V supplies. The lowest supply voltage recommended is 4.5 V.

It is a good design practice to bypass the supply pins with a 0.1 µF ceramic capacitor. It helps improve filtering of high frequency noise.

For dual supply operation, the negative supply (V−) must be applied at the same time, or before V+. If V+ is applied before V−, or in the case of a loss of V− supply, while either input is connected to ground or other low impedance source, excessive input current may result. Potentially damaging levels of input current can destroy the amplifier. If this condition can exist, simply add a 1k or larger resistor in series with the input to eliminate the problem.

TYPICAL APPLICATIONS

Direct Access Arrangement for Telephone Line Interface

Figure 34 shows a +5 V-only transmit/receive telephone line interface for a modem circuit. It allows full duplex transmission of modem signals on a transformer-coupled 600 Ω line in a differential manner. The transmit section gain can be set for the specific modem device output. Similarly the receive amplifier gain can be appropriately selected based on the modem device input requirements. The circuit operates on a single +5 V supply. The standard value resistors allow the use of a SIP packaged resistor array; this, coupled with a quad op amp in a single package, offers a compact, low part-count solution.

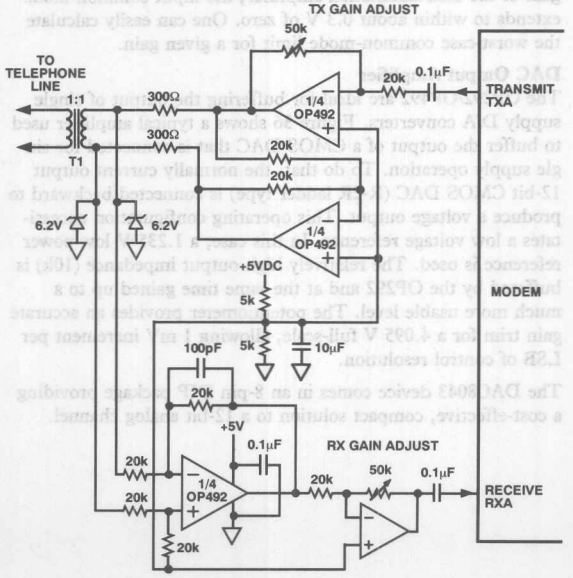


Figure 34. A Universal Direct Access Arrangement for Telephone Line Interface

9

A Single Supply Instrumentation Amplifier

A low cost single supply instrumentation amplifier can be built as shown in Figure 35. The circuit utilizes two op amps to form a high input impedance differential amplifier. Gain can be set by selecting resistor R_G which can be calculated using the transfer function equation. Normally, $V_{REFERENCE}$ is set to 0 V. Then the output voltage is a function of the gain times the differential input voltage. However, the output can be offset by setting $V_{REFERENCE}$ from 0 V to 4 V, as long as the input common-mode voltage of the amplifier is not exceeded.

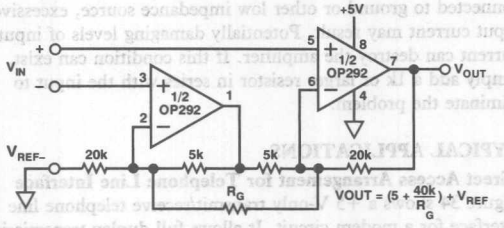


Figure 35. A Single Supply Instrumentation Amplifier

In this configuration, while the output can swing to near zero volts, one needs to be careful because the input's common-mode voltage range cannot operate to zero volts. This is because of the limitation of the circuit configuration where the first amplifier must be able to swing below ground in order to attain a 0 V common-mode voltage, which it cannot do. Depending on the gain of the instrumentation amplifier, the input common-mode extends to within about 0.3 V of zero. One can easily calculate the worst-case common-mode limit for a given gain.

DAC Output Amplifier

The OP292/OP492 are ideal for buffering the output of single supply D/A converters. Figure 36 shows a typical amplifier used to buffer the output of a CMOS DAC that is connected for single supply operation. To do that, the normally current output 12-bit CMOS DAC (R-2R ladder type) is connected backward to produce a voltage output. This operating configuration necessitates a low voltage reference. In this case, a 1.235 V low power reference is used. The relatively high output impedance (10k) is buffered by the OP292 and at the same time gained up to a much more usable level. The potentiometer provides an accurate gain trim for a 4.095 V full-scale, allowing 1 mV increment per LSB of control resolution.

The DAC8043 device comes in an 8-pin DIP package providing a cost-effective, compact solution to a 12-bit analog channel.

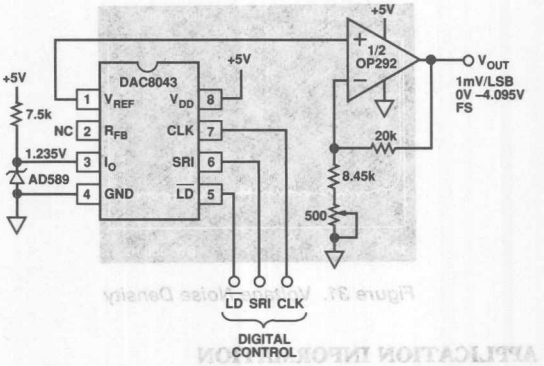
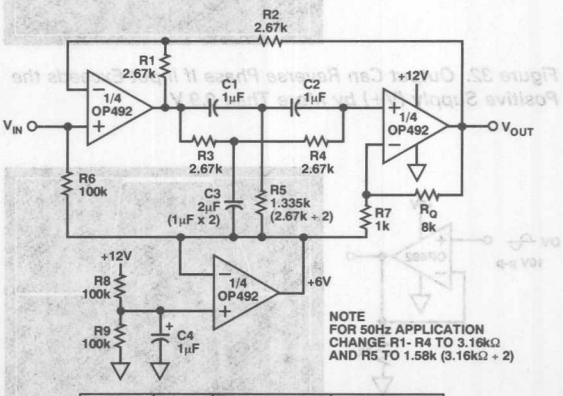


Figure 36. A 12-Bit Single-Supply DAC With Serial Bus Control

A 50 Hz/60 Hz Single-Supply Notch Filter

Figure 37 shows a notch filter that achieves nearly 30 dB of 60 Hz rejection while powered by only a single 12 V supply. The circuit also works well on +5 V systems. The filter utilizes a twin-T configuration whose frequency selectivity depends heavily on the relative matching of the capacitors and resistors in the twin-T section. Mylar is a good choice for the twin-T's capacitors, and the relative matching of the capacitors and resistors determines the filter's passband symmetry. Using 1% resistors and 5% capacitors produces satisfactory results.

The amount of rejection and the Q of the filter is solely determined by one resistor, and is shown in the table. The bottom amplifier is used to split the supply to bias the amplifier to mid-level. The circuit can be modified to reject 50 Hz by simply changing the resistors in the twin-T section (R1 through R4) from 2.67k to 3.16k, and change R5 to 1/2 of 3.16k. For best results, the common value resistors can be from a resistor array for optimum matching characteristics.



FILTER Q	R_Q (kΩ)	REJECTION (dB)	VOLTAGE GAIN
0.75	1.0	40	1.33
1.00	2.0	35	1.50
1.25	3.0	30	1.60
2.50	8.0	25	1.80
5.00	18	20	1.90
10.00	38	15	1.95

Figure 37. A Single-Supply 50 Hz/60 Hz Notch Filter

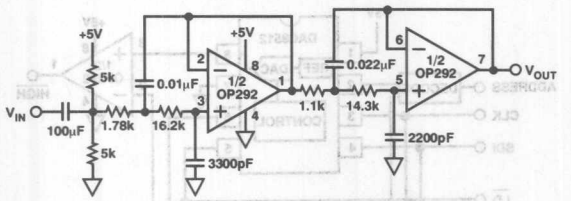


Figure 38. A 4-Pole Bessel Low Pass Filter Using Sallen-Key Topology

A 4-Pole Bessel Low-Pass Filter

The linear phase filter in Figure 38 is designed to roll off at a voiceband cutoff frequency of 3.6 kHz. The 4 poles are formed by two cascading stages of two-pole Sallen-Key filters.

A Low Cost, Linearized Thermistor Amplifier

An inexpensive thermometer amplifier circuit can be implemented using low cost thermistors. One such implementation is shown in Figure 39. The circuit measures temperature over the range of 0°C to +70°C to an accuracy of ±0.3°C as the linearization circuit works well within a narrow temperature range. However, it can measure higher temperature but at a slightly reduced accuracy. To achieve the aforementioned accuracy, the thermistor's nonlinearity must be corrected. This is done by connecting the thermistor in parallel with the 10k in the feedback loop of the first stage amplifier. A constant operating current of 281 μA is supplied by the resistor R1 with the +5 V reference from the REF-195 such that the thermistor's self-heating error is kept below 0.1°C.

In many cases, the thermistor is placed some distance from the signal conditioning circuit. Under this condition, a 0.1 μF capacitor placed across R2 will help to suppress noise pickup.

This linearization network creates an offset voltage which is corrected by summing a compensating current with potentiometer P1. The temperature dependent signal is amplified by the second stage, producing a transfer coefficient of −10 mV/°C at the output.

To calibrate, a precision decade box can be used in place of the thermistor. For 0°C trim, the decade box is set to 32.650k, and P1 is adjusted until the circuit's output reads 0 V. To trim the circuit at the full-scale temperature of 70°C, the decade box is then set to 1.752k and P2 is adjusted until the circuit reads −0.70 V.

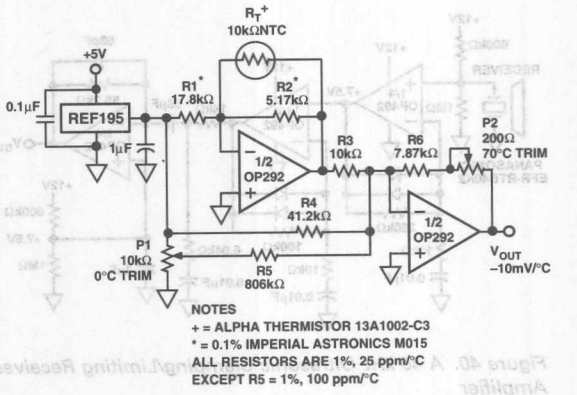


Figure 39. A Low Cost Linearized Thermistor Amplifier

A Single-Supply Ultrasonic Clamping/Limiting Receiver Amplifier

Figure 40 shows an ultrasonic receiver amplifier using the nonlinear impedance of low cost diodes to effectively control the gain for wide dynamic range. This circuit amplifies a 40 kHz ultrasonic signal through a pair of low cost clamping amplifiers before feeding a bandpass filter to extract a clean 40 kHz signal for processing.

The signal is ac-coupled into the false-ground bias node by virtue of the capacitive piezoelectric sensing element. Rather than using an amplifier to generate a supply splitting bias, the false ground voltage is generated by a low cost resistive voltage divider.

Each amplifier stage provides ac gain while passing on the dc self-bias. As long as the output signal at each stage is less than a diode's forward voltage, each amplifier has unrestricted gain to amplify low level signals. However, as the signal strength increases, the feedback diodes begin to conduct, shunting the feedback current, and thus reducing the gain. Although distorting the waveform, the diodes effectively maintain a relatively constant amplitude even with large signals that otherwise would saturate the amplifier. In addition, this design is considerably more stable than the feedback type AGC.

The overall circuit has a gain range from −2 to −400, where the inversion comes from the bandpass filter stage. Operating with a Q of 5, the filter restores a clean, undistorted signal to the output. The circuit also work well with 5 V supply systems.

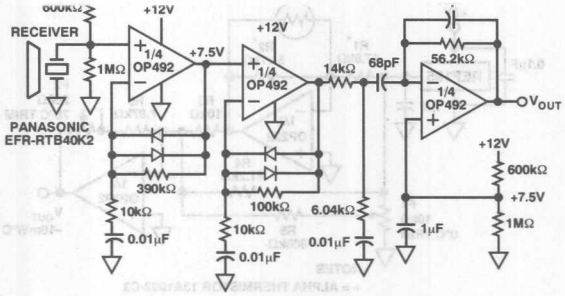


Figure 40. A 40 kHz Ultrasonic Clamping/Limiting Receiver Amplifier

Precision Single-Supply Voltage Comparator

The OP292/OP492 have excellent overload recovery characteristics, making them suitable for precision comparator applications. Figure 41 shows the saturation recovery characteristics of the OP492. The amplifier exhibits very little propagation delay. The amplifier compares a signal precisely to less than 0.5 mV offset error.

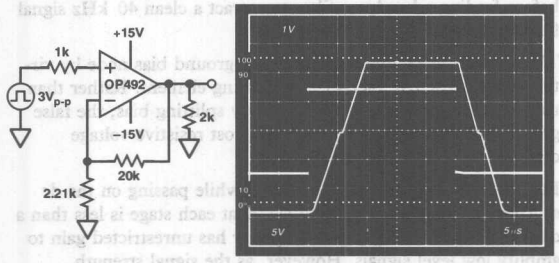


Figure 41. The OP492 Has Fast Overload Recovery for Comparator Applications

Programmable Precision Window Comparator

The OP292/OP492 can be used for precise level detection such as in test equipment where a signal is measured within a range. Figure 42 shows such an implementation. The threshold voltage level is set by a pair of 12-bit D/A converters. The DACs have serial interface thus minimizing interconnection requirements. The DAC8512 has a control resolution of 1 mV/bit. Thus for 5 V supply operation, maximum DAC output is 4.095 V. However, the OP292 will accept a maximum input of 4.0 V.

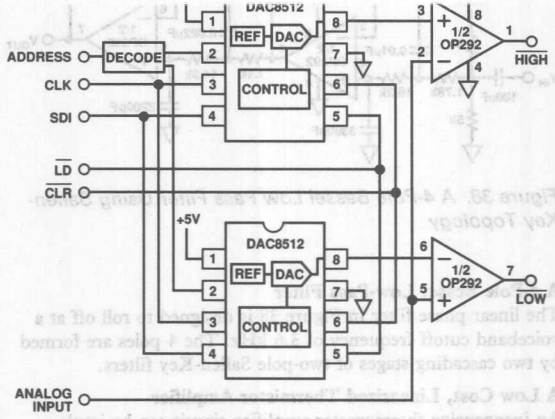


Figure 42. Programmable Window Comparator with 12-Bit Threshold Level Control

```
* OP292 SPICE Macro-model Rev. A, 6/93
*                              ARG / PMI
*
* Copyright 1993 by Analog Devices
*
* Refer to "README.DOC" file for License Statement. Use of
* this model indicates your acceptance of the terms and pro-
* visions in the License Statement.
*
* Node assignments
*                    noninverting input
*                    |  inverting input
*                    |  |  positive supply
*                    |  |  |  negative supply
*                    |  |  |  |  output
*                    |  |  |  |  |
.SUBCKT OP292        2  1  99 50 34
*
* INPUT STAGE AND POLE AT 40 MHz
*
I1      99   4    50E-6
IOS     2    1    10E-9
EOS     2    3    POLY(1) (21,30) 1.5E-3 75
CIN     1    2    3E-12
Q1      5    1    7    QP
Q2      6    3    8    QP
R3      5    50   2E3
R4      6    50   2E3
R5      4    7    966
R6      4    8    966
C1      5    6    .995E-12
*
* GAIN STAGE
*
EREF    98   0    (30,0)  1
G1      98   9    (5,6) 500E-6
R7      9    98   210.819E3
D1      9    10   DX
D2      11   9    DX
V1      99   10   .6
V2      11   50   .6
*
* ZERO/POLE AT 6 MHz/12 MHz
*
E1      12   98   (9,30)  2
R8      12   13   1
R9      13   98   1
C3      12   13   26.526E-9
*
* ZERO AT 15 MHz
*
E2      14   98   (13,30) 1E6
R10     14   15   1E6
R11     15   98   1
C4      14   15   10.610E-15
*
* COMMON MODE STAGE WITH ZERO AT 40 kHz
*
ECM     20   98   POLY(2)  (1,30)  (2,30)  0  0.5  0.5
R20     20   21   1E6
R21     21   98   1
C5      20   21   3.979E-12
```

```
*
* POLE AT 100 MHz
*
G2      98   16   (15,30) 1
R12     16   98   1
C6      16   98   1.592E-9
*
* OUTPUT STAGE
*
RS1     99   30   1E6
RS2     30   50   1E6
ISY     99   50   .44E-3
G3      31   50   POLY(1) (16,30) -1.635E-6 4E-6
R16     31   50   1E6
DCL     50   31   DZ
I2      99   32   250E-6
RCL     33   50   56
M1      32   31   50    50    MN L=9E-6 W=1000E-6 AD=15E-9 AS=15E-9
M2      34   31   50    50    MN L=9E-6 W=1000E-6 AD=15E-9 AS=15E-9
CC      31   32   14E-12
Q3      99   32   34    QNA
Q4      33   32   34    QPA
Q5      31   33   50    QNA

.MODEL QNA NPN(IS=1.19E-16 BF=253 NF=0.99 VAF=193 IKF=2.76E-3
+ ISE=2.57E-13 NE=5 BR=0.4 NR=0.988 VAR=15 IKR=1.465E-4
+ ISC=6.9E-16 NC=0.99 RB=2.0E3 IRB=7.73E-6 RBM=132.8 RE=4 RC=209
+ CJE=2.1E-13 VJE=0.573 MJE=0.364 FC=0.5 CJC=1.64E-13 VJC=0.534 MJC=0.5
+ CJS=1.37E-12 VJS=0.59 MJS=0.5 TF=0.43E-9 PTF=30)
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+ ISC=7.58E-16 NC=0.985 RB=1.52E3 IRB=1.67E-5 RBM=368.5 RE=6.31 RC=354.4
+ CJE=1.1E-13 VJE=0.745 MJE=0.33 FC=0.5 CJC=2.37E-13 VJC=0.762 MJC=0.4
+ CJS=7.11E-13 VJS=0.45 MJS=0.412 TF=1.0E-9 PTF=30)
.MODEL MN NMOS(LEVEL=3 VTO=1.3 RS=0.3 RD=0.3
+ TOX=8.5E-8 LD=1.48E-6 WD=1E-6 NSUB=1.53E16 UO=650 DELTA=10 VMAX=2E5
+ XJ=1.75E-6 KAPPA=0.8 ETA=0.066 THETA=0.01 TPG=1 CJ=2.9E-4 PB=0.837
+ MJ=0.407 CJSW=0.5E-9 MJSW=0.33)
.MODEL QP PNP(BF=61.5)
.MODEL DX D
.MODEL DZ D(BV=3.6)
.ENDS OP292
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* OP492 SPICE Macro-model                Rev. A, 6/93
*                                        ARG / PMI
*
* Copyright 1993 by Analog Devices
*
* Refer to "README.DOC" file for License Statement. Use of
* this model indicates your acceptance of the terms and pro-
* visions in the License Statement.
*
* Node assignments
*                    noninverting input
*                    |  inverting input
*                    |  |  positive supply
*                    |  |  |  negative supply
*                    |  |  |  |  output
*                    |  |  |  |  |
.SUBCKT OP492        2  1  99 50 34
*
* INPUT STAGE AND POLE AT 40 MHz
*
I1      99   4    50E-6
IOS     2    1    10E-9
EOS     2    3    POLY(1) (21,30) 1.5E-3 75
CIN     1    2    3E-12
Q1      5    1    7    QP
Q2      6    3    8    QP
R3      5    50   2E3
R4      6    50   2E3
R5      4    7    966
R6      4    8    966
C1      5    6    .995E-12
*
* GAIN STAGE
*
EREF    98   0    (30,0)   1
G1      98   9    (5,6)    500E-6
R7      9    98   210.819E3
D1      9    10   DX
D2      11   9    DX
V1      99   10   .6
V2      11   50   .6
*
* ZERO/POLE AT 6 MHz/12 MHz
*
E1      12   98   (9,30)   2
R8      12   13   1
R9      13   98   1
C3      12   13   26.526E-9
*
* ZERO AT 15 MHz
*
E2      14   98   (13,30)   1E6
R10     14   15   1E6
R11     15   98   1
C4      14   15   10.610E-15
*
* COMMON MODE STAGE WITH ZERO AT 40 kHz
*
ECM     20   98   POLY(2)   (1,30)   (2,30)   0   0.5   0.5
R20     20   21   1E6
R21     21   98   1
C5      20   21   3.979E-12
```

```
* POLE AT 100 MHz
*
G2      98   16   (15,30)   1
R12     16   98   1
C6      16   98   1.592E-9
*
* OUTPUT STAGE
*
RS1     99   30   1E6
RS2     30   50   1E6
ISY     99   50   .44E-3
G3      31   50   POLY(1)   (16,30)   -1.635E-6   4E-6
R16     31   50   1E6
DCL     50   31   DZ
I2      99   32   250E-6
RCL     33   50   56
M1      32   31   50   50   MN   L=9E-6   W=1000E-6   AD=15E-9   AS=15E-9
M2      34   31   50   50   MN   L=9E-6   W=1000E-6   AD=15E-9   AS=15E-9
CC      31   32   14E-12
Q3      99   32   34 QNA
Q4      33   32   34 QPA
Q5      31   33   50 QNA

.MODEL QNA NPN(IS=1.19E-16 BF=253 NF=0.99 VAF=193 IKF=2.76E-3
+ ISE=2.57E-13 NE=5 BR=0.4 NR=0.988 VAR=15 IKR=1.465E-4
+ ISC=6.9E-16 NC=0.99 RB=2.0E3 IRB=7.73E-6 RBM=132.8 RE=4 RC=209
+ CJE=2.1E-13 VJE=0.573 MJE=0.364 FC=0.5 CJC=1.64E-13 VJC=0.534 MJC=0.5
+ CJS=1.37E-12 VJS=0.59 MJS=0.5 TF=0.43E-9 PTF=30)
.MODEL QPA PNP(IS=5.21E-17 BF=131 NF=0.99 VAF=62 IKF=8.35E-4
+ ISE=1.09E-14 NE=2.61 BR=0.5 NR=0.984 VAR=15 IKR=3.96E-5
+ ISC=7.58E-16 NC=0.985 RB=1.52E3 IRB=1.67E-5 RBM=368.5 RE=6.31 RC=354.4
+ CJE=1.1E-13 VJE=0.745 MJE=0.33 FC=0.5 CJC=2.37E-13 VJC=0.762 MJC=0.4
+ CJS=7.11E-13 VJS=0.45 MJS=0.412 TF=1.0E-9 PTF=30)
.MODEL MN NMOS(LEVEL=3 VTO=1.3 RS=0.3 RD=0.3
+ TOX=8.5E-8 LD=1.48E-6 WD=1E-6 NSUB=1.53E16 UO=650 DELTA=10 VMAX=2E5
+ XJ=1.75E-6 KAPPA=0.8 ETA=0.066 THETA=0.01 TPG=1 CJ=2.9E-4 PB=0.837
+ MJ=0.407 CJSW=0.5E-9 MJSW=0.33)
.MODEL QP PNP(BF=61.5)
.MODEL DX D
.MODEL DZ D(BV=3.6)
.ENDS OP492
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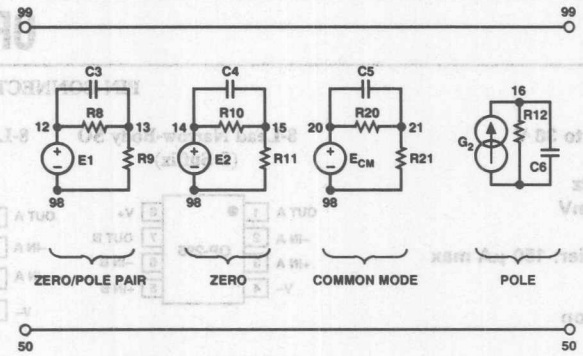
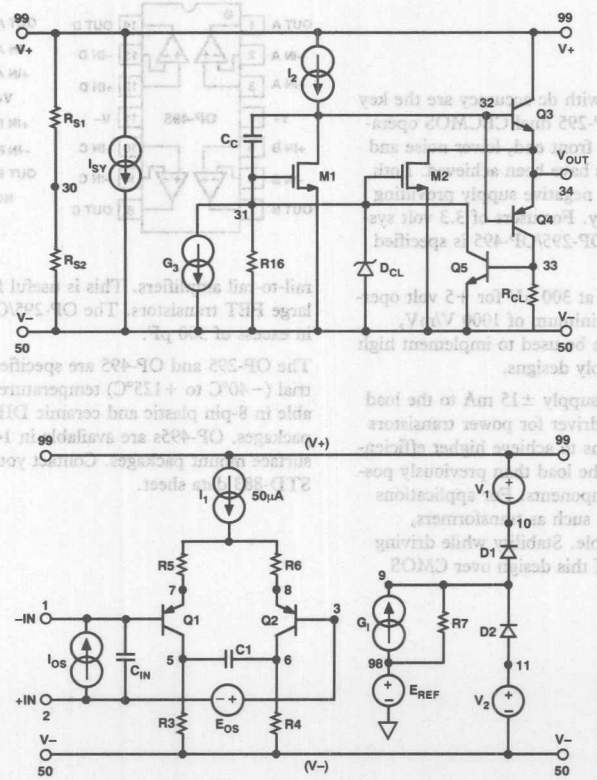
OP292/OP492 SPICE





Dual/Quad Rail-to-Rail Operational Amplifiers

OP295/OP495

FEATURES

- Rail-to-Rail Output Swing
- Single-Supply Operation: +3 V to 36 V
- Low Offset Voltage: 300 μV
- Gain Bandwidth Product: 75 kHz
- High Open-Loop Gain: 1000 V/mV
- Unity-Gain Stable
- Low Supply Current/Per Amplifier: 150 μA max

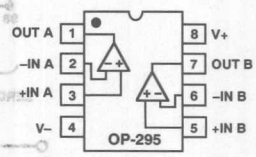
APPLICATIONS

- Battery Operated Instrumentation
- Servo Amplifiers
- Actuator Drives
- Sensor Conditioners
- Power Supply Control

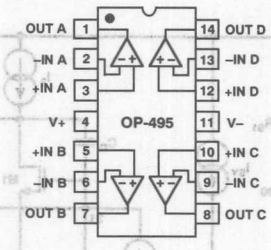
PIN CONNECTIONS

8-Lead Narrow-Body SO (S Suffix)

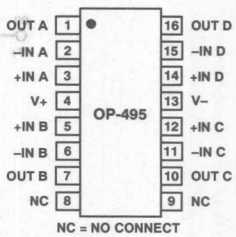
8-Lead Epoxy DIP (P Suffix)



14-Lead Epoxy DIP (P Suffix)



16-Lead SOL (300 Mil) (S Suffix)



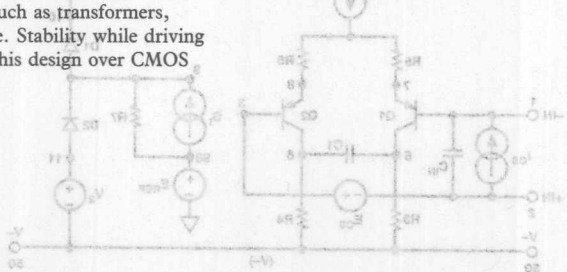
GENERAL DESCRIPTION

Rail-to-rail output swing combined with dc accuracy are the key features of the OP-495 quad and OP-295 dual CBCMOS operational amplifiers. By using a bipolar front end, lower noise and higher accuracy than CMOS designs have been achieved. Both input and output ranges include the negative supply providing the user "zero-in/zero-out" capability. For users of 3.3 volt systems such as lithium batteries, the OP-295/OP-495 is specified for three volt operation.

Maximum offset voltage is specified at 300 μV for +5 volt operation, and the open-loop gain is a minimum of 1000 V/mV, giving the user performance that can be used to implement high accuracy systems even in single supply designs.

The ability to swing rail-to-rail and supply ±15 mA to the load makes the OP-295/OP-495 an ideal driver for power transistors and "H" bridges. This allows designs to achieve higher efficiencies and to transfer more power to the load than previously possible without the use of discrete components. For applications that require driving inductive loads, such as transformers, increases in efficiency are also possible. Stability while driving capacitive loads is another benefit of this design over CMOS rail-to-rail amplifiers. This is useful for driving coax cable or large FET transistors. The OP-295/OP-495 is stable with loads in excess of 300 pF.

The OP-295 and OP-495 are specified over the extended industrial (−40°C to +125°C) temperature range. OP-295s are available in 8-pin plastic and ceramic DIP plus SO-8 surface mount packages. OP-495s are available in 14-pin plastic and SOL-16 surface mount packages. Contact your local sales office for MIL-STD-883 data sheet.



SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, V_{CM} = 2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			30	300	μV
Offset Voltage	V_{OS}	−40°C ≤ T_A ≤ +125°C			800	μV
Input Bias Current	I_B			8	20	nA
Input Bias Current	I_B	−40°C ≤ T_A ≤ +125°C			30	nA
Input Offset Current	I_{OS}			1	±3	nA
Input Offset Current	I_{OS}	−40°C ≤ T_A ≤ +125°C			±5	nA
Input Voltage Range	V_{CM}		0		+4.0	V
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 4.0 V, −40°C ≤ T_A ≤ +125°C	90	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, 0.005 ≤ V_{OUT} ≤ 4.0 V	1000	10,000		V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, −40°C ≤ T_A ≤ +125°C	500			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1	5	μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 100 kΩ to GND	4.98	5.0		V
Output Voltage Swing High	V_{OH}	R_L = 10 kΩ to GND	4.90	4.94		V
Output Voltage Swing Low	V_{OL}	I_{OUT} = 1 mA, −40°C ≤ T_A ≤ +125°C			0.11	V
Output Voltage Swing High	V_{OH}	I_{OUT} = 1 mA, −40°C ≤ T_A ≤ +125°C	4.5			V
Output Voltage Swing Low	V_{OL}	R_L = 100 kΩ to GND		0.7	2	mV
Output Voltage Swing Low	V_{OL}	R_L = 10 kΩ to GND		0.7	2	mV
Output Current	I_{OUT}		±11	±18		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±1.5 V ≤ V_S ≤ ±15 V	90	110		dB
Power Supply Rejection Ratio	PSRR	±1.5 V ≤ V_S ≤ ±15 V, −40°C ≤ T_A ≤ +125°C	85			dB
Supply Current Per Amplifier	I_{SY}	V_{OUT} = 2.5 V, R_L = ∞, −40°C ≤ T_A ≤ +125°C			150	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.03		V/μs
Gain Bandwidth Product	GBP			75		kHz
Phase Margin	θ_O			86		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		1.5		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		51		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.6		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = +3.0 V, V_{CM} = 1.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			100	500	μV
Input Bias Current	I_B			8	20	nA
Input Offset Current	I_{OS}			1	±3	nA
Input Voltage Range	V_{CM}		0		+2.0	V
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 2.0 V, −40°C ≤ T_A ≤ +125°C	90	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		750		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 10 kΩ to GND	2.9			V
Output Voltage Swing Low	V_{OL}	R_L = 10 kΩ to GND		0.7	2	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±1.5 V ≤ V_S ≤ ±15 V	90	110		dB
Power Supply Rejection Ratio	PSRR	±1.5 V ≤ V_S ≤ ±15 V, −40°C ≤ T_A ≤ +125°C	85			dB
Supply Current Per Amplifier	I_{SY}	V_{OUT} = 1.5 V, R_L = ∞, −40°C ≤ T_A ≤ +125°C			150	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.03		V/μs
Gain Bandwidth Product	GBP			75		kHz
Phase Margin	θ_O			85		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		1.6		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		53		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.6		pA/√Hz

Specifications subject to change without notice.

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INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			300	500	μV
Offset Voltage	V_{OS}	$-40°C \le T_A \le +125°C$			800	μV
Input Bias Current	I_B	$V_{CM} = 0$ V		7	20	nA
Input Bias Current	I_B	$V_{CM} = 0$ V, $-40°C \le T_A \le +125°C$			30	nA
Input Offset Current	I_{OS}	$V_{CM} = 0$ V		1	±3	nA
Input Offset Current	I_{OS}	$V_{CM} = 0$ V, $-40°C \le T_A \le +125°C$			±5	nA
Input Voltage Range	V_{CM}		−15		+13.5	V
Common-Mode Rejection	CMR	-15.0 V $\le V_{CM} \le +13.5$ V, $-40°C \le T_A \le +125°C$	90	110		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10$ kΩ	1000	4000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	$R_L = 100$ kΩ to GND	14.95			V
Output Voltage Swing High	V_{OH}	$R_L = 10$ kΩ to GND	14.80			V
Output Voltage Swing Low	V_{OL}	$R_L = 100$ kΩ to GND			−14.95	V
Output Voltage Swing Low	V_{OL}	$R_L = 10$ kΩ to GND			−14.85	V
Output Current	I_{OUT}		±15	±25		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm1.5$ V to ±15 V	90	110		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm1.5$ V to ±15 V, $-40°C \le T_A \le +125°C$	85			dB
Supply Current	I_{SY}	$V_O = 0$ V, $R_L = \infty$, $V_S = \pm18$ V, $-40°C \le T_A \le +125°C$			175	μA
Supply Voltage Range	V_S		+3 (±15)		+36 (±18)	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10$ kΩ		0.03		V/μs
Gain Bandwidth Product	GBP			85		kHz
Phase Margin	θ_O			83		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		1.25		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.6		pA/√Hz

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = +5.0 V, V_{CM} = 2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		300	μV max
Input Bias Current	I_B		20	nA max
Input Offset Current	I_{OS}		±2	nA max
Input Voltage Range[1]	V_{CM}		0 to +4	V min
Common-Mode Rejection	CMRR	$0 \le V_{CM} \le 4$ V	90	dB min
Power Supply Rejection Ratio	PSRR	±1.5 V $\le V_S \le \pm15$ V	90	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L = 10$ kΩ	1000	V/mV min
Output Voltage Swing High	V_{OH}	$R_L = 10$ kΩ	4.9	V min
Supply Current Per Amplifier	I_{SY}	$V_{OUT} = 2.5$ V, $R_L = \infty$	150	μA max

NOTES

Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

[1]Guaranteed by CMR test.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP295GP	−40°C to +125°C	8-Pin Plastic DIP	N-8
OP295GS	−40°C to +125°C	8-Pin SOIC	SO-8
OP295GBC	+25°C	DICE	

Model	Temperature Range	Package Description	Package Option*
OP495GP	−40°C to +125°C	14-Pin Plastic DIP	N-14
OP495GS	−40°C to +125°C	16-Pin SOL	R-16
OP495GBC	+25°C	DICE	

*For outline information see Package Information section.

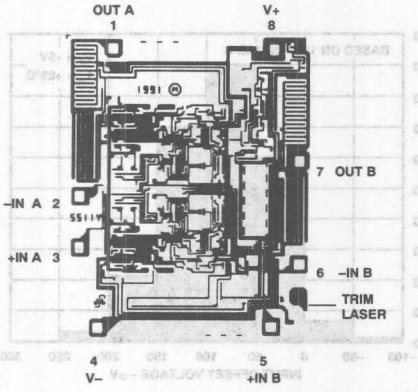
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Input Voltage[2]	±18 V
Differential Input Voltage[2]	36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
P, S Package	−65°C to +150°C
Operating Temperature Range	
OP-295G, OP-495G	−40°C to +125°C
Junction Temperature Range	
P, S Package	−65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec)	+300°C

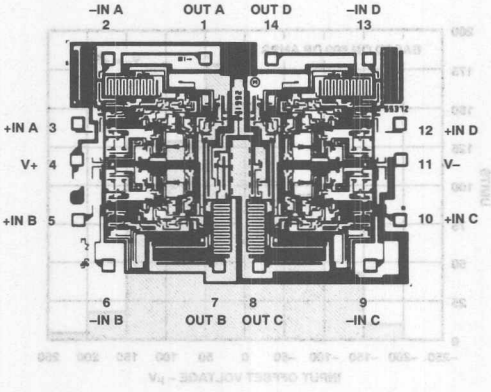
Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
16-Pin SOL (S)	98	30	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

DICE CHARACTERISTICS

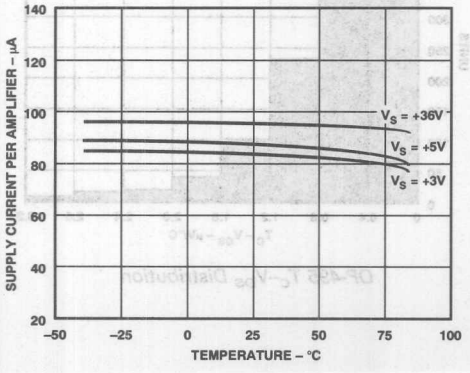


OP-295 Die Size 0.066 × 0.080 inch, 5,280 sq. mils.
Substrate (Die Backside) Is Connected to V+.
Transistor Count, 74.

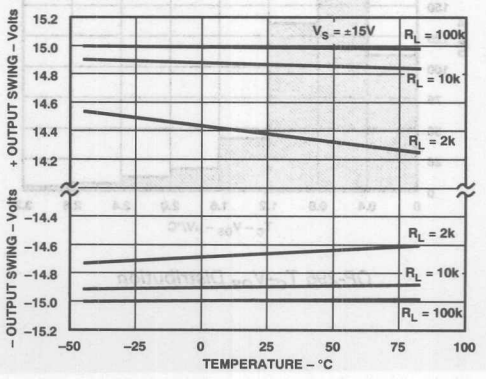


OP-495 Die Size 0.113 × 0.083 inch, 9,380 sq. mils.
Substrate (Die Backside) Is Connected to V+.
Transistor Count, 196.

Typical Characteristics—OP295/OP495

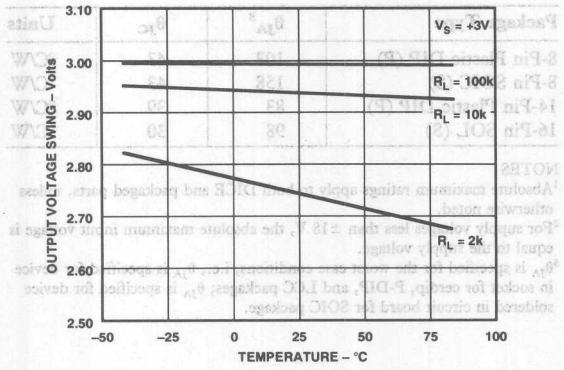


Supply Current Per Amplifier vs. Temperature

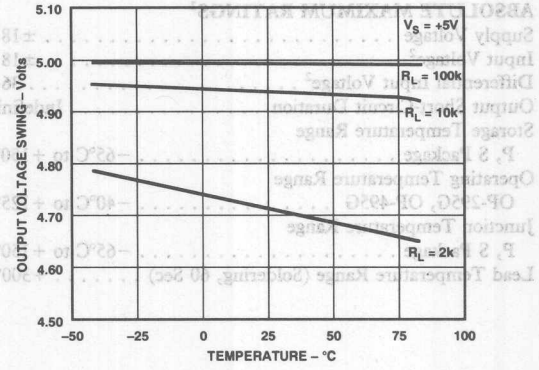


Output Voltage Swing vs. Temperature

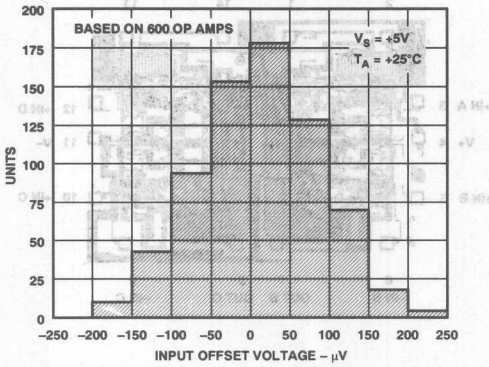
OP295/OP495–Typical Characteristics



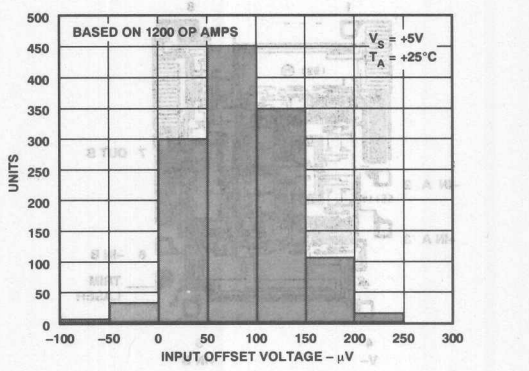
Output Voltage Swing vs. Temperature



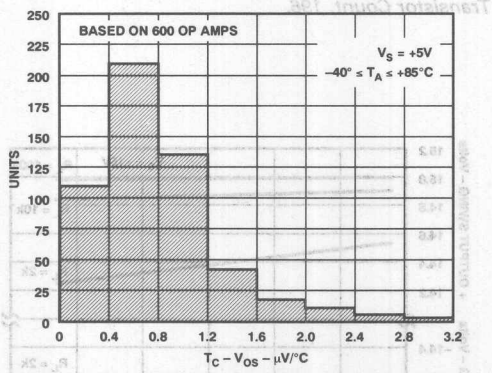
Output Voltage Swing vs. Temperature



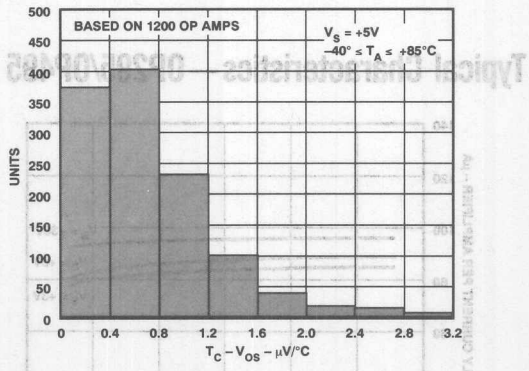
OP-295 Input Offset (V_{OS}) Distribution



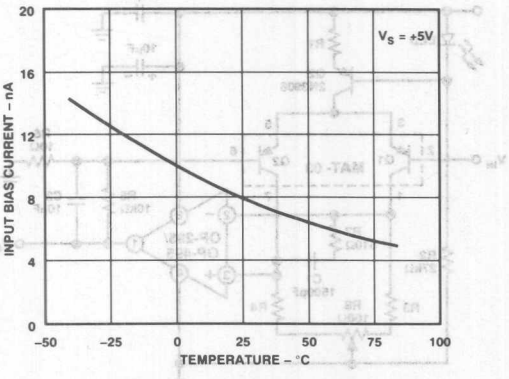
OP-495 Input Offset (V_{OS}) Distribution



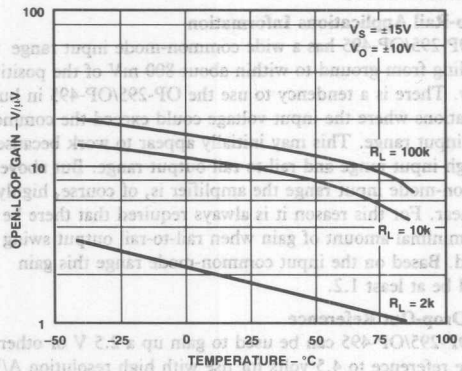
OP-295 T_C–V_{OS} Distribution



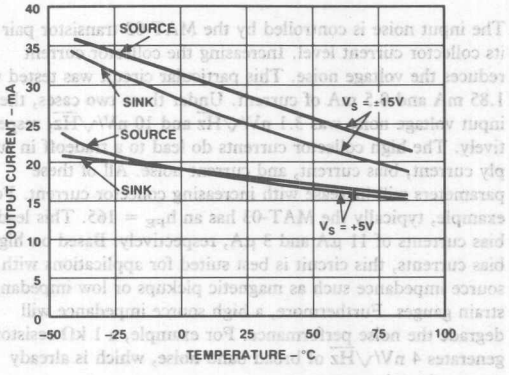
OP-495 T_C–V_{OS} Distribution



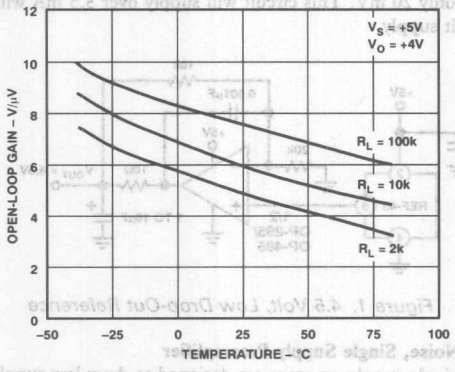
Input Bias Current vs. Temperature



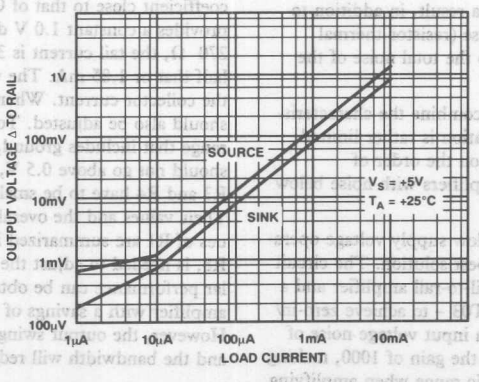
Open-Loop Gain vs. Temperature



Output Current vs. Temperature



Open-Loop Gain vs. Temperature



Output Voltage to Supply Rail vs. Sink and Source Load Current

APPLICATIONS

Rail-to-Rail Applications Information

The OP-295/OP-495 has a wide common-mode input range extending from ground to within about 800 mV of the positive supply. There is a tendency to use the OP-295/OP-495 in buffer applications where the input voltage could exceed the common-mode input range. This may initially appear to work because of the high input range and rail-to-rail output range. But above the common-mode input range the amplifier is, of course, highly nonlinear. For this reason it is always required that there be some minimal amount of gain when rail-to-rail output swing is desired. Based on the input common-mode range this gain should be at least 1.2.

Low Drop-Out Reference

The OP-295/OP-495 can be used to gain up a 2.5 V or other low voltage reference to 4.5 volts for use with high resolution A/D converters that operate from +5 volt only supplies. The circuit in Figure 1 will supply up to 10 mA. Its no-load drop-out voltage is only 20 mV. This circuit will supply over 3.5 mA with a +5 volt supply.

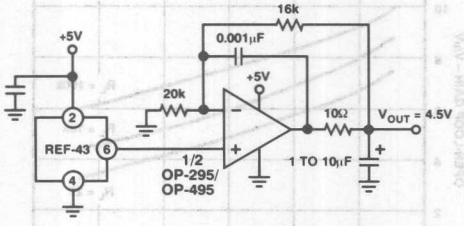


Figure 1. 4.5 Volt, Low Drop-Out Reference

Low Noise, Single Supply Preamplifier

Most single supply op amps are designed to draw low supply current, at the expense of having higher voltage noise. This tradeoff may be necessary because the system must be powered by a battery. However, this condition is worsened because all circuit resistances tend to be higher, as a result, in addition to the op amp's voltage noise, Johnson noise (resistor thermal noise) is also a significant contributor to the total noise of the system.

The choice of monolithic op amps that combine the characteristics of low noise and single supply operation is rather limited. Most single supply op amps have noise on the order of 30 to 60 nV/$\sqrt{\text{Hz}}$ and single supply amplifiers with noise below 5 nV/$\sqrt{\text{Hz}}$ do not exist.

In order to achieve both low noise and low supply voltage operation, discrete designs may provide the best solution. The circuit on Figure 2 uses the OP-295/OP-495 rail-to-rail amplifier and a matched PNP transistor pair – the MAT03 – to achieve zero-in/zero-out single supply operation with an input voltage noise of 3.1 nV/$\sqrt{\text{Hz}}$ at 100 Hz. R5 and R6 set the gain of 1000, making this circuit ideal for maximizing dynamic range when amplifying low level signals in single supply applications. The OP-295/OP-495 provides rail-to-rail output swings allowing this circuit to operate with 0 to 5 volt outputs. Only half of the OP-295/OP-495 is used leaving the other uncommitted op amp for use elsewhere.

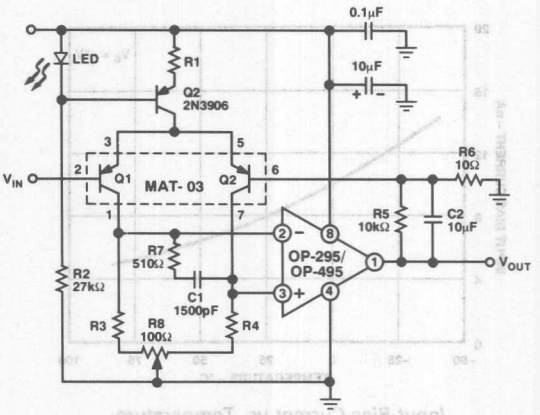


Figure 2. Low Noise Single Supply Preamplifier

The input noise is controlled by the MAT-03 transistor pair and its collector current level. Increasing the collector current reduces the voltage noise. This particular circuit was tested with 1.85 mA and 0.5 mA of current. Under these two cases, the input voltage noise was 3.1 nV/$\sqrt{\text{Hz}}$ and 10 nV/$\sqrt{\text{Hz}}$, respectively. The high collector currents do lead to a tradeoff in supply current, bias current, and current noise. All of these parameters will increase with increasing collector current. For example, typically the MAT-03 has an h_{FE} = 165. This leads to bias currents of 11 µA and 3 µA, respectively. Based on high bias currents, this circuit is best suited for applications with low source impedance such as magnetic pickups or low impedance strain gauges. Furthermore, a high source impedance will degrade the noise performance. For example, a 1 kΩ resistor generates 4 nV/$\sqrt{\text{Hz}}$ of broad band noise, which is already greater than the preamp.

The collector current is set by R1 in combination with the LED and Q2. The LED is a 1.6 V "Zener" that has temperature coefficient close to that of Q2's base-emitter junction, which provides a constant 1.0 V drop across R1. With R1 equal to 270 Ω, the tail current is 3.7 mA, and the collector current is half that or 1.85 mA. The value of R1 can be altered to adjust the collector current. Whenever R1 is changed, R3 and R4 should also be adjusted. To maintain a common-mode input range that includes ground, the collectors of the Q1 and Q2 should not go above 0.5 V, otherwise they could saturate. Thus, R3 and R4 have to be small enough to prevent this condition. Their values and the overall performance for two different values of R1 are summarized in Table I. Lastly, the potentiometer, R8, is needed to adjust the offset voltage to null it to zero. Similar performance can be obtained using an OP-90 as the output amplifier with a savings of about 185 µA of supply current. However, the output swing will not include the positive rail, and the bandwidth will reduce to approximately 250 Hz.

Table I. Single Supply Low Noise Preamp Performance

	I_C = 1.85 mA	I_C = 0.5 mA
R1	270 Ω	1.0 kΩ
R3, R4	200 Ω	910 Ω
e_n @ 100 Hz	3.15 nV/√Hz	8.6 nV/√Hz
e_n @ 10 Hz	4.2 nV/√Hz	10.2 nV/√Hz
I_{SY}	4.0 mA	1.3 mA
I_B	11 μA	3 μA
Bandwidth	1 kHz	1 kHz
Closed-Loop Gain	1000	1000

Driving Heavy Loads

The OP-295/OP-495 is well suited to drive loads by using a power transistor, Darlington or FET to increase the current to the load. The ability to swing to either rail can assure that the device is turned on hard. This results in more power to the load and an increase in efficiency over using standard op amps with their limited output swing. Driving power FETs is also possible with the OP-295/OP-495 because of its ability to drive capacitive loads of several hundred picofarads without oscillating.

Without the addition of external transistors the OP-295/OP-495 can drive loads in excess of ±15 mA with ±15 or 30 volt supplies. This drive capability is somewhat decreased at lower supply voltages. At ±5 volt supplies the drive current is ±11 mA.

Driving motors or actuators in two directions, in a single supply application is often accomplished using an "H" bridge. The principle is demonstrated in Figure 3a. From a single +5 volt supply this driver is capable of driving loads from 0.8 to 4.2 volts in both directions. Figure 3b shows the voltages at the inverting and noninverting outputs of the driver. There is a small crossover glitch that is frequency dependent and would not cause problems unless this was a low distortion application such as audio. If this is used to drive inductive loads, be sure to add diode clamps to protect the bridge from inductive kickback.

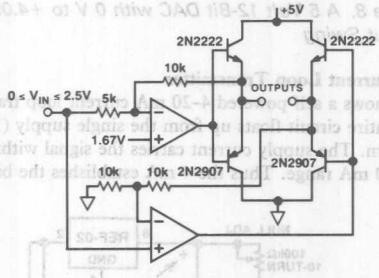


Figure 3a. "H" Bridge

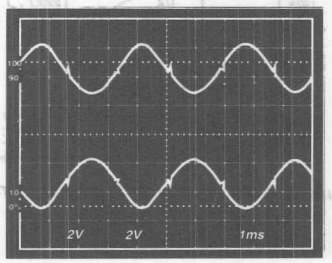


Figure 3b. "H" Bridge Outputs

Direct Access Arrangement

OP-295/OP-495 can be used in a single supply Direct Access Arrangement (DAA) as is shown in Figure 4. This figure shows a portion of a typical DAA capable of operating from a single +5 volt supply and it may also work on +3 volt supplies with minor modifications. Amplifiers A2 and A3 are configured so that the transmit signal TXA is inverted by A2 and is not inverted by A3. This arrangement drives the transformer differentially so that the drive to the transformer is effectively doubled over a single amplifier arrangement. This application takes advantage of the OP-295/OP-495's ability to drive capacitive loads, and to save power in single supply applications.

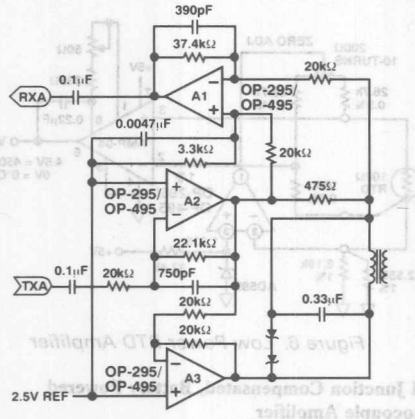


Figure 4. Direct Access Arrangement

A Single Supply Instrumentation Amplifier

The OP-295/OP-495 can be configured as a single supply instrumentation amplifier as in Figure 5. The input common-mode voltage range includes ground and the output swings to both rails.

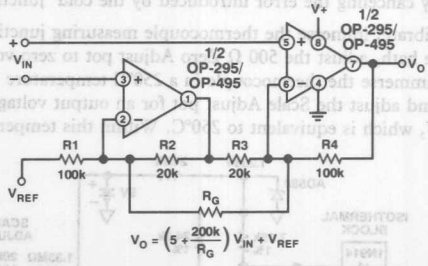


Figure 5. Single Supply Instrumentation Amplifier

Resistor R_G sets the gain of the instrumentation amplifier. Minimum gain is 6 (with no R_G). All resistors should be matched in absolute value as well as temperature coefficient to maximize common-mode rejection performance and minimize drift. This instrumentation amplifier can operate from a supply voltage as low as 3 volts.

9

low 5 V supply. The OP-295/OP-495 amplifier servos a constant 200 μA current to the bridge. The return current drops across the parallel resistors 6.19 kΩ and the 2.55 MΩ, developing a voltage that is servoed to 1.235 V, which is established by the AD589 bandgap reference. The 3-wire RTD provides a equal line resistance drop in both 100 Ω legs of the bridge, thus improving the accuracy.

The AMP-04 amplifies the differential bridge signal and converts it to a single-ended output. The gain is set by the series resistance of the 332 Ω resistor plus the 50 Ω potentiometer. The gain scales the output to produce a 4.5 V full scale. The 0.22 μF capacitor to the output provides a 7 Hz low-pass filter to keep noise at a minimum.

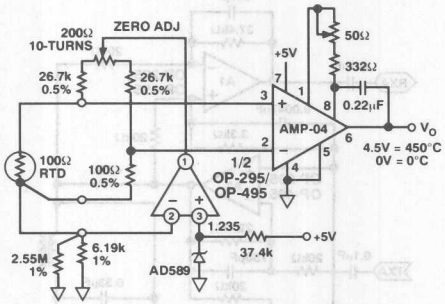


Figure 6. Low Power RTD Amplifier

A Cold Junction Compensated, Battery Powered Thermocouple Amplifier

The OP-295/OP-495's 150 μA quiescent current per amplifier consumption makes it useful for battery powered temperature measuring instruments. The K-type thermocouple terminates into an isothermal block where the terminated junctions' ambient temperature can be continuously monitored and corrected by summing an equal but opposite thermal EMF to the amplifier, thereby canceling the error introduced by the cold junctions.

To calibrate, immerse the thermocouple measuring junction in a 0°C ice bath, adjust the 500 Ω Zero Adjust pot to zero volts out. Then immerse the thermocouple in a 250°C temperature bath or oven and adjust the Scale Adjust pot for an output voltage of 2.50 V, which is equivalent to 250°C. Within this temperature

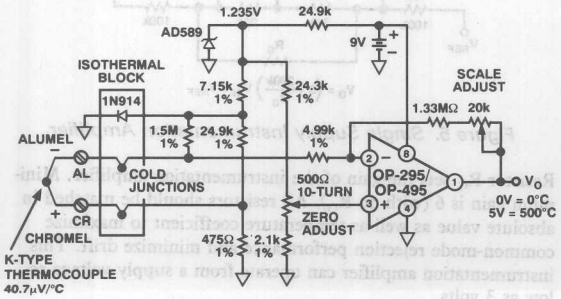


Figure 7. Battery Powered, Cold-Junction Compensated Thermocouple Amplifier

Even if the battery voltage is allowed to decay to as low as 7 volts, the rail-to-rail swing allows temperature measurements to 700°C. However, linearization may be necessary for temperatures above 250°C where the thermocouple becomes rather nonlinear. The circuit draws just under 500 μA supply current from a 9 V battery.

A 5 V Only, 12-Bit DAC That Swings 0 V to 4.095 V

Figure 8 shows a complete voltage output DAC with wide output voltage swing operating off a single +5 V supply. The serial input 12-bit D/A converter is configured as a voltage output device with the 1.235 V reference feeding the current output pin (I_{OUT}) of the DAC. The V_{REF} which is normally the input, now becomes the output.

The output voltage from the DAC is the binary weighted voltage of the reference, which is gained up by the output amplifier such that the DAC has a 1 mV per bit transfer function.

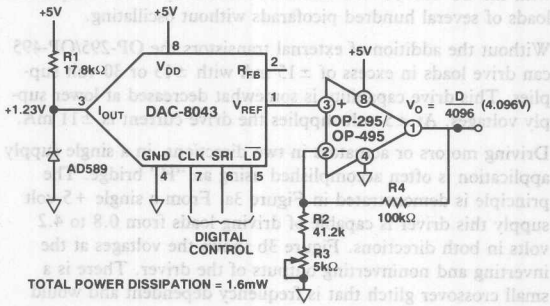


Figure 8. A 5 Volt 12-Bit DAC with 0 V to +4.095 Output Swing

4–20mA Current Loop Transmitter

Figure 9 shows a self-powered 4–20 mA current loop transmitter. The entire circuit floats up from the single supply (12 V to 36 V) return. The supply current carries the signal within the 4 mA to 20 mA range. Thus the 4 mA establishes the baseline

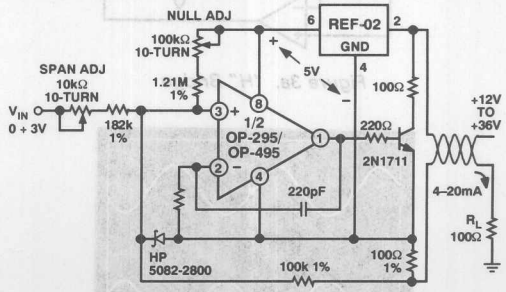


Figure 9. 4–20 mA Current Loop Transmitter

current budget with which the circuit must operate. This circuit consumes only 1.4 mA maximum quiescent current, making 2.6 mA of current available to power additional signal conditioning circuitry or to power a bridge circuit.

A 3 Volt Low-Dropout Linear Voltage Regulator

Figure 10 shows a simple 3 V voltage regulator design. The regulator can deliver 50 mA load current while allowing a 0.2 V dropout voltage. The OP-295/OP-495's rail-to-rail output swing handily drives the MJE350 pass transistor without requiring special drive circuitry. At no load, its output can swing less than the pass transistor's base-emitter voltage, turning the device nearly off. At full load, and at low emitter-collector voltages, the transistor beta tends to decrease. The additional base current is easily handled by the OP-295/OP-495 output.

The amplifier servos the output to a constant voltage, which feeds a portion of the signal to the error amplifier.

Higher output current, to 100 mA, is achievable at a higher dropout voltage of 3.8 V.

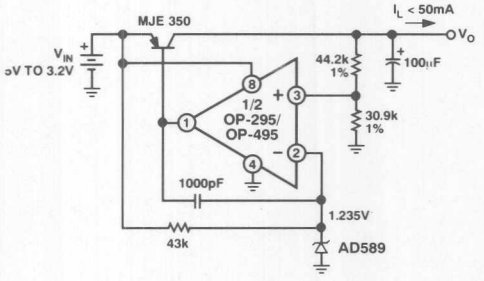


Figure 10. 3 V Low Dropout Voltage Regulator

Figure 11 shows the regulator's recovery characteristic when its output underwent a 20 mA to 50 mA step current change.

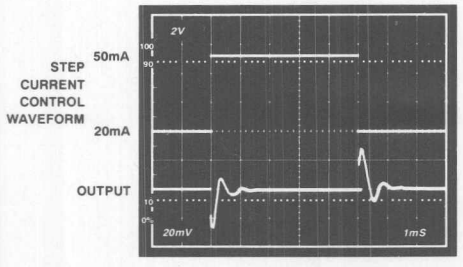


Figure 11. Output Step Load Current Recovery

Low Dropout, 500 mA Voltage Regulator with Fold-Back Current Limiting

Adding a second amplifier in the regulation loop as shown in Figure 12 provides an output current monitor as well as provides fold-back current limiting protection.

Amplifier A1 provides error amplification for the normal voltage regulation loop. As long as the output current is less than 1 ampere, amplifier A2's output swings to ground, reverse biasing the diode and effectively taking itself out of the circuit. However, as the output current exceeds 1 amp, the voltage that develops across the 0.1 Ω sense resistor forces the amplifier A2's output to go high, forward-biasing the diode, which in turn closes the current limit loop. At this point A2's lower output resistance dominates the drive to the power MOSFET transistor, thereby effectively removing the A1 voltage regulation loop from the circuit.

If the output current greater than 1 amp persists, the current limit loop forces a reduction of current to the load, which causes a corresponding drop in output voltage. As the output voltage drops, the current limit threshold also drops fractionally, resulting in a decreasing output current as the output voltage decreases, to the limit of less than 0.2 A at 1 V output. This "fold-back" effect reduces the power dissipation considerably during a short circuit condition, thus making the power supply far more forgiving in terms of the thermal design requirements. Small heat sinking on the power MOSFET can be tolerated.

The OP-295's rail-to-rail swing exacts higher gate drive to the power MOSFET, providing a fuller enhancement to the transistor. The regulator exhibits 0.2 V drop-out at 500 mA of load current. At 1 amp output, the drop-out voltage is typically 5.6 volts.

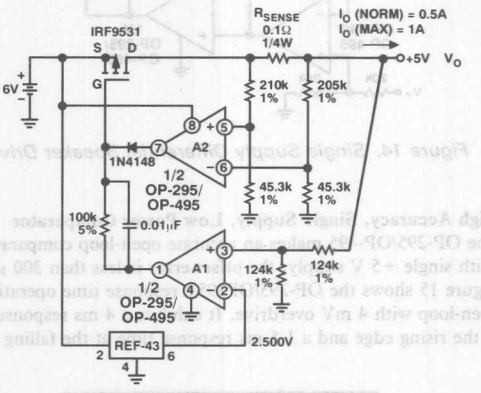


Figure 12. Low Dropout, 500 mA Voltage Regulator with Fold-back Current Limiting

Square Wave Oscillator

The oscillator circuit in Figure 13 shows the rail-to-rail swing helps maintain a constant oscillation frequency even though the supply voltage varies considerably. This works great in a battery powered system where no voltage regulation is required. The constant frequency comes from the fact that the 58.7 kΩ feedback sets up Schmitt Trigger threshold levels that are directly proportional to the supply voltage, as are the RC charge voltage levels. As a result, the RC charge time, and therefore the frequency, remain constant independent of supply voltage. The slew rate of the amplifier limits the oscillation frequency to a maximum of about 800 Hz at +5 V supply.

Single Supply Differential Speaker Driver

Connected as a differential speaker driver, the OP-295/OP-495 can deliver a minimum of 10 mA to the load. With a 600 Ω load, the OP-295/OP-495 can swing close to 5 volts peak-to-peak across the load.

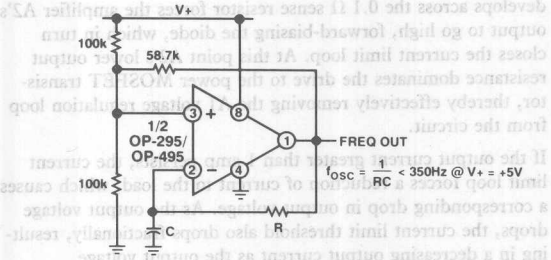


Figure 13. Square Wave Oscillator Has Stable Frequency Regardless of Supply Changes

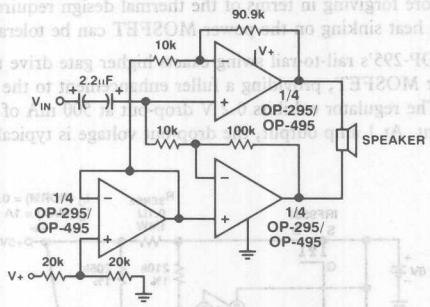


Figure 14. Single Supply Differential Speaker Driver

High Accuracy, Single Supply, Low Power Comparator

The OP-295/OP-495 makes an accurate open-loop comparator. With single +5 V supply, the offset error is less than 300 μV. Figure 15 shows the OP-295/OP495's response time operating open-loop with 4 mV overdrive. It exhibits a 4 ms response time at the rising edge and a 1.5 ms response time at the falling edge.

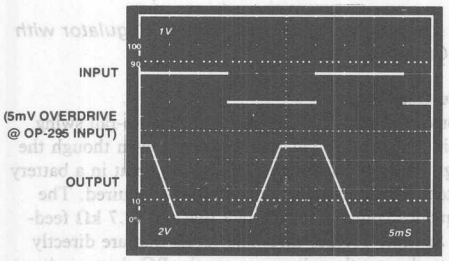


Figure 15. Open-Loop Comparator Response Time with 5 mV Overdrive

OP-295/OP-495 SPICE MODEL Macro-Model

```
* Node Assignments
*                    Noninverting Input
*                    |   Inverting Input
*                    |   |   Positive Supply
*                    |   |   |   Negative Supply
*                    |   |   |   |   Output
*                    |   |   |   |   |
.SUBCKT OP-295       1   2   99  50  20
*
* INPUT STAGE
*
I1      99   4    2E-6
R1      1    6    5E3
R2      2    5    5E3
CIN     1    2    2E-12
IOS     1    2    0.5E-9
D1      5    3    DZ
D2      6    3    DZ
VOS     7    6    30E-6
Q1      8    5    4    QP
Q2      9    7    4    QP
R3      8    50   25.8E3
R4      9    50   25.8E3
*
* GAIN STAGE
*
R7      10   98   270E6
G1      98   10   (9, 8) 27.8E-6
EREF    98   0    (39, 0) 1
R5      99   39   100E3
R6      39   50   100E3
*
* OUTPUT STAGE
*
I2      18   50   1.59E-6
V2      99   12   DC 2.2763
Q4      10   14   50   QNA   1.0
R11     14   50   33
M3      15   10   13   13   MN   L=9E-6 W=102E-6 AD=15E-10 AD=15E-10
M4      13   10   50   50   MN   L=9E-6 W=50E-6 AD=75E-11 AS=75E-11
D8      10   22   DX
V3      22   50   DC   6
M2      20   10   14   14   MN   L=9E-6 W=2000E-6 AD=30E-9 AS=30E-9
Q5      17   17   99   QPA   1.0
Q6      18   17   99   QPA   4.0
R8      18   99   2.2E6
Q7      18   19   99   QPA   1.0
R9      99   19   8
C2      18   99   20E-12
M6      15   12   17   99   MP   L=9E-6 W=27E-6 AD=405E-12 AS=405E-12
M1      20   18   19   99   MP   L=9E W=2000E-6 AD=30E-9 AS=30E-9
D4      21   18   DX
V4      99   21   DC   6
R10     10   11   6E3
C3      11   20   50E-12
.MODEL QNA NPN (IS=1.19E-16 BF =253 NF=0.99 VAF=193 IKF=2.76E-3
+ ISE=2.57E-13 NE=5 BR=0.4 NR=0.988 VAR=15 IKR=1.465E-4
+ ISC=6.9E-16 NC=0.99 RB=2.0E3 IRB=7.73E-6 RBM=132.8 RE=4 RC=209
+ CJE=2.1E-13 VJE=0.573 MJE=0.364 FC=0.5 CJC=1.64E-13 VJC=0.534
MJC=0.5
+ CJS=1.37E-12 VJS=0.59 MJS=0.5 TF=0.43E-9 PTF=30)
.MODEL QPA PNP (IS=5.21E-17 BF=131 NF=0.99 VAF=62 IKF=8.35E-4
+ ISE=1.09E-14 NE=2.61 BR=0.5 NR=0.984 VAR=15 IKR=3.96E-5
+ ISC=7.58E-16 NC=0.985 RB=1.52E3 IRB=1.67E-5 RBM=368.5 RE=6.31
RC=354.4
+ CJE=1.1E-13 VJE=0.745 MJE=0.33 FC=0.5 CJC=2.37E-13 VJC=0.762
MJC=0.4
+ CJS =7.11E-13 VJS=0.45 MJS=0.412 TF=1.0E-9 PTF=30)
.MODEL MN NMOS (LEVEL=3 VTO=1.3 RS=0.3 RD=0.3
+ TOX=8.5E-8 LD=1.48E-6 WD=1E-6 NSUB=1.53E16 UO=650 DELTA=10
VMAX=2E5
+ XJ=1.75E-6 KAPPA=0.8 ETA=0.066 THETA=0.01 TPG=1 CJ=2.9E-4
PB=0.837
+ MJ=0.407 CJSW=0.5E-9 MJSW=0.33)
.MODEL MP PMOS (LEVEL=3 VTO=-1.1 RS=0.7 RD=0.7
+ TOX=9.5E-8 LD=1.4E-6 WD=1E-6 NSUB=2.4E15 UO=650 DELTA =5.6
VMAX=1E5
+ XJ=1.75E-6 KAPPA=1.7 ETA=0.71 THETA=5.9E-3 TPG=-1 CJ=1.55E-4
PB=0.56
+ MJ=0.442 CJSW=0.4E-9 MJSW=0.33)
.MODEL DX D(IS=1E-15)
.MODEL DZ D (IS=1E-15, BV=7)
.MODEL QP PNP (BF=125)
.ENDS OP-295/OP-495
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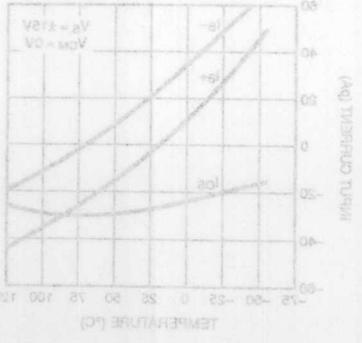


FEATURES

- **Precision Performance in Standard SO-8 Pinout**
- **Low Offset Voltage ..... 50μV Max**
- **Low Offset Voltage Drift ..... 0.6μV/°C Max**
- **Very Low Bias Current**
  +25°C ..... 100pA Max
  –55°C to +125°C ..... 450pA Max
- **Very High Open-Loop Gain ..... 2000V/mV Min**
- **Low Supply Current (Per Amplifier) ..... 625μA Max**
- **Operates From ±2V to ±20V Supplies**
- **High Common-Mode Rejection ..... 120dB Min**
- **Pin Compatible to LT1013, AD706, AD708, OP-221, LM158, and MC1458/1558 with Improved Performance**

APPLICATIONS

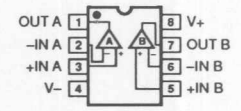
- **Strain Guage and Bridge Amplifiers**
- **High Stability Thermocouple Amplifiers**
- **Instrumentation Amplifiers**
- **Photo-Current Monitors**
- **High-Gain Linearity Amplifiers**
- **Long-Term Integrators/Filters**
- **Sample-and-Hold Amplifiers**
- **Peak Detectors**
- **Logarithmic Amplifiers**
- **Battery-Powered Systems**

GENERAL DESCRIPTION

The OP-297 is the first dual op amp to pack precision performance into the space-saving, industry standard 8-pin SO package. Its combination of precision with low power and extremely low input bias current makes the dual OP-297 useful in a wide variety of applications.

Precision performance of the OP-297 includes very low offset, under 50μV, and low drift, below 0.6μV/°C. Open-loop gain exceeds 2000V/mV insuring high linearity in every application. Errors due to common-mode signals are eliminated by the OP-297's common-mode rejection of over 120dB. The OP-297's power supply rejection of over 120dB minimizes offset voltage changes experienced in battery powered systems. Supply current of the OP-297 is under 625μA per amplifier and it can operate with supply voltages as low as ±2V. *Continued*

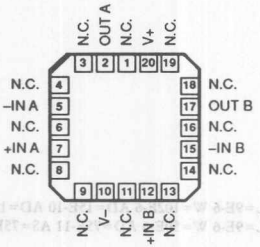
PIN CONNECTIONS



PLASTIC MINI-DIP (P-Suffix)

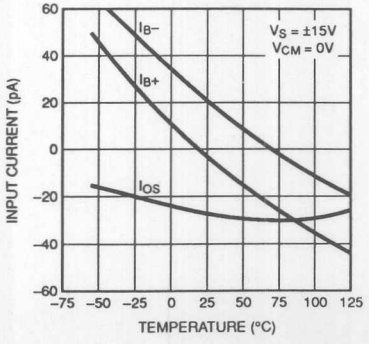
8-PIN CERDIP (Z-Suffix)

8-PIN SO (S-Suffix)

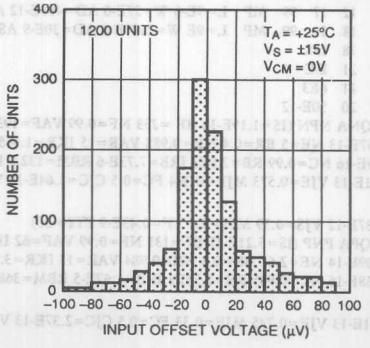


LCC (RC-Suffix)

LOW BIAS CURRENT OVER TEMPERATURE



VERY LOW OFFSET



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

GENERAL DESCRIPTION *Continued*

The OP-297 utilizes a super-beta input stage with bias current cancellation to maintain picoamp bias currents at all temperatures. This is in contrast to FET input op amps whose bias currents start in the picoamp range at 25°C, but double for every 10°C rise in temperature, to reach the nanoamp range above 85°C. Input bias current of the OP-297 is under 100pA at 25°C and is under 450pA over the military temperature range.

Combining precision, low power and low bias current, the OP-297 is ideal for a number of applications including instrumentation amplifiers, log amplifiers, photo-diode preamplifiers and long-term integrators. For a single device, see the OP-97; for a quad, see the OP-497.

ORDERING INFORMATION†

T_A = +25°C	PACKAGE			OPERATING
V_{OS} MAX (μV)	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	TEMPERATURE RANGE
50	OP297AZ/883*	—	OP297ARC/883*	MIL
50	OP297AZ	—	—	MIL
50	OP297EZ	—	—	MIL
100	OP297FZ	OP297FP	—	XIND
200	—	OP297GP	—	XIND
200	—	OP297GS††	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on extended industrial temperature range parts in CerDIP, and plastic DIP packages. For ordering information, see PMI's Data Book, Section 2.

†† For availability and burn-in information on SO packages, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Input Voltage (Note 2) ..... ±20V
Differential Input Voltage (Note 2) 40V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
  Z, RC-Package ..... –65°C to +175°C
  P, S-Package ..... –65°C to 150°C
Operating Temperature Range
  OP-297A (Z, RC) ..... –55°C to +125°C
  OP-297E, F (Z) ..... –40°C to +85°C
  OP-297F, G (P, S) ..... –40°C to +85°C
Junction Temperature
  Z, RC-Package ..... –65°C to +175°C
  P, S-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
8-Pin CerDIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	150	41	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

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ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-297A/E MIN	OP-297A/E TYP	OP-297A/E MAX	OP-297F MIN	OP-297F TYP	OP-297F MAX	OP-297G MIN	OP-297G TYP	OP-297G MAX	UNITS
Input Offset Voltage	V_{OS}		–	25	50	–	50	100	–	80	200	μV
Long-Term Input Voltage Stability			–	0.1	–	–	0.1	–	–	0.1	–	μV/mo
Input Offset Current	I_{OS}	V_{CM} = 0V	–	20	100	–	35	150	–	50	200	pA
Input Bias Current	I_B	V_{CM} = 0V	–	20	±100	–	35	±150	–	50	±200	pA
Input Noise Voltage	$e_{n\,p\text{-}p}$	0.1Hz to 10Hz	–	0.5	–	–	0.5	–	–	0.5	–	$\mu V_{p\text{-}p}$
Input Noise Voltage Density	e_n	f_O = 10Hz	–	20	–	–	20	–	–	20	–	$nV/\sqrt{Hz}$
		f_O = 1000Hz	–	17	–	–	17	–	–	17	–	
Input Noise Current Density	i_n	f_O = 10Hz	–	20	–	–	20	–	–	20	–	$fA/\sqrt{Hz}$
Input Resistance Differential Mode	R_{IN}		–	30	–	–	30	–	–	30	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	500	–	–	500	–	–	500	–	GΩ
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 2kΩ	2000	4000	–	1500	3200	–	1200	3200	–	V/mV

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-297A/E MIN	OP-297A/E TYP	OP-297A/E MAX	OP-297F MIN	OP-297F TYP	OP-297F MAX	OP-297G MIN	OP-297G TYP	OP-297G MAX	UNITS
Input Voltage Range	IVR	(Note 1)	±13	±14	–	±13	±14	–	±13	±14	–	V
Common-Mode Rejection	CMR	V_{CM} = ±13V	120	140	–	114	135	–	114	135	–	dB
Power Supply Rejection	PSR	V_S = ±2V to ±20V	120	130	–	114	125	–	114	125	–	dB
Output Voltage Swing	V_O	R_L = 10kΩ R_L = 2kΩ	±13 ±13	±14 ±13.7	– –	±13 ±13	±14 ±13.7	– –	±13 ±13	±14 ±13.7	– –	V
Supply Current Per Amplifier	I_{SY}	No Load	–	525	625	–	525	625	–	525	625	µA
Supply Voltage	V_S	Operating Range	±2	–	±20	±2	–	±20	±2	–	±20	V
Slew Rate	SR		0.05	0.15	–	0.05	0.15	–	0.05	0.15	–	V/µs
Gain Bandwith Product	GBWP	A_V = +1	–	500	–	–	500	–	–	500	–	kHz
Channel Separation	CS	V_O = 20V_{p-p} f_O = 10Hz	–	150	–	–	150	–	–	150	–	dB
Input Capacitance	C_{IN}		–	3	–	–	3	–	–	3	–	pF

NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A ≤ +125°C for OP-297A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-297A MIN	OP-297A TYP	OP-297A MAX	UNITS
Input Offset Voltage	V_{OS}		–	45	100	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.2	0.6	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	–	60	450	pA
Input Bias Current	I_B	V_{CM} = 0V	–	60	±450	pA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V, R_L = 2kΩ	1200	2700	–	V/mV
Input Voltage Range	IVR	(Note 1)	±13	±13.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±13	114	130	–	dB
Power Supply Rejection	PSR	V_S = ±2.5V to ±20V	114	125	–	dB
Output Voltage Swing	V_O	R_L = 10kΩ	±13	±13.4	–	V
Supply Current Per Amplifier	I_{SY}	No Load	–	575	750	µA
Supply Voltage	V_S	Operating Range	±2.5	–	±20	V

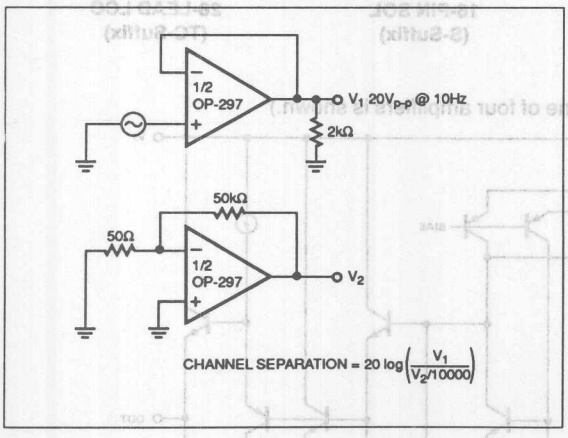
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ +85°C for OP-297E/F/G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-297E MIN	OP-297E TYP	OP-297E MAX	OP-297F MIN	OP-297F TYP	OP-297F MAX	OP-297G MIN	OP-297G TYP	OP-297G MAX	UNITS
Input Offset Voltage	V_{OS}		–	35	100	–	80	300	–	110	400	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.2	0.6	–	0.5	2.0	–	0.6	2.0	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	–	50	450	–	80	750	–	80	750	pA
Input Bias Current	I_B	V_{CM} = 0V	–	50	±450	–	80	±750	–	80	±750	pA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V, R_L = 2kΩ	1200	3200	–	1000	2500	–	800	2500	–	V/mV
Input Voltage Range	IVR	(Note 1)	±13	±13.5	–	±13	±13.5	–	±13	±13.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±13V	114	130	–	108	130	–	108	130	–	dB
Power Supply Rejection	PSR	V_S = ±2.5V to ±20V	114	0.15	–	108	0.15	–	108	0.3	–	dB
Output Voltage Swing	V_O	R_L = 10kΩ	±13	±13.4	–	±13	±13.4	–	±13	±13.4	–	V
Supply Current Per Amplifier	I_{SY}	No Load	–	550	750	–	550	750	–	550	750	µA
Supply Voltage	V_S	Operating Range	±2.5	–	±20	±2.5	–	±20	±2.5	–	±20	V

NOTE:
1. Guaranteed by CMR test.

CHANNEL SEPARATION TEST CIRCUIT



FEATURES

- **Low Input Offset Voltage ..... 150μV Max**
- **Low Offset Voltage Drift, Over –55°C to +125°C ..... 1.2μV/°C Max**
- **Low Supply Current (Per Amplifier) ..... 725μA Max**
- **High Open-Loop Gain ..... 5000V/mV Min**
- **Input Bias Current ..... 3nA Max**
- **Low Noise Voltage Density ..... 11nV/$\sqrt{Hz}$ at 1kHz**
- **Stable With Large Capacitive Loads ..... 10nF Typ**
- **Pin Compatible to OP-11, LM148, HA4741, RM4156, and LT1014 With Improved Performance**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE CERDIP 14-PIN	PACKAGE PLASTIC	PACKAGE LCC 28-CONTACT	OPERATING TEMPERATURE RANGE
150	OP400AY*	–	OP400ATC/883	MIL
150	OP400EY	–	–	IND
230	OP400FY	–	–	IND
300	–	OP400GP	–	COM
300	–	OP400GS††	–	COM
300	–	OP400HP	–	XIND
300	–	OP400HS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

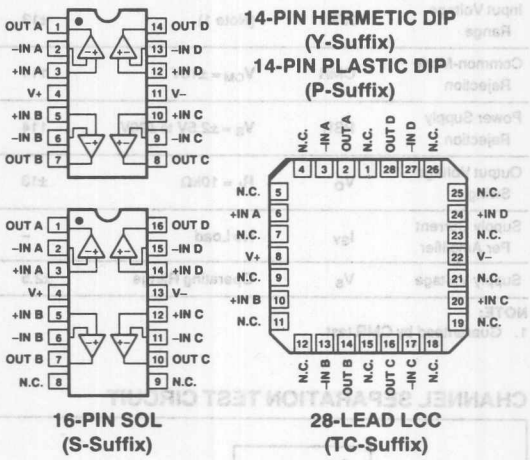
†† For availablity and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

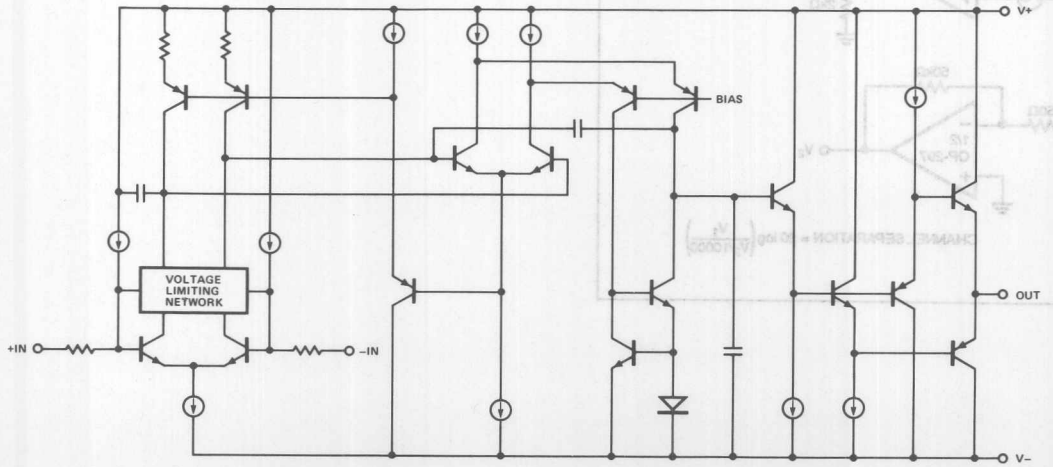
The OP-400 is the first monolithic quad operational amplifier that features OP-77 type performance. Precision performance no longer has to be sacrificed to obtain the space and cost savings offered by quad amplifiers.

The OP-400 features an extremely low input offset voltage of less than 150μV with a drift of under 1.2μV/°C, guaranteed

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (One of four amplifiers is shown.)



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

over the full military temperature range. Open-loop gain of the OP-400 is over 5,000,000 into a 10kΩ load; input bias current is under 3nA; CMR is above 120dB and PSRR below 1.8μV/V. On-chip zener-zap trimming is used to achieve the low input offset voltage of the OP-400 and eliminates the need for offset nulling. (The OP-400 conforms to the industry-standard quad pinout which does not have null terminals.)

The OP-400 features low power consumption, drawing less than 725μA per amplifier. The total current drawn by this quad amplifier is less than that of a single OP-07, yet the OP-400 offers significant improvements over this industry-standard op amp. Voltage noise density of the OP-400 is a low 11nV/$\sqrt{\text{Hz}}$ at 10Hz which is half that of most competitive devices.

The OP-400 is pin compatible with the OP-11, LM148, HA4741, RM4156, and LT1014 operational amplifiers and can be used to upgrade systems using these devices. The OP-400 is an ideal choice for applications requiring multiple precision operational amplifiers and where low power consumption is critical.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, TC, Y-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP-400A ..... –55°C to +125°C
OP-400E, OP-400F ..... –25°C to +85°C
OP-400G ..... 0°C to +70°C
OP-400H ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.
2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

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ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-400A/E MIN	OP-400A/E TYP	OP-400A/E MAX	OP-400F MIN	OP-400F TYP	OP-400F MAX	OP-400G/H MIN	OP-400G/H TYP	OP-400G/H MAX	UNITS
Input Offset Voltage	V_{OS}		—	40	150	—	60	230	—	80	300	μV
Long Term Input Voltage Stability			—	0.1	—	—	0.1	—	—	0.1	—	μV/mo
Input Offset Current	I_{OS}	V_{CM} = 0V	—	0.1	1.0	—	0.1	2.0	—	0.1	3.5	nA
Input Bias Current	I_B	V_{CM} = 0V	—	0.75	3.0	—	0.75	6.0	—	0.75	7.0	nA
Input Noise Voltage	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	—	0.5	—	$\mu V_{p\text{-}p}$
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 1000Hz (Note 1)	— —	22 11	36 18	— —	22 11	36 18	— —	22 11	— —	nV/$\sqrt{\text{Hz}}$
Input Noise Current	$i_{n\ p\text{-}p}$	0.1Hz to 10Hz	—	15	—	—	15	—	—	15	—	$pA_{p\text{-}p}$
Input Noise Current Density	i_n	f_O = 10Hz	—	0.6	—	—	0.6	—	—	0.6	—	pA/$\sqrt{\text{Hz}}$
Input Resistance Differential Mode	R_{IN}		—	10	—	—	10	—	—	10	—	MΩ
Input Resistance Common Mode	R_{INCM}		—	200	—	—	200	—	—	200	—	GΩ
Large Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10kΩ R_L = 2kΩ	5000 2000	12000 3500	— —	3000 1500	7000 3000	— —	3000 1500	7000 3000	— —	V/mV

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-400A/E MIN	OP-400A/E TYP	OP-400A/E MAX	OP-400F MIN	OP-400F TYP	OP-400F MAX	OP-400G/H MIN	OP-400G/H TYP	OP-400G/H MAX	UNITS
Input Voltage Range	IVR	Note 3	±12	±13	—	±12	±13	—	±12	±13	—	V
Common Mode Rejection	CMR	$V_{CM} = \pm 12V$	120	140	—	115	140	—	110	135	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.1	1.8	—	0.1	3.2	—	0.2	5.6	μV/V
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	±12.6 ±12.2	—	±12 ±11	±12.6 ±12.2	—	±12 ±11	±12.6 ±12.2	—	V
Supply Current Per Amplifier	I_{SY}	No Load	—	600	725	—	600	725	—	600	725	μA
Slew Rate	SR		0.1	0.15	—	0.1	0.15	—	0.1	0.15	—	V/μs
Gain Bandwidth Product	GBWP	$A_V = +1$	—	500	—	—	500	—	—	500	—	kHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 2)	123	135	—	123	135	—	123	135	—	dB
Input Capacitance	C_{IN}		—	3.2	—	—	3.2	—	—	3.2	—	pF
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	10	—	—	10	—	—	10	—	nF

NOTES:
1. Sample tested.
2. Guaranteed but not 100% tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$ for OP-400A, unless otherwise noted.

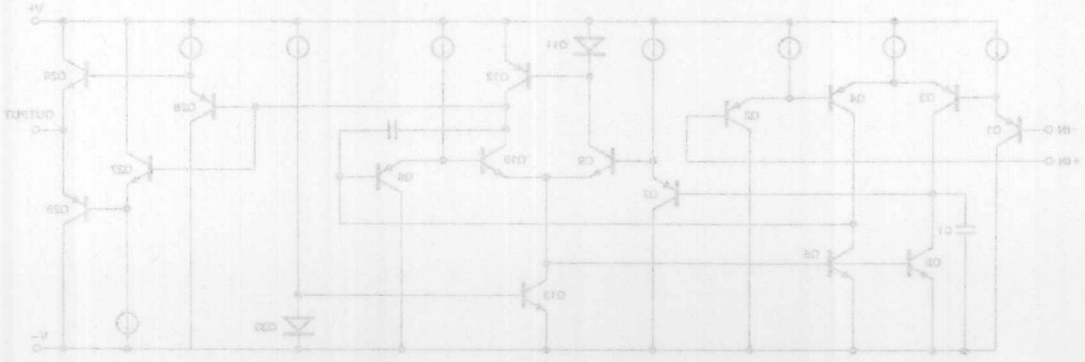
PARAMETER	SYMBOL	CONDITIONS	OP-400A MIN	OP-400A TYP	OP-400A MAX	UNITS
Input Offset Voltage	V_{OS}		—	70	270	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	1.2	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.1	2.5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	1.3	5.0	nA
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	3000 1000	9000 2300	—	V/mV
Input Voltage Range	IVR	Note 1	±12	±12.5	—	V
Common Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	130	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.2	3.2	μV/V
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	±12.4 ±12	—	V
Supply Current Per Amplifier	I_{SY}	No Load	—	600	775	μA
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	8	—	nF

NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le \pm 85°C$ for OP-400E/F, $0°C \le T_A \le +70°C$ for OP-400G, $-40°C \le T_A \le +85°C$ for OP-400H, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-400E MIN	OP-400E TYP	OP-400E MAX	OP-400F MIN	OP-400F TYP	OP-400F MAX	OP-400G/H MIN	OP-400G/H TYP	OP-400G/H MAX	UNITS
Input Offset Voltage	V_{OS}		–	60	220	–	80	350	–	110	400	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.3	1.2	–	0.3	2.0	–	0.6	2.5	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$ E, F, G Grades H Grade	– –	0.1 –	2.5 –	– –	0.1 –	3.5 –	– –	0.2 0.2	6.0 12.0	nA
Input Bias Current	I_B	$V_{CM} = 0V$ E, F, G Grades H Grade	– –	0.9 –	5.0 –	– –	0.9 –	10.0 –	– –	1.0 1.0	12.0 20.0	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	3000 1500	10000 2700	– –	2000 1000	5000 2000	– –	2000 1000	5000 2000	– –	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	135	–	110	135	–	105	130	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	–	0.15	3.2	–	0.15	5.6	–	0.3	10.0	µV/V
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	±12.4 ±12	– –	±12 ±11	±12.4 ±12	– –	±12 ±11	±12.6 ±12.2	– –	V
Supply Current Per Amplifier	I_{SY}	No Load	–	600	775	–	600	775	–	600	775	µA
Capacitive Load Stability		$A_V = +1$ No Oscillations	–	10	–	–	10	–	–	10	–	nF

NOTE:
1. Guaranteed by CMR test.



Quad Micropower Operational Amplifier

OP420

FEATURES

- **Low Supply Current ..... 200μA Max @ V_S = +5V**
- **Single-Supply Operation ..... +5V to +30V**
- **Dual-Supply Operation ..... ±2.5V to ±15V**
- **Low Input Offset Voltage ..... 500μV Typ**
- **Low Input Offset Voltage Drift ..... 5μV/°C Typ**
- **High Common-Mode Input Range ... V− to (V+ − 1.5V)**
- **High CMRR ..... 100dB Typ**
- **High Open-Loop Gain ..... 1100V/mV Typ**
- **LM 148 Pinout**
- **Available in Die Form**

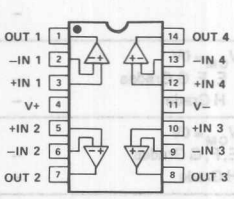
ORDERING INFORMATION †

T_A=+25°C V_{OS} MAX (mV)	PACKAGE CERDIP 14-PIN	PACKAGE LCC 20-CONTACT	PACKAGE PLASTIC	OPERATING TEMPERATURE RANGE
2.5	OP420BY	–	–	MIL
2.5	OP420FY	–	–	IND
4.0	OP420CY	OP420CRC/883	–	MIL
4.0	OP420GY	–	OP420GP	XIND
4.0	–	–	OP420GS	XIND
6.0	OP420HY	–	OP420HP	XIND
6.0	–	–	OP420HS	XIND

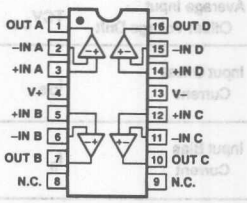
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

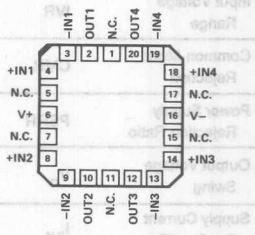
PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-Suffix)
14-PIN EPOXY DIP (P-Suffix)



16-PIN SOL (S-Suffix)



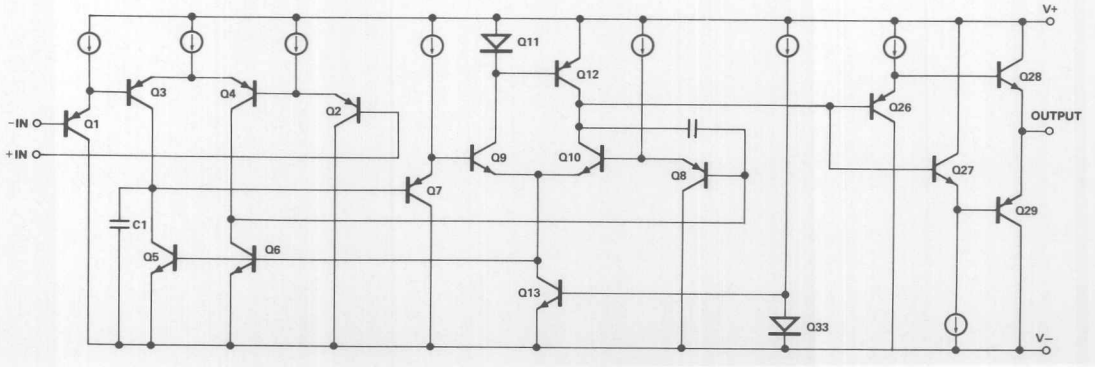
OP-420CRC/883
20-LEAD LCC
(RC-Suffix)

GENERAL DESCRIPTION

The OP-420 quad micropower operational amplifier is a single-chip quad patterned after the OP-20 precision micropower single operational amplifier. A Darlington PNP input stage allows the input common-mode voltage to include V−. The wide input range combined with low power-supply drain (~40μA/section at 5V), provides a unique solution for designs requiring high functional density and portable operation. Applications include two-wire transmitters for process control loops, battery-operated remote-line filters, signal preconditioning amplifiers, and a variety of multiple-gain block arrays.

For micropower applications requiring offset nulling, see the OP-20, OP-21 and OP-22 data sheets.

SIMPLIFIED SCHEMATIC (1/4 Shown)



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
(One Amplifier Only)
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Operating Temperature Range
OP-420BY, OP-420CY, OP-420CRC ..... –55°C to +125°C
OP-420FY ..... –25°C to +85°C
OP-420G, OP-420H ..... –40°C to +85°C
Junction Temperature(T_J) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	99	12	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

			OP-420B OP-420F			OP-420C OP-420G			OP-420H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	2.5	—	1	4	—	2	6	mV
Input Offset Current (Note 1)	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	1.5	—	0.8	2.5	—	1.2	6	nA
Input Bias Current (Note 1)	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	9	20	—	12	30	—	18	40	nA
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$	—	50	—	—	50	—	—	50	—	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$	—	0.12	—	—	0.12	—	—	0.12	—	$pA/\sqrt{Hz}$
Input Voltage Range	IVR	V+ = +5V, V– = 0V $V_S = \pm 15V$	0/3.5 –15/13.5	— —	— —	0/3.5 –15/13.5	— —	— —	0/3.5 –15/13.5	— —	— —	V
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V– = 0V $0V \le V_{CM} \le 3.5V$ $V_S = \pm 15V$ $-15V \le V_{CM} \le 13.5V$	83 83	100 100	— —	80 80	96 96	— —	76 76	90 90	— —	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; & V– = 0V, V+ = 5V to 30V	—	10	30	—	20	50	—	30	80	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$, $V_O = \pm 10V$	600	1100	—	400	900	—	200	800	—	V/mV
Slew Rate	SR		—	0.05	—	—	0.05	—	—	0.05	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$ $R_L = 10k\Omega$	—	150	—	—	150	—	—	150	—	kHz
Output Voltage Swing	V_O	V+ = 5V, V– = 0V, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 25k\Omega$	0.7/4.1 ±14.0	— —	— —	0.8/4.0 ±14.0	— —	— —	0.9/3.8 ±13.8	— —	— —	V
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	— —	140 330	200 360	— —	170 360	300 460	— —	200 390	400 600	μA

NOTE:
1. I_B and I_{OS} are measured at $V_{CM} = 0$.

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PARAMETER	SYMBOL	CONDITIONS	OP-420B / OP-420F MIN	OP-420B / OP-420F TYP	OP-420B / OP-420F MAX	OP-420C / OP-420G MIN	OP-420C / OP-420G TYP	OP-420C / OP-420G MAX	OP-420H MIN	OP-420H TYP	OP-420H MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	5	10	—	8	15	—	15	25	µV/°C
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	3.5	—	—	5.5	—	—	7.5	mV
Input Offset Current (Note 2)	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	3	—	—	4	—	—	8	nA
Input Bias Current (Note 2)	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	30	—	—	40	—	—	60	nA
Input Voltage Range	IVR	V+ = +5V, V− = 0V	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	−15/13.2	—	—	−15/13.2	—	—	−15/13.2	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V, $0V \le V_{CM} \le 3.2V$	76	96	—	73	92	—	73	86	—	dB
		$V_S = \pm 15V$, $-15V \le V_{CM} \le 13.2V$	76	96	—	73	92	—	73	86	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ and V− = 0V, V+ = 5V to 30V	—	15	50	—	25	80	—	40	100	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 50k\Omega$, $V_O = \pm 10V$	300	800	—	200	650	—	100	400	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, $R_L = 20k\Omega$	0.9/3.9	—	—	1.0/3.8	—	—	1.1/3.6	—	—	V
		$V_S = \pm 15V$, $R_L = 50k\Omega$	±13.8	—	—	±13.8	—	—	±13.6	—	—	
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	170	300	—	210	400	—	250	600	µA
		$V_S = \pm 15V$, No Load	—	390	500	—	420	640	—	500	800	

NOTES:
1. Sample tested.
2. I_B and I_{OS} are measured at $V_{CM} = 0$.

FEATURES

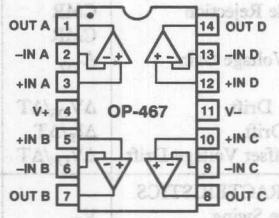
- High Slew Rate – 170 V/μs
- Wide Bandwidth – 28 MHz
- Fast Settling Time – <200 ns to 0.01%
- Low Offset Voltage – <500 μV
- Unity-Gain Stable
- Low Voltage Operation ±5 V to ±15 V
- Low Supply Current – <10 mA
- Drives Capacitive Loads

APPLICATIONS

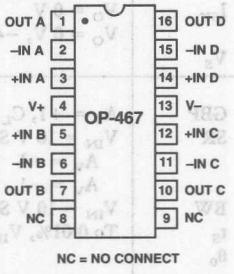
- High Speed Image Display Drivers
- High Frequency Active Filters
- Fast Instrumentation Amplifiers
- High Speed Detectors
- Integrators
- Photo Diode Preamps

PIN CONNECTIONS

14-Lead Ceramic DIP (Y Suffix) and 14-Lead Epoxy DIP (P Suffix)

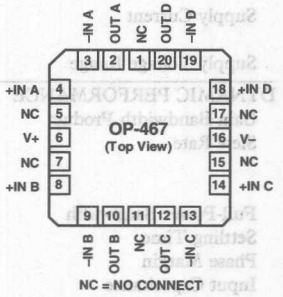


16-Lead SOL (S Suffix)



NC = NO CONNECT

20-Position Chip Carrier (RC Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

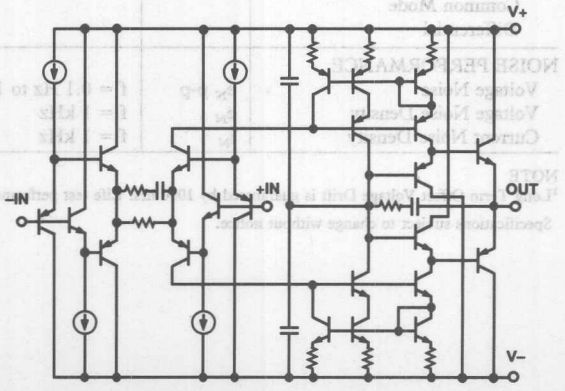
The OP-467 is a quad, high speed, precision operational amplifier. It offers the performance of a high speed op amp combined with the advantages of a precision operational amplifier all in a single package. The OP-467 is an ideal choice for applications where, traditionally, more than one op amp was used to achieve this level of speed and precision.

The OP-467's internal compensation ensures stable unity-gain operation, and it can drive large capacitive loads without oscillation. With a gain bandwidth product of 28 MHz driving a 30 pF load, output slew rate in excess of 170 V/μs, and settling time to 0.01% in less than 200 ns, the OP-467 provides excellent dynamic accuracy in high speed data-acquisition systems. The channel-to-channel separation is typically 60 dB at 10 MHz.

The dc performance of OP-467 includes less than 0.5 mV of offset, voltage noise density below 6 nV/$\sqrt{\text{Hz}}$ and total supply current under 10 mA. Common-mode rejection and power supply rejection ratios are typically 85 dB. PSRR is maintained to better than 40 dB with input frequencies as high as 1 MHz. The low offset and drift plus high speed and low noise, make the OP-467 usable in applications such as high speed detectors and instrumentation.

The OP-467 is specified for operation from ±5 V to ±15 V over the extended industrial temperature range (−40°C to +85°C) and is available in 14-pin plastic and ceramic DIP, plus SOL-16 and 20-lead LCC surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.



Simplified OP-467 Schematic

OP467—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.2	0.5	mV
		$-40°C \le T_A \le +85°C$			1	mV
Input Bias Current	I_B	V_{CM} = 0 V		150	600	nA
		V_{CM} = 0 V, $-40°C \le T_A \le +85°C$		150	700	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		10	100	nA
		V_{CM} = 0 V, $-40°C \le T_A \le +85°C$		10	150	nA
Common-Mode Rejection	CMR	V_{CM} = ±12 V	80	90		dB
	CMR	V_{CM} = ±12 V, $-40°C \le T_A \le +85°C$	80	88		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	83	86		dB
		R_L = 2 kΩ, $-40°C \le T_A \le +85°C$	77.5			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3.5		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			0.2		pA/°C
Long Term Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 1			750	µV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ	±13.0	±13.5		V
		R_L = 2 kΩ, $-40°C \le T_A \le +85°C$	±12.9	±13.12		V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$\pm 4.5\ V \le V_S = \pm 18\ V$	96	120		dB
		$-40°C \le T_A \le +85°C$	86	115		dB
Supply Current	I_{SY}	V_O = 0 V		8	10	mA
		V_O = 0 V, $-40°C \le T_A \le +85°C$			13	mA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	A_V = +1, C_L = 30 pF		28		MHz
Slew Rate	SR	V_{IN} = 10 V Step, R_L = 2 kΩ, C_L = 30 pF				
		A_V = +1	125	170		V/µs
		A_V = −1		350		V/µs
Full-Power Bandwidth	BW_p	V_{IN} = 10 V Step		2.7		MHz
Settling Time	t_S	To 0.01%, V_{IN} = 10 V Step		200		ns
Phase Margin	θ_0			45		Degrees
Input Capacitance						
Common Mode				2.0		pF
Differential				1.0		pF
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		0.15		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		6		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		8		pA/√Hz

NOTE

[1]Long Term Offset Voltage Drift is guaranteed by 1000 hrs. Life test performed on three independent wafer lots at +125°C, with an LTPD of 1.3.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.3	0.5	mV
		−40°C ≤ T_A ≤ +85°C			1	mV
Input Bias Current	I_B	V_{CM} = 0 V		125	600	nA
		V_{CM} = 0 V, −40°C ≤ T_A ≤ +85°C		150	700	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		20	100	nA
		V_{CM} = 0 V, −40°C ≤ T_A ≤ +85°C			150	nA
Common-Mode Rejection	CMR	V_{CM} = ±2.0 V	76	85		dB
	CMR	V_{CM} = ±2.0 V, −40°C ≤ T_A ≤ +85°C	76	80		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	80	83		dB
		R_L = 2 kΩ, −40°C ≤ T_A ≤ +85°C	74			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3.5		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			0.2		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ	±3.0	±3.5		V
		R_L = 2 kΩ, −40°C ≤ T_A ≤ +85°C	±3.0	±3.20		V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±4.5 V ≤ V_S = ±5.5 V	92	107		dB
		−40°C ≤ T_A ≤ +85°C	83	105		dB
Supply Current	I_{SY}	V_O = 0 V		8	10	mA
		V_O = 0 V, −40°C ≤ T_A ≤ +85°C			11	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	A_V = +1		22		MHz
Slew Rate	SR	V_{IN} = 5 V Step, R_L = 2 kΩ, C_L = 39 pF				
		A_V = +1		90		V/µs
		A_V = −1		90		V/µs
Full-Power Bandwidth	BW_p	V_{IN} = 5 V Step		2.5		MHz
Settling Time	t_S	To 0.01%, V_{IN} = 5 V Step		280		ns
Phase Margin	θ_0			45		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		0.15		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		7		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		8		pA/√Hz

Specifications subject to change without notice.

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OP-467 ELECTRICAL CHARACTERISTICS (V_S = ±15.0 V, T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		±0.5	mV max
Input Bias Current	I_B	V_{CM} = 0 V	600	nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	100	nA max
Input Voltage Range[1]			±12	V min/max
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12 V	80	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	96	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	83	dB min
Output Voltage Range	V_O	R_L = 2 kΩ	±13.0	V min
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞	10	mA max

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±26 V
Output Short-Circuit Duration . . . . . Limited
Storage Temperature Range
  Y, RC Packages . . . . . −65°C to +175°C
  P, S Packages . . . . . −65°C to +150°C
Operating Temperature Range
  OP-467A . . . . . −55°C to +125°C
  OP-467G . . . . . −40°C to +85°C
Junction Temperature Range
  Y, RC Packages . . . . . −65°C to +175°C
  P, S Packages . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
14-Pin Cerdip (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	88	23	°C/W
20-Contact LCC (RC)	78	33	°C/W

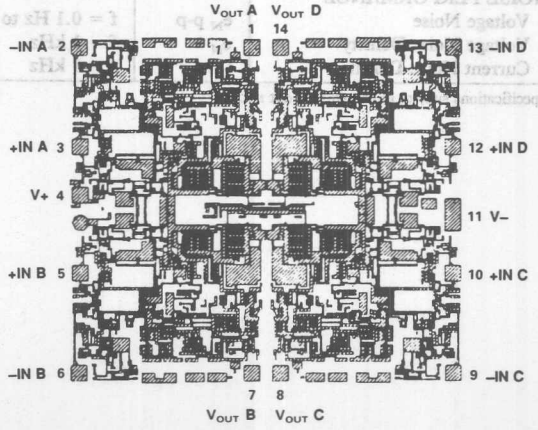
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP467AY/883	−55°C to +125°C	14-Pin Cerdip	Q-14
OP467ARC/883	−55°C to +125°C	20-Contact LCC	E-20A
OP467GP	−40°C to +85°C	14-Pin Plastic DIP	N-14
OP467GS	−40°C to +85°C	16-Pin SOL	R-16
OP467GBC	+25°C	DICE	

*For outline information see Package Information section.

DICE CHARACTERISTICS



OP-467 Die Size 0.111 X 0.100 inch, 11,100 sq. mils
Substrate is Connected to V+, Number of Transistors 165.

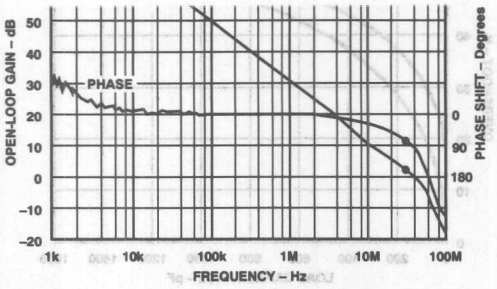


Figure 1. Open-Loop Gain, Phase vs. Frequency

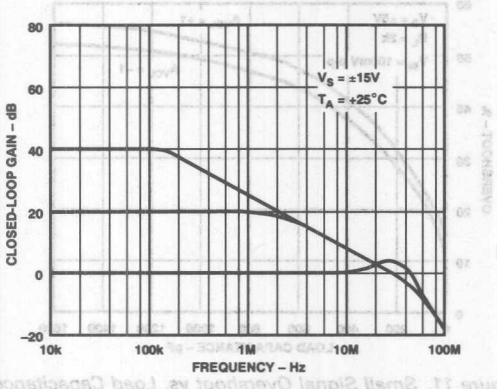


Figure 2. Closed-Loop Gain vs. Frequency

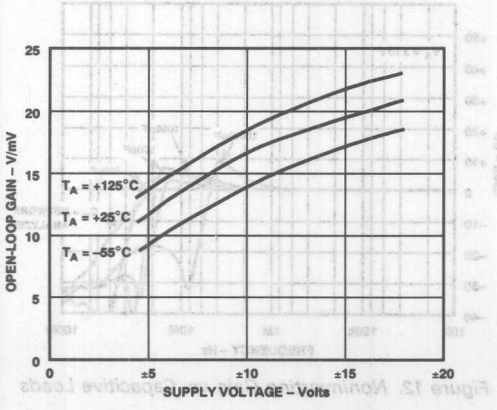


Figure 3. Open-Loop Gain vs. Supply Voltage

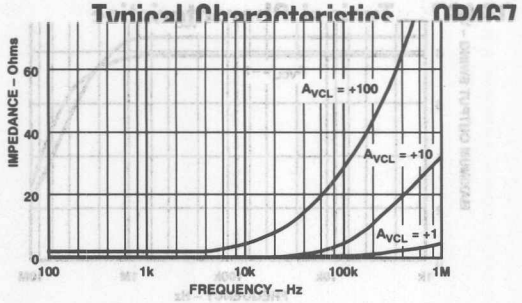


Figure 4. Closed-Loop Output Impedance vs. Frequency

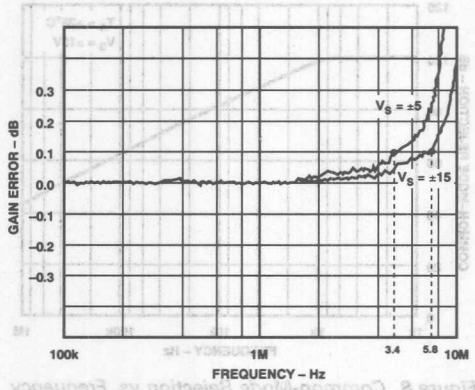


Figure 5. Gain Linearity vs. Frequency

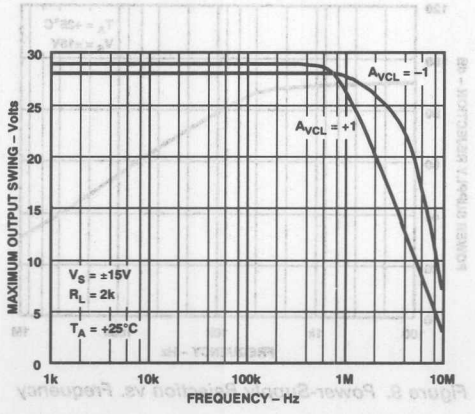


Figure 6. Max V_{OUT} Swing vs. Frequency

OP467—Typical Characteristics

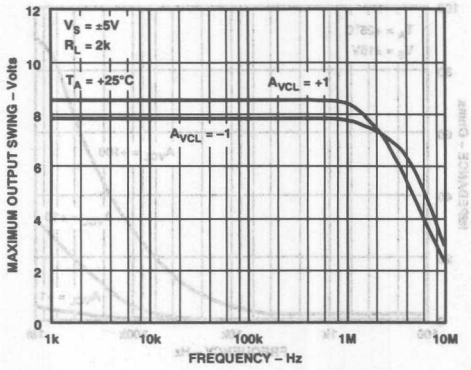


Figure 7. Max V_{OUT} Swing vs. Frequency

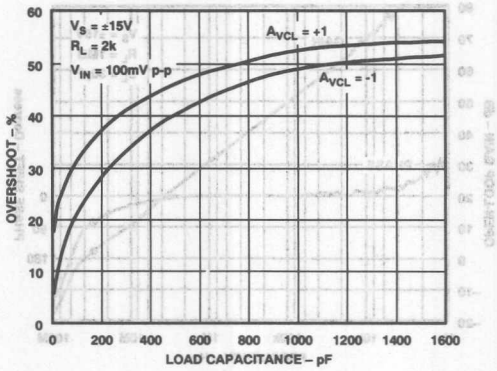


Figure 10. Small Signal Overshoot vs. Load Capacitance

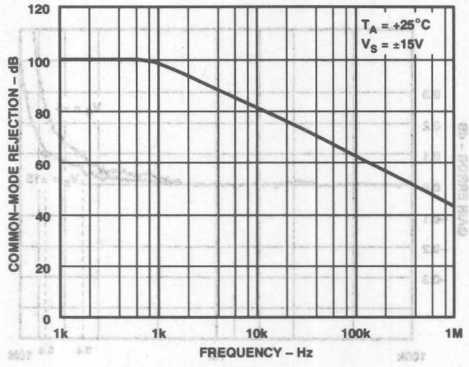


Figure 8. Common-Mode Rejection vs. Frequency

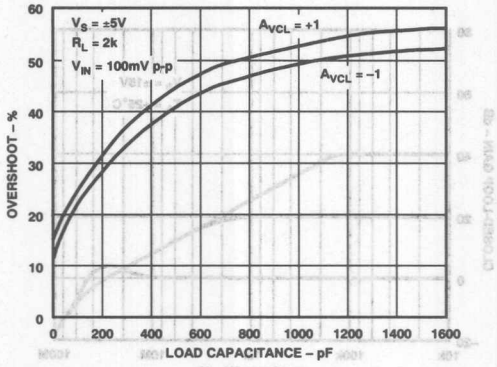


Figure 11. Small Signal Overshoot vs. Load Capacitance

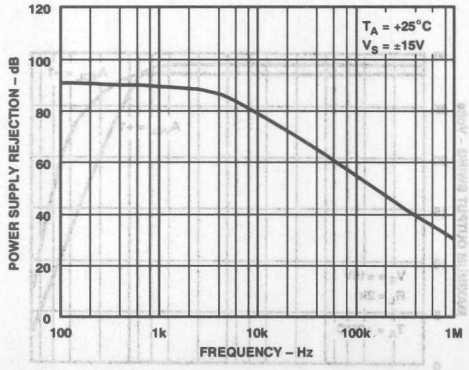


Figure 9. Power-Supply Rejection vs. Frequency

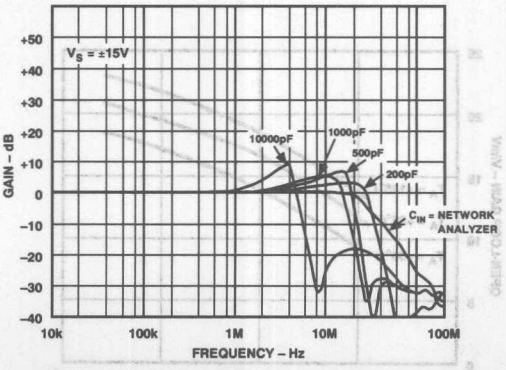


Figure 12. Noninverting Gain vs. Capacitive Loads

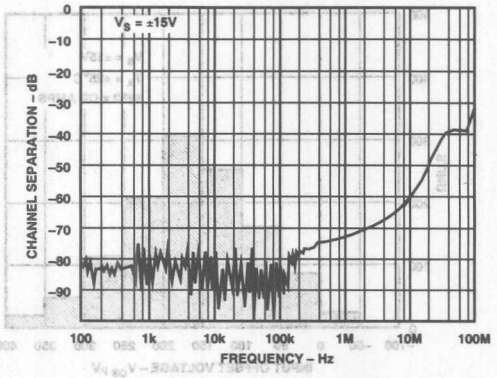


Figure 13. Channel Separation vs. Frequency

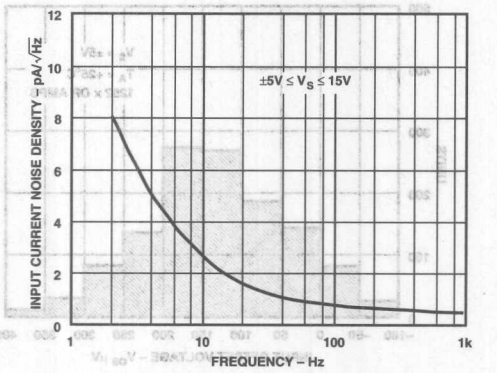


Figure 14. Input Current Noise Density vs. Frequency

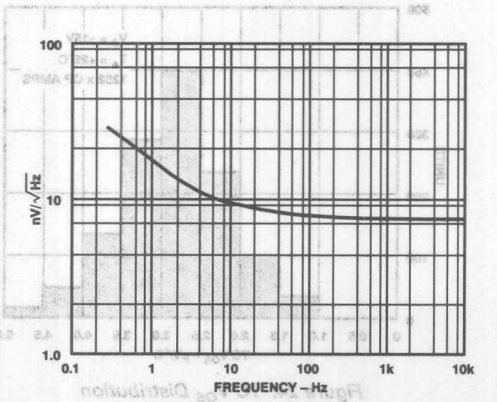


Figure 15. Voltage Noise Density vs. Frequency

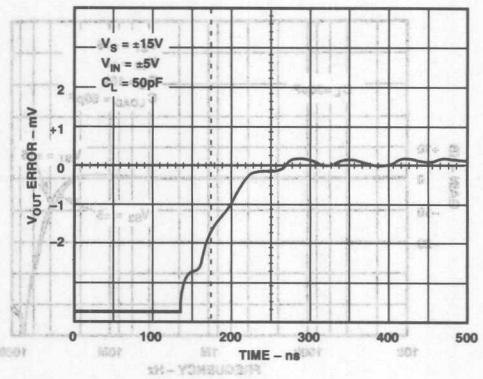


Figure 16. Settling Time, Negative Edge

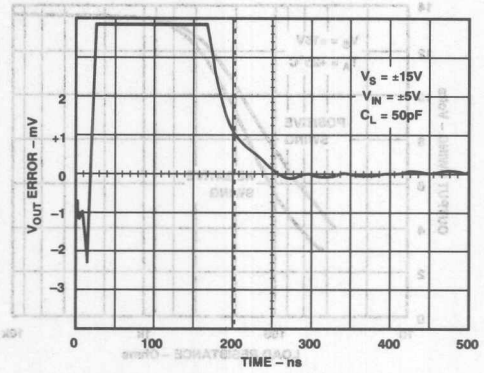


Figure 17. Settling Time, Positive Edge

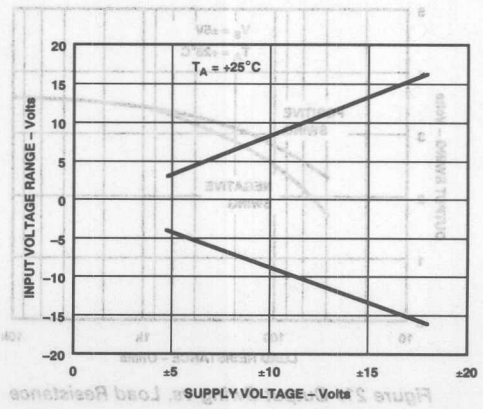


Figure 18. Input Voltage Range vs. Supply Voltage

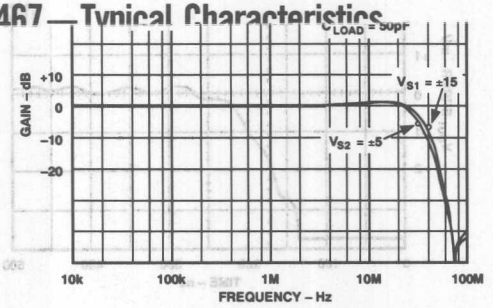


Figure 19. Noninverting Gain vs. Supply Voltage

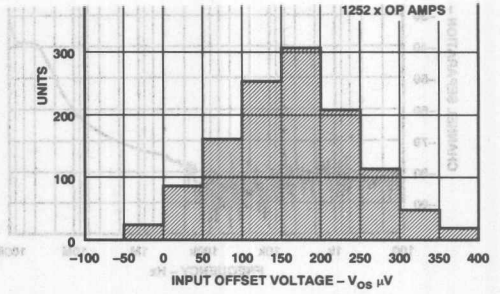


Figure 22. Input Offset Voltage Distribution

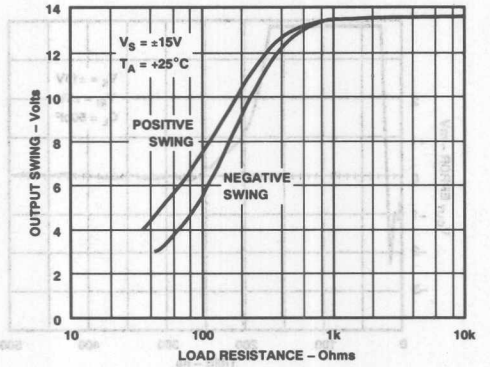


Figure 20. Output Swing vs. Load Resistance

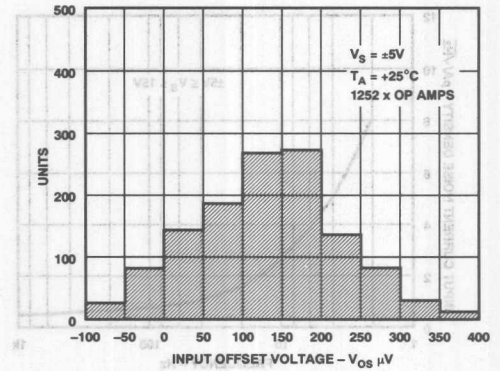


Figure 23. Input Offset Voltage Distribution

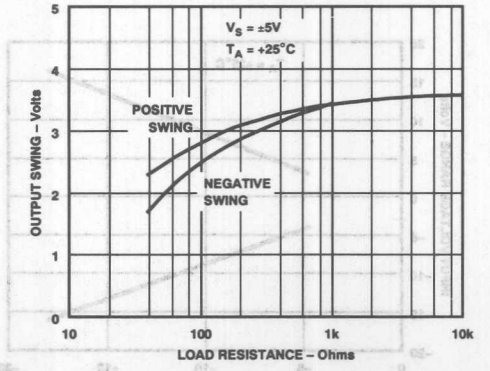


Figure 21. Output Swing vs. Load Resistance

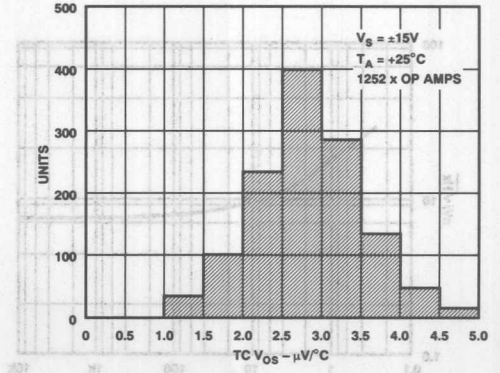


Figure 24. TC V_{OS} Distribution

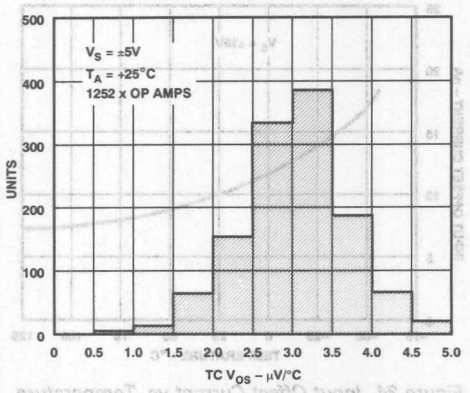


Figure 25. TC V_{OS} Distribution

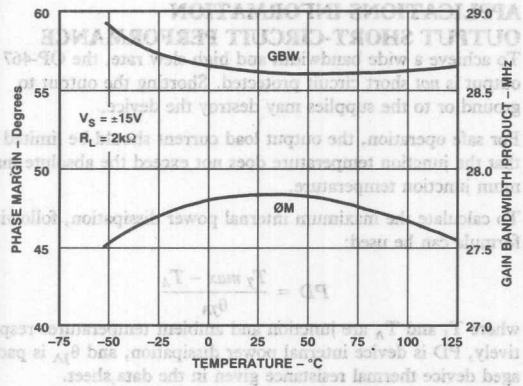


Figure 26. Phase Margin & Gain Bandwidth vs. Temperature

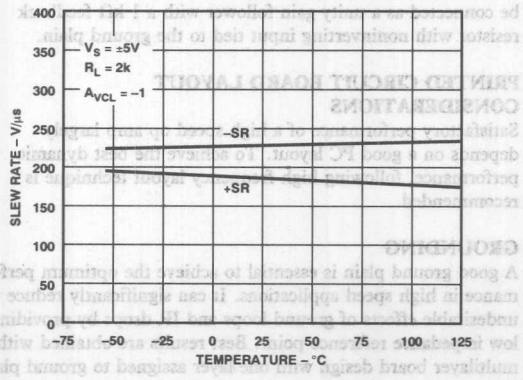


Figure 27. Slew Rate vs. Temperature

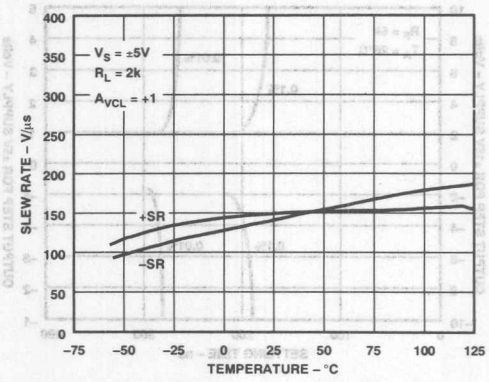


Figure 28. Slew Rate vs. Temperature

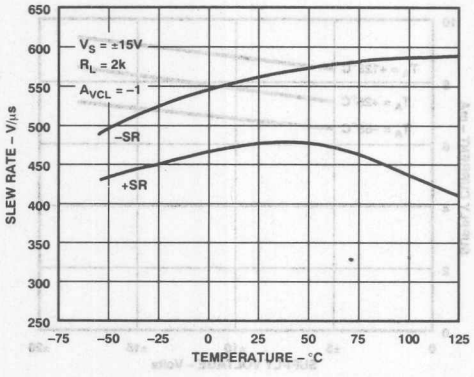


Figure 29. Slew Rate vs. Temperature

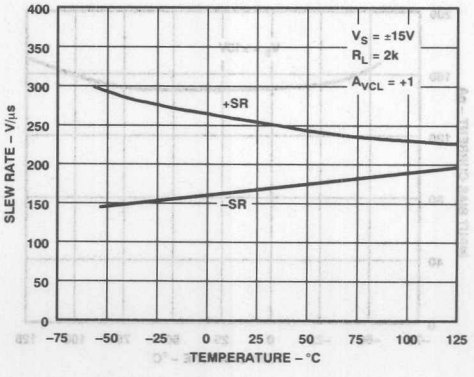


Figure 30. Slew Rate vs. Temperature

9

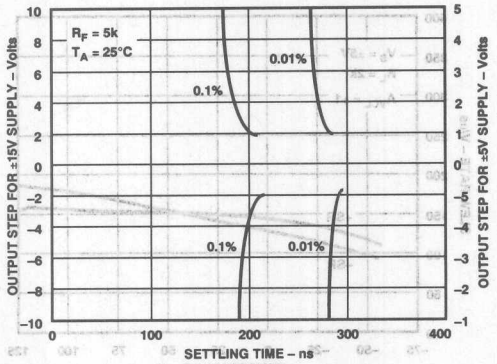


Figure 31. Settling Time vs. Output Step

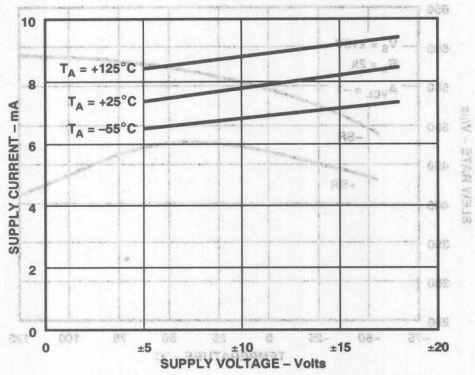


Figure 32. Supply Current vs. Supply Voltage

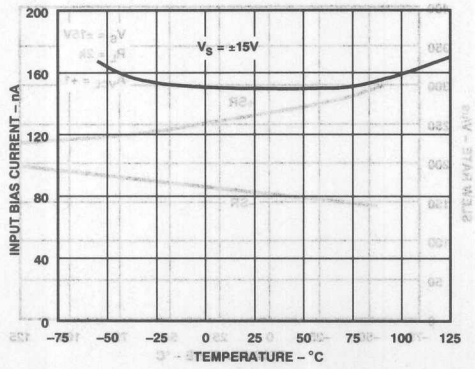


Figure 33. Input Bias Current vs. Temperature

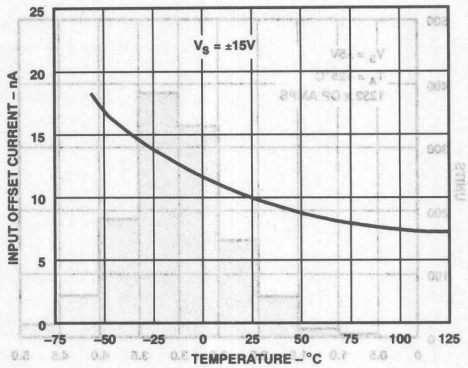


Figure 34. Input Offset Current vs. Temperature

APPLICATIONS INFORMATION

OUTPUT SHORT-CIRCUIT PERFORMANCE

To achieve a wide bandwidth and high slew rate, the OP-467 output is *not* short circuit protected. Shorting the output to ground or to the supplies may destroy the device.

For safe operation, the output load current should be limited so that the junction temperature does not exceed the absolute maximum junction temperature.

To calculate the maximum internal power dissipation, following formula can be used:

$$PD = \frac{T_J\ max - T_A}{\theta_{JA}}$$

where T_J and T_A are junction and ambient temperatures respectively, PD is device internal power dissipation, and θ_{JA} is packaged device thermal resistance given in the data sheet.

UNUSED AMPLIFIERS

It is recommended that any unused amplifiers in a quad package be connected as a unity gain follower with a 1 kΩ feedback resistor with noninverting input tied to the ground plain.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Satisfactory performance of a high speed op amp largely depends on a good PC layout. To achieve the best dynamic performance, following high frequency layout technique is recommended.

GROUNDING

A good ground plain is essential to achieve the optimum performance in high speed applications. It can significantly reduce the undesirable effects of ground loops and IR drops by providing a low impedance reference point. Best results are obtained with a multilayer board design with one layer assigned to ground plain. To maintain a continuous and low impedance ground, avoid running any traces on this layer.

POWER SUPPLY CONSIDERATIONS

In high frequency circuits, device lead length introduces an inductance in series with the circuit. This inductance combined with stray capacitance forms a high frequency resonance circuit. Poles generated by these circuits will cause gain peaking and additional phase shift reducing the op amp's phase margin and leading to an unstable operation.

A practical solution to this problem is to reduce the resonance frequency low enough to take advantage of the amplifier's power supply rejection.

This is easily done by placing capacitors across the supply line and the ground plain as close as possible to the device pin. Since capacitors also have internal parasitic components, such as stray inductance, selecting the right capacitor is important. To be effective, they should have low impedance over the frequency range of interest. Tantalum capacitors are an excellent choice for their high capacitance/size ratio, but their ESR (Effective Series Resistance) increases with frequency making them less effective. On the other hand, ceramic chip capacitors have excellent ESR and ESL (Effective Series Inductance) performance at higher frequencies, and because of their small size, they can be placed very close to the device pin, further reducing the stray inductance. Best results are achieved by using a combination of these two capacitors. A 5–10 μF tantalum parallel with a 0.1 μF ceramic chip caps are recommended. If additional isolation from high frequency resonances of the power supply is needed, a ferrite bead should be placed in series with the supply lines between the bypass caps and the power supply. A word of caution, addition of the ferrite bead will introduce a new pole and zero to frequency response of the circuit and could cause unstable operation if it is not selected properly.

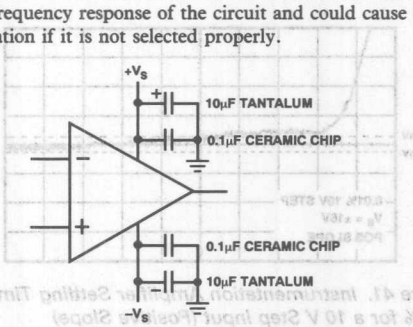


Figure 35. Recommended Power Supply Bypass

SIGNAL CONSIDERATIONS

Input and output traces need special attention to assure a minimum stray capacitance. Input nodes are very sensitive to capacitive reactance, particularly when connected to a high impedance circuit. Stray capacitance can inject undesirable signals from a noisy line into a high impedance input. Protect high impedance input traces by providing guard traces around them. This will also improve the channel separation significantly.

Additionally, any stray capacitance in parallel with the op amp's input capacitance generates a pole in the frequency response of the circuit. The additional phase shift caused by this pole will reduce the circuit's gain margin. If this pole is within the gain range of the op amp, it will cause unstable performance. To reduce these undesirable effects, use the lowest impedance where possible. Lowering the impedance at this node places the poles at a higher frequency, far above the gain range of the amplifier. Stray capacitance on the PC board can be reduced by making the traces narrow and as short as possible. Further reduction can be realized by choosing smaller pad size, increasing the spacing between the traces, and using PC board material with a low dielectric constant insulator (Dielectric Constant of some common insulators: air = 1, Teflon = 2.2, and FR4 = 4.7; with air being an ideal insulator).

Removing segments of the ground plain directly under the input and output pads is recommended.

Outputs of high speed amplifiers are very sensitive to capacitive loads. A capacitive load will introduce a pair of pole and zero to the circuit's frequency response, reducing the phase margin, leading to unstable operation or oscillation.

Generally, it is a good design practice to isolate the amplifier's output from any capacitive load by placing a resistor between the amplifier's output and the rest of the circuits. A series resistor of 10 to 100 ohms is normally sufficient to isolate the output from a capacitive load.

The OP-467 is internally compensated to provide stable operation, and is capable of driving large capacitive loads without oscillation.

Sockets are not recommended since they increase the lead inductance/capacitance and reduce the power dissipation of the package by increasing the leads thermal resistance. If sockets must be used, use Teflon* or pin sockets with the shortest leads possible.

PHASE REVERSAL

The OP-467 is immune to phase reversal; its inputs can exceed the supply rails by a diode drop without any phase reversal.

*Teflon is a registered trademark of E.I. du Pont Co.

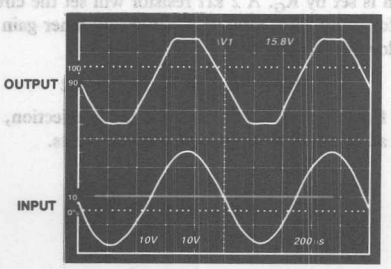


Figure 36. No Phase Reversal (A_V = +1)

high speed instrumentation and measurement circuits, where the amplifier is frequently exposed to large signals that overload the amplifier.

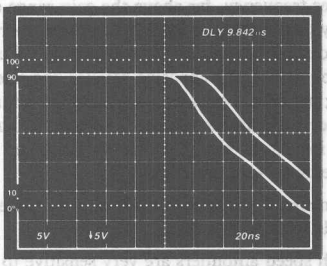


Figure 37. Saturation Recovery Time, Positive Rail

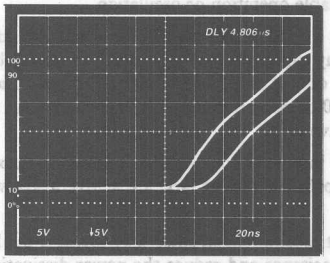


Figure 38. Saturation Recovery Time, Negative Rail

HIGH SPEED INSTRUMENTATION AMPLIFIER

The OP-467 performance lends itself to a variety of high speed applications, including high speed precision instrumentation amplifiers. Figure 39 represents a circuit commonly used for data acquisition, CCD imaging, and other high speed application.

Circuit gain is set by R_G. A 2 kΩ resistor will set the circuit gain to 2, for unity gain, remove R_G. For any other gain settings use the following formula:

$$G = 2/R_G \quad \textit{Resistor Value is in k}\Omega$$

R_C is used for adjusting the dc common-mode rejection, and C_C is used for ac common-mode rejection adjustments.

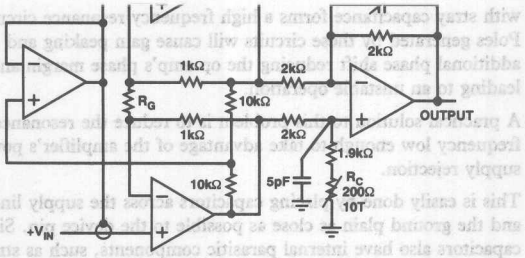


Figure 39. A High Speed Instrumentation Amplifier

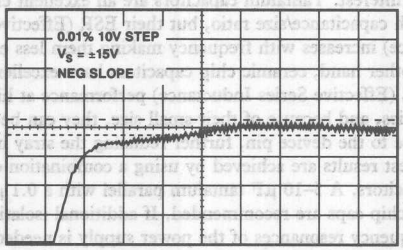


Figure 40. Instrumentation Amplifier Settling Time to 0.01% for a 10 V Step Input (Negative Slope)

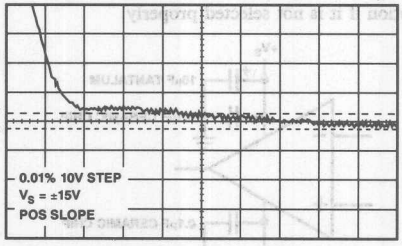


Figure 41. Instrumentation Amplifier Settling Time to 0.01% for a 10 V Step Input (Positive Slope)

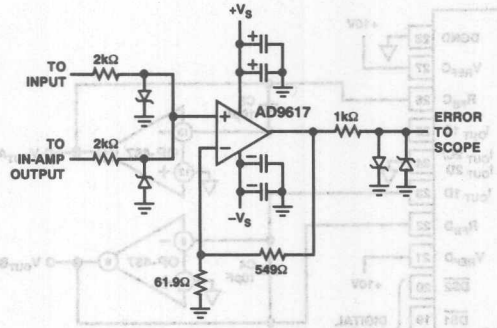


Figure 42. Settling Time Measurement Circuit

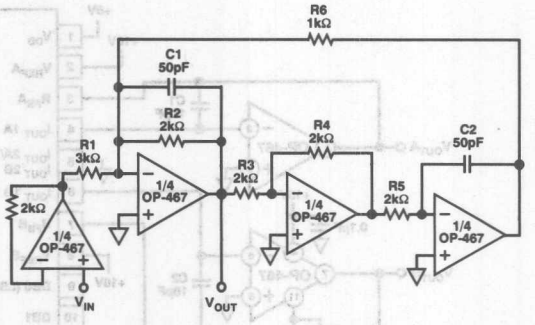


Figure 43. 2 MHz Biquad Filter

2 MHz BIQUAD BANDPASS FILTER

The circuit in Figure 43 is commonly used in medical imaging ultrasound receivers. The 30 MHz bandwidth is sufficient to accurately produce the 2 MHz center frequency, as the measured response shows in Figure 44. When the op amp's bandwidth is too close to the filter's center frequency, the amplifier's internal phase shift causes excess phase shift at 2 MHz, which alters the filter's response. In fact, if the chosen op amp has a bandwidth close to 2 MHz, the combined phase shift of the three op amps will cause the loop to oscillate.

Careful consideration must be given to the layout of this circuit as with any other high speed circuit.

If the phase shift introduced by the layout is large enough, it could alter the circuit performance, or worse, it will oscillate.

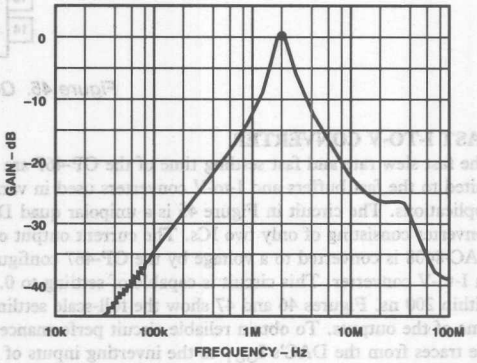


Figure 44. Biquad Filter Response

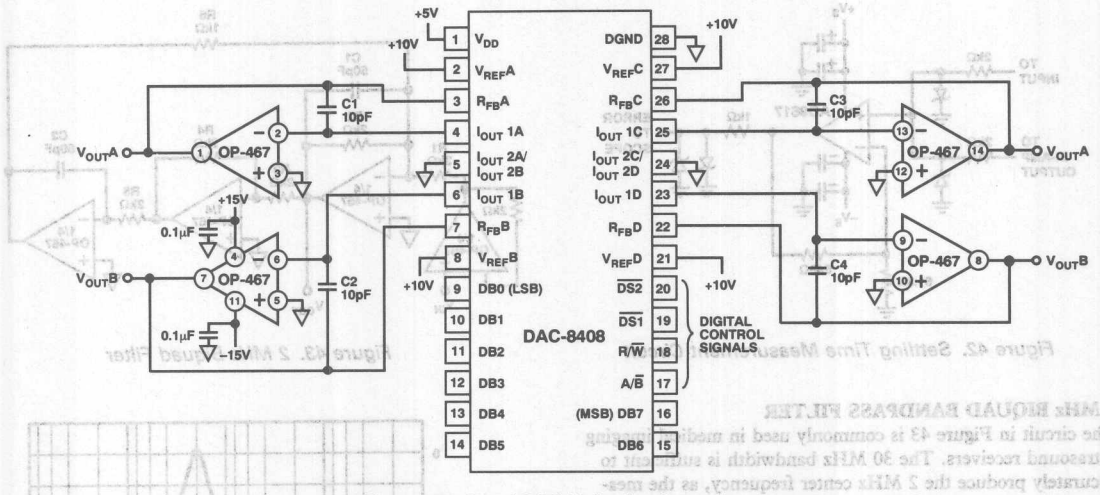


Figure 45. Quad DAC Unipolar Operation

FAST I-TO-V CONVERTER

The fast slew rate and fast settling time of the OP-467 are well suited to the fast buffers and I-to-V converters used in variety of applications. The circuit in Figure 45 is a unipolar quad D/A converter consisting of only two ICs. The current output of the DAC-8408 is converted to a voltage by the OP-467 configured as an I-to-V converter. This circuit is capable of settling to 0.1% within 200 ns. Figures 46 and 47 show the full-scale settling time of the outputs. To obtain reliable circuit performance, keep the traces from the DAC's I_{OUT} to the inverting inputs of the OP-467 short to minimize parasitic capacitance.

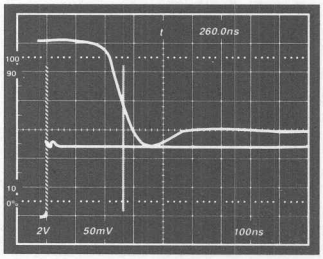


Figure 46. Voltage Output Settling Time

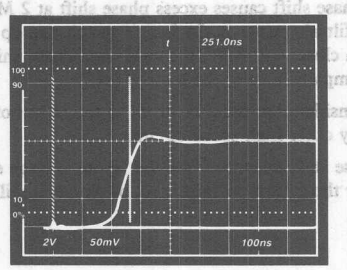


Figure 47. Voltage Output Settling Time

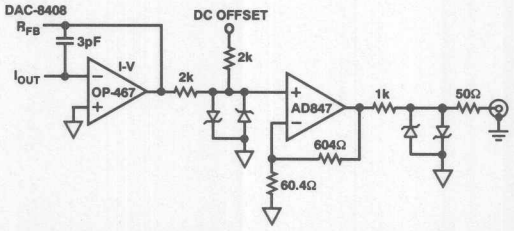


Figure 48. DAC V_{OUT} Settling Time Circuit

OP-467 SPICE MACRO-MODEL

```
* Node assignments
                    noninverting input
                    |   inverting input
                    |   |   positive supply
                    |   |   |   negative supply
                    |   |   |   |   output
                    |   |   |   |   |
*                   |   |   |   |   |
. SUBCKT OP-467     1   2   99  50  27
*
* INPUT STAGE
*
I1      4   50  10E-3
CIN     1   2   1E-12
IOS     1   2   5E-9
Q1      5   2   8   QN
Q2      6   7   9   QN
R3      99  5   185 . 681
R4      99  6   185 . 681
R5      8   4   180 . 508
R6      9   4   180 . 508
EOS     7   1   POLY (1)  (14,20)  50E-6 1
EREF    98  0   (20,0) 1
*
* GAIN STAGE AND DOMINANT POLE AT 1.5 kHz
*
R7      10  98  3 . 714E6
C2      10  98  28 . 571E-12
G1      98  10  (5,6)  5 . 386E-3
V1      99  11  1 . 6
V2      12  50  1 . 6
D1      10  11  DX
D2      12  10  DX
RC      10  28  1 . 4E3
CC      28  27  12E-12
*
* COMMON-MODE STAGE WITH ZERO AT 1.26 kHz
*
ECM     13  98  POLY (2)      (1,20)  (2,20) 0 0 . 5 0 . 5
R8      13  14  1E6
R9      14  98  25 . 119
C3      13  14  126 . 721E-12
*
* POLE AT 400E6
*
R10     15  98  1E6
C4      15  98  0 . 398E-15
G2      98  15  (10,20) 1E-6
*
* OUTPUT STAGE
*
ISY     99  50  −8 . 183E-3
RMP1    99  20  96 . 429E3
RMP2    20  50  96 . 429E3
RO1     99  26  200
RO2     26  50  200
L1      26  27  1E-7
GO1     26  99  (99,15)  5E-3
GO2     50  26  (15,50)  5E-3
G4      23  50  (15,26)  5E-3
G5      24  50  (26,15)  5E-3
V3      21  26  50
V4      26  22  50
D3      15  21  DX
D4      22  15  DX
D5      99  23  DX
D6      99  24  DX
D7      50  23  DY
D8      50  24  DY
*
* MODELS USED
*
. MODEL QN NPN (BF=33.333E3)
. MODEL DX D
. MODEL DY D (BV=50)
. ENDS OP-467
```

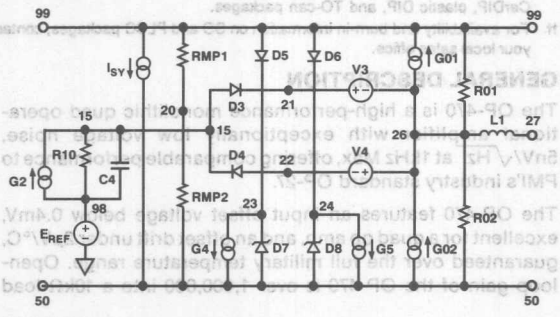


Figure 49. Spice Macro-Model Output Stage

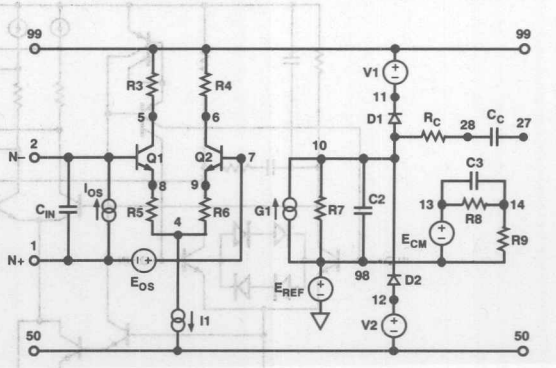


Figure 50. Spice Macro-Model Input and Gain Stage

Very Low Noise Quad Operational Amplifier

OP470

FEATURES

- Very Low Noise ..... 5nV/$\sqrt{Hz}$ @ 1kHz Max
- Excellent Input Offset Voltage ..... 0.4mV Max
- Low Offset Voltage Drift ..... 2μV/°C Max
- Very High Gain ..... 1000V/mV Min
- Outstanding CMR ..... 110dB Min
- Slew Rate ..... 2V/μs Typ
- Gain-Bandwidth Product ..... 6MHz Typ
- Industry Standard Quad Pinouts
- Available in Die Form

ORDERING INFORMATION †

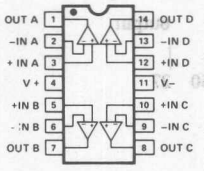
T_A = +25°C V_{OS} MAX (μV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP 14-PIN	PLASTIC	LCC*	
400	–	–	OP470ARC/883	MIL
400	OP470AY*	–	OP470ATC/883	MIL
400	OP470EY	–	–	IND
800	OP470FY	–	–	IND
1000	–	OP470GP	–	XIND
1000	–	OP470GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

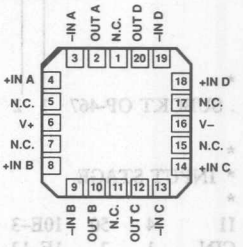
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS

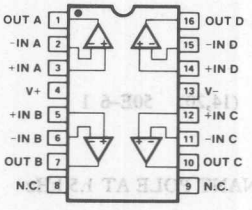


14-PIN HERMETIC DIP
(Y-Suffix)

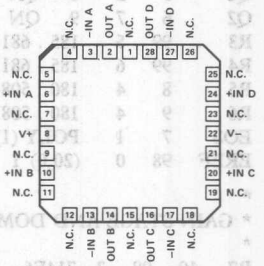
14-PIN PLASTIC MINI-DIP
(P-Suffix)



20-LEAD LCC
(RC-Suffix)



16-PIN SOL
(S-Suffix)



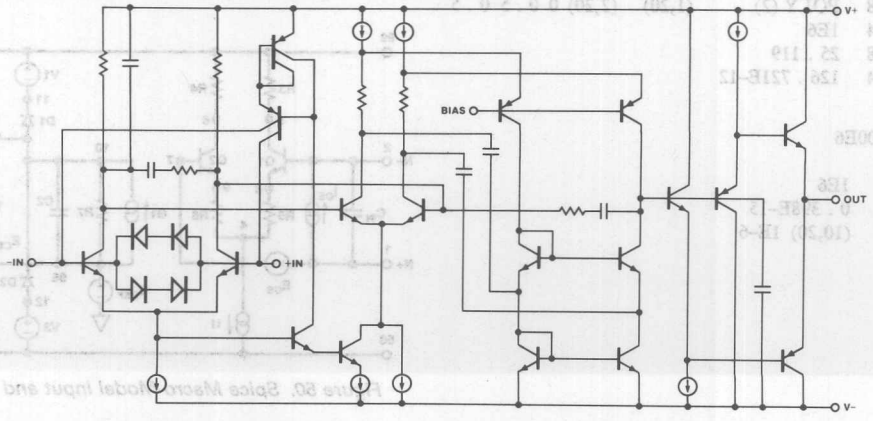
28-LEAD LCC
(TC-Suffix)

GENERAL DESCRIPTION

The OP-470 is a high-performance monolithic quad operational amplifier with exceptionally low voltage noise, 5nV/$\sqrt{Hz}$ at 1kHz Max, offering comparable performance to PMI's industry standard OP-27.

The OP-470 features an input offset voltage below 0.4mV, excellent for a quad op amp, and an offset drift under 2μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP-470 is over 1,000,000 into a 10kΩ load insuring excellent gain accuracy and linearity, even in high-gain applications. Input bias current is under 25nA which reduces errors due to signal source resistance. The OP-470's CMR of over 110dB and PSRR of less than 1.8μV/V significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the quad OP-470 is half that of four OP-27s, a significant advantage for power con-

SIMPLIFIED SCHEMATIC



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scious applications. The OP-470 is unity-gain stable with a gain-bandwidth product of 6MHz and a slew rate of 2V/μs.

The OP-470 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers, and low-noise active filters.

The OP-470 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP-11, LM148/149, HA4741, HA5104, and RM4156 quad op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP-471, with a slew rate of 8V/μs, is recommended.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, TC, Y-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP-470A ..... –55°C to +125°C
OP-470E, OP-470F ..... –25°C to +85°C
OP-470G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	30	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-470's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

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ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			OP-470A/E			OP-470F			OP-470G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.1	0.4	—	0.2	0.8	—	0.4	1.0	mV
Input Offset Current	I_{OS}	V_{CM} = 0V	—	3	10	—	6	20	—	12	30	nA
Input Bias Current	I_B	V_{CM} = 0V	—	6	25	—	15	50	—	25	60	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	80	200	—	80	200	—	80	200	nV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	3.8	6.5	—	3.8	6.5	—	3.8	6.5	$nV/\sqrt{Hz}$
		f_O = 100Hz	—	3.3	5.5	—	3.3	5.5	—	3.3	5.5	
		f_O = 1kHz (Note 2)	—	3.2	5.0	—	3.2	5.0	—	3.2	5.0	
Input Noise Current Density	i_n	f_O = 10Hz	—	1.7	—	—	1.7	—	—	1.7	—	$pA/\sqrt{Hz}$
		f_O = 100Hz	—	0.7	—	—	0.7	—	—	0.7	—	
		f_O = 1kHz	—	0.4	—	—	0.4	—	—	0.4	—	
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V, R_L = 10kΩ	1000	2300	—	800	1700	—	800	1700	—	V/mV
		R_L = 2kΩ	500	1200	—	400	900	—	400	900	—	
Input Voltage Range	IVR	(Note 3)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	110	125	—	100	120	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	0.56	1.8	—	1.0	5.6	—	1.0	5.6	μV/V
Slew Rate	SR		1.4	2	—	1.4	2	—	1.4	2	—	V/μs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9	11	—	9	11	—	9	11	mA
Gain Bandwidth Product	GBW	A_V = +10	—	6	—	—	6	—	—	6	—	MHz
Channel Separation	CS	V_O = 20V_{p-p} f_O = 10Hz (Note 1)	125	155	—	125	155	—	125	155	—	dB
Input Capacitance	C_{IN}		—	2	—	—	2	—	—	2	—	pF
Input Resistance Differential-Mode	R_{IN}		—	0.4	—	—	0.4	—	—	0.4	—	MΩ
Input Resistance Common-Mode	R_{INCM}		—	11	—	—	11	—	—	11	—	GΩ
Settling Time	t_s	A_V = +1 to 0.1%	—	5.5	—	—	5.5	—	—	5.5	—	μs
		to 0.01%	—	6.0	—	—	6.0	—	—	6.0	—	

NOTES:
1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, −55°C ≤ T_A ≤ 125°C for OP-470A, unless otherwise noted.

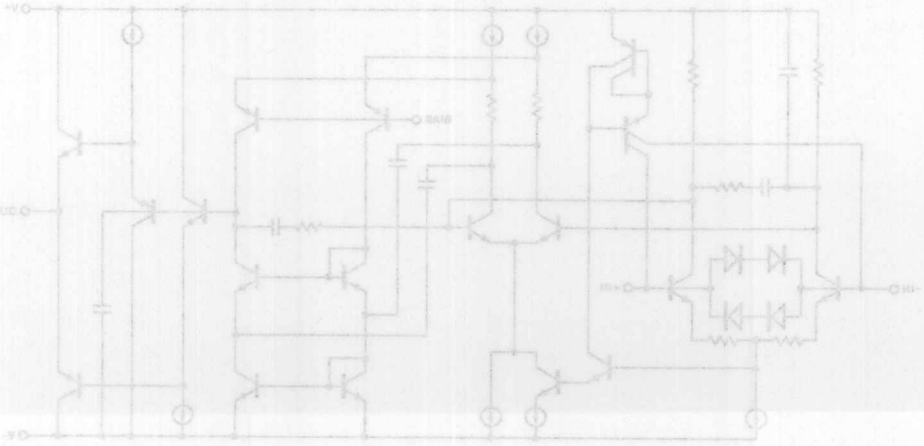
PARAMETER	SYMBOL	CONDITIONS	OP-470A MIN	OP-470A TYP	OP-470A MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.14	0.6	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	μV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	—	5	20	nA
Input Bias Current	I_B	V_{CM} = 0V	—	15	50	nA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10kΩ R_L = 2kΩ	750 400	1600 800	— —	V/mV
Input Voltage Range	IVR	(Note 1)	±11	±12	—	V
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	100	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	1.0	5.6	μV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	mA

NOTE:
1. Guaranteed by CMR test.

PARAMETER	SYMBOL	CONDITIONS	OP-470E MIN	OP-470E TYP	OP-470E MAX	OP-470F MIN	OP-470F TYP	OP-470F MAX	OP-470G MIN	OP-470G TYP	OP-470G MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.12	0.5	—	0.24	1.0	—	0.5	1.5	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	—	0.6	4	—	2	—	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	—	4	20	—	7	40	—	20	50	nA
Input Bias Current	I_B	V_{CM} = 0V	—	11	50	—	20	70	—	40	75	nA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10kΩ R_L = 2kΩ	800 400	1800 900	— —	600 300	1400 700	— —	600 300	1500 800	— —	V/mV
Input Voltage Range	IVR	(Note 1)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	100	120	—	90	115	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	0.7	5.6	—	1.8	10	—	1.8	10	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	—	9.2	11	—	9.3	11	mA

NOTE:
1. Guaranteed by CMR test.

9



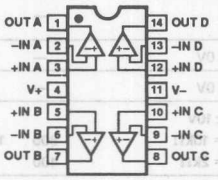
High Speed, Low Noise Quad Operational Amplifier

OP471

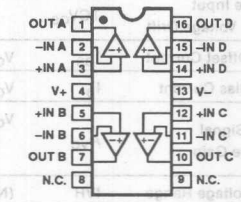
FEATURES

- Excellent Speed ..... 8V/μs Typ
- Low Noise ..... 11nV/√Hz @ 1kHz Max
- Unity-Gain Stable
- High Gain-Bandwidth ..... 6.5MHz Typ
- Low Input Offset Voltage ..... 0.8mV Max
- Low Offset Voltage Drift ..... 4μV/° C Max
- High Gain ..... 500V/mV Min
- Outstanding CMR ..... 105 dB Min
- Industry Standard Quad Pinouts
- Availiable in Die Form

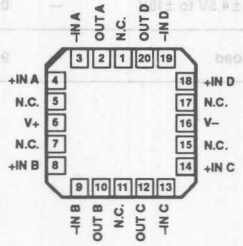
PIN CONNECTIONS



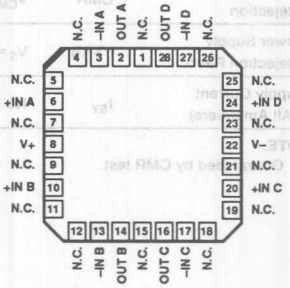
14-PIN HERMETIC DIP
(Y-Suffix)
14-PIN PLASTIC DIP
(P-Suffix)



16-PIN SOL
(S-Suffix)



20-LEAD LCC
(RC-Suffix)



28-LEAD LCC
(TC-Suffix)

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP	PLASTIC	LCC*	
800	OP471AY*	–	OP471ATC/883	MIL
800	–	–	OP471ARC/883	MIL
800	OP471EY	–	–	IND
1500	OP471FY	–	–	IND
1800	–	OP471GP	–	XIND
1800	–	OP471GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

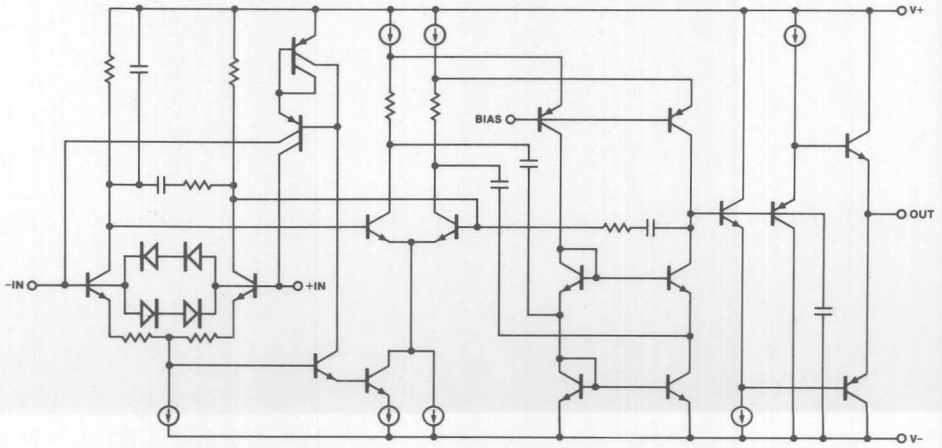
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-471 is a monolithic quad op amp featuring low noise, 11nV/√Hz Max @ 1kHz, excellent speed, 8V/μs typical, a gain-bandwidth of 6.5MHz, and unity-gain stability.

The OP-471 has an input offset voltage under 0.8mV and an input offset voltage drift below 4μV/°C, guaranteed over the full military temperature range. Open loop gain of the OP-471 is over 500,000 into a 10kΩ load insuring outstanding gain accuracy and linearity. The input bias current is under 25nA

SIMPLIFIED SCHEMATIC (One of four amplifiers is shown.)



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limiting errors due to signal source resistance. The OP-471's CMR of over 105dB and PSRR of under 5.6μV/V significantly reduce errors caused by ground noise and power supply fluctuations.

The OP-471 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers and low-noise active filters.

The OP-471 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP-11, LM148/149, HA4741, RM4156, MC33074, TL084 and TL074 quad op amps and can be used to upgrade systems using these devices.

For applications requiring even lower voltage noise the OP-470, with a voltage density of 5nV/$\sqrt{\text{Hz}}$ Max @ 1kHz, is recommended.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 3) ..... ±1.0V
Differential Input Current (Note 3) ..... ±25mW
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, RC, TC, Y-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP-471A ..... –55°C to +125°C
OP-471E, OP-471F ..... –25°C to +85°C
OP-471G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	30	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.
3. The OP-471's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.

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ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			OP-471A/E			OP-471F			OP-471G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.25	0.8	—	0.5	1.5	—	1.0	1.8	mV
Input Offset Current	I_{OS}	V_{CM} = 0V	—	4	10	—	7	20	—	12	30	nA
Input Bias Current	I_B	V_{CM} = 0V	—	7	25	—	15	50	—	25	60	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	250	500	—	250	500	—	250	500	nV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	9	16	—	9	16	—	9	16	$nV/\sqrt{Hz}$
		f_O = 100Hz	—	7	12	—	7	12	—	7	12	
		f_O = 1kHz (Note 2)	—	6.5	11	—	6.5	11	—	6.5	11	
Input Noise Current Density	i_n	f_O = 10Hz	—	1.7	—	—	1.7	—	—	1.7	—	$pA/\sqrt{Hz}$
		f_O = 100Hz	—	0.7	—	—	0.7	—	—	0.7	—	
		f_O = 1kHz	—	0.4	—	—	0.4	—	—	0.4	—	
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V										
		R_L = 10kΩ	500	700	—	300	500	—	300	500	—	V/mV
		R_L = 2kΩ	350	550	—	175	275	—	175	275	—	
Input Voltage Range	IVR	(Note 3)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	105	120	—	95	115	—	95	115	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	1	5.6	—	5.6	17.8	—	5.6	17.8	μV/V
Slew Rate	SR		6.5	8	—	6.5	8	—	6.5	8	—	V/μs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	—	9.2	11	—	9.2	11	mA
Gain-Bandwidth Product	GBW	A_V = +10	—	6.5	—	—	6.5	—	—	6.5	—	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$, f_O = 10Hz (Note 1)	125	150	—	125	150	—	125	150	—	dB
Input Capacitance	C_{IN}		—	2.6	—	—	2.6	—	—	2.6	—	pF
Input Resistance Differential-Mode	R_{IN}		—	1.1	—	—	1.1	—	—	1.1	—	MΩ
Input Resistance Common-Mode	R_{INCM}		—	11	—	—	11	—	—	11	—	GΩ
Settling Time	t_s	A_V = +1 to 0.1%	—	4.5	—	—	4.5	—	—	4.5	—	μs
		to 0.01%	—	7.5	—	—	7.5	—	—	7.5	—	

NOTES:
1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, −55°C ≤ T_A ≤ 125°C for OP-471A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-471A MIN	OP-471A TYP	OP-471A MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.4	1.2	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1	4	μV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	—	6	20	nA
Input Bias Current	I_B	V_{CM} = 0V	—	16	50	nA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V, R_L = 10kΩ	375	500	—	V/mV
		R_L = 2kΩ	250	350	—	
Input Voltage Range	IVR	(Note 1)	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	100	115	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	5.6	10	μV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.3	11	mA

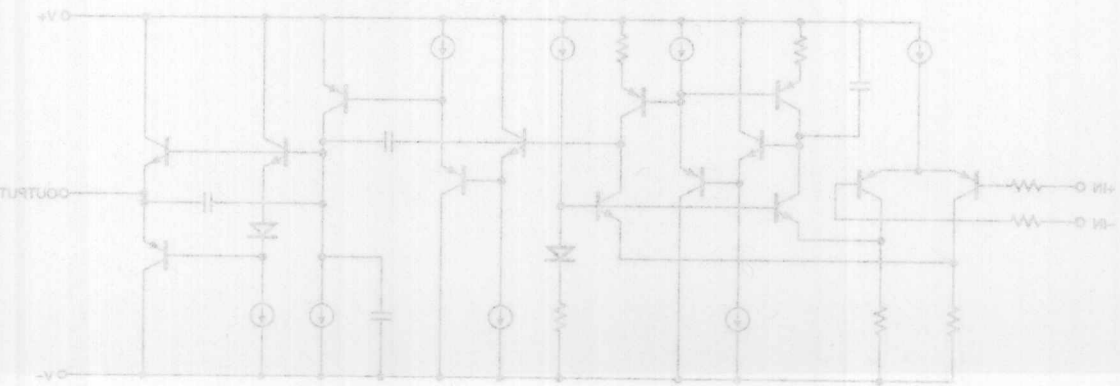
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-471E/F, $-40°C \le T_A \le +85°C$ for OP-471G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-471E MIN	OP-471E TYP	OP-471E MAX	OP-471F MIN	OP-471F TYP	OP-471F MAX	OP-471G MIN	OP-471G TYP	OP-471G MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.3	1.1	—	0.6	2.0	—	1.2	2.5	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1	4	—	2	7	—	4	—	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	5	20	—	8	40	—	20	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	13	50	—	25	70	—	40	75	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	375 250	600 400	—	200 125	400 200	—	200 125	400 200	—	V/mV
Input Voltage Range	IVR	(Note 1)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	3.2	10	—	18	31.6	—	18	31.6	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.3	11	—	9.3	11	—	9.3	11	mA

NOTE:
1. Guaranteed by CMR test.

9



Low-Voltage Micropower Quad Operational Amplifier

OP490

FEATURES

- Single/Dual Supply Operation ..... +1.6V to +36V
  ..... ±0.8V to ±18V
- True Single-Supply Operation; Input and Output Voltage Ranges Include Ground
- Low Supply Current ..... 80µA Max
- High Output Drive ..... 5mA Min
- Low Offset Voltage ..... 0.5mA Max
- High Open-Loop Gain ..... 700V/mV Min
- Outstanding PSRR ..... 5.6µV/V Min
- Industry Standard Quad Pinouts
- Available in Die Form

ORDERING INFORMATION †

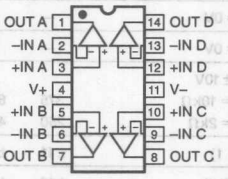
T_A = +25°C V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP 14-PIN	PLASTIC	LCC 28-CONTACT	
0.5	OP490AY*	–	OP490ATC/883	MIL
0.5	OP490EY	–	–	IND
0.75	OP490FY	–	–	IND
1.0	–	OP490GP	–	XIND
1.0	–	OP490GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

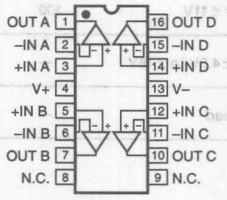
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS

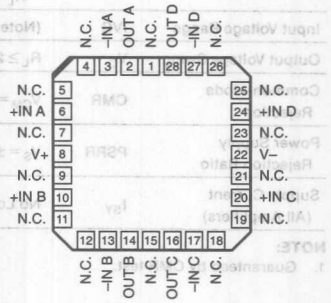


14-PIN HERMETIC DIP (Y-Suffix)

14-PIN PLASTIC DIP (P-Suffix)



16-PIN SOL (S-Suffix)



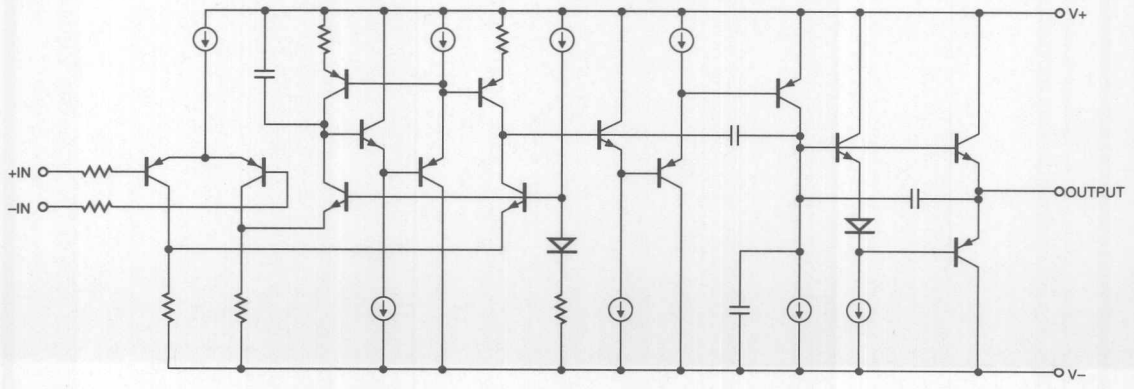
28-PIN LCC (TC-Suffix)

GENERAL DESCRIPTION

The OP-490 is a high-performance micropower quad op amp that operates from a single supply of +1.6V to +36V or from dual supplies of ±0.8V to ±18V. Input voltage range includes the negative rail allowing the OP-490 to accommodate input signals down to ground in single-supply operation. The OP-490's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

Continued

SIMPLIFIED SCHEMATIC (One of four amplifiers is shown.)



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

GENERAL DESCRIPTION *Continued*

The quad OP-490 draws less than 20μA of quiescent supply current per amplifier, but each amplifier is able to deliver over 5mA of output current to a load. Input offset voltage is under 0.5mV with offset drift below 5μV/°C over the military temperature range. Gain exceeds over 700,000 and CMR is better than 100dB. A PSRR of under 5.6μV/V minimizes offset voltage changes experienced in battery powered systems.

The quad OP-490 combines high performance with the space and cost savings of quad amplifiers. The minimal voltage and current requirements of the OP-490 makes it ideal for battery and solar powered applications, such as portable instruments and remote sensors.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Differential Input Voltage ..... [(V–) – 20V] to [(V+) + 20V]
Common-Mode Input Voltage ..... [(V–) – 20V] to [(V+) + 20V]
Output Short-Circuit Duration ..... Continuous

Storage Temperature Range
TC, Y, P Package ..... –65°C to +150°C
Operating Temperature Range
OP-490A ..... –55°C to +125°C
OP-490E, OP-490F ..... –25°C to +85°C
OP-490G ..... –40°C to +85°C
Junction Temperature (Tj) ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	99	12	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
28-Contact LCC (TC)	78	30	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.
2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±1.5V to ±15V, T_A = +25°C, unless otherwise noted.

			OP-490A/E			OP-490F			OP-490G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.2	0.5	–	0.4	0.75	–	0.6	1.0	mV
Input Offset Current	I_{OS}	V_{CM} = 0V	–	0.4	3	–	0.4	5	–	0.4	5	nA
Input Bias Current	I_B	V_{CM} = 0V	–	4.2	15	–	4.2	20	–	4.2	25	nA
Large-Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V										
		R_L = 100kΩ	700	1200	–	500	1000	–	400	800	–	V/mV
		R_L = 10kΩ	350	600	–	250	500	–	200	400	–	
		R_L = 2kΩ	125	250	–	100	200	–	100	200	–	
		V+ = 5V, V– = 0V, 1V < V_O < 4V										
		R_L = 100kΩ	200	400	–	125	300	–	100	250	–	
		R_L = 10kΩ	100	180	–	75	140	–	70	140	–	
Input Voltage Range	IVR	V+ = 5V, V– = 0V	0/4	–	–	0/4	–	–	0/4	–	–	V
		V_S = ±15V (Note 1)	–15/13.5	–	–	–15/13.5	–	–	–15/13.5	–	–	
Output Voltage Swing	V_O	V_S = ±15V										
		R_L = 10kΩ	±13.5	±14.2	–	±13.5	±14.2	–	±13.5	±14.2	–	V
		R_L = 2kΩ	±10.5	±11.5	–	±10.5	±11.5	–	±10.5	±11.5	–	
	V_{OH}	V+ = 5V, V– = 0V										V
		R_L = 2kΩ	4.0	4.2	–	4.0	4.2	–	4.0	4.2	–	
	V_{OL}	V+ = 5V, V– = 0V										μV
		R_L = 10kΩ	–	100	500	–	100	500	–	100	500	
Common-Mode Rejection	CMR	V+ = 5V, V– = 0V, 0V < V_{CM} < 4V	90	110	–	80	100	–	80	100	–	dB
		V_S = ±15V, –15V < V_{CM} < 13.5V	100	130	–	90	120	–	90	120	–	
Power Supply Rejection Ratio	PSRR		–	1.0	5.6	–	3.2	10	–	3.2	10	μV/V
Slew Rate	SR	V_S = ±15V	5	12	–	5	12	–	5	12	–	V/ms
Supply Current (All Amplifiers)	I_{SY}	V_S = 1.5V No Load	–	40	60	–	40	60	–	40	60	μA
		V_S = ±15V No Load	–	60	80	–	60	80	–	60	80	
Capacitive Load Stability		A_V = +1	–	650	–	–	650	–	–	650	–	pF
Input Noise Voltage	e_{np-p}	f_O = 0.1Hz to 10Hz, V_S = ±15V	–	3	–	–	3	–	–	3	–	μV_{p-p}

PARAMETER	SYMBOL	CONDITIONS	OP-490A/E MIN	OP-490A/E TYP	OP-490A/E MAX	OP-490F MIN	OP-490F TYP	OP-490F MAX	OP-490G MIN	OP-490G TYP	OP-490G MAX	UNITS
Input Resistance Differential Mode	R_{IN}	V_S = ±15V	–	30	–	–	30	–	–	30	–	MΩ
Input Resistance Common Mode	R_{INCM}	V_S = ±15V	–	20	–	–	20	–	–	20	–	GΩ
Gain Bandwidth Product	GBWP	A_V = +1	–	20	–	–	20	–	–	20	–	kHz
Channel Separation	CS	f_O = 10Hz V_O = 20V V_S = ±15V (Note 2)	120	150	–	120	150	–	120	150	–	dB

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed but not 100% tested.

ELECTRICAL CHARACTERISTICS at V_S = ±1.5V to ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-490A MIN	OP-490A TYP	OP-490A MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.4	1.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	V_S = ±15V	–	2	5	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1.5	5	nA
Input Bias Current	I_B	V_{CM} = 0V	–	4.4	20	nA
Large-Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V R_L = 100kΩ	225	400	–	V/mV
		R_L = 10kΩ	125	240	–	
		R_L = 2kΩ	50	110	–	
		V+ = 5V, V– = 0V, 1V < V_O < 4V R_L = 100kΩ	100	200	–	
		R_L = 10kΩ	50	110	–	
Input Voltage Range	IVR	V+ = 5V, V– = 0V	0/3.5	–	–	V
		V_S = ±15V (Note 1)	–15/13.5	–	–	
Output Voltage Swing	V_O	V_S = ±15V R_L = 10kΩ	±13	±13.7	–	V
		R_L = 2kΩ	±10	±11	–	
	V_{OH}	V+ = 5V, V– = 0V R_L = 2kΩ	3.9	4.1	–	V
	V_{OL}	V+ = 5V, V– = 0V R_L = 10kΩ	–	100	500	µV
Common-Mode Rejection	CMR	V+ = 5V, V– = 0V, 0V < V_{CM} < 3.5V	85	105	–	dB
		V_S = ±15V, –15V < V_{CM} < 13.5V	95	115	–	
Power Supply Rejection Ratio	PSRR		–	3.2	10	µV/V
Supply Current (All Amplifiers)	I_{SY}	V_S = ±1.5V No Load	–	70	100	µA
		V_S = ±15V	–	90	120	

NOTE:
1. Guaranteed by CMR test.

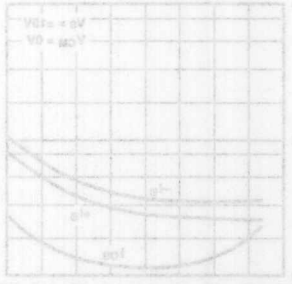
ELECTRICAL CHARACTERISTICS

at $V_S = \pm1.5V$ to $\pm15V$, $-25°C \le T_A \le +85°C$ for OP-490E/F, $-40°C \le T_A \le +85°C$ for OP-490G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-490E MIN	OP-490E TYP	OP-490E MAX	OP-490F MIN	OP-490F TYP	OP-490F MAX	OP-490G MIN	OP-490G TYP	OP-490G MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.32	0.8	–	0.6	1.35	–	0.8	1.5	mV
Average Input Offset Voltage Drift	TCV_{OS}	$V_S = \pm15V$	–	2	5	–	4	–	–	4	–	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	0.8	3	–	1.0	5	–	1.3	7	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	4.4	15	–	4.4	20	–	4.4	25	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_O = \pm10V$										V/mV
		$R_L = 100k\Omega$	500	800	–	350	700	–	300	600	–	
		$R_L = 10k\Omega$	250	400	–	175	350	–	150	250	–	
		$R_L = 2k\Omega$	100	200	–	75	150	–	75	125	–	
		V+ = 5V, V– = 0V, $1V < V_O < 4V$										
		$R_L = 100k\Omega$	150	280	–	100	220	–	80	160	–	
		$R_L = 10k\Omega$	75	140	–	50	110	–	40	90	–	
Input Voltage Range	IVR	V+ = 5V, V– = 0V	0/3.5	–	–	0/3.5	–	–	0/3.5	–	–	V
		$V_S = \pm15V$ (Note 1)	–15/13.5	–	–	–15/13.5	–	–	–15/13.5	–	–	
Output Voltage Swing	V_O	$V_S = \pm15V$										V
		$R_L = 10k\Omega$	±13	±14	–	±13	±14	–	±13	±14	–	
		$R_L = 2k\Omega$	±10	±11	–	±10	±11	–	±10	±11	–	
	V_{OH}	V+ = 5V, V– = 0V										V
		$R_L = 2k\Omega$	3.9	4.1	–	3.9	4.1	–	3.9	4.1	–	
	V_{OL}	V+ = 5V, V– = 0V										µV
		$R_L = 10k\Omega$	–	100	500	–	100	500	–	100	500	
Common-Mode Rejection	CMR	V+ = 5V, V– = 0V, $0V < V_{CM} < 3.5V$	90	110	–	80	100	–	80	100	–	dB
		$V_S = \pm15V$, $-15V < V_{CM} < 13.5V$	100	120	–	90	110	–	90	110	–	
Power Supply Rejection Ratio	PSRR		–	1.0	5.6	–	3.2	10	–	5.6	17.8	µV/V
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm1.5V$ No Load	–	65	100	–	65	100	–	60	100	µA
		$V_S = \pm15V$ No Load	–	80	120	–	80	120	–	75	120	

NOTE:

1. Guaranteed by CMR test.



Precision Picoampere Input Current Quad Operational Amplifier

OP497

FEATURES

- Low Offset Voltage: 50 μV max
- Low Offset Voltage Drift: 0.5 μV/°C max
- Very Low Bias Current
  - +25°C: 100 pA max
  - −55°C to +125°C: 450 pA max
- Very High Open-Loop Gain: 2000 V/mV min
- Low Supply Current (per Amplifier): 625 μA max
- Operates from ±2 V to ±20 V Supplies
- High Common-Mode Rejection: 120 dB min

APPLICATIONS

- Strain Gage and Bridge Amplifiers
- High Stability Thermocouple Amplifiers
- Instrumentation Amplifiers
- Photo-Current Monitors
- High-Gain Linearity Amplifiers
- Long-Term Integrators/Filters
- Sample-and-Hold Amplifiers
- Peak Detectors
- Logarithmic Amplifiers
- Battery-Powered Systems

GENERAL DESCRIPTION

The OP-497 is a quad op amp with precision performance in the space saving, industry standard 16-pin SOIC package. Its combination of exceptional precision with low power and extremely low input bias current makes the quad OP-497 useful in a wide variety of applications.

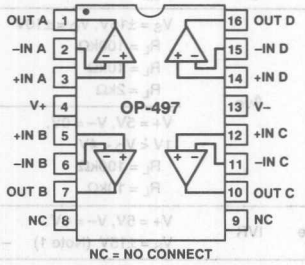
Precision performance of the OP-497 includes very low offset, under 50 μV, and low drift, below 0.5 μV/°C. Open-loop gain exceeds 2000 V/mV insuring high linearity in every application. Errors due to common-mode signals are eliminated by the OP-497's common-mode rejection of over 120 dB. The OP-497's power supply rejection of over 120 dB minimizes offset voltage changes experienced in battery powered systems. Supply current of the OP-497 is under 625 μA per amplifier, and it can operate with supply voltages as low as ±2 V.

The OP-497 utilizes a superbeta input stage with bias current cancellation to maintain picoamp bias currents at all temperatures. This is in contrast to FET input op amps whose bias currents start in the picoamp range at 25°C, but double for every 10°C rise in temperature, to reach the nanoamp range above 85°C. Input bias current of the OP-497 is under 100 pA at 25°C and is under 450 pA over the military temperature range.

Combining precision, low power and low bias current, the OP-497 is ideal for a number of applications including instrumentation amplifiers, log amplifiers, photo-diode preamplifiers and long term integrators. For a single device see the OP-97, for a dual see the OP-297.

PIN CONNECTIONS

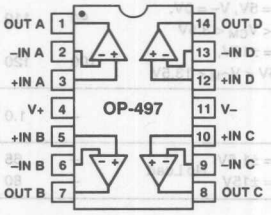
16-Lead Wide Body SOIC
(S Suffix)



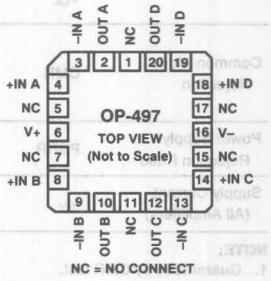
NC = NO CONNECT

14-Lead Plastic Dip
(P Suffix)

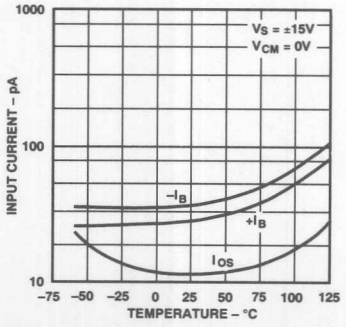
14-Lead Ceramic Dip
(Y Suffix)



20-Position Chip Carrier
(RC Suffix)



NC = NO CONNECT



Input Bias, Offset Current vs. Temperature

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Condition	A Min	A Typ	A Max	B/F Min	B/F Typ	B/F Max	C/G Min	C/G Typ	C/G Max	Units
INPUT CHARACTERISTICS												
Offset Voltage	V_{OS}			20	50		40	75		80	150	µV
		−40°C < T_A < +85°C					70	150		120	250	
		−55°C < T_A < +125°C		40	100		80	150		140	300	
Average Input Offset Voltage Drift	TCV_{OS}	T_{min}–T_{max}		0.2	0.5		0.4	1.0		0.6	1.5	µV/°C
Long Term Input Offset Voltage Stability				0.1			0.1			0.1		µV/Mo
Input Bias Current	I_B	V_{CM} = 0 V		30	100		40	150		60	200	pA
		−40°C < T_A < +85°C					60	200		80	300	
		−55°C < T_A < +125°C		80	450		110	600		130	600	
Average Input Bias Current Drift	TC_{IB}	−40°C < T_A < +85°C					0.3			0.3		
		−55°C < T_A < +125°C		0.5			0.7			0.7		pA/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		15	100		30	150		50	200	pA
		−40°C < T_A < +85°C					50	200		80	300	
		−55°C < T_A < +125°C		35	400		60	600		90	600	
Average Input Offset Current Drift	T_CI_{OS}			0.2			0.3			0.4		pA/°C
Input Voltage Range[1]	IVR		±13	±14		±13	±14		±13	±14		V
		T_{min}–T_{max}	±13	±13.5		±13	±13.5		±13	±13.5		
Common-Mode Rejection	CMR	V_{CM} = ±13 V	120	140		114	135		114	135		dB
		T_{min}–T_{max}	114	130		108	120		108	120		
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V R_L = 2 kΩ	2000	6000		1500	4000		1200	4000		V/mV
		−40°C ≤ T_A ≤ +85°C				800	2000		800	2000		
		−55°C ≤ T_A ≤ +125°C	1200	4000		1000	3000		800	3000		
Input Resistance Differential Mode	R_{IN}			30			30			30		MΩ
Input Resistance Common Mode	R_{INCM}			500			500			500		GΩ
Input Capacitance	C_{IN}			3			3			3		pF
OUTPUT CHARACTERISTICS												
Output Voltage Swing	V_O	R_L = 2 kΩ	±13	±13.7		±13	±13.7		±13	±13.7		V
		R_L = 10 kΩ	±13	±14		±13	±14		±13	±14		
		T_{min}–T_{max}, R_L = 10 kΩ	±13	±13.5		±13	±13.5		±13	±13.5		
Short Circuit	I_{SC}			±25			±25			±25		mA
POWER SUPPLY												
Power Supply Rejection Ratio	PSRR	V_S = ±2 V to ±20 V	120	140		114	135		114	135		dB
		V_S = ±2.5 V to ±20 V										
		T_{min}–T_{max}	114	130		108	120		108	120		
Supply Current (per Amplifier)	I_{SY}	No Load		525	625		525	625		525	625	µA
		T_{min}–T_{max}		580	750		580	750		580	750	
Supply Voltage Range	V_S	Operating Range	±2		±20	±2		±20	±2		±20	V
		T_{min}–T_{max}	±2.5		±20	±2.5		±20	±2.5		±20	
DYNAMIC PERFORMANCE												
Slew Rate	SR		0.05	0.15		0.05	0.15		0.05	0.15		V/µs
Gain Bandwidth Product	GBW			500			500			500		kHz
Channel Separation	CS	V_O = 20 V p–p fo = 10 Hz		150			150			150		dB
NOISE PERFORMANCE												
Voltage Noise	e_n p–p	0.1 Hz to 10 Hz		0.3			0.3			0.3		µV p–p
Voltage Noise Density	e_n = 10 Hz			17			17			17		nV/√Hz
	e_n = 1 kHz			15			15			15		nV/√Hz
Current Noise Density	i_n = 10 Hz			20			20			20		fA/√Hz

NOTE
[1]Guaranteed by CMR Test.
Specifications subject to change without notice.

9

Parameter	Symbol	Condition	OP-497 GBC Limit	Units
Input Offset Voltage	V_{OS}		150	μV max
Input Offset Current	I_{OS}	V_{CM} = 0 V	150	pA max
Input Bias Current	I_B	V_{CM} = 0 V	150	pA max
Input Voltage Range[1]	IVR		±13	V min
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V, $R_L \leq 10$ kΩ	1500	V/mV min
Common-Mode Rejection	CMR	V_{CM} = ±13 V	114	dB min
Power Supply Rejection	PSR	V_S = ±2 V to ±20 V	114	dB min
Output Voltage Swing	V_O	$R_L \leq 10$ kΩ	±13	V min
		$R_L \leq 2$ kΩ	±13	V min
Supply Current per Amplifier	I_{SY}	No Load	625	μA max

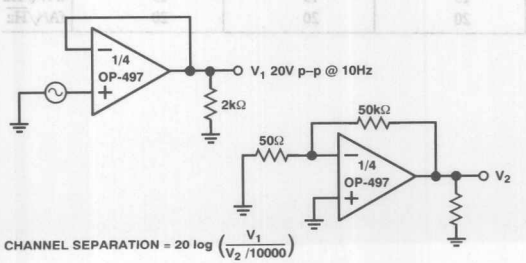
NOTE
[1]Guaranteed by CMR test. Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±20 V
Input Voltage[2] . . . . . ±20 V
Differential Input Voltage[2] . . . . . 40 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
  Y, RC Package . . . . . −65°C to +175°C
  P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
  OP-497A, B, C (Y) . . . . . −55°C to +125°C
  OP-497F, G (Y) . . . . . −40°C to +85°C
  OP-497F, G (P, S) . . . . . −40°C to +85°C
Junction Temperature
  Y, RC Package . . . . . −65°C to +175°C
  P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
14-Pin Cerdip (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	33	°C/W
16-Pin SOIC (S)	92	23	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.



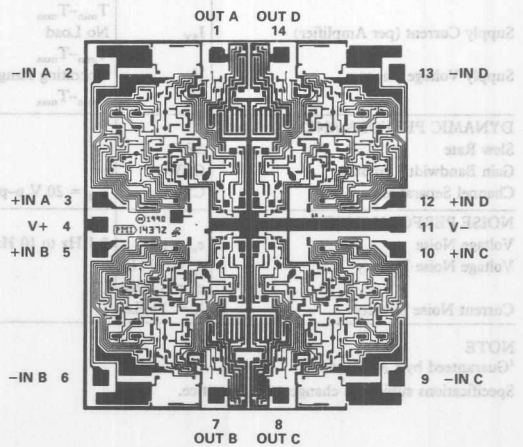
Channel Separation Test Circuit

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP497AY	−55°C to +125°C	14-Pin Cerdip	Q-14
OP497BY	−55°C to +125°C	14-Pin Cerdip	Q-14
OP497CY	−55°C to +125°C	14-Pin Cerdip	Q-14
OP497BRC/883	−55°C to +125°C	20-Contact LCC	E-20A
OP497FY	−40°C to +85°C	14-Pin Cerdip	Q-14
OP497FP	−40°C to +85°C	14-Pin Plastic DIP	N-14
OP497FS	−40°C to +85°C	16-Pin SOIC	R-16
OP497GY	−40°C to +85°C	14-Pin Cerdip	Q-14
OP497GP	−40°C to +85°C	14-Pin Plastic DIP	N-14
OP497GS	−40°C to +85°C	16-Pin SOIC	R-16

*For outline information see Package Information section.

DICE CHARACTERISTICS



Die Size 0.112 × 0.129 inch, 14,448 sq. mils

Instrumentation Amplifiers
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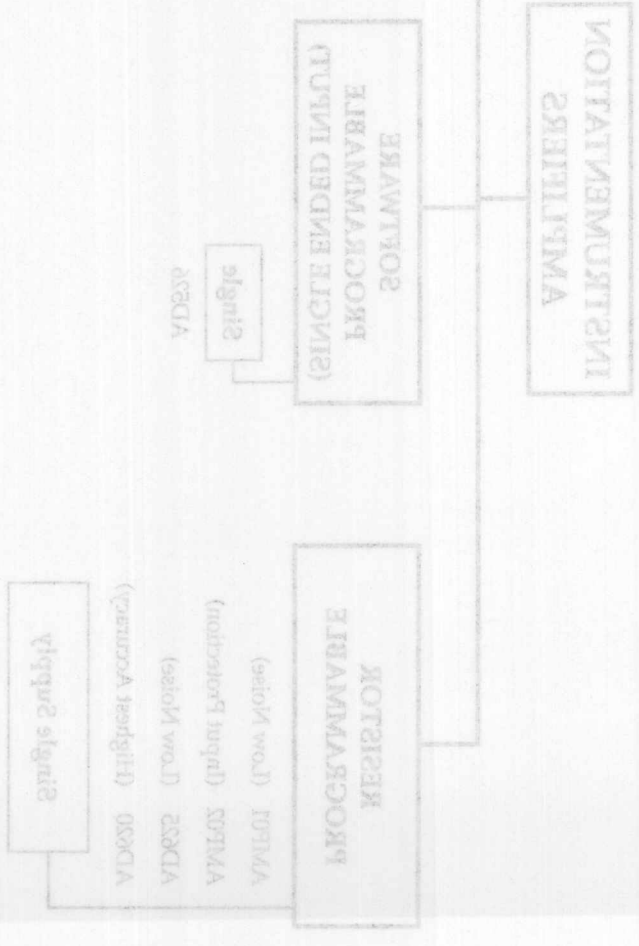
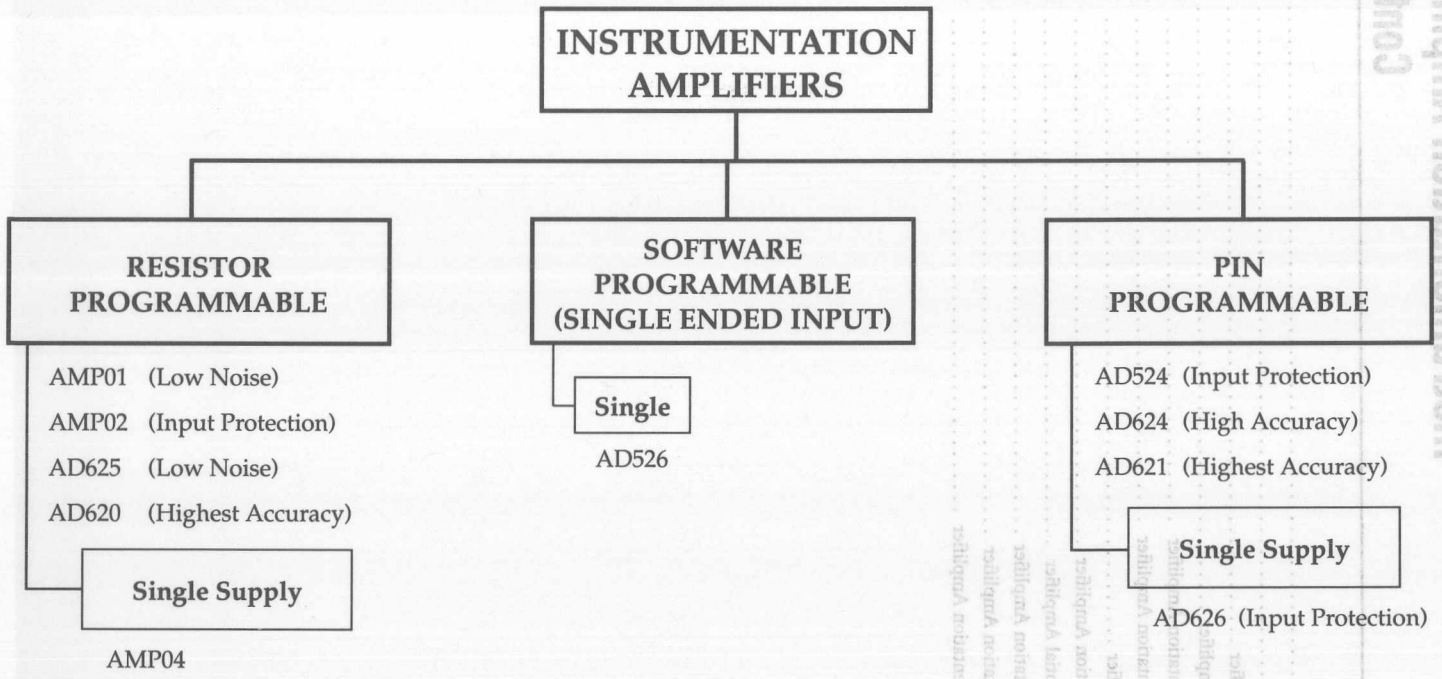


Selection Tree — Instrumentation Amplifiers



Selection Guide—Instrumentation Amplifiers

Category	Model	Gain Range	Gain Error* ± % max (G=1)	Gain TC* ppm/°C max (G=1)	Nonlinearity % max (G=1)	Input Offset Voltage µV max	Input Offset Current nA max	Voltage Noise @ 1 kHz nV/√Hz RTI typ	Slew Rate Volts/µs typ	Power Supply Range ± Volts	Package Options[1]	Temp Ranges[2]	Page[3]
High	**AD524**	**1 to 1,000**	**0.02**	**5**	**0.003**	**50**	**10**	**7**	**5**	**6 to 18**	**D, E**	**I, M/$_D$**	**10–5**
Accuracy	**AD620**	**1 to 10,000**	**0.02**	**−50 (G≤1000)**	**0.004 (G≤1000)**	**50**	**0.5**	**16.4**	**1.2**	**2.3 to 18**	**N, Q, R**	**I, M**	**10–11**
	AD621	**10 to 100**	**0.05 (G=10 or 100)**	**5 (G=10)**	**0.001 (G=10)**	**125**	**0.5**	**17**	**1.2**	**2.3 to 18**	**N, Q, R**	**I, M**	**10–15**
	AMP02	**1 to 10,000**	**0.02**	**50 (G≤1000)**	**0.006 (G≤1000)**	**100**	**5**	**9**	**6**	**4.5 to 18**	**N, Q, R**	**I, M/$_S$**	**10–35**
	AD624	**1 to 1,000**	**0.02**	**5**	**±0.001**	**25**	**±10**	**4**	**5**	**6 to 18**	**D**	**I, M/**	**10–19**
Low	**AD624**	**1 to 1,000**	**0.02**	**5**	**±0.001**	**25**	**±10**	**4**	**5**	**6 to 18**	**D**	**I, M/**	**10–19**
Voltage	**AD625**	**1 to 10,000**	**0.02**	**5 (G≤1000)**	**0.001 (G≤256)**	**25**	**±5**	**4**	**5**	**6 to 18**	**D, N**	**C, I, M/$_D$**	**10–22**
Noise	**AMP01**	**0.1 to 10,000**	**0.6 (G=1–1 k)**	**10 (G≤1000)**	**0.01**	**50**	**1**	**5**	**4.5**	**4.5 to 18**	**E, Q, R**	**C, I, M**	**10–29**
Resistor	**AD620**	**1 to 10,000**	**0.02**	**−50 (G≤1000)**	**0.004 (G≤1000)**	**50**	**0.5**	**16.4**	**1.2**	**2.3 to 18**	**N, Q, R**	**I, M**	**10–11**
Programmable	**AD625**	**1 to 10,000**	**0.02**	**5 (G≤1000)**	**0.001 (G≤256)**	**25**	**±5**	**4**	**5**	**6 to 18**	**D, N**	**C, I, M/$_D$**	**10–22**
Gain	**AMP02**	**1 to 10,000**	**0.02**	**50 (G≤1000)**	**0.006 (G≤1000)**	**100**	**5**	**9**	**6**	**4.5 to 18**	**N, Q, R**	**I, M/$_S$**	**10–35**
	AMP04	**1 to 1,000**	**0.5**	**N/A**	**0.012 (typ)**	**200**	**5**	**N/A**	**0.12**	**2.25 to 18**	**N, R**	**I, M**	**10–39**
Software Prog. Gain	**AD526‡**	**1, 2, 4, 8, 16**	**0.01**	**2**	**0.0035**	**500**	**–**	**30**	**6**	**4.5 to 16.5**	**D, N**	**C, I, M/$_D$**	**10–8**
Single	**AD626¶**	**10 to 100**	**0.6 (G=10 or 100)**	**30 (G=10)**	**0.016 (G=10)**	**2500**	**N/A****	**250**	**0.22**	**+2.4 to +12**	**N, Q, R**	**I, M**	**10–5**
Supply	**AMP04**	**1 to 1,000**	**0.5**	**N/A**	**0.012 (typ)**	**200**	**5**	**N/A**	**0.12**	**+4.5 to +36**	**N, R**	**I, M**	**10–39**
Low	**AD620**	**1 to 10,000**	**0.02**	**−50 (G≤1000)**	**0.04 (G≤1000)**	**50**	**0.5**	**16.4**	**1.2**	**2.3 to18**	**N, Q, R**	**I, M**	**10–11**
Power	**AD621**	**10 to 100**	**0.05 (G=10 or 100)**	**5 (G=10)**	**0.01 (G=10)**	**50**	**0.5**	**17**	**1.2**	**2.3 to 18**	**N, Q, R**	**I, M**	**10–15**
	AMP04	**1 to 1,000**	**0.5**	**N/A**	**0.012 (typ)**	**200**	**5**	**N/A**	**0.12**	**2.25 to18**	**N, R**	**I, M**	**10–39**
	AD626	**10 to 100**	**0.3 (G=10)**	**30 (G=10)**	**0.055 (G=10)**	**250**	**N/A****	**250**	**0.22**	**1.2 to 6**	**N, Q, R**	**I, M**	**10–25**
Input	**AD524**	**1 to 1,000**	**0.02**	**5**	**0.003**	**50**	**±10**	**7**	**5**	**6 to 18**	**D, E**	**I, M/$_D$**	**10–5**
Protected	**AMP02**	**1 to 10,000**	**0.02**	**50 (G≤1000)**	**0.006 (G≤1000)**	**100**	**5**	**9**	**6**	**4.5 to 18**	**N, Q, R**	**I, M/$_S$**	**10–35**
Differential	AMP03	1	0.008	0.015	–	400	–	–	9.5	6 to 18	D, H	I, M	A 4–149
Amp	**AD626**	**10 to 100**	**0.3 (G=10)**	**30 (G=10)**	**0.055 (G=10)**	**250**	**N/A****	**250**	**0.22**	**1.2 to 6**	**N, Q, R**	**I, M**	**10–25**
	SSM2143	**0.5**	**0.1**	**–**	**–**	**1200**	**–**	**–**	**10**	**6 to 18**	**N, R**	**I**	**14–28**
Low Input	**AD620**	**1 to 10,000**	**0.02**	**−50 (G≤1000)**	**0.004 (G≤1000)**	**50**	**0.5**	**16.4**	**1.2**	**2.3 to 18**	**N, Q, R**	**I, M**	**10–11**
Bias	**AD621**	**10 to 100**	**0.05 (G=10 or 100)**	**5 (G=10)**	**0.001 (G=10)**	**50**	**0.5**	**17**	**1.2**	**2.3 to18**	**N, Q, R**	**I, M**	**10–15**
Current	AMP05	0.1 to 2,000	0.5 (G=1–1 k)	20 (G≤1000)	0.001 (typ)	1000	0.025	350	7.5	4.5 to 18	Q	I, M/$_S$	A 4–165

*Does not include effects of external gain resistor (Rg).
‡Digitally programmable.
¶AD626 is specified differently for single and dual supply operation.
**Resistance equals 200 kΩ.
[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]A = *Amplifier Reference Manual*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Selection Guide — Instrumentation Amplifiers

ANALOG DEVICES

Precision Instrumentation Amplifier

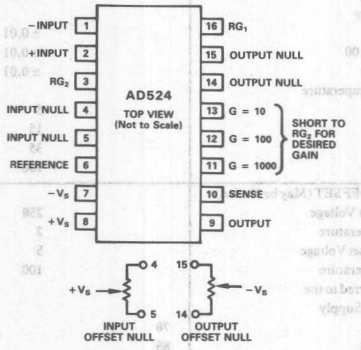
AD524

FEATURES

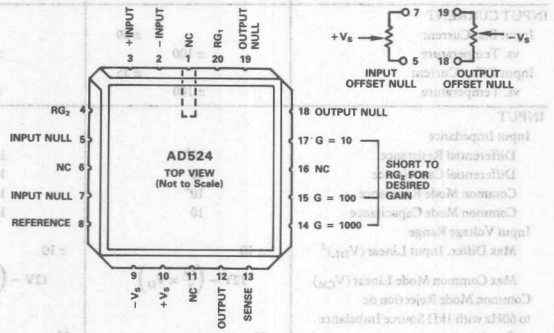
- Low Noise: 0.3μV p-p 0.1Hz to 10Hz
- Low Nonlinearity: 0.003% (G = 1)
- High CMRR: 120dB (G = 1000)
- Low Offset Voltage: 50μV
- Low Offset Voltage Drift: 0.5μV/°C
- Gain Bandwidth Product: 25MHz
- Pin Programmable Gains of 1, 10, 100, 1000
- Input Protection, Power On – Power Off
- No External Components Required
- Internally Compensated
- MIL-STD-883B and Chips Available
- 16-Pin Ceramic DIP and SOIC Packages and 20-Terminal Leadless Chip Carriers Available
- Available in Tape and Reel in Accordance with EIA-481A Standard
- Standard Military Drawing Also Available

CONNECTION DIAGRAMS

Ceramic (D) and SOIC (R) Packages



Leadless Chip Carrier (E) Package



PRODUCT DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low offset voltage drift, and low noise makes the AD524 suitable for use in many data acquisition systems.

The AD524 has an output offset voltage drift of less than 25μV/°C, input offset voltage drift of less than 0.5μV/°C, CMR above 90dB at unity gain (120dB at G = 1000) and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications the AD524 also has a 25MHz gain bandwidth product (G = 100). To make it suitable for high speed data acquisition systems the AD524 has an output slew rate of 5V/μs and settles in 15μs to 0.01% for gains of 1 to 100.

As a complete amplifier the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1,000. For other gain settings between 1 and 1000 only a single resistor is required. The AD524 input is fully protected for both power on and power off fault conditions.

The AD524 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "A" grade, the low drift "B" grade and lower drift, higher linearity "C" grade are specified from −25°C to +85°C. The "S" grade guarantees performance to specification over the extended temperature range −55°C to +125°C. Devices are available in 16-pin ceramic DIP and SOIC packages and a 20-terminal leadless chip carrier.

PRODUCT HIGHLIGHTS

1. The AD524 has guaranteed low offset voltage, offset voltage drift and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100 and 1000, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD524 is input protected for both power on and power off fault conditions.
5. The AD524 offers superior dynamic performance with a gain bandwidth product of 25MHz, full power response of 75kHz and a settling time of 15μs to 0.01% of a 20V step (G = 100).

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD524 SPECIFICATIONS

(External Resistor Gain Programming)	$\left[\frac{40,000}{R_G}+1\right]\pm 20\%$	$\left[\frac{40,000}{R_G}+1\right]\pm 20\%$	$\left[\frac{40,000}{R_G}+1\right]\pm 20\%$	$\left[\frac{40,000}{R_G}+1\right]\pm 20\%$	
Gain Range (Pin Programmable)	1 to 1000	1 to 1000	1 to 1000	1 to 1000	
Gain Error[1]					
G = 1	±0.05	±0.03	±0.02	±0.05	%
G = 10	±0.25	±0.15	±0.1%	±0.25	%
G = 100	±0.5	±0.35	±0.25	±0.5	%
G = 1000	±2.0	±1.0	±0.5	±2.0	%
Nonlinearity					
G = 1	±0.01	±0.005	±0.003	±0.01	%
G = 10, 100	±0.01	±0.005	±0.003	±0.01	%
G = 1000	±0.01	±0.01	±0.01	±0.01	%
Gain vs. Temperature					
G = 1	5	5	5	5	ppm/°C
G = 10	15	10	10	10	ppm/°C
G = 100	35	25	25	25	ppm/°C
G = 1000	100	50	50	50	ppm/°C
VOLTAGE OFFSET (May be Nulled)					
Input Offset Voltage	250	100	50	100	µV
vs. Temperature	2	0.75	0.5	2.0	µV/°C
Output Offset Voltage	5	3	2.0	3.0	mV
vs. Temperature	100	50	25	50	µV/°C
Offset Referred to the Input vs. Supply					
G = 1	70	75	80	75	dB
G = 10	85	95	100	95	dB
G = 100	95	105	110	105	dB
G = 1000	100	110	115	110	dB
INPUT CURRENT					
Input Bias Current	±50	±25	±15	±50	nA
vs. Temperature	±100	±100	±100	±100	pA/°C
Input Offset Current	±35	±15	±10	±35	nA
vs. Temperature	±100	±100	±100	±100	pA/°C
INPUT					
Input Impedance					
Differential Resistance	10^9	10^9	10^9	10^9	Ω
Differential Capacitance	10	10	10	10	pF
Common Mode Resistance	10^9	10^9	10^9	10^9	Ω
Common Mode Capacitance	10	10	10	10	pF
Input Voltage Range					
Max Differ. Input Linear (V_{DL})[2]	±10	±10	±10	±10	V
Max Common Mode Linear (V_{CM})	$12V-\left(\frac{G}{2}\times V_D\right)$	$12V-\left(\frac{G}{2}\times V_D\right)$	$12V-\left(\frac{G}{2}\times V_D\right)$	$12V-\left(\frac{G}{2}\times V_D\right)$	V
Common Mode Rejection dc to 60Hz with 1kΩ Source Imbalance					
G = 1	70	75	80	70	dB
G = 10	90	95	100	90	dB
G = 100	100	105	110	100	dB
G = 1000	110	115	120	110	dB
OUTPUT RATING					
V_{OUT}, R_L = 2kΩ	±10	±10	±10	±10	V
DYNAMIC RESPONSE					
Small Signal –3dB					
G = 1	1	1	1	1	MHz
G = 10	400	400	400	400	kHz
G = 100	150	150	150	150	kHz
G = 1000	25	25	25	25	kHz
Slew Rate	5.0	5.0	5.0	5.0	V/µs
Settling Time to 0.01%, 20V Step					
G = 1 to 100	15	15	15	15	µs
G = 1000	75	75	75	75	µs
NOISE					
Voltage Noise, 1kHz					
R.T.I.	7	7	7	7	nV/√Hz
R.T.O.	90	90	90	90	nV/√Hz
R.T.I., 0.1 to 10Hz					
G = 1	15	15	15	15	µV p-p
G = 10	2	2	2	2	µV p-p
G = 100, 1000	0.3	0.3	0.3	0.3	µV p-p
Current Noise					
0.1Hz to 10Hz	60	60	60	60	pA p-p

Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Units
SENSE INPUT													
R_{IN}		20			20			20			20		kΩ ±20%
I_{IN}		15			15			15			15		μA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}		40			40			40			40		kΩ ±20%
I_{IN}		15			15			15			15		μA
Voltage Range	±10			±10			10			10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	−25		+85	−25		+85	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY													
Power Supply Range	±6	±15	±18	±6	±15	±18	±6	±15	±18	±6	±15	±18	V
Quiescent Current		3.5	5.0		3.5	5.0		3.5	5.0		3.5	5.0	mA

NOTES
[1]Does not include effects of external resistor R_G.
[2]V_{OL} is the maximum differential input voltage at G = 1 for specified nonlinearity.
V_{DL} at other gains = 10V/G.
V_D = Actual differential input voltage.
Example: G = 10, V_D = 0.50
V_{CM} = 12V − (10/2 × 0.50V) = 9.5V
Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

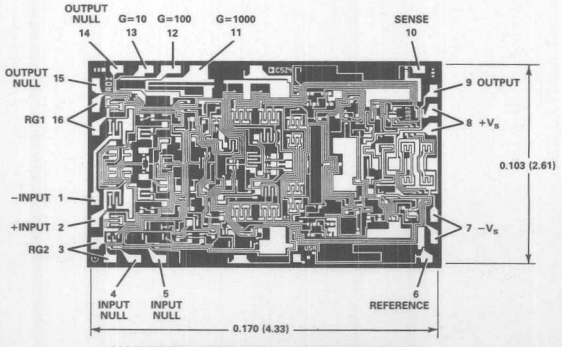
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation 450mW
Input Voltage,[2]
(Either Input Simultaneously) $|V_{IN}| + |V_S|$ . . . . . <36V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
(R) . . . . . −65°C to +125°C
(D, E) . . . . . −65°C to +150°C
Operating Temperature Range
AD524A/B/C . . . . . −25°C to +85°C
AD524S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Max input voltage specification refers to maximum voltage to which either input terminal may be raised with or without device power applied. For example, with ±18 volt supplies max V_{IN} is ±18 volts, with zero supply voltage max V_{IN} is ±36 volts.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



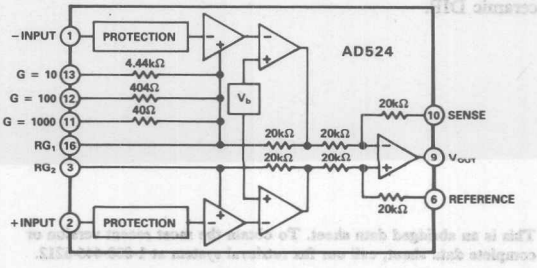
PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE D-16 AND R-16 16-PIN CERAMIC PACKAGES.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD524AD	−40°C to +85°C	16-Pin Ceramic DIP	D-16
AD524AE	−40°C to +85°C	20-Pin Leadless Chip Carrier	E-20A
AD524AR	−40°C to +85°C	16-Pin Gull-Wing SOIC	R-16
AD524AR-REEL	−40°C to +85°C	Tape & Reel Packaging	
AD524BD	−40°C to +85°C	16-Pin Ceramic DIP	D-16
AD524BE	−40°C to +85°C	20-Pin Leadless Chip Carrier	E-20A
AD524CD	−40°C to +85°C	16-Pin Ceramic DIP	D-16
AD524SD	−55°C to +125°C	16-Pin Ceramic DIP	D-16
AD524SD/883B	−55°C to +125°C	16-Pin Ceramic DIP	D-16
AD524SE/883B	−55°C to +125°C	20-Pin Leadless Chip Carrier	E-20A
AD524AChips	−40°C to +85°C	Die	
AD524SChips	−55°C to +125°C	Die	

*For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM



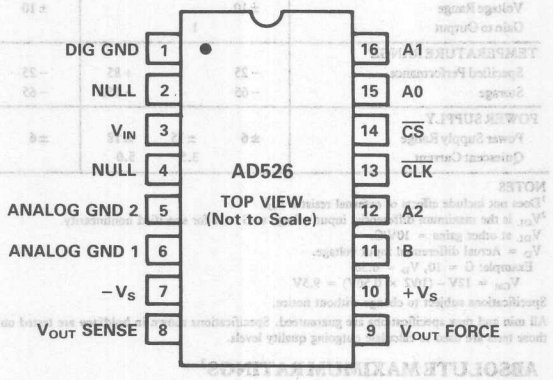
Software Programmable Gain Amplifier

AD526

FEATURES

- Digitally Programmable Binary Gains from 1 to 16
- Two-Chip Cascade Mode Achieves Binary Gain from 1 to 256
- Gain Error:
  - 0.01% max, Gain = 1, 2, 4 (C Grade)
  - 0.02% max, Gain = 8, 16 (C Grade)
  - 0.5ppm/°C Drift Over Temperature
- Fast Settling Time
  - 10V Signal Change:
    - 0.01% in 4.5µs (Gain = 16)
  - Gain Change:
    - 0.01% in 5.6µs (Gain = 16)
- Low Nonlinearity: ±0.005% FSR max (J Grade)
- Excellent DC Accuracy:
  - Offset Voltage: 0.5mV max (C Grade)
  - Offset Voltage Drift: 3µV/°C (C Grade)
- TTL Compatible Digital Inputs
- Standard Military Drawing Available

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD526 is a single-ended, monolithic software programmable gain amplifier (SPGA) that provides gains of 1, 2, 4, 8 and 16. It is complete, including amplifier, resistor network and TTL-compatible latched inputs, and requires no external components.

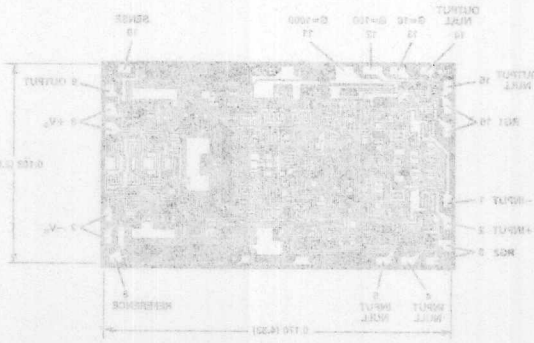
Low gain error and low nonlinearity make the AD526 ideal for precision instrumentation applications requiring programmable gain. The small signal bandwidth is 350kHz at a gain of 16. In addition, the AD526 provides excellent dc precision. The FET-input stage results in a low bias current of 50pA. A guaranteed maximum input offset voltage of 0.5mV max (C grade) and low gain error (0.01%, G = 1, 2, 4, C grade) are accomplished using Analog Devices' laser trimming technology.

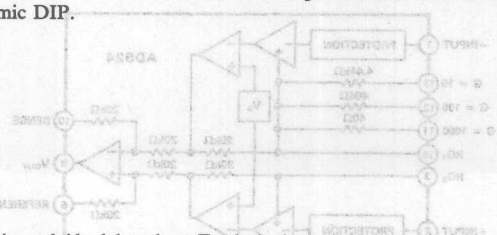
To provide flexibility to the system designer, the AD526 can be operated in either latched or transparent mode. The force/sense configuration preserves accuracy when the output is connected to remote or low impedance loads.

The AD526 is offered in one commercial (0 to +70°C) grade, J, and three industrial grades, A, B and C, which are specified from −40°C to +85°C. The S grade is specified from −55°C to +125°C. The military version is available processed to MIL-STD 883B, Rev C. The J grade is supplied in a 16-pin plastic DIP, and the other grades are offered in a 16-pin hermetic side-brazed ceramic DIP.

APPLICATION HIGHLIGHTS

1. **Dynamic Range Extension for ADC Systems:** A single AD526 in conjunction with a 12-bit ADC can provide 96dB of dynamic range for ADC systems.
2. **Gain Ranging Pre-Amps:** The AD526 offers complete digital gain control with precise gains in binary steps from 1 to 16. Additional gains of 32, 64, 128 and 256 are possible by cascading two AD526s.





This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise otherwise specified)

	AD526J			AD526A			AD526B/S			AD526C			
Model	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
GAIN													
Gain Range													
(Digitally Programmable)		1, 2, 4, 8, 16			1, 2, 4, 8, 16			1, 2, 4, 8, 16			1, 2, 4, 8, 16		
Gain Error													
G = 1			**0.05**			**0.02**			**0.01**			**0.01**	%
G = 2			**0.05**			**0.03**			**0.02**			**0.01**	%
G = 4			**0.10**			**0.03**			**0.02**			**0.01**	%
G = 8			**0.15**			**0.07**			**0.04**			**0.02**	%
G = 16			**0.15**			**0.07**			**0.04**			**0.02**	%
Gain Error Drift													
Over Temperature													
G = 1		0.5	2.0		0.5	2.0		0.5	2.0		0.5	2.0	ppm/°C
G = 2		0.5	2.0		0.5	2.0		0.5	2.0		0.5	2.0	ppm/°C
G = 4		0.5	3.0		0.5	3.0		0.5	3.0		0.5	3.0	ppm/°C
G = 8		0.5	5.0		0.5	5.0		0.5	5.0		0.5	5.0	ppm/°C
G = 16		1.0	5.0		1.0	5.0		1.0	5.0		1.0	5.0	ppm/°C
Gain Error (T_{min} to T_{max})													
G = 1			0.06			**0.03**			**0.02**			**0.015**	%
G = 2			0.06			**0.04**			**0.03**			**0.015**	%
G = 4			0.12			**0.04**			**0.03**			**0.015**	%
G = 8			0.17			**0.08**			**0.05**			**0.03**	%
G = 16			0.17			**0.08**			**0.05**			**0.03**	%
Nonlinearity													
G = 1			**0.005**			**0.005**			**0.005**			**0.0035**	% FSR
G = 2			0.001			0.001			0.001			0.001	% FSR
G = 4			0.001			0.001			0.001			0.001	% FSR
G = 8			0.001			0.001			0.001			0.001	% FSR
G = 16			0.001			0.001			0.001			0.001	% FSR
Nonlinearity (T_{min} to T_{max})													
G = 1			0.01			**0.01**			**0.01**			**0.007**	% FSR
G = 2			0.001			0.001			0.001			0.001	% FSR
G = 4			0.001			0.001			0.001			0.001	% FSR
G = 8			0.001			0.001			0.001			0.001	% FSR
G = 16			0.001			0.001			0.001			0.001	% FSR
VOLTAGE OFFSET, ALL GAINS													
Input Offset Voltage		0.4	**1.5**		0.25	**0.7**		0.25	**0.5**		0.25	**0.5**	mV
Input Offset Voltage Drift Over Temperature		5	20		3	10		3	10		3	10	µV/°C
Input Offset Voltage T_{min} to T_{max}			2.0			**1.0**			**0.8**			**0.8**	mV
Input Offset Voltage vs. Supply (V_S ± 10%)	80			80			84			90			dB
INPUT BIAS CURRENT													
Over Input Voltage Range ± 10V		50	**150**		50	**150**		50	**150**		50	**150**	pA
ANALOG INPUT CHARACTERISTICS													
Voltage Range													
(Linear Operation)	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Capacitance		5			5			5			5		pF
RATED OUTPUT													
Voltage	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Current (V_{OUT} = ± 10V)	**±5**	±10		**±5**	±10		**±5**	±10		**±5**	±10		mA
Short-Circuit Current	**15**	30		**15**	30		**15**	30		**15**	30		mA
DC Output Resistance		0.002			0.002			0.002			0.002		Ω
Load Capacitance (For Stable Operation)		700			700			700			700		pF
NOISE, ALL GAINS													
Voltage Noise, RTI													
0.1Hz to 10Hz		3			3			3			3		µV p-p
Voltage Noise Density, RTI													
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		60			60			60			60		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz

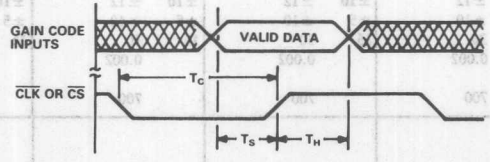
10

DYNAMIC RESPONSE																
– 3dB Bandwidth (Small Signal)																
G = 1		4.0			4.0			4.0			4.0					MHz
G = 2		2.0			2.0			2.0			2.0					MHz
G = 4		1.5			1.5			1.5			1.5					MHz
G = 8		0.65			0.65			0.65			0.65					MHz
G = 16		0.35			0.35			0.35			0.35					MHz
Signal Settling Time to 0.01%																
(ΔV_{OUT} = ± 10V)																
G = 1		2.1	4		2.1	4		2.1	4		2.1	4				µs
G = 2		2.5	5		2.5	5		2.5	5		2.5	5				µs
G = 4		2.7	5		2.7	5		2.7	5		2.7	5				µs
G = 8		3.6	7		3.6	7		3.6	7		3.6	7				µs
G = 16		4.1	7		4.1	7		4.1	7		4.1	7				µs
Full Power Bandwidth																
G = 1, 2, 4		0.10			0.10			0.10			0.10					MHz
G = 8, 16		0.35			0.35			0.35			0.35					MHz
Slew Rate																
G = 1, 2, 4	**4**	6		**4**	6		**4**	6		**4**	6					V/µs
G = 8, 16	**18**	24		**18**	24		**18**	24		**18**	24					V/µs
DIGITAL INPUTS																
(T_{min} to T_{max})																
Input Current (V_H = 5V)	60	100	140	60	100	140	60	100	140	60	100	140				µA
Logic "1"	2		6	2		6	2		6	2		6				V
Logic "0"	0		0.8	0		0.8	0		0.8	0		0.8				V
TIMING[1]																
(V_L = 0.2V, V_H = 3.7V)																
A0, A1, A2																
T_C	50			50			50			50						ns
T_S	30			30			30			30						ns
T_H	30			30			30			30						ns
B																
T_C	50			50			50			50						ns
T_S	40			40			40			40						ns
T_H	10			10			10			10						ns
TEMPERATURE RANGE																
Specified Performance	0		+70	–40		+85	–40/–55		+85/+125	–40		+85				°C
Storage	–65		+125	–65		+150	–65		+150	–65		+150				°C
POWER SUPPLY																
Operating Range	±4.5		±16.5	±4.5		±16.5	±4.5		±16.5	±4.5		±16.5				V
Positive Supply Current		10	14		10	14		10	14		10	14				mA
Negative Supply Current		10	13		10	13		10	13		10	13				mA
PACKAGE OPTIONS[2]																
Plastic (N-16)		AD526JN														
Ceramic DIP (D-16)					AD526AD			AD526BD AD526SD AD526SD/883B			AD526CD					

NOTES
[1]Refer to Figure 35 for definitions.
FSR = Full-Scale Range = 20V.
RTI = Referred to Input.
[2]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



T_C = MINIMUM CLOCK CYCLE
T_S = DATA SETUP TIME
T_H = DATA HOLD TIME

NOTE: THRESHOLD LEVEL FOR GAIN CODE, CS, AND CLK IS 1.4V.

Figure 35. AD526 Timing

Low Cost, Low Power Instrumentation Amplifier

AD620

FEATURES

EASY TO USE
- Gain Set with One External Resistor (Gain Range 1 to 1000)
- Wide Power Supply Range (±2.3 V to ±18 V)
- Higher Performance than Three Op Amp IA Designs
- Available in 8-Pin DIP and SOIC Packaging
- Low Power, 1.3 mA max Supply Current

EXCELLENT DC PERFORMANCE ("A GRADE")
- 125 μV max, Input Offset Voltage (50 μV max "B" Grade)
- 1 μV/°C max, Input Offset Drift
- 2.0 nA max, Input Bias Current
- 93 dB min Common-Mode Rejection Ratio (G = 10)

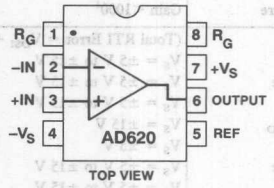
LOW NOISE
- 9 nV/√Hz, @ 1 kHz, Input Voltage Noise
- 0.28 μV p-p Noise (0.1 Hz to 10 Hz)

EXCELLENT AC SPECIFICATIONS
- 120 kHz Bandwidth (G = 100)
- 15 μs Settling Time to 0.01%

APPLICATIONS
- Weigh Scales
- ECG and Medical Instrumentation
- Transducer Interface
- Data Acquisition Systems
- Industrial Process Controls
- Battery Powered and Portable Equipment

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages

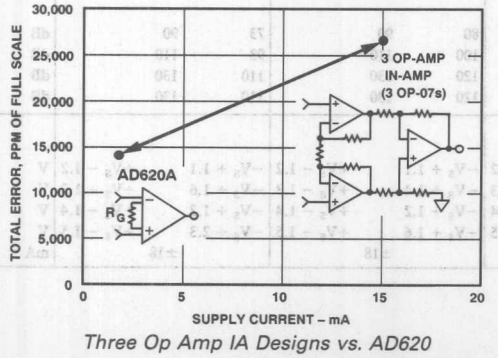


PRODUCT DESCRIPTION

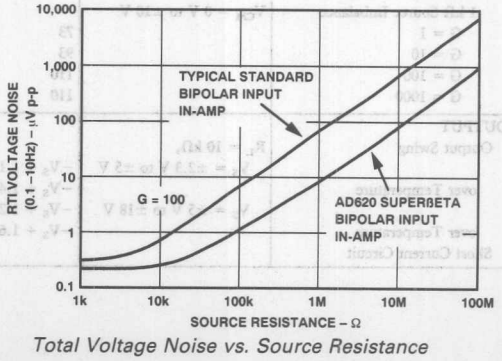
The AD620 is a low cost, high accuracy instrumentation amplifier which requires only one external resistor to set gains of 1 to 1000. Furthermore, the AD620 features 8-pin SOIC and DIP packaging that is smaller than discrete designs, and offers lower power (only 1.3 mA max supply current), making it a good fit for battery powered, portable (or remote) applications.

The AD620, with its high accuracy of 40 ppm maximum nonlinearity, low offset voltage of 50 μV max and offset drift of 0.6 μV/°C max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the AD620 make it well suited for medical applications such as ECG and noninvasive blood pressure monitors.

The low input bias current of 1.0 nA max is made possible with the use of Superβeta processing in the input stage. The AD620 works well as a preamplifier due to its low input voltage noise of 9 nV/√Hz at 1 kHz, 0.28 μV p-p in the 0.1 Hz to 10 Hz band, 0.1 pA/√Hz input current noise. Also, the AD620 is well suited for multiplexed applications with its settling time of 15 μs to 0.01% and its cost is low enough to enable designs with one in amp per channel.



Three Op Amp IA Designs vs. AD620



Total Voltage Noise vs. Source Resistance

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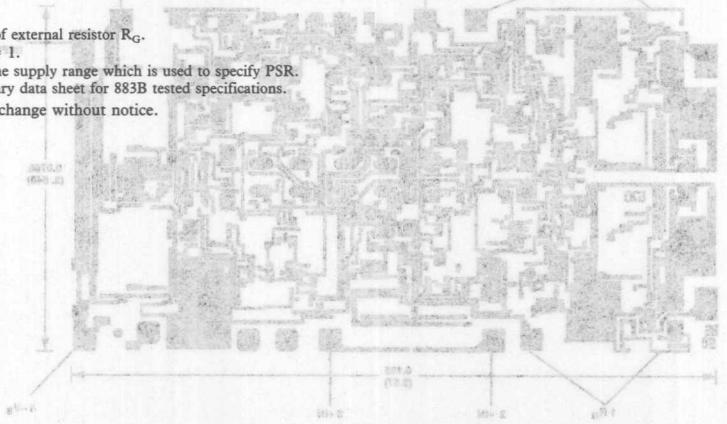
REV. D

AD620—SPECIFICATIONS (typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ unless otherwise noted)

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[4] Min	AD620S[4] Typ	AD620S[4] Max	Units
GAIN	G = 1 + (49.4 k/R_G)										
Gain Range		1		10,000	1		10,000	1		10,000	
Gain Error[1]	V_{OUT} = ±10 V										
G = 1			0.03	0.10		0.01	0.02		0.03	0.10	%
G = 10			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 100			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 1000			0.40	0.70		0.35	0.50		0.40	0.70	%
Nonlinearity,	V_{OUT} = −10 V to +10 V,										
G = 1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
G = 1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
Gain vs. Temperature	Gain <1000[1]			−50			−50			−50	ppm/°C
VOLTAGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V		30	125		15	50		30	125	µV
over Temperature	V_S = ±5 V to ±15 V			185			85			225	µV
Average TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Output Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	µV
	V_S = ±5 V			1500			750			1500	µV
over Temperature	V_S = ±5 V to ±15 V			2000			1000			2000	µV
Average TC	V_S = ±5 V to ±15 V		5.0	15		2.5	7.0		5.0	15	µV/°C
Offset Referred to the Input vs. Supply (PSR)	V_S = ±2.3 V to ±18 V										
G = 1		80	100		80	100		80	100		dB
G = 10		95	120		100	120		95	120		dB
G = 100		110	140		120	140		110	140		dB
G = 1000		110	140		120	140		110	140		dB
INPUT CURRENT											
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2.0	nA
over Temperature				2.5			1.5			4.0	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10||2			10||2			10||2		GΩ||pF
Common-Mode			10||2			10||2			10||2		GΩ||pF
Input Voltage Range[2]	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	V
over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	V
over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.3		$+V_S$ − 1.4	V
Common-Mode Rejection Ratio DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = 0 V to ±10 V										
G = 1		73	90		80	90		73	90		dB
G = 10		93	110		100	110		93	110		dB
G = 100		110	130		120	130		110	130		dB
G = 1000		110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	V
over Temperature		$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.6		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	V
over Temperature		$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 2.3		$+V_S$ − 1.5	V
Short Current Circuit			±18			±18			±18		mA

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[4] Min	AD620S[4] Typ	AD620S[4] Max	Units
DYNAMIC RESPONSE											
Small Signal −3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/μs
Settling Time to 0.01%	10 V Step										
G = 1–100			15			15			15		μs
G = 1000			150			150			150		μs
NOISE											
Voltage Noise, 1 kHz	Total RTI Noise = $\sqrt{(e^2_{ni}) + (e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/$\sqrt{\text{Hz}}$
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/$\sqrt{\text{Hz}}$
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	μV p-p
G = 10			0.55			0.55	0.8		0.55	0.8	μV p-p
G = 100–1000			0.28			0.28	0.4		0.28	0.4	μV p-p
Current Noise	f = 1 kHz		100			100			100		fA/$\sqrt{\text{Hz}}$
0.1 Hz to 10 Hz			10			10			10		pA p-p
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		+50	+60		+50	+60		+50	+60	μA
Voltage Range		$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range[3]		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
for Specified Performance			−40 to +85			−40 to +85			−55 to +125		°C

NOTES
[1]Does not include effects of external resistor R_G.
[2]One input grounded. G = 1.
[3]This is defined as the same supply range which is used to specify PSR.
[4]See Analog Devices military data sheet for 883B tested specifications.
Specifications subject to change without notice.



10

Internal Power Dissipation[2]	650 mW
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	±25 V
Output Short Circuit Duration	Indefinite
Storage Temperature Range (Q)	−65°C to +150°C
Storage Temperature Range (N, R)	−65°C to +125°C
Operating Temperature Range	
AD620 (A, B)	−40°C to +85°C
AD620 (S)	−55°C to +125°C
Lead Temperature Range	
(Soldering 10 seconds)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Pin Plastic Package: θ_{JA} = 95°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt

Model	Temperature Range	Package Option
AD620AN	−40°C to +85°C	N-8
AD620BN	−40°C to +85°C	N-8
AD620AR	−40°C to +85°C	R-8
AD620BR	−40°C to +85°C	R-8
AD620AChips	−40°C to +85°C	Die Form
AD620SQ/883B	−55°C to +125°C	Q-8

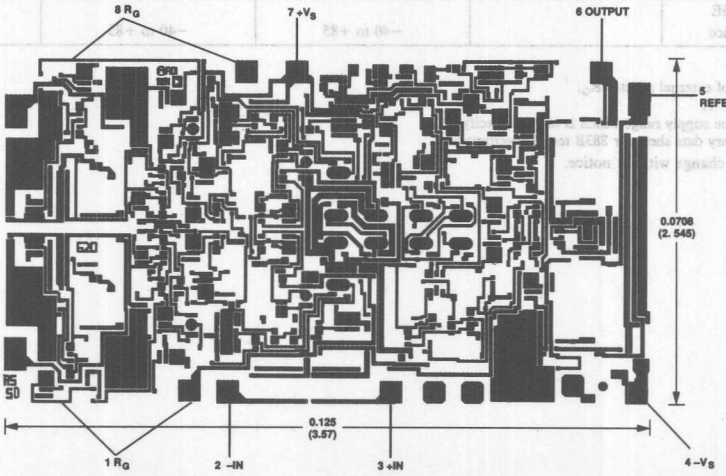
*N = Plastic DIP; Q = Cerdip; R = SOIC.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD620 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



Low Drift, Low Power Instrumentation Amplifier

AD621

FEATURES

EASY TO USE
- Pin-Strappable Gains of 10 & 100
- All Errors Specified for Total System Performance
- Higher Performance than Discrete In-Amp Designs
- Available in 8-Pin DIP and SOIC
- Low Power, 1.3 mA max Supply Current
- Wide Power Supply Range (±2.3 V to ±18 V)

EXCELLENT DC PERFORMANCE
- 0.15% max, Total Gain Error
- ±5 ppm/°C, Total Gain Drift
- 125 μV max, Total Offset Voltage
- 1.0 μV/°C max, Offset Voltage Drift

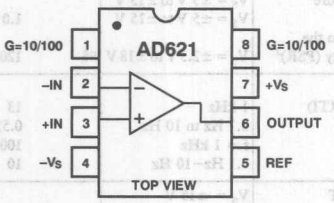
LOW NOISE
- 9 nV/√Hz, @ 1 kHz, Input Voltage Noise
- 0.28 μV p–p Noise (0.1 Hz to 10 Hz)

EXCELLENT AC SPECIFICATIONS
- 800 kHz Bandwidth (G = 10), 200 kHz (G = 100)
- 12 μs Settling Time to 0.01%

APPLICATIONS
- Weigh Scales
- Transducer Interface & Data Acquisition Systems
- Industrial Process Controls
- Battery Powered and Portable Equipment

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages

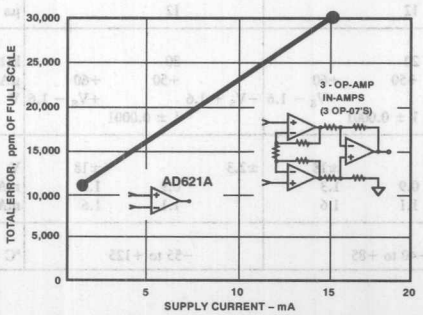


PRODUCT DESCRIPTION

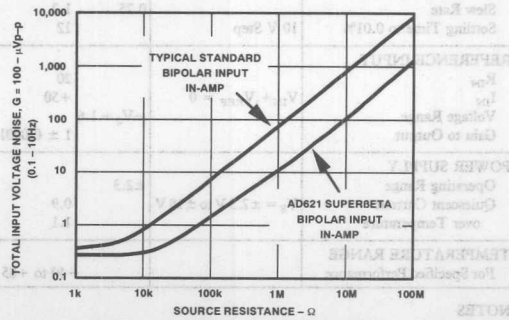
The AD621 is an easy to use, low cost, low power, high accuracy instrumentation amplifier which is ideally suited for a wide range of applications. Its unique combination of high performance, small size and low power, outperforms discrete in amp implementations. High functionality, low gain errors and low gain drift errors are achieved by the use of internal gain setting resistors. Fixed gains of 10 and 100 can be easily set via external pin strapping. The AD621 is fully specified as a total system, therefore, simplifying the design process.

For portable or remote applications, where power dissipation, size and weight are critical, the AD621 features a very low supply current of 1.3 mA max and is packaged in a compact 8-pin SOIC, 8-pin plastic DIP or 8-pin cerdip. The AD621 also excels in applications requiring high total accuracy, such as precision data acquisition systems used in weigh scales and transducer interface circuits. Low maximum error specifications including nonlinearity of 10 ppm, gain drift of 5 ppm/°C, 50 μV offset voltage and 0.6 μV/°C offset drift ("B" grade), make possible total system performance at a lower cost than has been previously achieved with discrete designs or with other monolithic instrumentation amplifiers.

When operating from high source impedances, as in ECG and blood pressure monitors, the AD621 features the ideal combination of low noise and low input bias currents. Voltage noise is specified as 9 nV√Hz at 1 kHz and 0.28 μV p–p from 0.1 Hz to 10 Hz. Input current noise is also extremely low at 0.1 pA/√Hz. The AD621 outperforms FET input devices with an input bias current specification of 1.5 nA max over the full industrial temperature range.



Three Op Amp IA Designs vs. AD621



Total Voltage Noise vs. Source Resistance

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD621—SPECIFICATIONS

Gain = 10 (typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ unless otherwise noted)

Parameter	Conditions	AD621A Min	AD621A Typ	AD621A Max	AD621B Min	AD621B Typ	AD621B Max	AD621S[1] Min	AD621S[1] Typ	AD621S[1] Max	Units
GAIN											
Gain Error	V_{OUT} = ±10 V			0.15			0.05			0.15	%
Nonlinearity											
V_{OUT} = −10 V to +10 V	R_L = 2 kΩ		2	10		2	10		2	10	ppm of FS
Gain vs. Temperature			−1.5	±5		−1.5	±5		−1	±5	ppm/°C
TOTAL VOLTAGE OFFSET											
Offset (RTI)	V_S = ±15 V		75	250		50	125		75	250	µV
over Temperature	V_S = ±5 V to ±15 V			400			215			500	µV
Average TC	V_S = ±5 V to ±15 V		1.0	2.5		0.6	1.5		1.0	2.5	µV/°C
Offset Referred to the Input vs. Supply (PSR)[2]	V_S = ±2.3 V to ±18 V	95	120		100	120		95	120		dB
TOTAL NOISE											
Voltage Noise, (RTI)	1 kHz		13	17		13	17		13	17	nV/√Hz
RTI	0.1 Hz to 10 Hz		0.55			0.55	0.8		0.55	0.8	µV p–p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
	0.1 Hz–10 Hz		10			10			10		pA p–p
INPUT CURRENT	V_S = ±15 V										
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10||2			10||2			10||2		GΩ|pF
Common-Mode			10||2			10||2			10||2		GΩ|pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	V
over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	V
over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.3		$+V_S$ − 1.4	V
Common-Mode Rejection Ratio DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = 0 V to ±10 V	93	110		100	110		93	110		dB
OUTPUT											
Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	V
over Temperature		$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.6		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	V
over Temperature		$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 2.3		$+V_S$ − 1.5	V
Short Current Circuit			±18			±18			±18		mA
DYNAMIC RESPONSE											
Small Signal, −3 dB Bandwidth			800			800			800		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step		12			12			12		µs
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN}+, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$-V_S$ + 1.6		$+V_S$ − 1.6	$-V_S$ + 1.6		$+V_S$ − 1.6	$-V_S$ + 1.6		$+V_S$ − 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance			−40 to +85			−40 to +85			−55 to +125		°C

NOTES

[1]See Analog Devices military data sheet for 883B tested specifications.

[2]This is defined as the supply range over which PSRR is defined.

[3]Input Voltage Range = CMV + (Gain × V_{DIFF}).

Specifications subject to change without notice.

Gain = 100 (typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ unless otherwise noted)

Parameter	Conditions	AD621A Min	AD621A Typ	AD621A Max	AD621B Min	AD621B Typ	AD621B Max	AD621S[1] Min	AD621S[1] Typ	AD621S[1] Max	Units
GAIN											
Gain Error	V_{OUT} = ±10 V			0.15			0.05			0.15	%
Nonlinearity											
V_{OUT} = −10 V to +10 V	R_L = 2 kΩ		2	10		2	10		2	10	ppm of FS
Gain vs. Temperature			−1	±5		−1	±5		−1	±5	ppm/°C
TOTAL VOLTAGE OFFSET											
Offset (RTI)	V_S = ±5 V ±15 V		35	125		25	50		35	125	µV
over Temperature	V_S = ±5 V to ±15 V			185			215			225	µV
Average TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Offset Referred to the Input vs. Supply (PSR)[2]	V_S = ±2.3 V to ±18 V	110	140		120	140		110	140		dB
TOTAL NOISE											
Voltage Noise, (RTI)	1 kHz		9	13		9	13		9	13	nV/√Hz
RTI	0.1 Hz to 10 Hz		0.28			0.28	0.4		0.28	0.4	µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
	0.1 Hz−10 Hz		10			10			10		pA p-p
INPUT CURRENT	V_S = ±15 V										
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10||2			10||2			10||2		GΩ||pF
Common-Mode			10||2			10||2			10||2		GΩ||pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	V
over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	V
over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.3		$+V_S$ − 1.4	V
Common-Mode Rejection Ratio DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = 0 V to ±10 V	110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	V
over Temperature		$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.6		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	V
over Temperature		$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 2.3		$+V_S$ − 1.5	V
Short Current Circuit			±18			±18			±18		mA
DYNAMIC RESPONSE											
Small Signal, −3 dB Bandwidth			200			200			200		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step		12			12			12		µs
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN}+, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$-V_S$ + 1.6		$+V_S$ − 1.6	$-V_S$ + 1.6		$+V_S$ − 1.6	$-V_S$ + 1.6		$+V_S$ − 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance			−40 to +85			−40 to +85			−55 to +125		°C

NOTES
[1]See Analog Devices military data sheet for 883B tested specifications.
[2]This is defined as the supply range over which PSRR is defined.
[3]Input Voltage Range = CMV + (Gain × V_{DIFF}).
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 650 mW
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±25 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD621A, B . . . . . −40°C to +85°C
AD621S[3] . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering 10 seconds) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin Plastic DIP Package: θ_{JA} = 95°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt
[3]See Analog Devices' military data sheet for 883B specifications.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD621 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

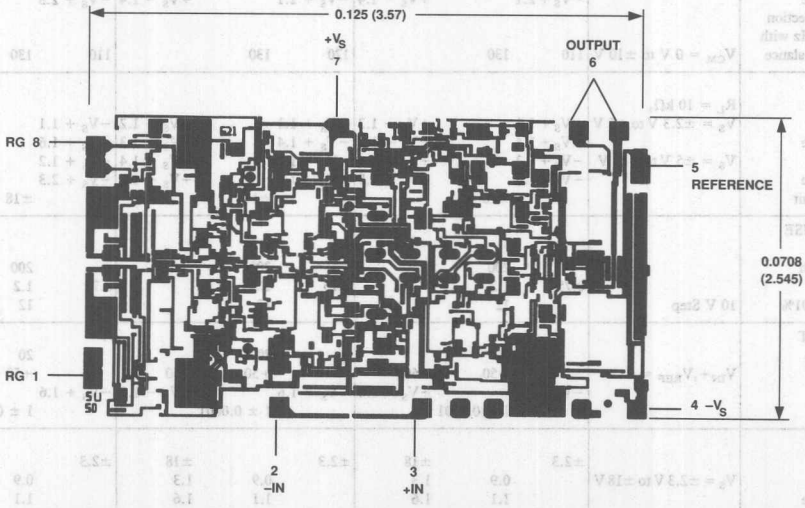
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD621AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD621BN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD621AR	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD621BR	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD621SQ/883B[2]	−55°C to +125°C	8-Pin Cerdip	Q-8
AD621ACHIPS	−40°C to +85°C	Die	

NOTES
[1]For outline information see Package Information section.
[2]See Analog Devices' military data sheet for 883B specifications.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm)
Contact factory for latest dimensions



ANALOG DEVICES

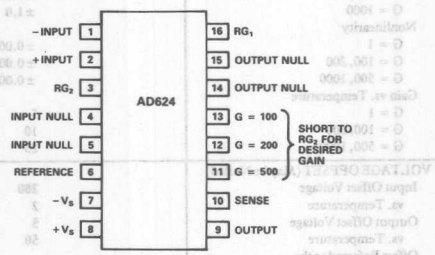
Precision Instrumentation Amplifier

AD624

FEATURES

Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Gain TC: 5ppm max (G = 1)
Low Nonlinearity: 0.001% max (G = 1 to 200)
High CMRR: 130dB min (G = 500 to 1000)
Low Input Offset Voltage: 25μV, max
Low Input Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 100, 200, 500, 1000
No External Components Required
Internally Compensated

CONNECTION DIAGRAM



FOR GAIN OF 1000 SHORT RG_1 TO PIN 12 AND PINS 11 AND 13 TO RG_2

PRODUCT DESCRIPTION

The AD624 is a high precision, low noise, instrumentation amplifier designed primarily for use with low level transducers, including load cells, strain gauges and pressure transducers. An outstanding combination of low noise, high gain accuracy, low gain temperature coefficient and high linearity make the AD624 ideal for use in high resolution data acquisition systems.

The AD624C has an input offset voltage drift of less than 0.25μV/°C, output offset voltage drift of less than 10μV/°C, CMRR above 80dB at unity gain (130dB at G=500) and a maximum nonlinearity of 0.001% at G=1. In addition to these outstanding dc specifications, the AD624 exhibits superior ac performance as well. A 25MHz gain bandwidth product, 5V/μs slew rate and 15μs settling time permit the use of the AD624 in high speed data acquisition applications.

The AD624 does not need any external components for pre-trimmed gains of 1, 100, 200, 500 and 1000. Additional gains such as 250 and 333 can be programmed within one percent accuracy with external jumpers. A single external resistor can also be used to set the 624's gain to any value in the range of 1 to 10,000.

PRODUCT HIGHLIGHTS

1. The AD624 offers outstanding noise performance. Input noise is typically less than $4nV/\sqrt{Hz}$ at 1kHz.
2. The AD624 is a functionally complete instrumentation amplifier. Pin programmable gains of 1, 100, 200, 500 and 1000 are provided on the chip. Other gains are achieved through the use of a single external resistor.
3. The offset voltage, offset voltage drift, gain accuracy and gain temperature coefficients are guaranteed for all pre-trimmed gains.
4. The AD624 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effect of offset voltage in gain ranging applications.
5. A sense terminal is provided to enable the user to minimize the errors induced through long leads. A reference terminal is also provided to permit level shifting at the output.

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Gain Equation (External Resistor Gain Programming)	$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$				
Gain Range (Pin Programmable)	1 to 1000			1 to 1000			1 to 1000			1 to 1000				
Gain Error														
G = 1			±0.05			±0.03			±0.02			±0.05		%
G = 100			±0.25			±0.15			±0.1			±0.25		%
G = 200, 500			±0.5			±0.35			±0.25			±0.5		%
G = 1000			±1.0			±1.0			±1.0			±1.0		%
Nonlinearity														
G = 1			±0.005			±0.003			±0.001			±0.005		%
G = 100, 200			±0.005			±0.003			±0.001			±0.005		%
G = 500, 1000			±0.005			±0.005			±0.005			±0.005		%
Gain vs. Temperature														
G = 1			5			5			5			5		ppm/°C
G = 100, 200			10			10			10			10		ppm/°C
G = 500, 1000			25			15			15			15		ppm/°C
VOLTAGE OFFSET (May be Nulled)														
Input Offset Voltage			200			75			25			75		μV
vs. Temperature			2			0.5			0.25			2.0		μV/°C
Output Offset Voltage			5			3			2			3		mV
vs. Temperature			50			25			10			50		μV/°C
Offset Referred to the Input vs. Supply														
G = 1	70			75			80			75				dB
G = 100, 200	95			105			110			105				dB
G = 500, 1000	100			110			115			110				dB
INPUT CURRENT														
Input Bias Current			±50			±25			±15			±50		nA
vs. Temperature		±50			±50			±50			±50			pA/°C
Input Offset Current			±35			±15			±10			±35		nA
vs. Temperature		±20			±20			±20			±20			pA/°C
INPUT														
Input Impedance														
Differential Resistance		10^9			10^9			10^9			10^9			Ω
Differential Capacitance		10			10			10			10			pF
Common-Mode Resistance		10^9			10^9			10^9			10^9			Ω
Common-Mode Capacitance		10			10			10			10			pF
Input Voltage Range[1]														
Max Differ. Input Linear (V_{DL})	±10			±10			±10			±10				V
Max Common-Mode Linear (V_{CM})	$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$				V
Common-Mode Rejection dc to 60Hz with 1kΩ Source Imbalance														
G = 1	70			75			80			70				dB
G = 100, 200	100			105			110			100				dB
G = 500, 1000	110			120			130			110				dB
OUTPUT RATING														
V_{OUT}, R_L = 2kΩ		±10			±10			±10			±10			V
DYNAMIC RESPONSE														
Small Signal – 3dB														
G = 1		1			1			1			1			MHz
G = 100		150			150			150			150			kHz
G = 200		100			100			100			100			kHz
G = 500		50			50			50			50			kHz
G = 1000		25			25			25			25			kHz
Slew Rate		5.0			5.0			5.0			5.0			V/μs
Settling Time to 0.01%, 20V Step														
G = 1 to 200		15			15			15			15			μs
G = 500		35			35			35			35			μs
G = 1000		75			75			75			75			μs
NOISE														
Voltage Noise, 1kHz														
R.T.I.		4			4			4			4			$nV/\sqrt{Hz}$
R.T.O.		75			75			75			75			$nV/\sqrt{Hz}$
R.T.I., 0.1 to 10Hz														
G = 1		10			10			10			10			μV p-p
G = 100		0.3			0.3			0.3			0.3			μV p-p
G = 200, 500, 1000		0.2			0.2			0.2			0.2			μV p-p
Current Noise														
0.1Hz to 10Hz		60			60			60			60			pA p-p
SENSE INPUT														
R_{IN}	8	10	12	8	10	12	8	10	12	8	10	12		kΩ
I_{IN}		30			30			30			30			μA
Voltage Range	±10			±10			±10			±10				V
Gain to Output		1			1			1			1			%
REFERENCE INPUT														
R_{IN}	16	20	24	16	20	24	16	20	24	16	20	24		kΩ
I_{IN}		30			30			30			30			μA
Voltage Range	±10			±10			±10			±10				V
Gain to Output		1			1			1			1			%

Model	AD624A Min	AD624A Typ	AD624A Max	AD624B Min	AD624B Typ	AD624B Max	AD624C Min	AD624C Typ	AD624C Max	AD624S Min	AD624S Typ	AD624S Max	Units
TEMPERATURE RANGE													
Specified Performance	−25		+85	−25		+85	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY													
Power Supply Range	±6	±15	±18	±6	±15	±18	±6	±15	±18	±6	±15	±18	V
Quiescent Current		3.5	5		3.5	5		3.5	5		3.5	5	mA
PACKAGE OPTION[2]													
Ceramic (D-16)	AD624AD			AD624BD			AD624CD			AD624SD, AD624SD/883B			
Chips Available	AD624AChips									AD624SChips			

NOTES

[1] V_{DL} is the maximum differential input voltage at G = 1 for specified nonlinearity. V_{DL} at other gains = 10V/G. V_D = actual differential input voltage. Example: G = 10, V_D = 0.50. V_{CM} = 12V − (10/2 × 0.50V) = 9.5V.

[2] For outline information see Package Information section.

Specifications subject to change without notice.

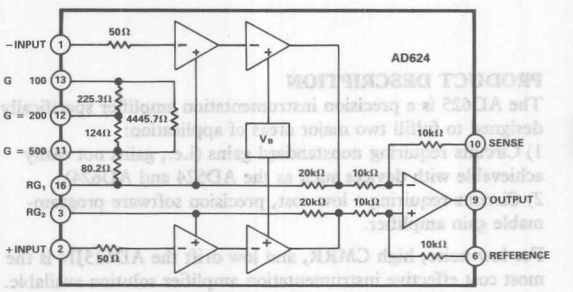
Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±18V
Internal Power Dissipation 420mW
Input Voltage . . . . . ±V_S
Differential Input Voltage . . . . . ±V_S
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD624A/B/C . . . . . −25°C to +85°C
AD624S . . . . . −55°C to +125°C
Lead Temperature (Soldering, 60secs) . . . . . +300°C

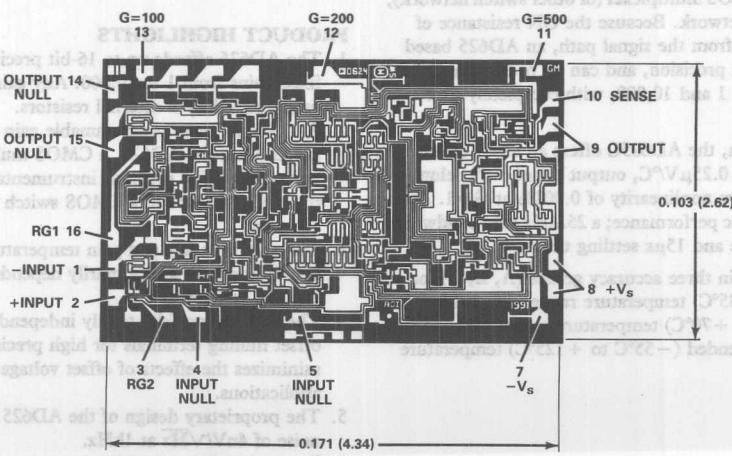
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL BLOCK DIAGRAM



METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Programmable Gain Instrumentation Amplifier

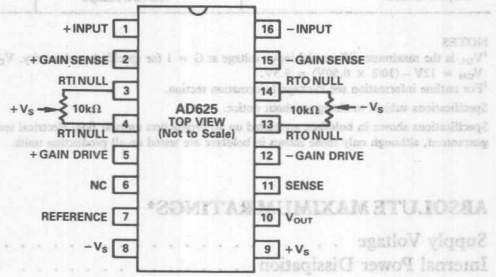
AD625

FEATURES

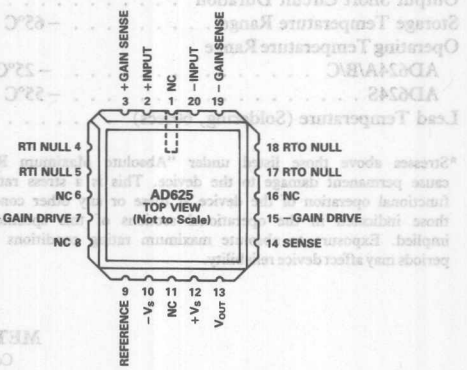
- User Programmable Gains of 1 to 10,000
- Low Gain Error: 0.02% max
- Low Gain TC: 5ppm/°C max
- Low Nonlinearity: 0.001% max
- Low Offset Voltage: 25μV
- Low Noise 4nV/√Hz (at 1kHz) RTI
- Gain Bandwidth Product: 25MHz
- 16-Pin Ceramic or Plastic DIP Package, 20-Pin LCC Package
- Standard Military Drawing Available
- MIL-Standard Parts Available
- Low Cost

CONNECTION DIAGRAMS

Ceramic DIP (D) and Plastic DIP (N) Packages



Leadless Chip Carrier (E) Package



PRODUCT DESCRIPTION

The AD625 is a precision instrumentation amplifier specifically designed to fulfill two major areas of application:
1) Circuits requiring nonstandard gains (i.e., gains not easily achievable with devices such as the AD524 and AD624).
2) Circuits requiring a low cost, precision software programmable gain amplifier.

For low noise, high CMRR, and low drift the AD625JN is the most cost effective instrumentation amplifier solution available. An additional three resistors allow the user to set any gain from 1 to 10,000. The error contribution of the AD625JN is less than 0.05% gain error and under 5ppm/°C gain TC; performance limitations are primarily determined by the external resistors. Common-mode rejection is independent of the feedback resistor matching.

A software programmable gain amplifier (SPGA) can be configured with the addition of a CMOS multiplexer (or other switch network), and a suitable resistor network. Because the ON resistance of the switches is removed from the signal path, an AD625 based SPGA will deliver 12-bit precision, and can be programmed for any set of gains between 1 and 10,000, with completely user selected gain steps.

For the highest precision, the AD625C offers an input offset voltage drift of less than 0.25μV/°C, output offset drift below 15μV/°C, and a maximum nonlinearity of 0.001% at G=1. All grades exhibit excellent ac performance; a 25MHz gain bandwidth product, 5V/μs slew rate and 15μs settling time.

The AD625 is available in three accuracy grades (A, B, C) for industrial (−40°C to +85°C) temperature range, two grades (J, K) for commercial (0 to +70°C) temperature range, and one (S) grade rated over the extended (−55°C to +125°C) temperature range.

PRODUCT HIGHLIGHTS

1. The AD625 affords up to 16-bit precision for user selected fixed gains from 1 to 10,000. Any gain in this range can be programmed by 3 external resistors.
2. A 12-bit software programmable gain amplifier can be configured using the AD625, a CMOS multiplexer and a resistor network. Unlike previous instrumentation amplifier designs, the ON resistance of a CMOS switch does not affect the gain accuracy.
3. The gain accuracy and gain temperature coefficient of the amplifier circuit are primarily dependent on the user selected external resistors.
4. The AD625 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effects of offset voltage in gain-ranging applications.
5. The proprietary design of the AD625 provides input voltage noise of 4nV/√Hz at 1kHz.
6. External resistor matching is not required to maintain high common-mode rejection.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (typical @ $V_S = \pm 15V$, $R_L = 2k\Omega$ and $T_A = +25°C$ unless otherwise specified)

Model	AD625A/J/S Min	AD625A/J/S Typ	AD625A/J/S Max	AD625B/K Min	AD625B/K Typ	AD625B/K Max	AD625C Min	AD625C Typ	AD625C Max	Units
GAIN										
Gain Equation		$\frac{2R_F}{R_G}+1$			$\frac{2R_F}{R_G}+1$			$\frac{2R_F}{R_G}+1$		
Gain Range	1		10,000	1		10,000	1		10,000	
Gain Error[1]		±.035	**±0.05**		±0.02	**±0.03**		±0.01	**±0.02**	%
Nonlinearity, Gain = 1-256			±0.005			±0.002			±0.001	%
Gain>256			±0.01			±0.008			±0.005	%
Gain vs. Temp. Gain<1000[1]			5			5			5	ppm/°C
GAIN SENSE INPUT										
Gain Sense Current		300	**500**		150	**250**		50	**100**	nA
vs. Temperature		5	20		2	15		2	10	nA/°C
Gain Sense Offset Current		150	**500**		75	**250**		50	**100**	nA
vs. Temperature		2	15		1	10		1	5	nA/°C
VOLTAGE OFFSET (May be Nulled)										
Input Offset Voltage		50	**200**		25	**50**		10	**25**	µV
vs. Temperature		1	2/2		0.25	**0.50/1**		0.1	**0.25**	µV/°C
Output Offset Voltage		4	5		2	**3**		1	**2**	mV
vs. Temperature		20	**50/50**		10	**25/40**		10	**15**	µV/°C
Offset Referred to the Input vs. Supply										
G = 1	**70**	75		**75**	85		**80**	90		dB
G = 10	85	95		90	100		95	105		dB
G = 100	95	100		105	110		110	120		dB
G = 1000	**100**	110		**110**	120		**115**	140		dB
INPUT CURRENT										
Input Bias Current		±30	**±50**		±20	**±25**		±10	**±15**	nA
vs. Temperature		±50			±50			±50		pA/°C
Input Offset Current		±2	**±35**		±1	**±15**		±1	**±5**	nA
vs. Temperature		±20			±20			±20		pA/°C
INPUT										
Input Impedance										
Differential Resistance		1			1			1		GΩ
Differential Capacitance		4			4			4		pF
Common-Mode Resistance		1			1			1		GΩ
Common-Mode Capacitance		4			4			4		pF
Input Voltage Range										
Differ. Input Linear (V_{DL})[2]	±10			±10			±10			V
Common-Mode Linear (V_{CM})	$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			
Common-Mode Rejection Ratio dc to 60Hz with 1kΩ Source Imbalance										
G = 1	**70**	75		**75**	85		**80**	90		dB
G = 10	90	95		95	105		100	115		dB
G = 100	100	105		105	115		110	125		dB
G = 1000	**110**	115		**115**	125		**120**	140		dB
OUTPUT RATING		±10V @5mA			±10V @5mA			±10V @5mA		
DYNAMIC RESPONSE										
Small Signal − 3dB										
G = 1 (R_F = 20kΩ)		650			650			650		kHz
G = 10		400			400			400		kHz
G = 100		150			150			150		kHz
G = 1000		25			25			25		kHz
Slew Rate		5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20V Step										
G = 1 to 200		15			15			15		µs
G = 500		35			35			35		µs
G = 1000		75			75			75		µs
NOISE										
Voltage Noise, 1kHz										
R.T.I.		4			4			4		nV/√Hz
R.T.O.		75			75			75		nV/√Hz
R.T.I., 0.1 to 10Hz										
G = 1		10			10			10		µV p-p
G = 10		1.0			1.0			1.0		µV p-p
G = 100		0.3			0.3			0.3		µV p-p
G = 1000		0.2			0.2			0.2		µV p-p
Current Noise										
0.1Hz to 10Hz		60			60			60		pA p-p

Model	AD625A/J/S Min	AD625A/J/S Typ	AD625A/J/S Max	AD625B/K Min	AD625B/K Typ	AD625B/K Max	AD625C Min	AD625C Typ	AD625C Max	Units
SENSE INPUT										
R_{IN}		10			10			10		kΩ
I_{IN}		30			30			30		μA
Voltage Range	±10			±10			±			V
Gain to Output		1 ± 0.01			1 ± 0.01			1 ± 0.01		%
REFERENCE INPUT										
R_{IN}		20			20			20		kΩ
I_{IN}		30			30			30		μA
Voltage Range	±10			±10			±			V
Gain to Output		1 ± 0.01			1 ± 0.01			1 ± 0.01		%
TEMPERATURE RANGE										
Specified Performance										
J/K Grades	0		+70	0		+70				°C
A/B/C Grades	−40		+85	−40		+85	−40		+85	°C
S Grade	−55		+125							
Storage	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY										
Power Supply Range		±6 to ±18			±6 to ±18			±6 to ±18		V
Quiescent Current		3.5	5		3.5	5		3.5	5	mA

NOTES
[1]Gain Error and Gain TC are for the AD625 only. Resistor network errors will add to the specified errors.
[2]V_{DL} is the maximum differential input voltage at G = 1 for specified nonlinearity.
V_{DL} at other gains = 10V/G.
V_D = actual differential input voltage.
Example: G = 10, V_D = 0.50
V_{CM} = 12V–(10/2 × 0.50V) = 9.5V.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation 450mW
Input Voltage . . . . . ±V_S
Differential Input Voltage . . . . . ±V_S
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (D, E) . . . . . −65°C to +150°C
(N) . . . . . −65°C to +125°C
Operating Temperature Range
AD625J/K . . . . . 0 to +70°C
AD625A/B/C . . . . . −40°C to +85°C
AD625S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering, 60 seconds) . . . . . +300°C

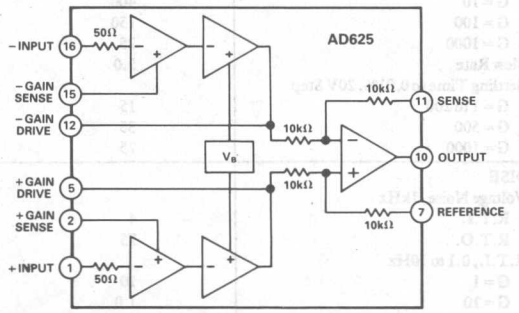
NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD625AD	−40°C to +85°C	16-Pin Ceramic DIP	D-16
AD625BD	−40°C to +85°C	16-Pin Ceramic DIP	D-16
AD625CD	−40°C to +85°C	16-Pin Ceramic DIP	D-16
AD625SD	−55°C to +125°C	16-Pin Ceramic DIP	D-16
AD625SD/883B	−55°C to +125°C	16-Pin Ceramic DIP	D-16
AD625SE/883B	−55°C to +125°C	20-Pin Leadless Chip Carrier	E-20A
AD625JN	−40°C to +85°C	16-Pin Plastic DIP	N-16
AD625KN	−40°C to +85°C	16-Pin Plastic DIP	N-16
AD625AChips	−40°C to +85°C	Die	
AD625SChips	−55°C to +125°C	Die	
5962–8771901EA	Standard Military Drawing Available		

*For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM
("N" AND "D" PACKAGE PINOUT)



Low Cost, Single Supply Differential Amplifier

AD626

FEATURES

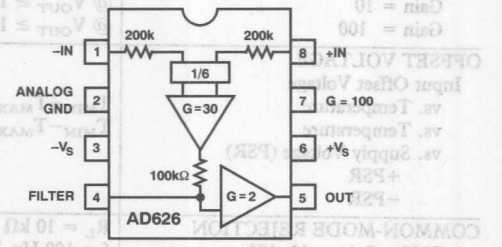
- Pin Selectable Gains of 10 and 100
- True Single Supply Operation
  - Single Supply Range of +2.4 V to +10 V
  - Dual Suppy Range of ±1.2 V to ±6 V
  - Wide Output Voltage Range of 30 mV to 4.7 V
- Optional Low-Pass Filtering
- Excellent DC Performance
  - Low Input Offset Voltage: 500 μV max
  - Large Common-Mode Range: 0 V to +54 V
  - Low Power: 1.2 mW (V_S = +5 V)
  - Good CMR of 90 dB typ
- AC Performance
  - Fast Settling Time: 24 μs (0.01%)
- Includes Input Protection
  - Series Resistive Inputs (R_{IN} = 200 kΩ)
  - RFI Filters Included
  - Allows 50 V Continuous Overload

APPLICATIONS

- Current Sensing
- Interface for Pressure Transducers, Position Indicators, Strain Gages, and Other Low Level Signal Sources

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N) and SOIC (R) Packages



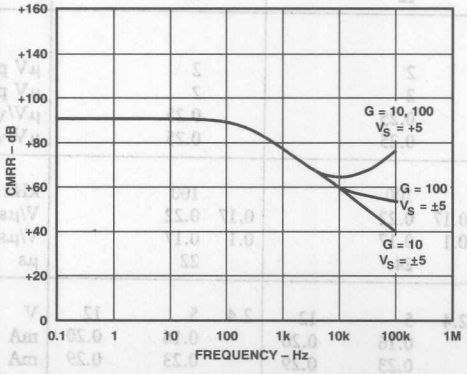
PRODUCT DESCRIPTION

The AD626 is a low cost, true single supply differential amplifier designed for amplifying and low-pass filtering small differential voltages from sources having a large common-mode voltage.

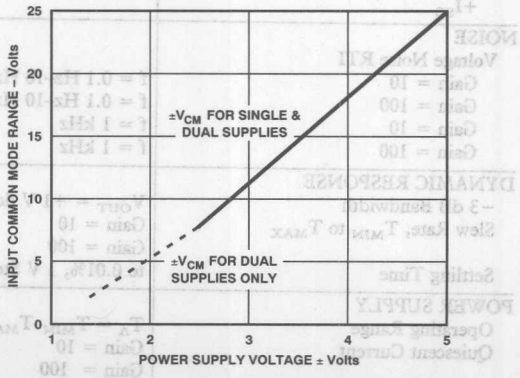
The AD626 can operate from either a single supply of +2.4 V to +10 V, or dual supplies of ±1.2 V to ±6 V. The input common-mode range of this amplifier is equal to 6 (+V_S −1 V) which provides a +24 V CMR while operating from a +5 V supply. Furthermore, the AD626 features a CMR of 90 dB typ.

The amplifier's inputs are protected against continuous overload of up to 50 V, and RFI filters are included in the attenuator network. The output range is +0.03 V to +4.9 V using a +5 V supply. The amplifier provides a preset gain of 10, but gains between 10 to 100 can be easily configured with an external resistor. Furthermore, a gain of 100 is available by connecting the G = 100 pin to analog ground. The AD626 also offers low- pass filter capability by connecting a capacitor between the filter pin and analog ground.

The AD626A and AD626B operate over the industrial temperature range of −40°C to +85°C. The AD626 is available in two 8-pin packages: a plastic mini-DIP and SOIC.



Common-Mode Rejection vs. Frequency



Input Common-Mode Range vs. Supply

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

REV. B

AD626—SPECIFICATIONS

SINGLE SUPPLY (@ $+V_S$ = +5 V and T_A = +25°C)

Model	Conditions	AD626A Min	AD626A Typ	AD626A Max	AD626B Min	AD626B Typ	AD626B Max	Units
GAIN								
Gain Accuracy	Total Error							
Gain = 10	@ $V_{OUT} \geq$ 100 mV dc		0.04	1.0		0.2	0.6	%
Gain = 100	@ $V_{OUT} \geq$ 100 mV dc		0.1	1.0		0.5	0.6	%
Over Temperature, $T_A = T_{MIN}$–T_{MAX}	G = 10			50			30	ppm/°C
	G = 100			150			120	ppm/°C
Gain Linearity								
Gain = 10	@ $V_{OUT} \geq$ 100 mV dc		0.014	0.016		0.014	0.016	%
Gain = 100	@ $V_{OUT} \geq$ 100 mV dc		0.014	0.02		0.014	0.02	%
OFFSET VOLTAGE								
Input Offset Voltage			1.9	2.5		1.9	2.5	mV
vs. Temperature	T_{MIN}–T_{MAX}, G = 10 or 100			2.9			2.9	mV
vs. Temperature	T_{MIN}–T_{MAX}, G = 10 or 100			6			6	µV/°C
vs. Supply Voltage (PSR)								
+PSR		74	80		74	80		dB
−PSR		64	66		64	66		dB
COMMON-MODE REJECTION	R_L = 10 kΩ							
+CMR Gain = 10, 100	f = 100 Hz, V_{CM} = +24 V	66	90		80	90		dB
±CMR Gain = 10, 100	f = 10 kHz, V_{CM} = 6 V	55	64		55	64		dB
−CMR Gain = 10, 100[1]	f = 100 Hz, V_{CM} = −2 V	60	85		73	85		dB
COMMON-MODE VOLTAGE RANGE								
+CMV Gain = 10	CMR > 85 dB		+24			+24		V
−CMV Gain = 10	CMR > 85 dB		−2			−2		V
INPUT								
Input Resistance								
Differential			200			200		kΩ
Common Mode			100			100		kΩ
Input Voltage Range (Common Mode)			6 (V_S−1)			6 (V_S−1)		V
OUTPUT								
Output Voltage Swing	R_L = 10 kΩ							
Positive	Gain = 10	4.7	4.90		4.7	4.90		V
	Gain = 100	4.7	4.90		4.7	4.90		V
Negative	Gain = 10	0.03			0.03			V
	Gain = 100	0.03			0.03			V
Short Circuit Current								
$+I_{SC}$			12			12		mA
NOISE								
Voltage Noise RTI								
Gain = 10	f = 0.1 Hz–10 Hz		2			2		µV p–p
Gain = 100	f = 0.1 Hz–10 Hz		2			2		µV p–p
Gain = 10	f = 1 kHz		0.25			0.25		$\mu V/\sqrt{Hz}$
Gain = 100	f = 1 kHz		0.25			0.25		$\mu V/\sqrt{Hz}$
DYNAMIC RESPONSE								
−3 dB Bandwidth	V_{OUT} = +1 V dc		100			100		kHz
Slew Rate, T_{MIN} to T_{MAX}	Gain = 10	0.17	0.22		0.17	0.22		V/µs
	Gain = 100	0.1	0.17		0.1	0.17		V/µs
Settling Time	to 0.01%, 1 V Step		24			22		µs
POWER SUPPLY								
Operating Range	$T_A = T_{MIN}$–T_{MAX}	2.4	5	12	2.4	5	12	V
Quiescent Current	Gain = 10		0.16	0.20		0.16	0.20	mA
	Gain = 100		0.23	0.29		0.23	0.29	mA
TRANSISTOR COUNT	# of Transistors		46			46		

NOTES

[1]At temperatures above +25°C, −CMV degrades at the rate of 12 mV/°C; i.e., @ +25°C CMV = −2 V, @ +85°C CMV = −1.28 V.

Specifications subject to change without notice.

DUAL SUPPLY (@ $+V_S = \pm5$ V and $T_A = +25°C$)

Model	Conditions	AD626A Min	AD626A Typ	AD626A Max	AD626B Min	AD626B Typ	AD626B Max	Units
GAIN								
Gain Accuracy	Total Error							
Gain = 10	R_L = 10 kΩ		0.2	0.5		0.1	0.3	%
Gain = 100			0.25	1.0		0.15	0.6	%
Over Temperature, $T_A = T_{MIN}$–T_{MAX}								
	G = 10			50			30	ppm/°C
	G = 100			100			80	ppm/°C
Gain Linearity								
Gain = 10			0.045	0.055		0.045	0.055	%
Gain = 100			0.01	0.015		0.01	0.015	%
OFFSET VOLTAGE								
Input Offset Voltage			50	500		50	250	μV
vs. Temperature	T_{MIN}–T_{MAX}, G = 10 or 100			1.0			0.5	mV
vs. Temperature	T_{MIN}–T_{MAX}, G = 10 or 100		1.0			0.5		μV/°C
vs. Supply Voltage (PSR)								
+PSR		74	80		74	80		dB
−PSR		64	66		64	66		dB
COMMON-MODE REJECTION	R_L = 10 kΩ							
±CMR Gain = 10, 100	f = 100 Hz, V_{CM} = 24 V	66	90		80	90		dB
±CMR Gain = 10, 100	f = 10 kHz, V_{CM} = 6 V	55	60		55	60		dB
COMMON-MODE VOLTAGE RANGE								
+CMV Gain = 10	CMR > 85 dB		26.5			26.5		V
−CMV Gain = 10	CMR > 85 dB		32.5			32.5		V
INPUT								
Input Resistance								
Differential			200			200		kΩ
Common Mode			110			110		kΩ
Input Voltage Range (Common Mode)			6 (V_S−1)			6 (V_S−1)		V
OUTPUT								
Output Voltage Swing	R_L = 10 kΩ							
Positive	Gain = 10, 100	4.7	4.90		4.7	4.90		V
Negative	Gain = 10	1.65	2.1		1.65	2.1		V
	Gain = 100	1.45	1.8		1.45	1.8		V
Short Circuit Current								
$+I_{SC}$			12			12		mA
$-I_{SC}$			0.5			0.5		mA
NOISE								
Voltage Noise RTI								
Gain = 10	f = 0.1 Hz–10 Hz		2			2		μV p–p
Gain = 100	f = 0.1 Hz–10 Hz		2			2		μV p–p
Gain = 10	f = 1 kHz		0.25			0.25		μV/√Hz
Gain = 100	f = 1 kHz		0.25			0.25		μV/√Hz
DYNAMIC RESPONSE								
−3 dB Bandwidth	V_{OUT} = +1 V dc		100			100		kHz
Slew Rate, T_{MIN} to T_{MAX}	Gain = 10	0.17	0.22		0.17	0.22		V/μs
	Gain = 100	0.1	0.17		0.1	0.17		V/μs
Settling Time	to 0.01%, 2 V Step		24			24		μs
POWER SUPPLY								
Operating Range	$T_A = T_{MIN}$–T_{MAX}	±1.2	±5	±6	±1.2	±5	±6	V
Quiescent Current	Gain = 10		1.5	2		1.5	2	mA
	Gain = 100		1.5	2		1.5	2	mA
TRANSISTOR COUNT	# of Transistors		46			46		

10

Supply Voltage	+36 V
Internal Power Dissipation[2]	
Peak Input Voltage	60 V
Maximum Reversed Supply Voltage Limit	−34 V
Output Short Circuit Duration	Indefinite
Storage Temperature Range (N, R)	−65°C to +125°C
Operating Temperature Range	
AD626A/B	−40°C to +85°C
Lead Temperature Range (Soldering 60 sec)	+300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]8-Pin Plastic Package: θ_{JA} = 100°C/Watt, θ_{JC} = 50°C/Watt
8-Pin Plastic SOIC Package: θ_{JA} = 160°C/Watt, θ_{JC} = 42°C/Watt

An ESD classification per method 3015.6 of MIL STD 883C has been performed on the AD626, which is a Class 1 device.

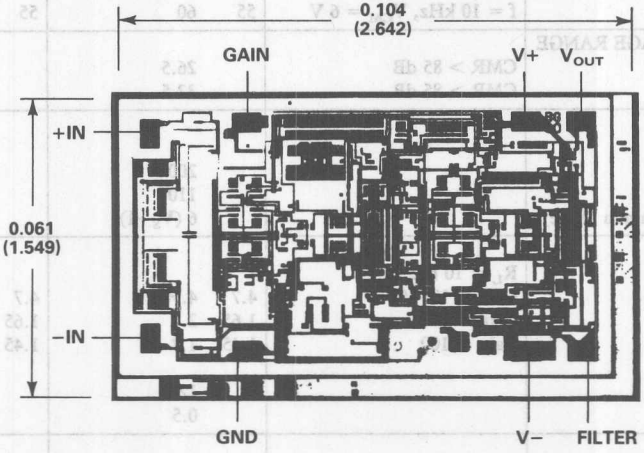
ORDERING GUIDE

Model	Temperature Range	Package Options*
AD626AN	−40°C to +85°C	N-8
AD626AR	−40°C to +85°C	R-8
AD626BN	−40°C to +85°C	N-8

*N = Plastic DIP; R = Small Outline IC. For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



Low Noise, Precision Instrumentation Amplifier

AMP01

FEATURES

- Low Offset Voltage ..... 50μV Max
- Very Low Offset Voltage Drift ..... 0.3μV/°C Max
- Low Noise ..... $0.12\mu V_{p-p}$ (0.1Hz to 10Hz)
- Excellent Output Drive ..... ±10V at ±50mA
- Capacitive Load Stability ..... to 1μF
- Gain Range ..... 0.1 to 10,000
- Excellent Linearity ..... 16-Bit at G = 1000
- High CMR ..... 125dB Min (G = 1000)
- Low Bias Current ..... 4nA Max
- May be Configured as a Precision Op-Amp
- Output-Stage Thermal Shutdown
- Available in Die Form

ORDERING INFORMATION†

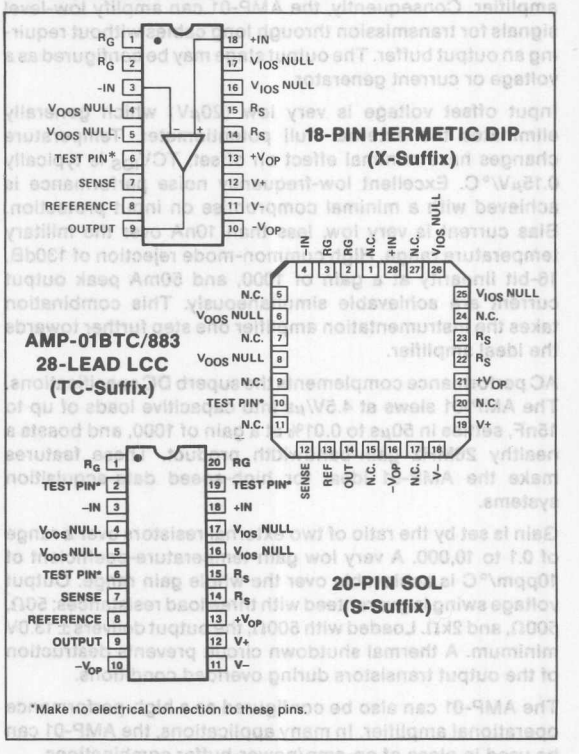
PACKAGE			OPERATING
CERDIP 18-PIN	LCC	PLASTIC 20-PIN	TEMPERATURE RANGE
AMP01AX*	—	—	MIL
AMP01BX*	AMP01BTC/883	—	MIL
AMP01EX	—	—	IND
AMP01FX	—	—	IND
—	—	AMP01GS††	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

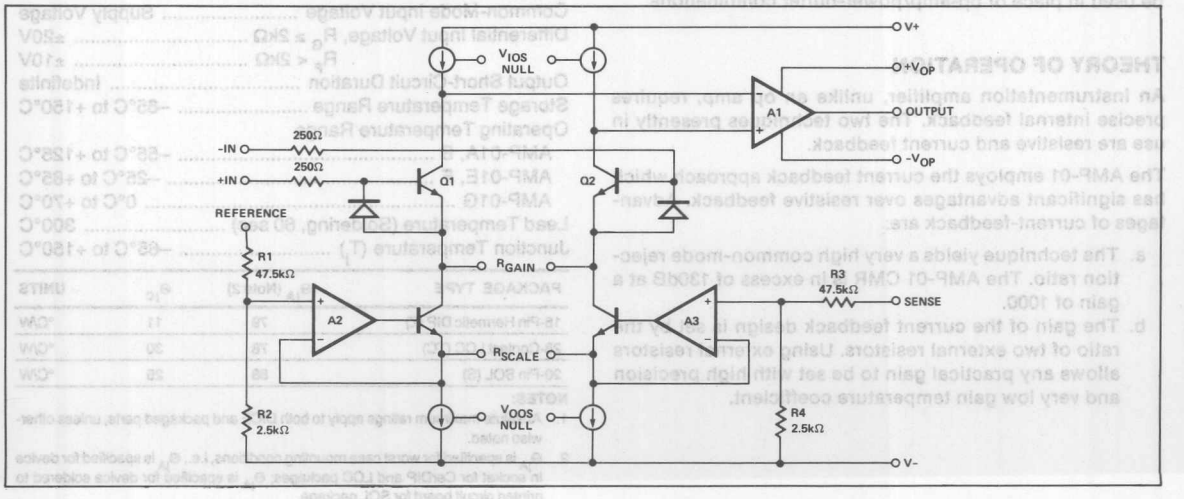
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



Manufactured under the following U.S. patents: 4,471,321 and 4,503,381.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AMP01

GENERAL DESCRIPTION

The AMP-01 is a monolithic instrumentation amplifier designed for high-precision data acquisition and instrumentation applications. The design combines the conventional features of an instrumentation amplifier with a high-current output stage. The output remains stable with high capacitance loads (1μF), a unique ability for an instrumentation amplifier. Consequently, the AMP-01 can amplify low-level signals for transmission through long cables without requiring an output buffer. The output stage may be configured as a voltage or current generator.

Input offset voltage is very low (20μV) which generally eliminates the external null potentiometer. Temperature changes have minimal effect on offset; TCV_{IOS} is typically 0.15μV/°C. Excellent low-frequency noise performance is achieved with a minimal compromise on input protection. Bias current is very low, less than 10nA over the military temperature range. High common-mode rejection of 130dB, 16-bit linearity at a gain of 1000, and 50mA peak output current are achievable simultaneously. This combination takes the instrumentation amplifier one step further towards the ideal amplifier.

AC performance complements the superb DC specifications. The AMP-01 slews at 4.5V/μs into capacitive loads of up to 15nF, settles in 50μs to 0.01% at a gain of 1000, and boasts a healthy 26MHz gain-bandwidth product. These features make the AMP-01 ideal for high-speed data-acquisition systems.

Gain is set by the ratio of two external resistors over a range of 0.1 to 10,000. A very low gain-temperature-coefficient of 10ppm/°C is achievable over the whole gain range. Output voltage swing is guaranteed with three load resistances; 50Ω, 500Ω, and 2kΩ. Loaded with 500Ω, the output delivers ±13.0V minimum. A thermal shutdown circuit prevents destruction of the output transistors during overload conditions.

The AMP-01 can also be configured as a high-performance operational amplifier. In many applications, the AMP-01 can be used in place of op-amp/power-buffer combinations.

THEORY OF OPERATION

An instrumentation amplifier, unlike an op amp, requires precise internal feedback. The two techniques presently in use are resistive and current feedback.

The AMP-01 employs the current feedback approach which has significant advantages over resistive feedback. Advantages of current-feedback are:

a. The technique yields a very high common-mode rejection ratio. The AMP-01 CMR is in excess of 130dB at a gain of 1000.
b. The gain of the current feedback design is set by the ratio of two external resistors. Using external resistors allows any practical gain to be set with high precision and very low gain temperature coefficient.
c. The current-feedback design is immune to CMR degradation when series resistance is added to the reference input. A small (trimmable) offset change results from added resistance, e.g. a printed circuit track.

The AMP-01 utilizes low-drift thin-film resistors to minimize output offset temperature drift. A feedback voltage-to-current converter is employed having high linearity and low noise, particularly at low frequencies. Parameter shifts during packaging are eliminated by a post-assembly trimming technique which electronically adjusts the output offset voltage.

The AMP-01 input transistors Q1 and Q2 feed active loads, yielding stage gain in excess of 4000 (see simplified schematic) The output amplifier, A1, is a two-stage design having a gain of about 50,000 driving a 100Ω load. Overall gain of 2×10^8 yields excellent linearity, even at high closed-loop gains.

Low bias current is achieved by using Ion-implanted superbeta transistors combined with a new bias-current cancellation system, patents applied for. Input bias current remains below 10nA over the military temperature range, −55°C to +125°C.

Superbeta transistors use a new transistor geometry resulting in an input noise of only $5nV/\sqrt{Hz}$ at G = 1000. Noise includes contributions from the gain-setting resistor and internal overload-protection resistor. The input stage achieves an offset voltage drift of less than 0.3μV/°C (E Grade).

The AMP-01 uses a unique two-pole compensation scheme where the load capacitance is incorporated into the dominate pole. Stable operation results even with high capacitance loads. The high output current capability (90mA peak) allows the 4.5V/μs slew-rate to be maintained with load capacitance as high as 15nF.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Common-Mode Input Voltage ..... Supply Voltage
Differential Input Voltage, $R_G \geq 2k\Omega$ ..... ±20V
$R_F < 2k\Omega$ ..... ±10V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
AMP-01A, B ..... −55°C to +125°C
AMP-01E, F ..... −25°C to +85°C
AMP-01G ..... 0°C to +70°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... −65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (Z)	79	11	°C/W
28-Contact LCC (TC)	78	30	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A MIN	AMP-01A TYP	AMP-01A MAX	AMP-01B MIN	AMP-01B TYP	AMP-01B MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	$T_A = 25°C$	—	20	50	—	40	100	µV
		$-55°C \le T_A \le +125°C$	—	40	80	—	60	150	
Input Offset Voltage Drift	TCV_{IOS}	$-55°C \le T_A \le +125°C$	—	0.15	0.3	—	0.3	1.0	µV/°C
Output Offset Voltage	V_{OOS}	$T_A = 25°C$	—	1	3	—	2	6	mV
		$-55°C \le T_A \le +125°C$	—	3	6	—	6	10	
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$ $-55°C \le T_A \le +125°C$	—	20	50	—	50	120	µV/°C
Offset Referred to Input vs. Positive Supply V+ = +5V to +15V	PSR	G = 1000	120	130	—	110	120	—	dB
		G = 100	110	130	—	100	120	—	
		G = 10	95	110	—	90	100	—	
		G = 1	75	90	—	70	80	—	
		$-55°C \le T_A \le +125°C$							
		G = 1000	120	130	—	110	120	—	dB
		G = 100	110	130	—	100	120	—	
		G = 10	95	110	—	90	100	—	
		G = 1	75	90	—	70	80	—	
Offset Referred to Input vs. Negative Supply V− = −5V to −15V	PSR	G = 1000	105	125	—	105	115	—	dB
		G = 100	90	105	—	90	95	—	
		G = 10	70	85	—	70	75	—	
		G = 1	50	65	—	50	60	—	
		$-55°C \le T_A \le +125°C$							
		G = 1000	105	125	—	105	115	—	dB
		G = 100	90	105	—	90	95	—	
		G = 10	70	85	—	70	75	—	
		G = 1	50	65	—	50	60	—	
Input Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	±6	—	—	±6	—	mV
Output Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	±100	—	—	±100	—	mV
INPUT CURRENT									
Input Bias Current	I_B	$T_A = 25°C$	—	1	4	—	2	6	nA
		$-55°C \le T_A \le +125°C$	—	4	10	—	6	15	
Input Bias Current Drift	TCI_B	$-55°C \le T_A \le +125°C$	—	40	—	—	50	—	pA/°C
Input Offset Current	I_{OS}	$T_A = 25°C$	—	0.2	1.0	—	0.5	2.0	nA
		$-55°C \le T_A \le +125°C$	—	0.5	3.0	—	1.0	6.0	
Input Offset Current Drift	TCI_{OS}	$-55°C \le T_A \le +125°C$	—	3	—	—	5	—	pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G = 1000	—	1	—	—	1	—	GΩ
		Differential, G ≤ 100	—	10	—	—	10	—	
		Common-Mode, G = 1000	—	20	—	—	20	—	
Input Voltage Range	IVR	$T_A = 25°C$ (Note 2)	±10.5	—	—	±10.5	—	—	V
		$-55°C \le T_A \le +125°C$	±10.0	—	—	±10.0	—	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$, 1kΩ source imbalance							
		G = 1000	125	130	—	115	125	—	dB
		G = 100	120	130	—	110	125	—	
		G = 10	100	120	—	95	110	—	
		G = 1	85	100	—	75	90	—	
		$-55°C \le T_A \le +125°C$							
		G = 1000	120	125	—	110	120	—	dB
		G = 100	115	125	—	105	120	—	
		G = 10	95	115	—	90	105	—	
		G = 1	80	95	—	75	90	—	

NOTES:

1. V_{IOS} and V_{OOS} nulling has minimal affect on TCV_{IOS} and TCV_{OOS}, respectively.
2. Refer to section on common-mode rejection.

10

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	T_A = +25°C	–	20	50	–	40	100	µV
		$T_{MIN} \le T_A \le T_{MAX}$	–	40	80	–	60	150	
Input Offset Voltage Drift	TCV_{IOS}	$T_{MIN} \le T_A \le T_{MAX}$ (Note 2)	–	0.15	0.3	–	0.3	1.0	µV/°C
Output Offset Voltage	V_{OOS}	T_A = +25°C	–	1	3	–	2	6	mV
		$T_{MIN} \le T_A \le T_{MAX}$	–	3	6	–	6	10	
Output Offset Voltage Drift	TCV_{OOS}	RG = ∞ (Note 2)	–	20	100	–	50	120	µV/°C
		$T_{MIN} \le T_A \le T_{MAX}$							
Offset Referred to Input vs. Positive Supply V+ = +5V to +15V	PSR	G = 1000	120	130	–	110	120	–	dB
		G = 100	110	130	–	100	120	–	
		G = 10	95	110	–	90	100	–	
		G = 1	75	90	–	70	80	–	
		$T_{MIN} \le T_A \le T_{MAX}$							
		G = 1000	120	130	–	110	120	–	dB
		G = 100	110	130	–	100	120	–	
		G = 10	95	110	–	90	100	–	
		G = 1	75	90	–	70	80	–	
Offset Referred to Input vs. Negative Supply V– = –5V to –15V	PSR	G = 1000	110	125	–	105	115	–	dB
		G = 100	95	105	–	90	95	–	
		G = 10	75	85	–	70	75	–	
		G = 1	55	65	–	50	60	–	
		$T_{MIN} \le T_A \le T_{MAX}$							
		G = 1000	110	125	–	105	115	–	dB
		G = 100	95	105	–	90	95	–	
		G = 10	75	85	–	70	75	–	
		G = 1	55	65	–	50	60	–	
Input Offset Voltage Trim Range		V_S = ±4.5V to ±18V (Note 1)	–	±6	–	–	±6	–	mV
Output Offset Voltage Trim Range		V_S = ±4.5V to ±18V (Note 1)	–	±100	–	–	±100	–	mV
INPUT CURRENT									
Input Bias Current	I_B	T_A = +25°C	–	1	4	–	2	6	mV
		$T_{MIN} \le T_A \le T_{MAX}$	–	4	10	–	6	15	
Input Bias Current Drift	TCI_B	$T_{MIN} \le T_A \le T_{MAX}$	–	40	–	–	50	–	pA/°C
Input Offset Current	I_B	T_A = +25°C	–	0.2	1.0	–	0.5	2.0	mV
		$T_{MIN} \le T_A \le T_{MAX}$	–	0.5	3.0	–	1.0	6.0	
Input Offset Current Drift	TCI_{OS}	$T_{MIN} \le T_A \le T_{MAX}$	–	3	–	–	5	–	pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G = 1000	–	1	–	–	1	–	GΩ
		Differential, G ≤ 100	–	10	–	–	10	–	
		Common-Mode, G = 1000	–	20	–	–	20	–	
Input Voltage Range	IVR	T_A = +25°C (Note 3)	±10.5	–	–	±10.5	–	–	V
		$T_{MIN} \le T_A \le T_{MAX}$	±10.0	–	–	±10.0	–	–	
Common-Mode Rejection	CMR	V_{CM} = ±10V, 1kΩ source imbalance							
		G = 1000	125	130	–	115	125	–	dB
		G = 100	120	130	–	110	125	–	
		G = 10	100	120	–	95	110	–	
		G = 1	85	100	–	75	90	–	
		$T_{MIN} \le T_A \le T_{MAX}$							
		G = 1000	120	125	–	110	120	–	dB
		G = 100	115	125	–	105	120	–	
		G = 10	95	115	–	90	105	–	
		G = 1	80	95	–	75	90	–	

NOTES:

1. V_{IOS} and V_{OOS} nulling has minimal effect on TCV_{IOS} and TCV_{OOS}, respectively.
2. Sample tested.
3. Refer to section on common-mode rejection.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A/E MIN	AMP-01A/E TYP	AMP-01A/E MAX	AMP-01B/F/G MIN	AMP-01B/F/G TYP	AMP-01B/F/G MAX	UNITS
GAIN									
Gain Equation Accuracy		$G = \frac{20 \times R_S}{R_G}$ Accuracy Measured from G = 1 to 1000	—	0.3	0.6	—	0.5	0.8	%
Gain Range	G		0.1	—	10k	0.1	—	10k	V/V
Nonlinearity		G = 1000 (Note 1)	—	0.0007	0.005	—	0.0007	0.005	%
		G = 100	—	—	0.005	—	—	0.005	
		G = 10	—	—	0.005	—	—	0.007	
		G = 1	—	—	0.010	—	—	0.015	
Temperature Coefficient	G_{TC}	$1 \le G \le 1000$ (Notes 1, 2)	—	5	10	—	5	15	ppm/°C
OUTPUT RATING									
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	±13.0	±13.8	—	±13.0	±13.8	—	V
		$R_L = 500\Omega$	±13.0	±13.5	—	±13.0	±13.5	—	
		$R_L = 50\Omega$	±2.5	±4.0	—	±2.5	±4.0	—	
		$R_L = 2k\Omega$ Over Temp.	±12.0	±13.8	—	±12.0	±13.8	—	V
		$R_L = 500\Omega$ (Note 3)	±12.0	±13.5	—	±12.0	±13.5	—	
Positive Current Limit		Output-to-Ground Short	60	100	120	60	100	120	mA
Negative Current Limit		Output-to-Ground Short	60	90	120	60	90	120	mA
Capacitive Load Stability		$1 \le G \le 1000$ No Oscillations, (Note 1)	0.1	1	—	0.1	1	—	µF
Thermal Shutdown Temperature		Junction Temperature	—	165	—	—	165	—	°C
NOISE									
Voltage Density, RTI	e_n	f_O = 1kHz							$nV/\sqrt{Hz}$
		G = 1000	—	5	—	—	5	—	
		G = 100	—	10	—	—	10	—	
		G = 10	—	59	—	—	59	—	
		G = 1	—	540	—	—	540	—	
Noise Current Density, RTI	i_n	f_O = 1kHz, G = 1000	—	0.15	—	—	0.15	—	$pA/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz							μV_{p-p}
		G = 1000	—	0.12	—	—	0.12	—	
		G = 100	—	0.16	—	—	0.16	—	
		G = 10	—	1.4	—	—	1.4	—	
		G = 1	—	13	—	—	13	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz, G = 1000	—	2	—	—	2	—	pA_{p-p}
DYNAMIC RESPONSE									
Small-Signal Bandwidth (–3dB)	BW	G = 1	—	570	—	—	570	—	kHz
		G = 10	—	100	—	—	100	—	
		G = 100	—	82	—	—	82	—	
		G = 1000	—	26	—	—	26	—	
Slew Rate	SR	G = 10	3.5	4.5	—	3.0	4.5	—	V/µs
Settling Time	t_S	To 0.01%, 20V step							µs
		G = 1	—	12	—	—	12	—	
		G = 10	—	13	—	—	13	—	
		G = 100	—	15	—	—	15	—	
		G = 1000	—	50	—	—	50	—	

NOTES:
1. Guaranteed by design.
2. Gain tempco does not include the effects of gain and scale resistor tempco match.
3. $-55°C \le T_A \le +125°C$ for A/B grades, $-25°C \le T_A \le +85°C$ for E/F grades, $0°C \le T_A \le 70°C$ FOR G grades.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A/E MIN	AMP-01A/E TYP	AMP-01A/E MAX	AMP-01B/F/G MIN	AMP-01B/F/G TYP	AMP-01B/F/G MAX	UNITS
SENSE INPUT									
Input Resistance	R_{IN}		35	50	65	35	50	65	kΩ
Input Current	I_{IN}	Referenced to V–	—	280	—	—	280	—	μA
Voltage Range		(Note 1)	−10.5	—	+15	−10.5	—	+15	V
REFERENCE INPUT									
Input Resistance	R_{IN}		35	50	65	35	50	65	kΩ
Input Current	I_{IN}	Referenced to V–	—	280	—	—	280	—	μA
Voltage Range		(Note 1)	−10.5	—	+15	−10.5	—	+15	V
Gain to Output			—	1	—	—	1	—	V/V
POWER SUPPLY $-25°C \le T_A \le +85°C$ for E/F Grades, $-55°C \le T_A \le +125°C$ for A/B Grades									
Supply Voltage Range	V_S	+V linked to $+V_{OP}$ −V linked to $-V_{OP}$	±4.5	—	±18	±4.5	—	±18	V
Quiescent Current	I_Q	+V linked to $+V_{OP}$	—	3.0	4.8	—	3.0	4.8	mA
		−V linked to $-V_{OP}$	—	3.4	4.8	—	3.4	4.8	

NOTE:
1. Guaranteed by design.

FEATURES

- Low Offset Voltage ..... 100µV Max
- Low Drift ..... 2µV/°C Max
- Wide Gain Range ..... 1 to 10,000
- High Common-Mode Rejection ..... 115dB Min
- High Bandwidth (G = 1000) ..... 200kHz Typ
- Gain Equation Accuracy ..... 0.5% Max
- Single Resistor Gain Set
- Input Overvoltage Protection
- Low Cost
- Available In Die Form

APPLICATIONS

- Differential Amplifier
- Strain Gauge Amplifier
- Thermocouple Amplifier
- RTD Amplifier
- Programmable Gain Instrumentation Amplifier
- Medical Instrumentation
- Data Acquisition Systems

ORDERING INFORMATION †

T_A = +25°C V_{IOS} MAX (µV)	V_{OOS} MAX (mV)	PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
100	4	AMP02EP	XIND
200	8	AMP02FP	XIND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The AMP-02 is the first precision instrumentation amplifier available in an 8-pin package. Gain of the AMP-02 is set by a single external resistor, and can range from 1 to 10,000. No gain set resistor is required for unity gain. The AMP-02 includes an input protection network that allows the inputs to be taken 60V beyond either supply rail without damaging the device.

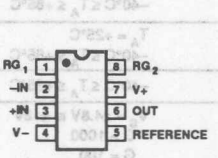
Laser trimming reduces the input offset voltage to under 100µV. Output offset voltage is below 4mV and gain accuracy is better than 0.5% for gain of 1000. PMI's proprietary thin-film resistor process keeps the gain temperature coefficient under 50 ppm/°C.

Due to the AMP-02's design, its bandwidth remains very high over a wide range of gain. Slew rate is over 4V/µs making the AMP-02 ideal for fast data acquisition systems.

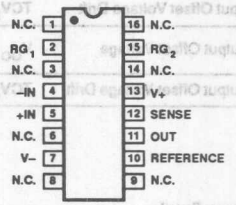
A reference pin is provided to allow the output to be referenced to an external DC level. This pin may be used for offset correction or level shifting as required. In the 8-pin package, sense is internally connected to the output.

For an instrumentation amplifier with the highest precision, consult the AMP-01 data sheet. For the highest input impedance and speed, consult the AMP-05 data sheet.

PIN CONNECTIONS

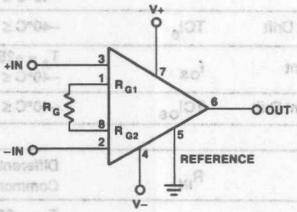


EPOXY MINI-DIP
(P-Suffix)



16-PIN SOL
(S-Suffix)

BASIC CIRCUIT CONNECTIONS



$$G = \frac{V_{OUT}}{(+IN) - (-IN)} = \left(\frac{50k\Omega}{R_G}\right) + 1$$

FOR SOL CONNECT SENSE TO OUTPUT

10

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AMP02

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Common-Mode Input Voltage ..... [(V–) – 60V] to [(V+) + 60V]
Differential Input Voltage ..... [(V–) – 60V] to [(V+) + 60V]
Output Short-Circuit Duration ..... Continuous
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	96	37	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTE:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-02E MIN	AMP-02E TYP	AMP-02E MAX	AMP-02F MIN	AMP-02F TYP	AMP-02F MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	T_A = +25°C	–	20	100	–	40	200	µV
		–40°C ≤ T_A ≤ +85°C	–	50	200	–	100	350	
Input Offset Voltage Drift	TCV_{IOS}	–40°C ≤ T_A ≤ +85°C	–	0.5	2	–	1	4	µV/°C
Output Offset Voltage	V_{OOS}	T_A = +25°C	–	1	4	–	2	8	mV
		–40°C ≤ T_A ≤ +85°C	–	4	10	–	9	20	
Output Offset Voltage Drift	TCV_{OOS}	–40°C ≤ T_A ≤ +85°C	–	50	100	–	100	200	µV/°C
Power Supply Rejection	PSR	V_S = ±4.8V to ±18V							
		G = 1000	115	128	–	110	115	–	dB
		G = 100	115	125	–	110	115	–	
		G = 10	100	110	–	95	100	–	
		G = 1	80	90	–	75	80	–	
		V_S = ±4.8V to ±18V, –40°C ≤ T_A ≤ +85°C							
		G = 1000	110	120	–	105	110	–	dB
		G = 100	110	120	–	105	110	–	
		G = 10	95	110	–	90	95	–	
		G = 1	75	90	–	70	75	–	
INPUT CURRENT									
Input Bias Current	I_B	T_A = +25°C	–	2	10	–	4	20	nA
		–40°C ≤ T_A ≤ +85°C	–	12	30	–	20	40	
Input Bias Current Drift	TCI_B	–40°C ≤ T_A +85°C	–	150	–	–	250	–	pA/°C
Input Offset Current	I_{OS}	T_A = +25°C	–	1.2	5	–	2	10	nA
		–40°C ≤ T_A ≤ +85°C	–	1.8	15	–	3	20	
Input Offset Current Drift	TCI_{OS}	–40°C ≤ T_A ≤ +85°C	–	9	–	–	15	–	pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G ≤ 1000	–	10	–	–	10	–	GΩ
		Common-Mode, G = 1000	–	16.5	–	–	16.5	–	
Input Voltage Range	IVR	T_A = +25°C (Note 3)	±11	–	–	±11	–	–	V
		–40°C ≤ T_A ≤ +85°C	±11	–	–	±11	–	–	
Common-Mode Rejection	CMR	V_{CM} = ±11V							
		G = 1000	115	120	–	110	115	–	dB
		G = 100	115	120	–	110	115	–	
		G = 10	100	115	–	95	110	–	
		G = 1	80	95	–	75	90	–	
		V_{CM} = ±11V, –40°C ≤ T_A ≤ +85°C							
		G = 1000	110	120	–	105	115	–	dB
		G = 100	110	120	–	105	115	–	
		G = 10	95	110	–	90	105	–	
		G = 1	75	90	–	70	85	–	

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted. *Continued*

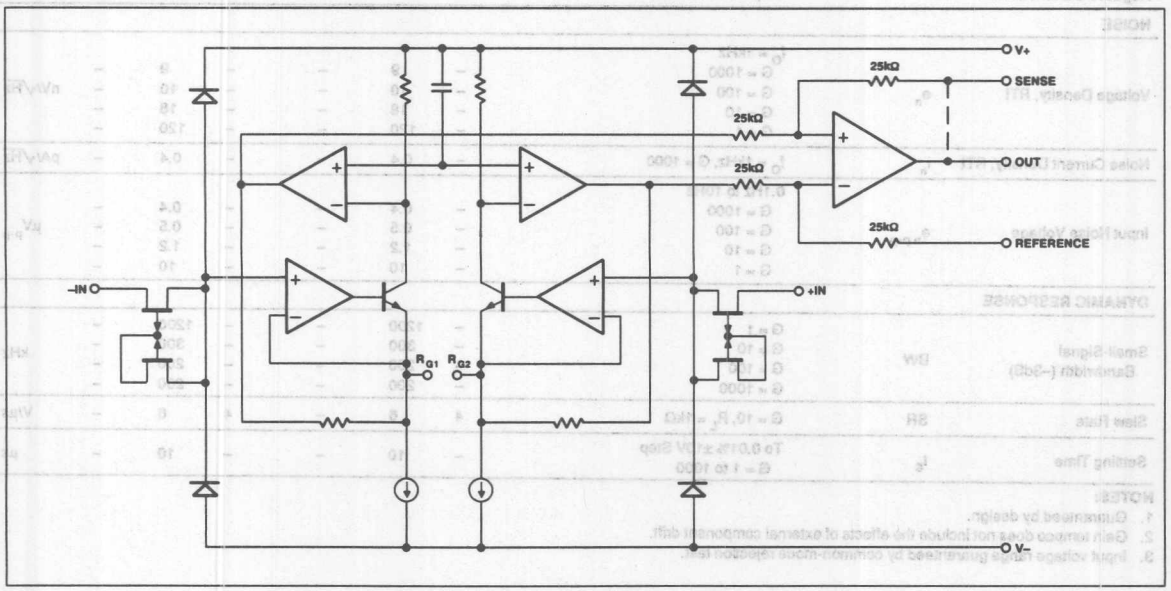
PARAMETER	SYMBOL	CONDITIONS	AMP-02E MIN	AMP-02E TYP	AMP-02E MAX	AMP-02F MIN	AMP-02F TYP	AMP-02F MAX	UNITS
GAIN									
Gain Equation Accuracy	$G = \frac{50k\Omega}{R_G} + 1$	G = 1000	–	–	0.50	–	–	0.70	%
		G = 100	–	–	0.30	–	–	0.50	
		G = 10	–	–	0.25	–	–	0.40	
		G = 1	–	–	0.02	–	–	0.05	
Gain Range	G		1	–	10k	1	–	10k	V/V
Nonlinearity		G = 1 to 1000	–	0.006	–	–	0.006	–	%
Temperature Coefficient	G_{TC}	$1 \le G \le 1000$ (Notes 1, 2)	–	20	50	–	20	50	ppm/°C
OUTPUT RATING									
Output Voltage Swing	V_{OUT}	$T_A = +25°C$, $R_L = 1k\Omega$	±12	±13	–	±12	±13	–	V
		$R_L = 1k\Omega$, $-40°C \le T_A \le +85°C$	±11	±12	–	±11	±12	–	
Positive Current Limit		Output-to-Ground Short	–	22	–	–	22	–	mA
Negative Current Limit		Output-to-Ground Short	–	32	–	–	32	–	mA
NOISE									
Voltage Density, RTI	e_n	f_O = 1kHz							nV/√Hz
		G = 1000	–	9	–	–	9	–	
		G = 100	–	10	–	–	10	–	
		G = 10	–	18	–	–	18	–	
		G = 1	–	120	–	–	120	–	
Noise Current Density, RTI	i_n	f_O = 1kHz, G = 1000	–	0.4	–	–	0.4	–	pA/√Hz
Input Noise Voltage	$e_{n\,p\text{-}p}$	0.1Hz to 10Hz							$\mu V_{p\text{-}p}$
		G = 1000	–	0.4	–	–	0.4	–	
		G = 100	–	0.5	–	–	0.5	–	
		G = 10	–	1.2	–	–	1.2	–	
		G = 1	–	10	–	–	10	–	
DYNAMIC RESPONSE									
Small-Signal Bandwidth (–3dB)	BW	G = 1	–	1200	–	–	1200	–	kHz
		G = 10	–	300	–	–	300	–	
		G = 100	–	200	–	–	200	–	
		G = 1000	–	200	–	–	200	–	
Slew Rate	SR	G = 10, $R_L = 1k\Omega$	4	6	–	4	6	–	V/µs
Settling Time	t_S	To 0.01% ±10V Step G = 1 to 1000	–	10	–	–	10	–	µs

NOTES:
1. Guaranteed by design.
2. Gain tempco does not include the effects of external component drift.
3. Input voltage range guaranteed by common-mode rejection test.

10

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
SENSE INPUT									
Input Resistance	R_{IN}		–	25	–	–	25	–	kΩ
Voltage Range			–	±11	–	–	±11	–	V
REFERENCE INPUT									
Input Resistance	R_{IN}		–	50	–	–	50	–	kΩ
Voltage Range			–	±11	–	–	±11	–	V
Gain to Output			–	1	–	–	1	–	V/V
POWER SUPPLY									
Supply Voltage Range	V_S		±4.5	–	±18	±4.5	–	±18	V
Supply Current	I_{SY}	T_A = +25°C −40°C ≤ T_A ≤ +85°C	– –	5 5	6 6	– –	5 5	6 6	mA

SIMPLIFIED SCHEMATIC



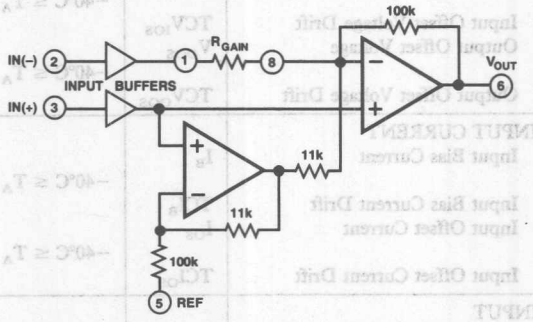
Precision Single Supply Instrumentation Amplifier

AMP04*

FEATURES
- Single Supply Operation
- Low Supply Current: 700 μA max
- Wide Gain Range: 1 to 1000
- Low Offset Voltage: 150 μV max
- Zero-In/Zero-Out
- Single-Resistor Gain Set
- 8-pin Mini-DIP and SO packages

APPLICATIONS
- Strain Gages
- Thermocouples
- RTDs
- Battery Powered Equipment
- Medical Instrumentation
- Data Acquisition Systems
- PC Based Instruments
- Portable Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AMP-04 is a single-supply instrumentation amplifier designed to work over a +5 volt to ±15 volt supply range. It offers an excellent combination of accuracy, low power consumption, wide input voltage range, and excellent gain performance.

Gain is set by a single external resistor and can be from 1 to 1000. Input common-mode voltage range allows the AMP-04 to handle signals with full accuracy from ground to within 1 volt of the positive supply. And the output can swing to within 1 volt of the positive supply. Gain bandwidth is over 700 kHz. In addition to being easy to use, the AMP-04 draws only 700 μA of supply current.

For high resolution data acquisition systems, laser trimming of low drift thin-film resistors limits the input offset voltage to under 150 μV, and allows the AMP-04 to offer gain nonlinearity of 0.005% and a gain tempco of 30 ppm/°C.

A proprietary input structure limits input offset currents to less than 5 nA with drift of only 8 pA/°C, allowing direct connection of the AMP-04 to high impedance transducers and other signal sources.

*Protected by U.S. Patent No. 5,075,633.

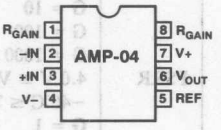
The AMP-04 is specified over the extended industrial (−40°C to +85°C) temperature range. AMP-04s are available in plastic and ceramic DIP plus SO-8 surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.

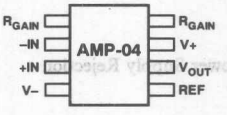
10

PIN CONNECTIONS

8-Lead Epoxy DIP (P Suffix)



8-Lead Narrow-Body SO (S Suffix)



AMP04—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = +5 V, V_{CM} = +2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	AMP-04E Min	AMP-04E Typ	AMP-04E Max	AMP-04F Min	AMP-04F Typ	AMP-04F Max	Units
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}			30	150			300	μV
		−40°C ≤ T_A ≤ +85°C			300			600	μV
Input Offset Voltage Drift	TCV_{IOS}				3			6	μV/°C
Output Offset Voltage	V_{OOS}			0.5	1.5			3	mV
		−40°C ≤ T_A ≤ +85°C			3			6	mV
Output Offset Voltage Drift	TCV_{OOS}				30			50	μV/°C
INPUT CURRENT									
Input Bias Current	I_B			22	30			40	nA
		−40°C ≤ T_A ≤ +85°C			50			60	nA
Input Bias Current Drift	TCI_B			65			65		pA/°C
Input Offset Current	I_{OS}			1	5			10	nA
		−40°C ≤ T_A ≤ +85°C			10			15	nA
Input Offset Current Drift	TCI_{OS}			8			8		pA/°C
INPUT									
Common-Mode Input Resistance				4			4		GΩ
Differential Input Resistance				4			4		GΩ
Input Voltage Range	V_{IN}		0		3.0	0		3.0	V
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 3.0 V							
		G = 1	60	80		55			dB
		G = 10	80	100		75			dB
		G = 100	90	105		80			dB
		G = 1000	90	105		80			dB
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 2.5 V							
		−40°C ≤ T_A ≤ +85°C							
		G = 1	55			50			dB
		G = 10	75			70			dB
		G = 100	85			75			dB
		G = 1000	85			75			dB
Power Supply Rejection	PSRR	4.0 V ≤ V_S ≤ 12 V							
		−40°C ≤ T_A ≤ +85°C							
		G = 1	95			85			dB
		G = 10	105			95			dB
		G = 100	105			95			dB
		G = 1000	105			95			dB
GAIN (G = 100 K/R_{GAIN})									
Gain Equation Accuracy		G = 1 to 100		0.2	0.5			0.75	%
		G = 1 to 100							
		−40°C ≤ T_A ≤+85°C			0.8			1.0	%
		G = 1000		0.4			0.75		%
Gain Range	G		1		1000	1		1000	V/V
Nonlinearity		G = 1, R_L = 5 kΩ		0.005					%
		G = 10, R_L = 5 kΩ		0.015					%
		G = 100, R_L = 5 kΩ		0.025					%
Gain Temperature Coefficient	ΔG/ΔT			30			50		ppm/°C
OUTPUT									
Output Voltage Swing High	V_{OH}	R_L = 2 kΩ	4.0	4.2		4.0			V
		R_L = 2 kΩ							
		−40°C ≤ T_A ≤ +85°C	3.8			3.8			V
Output Voltage Swing Low	V_{OL}	R_L = 2 kΩ							
		−40°C ≤ T_A ≤ +85°C			2.0			2.5	mV
Output Current Limit		Sink		30			30		mA
		Source		15			15		mA

Parameter	Symbol	Conditions	AMP-04E Min	AMP-04E Typ	AMP-04E Max	AMP-04F Min	AMP-04F Typ	AMP-04F Max	Units
NOISE									
Noise Voltage Density, RTI	e_N	f = 1 kHz, G = 1		270			270		nV/$\sqrt{Hz}$
		f = 1 kHz, G = 10		45			45		nV/$\sqrt{Hz}$
		f = 100 Hz, G = 100		30			30		nV/$\sqrt{Hz}$
		f = 100 Hz, G = 1000		25			25		nV/$\sqrt{Hz}$
Noise Current Density, RTI	i_N	f = 100 Hz, G = 100		4			4		pA/$\sqrt{Hz}$
Input Noise Voltage	e_N p-p	0.1 to 10 Hz, G = 1		7			7		µV p-p
		0.1 to 10 Hz, G = 10		1.5			1.5		µV p-p
		0.1 to 10 Hz, G = 100		0.7			0.7		µV p-p
DYNAMIC RESPONSE									
Small Signal Bandwidth	BW	G = 1, −3 dB		300			300		kHz
POWER SUPPLY									
Supply Current	I_{SY}			550	700			700	µA
		−40°C ≤ T_A ≤ +85°C			850			850	µA

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (V_S = ±15 V, V_{CM} = 0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	AMP-04E Min	AMP-04E Typ	AMP-04E Max	AMP-04F Min	AMP-04F Typ	AMP-04F Max	Units
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}			80	400			600	µV
		−40°C ≤ T_A ≤ +85°C			600			900	µV
Input Offset Voltage Drift	TCV_{IOS}				3			6	µV/°C
Output Offset Voltage	V_{OOS}			1	3			6	mV
		−40°C ≤ T_A ≤ +85°C			6			9	mV
Output Offset Voltage Drift	TCV_{OOS}				30			50	µV/°C
INPUT CURRENT									
Input Bias Current	I_B			17	30			40	nA
		−40°C ≤ T_A ≤ +85°C			50			60	nA
Input Bias Current Drift	TCI_B			65			65		pA/°C
Input Offset Current	I_{OS}			2	5			10	nA
		−40°C ≤ T_A ≤ +85°C			15			20	nA
Input Offset Current Drift	TCI_{OS}			28			28		pA/°C
INPUT									
Common-Mode Input Resistance				4					GΩ
Differential-Mode Input Resistance				4					GΩ
Input Voltage Range	V_{IN}		−12		+12	−12		+12	V
Common-Mode Rejection	CMR	−12 V ≤ V_{CM} ≤ +12 V							
		G = 1	60	80		55			dB
		G = 10	80	100		75			dB
		G = 100	90	105		80			dB
		G = 1000	90	105		80			dB
	CMR	−11 V ≤ V_{CM} ≤ +11 V −40°C ≤ T_A ≤ +85°C							
		G = 1	55			50			dB
		G = 10	75			70			dB
		G = 100	85			75			dB
		G = 1000	85			75			dB
Power Supply Rejection	PSRR	±2.5 V ≤ V_S ≤ ±18 V −40°C ≤ T_A ≤ +85°C							
		G = 1	75			70			dB
		G = 10	90			80			dB
		G = 100	95			85			dB
		G = 1000	95			85			dB

Parameter	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Units
GAIN (G = 100 K/R_{GAIN})									
Gain Equation Accuracy		G = 1 to 100		0.2	0.5			0.75	%
		G = 1000		0.4			0.75		%
		G = 1 to 100							
		−40°C ≤ T_A ≤ +85°C			0.8			1.0	%
Gain Range	G		1		1000	1		1000	V/V
Nonlinearity		G = 1, R_L = 5 kΩ		0.005			0.005		%
		G = 10, R_L = 5 kΩ		0.015			0.015		%
		G = 100, R_L = 5 kΩ		0.025			0.025		%
Gain Temperature Coefficient	ΔG/ΔT			30			50		ppm/°C
OUTPUT									
Output Voltage Swing High	V_{OH}	R_L = 2 kΩ	+13	+13.4		+13			V
		R_L = 2 kΩ							
		−40°C ≤ T_A ≤ +85°C	+12.5			+12.5			V
Output Voltage Swing Low	V_{OL}	R_L = 2 kΩ							
		−40°C ≤ T_A ≤ +85°C			−14.5			−14.5	V
Output Current Limit		Sink		30			30		mA
		Source		15			15		mA
NOISE									
Noise Voltage Density, RTI	e_N	f = 1 kHz, G = 1		270			270		nV/√Hz
		f = 1 kHz, G = 10		45			45		nV/√Hz
		f = 100 Hz, G = 100		30			30		nV/√Hz
		f = 100 Hz, G = 1000		25			25		nV/√Hz
Noise Current Density, RTI	i_N	f = 100 Hz, G = 100		4			4		pA/√Hz
Input Noise Voltage	e_N p-p	0.1 to 10 Hz, G = 1		5			5		μV p-p
	e_N p-p	0.1 to 10 Hz, G = 10		1			1		μV p-p
	e_N p-p	0.1 to 10 Hz, G = 100		0.5			0.5		μV p-p
DYNAMIC RESPONSE									
Small Signal Bandwidth	BW	G = 1, −3 dB		700			700		kHz
POWER SUPPLY									
Supply Current	I_{SY}			750	900			900	μA
	I_{SY}	−40°C ≤ T_A ≤ +85°C			1100			1100	μA

Specifications subject to change without notice.

WAFER TEST LIMITS (V_S = +5 V, V_{CM} = +2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
OFFSET VOLTAGE				
Input Offset Voltage	V_{IOS}		300	μV max
Output Offset Voltage	V_{OOS}		3	mV max
INPUT CURRENT				
Input Bias Current	I_B		40	nA max
Input Offset Current	I_{OS}		10	nA max
INPUT				
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 3.0 V		
		G = 1	55	dB min
		G = 10	75	dB min
		G = 100	80	dB min
		G = 1000	80	dB min
Common-Mode Rejection	CMR	V_S = ±15 V, −12 V ≤ V_{CM} ≤ +12 V		
		G = 1	55	dB min
		G = 10	75	dB min
		G = 100	80	dB min

Parameter	Symbol	Conditions	Limit	Units
Power Supply Rejection	PSRR	G = 1000 4.0 V ≤ V_S ≤ 12 V	80	dB min
		G = 1	85	dB min
		G = 10	95	dB min
		G = 100	95	dB min
		G = 1000	95	dB min
GAIN (G = 100 K/R_{GAIN})				
Gain Equation Accuracy		G = 1 to 100	0.75	% max
OUTPUT				
Output Voltage Swing High	V_{OH}	R_L = 2 kΩ	4.0	V min
Output Voltage Swing Low	V_{OL}	R_L = 2 kΩ	2.5	mV max
POWER SUPPLY				
Supply Current	I_{SY}	V_S = ±15	900	μA max
			700	μA max

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

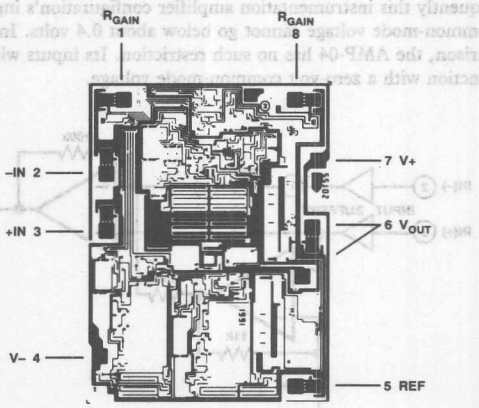
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Common-Mode Input Voltage[2] . . . . . ±18 V
Differential Input Voltage . . . . . 36 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
Z Package . . . . . −65°C to +175°C
P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
AMP-04A . . . . . −55°C to +125°C
AMP-04E, F . . . . . −40°C to +85°C
Junction Temperature Range
Z Package . . . . . −65°C to +175°C
P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

DICE CHARACTERISTICS



AMP-04 Die Size 0.075 × 0.99 inch, 7,425 sq. mils.
Substrate (Die Backside) Is Connected to V+.
Transistor Count, 81.

ORDERING GUIDE

Model	Temperature Range	V_{OS} @ +5 V T_A = +25°C	Package Description	Package Option[1]
AMP04EP	XIND	150 μV	Plastic DIP	N-8
AMP04FP	XIND	300 μV	Plastic DIP	N-8
AMP04FS	XIND	300 μV	SOIC	SO-8
AMP04AZ	MIL	Note 2	Cerdip	Q-8
AMP04GBC	+25°C	300 μV		

NOTES
[1]For outline information see Package Information section.
[2]Consult MIL-STD-883 data sheet.

APPLICATIONS

Common-Mode Rejection

The purpose of the instrumentation amplifier is to amplify the difference between the two input signals while ignoring offset and noise voltages common to both inputs. One way of judging the device's ability to reject this offset is the common-mode gain, which is the ratio between a change in the common-mode voltage and the resulting output voltage change. Instrumentation amplifiers are often judged by the common-mode rejection ratio, which is equal to 20 × $\log_{10}$ of the ratio of the user-selected differential signal gain to the common-mode gain, commonly called the CMRR. The AMP-04 offers excellent CMRR, guaranteed to be greater than 90 dB at gains of 100 or greater. Input offsets attain very low temperature drift by proprietary laser-trimmed thin-film resistors and high gain amplifiers.

Input Common-Mode Range Includes Ground

The AMP-04 employs a patented topology (Figure 1) that uniquely allows the common-mode input voltage to truly extend to zero volts where other instrumentation amplifiers fail. To illustrate, take for example the single supply, gain of 100 instrumentation amplifier as in Figure 2. As the inputs approach zero volts, in order for the output to go positive, amplifier A's output (V_{OA}) must be allowed to go below ground, to −0.094 volts. Clearly this is not possible in a single supply environment. Consequently this instrumentation amplifier configuration's input common-mode voltage cannot go below about 0.4 volts. In comparison, the AMP-04 has no such restriction. Its inputs will function with a zero-volt common-mode voltage.

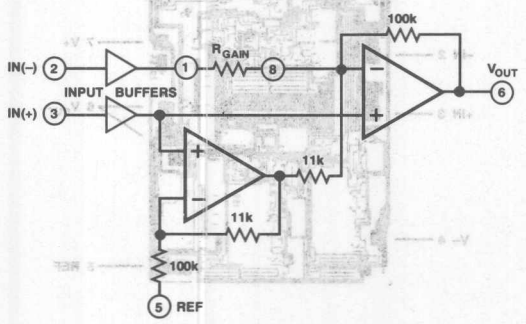


Figure 1. Functional Block Diagram

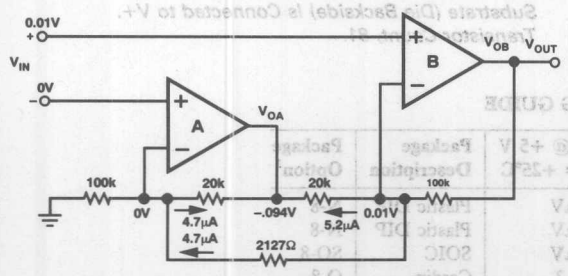


Figure 2. Gain = 100 Instrumentation Amplifier

Input Common-Mode Voltage Below Ground

Although not tested and guaranteed, the AMP-04 inputs are biased in a way that they can amplify signals linearly with common-mode voltage as low as −0.25 volts below ground. This holds true over the industrial temperature range from −40°C to +85°C.

Extended Positive Common-Mode Range

On the high side, other instrumentation amplifier configurations, such as the three op amp instrumentation amplifier, can have severe positive common-mode range limitations. Figure 3 shows an example of a gain of 1001 amplifier, with an input common-mode voltage of 10 volts. For this circuit to function, V_{OB} must swing to 15.01 volts in order for the output to go to 10.01 volts. Clearly no op amp can handle this swing range (given a +15 V supply) as the output will saturate long before it reaches the supply rails. Again the AMP-04's topology does not have this limitation. Figure 4 illustrates the AMP-04 operating at the same common-mode conditions as in Figure 3. None of the internal nodes has a signal high enough to cause amplifier saturation. As a result, the AMP-04 can accommodate much wider common-mode range than most instrumentation amplifiers.

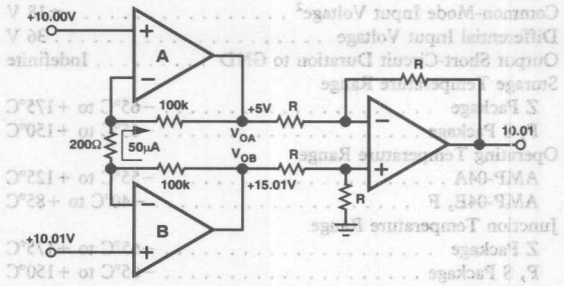


Figure 3. Gain = 1001, Three Op Amp Instrumentation Amplifier

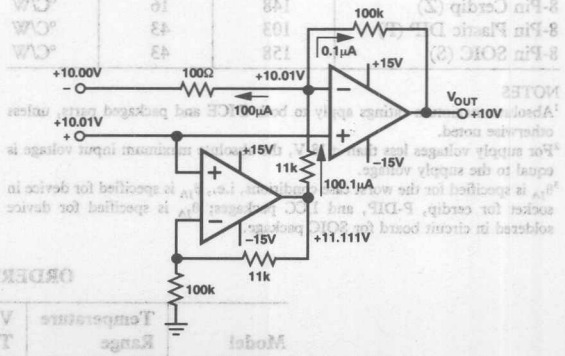


Figure 4. Gain = 1000, AMP-04

Programming the Gain

The gain of the AMP-04 is programmed by the user by selecting a single external resistor—R_{GAIN}:

$$Gain = 100\ k\Omega/R_{GAIN}$$

The output voltage is then defined as the differential input voltage times the gain.

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \text{Gain}$$

In single supply systems, offsetting the ground is often desired for several reasons. Ground may be offset from zero to provide a quieter signal reference point, or to offset "zero" to allow a unipolar signal range to represent both positive and negative values.

In noisy environments such as those having digital switching, switching power supplies or externally generated noise, ground may not be the ideal place to reference a signal in a high accuracy system.

Often, real world signals such as temperature or pressure may generate voltages that are represented by changes in polarity. In a single supply system the signal input cannot be allowed to go below ground, and therefore the signal must be offset to accommodate this change in polarity. On the AMP-04, a reference input pin is provided to allow offsetting of the input range.

The gain equation is more accurately represented by including this reference input.

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times Gain + V_{REF}$$

Grounding

The most common problems encountered in high performance analog instrumentation and data acquisition system designs are found in the management of offset errors and ground noise. Primarily, the designer must consider temperature differentials and thermocouple effects due to dissimilar metals, IR voltage drops, and the effects of stray capacitance. The problem is greatly compounded when high speed digital circuitry, such as that accompanying data conversion components, is brought into the proximity of the analog section. Considerable noise and error contributions such as fast-moving logic signals that easily propagate into sensitive analog lines, and the unavoidable noise common to digital supply lines must all be dealt with if the accuracy of the carefully designed analog section is to be preserved.

Besides the temperature drift errors encountered in the amplifier, thermal errors due to the supporting discrete components should be evaluated. The use of high quality, low-TC components where appropriate is encouraged. What is more important, large thermal gradients can create not only unexpected changes in component values, but also generate significant thermoelectric voltages due to the interface between dissimilar metals such as lead solder, copper wire, gold socket contacts, Kovar lead frames, etc. Thermocouple voltages developed at these junctions commonly exceed the TCV_{OS} contribution of the AMP-04. Component layout that takes into account the power dissipation at critical locations in the circuit and minimizes gradient effects and differential common-mode voltages by taking advantage of input symmetry will minimize many of these errors.

High accuracy circuitry can experience considerable error contributions due to the coupling of stray voltages into sensitive areas, including high impedance amplifier inputs which benefit from such techniques as ground planes, guard rings, and shields. Careful circuit layout, including good grounding and signal routing practice to minimize stray coupling and ground loops is recommended. Leakage currents can be minimized by using high quality socket and circuit board materials, and by carefully cleaning and coating complete board assemblies.

As mentioned above, the high speed transition noise found in logic circuitry is the sworn enemy of the analog circuit designer. Great care must be taken to maintain separation between them to minimize coupling. A major path for these error voltages will be found in the power supply lines. Low impedance, load related variations and noise levels that are completely acceptable in the high thresholds of the digital domain make the digital supply unusable in nearly all high performance analog applications. The user is encouraged to maintain separate power and ground between the analog and digital systems wherever possible, joining only at the supply itself if necessary, and to observe careful grounding layout and bypass capacitor scheduling in sensitive areas.

Input Shield Drivers

High impedance sources and long cable runs from remote transducers in noisy industrial environments commonly experience significant amounts of noise coupled to the inputs. Both stray capacitance errors and noise coupling from external sources can be minimized by running the input signal through shielded cable. The cable shield is often grounded at the analog input common, however improved dynamic noise rejection and a reduction in effective cable capacitance is achieved by driving the shield with a buffer amplifier at a potential equal to the voltage seen at the input. Driven shields are easily realized with the AMP-04. Examination of the simplified schematic shows that the potentials at the gain set resistor pins of the AMP-04 follow the inputs precisely. As shown in Figure 5, shield drivers are easily realized by buffering the potential at these pins by a dual, single supply op amp such as the OP-213. Alternatively, applications with single-ended sources or that use twisted-pair cable could drive a single shield. To minimize error contributions due to this additional circuitry, all components and wiring should remain in proximity to the AMP-04 and careful grounding and bypassing techniques should be observed.

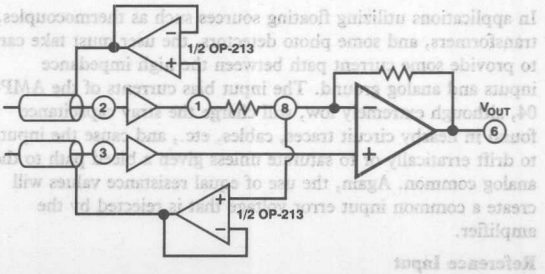


Figure 5. Cable Shield Drivers

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To achieve optimal performance, the user needs to take into account a number of error sources found in instrumentation amplifiers. These consist primarily of input and output offset voltages and leakage currents.

The input and output offset voltages are independent from one another, and must be considered separately. The input offset component will of course be directly multiplied by the gain of the amplifier, in contrast to the output offset voltage that is independent of gain. Therefore, the output error is the dominant factor at low gains, and the input error grows to become the greater problem as gain is increased. The overall equation for offset voltage error referred to the output (RTO) is:

$$V_{OS}\,(RTO) = (V_{IOS} \times G) + V_{OOS}$$

where V_{IOS} is the input offset voltage and V_{OOS} the output offset voltage, and G is the programmed amplifier gain.

The change in these error voltages with temperature must also be taken into account. The specification TCV_{OS}, referred to the output, is a combination of the input and output drift specifications. Again, the gain influences the input error but not the output, and the equation is:

$$TCV_{OS}\,(RTO) = (TCV_{IOS} \times G) + TCV_{OOS}$$

In some applications the user may wish to define the error contribution as referred to the input, and treat it as an input error. The relationship is:

$$TCV_{OS}\,(RTI) = TCV_{IOS} + (TCV_{OOS} / G)$$

The bias and offset currents of the input transistors also have an impact on the overall accuracy of the input signal. The input leakage, or bias currents of both inputs will generate an additional offset voltage when flowing through the signal source resistance. Changes in this error component due to variations with signal voltage and temperature can be minimized if both input source resistances are equal, reducing the error to a common-mode voltage which can be rejected. The difference in bias current between the inputs, the offset current, generates a differential error voltage across the source resistance that should be taken into account in the user's design.

In applications utilizing floating sources such as thermocouples, transformers, and some photo detectors, the user must take care to provide some current path between the high impedance inputs and analog ground. The input bias currents of the AMP-04, although extremely low, will charge the stray capacitance found in nearby circuit traces, cables, etc., and cause the input to drift erratically or to saturate unless given a bleed path to the analog common. Again, the use of equal resistance values will create a common input error voltage that is rejected by the amplifier.

Reference Input

The V_{REF} input is used to set the system ground. For dual supply operation it can be connected to ground to give zero volts out with zero volts differential input. In single supply systems it could be connected either to the negative supply or to a pseudo-ground between the supplies. In any case, the REF input must be driven with low impedance.

Noise Filtering

Unlike most previous instrumentation amplifiers, the output stage's inverting input (Pin 8) is accessible. By placing a capacitor across the AMP-04's feedback path (Figure 6, Pins 6 and 8)

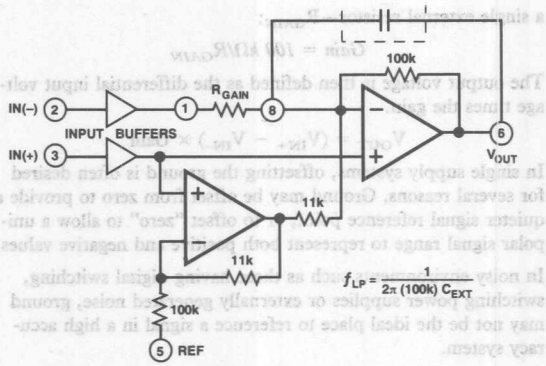


Figure 6. Noise Band Limiting

a single-pole low-pass filter is produced. The cutoff frequency (f_{LP}) follows the relationship:

$$f_{LP} = \frac{1}{2\pi\,(100\ k\Omega)\,C_{ext}}$$

Filtering can be applied to reduce wide band noise. Figure 7a shows a 10 Hz low-pass filter, gain of 1000 for the AMP-04. Figures 7b and 7c illustrate the effect of filtering on noise. The photo in Figure 7b shows the output noise before filtering. By adding a 0.15 μF capacitor, the noise is reduced by about a factor of 4 as shown in Figure 7c.

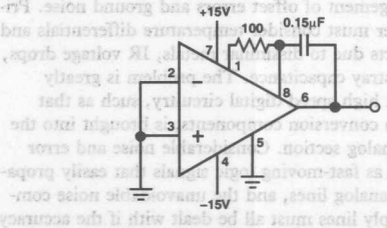


Figure 7a. 10 Hz Low-Pass Filter

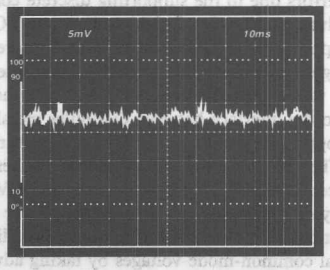


Figure 7b. Unfiltered AMP-04 Output

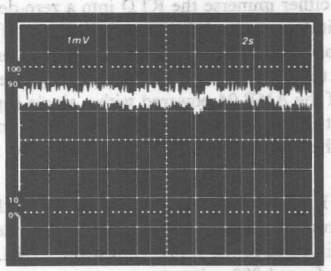


Figure 7c. 10 Hz Low-Pass Filtered Output

Power Supply Considerations

In dual supply applications (for example ±15 V) if the input is connected to a low resistance source less than 100 Ω, a large current may flow in the input leads if the positive supply is applied before the negative supply during power-up. A similar condition may also result upon a loss of the negative supply. If these conditions could be present in you system, it is recommended that a series resistor up to 1 kΩ be added to the input leads to limit the input current.

This condition can not occur in a single supply environment as losing the negative supply effectively removes any current return path.

Offset Nulling in Dual Supply

Offset may be nulled by feeding a correcting voltage at the V_{REF} pin (Pin 5). However, it is important that the pin be driven with a low impedance source. Any measurable resistance will degrade the amplifier's common-mode rejection performance as well as its gain accuracy. An op amp may be used to buffer the offset null circuit as in Figure 8.

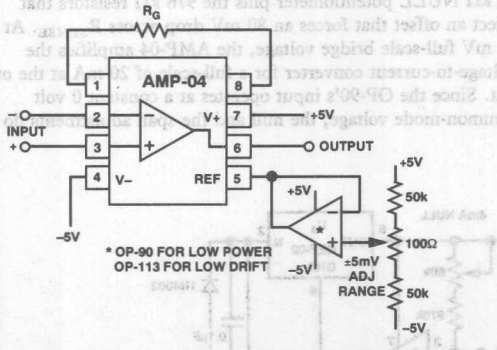


Figure 8. Offset Adjust for Dual Supply Applications

Offset Nulling in Single Supply

Nulling the offset in single supply systems is difficult because the adjustment is made to try to attain zero volts. At zero volts out, the output is in saturation (to the negative rail) and the output voltage is indistinguishable from the normal offset error. Consequently the offset nulling circuit in Figure 9 must be used with caution.

First, the potentiometer should be adjusted to cause the output to swing in the positive direction; then adjust it in the reverse direction, causing the output to swing toward ground, until the output just stops changing. At that point the output is at the saturation limit.

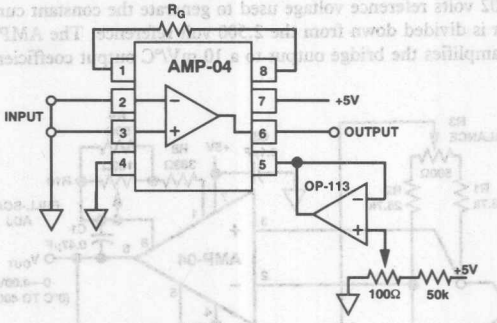


Figure 9. Offset Adjust for Single Supply Applications

Alternative Nulling Method

An alternative null correction technique is to inject an offset current into the summing node of the output amplifier as in Figure 10. This method does not require an external op amp. However the drawback is that the amplifier will move off its null as the input common-mode voltage changes. It is a less desirable nulling circuit than the previous method.

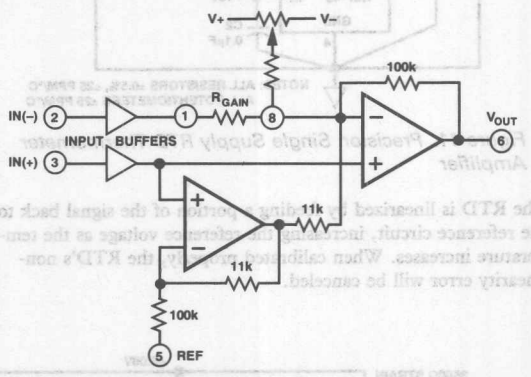


Figure 10. Current Injection Offsetting Is Not Recommended

APPLICATION CIRCUITS

Low Power Precision Single Supply RTD Amplifier

Figure 11 shows a linearized RTD amplifier that is powered off a single +5 volt supply. However, the circuit will work up to 36 volts without modification. The RTD is excited by a 100 μA constant current that is regulated by amplifier A (OP-295). The 0.202 volts reference voltage used to generate the constant current is divided down from the 2.500 volt reference. The AMP-04 amplifies the bridge output to a 10 mV/°C output coefficient.

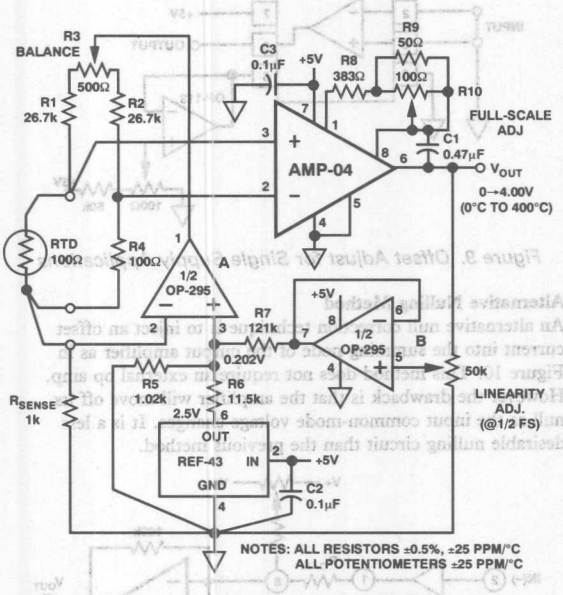


Figure 11. Precision Single Supply RTD Thermometer Amplifier

The RTD is linearized by feeding a portion of the signal back to the reference circuit, increasing the reference voltage as the temperature increases. When calibrated properly, the RTD's nonlinearity error will be canceled.

To calibrate, either immerse the RTD into a zero-degree ice bath or substitute an exact 100 Ω resistor in place of the RTD. Then adjust bridge BALANCE potentiometer R3 for a 0 volt output. Note that a 0 volt output is also the negative output swing limit of the AMP-04 powered with a single supply. Therefore, be sure to adjust R3 to first cause the output to swing positive and then back off until the output just stop swinging negatively.

Next, set the LINEARITY ADJ. potentiometer to the mid-range. Substitute an exact 247.04 Ω resistor (equivalent to 400°C temperature) in place of the RTD. Adjust the FULL-SCALE potentiometer for a 4.000 volts output.

Finally substitute a 175.84 Ω resistor (equivalent to 200°C temperature), and adjust the LINEARITY ADJ potentiometer for a 2.000 volts at the output. Repeat the full-scale and the half-scale adjustments as needed.

When properly calibrated, the circuit achieves better than ±0.5°C accuracy within a temperature measurement range from 0°C to 400°C.

Precision 4–20mA Loop Transmitter With Noninteractive Trim

Figure 12 shows a full bridge strain gage transducer amplifier circuit that is powered off the 4–20 mA current loop. The AMP-04 amplifies the bridge signal differentially and is converted to a current by the output amplifier. The total quiescent current drawn by the circuit, which includes the bridge, the amplifiers, and the resistor biasing, is only a fraction of the 4 mA null current that flows through the current-sense resistor R_{SENSE}. The voltage across R_{SENSE} feeds back to the OP-90's input, whose common-mode is fixed at the current summing reference voltage, thus regulating the output current.

With no bridge signal, the 4 mA null is simply set up by the 50 kΩ NULL potentiometer plus the 976 kΩ resistors that inject an offset that forces an 80 mV drop across R_{SENSE}. At a 50 mV full-scale bridge voltage, the AMP-04 amplifies the voltage-to-current converter for a full-scale of 20 mA at the output. Since the OP-90's input operates at a constant 0 volt common-mode voltage, the null and the span adjustments do

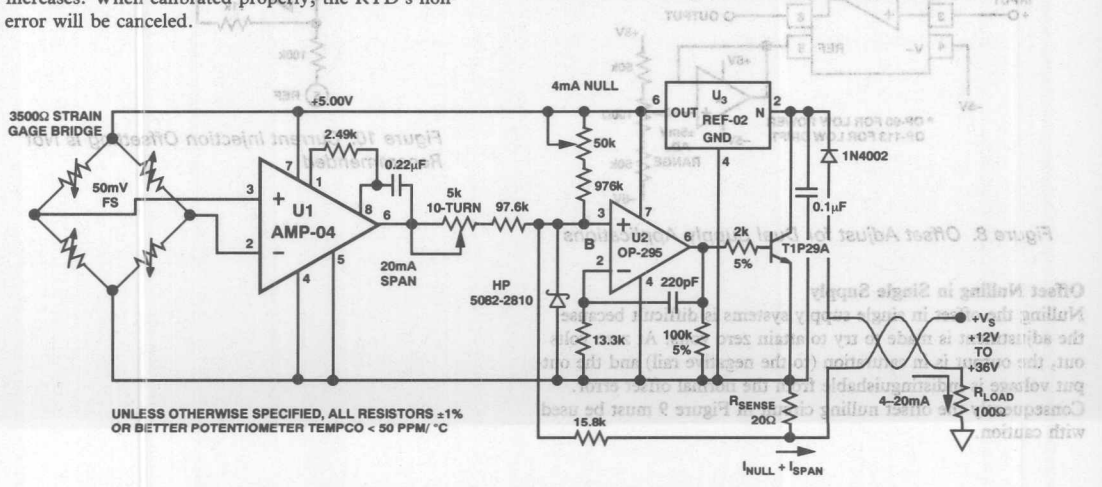


Figure 12. Precision 4–20 mA Loop Transmitter Features Noninteractive Trims

not interact with one another. Calibration is simple and easy with the NULL adjusted first, followed by SPAN adjust. The entire circuit can be remotely placed, and powered from the 4–20 mA 2-wire loop.

4–20 mA Loop Receiver

At the receiving end of a 4–20 mA loop, the AMP-04 makes a convenient differential receiver to convert the current back to a usable voltage (Figure 13). The 4–20 mA signal current passes through a 100 Ω sense resistor. The voltage drop is differentially amplified by the AMP-04. The 4 mA offset is removed by the offset correction circuit.

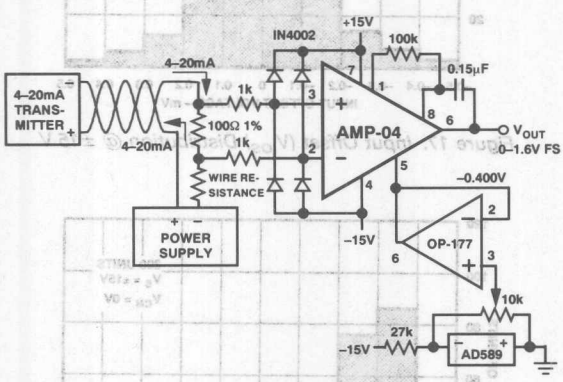


Figure 13. 4 to 20 mA Line Receiver

Low Power, Pulsed Load-Cell Amplifier

Figure 14 shows a 350 Ω load cell that is pulsed with a low duty cycle to conserve power. The OP-295's rail-to-rail output capability allows a maximum voltage of 10 volts to be applied to the bridge. The bridge voltage is selectively pulsed on when a measurement is made. A negative-going pulse lasting 200 ms should be applied to the MEASURE input. The long pulse width is necessary to allow ample settling time for the long time constant of the low-pass filter around the AMP-04. A much faster settling time can be achieved by omitting the filter capacitor.

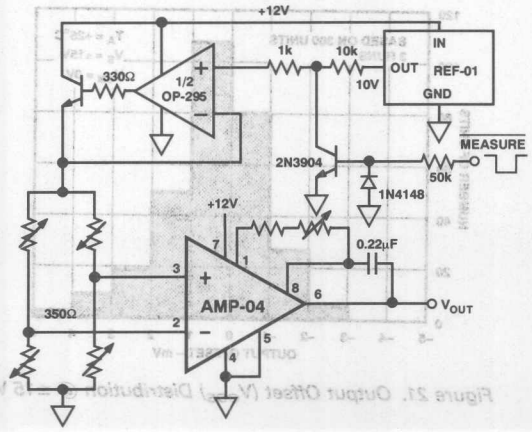


Figure 14. Pulsed Load Cell Bridge Amplifier

Single Supply Programmable Gain Instrumentation Amplifier

Combining with the single supply ADG221 quad analog switch, the AMP-04 makes a useful programmable gain amplifier that can handle input and output signals at zero volts. Figure 15 shows the implementation. A logic low input to any of the gain control ports will cause the gain to change by shorting a gain-set resistor across AMP-04's Pins 1 and 8. Trimming is required at higher gains to improve accuracy because the switch ON-resistance becomes a more significant part of the gain-set resistance. The gain of 500 setting has two switches connected in parallel to reduce the switch resistance.

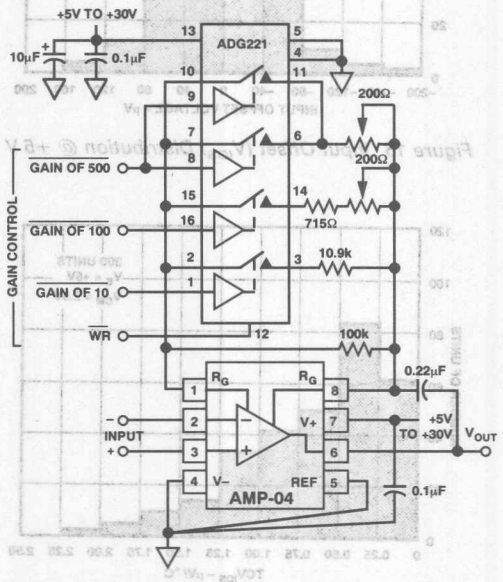
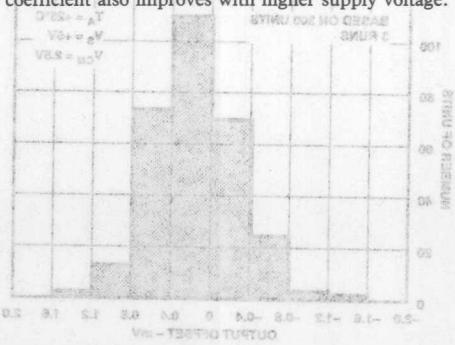


Figure 15. Single Supply Programmable Gain Instrumentation Amplifier

The switch ON resistance is lower if the supply voltage is 12 volts or higher. Additionally the overall amplifier's temperature coefficient also improves with higher supply voltage.



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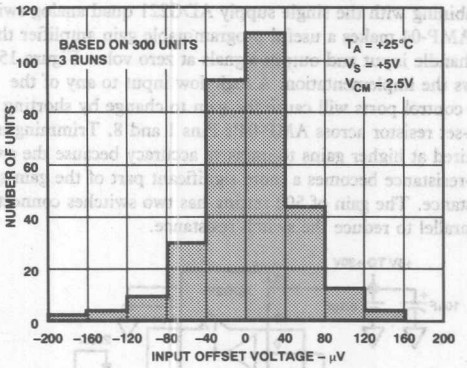


Figure 16. Input Offset (V_{IOS}) Distribution @ +5 V

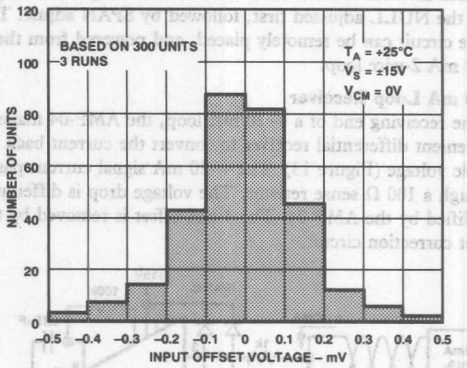


Figure 17. Input Offset (V_{IOS}) Distribution @ ±15 V

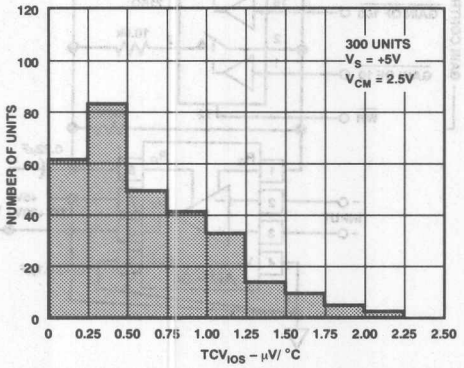


Figure 18. Input Offset Drift (TCV_{IOS}) Distribution @ +5 V

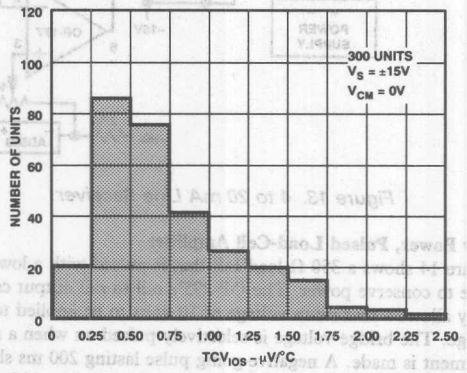


Figure 19. Input Offset Drift (TCV_{IOS}) Distribution @ ±15 V

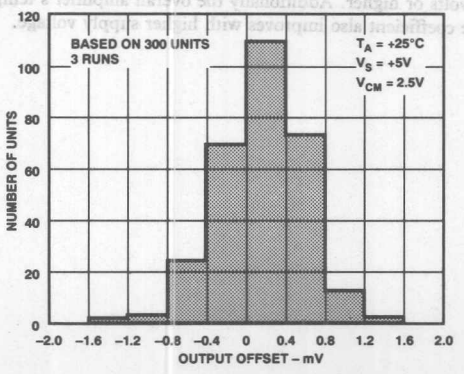


Figure 20. Output Offset (V_{OOS}) Distribution @ +5 V

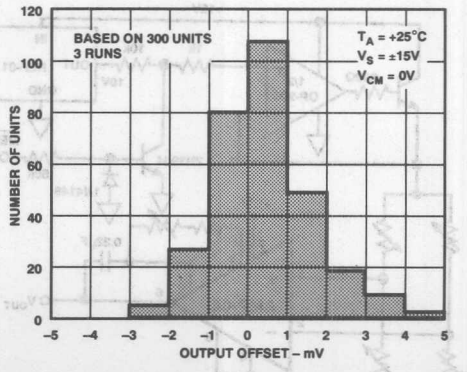


Figure 21. Output Offset (V_{OOS}) Distribution @ ±15 V

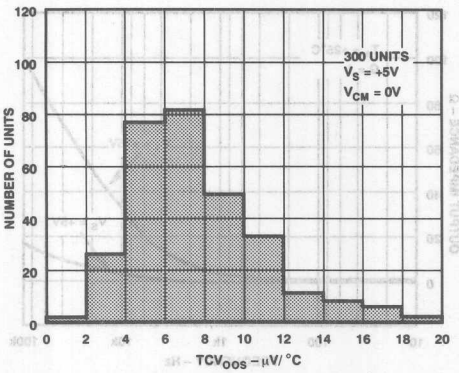


Figure 22. Output Offset Drift (TCV_{OOS}) Distribution @ +5 V

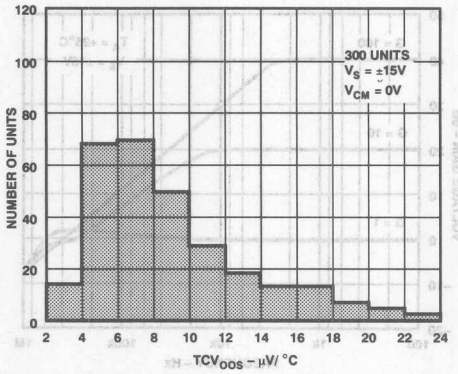


Figure 23. Output Offset Drift (TCV_{OOS}) Distribution @ ±15 V

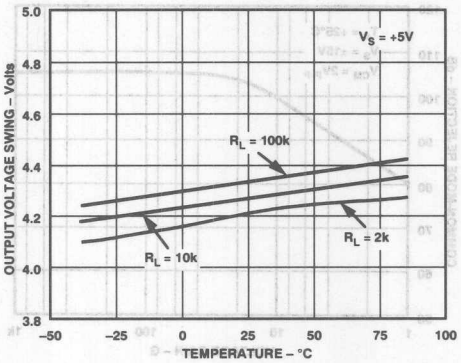


Figure 24. Output Voltage Swing vs. Temperature @ +5 V

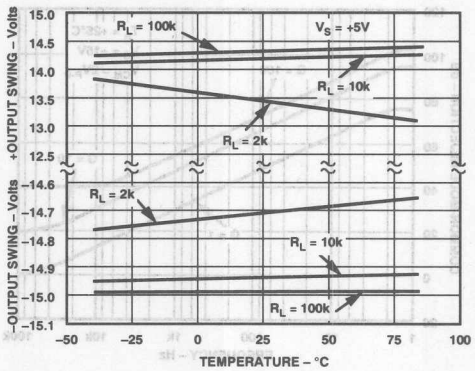


Figure 25. Output Voltage Swing vs. Temperature @ ±15 V

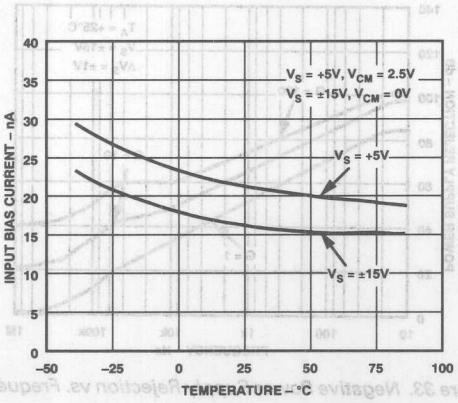


Figure 26. Input Bias Current vs. Temperature

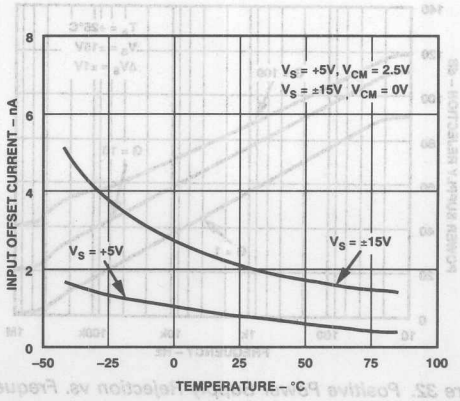


Figure 27. Input Offset Current vs. Temperature

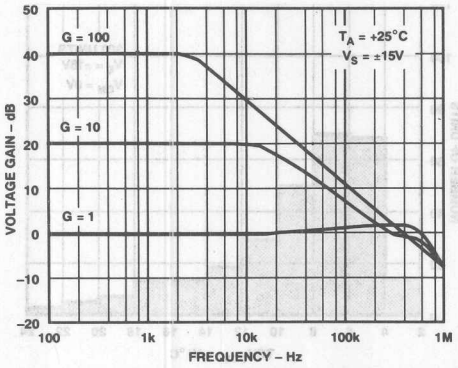


Figure 28. Closed-Loop Voltage Gain vs. Frequency

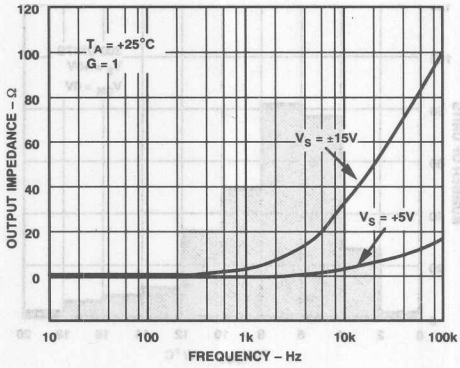


Figure 29. Closed-Loop Output Impedance vs. Frequency

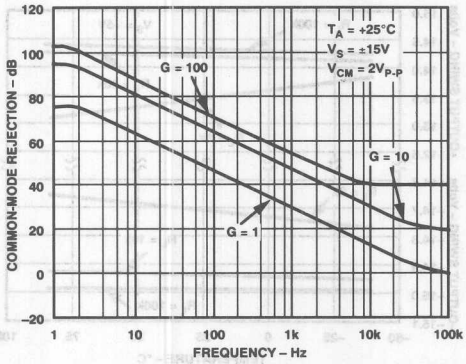


Figure 30. Common-Mode Rejection vs. Frequency

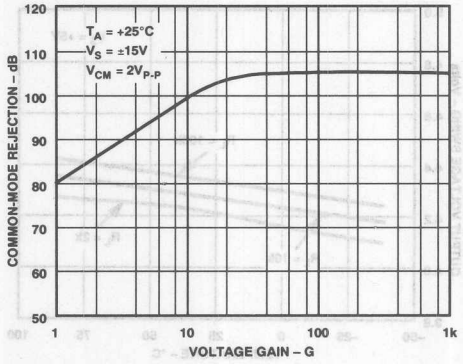


Figure 31. Common-Mode Rejection vs. Voltage Gain

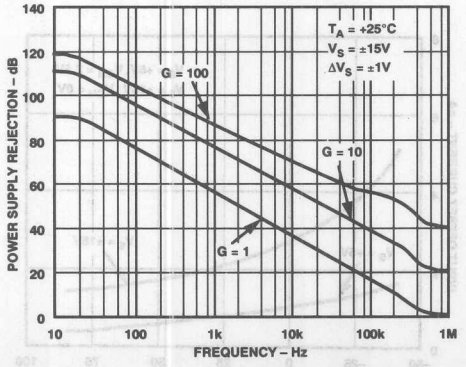


Figure 32. Positive Power Supply Rejection vs. Frequency

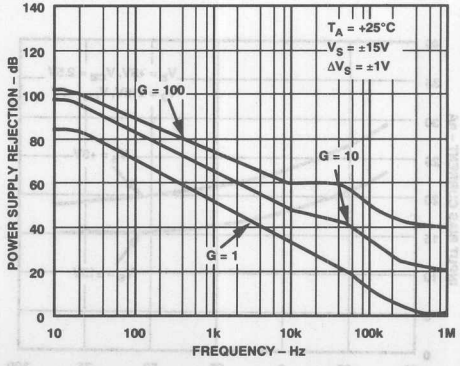


Figure 33. Negative Power Supply Rejection vs. Frequency

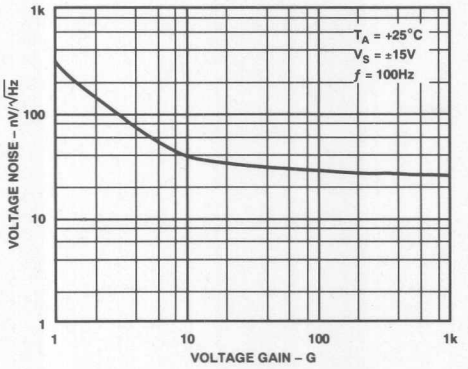


Figure 34. Voltage Noise Density vs. Gain

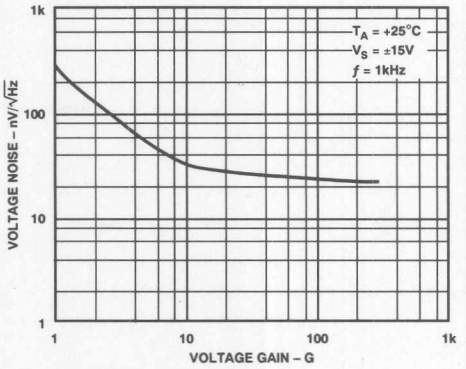


Figure 35. Voltage Noise Density vs. Gain, f = 1 kHz

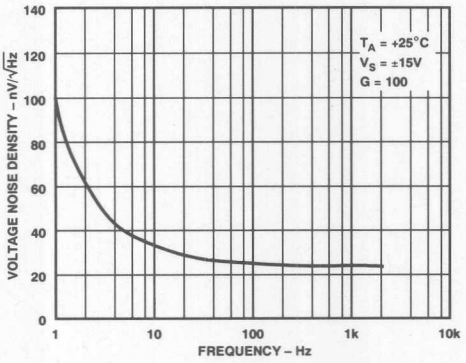
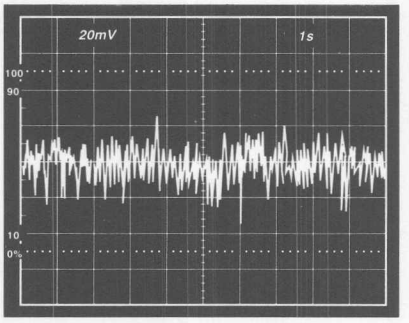


Figure 36. Voltage Noise Density vs. Frequency



V_S = ±15V, GAIN = 1000, 0.1 TO 10 Hz BANDPASS

Figure 37. Input Noise Voltage

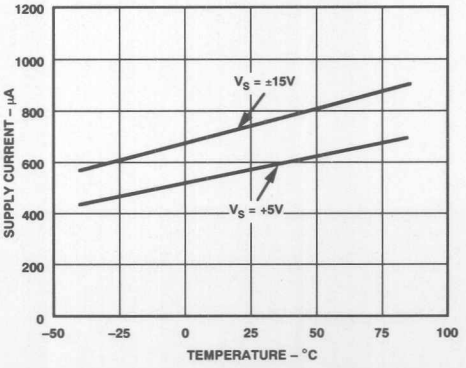


Figure 38. Supply Current vs. Temperature

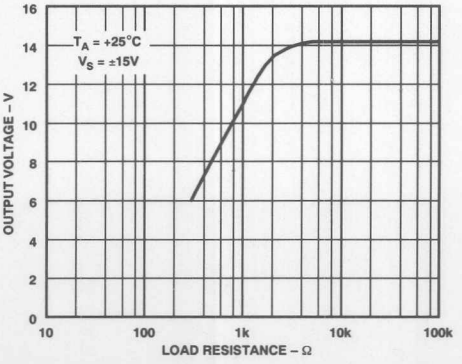


Figure 39. Maximum Output Voltage vs. Load Resistance

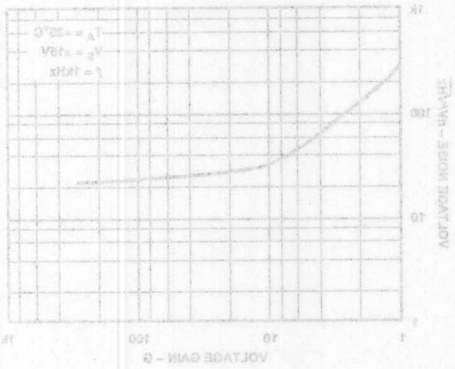


Figure 34. Voltage Noise Density vs. Gain

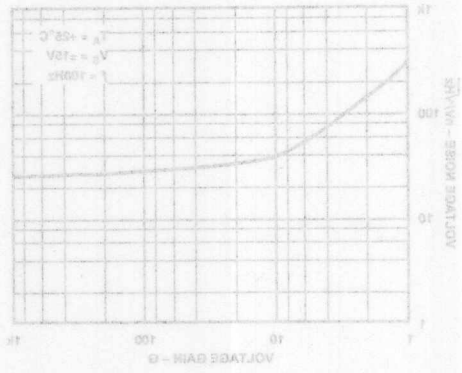


Figure 35. Voltage Noise Density vs. Gain, f = 1 kHz

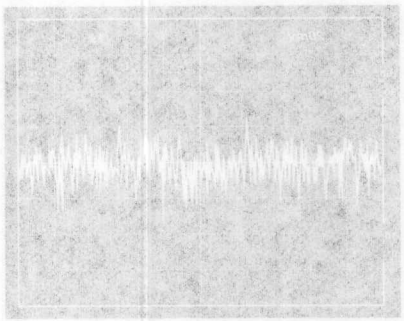


Figure 37. Input Noise Voltage

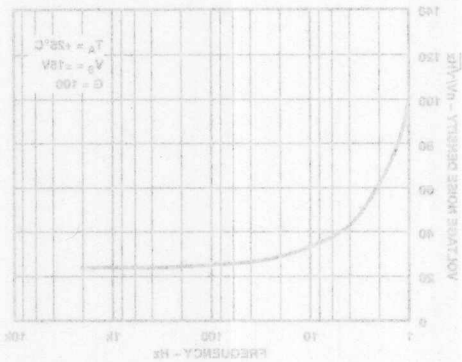


Figure 36. Voltage Noise Density vs. Frequency

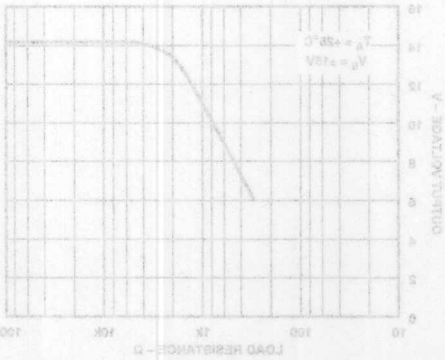


Figure 39. Maximum Output Voltage vs. Load Resistance

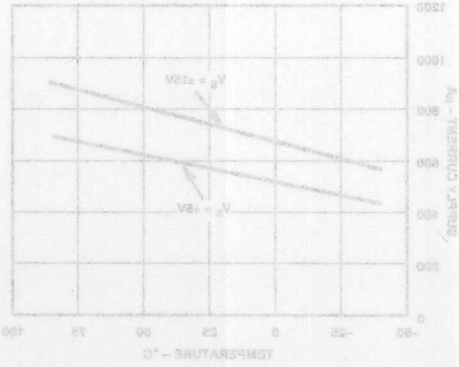


Figure 38. Supply Current vs. Temperature

Isolation Amplifiers
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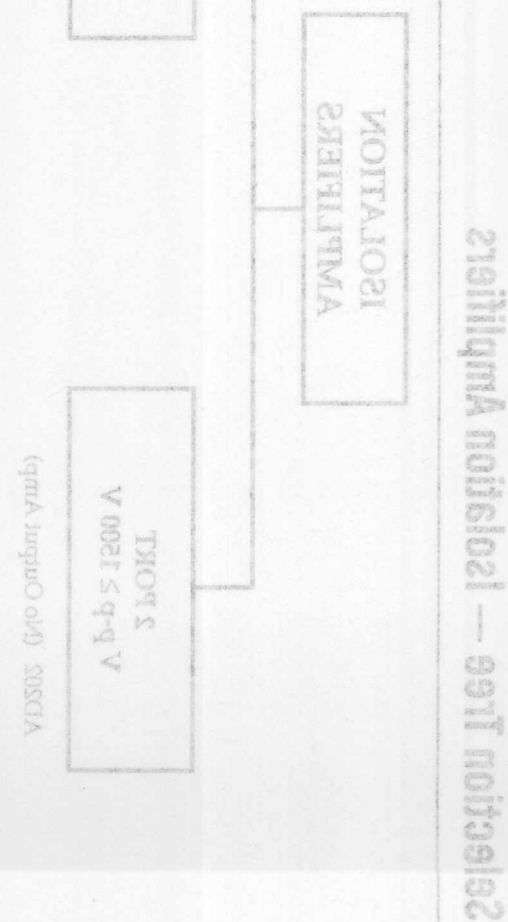
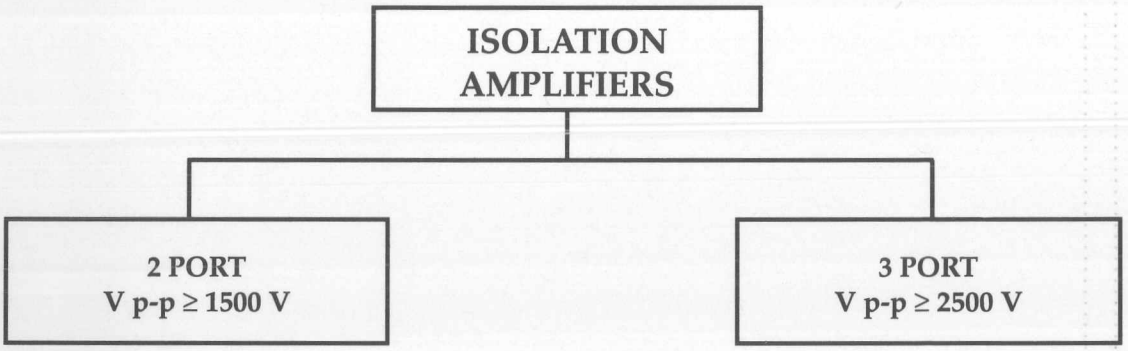


11

Selection Tree — Isolation Amplifiers



AD202 (No Output Amp)

AD204* (With Output Amp)

AD210 (20 kHz BW)

*Multichannel: Require Clock Driver AD246

Selection Guide—Isolation Amplifiers

Model	Peak Volt Iso V pk	Gain Range V/V	Gain Nonlin % max	Freq Resp kHz	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
289	2500	1–100	0.012–0.05	20	Module	C	Precision, Wide Bandwidth, Synchronized	A 5–75
290A	1500	1–100	0.1–0.25	2.5	Module	I	Single Channel, General Purpose	A 5–81
292A	1500	1–100	0.1–0.25	2.5	Module	I	Multichannel, General Purpose	A 5–81
AD202	**1000–2000**	**1–100**	**0.025–0.05**	**2**	**N, Y**	**C**	**Lowest Cost, Small Size, Single Channel**	**11–5**
AD203	2000	1–100	0.025	10	N	M	Rugged, Military Temperature Range, Wide Bandwidth	A 5–19
AD204	**1000–2000**	**1–100**	**0.025-0.05**	**5**	**N, Y**	**I**	**Lowest Cost, Small Size, Multichannel**	**11–5**
AD208	1000–2000	1–1000	0.015–0.03	0.4–4 kHz	Y	I	Precision, Low Cost, Single Channel, mV Input	A 5–41
AD210	**2500–3500**	**1–100**	**0.012–0.025**	**20**	**N**	**I**	**Precision, 3-Port Isolation, Wide Bandwidth**	**11–12**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]A = *Amplifier Reference Manual*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Selection Guide — Isolation Amplifiers

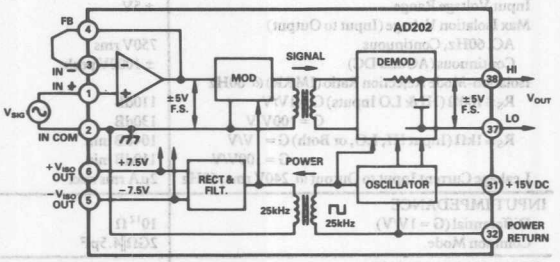
Low Cost, Miniature Isolation Amplifiers

AD202/AD204

FEATURES
Small Size: 4 Channels/Inch
Low Power: 35mW (AD204)
High Accuracy: ±0.025% max Nonlinearity (K Grade)
High CMR: 130dB (Gain = 100V/V)
Wide Bandwidth: 5kHz Full-Power (AD204)
High CMV Isolation: ±2000V pk Continuous (K Grade) (Signal and Power)
Isolated Power Outputs
Uncommitted Input Amplifier

APPLICATIONS
Multichannel Data Acquisition
Current Shunt Measurements
Motor Controls
Process Signal Isolation
High Voltage Instrumentation Amplifier

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD202 and AD204 are general purpose, two-port, transformer-coupled isolation amplifiers that may be used in a broad range of applications where input signals must be measured, processed and/or transmitted without a galvanic connection. These industry standard isolation amplifiers offer a complete isolation function, with both signal and power isolation provided for in a single compact plastic SIP or DIP style package. The primary distinction between the AD202 and the AD204 is that the AD202 is powered directly from a +15V dc supply while the AD204 is powered by an externally supplied clock, such as the recommended AD246 Clock Driver.

The AD202 and AD204 provide total galvanic isolation between the input and output stages of the isolation amplifier through the use of internal transformer-coupling. The functionally complete AD202 and AD204 eliminate the need for an external, user-supplied dc/dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs.

The design of the AD202 and AD204 emphasizes maximum flexibility and ease of use, including the availability of an uncommitted op amp on the input stage. They feature a bipolar ±5V output range, an adjustable gain range of from 1 to 100V/V, ±0.025% max nonlinearity (K grade), 130dB of CMR and the AD204 consumes a low 35mW of power.

PRODUCT HIGHLIGHTS

The AD202 and AD204 are full-featured isolators offering numerous benefits to the user:

Small Size: The AD202 and AD204 are available in SIP and DIP form packages. The SIP package is just 0.25" wide, giving the user a channel density of four channels per inch. The isolation barrier is positioned to maximize input to output spacing. For applications requiring a low profile, the DIP package provides a height of just 0.350".

High Accuracy: With a maximum nonlinearity of ±0.025% for the AD202K/AD204K (±0.05% for the AD202J/AD204J) and low drift over temperature, the AD202 and AD204 provide high isolation without loss of signal integrity.

Low Power: Power consumption of 35mW (AD204) and 75mW (AD202) over the full signal range makes these isolators ideal for use in applications with large channel counts or tight power budgets.

Wide Bandwidth: The AD204's full-power bandwidth of 5kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Excellent Common-Mode Performance: The AD202K/AD204K provide ±2000V pk continuous common-mode isolation, while the AD202J/AD204J provide ±1000V pk continuous common-mode isolation. All models have a total common-mode input capacitance of less than 5pF inclusive of power isolation. This results in CMR ranging from 130dB at a gain of 100 to 104dB (minimum at unity gain) and very low leakage current (2μA maximum).

Flexible Input: An uncommitted op amp is provided at the input of all models. This provides buffering and gain as required, and facilitates many alternative input functions including filtering, summing, high-voltage ranges, and current (transimpedance) input.

Isolated Power: The AD204 can supply isolated power of ±7.5V at 2mA. This is sufficient to operate a low-drift input preamp, provide excitation to a semiconductor strain gage, or to power any of a wide range of user-supplied ancillary circuits. The AD202 can supply ±7.5V at 0.4mA which is sufficient to operate adjustment networks or low-power references and op amps, or to provide an open-input alarm.

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

vs. Temperature	± 20ppm/°C typ (± 45ppm/°C max)	*	*	*
vs. Time	± 50ppm/1000 Hours	*	*	*
vs. Supply Voltage	± 0.01%/V	± 0.01%/V	± 0.01%/V	± 0.01%/V
Nonlinearity (G = 1V/V)[1]	± 0.05% max	± 0.025% max	± 0.05% max	± 0.025% max
Nonlinearity vs. Isolated Supply Load	± 0.0015%/mA	*	*	*
INPUT VOLTAGE RATINGS				
Input Voltage Range	± 5V	*	*	*
Max Isolation Voltage (Input to Output)				
AC, 60Hz, Continuous	750V rms	1500V rms	750V rms	1500V rms
Continuous (AC and DC)	± 1000V peak	± 2000V peak	± 1000V peak	± 2000V peak
Isolation-Mode Rejection Ratio (IMRR) @ 60Hz				
$R_S \leq 100\Omega$ (HI & LO Inputs) G = 1V/V	110dB	110dB	105dB	105dB
G = 100V/V	130dB	*	*	*
$R_S \leq 1k\Omega$ (Input HI, LO, or Both) G = 1V/V	104dB min	104dB min	100dB min	100dB min
G = 100V/V	110dB min	*	*	*
Leakage Current Input to Output @ 240V rms, 60Hz	2μA rms max	*	*	*
INPUT IMPEDANCE				
Differential (G = 1V/V)	$10^{12}\ \Omega$	*	*	*
Common Mode	$2G\Omega \| 4.5pF$	*	*	*
INPUT BIAS CURRENT				
Initial, @ + 25°C	± 30pA	*	*	*
vs. Temperature (0 to + 70°C)	± 10nA	*	*	*
INPUT DIFFERENCE CURRENT				
Initial, @ + 25°C	± 5pA	*	*	*
vs. Temperature (0 to + 70°C)	± 2nA	*	*	*
INPUT NOISE				
Voltage, 0.1 to 100Hz	4μV p-p	*	*	*
f > 200Hz	$50nV/\sqrt{Hz}$	*	*	*
FREQUENCY RESPONSE				
Bandwidth ($V_O \leq 10V$ p-p, G = 1-50V/V)	5kHz	5kHz	2kHz	2kHz
Settling Time, to ± 10mV (10V Step)	1ms	*	*	*
OFFSET VOLTAGE (RTI)				
Initial, @ + 25°C Adjustable to Zero	$(\pm 15 \pm 15/G)$mV max	$(\pm 5 \pm 5/G)$mV max	$(\pm 15 \pm 15/G)$mV max	$(\pm 5 \pm 5/G)$mV max
vs. Temperature (0 to + 70°C)	$\left(\pm 10 \pm \frac{10}{G}\right)\mu V/°C$	*	*	*
RATED OUTPUT				
Voltage (Out HI to Out LO)	± 5V	*	*	*
Voltage at Out HI or Out LO (Ref. Pin 32)	± 6.5V	*	*	*
Output Resistance	3kΩ	3kΩ	7kΩ	7kΩ
Output Ripple, 100kHz Bandwidth	10mV pk-pk	*	*	*
5kHz Bandwidth	0.5mV rms	*	*	*
ISOLATED POWER OUTPUT[2]				
Voltage, No Load	± 7.5V	*	*	*
Accuracy	± 10%	*	*	*
Current	2mA (Either Output)[3]	2mA (Either Output)[3]	400μA Total	400μA Total
Regulation, No Load to Full Load	5%	*	*	*
Ripple	100mV pk-pk	*	*	*
OSCILLATOR DRIVE INPUT				
Input Voltage	15V pk-pk nominal	15V pk-pk nominal	N/A	N/A
Input Frequency	25kHz nominal	25kHz nominal	N/A	N/A
POWER SUPPLY (AD202 Only)				
Voltage, Rated Performance	N/A	N/A	+ 15V ± 5%	+ 15V ± 5%
Voltage, Operating	N/A	N/A	+ 15V ± 10%	+ 15V ± 10%
Current, No Load (V_S = + 15V)	N/A	N/A	5mA	5mA
TEMPERATURE RANGE				
Rated Performance	0 to + 70°C	*	*	*
Operating	− 40°C to + 85°C	*	*	*
Storage	− 40°C to + 85°C	*	*	*
PACKAGE DIMENSIONS[4]				
SIP Package (Y)	2.08" × 0.250" × 0.625"	*	*	*
DIP Package (N)	2.10" × 0.700" × 0.350"	*	*	*

NOTES
*Specifications same as AD204J.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]1.0μF min decoupling required (see text).
[3]3mA with one supply loaded.
[4]Width is 0.25" typ, 0.26" max.
Specifications subject to change without notice.

PIN DESIGNATIONS

AD202/AD204 SIP PACKAGE

PIN	FUNCTION
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	−INPUT
4	INPUT FEEDBACK
5	−V_{ISO} OUTPUT
6	+V_{ISO} OUTPUT
31	+15V POWER IN (AD202 ONLY)
32	CLOCK/POWER COMMON
33	CLOCK INPUT (AD204 ONLY)
37	OUTPUT LO
38	OUTPUT HI

AD202/AD204 DIP PACKAGE

PIN	FUNCTION
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	−INPUT
18	OUTPUT LO
19	OUTPUT HI
20	+15V POWER IN (AD202 ONLY)
21	CLOCK INPUT (AD204 ONLY)
22	CLOCK/POWER COMMON
36	+V_{ISO} OUTPUT
37	−V_{ISO} OUTPUT
38	INPUT FEEDBACK

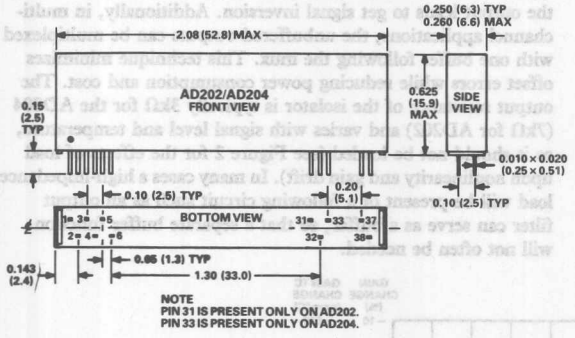
ORDERING GUIDE

Model	Package Option	Max Common-Mode Voltage (Peak)	Max Linearity
AD202JY	SIP	1000V	±0.05%
AD202KY	SIP	2000V	±0.025%
AD202JN	DIP	1000V	±0.05%
AD202KN	DIP	2000V	±0.025%
AD204JY	SIP	1000V	±0.05%
AD204KY	SIP	2000V	±0.025%
AD204JN	DIP	1000V	±0.05%
AD204KN	DIP	2000V	±0.025%

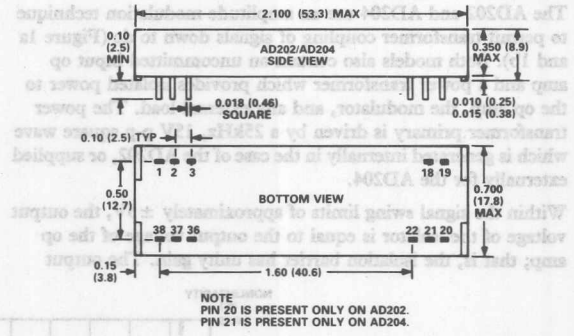
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

AD202/AD204 SIP PACKAGE



AD202/AD204 DIP PACKAGE



DIFFERENCES BETWEEN THE AD202 AND AD204

The primary distinction between the AD202 and AD204 is in the method by which they are powered: the AD202 operates directly from +15V dc while the AD204 is powered by a non-isolated externally-supplied clock (AD246) which can drive up to 32 AD204s. The main advantages of using the externally-clocked AD204 over the AD202 are reduced cost in multichannel applications, lower power consumption, and higher bandwidth. In addition, the AD204 can supply substantially more isolated power than the AD202.

Of course, in a great many situations, especially where only one or a few isolators are used, the convenience of stand-alone operation provided by the AD202 will be more significant than any of the AD204's advantages. There may also be cases where it is desirable to accommodate either device interchangeably, so the pinouts of the two products have been designed to make that easy to do.

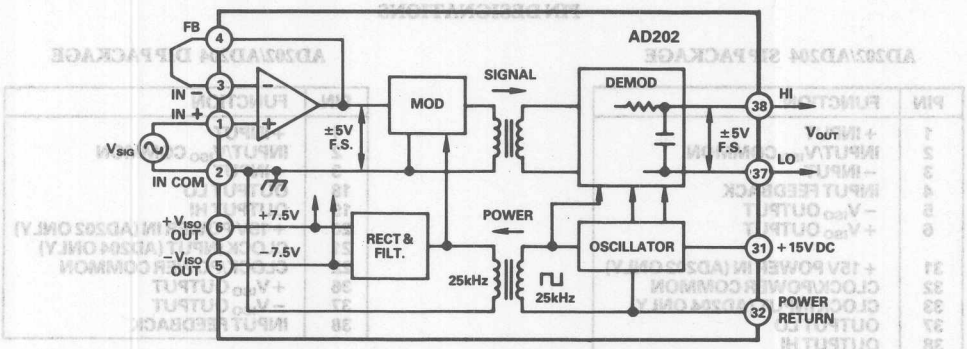


Figure 1a. AD202 Functional Block Diagram

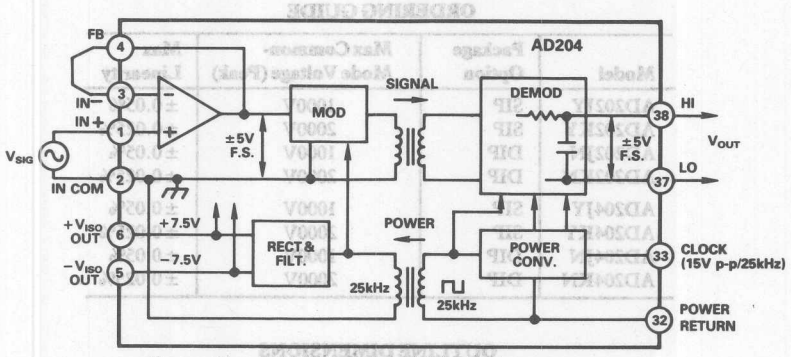


Figure 1b. AD204 Functional Block Diagram
(Pin Designations Apply to the DIP-Style Package.)

INSIDE THE AD202 AND AD204

The AD202 and AD204 use an amplitude modulation technique to permit transformer coupling of signals down to dc (Figure 1a and 1b). Both models also contain an uncommitted input op amp and a power transformer which provides isolated power to the op amp, the modulator, and any external load. The power transformer primary is driven by a 25kHz, 15V p-p square wave which is generated internally in the case of the AD202, or supplied externally for the AD204.

Within the signal swing limits of approximately ±5V, the output voltage of the isolator is equal to the output voltage of the op amp; that is, the isolation barrier has unity gain. The output signal is not internally buffered, so the user is free to interchange the output leads to get signal inversion. Additionally, in multi-channel applications, the unbuffered outputs can be multiplexed with one buffer following the mux. This technique minimizes offset errors while reducing power consumption and cost. The output resistance of the isolator is typically 3kΩ for the AD204 (7kΩ for AD202) and varies with signal level and temperature, so it should not be loaded (see Figure 2 for the effects of load upon nonlinearity and gain drift). In many cases a high-impedance load will be present or a following circuit such as an output filter can serve as a buffer, so that a separate buffer function will not often be needed.

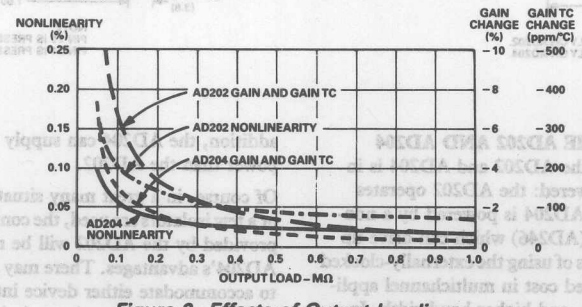


Figure 2. Effects of Output Loading

(Circuit figures shown on this page are for SIP style packages. Refer to page 3 for proper DIP package pin-out.)

USING THE AD202 AND AD204

Powering the AD202. The AD202 requires only a single +15V power supply connected as shown in Figure 3a. A bypass capacitor is provided in the module.

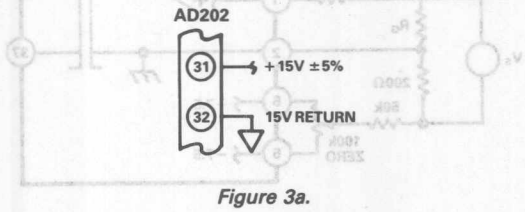


Figure 3a.

Powering the AD204. The AD204 gets its power from an externally supplied clock signal (a 15V p-p square wave with a nominal frequency of 25kHz) as shown in Figure 3b.

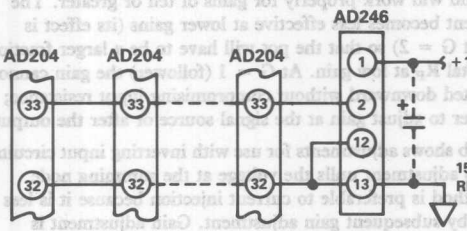


Figure 3b.

AD246 Clock Driver. The AD246 is a compact, inexpensive clock driver that can be used to obtain the required clock from a single 15V supply. Alternatively, the circuit shown in Figure 4 (essentially an AD246) can be used. In either case, one clock circuit can operate at least 32 AD204s at the rated minimum supply voltage of 14.25V and one additional isolator can be operated for each 40mV increase in supply voltage up to 15V. A supply bypass capacitor is included in the AD246, but if many AD204s are operated from a single AD246, an external bypass capacitor should be used with a value of at least 1μF for every five isolators used. Place the capacitor as close as possible to the clock driver.

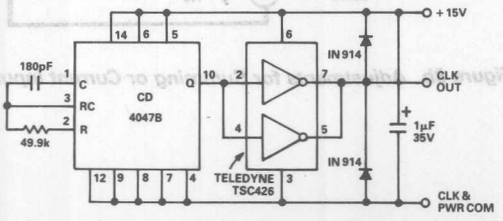


Figure 4. Clock Driver

(Circuit figures shown on this page are for SIP style packages. Refer to page 3 for proper DIP package pin-out.)

Input Configurations. The AD202 and AD204 have been designed to be very easy to use in a wide range of applications. The basic connection for standard unity gain applications, useful for signals up to ±5V, is shown in Figure 5; some of the possible variations are described below. When smaller signals must be

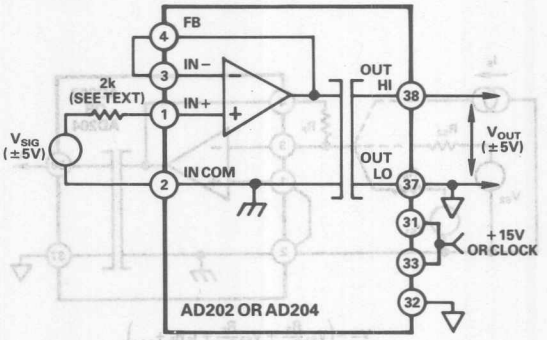


Figure 5. Basic Unity-Gain Application

handled, Figure 6 shows how to get gain while preserving a very high input resistance. The value of feedback resistor R_F should be kept above 20kΩ for best results. Whenever a gain of more than five is taken, a 100pF capacitor from FB to IN COM is required. At lower gains this capacitor is unnecessary, but it will not adversely affect performance if used.

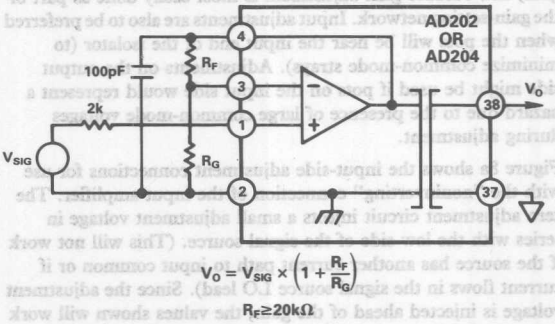


Figure 6. Input Connections for Gain > 1

The "noninverting" circuit of Figures 5 and 6 can also be used to advantage when a signal inversion is needed: just interchange either the input leads or the output leads to get inversion. This approach retains the high input resistance of the "noninverting" circuit, and at unity gain no gain-setting resistors are needed.

When the isolator is not powered, a negative input voltage of more than about 2V will cause an input current to flow. If the signal source can supply more than a few mA under such conditions, the 2kΩ resistor shown in series with IN+ should be used to limit current to a safe value. This is particularly important with the AD202, which may not start if a large input current is present.

for example, a ±50V input span can be accommodated with R_F = 20k and R_S = 200k. Once again, a capacitor from FB to IN COM is required for gains above 5.

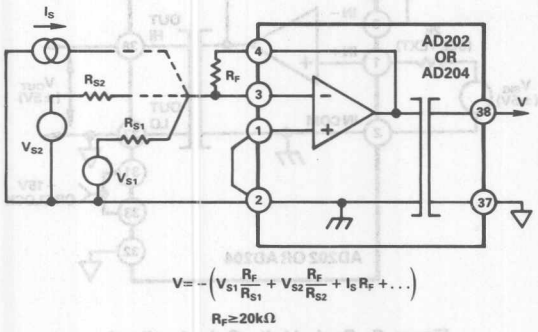


Figure 7. Connections for Summing or Current Inputs

Adjustments. When gain and zero adjustments are needed, the circuit details will depend on whether adjustments are to be made at the isolator input or output, and (for input adjustments) on the input circuit used. Adjustments are usually best done on the input side, because it is better to null the zero ahead of the gain, and because gain adjustment is most easily done as part of the gain-setting network. Input adjustments are also to be preferred when the pots will be near the input end of the isolator (to minimize common-mode strays). Adjustments on the output side might be used if pots on the input side would represent a hazard due to the presence of large common-mode voltages during adjustment.

Figure 8a shows the input-side adjustment connections for use with the "noninverting" connection of the input amplifier. The zero adjustment circuit injects a small adjustment voltage in series with the low side of the signal source. (This will not work if the source has another current path to input common or if current flows in the signal source LO lead). Since the adjustment voltage is injected ahead of the gain, the values shown will work for any gain. Keep the resistance in series with input LO below a few hundred ohms to avoid CMR degradation.

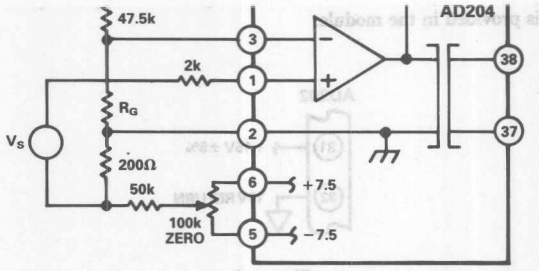


Figure 8a. Adjustments for Noninverting Connection of Op Amp

Also shown in Figure 8a is the preferred means of adjusting the gain-setting network. The circuit shown gives a nominal R_F of 50kΩ, and will work properly for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G = 2) so that the pot will have to be a larger fraction of the total R_F at low gain. At G = 1 (follower) the gain cannot be adjusted downward without compromising input resistance; it is better to adjust gain at the signal source or after the output.

Figure 8b shows adjustments for use with inverting input circuits. The zero adjustment nulls the voltage at the summing node. This method is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is again done in the feedback; but in this case it will work all the way down to unity gain (and below) without alteration.

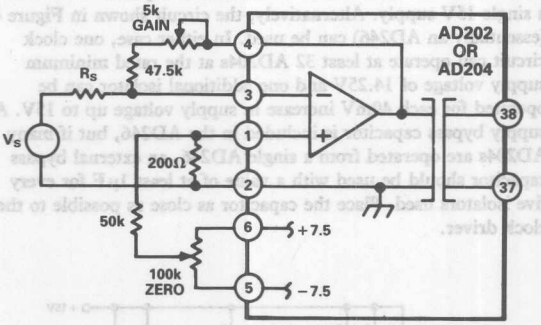


Figure 8b. Adjustments for Summing or Current Input

(Circuit figures shown on this page are for SIP style packages. Refer to page 3 for proper DIP package pin-out.)

Figure 9 shows how zero adjustment is done at the output by taking advantage of the semi-floating output port. The range of this adjustment will have to be increased at higher gains; if that is done, be sure to use a suitably stable supply voltage for the pot circuit.

There is no easy way to adjust gain at the output side of the isolator itself. If gain adjustment must be done on the output side, it will have to be in a following circuit such as an output buffer or filter.

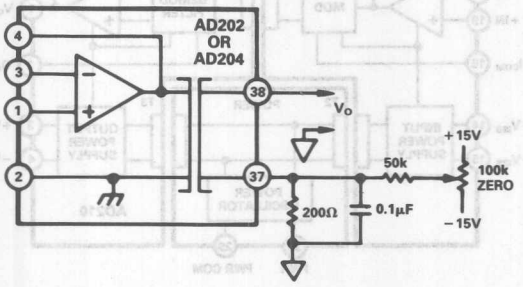


Figure 9. Output-Side Zero Adjustment

Common-Mode Performance. Figures 10a and 10b show how the common-mode rejection of the AD202 and AD204 varies with frequency, gain, and source resistance. For these isolators, the significant resistance will normally be that the path from the source of the common-mode signal to IN COM. The AD202 and AD204 also perform well in applications requiring rejection of fast common-mode steps, as described in the Applications section.

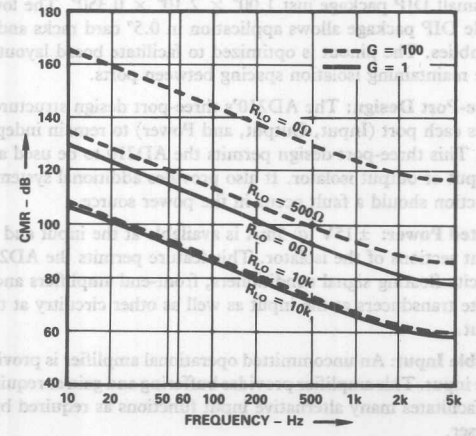


Figure 10a. AD204

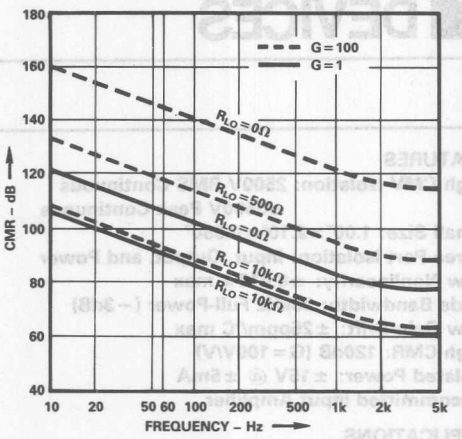


Figure 10b. AD202

APPLICATION EXAMPLE

Process Current Input with Offset. Figure 11 shows an isolator receiver which translates a 4-20mA process current signal into a 0 to +10V output. A 1V to 5V signal appears at the isolator's output, and a −1V reference applied to output LO provides the necessary level shift (in multichannel applications, the reference can be shared by all channels). This technique is often useful for getting offset with a follower-type output buffer.

The circuit as shown requires a source compliance of at least 5V, but if necessary that can be reduced by using a lower value of current-sampling resistor and configuring the input amplifier for a small gain.

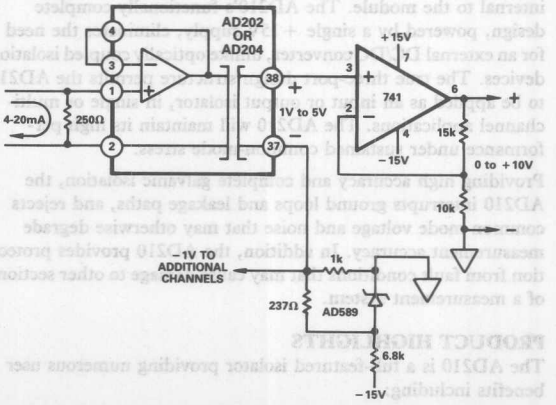


Figure 11. Process Current Input Isolator with Offset

(Circuit figures shown on this page are for SIP style packages. Refer to page 3 for proper DIP package pin-out.)

Precision, Wide Bandwidth, 3-Port Isolation Amplifier

AD210*

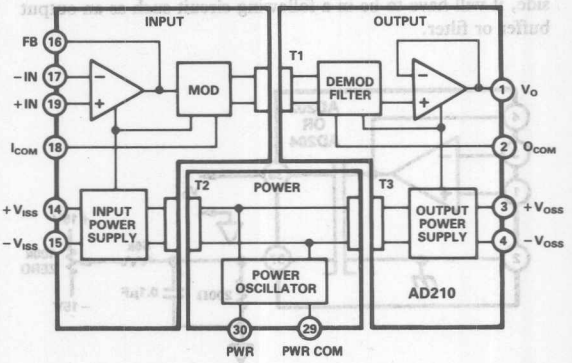
FEATURES

High CMV Isolation: 2500V RMS Continuous
±3500V Peak Continuous
Small Size: 1.00″ × 2.10″ × 0.350″
Three-Port Isolation: Input, Output, and Power
Low Nonlinearity: ±0.012% max
Wide Bandwidth: 20kHz Full-Power (−3dB)
Low Gain Drift: ±25ppm/°C max
High CMR: 120dB (G = 100V/V)
Isolated Power: ±15V @ ±5mA
Uncommitted Input Amplifier

APPLICATIONS

Multichannel Data Acquisition
High Voltage Instrumentation Amplifier
Current Shunt Measurements
Process Signal Isolation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD210 is the latest member of a new generation of low cost, high performance isolation amplifiers. This three-port, wide bandwidth isolation amplifier is manufactured with surface-mounted components in an automated assembly process. The AD210 combines design expertise with state-of-the-art manufacturing technology to produce an extremely compact and economical isolator whose performance and abundant user features far exceed those offered in more expensive devices.

The AD210 provides a complete isolation function with both signal and power isolation supplied via transformer coupling internal to the module. The AD210's functionally complete design, powered by a single +15V supply, eliminates the need for an external DC/DC converter, unlike optically coupled isolation devices. The true three-port design structure permits the AD210 to be applied as an input or output isolator, in single or multi-channel applications. The AD210 will maintain its high performance under sustained common-mode stress.

Providing high accuracy and complete galvanic isolation, the AD210 interrupts ground loops and leakage paths, and rejects common-mode voltage and noise that may otherwise degrade measurement accuracy. In addition, the AD210 provides protection from fault conditions that may cause damage to other sections of a measurement system.

PRODUCT HIGHLIGHTS

The AD210 is a full-featured isolator providing numerous user benefits including:

High Common-Mode Performance: The AD210 provides 2500V rms (Continuous) and ±3500V peak (Continuous) common-mode voltage isolation between any two ports. Low input to output capacitance of 5pF results in a 120dB CMR at a gain of 100, and a low leakage current (2μA rms max @ 240V rms, 60Hz).

High Accuracy: With maximum nonlinearity of ±0.012% (B Grade), gain drift of ±25ppm/°C max, and input offset drift of (±10 ± 30/G) μV/°C, the AD210 assures signal integrity while providing high level isolation.

Wide Bandwidth: The AD210's full-power bandwidth of 20kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Small Size: The AD210 provides a complete isolation function in a small DIP package just 1.00″ × 2.10″ × 0.350″. The low profile DIP package allows application in 0.5″ card racks and assemblies. The pinout is optimized to facilitate board layout while maintaining isolation spacing between ports.

Three-Port Design: The AD210's three-port design structure allows each port (Input, Output, and Power) to remain independent. This three-port design permits the AD210 to be used as an input or output isolator. It also provides additional system protection should a fault occur in the power source.

Isolated Power: ±15V @ 5mA is available at the input and output sections of the isolator. This feature permits the AD210 to excite floating signal conditioners, front-end amplifiers and remote transducers at the input as well as other circuitry at the output.

Flexible Input: An uncommitted operational amplifier is provided at the input. This amplifier provides buffering and gain as required, and facilitates many alternative input functions as required by the user.

*Covered by U.S. Patent No. 4,703,283.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

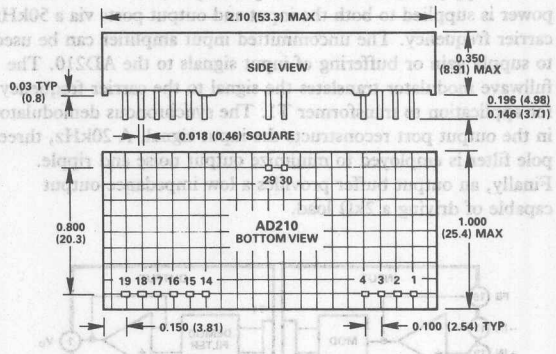
SPECIFICATIONS (typical @ +25°C, & V_S = +15 V unless otherwise noted)

Model	AD210AN	AD210BN	AD210JN
GAIN			
Range	1V/V – 100V/V	*	*
Error	± 2% max	± 1% max	*
vs. Temperature (0 to + 70°C)	± 25ppm/°C max	*	*
(– 25°C to + 85°C)	± 50ppm/°C max	*	*
vs. Supply Voltage	± 0.002%/V	*	*
Nonlinearity[1]	± 0.025% max	± 0.012% max	*
Nonlinearity vs. Isolated Supply Load	± 0.002%/mA	*	*
INPUT VOLTAGE RATINGS			
Linear Differential Range	± 10V	*	*
Maximum Safe Differential Input	± 15V	*	*
Max. CMV Input-to-Output			
ac, 60Hz, Continuous	2500V rms	*	1500V rms
dc, Continuous	± 3500V peak	*	± 2000V peak
Common-Mode Rejection			
60Hz, G = 100V/V			
$R_S \leq 500\Omega$ Impedance Imbalance	120dB	*	*
Leakage Current Input-to-Output			
@ 240Vrms, 60Hz	2μA rms max	*	*
INPUT IMPEDANCE			
Differential	$10^{12}\Omega$	*	*
Common Mode	$5G\Omega \| 5pF$	*	*
INPUT BIAS CURRENT			
Initial, @ + 25°C	30pA typ (400pA max)	*	*
vs. Temperature (0 to + 70°C)	10nA max	*	*
(– 25°C to + 85°C)	30nA max	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ + 25°C	5pA typ (200pA max)	*	*
vs. Temperature (0 to + 70°C)	2nA max	*	*
(– 25°C to + 85°C)	10nA max	*	*
INPUT NOISE			
Voltage (1kHz)	$18nV/\sqrt{Hz}$	*	*
(10Hz to 10kHz)	4μV rms	*	*
Current (1kHz)	$0.01pA/\sqrt{Hz}$	*	*
FREQUENCY RESPONSE			
Bandwidth (– 3dB)			
G = 1V/V	20kHz	*	*
G = 100V/V	15kHz	*	*
Settling Time (± 10mV, 20V Step)			
G = 1V/V	150μs	*	*
G = 100V/V	500μs	*	*
Slew Rate (G = 1V/V)	1V/μs	*	*
OFFSET VOLTAGE (RTI)[2]			
Initial, @ + 25°C	(± 15 ± 45/G)mV max	(± 5 ± 15/G)mV max	*
vs. Temperature (0 to + 70°C)	(± 10 ± 30/G)μV/°C	*	*
(– 25°C to + 85°C)	(± 10 ± 50/G)μV/°C	*	*
RATED OUTPUT[3]			
Voltage, 2kΩ Load	± 10V min	*	*
Impedance	1Ω max	*	*
Ripple, (Bandwidth = 100kHz)	10mV p-p max	*	*
ISOLATED POWER OUTPUTS[4]			
Voltage, No Load	± 15V	*	*
Accuracy	± 10%	*	*
Current	± 5mA	*	*
Regulation, No Load to Full Load	See Text	*	*
Ripple	See Text	*	*
POWER SUPPLY			
Voltage, Rated Performance	+ 15V dc ± 5%	*	*
Voltage, Operating	+ 15V dc ± 10%	*	*
Current, Quiescent	50mA	*	*
Current, Full Load – Full Signal	80mA	*	*
TEMPERATURE RANGE			
Rated Performance	– 25°C to + 85°C	*	*
Operating	– 40°C to + 85°C	*	*
Storage	– 40°C to + 85°C	*	*
PACKAGE DIMENSIONS			
Inches	1.00 × 2.10 × 0.350	*	*
Millimeters	25.4 × 53.3 × 8.9	*	*

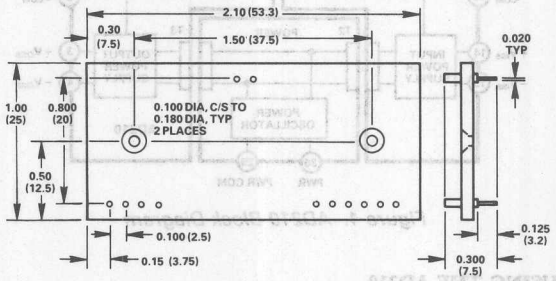
NOTES
*Specifications same as AD210AN.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]RTI – Referred to Input
[3]A reduced signal swing is recommended when both $\pm V_{ISS}$ and $\pm V_{OSS}$ supplies are fully loaded, due to supply voltage reduction.
[4]See text for detailed information.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1059 Mating Socket



AD210 Pin Designations

PIN	DESIGNATION	FUNCTION
1	V_O	Output
2	O_{COM}	Output Common
3	$+V_{OSS}$	+ Isolated Power @ Output
4	$-V_{OSS}$	– Isolated Power @ Output
14	$+V_{ISS}$	+ Isolated Power @ Input
15	$-V_{ISS}$	– Isolated Power @ Input
16	FB	Input Feedback
17	– IN	– Input
18	I_{COM}	Input Common
19	+ IN	+ Input
29	Pwr Com	Power Common
30	Pwr	Power Input

CAUTION
ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

11

INSIDE THE AD210

The AD210 basic block diagram is illustrated in Figure 1. A +15V supply is connected to the power port, and ±15V isolated power is supplied to both the input and output ports via a 50kHz carrier frequency. The uncommitted input amplifier can be used to supply gain or buffering of input signals to the AD210. The fullwave modulator translates the signal to the carrier frequency for application to transformer T1. The synchronous demodulator in the output port reconstructs the input signal. A 20kHz, three-pole filter is employed to minimize output noise and ripple. Finally, an output buffer provides a low impedance output capable of driving a 2kΩ load.

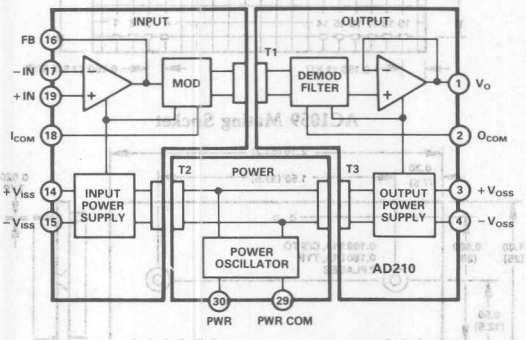


Figure 1. AD210 Block Diagram

USING THE AD210

The AD210 is very simple to apply in a wide range of applications. Powered by a single +15V power supply, the AD210 will provide outstanding performance when used as an input or output isolator, in single and multichannel configurations.

Input Configurations: The basic unity gain configuration for signals up to ±10V is shown in Figure 2. Additional input amplifier variations are shown in the following figures. For smaller signal levels Figure 3 shows how to obtain gain while maintaining a very high input impedance.

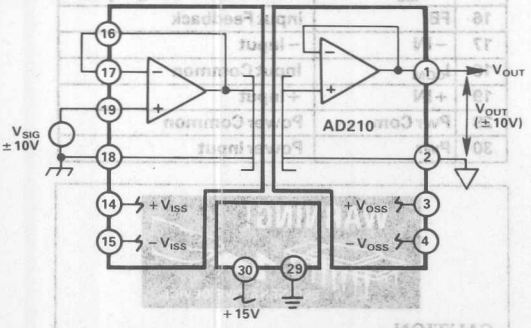


Figure 2. Basic Unity Gain Configuration

The high input impedance of the circuits in Figures 2 and 3 can be maintained in an inverting application. Since the AD210 is a three-port isolator, either the input leads or the output leads may be interchanged to create the signal inversion.

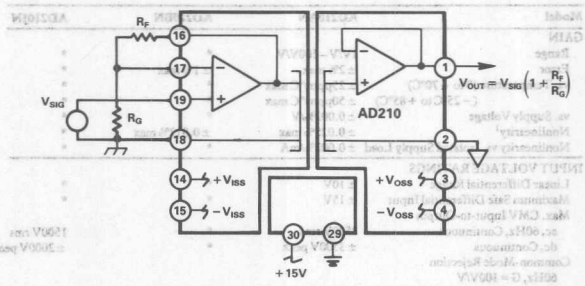


Figure 3. Input Configuration for G>1

Figure 4 shows how to accommodate current inputs or sum currents or voltages. This circuit configuration can also be used for signals greater than ±10V. For example, a ±100V input span can be handled with $R_F = 20k\Omega$ and $R_{S1} = 200k\Omega$.

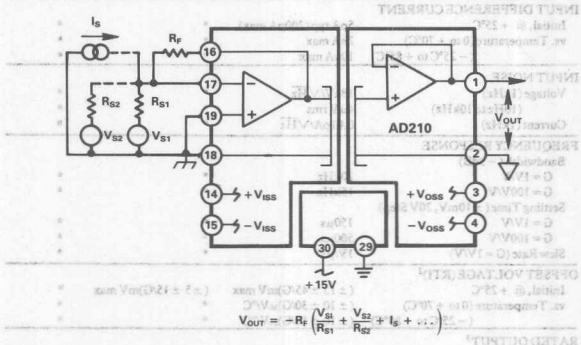


Figure 4. Summing or Current Input Configuration

Adjustments

When gain and offset adjustments are required, the actual circuit adjustment components will depend on the choice of input configuration and whether the adjustments are to be made at the isolator's input or output. Adjustments on the output side might be used when potentiometers on the input side would represent a hazard due to the presence of high common-mode voltage during adjustment. Offset adjustments are best done at the input side, as it is better to null the offset ahead of the gain.

Figure 5 shows the input adjustment circuit for use when the input amplifier is configured in the noninverting mode. This offset adjustment circuit injects a small voltage in series with the

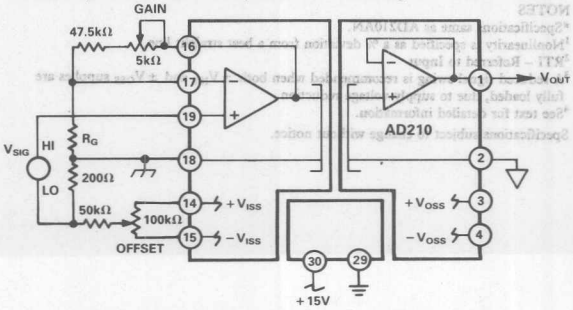


Figure 5. Adjustments for Noninverting Input

low side of the signal source. This will not work if the source has another current path to input common or if current flows in the signal source LO lead. To minimize CMR degradation, keep the resistor in series with the input LO below a few hundred ohms.

Figure 5 also shows the preferred gain adjustment circuit. The circuit shows R_F of 50kΩ, and will work for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G=2) so that the pot will have to be a larger fraction of the total R_F at low gain. At G=1 (follower) the gain cannot be adjusted downward without compromising input impedance; it is better to adjust gain at the signal source or after the output.

Figure 6 shows the input adjustment circuit for use when the input amplifier is configured in the inverting mode. The offset adjustment nulls the voltage at the summing node. This is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is made in the feedback and will work for gains from 1 to 100V/V.

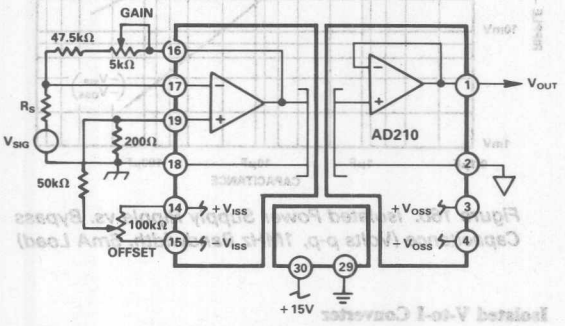


Figure 6. Adjustments for Inverting Input

Figure 7 shows how offset adjustments can be made at the output, by offsetting the floating output port. In this circuit, ±15V would be supplied by a separate source. The AD210's output amplifier is fixed at unity, therefore, output gain must be made in a subsequent stage.

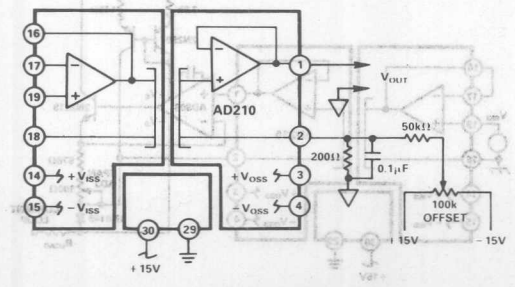


Figure 7. Output-Side Offset Adjustment

PERFORMANCE CHARACTERISTICS

Common-Mode Rejection: Figure 9 shows the common-mode rejection of the AD210 versus frequency, gain and input source resistance. For maximum common-mode rejection of unwanted signals, keep the input source resistance low and carefully lay out the input, avoiding excessive stray capacitance at the input terminals.

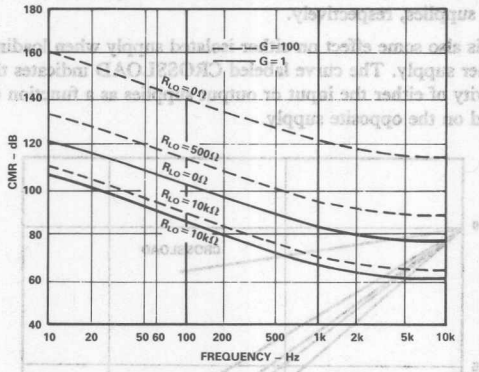


Figure 9. Common-Mode Rejection vs. Frequency

Phase Shift: Figure 10 illustrates the AD210's low phase shift and gain versus frequency. The AD210's phase shift and wide bandwidth performance make it well suited for applications like power monitors and controls systems.

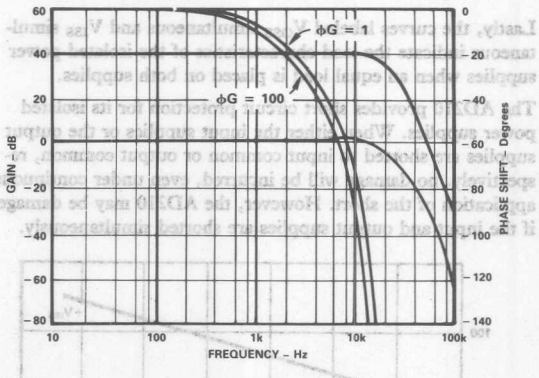


Figure 10. Phase Shift and Gain vs. Frequency

at 5mA.

The load characteristics of the isolated power supplies are shown in Figure 15. For example, when measuring the load rejection of the input isolated supplies V_{ISS}, the load is placed between $+V_{ISS}$ and $-V_{ISS}$. The curves labeled V_{ISS} and V_{OSS} are the individual load rejection characteristics of the input and the output supplies, respectively.

There is also some effect on either isolated supply when loading the other supply. The curve labeled CROSSLOAD indicates the sensitivity of either the input or output supplies as a function of the load on the opposite supply.

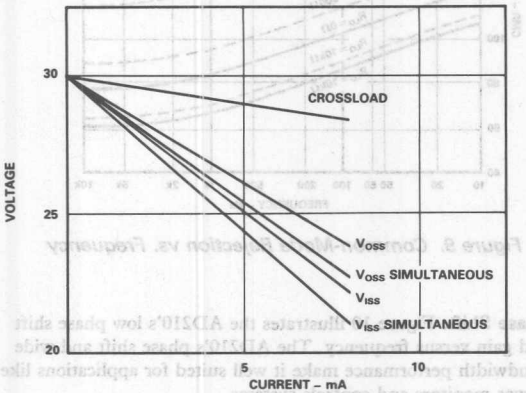


Figure 15. Isolated Power Supplies vs. Load

Lastly, the curves labeled V_{OSS} simultaneous and V_{ISS} simultaneous indicate the load characteristics of the isolated power supplies when an equal load is placed on both supplies.

The AD210 provides short circuit protection for its isolated power supplies. When either the input supplies or the output supplies are shorted to input common or output common, respectively, no damage will be incurred, even under continuous application of the short. However, the AD210 may be damaged if the input and output supplies are shorted simultaneously.

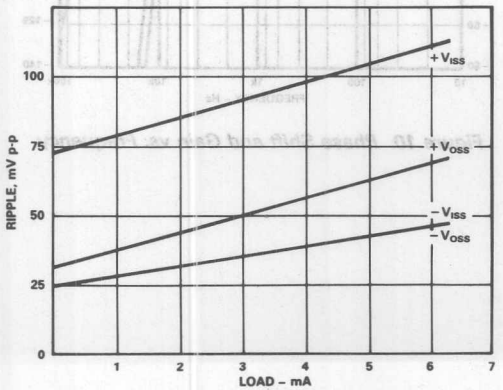


Figure 16a. Isolated Supply Ripple vs. Load (External 4.7μF Bypass)

The isolated power supplies exhibit some ripple which varies as a function of load. Figure 16a shows this relationship. The AD210 has internal bypass capacitance to reduce the ripple to a point where performance is not affected, even under full load. Since the internal circuitry is more sensitive to noise on the negative supplies, these supplies have been filtered more heavily. Should a specific application require more bypassing on the isolated power supplies, there is no problem with adding external capacitors. Figure 16b depicts supply ripple as a function of external bypass capacitance under full load.

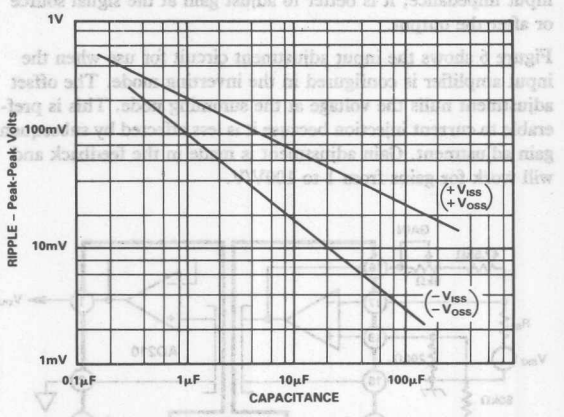


Figure 16b. Isolated Power Supply Ripple vs. Bypass Capacitance (Volts p-p, 1MHz Bandwidth, 5mA Load)

Isolated V-to-I Converter

Illustrated in Figure 19, the AD210 is used to convert a 0 to +10V input signal to an isolated 4-20mA output current. The AD210 isolates the 0 to +10V input signal and provides a proportional voltage at the isolator's output. The output circuit converts the input voltage to a 4-20mA output current, which in turn is applied to the loop load R_{LOAD}.

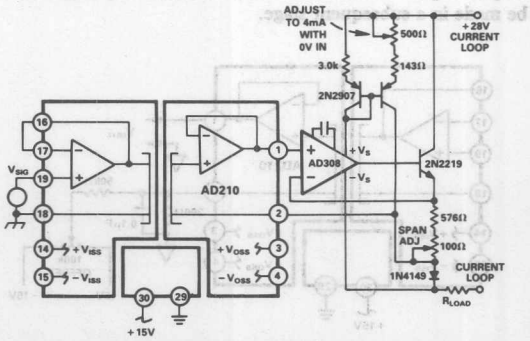


Figure 19. Isolated Voltage-to-Current Loop Converter

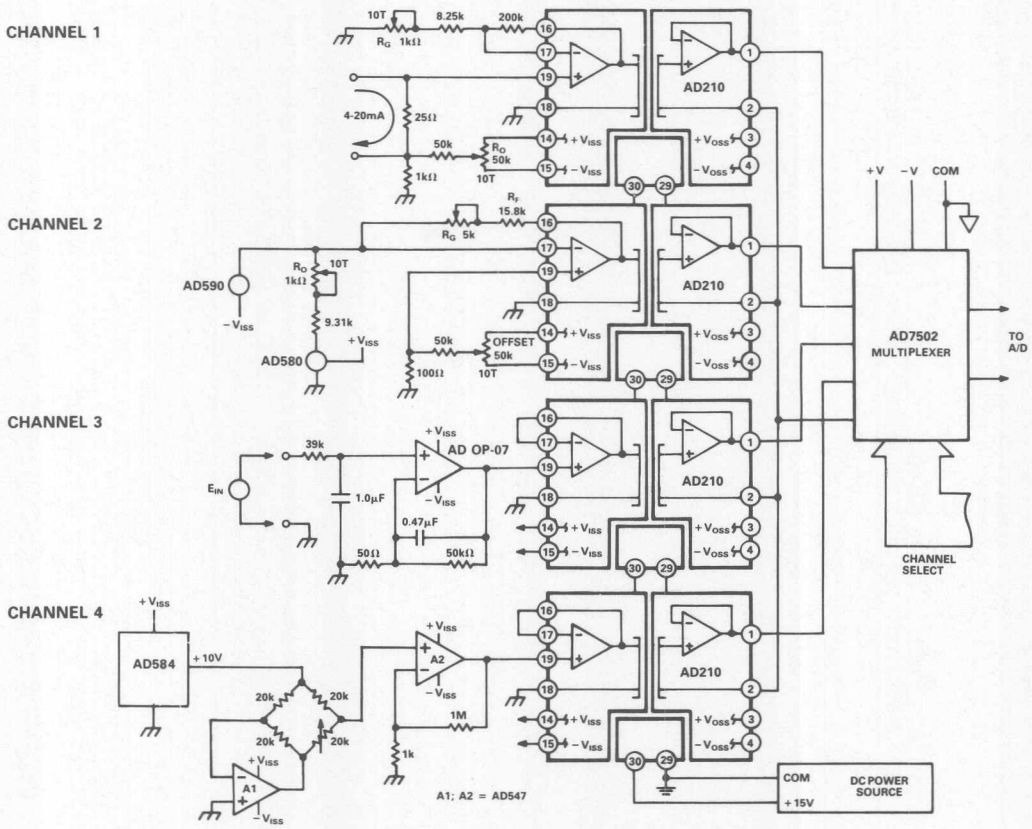


Figure 22. Multichannel Data Acquisition Front End

MULTICHANNEL DATA ACQUISITION FRONT-END

Illustrated in Figure 22 is a four-channel data acquisition front-end used to condition and isolate several common input signals found in various process applications. In this application, each AD210 will provide complete isolation from input to output as well as channel to channel. By using an isolator per channel, maximum protection and rejection of unwanted signals is obtained. The three-port design allows the AD210 to be configured as an input or output isolator. In this application the isolators are configured as input devices with the power port providing additional protection from possible power source faults.

Channel 1: The AD210 is used to convert a 4-20mA current loop input signal into a 0-10V input. The 25Ω shunt resistor converts the 4-20mA current into a +100 to +500mV signal. The signal is offset by −100mV via R_O to produce a 0 to +400mV input. This signal is amplified by a gain of 25 to produce the desired 0 to +10V output. With an open circuit, the AD210 will show −2.5V at the output.

Channel 2: In this channel, the AD210 is used to condition and isolate a current output temperature transducer, Model AD590. At +25°C, the AD590 produces a nominal current of 298.2μA. This level of current will change at a rate of 1μA/°C. At −17.8°C (0°F), The AD590 current will be reduced by 42.8μA to +255.4μA. The AD580 reference circuit provides an equal but opposite current, resulting in a zero net current flow, producing a 0V output from the AD210. At +100°C (+212°F), the AD590 current output will be 373.2μA minus the 255.4μA offsetting current from the AD580 circuit to yield a +117.8μA input current. This current is converted to a voltage via R_F and R_G to produce an output of +2.12V. Channel 2 will produce an output of +10mV/°F over a 0 to +212°F span.

Channel 3: Channel 3 is a low level input channel configured with a high gain amplifier used to condition millivolt signals. With the AD210's input set to unity and the input amplifier set for a gain of 1000, a ±10mV input will produce a ±10V at the AD210's output.

Channel 4: Channel 4 illustrates one possible configuration for conditioning a bridge circuit. The AD584 produces a +10V excitation voltage, while A1 inverts the voltage, producing negative excitation. A2 provides a gain of 1000V/V to amplify the low level bridge signal. Additional gain can be obtained by reconfiguration of the AD210's input amplifier. $\pm V_{ISS}$ provides the complete power for this circuit, eliminating the need for a separate isolated excitation source.

Each channel is individually addressed by the multiplexer's channel select. Additional filtering or signal conditioning should follow the multiplexer, prior to an analog-to-digital conversion stage.

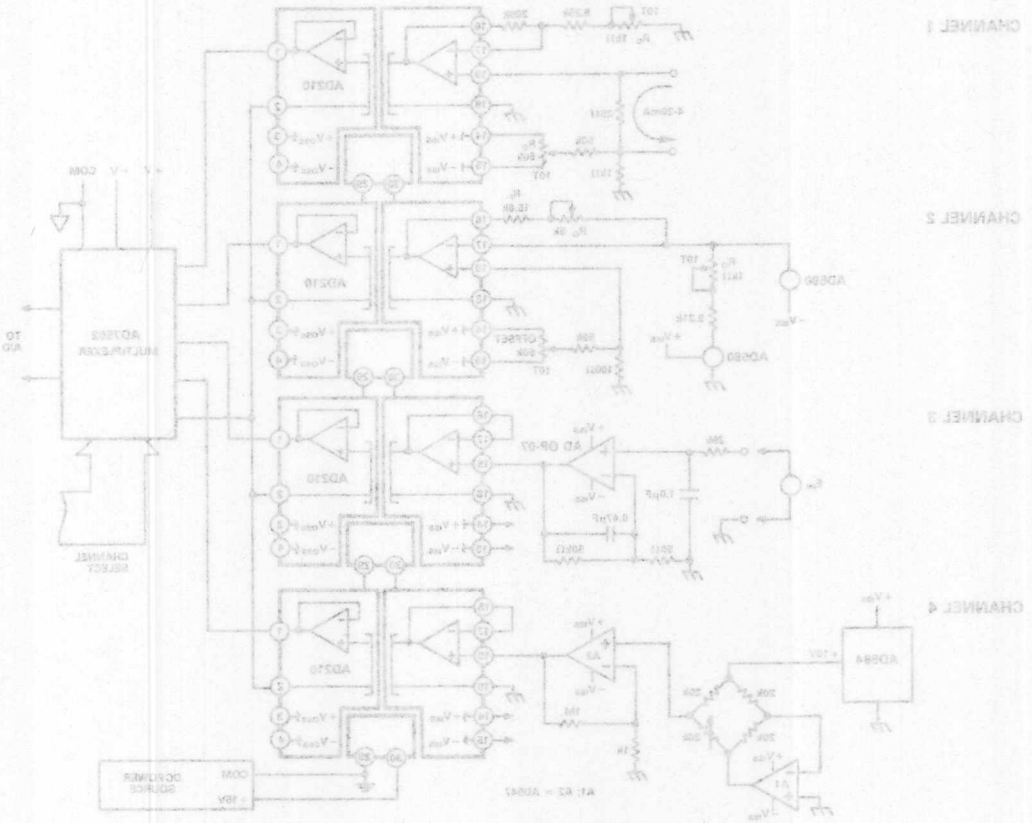


Figure 22. Multichannel Data Acquisition Front End

MULTICHANNEL DATA ACQUISITION FRONT-END

Illustrated in Figure 22 is a four-channel data acquisition front-end used to condition and isolate several common input signals found in various process applications. In this application, each AD210 will provide complete isolation from input to output as well as channel to channel. By using an isolator per channel, maximum protection and rejection of unwanted signals is obtained. The three-port design allows the AD210 to be configured as an input or output isolator. In this application the isolators are configured as input devices with the power port providing additional protection from possible power source faults.

Channel 1: The AD210 is used to convert a 4-20mA current loop input signal into a 0-10V input. The 25Ω shunt resistor converts the 4-20mA current into a +100 to +500mV signal. The signal is offset by −100mV via R_O to produce a 0 to +400mV input. This signal is amplified by a gain of 25 to produce the desired 0 to +10V output. With an open circuit, the AD210 will show −2.5V at the output.

Channel 2: In this channel, the AD210 is used to condition and isolate a current output temperature transducer, Model AD590. At +25°C, the AD590 produces a nominal current of 298.2μA. This level of current will change at a rate of 1μA/°C. At −17.8°C (0°F), The AD590 current will be reduced by 42.8μA to +255.4μA. The AD580 reference circuit provides an equal but opposite current, resulting in a zero net current flow, producing a 0V output from the AD210. At +100°C (+212°F), the AD590 current output will be 373.2μA minus the 255.4μA offsetting current from the AD580 circuit to yield a +117.8μA input current. This current is converted to a voltage via R_F and R_O to produce an output of +2.12V. Channel 2 will produce an output of +10mV/°F over a 0 to +212°F span.

Channel 3: Channel 3 is a low level input channel configured with a high gain amplifier used to condition millivolt signals. With the AD210's input set to unity and the input amplifier set for a gain of 1000, a ±10mV input will produce a ±10V at the AD210's output.

Channel 4: Channel 4 illustrates one possible configuration for conditioning a bridge circuit. The AD584 produces a +10V excitation voltage, while A1 inverts the voltage, producing negative excitation. A2 provides a gain of 1000V/V to amplify the low level bridge signal. Additional gain can be obtained by reconfiguration of the AD210's input amplifier. $\pm V_{ISS}$ provides the complete power for this circuit, eliminating the need for a separate isolated excitation source.

Each channel is individually addressed by the multiplexer's channel select. Additional filtering or signal conditioning should follow the multiplexer, prior to an analog-to-digital conversion stage.

Comparators
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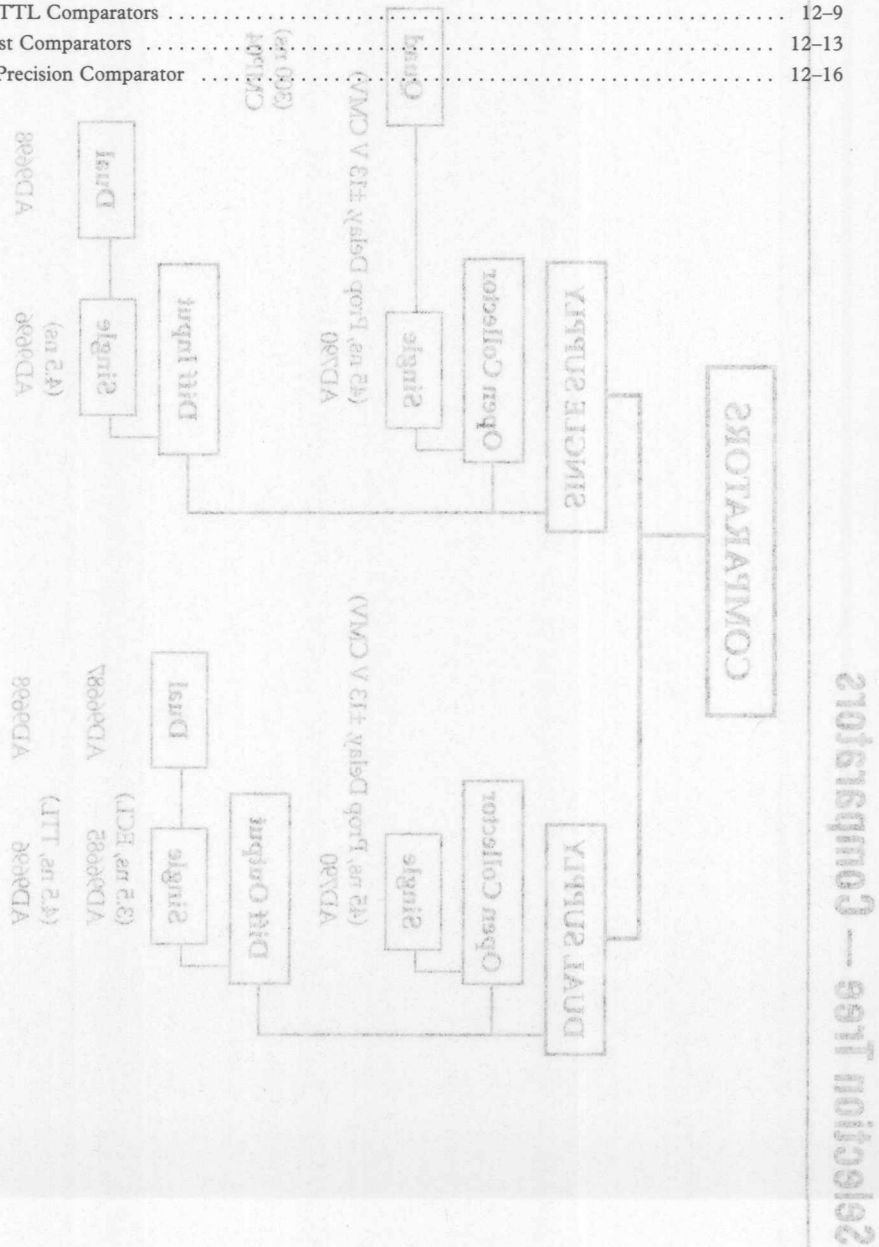

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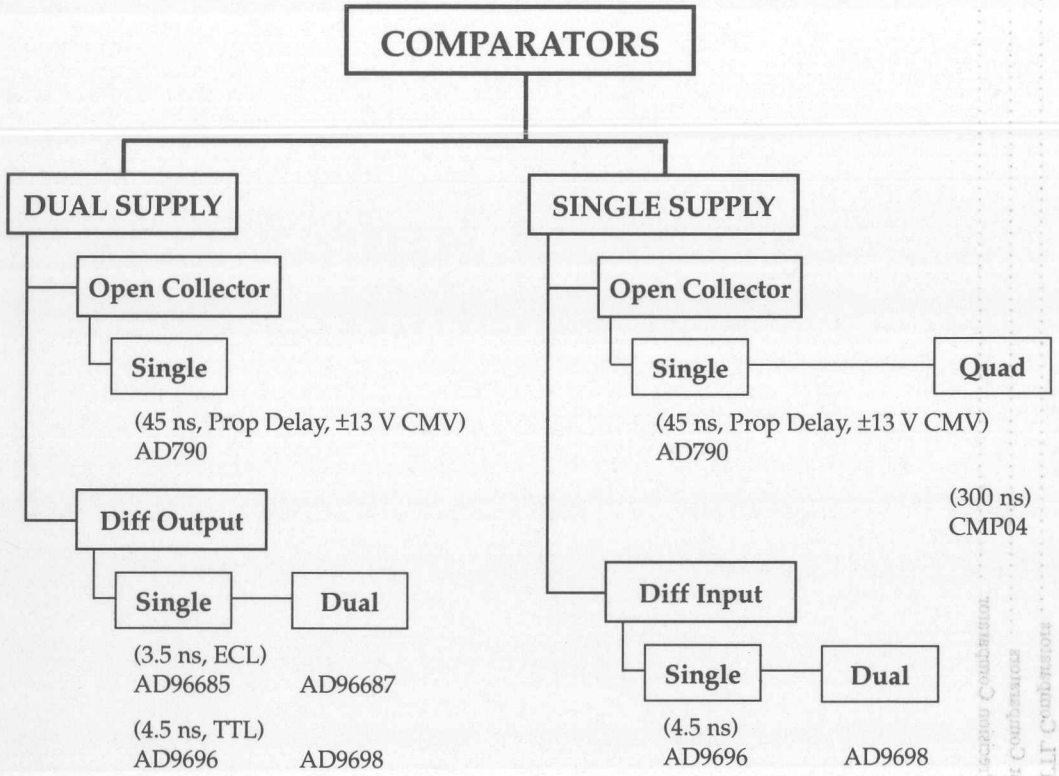
Selection Tree — Comparators



Selection Guide—Comparators

Model	Prop Delay ns max	Dispersion ps	Logic	V_{OS} mV max	Package Options[1]	Temp Ranges[2]	Comments	Page
AD1317	2.5	250	ECL	10	Z	I, $M/_{D}$	Dedicated Window Comparator with Wide CM Range	SL (
AD96685	**3.5**	**50**	**ECL**	**2**	**E, H, P, Q, R**	**I, $M/_{D}$**	**Ultrafast**	**12–1**
AD96687	**3.5**	**50**	**ECL**	**2**	**E, P, Q, R**	**I, M/**	**Dual AD96685**	**12–1**
AD9696	**7.0**	**100**	**TTL**	**2**	**H, N, Q, R, Z**	**C, M/**	**Single Comparator**	**12–5**
AD9698	**7.0**	**100**	**TTL**	**2**	**H, Q, R, Z**	**C, M/**	**Dual Comparator**	**12–5**
AD790	**45**	**—**	**TTL**	**0.25–1**	**N, Q, R**	**C, I, $M/_{D}$**	**Fast, Precise Single or Dual Supply**	**12–5**
CMP05	55	—	TTL	0.6	H, N, Q, R	I, M/	High Speed Precision Comparator	A 3-
CMP01	180	—	TTL	0.8	H, N, Q	C, $M/_{D}$	Fast Precision Comparator	A 3-
CMP02	270	—	TTL	0.8	H, N, Q	C, M	Low Input Current Precision Comparator	A 3-
CMP04	**300 typ**	**—**	**TTL**	**1.0**	**N, Q, R**	**I, $M/_{D}$**	**Quad Low Power Precision Comparator**	**12–1**
PM139	1300	—	TTL	2	D, E, N	I, $M/_{DJ}$	Low Power, Single or Dual Supply	A 3-
PM239	1300	—	TTL	2	D, E, N	I, M	Low Power, Single or Dual Supply	A 3-

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic P
M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S =
Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Ch
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings
temperature designator will be followed by: / to indicate 883B, $_{J}$ for JAN, $_{D}$ for SMD, and $_{S}$ for space level.
[3]A = *Amplifier Reference Manual*; SL = *Special Linear Reference Manual*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Selection Guide — Comparators

Model	Prop Delay ns	Dispersion ns	Voltage mV	Package Options[1]	Temp Ranges[2]	Comments	Page[3]
ADJ817	2.5	250	10	2	I, MIL	Dedicated Window Comparator with Wide CM Range	5-15
ADC6685	3.5	50	2	E, H, J, Q, R	I, MIL	Differential	5-13
ADC6687	3.5	95	2	E, J, Q, R	I, MIL	Dual ADC6685	5-13
ADC6686	7.5	100	2	H, N, Q, R, Z	C, MIL	Single Quad Comparator	5-9
ADC6688	7.0	100	2	H, N, Q, R, Z	C, MIL	Dual Comparator	5-9
ADC790	45	—	0.25–1	N, Q, R	C, I, MIL	Fast, Precise Single or Dual Supply	5-5
ADC795	55	—	0.5	H, N, Q, R	I, MIL	High Speed Precision Comparator	4-31
CMP01	180	—	0.8	H, N, Q	C, MIL	Fast Precision Comparator	4-27
CMP02	270	—	0.8	H, N, Q	C, MIL	Low Input Current Precision Comparator	4-35
CMP08	300 typ	—	1.0	N, Q, R	I, MIL	Quad Low Power, Precision Comparator	5-39
PM139	1300	—	2	D, E, N	I, MIL	Low Power, Single or Dual Supply	5-45
PM239	1300	—	2	D, E, N	I, MIL	Low Power, Dual Supply	5-45

Package Options: D = Hermetic DIP, Ceramic or Plastic Leadless Chip Carrier; E = Ceramic Flatpack; Q = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = 14-Lead Ceramic Flatpack; N = Hermetic Molded Can DIP; P = Plastic or Epoxy Sealed DIP; Q = Cerpak; R = Small Outline, "SOIC" Package; S3 = SOIC–Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-5/-71; U = TSOP—Thin Small Outline Package; W = Ceramic Surface Mount; Y = Ceramic Leaded Chip Carrier; Z = Ceramic Dip Carrier.

Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, –40°C to +85°C (Some older products, –25°C to +85°C); M = Military, –55°C to +125°C. If a device has multiple grade offerings, the M = Hermetic DIP, Ceramic or Plastic Leadless Chip Carrier; P = Plastic or Epoxy Sealed DIP; Q = Cerpak; R = Small Outline, "SOIC" Package; S3 = SOIC–Shrink Small Outline Package; S = Plastic

Reference Data sheet reference number in this volume.

A = Analog Devices Military; ST = Special Linear Reference Manual. All other entries refer to this volume.

Fast, Precision Comparator

AD790

FEATURES

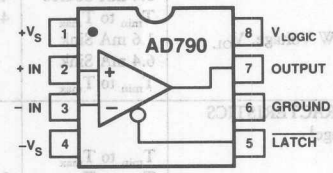
- 45 ns max Propagation Delay
- Single +5 V or Dual ±15 V Supply Operation
- CMOS or TTL Compatible Output
- 250 μV max Input Offset Voltage
- 500 μV max Input Hysteresis Voltage
- 15 V max Differential Input Voltage
- On-Board Latch
- 60 mW Power Dissipation
- Available in 8-Pin Plastic and Hermetic Cerdip Packages
  - MIL-STD-883B Processing Available
- Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

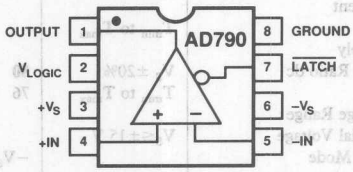
- Zero-Crossing Detectors
- Overvoltage Detectors
- Pulse-Width Modulators
- Precision Rectifiers
- Discrete A/D Converters
- Delta-Sigma Modulator A/Ds

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) and Cerdip (Q) Packages



8-Pin SOIC (R) Package



PRODUCT DESCRIPTION

The AD790 is a fast (45 ns), precise voltage comparator, with a number of features that make it exceptionally versatile and easy to use. The AD790 may operate from either a single +5 V supply or a dual ±15 V supply. In the single-supply mode, the AD790's inputs may be referred to ground, a feature not found in other comparators. In the dual-supply mode it has the unique ability of handling a maximum differential voltage of 15 V across its input terminals, easing their interfacing to large amplitude and dynamic signals.

This device is fabricated using Analog Devices' Complementary Bipolar (CB) process – which gives the AD790's combination of fast response time and outstanding input voltage resolution (1 mV max). To preserve its speed and accuracy, the AD790 incorporates a "low glitch" output stage that does not exhibit the large current spikes normally found in TTL or CMOS output stages. Its controlled switching reduces power supply disturbances that can feed back to the input and cause undesired oscillations. The AD790 also has a latching function which makes it suitable for applications requiring synchronous operation.

The AD790 is available in five performance grades. The AD790J and the AD790K are rated over the commercial temperature range of 0 to +70°C. The AD790A and AD790B are rated over the industrial temperature range of −40°C to +85°C. The AD790S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

PRODUCT HIGHLIGHTS

1. The AD790's combination of speed, precision, versatility and low cost makes it suitable as a general purpose comparator in analog signal processing and data acquisition systems.
2. Built-in hysteresis and a low-glitch output stage minimize the chance of unwanted oscillations, making the AD790 easier to use than standard open-loop comparators.
3. The hysteresis combined with a wide input voltage range enables the AD790 to respond to both slow, low level (e.g., 10 mV) signals and fast, large amplitude (e.g., 10 V) signals.
4. A wide variety of supply voltages are acceptable for operation of the AD790, ranging from single +5 V to dual +5 V/ −12 V, ±5 V, or +5 V/±15 V supplies.
5. The AD790's power dissipation is the lowest of any comparator in its speed range.
6. The AD790's output swing is symmetric between V_{LOGIC} and ground, thus providing a predictable output under a wide range of input and output conditions.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Parameter	Conditions	AD790J/A Min	AD790J/A Typ	AD790J/A Max	AD790K/B Min	AD790K/B Typ	AD790K/B Max	AD790S Min	AD790S Typ	AD790S Max	Units
RESPONSE CHARACTERISTIC	100 mV Step										
Propagation Delay, t_{PD}	5 mV Overdrive		40	45		40	45		40	45	ns
	T_{min} to T_{max}			45/50			45/50			60	ns
OUTPUT CHARACTERISTICS											
Output HIGH Voltage, V_{OH}	1.6 mA Source		4.65			4.65			4.65		
	6.4 mA Source	**4.3**	4.45		**4.3**	4.45		**4.3**	4.45		V
	T_{min} to T_{max}	4.3/**4.3**			**4.3**			**4.3**			V
Output LOW Voltage, V_{OL}	1.6 mA Sink		0.35			0.35			0.35		V
	6.4 mA Sink		0.44	**0.5**		0.44	**0.5**		0.44	**0.5**	V
	T_{min} to T_{max}			0.5/**0.5**			**0.5**			**0.5**	V
INPUT CHARACTERISTICS											
Offset Voltage[1]			0.2	**1.0**		0.05	**0.25**		0.2	**1.0**	mV
	T_{min} to T_{max}			1.5			**0.5**			**1.5**	mV
Hysteresis[2]	T_{min} to T_{max}	0.3	0.4	0.6	**0.3**	0.4	**0.5**	**0.3**	0.4	**0.65**	mV
Bias Current	Either Input		2.5	5		1.8	**3.5**		2.5	5	μA
	T_{min} to T_{max}			6.5			**4.5**			7	μA
Offset Current			0.04	**0.25**		0.02	**0.15**		0.04	**0.25**	μA
	T_{min} to T_{max}			0.3			**0.2**			**0.4**	μA
Power Supply											
Rejection Ratio dc	V_S ±20%	**80**	90		**88**	100		**80**	90		dB
	T_{min} to T_{max}	76	88		**85**	93		**76**	85		dB
Input Voltage Range											
Differential Voltage	V_S≤±15 V			**±V_S**			**±V_S**			**±V_S**	V
Common Mode		$-V_S$		$+V_S-2$ V	$-V_S$		$+V_S-2$ V	$-V_S$		$+V_S-2$ V	V
Common Mode											
Rejection Ratio	−10 V<V_{CM} <+10 V	**80**	95		**88**	105		**80**	95		dB
	T_{min} to T_{max}	76	90		**85**	100		**76**	88		dB
Input Impedance			20‖2			20‖2			20‖2		MΩ‖pF
LATCH CHARACTERISTICS											
Latch Hold Time, t_H			25	35		25	35		25	35	ns
Latch Setup Time, t_S			5	10		5	10		5	10	ns
LOW Input Level,V_{IL}	T_{min} to T_{max}			0.8			**0.8**			**0.8**	V
HIGH Input Level, V_{IH}	T_{min} to T_{max}	1.6			**1.6**			**1.6**			V
Latch Input Current			2.3	5		2.3	3.5		2.3	5	μA
	T_{min} to T_{max}			7			5			8	μA
SUPPLY CHARACTERISTICS											
Diff Supply Voltage[3]	V_{LOGIC} = 5 V										
	T_{min} to T_{max}	4.5		33	**4.5**		**33**	**4.7**		**33**	V
Logic Supply	T_{min} to T_{max}	4.0		7	**4.0**		**7**	**4.2**		**7**	V
Quiescent Current											
$+V_S$	$+V_S$ = 15 V		8	**10**		8	**10**		8	**10**	mA
$-V_S$	$-V_S$ = −15 V		4	5		4	5		4	5	mA
V_{LOGIC}	V_{LOGIC} = 5 V		2	**3.3**		2	**3.3**		2	**3.3**	mA
Power Dissipation				**242**			**242**			**242**	mW
TEMPERATURE RANGE											
Rated Performance	T_{min} to T_{max}	0 to +70/−40 to +85			0 to +70/−40 to +85			−55 to +125			°C

NOTES

[1]Defined as the average of the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[2]Defined as half the magnitude between the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[3]+V_S must be no lower than (V_{LOGIC} −0.5 V) in any supply operating conditions, except during power up.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final test.

Specifications subject to change without notice.

Parameter	Conditions	AD790J/A Min	AD790J/A Typ	AD790J/A Max	AD790K/B Min	AD790K/B Typ	AD790K/B Max	AD790S Min	AD790S Typ	AD790S Max	Units
RESPONSE CHARACTERISTIC	100 mV Step										
Propagation Delay, t_{PD}	5 mV Overdrive		45	50		45	50		45	50	ns
	T_{min} to T_{max}			50/60			50/60			65	ns
OUTPUT CHARACTERISTICS											
Output HIGH Voltage, V_{OH}	1.6 mA Source		4.65			4.65			4.65		
	6.4 mA Source	**4.3**	4.45		**4.3**	4.45		**4.3**	4.45		V
	T_{min} to T_{max}	4.3			**4.3**			**4.3**			V
Output LOW Voltage, V_{OL}	1.6 mA Sink		0.35			0.35			0.35		V
	6.4 mA Sink		0.44	**0.5**		0.44	**0.5**		0.44	**0.5**	V
	T_{min} to T_{max}			0.5			**0.5**			**0.5**	V
INPUT CHARACTERISTICS											
Offset Voltage[2]			0.45	**1.5**		0.35	**0.6**		0.45	**1.5**	mV
	T_{min} to T_{max}			2.0			**0.85**			**2.0**	mV
Hysteresis[3]	T_{min} to T_{max}	0.3	0.5	0.75	**0.3**	0.5	**0.65**	**0.3**	0.7	**1.0**	mV
Bias Current	Either Input		2.7	5		2.0	**3.5**		2.7	5	μA
	T_{min} to T_{max}			7			5			**8**	μA
Offset Current			0.04	**0.25**		0.02	**0.15**		0.04	**0.25**	μA
	T_{min} to T_{max}			0.3			**0.2**			**0.4**	μA
Power Supply											
Rejection Ratio dc	4.5 V≤V_S≤5.5 V	**80**	90		**86**	100		**80**	90		dB
	T_{min} to T_{max}	**76/76**	88		**82**	93		**76**	85		dB
Input Voltage Range											
Differential Voltage				**±V_S**			**±V_S**			**±V_S**	V
Common Mode		0		+V_S−2 V	0		+V_S−2 V	0		+V_S−2 V	V
Input Impedance			20‖2			20‖2			20‖2		MΩ‖pF
LATCH CHARACTERISTICS											
Latch Hold Time, t_H			25	35		25	35		25	35	ns
Latch Setup Time, t_S			5	10		5	10		5	10	ns
LOW Input Level, V_{IL}	T_{min} to T_{max}			0.8			**0.8**			**0.8**	V
HIGH Input Level, V_{IH}	T_{min} to T_{max}	1.6			**1.6**			**1.6**			V
Latch Input Current			2.3	5		2.3	3.5		2.3	5	μA
	T_{min} to T_{max}			7			5			**8**	μA
SUPPLY CHARACTERISTICS											
Supply Voltage[4]	T_{min} to T_{max}	4.5		7	4.5		**7**	**4.7**		**7**	V
Quiescent Current			10	**12**		10	**12**		10	**12**	mA
Power Dissipation				**60**			**60**			**60**	mW
TEMPERATURE RANGE											
Rated Performance	T_{min} to T_{max}	0 to +70/−40 to +85			0 to +70/−40 to +85			−55 to +125			°C

NOTES

[1]Pin 1 tied to Pin 8, and Pin 4 tied to Pin 6.

[2]Defined as the average of the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[3]Defined as half the magnitude between the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[4]$-V_S$ must not be connected above ground.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final test.

ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage	±18 V
Internal Power Dissipation[2]	500 mW
Differential Input Voltage	±16.5 V
Output Short Circuit Duration	Indefinite
Storage Temperature Range	
(N, R)	−65°C to +125°C
(Q)	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	+300°C
Logic Supply Voltage	7 V

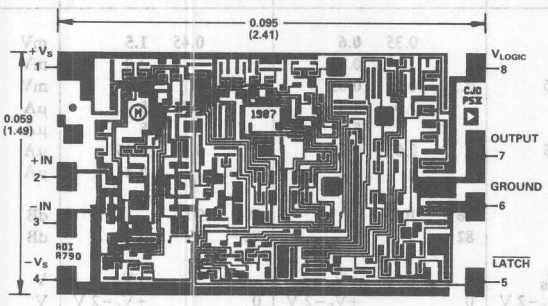
NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functionalop-eration of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal characteristics: plastic N-8 package: θ_{JA} = 90°C/watt; ceramic Q-8 package: θ_{JA} = 110°C/watt; θ_{JC} = 30°C/watt.
SOIC (R-8) package: θ_{JA} = 160°C/watt; θ_{JC} = 42°C/watt.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).
Call factory for chip specifications.



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD790JN	0°C to +70°C	Plastic DIP	N-8
AD790JR	0°C to +70°C	SOIC	R-8
AD790JR-REEL	0°C to +70°C	Reel	
AD790KN	0°C to +70°C	Plastic DIP	N-8
AD790AQ	−40°C to +85°C	Cerdip	Q-8
AD790BQ	−40°C to +85°C	Cerdip	Q-8
AD790SQ	−55°C to +125°C	Cerdip	Q-8
AD790SQ/883B	−55°C to +125°C	Cerdip	Q-8
AD790S Chips	−55°C to +125°C	Die	

*For outline information see Package Information section.

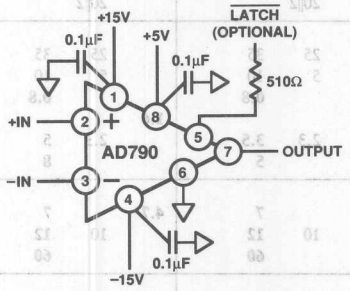


Figure 1. Basic Dual Supply Configuration (N, Q Package Pinout)

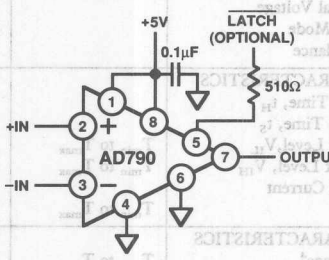


Figure 2. Basic Single Supply Configuration (N, Q Package Pinout)

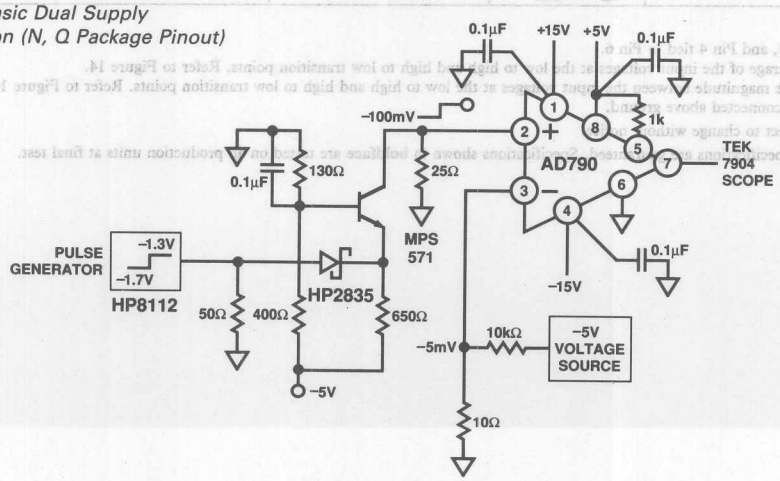


Figure 3. Response Time Test Circuit (N, Q Package Pinout)

Ultrafast TTL Comparators

AD9696/AD9698

FEATURES
4.5 ns Propagation Delay
200 ps Maximum Propagation Delay Dispersion
Single +5 V or ±5 V Supply Operation
Complementary Matched TTL Outputs

APPLICATIONS
High Speed Line Receivers
Peak Detectors
Window Comparators
High Speed Triggers
Ultrafast Pulse Width Discriminators

GENERAL DESCRIPTION

The AD9696 and AD9698 are ultrafast TTL-compatible voltage comparators able to achieve propagation delays previously possible only in high performance ECL devices. The AD9696 is a single comparator providing 4.5 ns propagation delay, 200 ps maximum delay dispersion and 1.7 ns setup time. The AD9698 is a dual comparator with equally high performance; both devices are ideal for critical timing circuits in such applications as ATE, communications receivers and test instruments.

Both devices allow the use of either a single +5 V supply or ±5 V supplies. The choice of supplies determines the common mode input voltage range available: −2.2 V to +3.7 V for ±5 V operation, +1.4 V to +3.7 V for single +5 V supply operation.

The differential input stage features high precision, with offset voltages which are less than 2 mV and offset currents less than 1 μA. A latch enable input is provided to allow operation in either sample-and-hold or track-and-hold applications.

The AD9696 and AD9698 are both available as commercial temperature range devices operating from ambient temperatures of 0°C to +70°C, and as extended temperature range devices for ambient temperatures from −55°C to +125°C. Both versions are available qualified to MIL-STD-883 class B.

Package options for the AD9696 include a 10-pin TO-100 metal can, an 8-pin ceramic DIP, an 8-pin plastic DIP, and an 8-lead small outline plastic package. The AD9698 is available in a 16-pin ceramic DIP, a 16-lead ceramic gullwing, a 16-pin plastic DIP, and a 16-lead small outline plastic package. Military qualified versions of the AD9696 come in the TO-100 can and ceramic DIP; the dual AD9698 comes in ceramic DIP.

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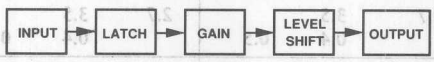
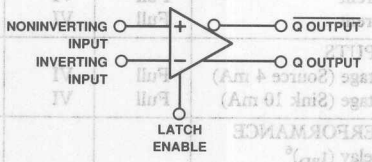
FUNCTIONAL BLOCK DIAGRAM

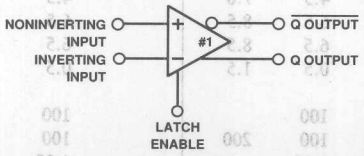
AD9696/AD9698 Architecture

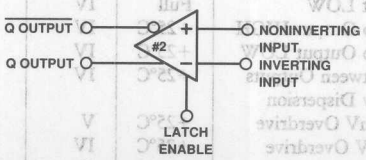


AD9696



AD9698





This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9696/AD9698—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S/-V_S$) . . . . . +7 V/−7 V
Input Voltage Range . . . . . ±5 V
Differential Input Voltage . . . . . 5.4 V
Latch Enable Voltage . . . . . −0.5 V to $+V_S$
Output Current (Continuous) . . . . . 20 mA
Power Dissipation . . . . . 600 mW

Operating Temperature Range[2]
AD9696/AD9698KH/KN/KQ/KR[3] . . . . . 0°C to +70°C
AD9696/AD9698TH/TQ[3] . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature
KH/KQ/TH/TQ Suffixes . . . . . +175°C
KN/KR Suffixes . . . . . +150°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages = −5.2 V and +5.0 V; load as specified in Note 4, unless otherwise indicated)

Parameter	Temp	Test Level	0°C to +70°C AD9696/AD9698 KH/KN/KQ/KR[3] Min	Typ	Max	−55°C to +125°C AD9696/AD9698 TH/TQ[3] Min	Typ	Max	Units
INPUT CHARACTERISTICS									
Input Offset Voltage[5]	+25°C	I		1.0	2.0		1.0	2.0	mV
	Full	VI			3.0			3.0	mV
Input Offset Voltage Drift	Full	V		10			10		µV/°C
Input Bias Current	+25°C	I		16	55		16	55	µA
	Full	VI			110			110	µA
Input Offset Current	+25°C	I		0.4	1.0		0.4	1.0	µA
	Full	VI			1.3			1.3	µA
Input Capacitance	+25°C	V		3			3		pF
Input Voltage Range									
±5.0 V	Full	VI	−2.2		+3.7	−2.2		+3.7	V
+5.0 V	Full	VI	+1.4		+3.7	+1.4		+3.7	V
Common Mode Rejection Ratio									
±5.0 V	Full	VI	80	85		80	85		dB
+5.0 V	Full	VI	57	63		57	63		dB
LATCH ENABLE INPUT									
Logic "1" Voltage Threshold	Full	VI	2.0			2.0			V
Logic "0" Voltage Threshold	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			10			10	µA
Logic "0" Current	Full	VI			1			1	µA
DIGITAL OUTPUTS									
Logic "1" Voltage (Source 4 mA)	Full	VI	2.7	3.5		2.7	3.5		V
Logic "0" Voltage (Sink 10 mA)	Full	VI		0.4	0.5		0.4	0.5	V
SWITCHING PERFORMANCE									
Propagation Delay (t_{PD})[6]									
Input to Output HIGH	Full	IV		4.5	7.0		4.5	7.0	ns
Input to Output LOW	Full	IV		4.5	7.0		4.5	7.0	ns
Latch Enable to Output HIGH	+25°C	IV		6.5	8.5		6.5	8.5	ns
Latch Enable to Output LOW	+25°C	IV		6.5	8.5		6.5	8.5	ns
Delta Delay Between Outputs	+25°C	IV		0.5	1.5		0.5	1.5	ns
Propagation Delay Dispersion									
20 mV to 100 mV Overdrive	+25°C	V		100			100		ps
100 mV to 1.0 V Overdrive	+25°C	IV		100	200		100	200	ps
Rise Time[11]	+25°C	V		1.85			1.85		ns
Fall Time[11]	+25°C	V		1.35			1.35		ns
Latch Enable									
Pulse Width [$t_{PW(E)}$]	+25°C	IV	3.5	2.5		3.5	2.5		ns
Setup Time (t_S)	+25°C	IV	3	1.7		3	1.7		ns
Hold Time (t_H)	+25°C	IV	3	1.9		3	1.9		ns

Parameter	Temp	Test Level	0°C to +70°C AD9696/AD9698 KH/KN/KQ/KR[3] Min	Typ	Max	−55°C to +125°C AD9696/AD9698 TH/TQ[3] Min	Typ	Max	Units
POWER SUPPLY[7]									
Positive Supply Current[8]									(+5.0 V)
AD9696	Full	VI		26	32		26	32	mA
AD9698	Full	VI		52	64		52	64	mA
Negative Supply Current[9]									(−5.2 V)
AD9696	Full	VI		2.5	4.0		2.5	4.0	mA
AD9698	Full	VI		5.0	8.0		5.0	8.0	mA
Power Dissipation									
AD9696 +5.0 V	Full	V		130			130		mW
AD9696 ±5.0 V	Full	V		146			146		mW
AD9698 +5.0 V	Full	V		260			260		mW
AD9698 ±5.0 V	Full	V		292			292		mW
Power Supply Rejection Ratio[10]	+25°C	VI	70			70			dB
	Full	VI	65			65			dB

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances:

AD9696 Metal Can	θ_{JA} = 170°C/W	θ_{JC} = 50°C/W
AD9696 Ceramic DIP	θ_{JA} = 110°C/W	θ_{JC} = 20°C/W
AD9696 Plastic DIP	θ_{JA} = 160°C/W	θ_{JC} = 30°C/W
AD9696 Plastic SOIC	θ_{JA} = 180°C/W	θ_{JC} = 30°C/W
AD9698 Ceramic DIP	θ_{JA} = 90°C/W	θ_{JC} = 25°C/W
AD9698 Plastic DIP	θ_{JA} = 100°C/W	θ_{JC} = 20°C/W
AD9698 Plastic SOIC	θ_{JA} = 120°C/W	θ_{JC} = 20°C/W

[3]Suffixes KH and TH apply only to model AD9696; AD9698 not available in metal can.

[4]Load circuit has 420 Ω from $+V_S$ to output; 460 Ω from output to ground.

[5]$R_S \leq 100\ \Omega$.

[6]Propagation delays measured with 100 mV pulse; 10 mV overdrive.

[7]Supply voltages should remain stable within ±5% for normal operation.

[8]Specification applies to both +5 V and ±5 V supply operation.

[9]Specification applies to only ±5 V supply operation.

[10]Measured with nominal values ±5% of $+V_S$ and $-V_S$.

[11]Although fall time is faster than rise time, the complementary outputs cross at midpoint of logic swing because of delay on start of falling edge.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Package	Temperature	Package Option[1]
AD9696KH	TO-100 Can	0°C to +70°C	H-10A
AD9696KN	Plastic DIP	0°C to +70°C	N-8
AD9696KR	SOIC	0°C to +70°C	R-8
AD9696KQ	Cerdip	0°C to +70°C	Q-8
AD9696TH	TO-100 Can	−55°C to +125°C	H-10A
AD9696TQ	Cerdip	−55°C to +125°C	Q-8
AD9696TZ/883B[2]	Gullwing	−55°C to +125°C	Z-8A
AD9698KN	Plastic DIP	0°C to +70°C	N-16
AD9698KR	SOIC	0°C to +70°C	R-16A
AD9698KQ	Cerdip	0°C to +70°C	Q-16
AD9698TQ	Cerdip	−55°C to +125°C	Q-16
AD9698TZ/883B[3]	Gullwing	−55°C to +125°C	Z-16

NOTES

[1]H = Hermetic Metal Can, N = Plastic DIP, Q = Cerdip, R = Small Outline (SOIC), Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.

[2]Refer to AD9696TZ/883B military data sheet.

[3]Refer to AD9698TZ/883B military data sheet.

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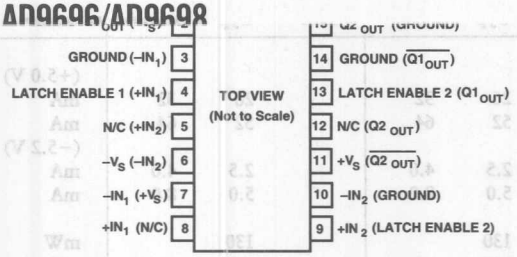
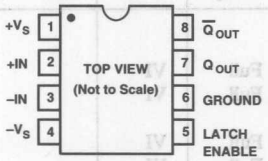
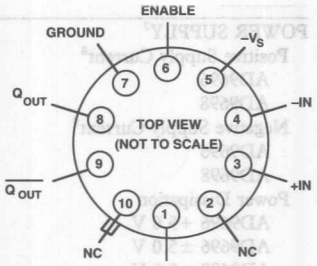


AD9698KN/KQ/TQ
[AD9698KR/TZ PINOUTS SHOWN IN ( )]



AD9696KN/KR/KQ/TQ/TZ



AD9696KH/TH

PIN DESCRIPTIONS

Name	Function
$Q1_{OUT}$	One of two complementary outputs. $Q1_{OUT}$ will be at logic HIGH if voltage at $+IN_1$ is greater than voltage at $-IN_1$ and LATCH ENABLE 1 is at logic LOW.
$\overline{Q1_{OUT}}$	One of two complementary outputs. $\overline{Q1_{OUT}}$ will be at logic HIGH if voltage at $-IN_1$ is greater than voltage at $+IN_1$ and LATCH ENABLE 1 is at logic LOW.
GROUND	Analog and digital ground return. All GROUND pins should be connected together and to a low impedance ground plane near the comparator.
LATCH ENABLE 1	Output at $Q1_{OUT}$ will track differential changes at the inputs when LATCH ENABLE 1 is at logic LOW. When LATCH ENABLE 1 is at logic HIGH, the output at $Q1_{OUT}$ will reflect the input state at the application of the latch command, delayed by the Latch Enable Setup Time (t_S). Since the architecture of the input stage (see block diagram) is faster than the logic of the latch stage, data will typically be latched if applied to the comparator(s) within 1.7 ns after the latch. This is the Setup Time (t_S); for guaranteed performance, t_S must be 3 ns.
N/C	No internal connection to comparator.
$-V_S$	Negative power supply connection; nominally −5.2 V.
$-IN_1$	Inverting input of differential input stage for Comparator #1.
$+IN_1$	Noninverting input of differential input stage for Comparator #1.
$+IN_2$	Noninverting input of differential input stage for Comparator #2.
$-IN_2$	Inverting input of differential input stage for Comparator #2.
$+V_S$	Positive power supply connection; nominally +5 V.
LATCH ENABLE 2	Output at $Q2_{OUT}$ will track differential changes at the inputs when LATCH ENABLE 2 is at logic LOW. When LATCH ENABLE 2 is at logic HIGH, the output at $Q2_{OUT}$ will reflect the input state at the application of the latch command, delayed by the Latch Enable Setup Time (t_S). Since the architecture of the input stage (see block diagram) is faster than the logic of the latch stage, data will typically be latched if applied to the comparator(s) within 1.7 ns after the latch. This is the Setup Time (t_S); for guaranteed performance, t_S must be 3 ns.
$\overline{Q2_{OUT}}$	One of two complementary outputs. $\overline{Q2_{OUT}}$ will be at logic HIGH if voltage at $-IN_2$ is greater than voltage at $+IN_2$ and LATCH ENABLE 2 is at logic LOW.
$Q2_{OUT}$	One of two complementary outputs. $Q2_{OUT}$ will be at logic HIGH if voltage at $+IN_2$ is greater than voltage at $-IN_2$ and LATCH ENABLE 2 is at logic LOW.

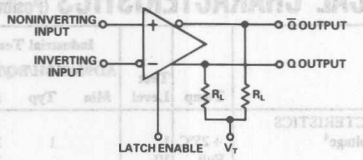
Ultrafast Comparators

AD96685/AD96687

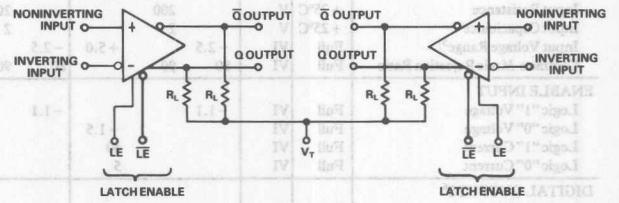
FEATURES
Fast: 2.5ns Propagation Delay
Low Power: 118mW per Comparator
Packages: DIP, TO-100, SOIC, PLCC
Power Supplies: +5V, −5.2V
Logic Compatibility: ECL
MIL-STD-883 Versions Available
50ps Delay Dispersion

APPLICATIONS
High Speed Triggers
High Speed Line Receivers
Threshold Detectors
Window Comparators
Peak Detectors

AD96685 FUNCTIONAL BLOCK DIAGRAM



AD96687 FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω – 200Ω CONNECTED TO −2.0V, OR 200Ω – 2000Ω

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GENERAL DESCRIPTION

The AD96685 and AD96687 are ultrafast voltage comparators. The AD96685 is a single comparator with 2.5ns propagation delay; the AD96687 is an equally fast dual comparator. Both devices feature 50ps propagation delay dispersion which is a particularly important characteristic of high speed comparators. It is a measure of the difference in propagation delay under differing overdrive conditions.

A fast, high precision differential input stage permits consistent propagation delay with a wide variety of signals in the common-mode range from −2.5V to +5V. Outputs are complementary digital signals fully compatible with ECL 10K and 10KH logic families. The outputs provide sufficient drive current to directly drive transmission lines terminated in 50Ω to −2V. A level-sensitive latch input is included which permits tracking, track-hold, or sample-hold modes of operation.

The AD96685 and AD96687 are available in both industrial, −25°C to +85°C, and military temperature ranges. Industrial range devices are available in 16-pin DIP, SOIC, and 20-lead PLCC; additionally, the AD96685 is available in a 10-pin, TO-100 metal can. Both devices are available qualified to MIL-STD-883, Class B in 16-pin ceramic DIP and 20-lead ceramic LCC; the TO-100 version of the AD96685 is also mil-qualified.

ORDERING GUIDE

Device	Type	Temperature Range	Description	Package Options*
AD96685BH	Single	−25°C to +85°C	10-Pin Can, Industrial	H-10A
AD96685BP	Single	−25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96685BQ	Single	−25°C to +85°C	16-Pin DIP, Industrial	Q-16
AD96685BR	Single	−25°C to +85°C	16-Pin SOIC, Industrial	R-16
AD96685TE	Single	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD96685TH	Single	−55°C to +125°C	10-Pin Can, Extended Temperature	H-10A
AD96685TQ	Single	−55°C to +125°C	16-Pin DIP, Extended Temperature	Q-16
AD96687BP	Dual	−25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96687BQ	Dual	−25°C to +85°C	16-Pin DIP, Industrial	Q-16
AD96687BR	Dual	−25°C to +85°C	16-Pin SOIC, Industrial	R-16
AD96687TE	Dual	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD96687TQ	Dual	−55°C to +125°C	16-Pin DIP, Extended Temperature	Q-16

*For outline information see Package Information section.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD96685/AD96687 — SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +6.5V
Negative Supply Voltage ($-V_S$) . . . . . −6.5V
Input Voltage Range[2] . . . . . ±5V
Differential Input Voltage 5.5V
Latch Enable Voltage . . . . . $-V_S$ to 0V
Output Current 30mA

Operating Temperature Range[3]
AD96685/87/BH/BQ/BP/BR . . . . . −25°C to +85°C
AD96685/87/TE/TH/TQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −55°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Positive Supply Voltage = +5.0V; Negative Supply Voltage = −5.2V, unless otherwise stated)

			Industrial Temp. Range −25°C to +85°C						Extended Temp. Range −55°C to +125°C						
			AD96685BH/BQ/BP/BR			AD96687BQ/BP/BR			AD96685TE/TH/TQ			AD96687TE/TQ			
Parameter	Temp	Test Level	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
INPUT CHARACTERISTICS															
Input Offset Voltage[4]	+25°C	I		1	2		1	2		1	2		1	2	mV
	Full	VI			3			3			3			3	mV
Input Offset Drift	Full	V		20			20			20			20		µV/°C
Input Bias Current	+25°C	I		7	10		7	10		7	10		7	10	µA
	Full	VI			13			13			16			16	µA
Input Offset Current	+25°C	I		0.1	1.0		0.1	1.0		0.1	1.0		0.1	1.0	µA
	Full	VI			1.2			1.2			1.2			1.2	µA
Input Resistance	+25°C	V		200			200			200			200		kΩ
Input Capacitance	+25°C	V		2			2			2			2		pF
Input Voltage Range[5]	Full	VI	−2.5		+5.0	−2.5		+5.0	−2.5		+5.0	−2.5		+5.0	V
Common-Mode Rejection Ratio	Full	VI	80	90		80	90		80	90		80	90		dB
ENABLE INPUT															
Logic "1" Voltage	Full	VI	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5			−1.5			−1.5	V
Logic "1" Current	Full	VI			40			40			40			40	µA
Logic "0" Current	Full	VI			5			5			5			5	µA
DIGITAL OUTPUTS[6]															
Logic "1" Voltage	Full	VI	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5			−1.5			−1.5	V
SWITCHING PERFORMANCE[6]															
Propagation Delays[7]															
Input to Output HIGH	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Input to Output LOW	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Latch Enable to Output HIGH	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Latch Enable to Output LOW	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Dispersion[8]	+25°C	V		50			50			50			50		ps
Latch Enable															
Minimum Pulse Width	+25°C	IV		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	ns
Minimum Setup Time	+25°C	IV		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
Minimum Hold Time	+25°C	IV		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
POWER SUPPLY[9]															
Positive Supply Current (+5.0V)	Full	VI		8	9		15	18		8	9		15	18	mA
Negative Supply Current (−5.2V)	Full	VI		15	18		31	36		15	18		31	36	mA
Power Supply Rejection Ratio[10]	Full	VI	60	70		60	70		60	70		60	70		dB

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Under no circumstances should the input voltages exceed the supply voltages.

[3]Typical thermal impedances . . .

AD96685 Metal Can	$\theta_{JA} = 172°C/W; \theta_{JC} = 52°C/W$
AD96685 Ceramic	$\theta_{JA} = 115°C/W; \theta_{JC} = 57°C/W$
AD96685 LCC	$\theta_{JA} = 172°C/W; \theta_{JC} = 65°C/W$
AD96685 SOIC	$\theta_{JA} = 170°C/W; \theta_{JC} = 60°C/W$
AD96685 PLCC	$\theta_{JA} = 88°C/W; \theta_{JC} = 45°C/W$
AD96687 Ceramic	$\theta_{JA} = 115°C/W; \theta_{JC} = 57°C/W$
AD96687 LCC	$\theta_{JA} = 82°C/W; \theta_{JC} = 31°C/W$
AD96687 SOIC	$\theta_{JA} = 92°C/W; \theta_{JC} = 47°C/W$
AD96687 PLCC	$\theta_{JA} = 81°C/W; \theta_{JC} = 45°C/W$

[4]$R_S = 100\Omega$.

[5]Input Voltage Range can be extended to −3.3V if $-V_S = -6.0V$.

[6]Outputs terminated through 50Ω to −2.0V.

[7]Propagation delays measured with 100mV pulse (10mV overdrive), to 50% transition point of the output.

[8]Change in propagation Delay from 100mV to 1V input overdrive.

[9]Supply voltages should remain stable within ±5% for normal operation.

[10]Measured at ±5% of $+V_S$ and $-V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C; 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

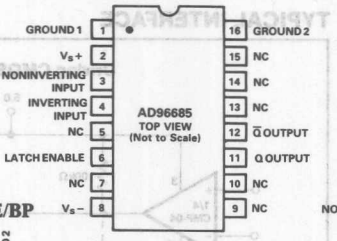
FUNCTIONAL DESCRIPTION

Pin Name	Description
$+V_S$	– Positive supply terminal, nominally +5.0V.
NONINVERTING INPUT	– Noninverting analog input of the differential input stage. The NONINVERTING INPUT must be driven in conjunction with the INVERTING INPUT.
INVERTING INPUT	– Inverting analog input of the differential input stage. The INVERTING INPUT must be driven in conjunction with the NONINVERTING INPUT.
LATCH ENABLE	– In the "compare" mode (logic HIGH), the output will track changes at the input of the comparator. In the "latch" mode (logic LOW), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. $\overline{\text{LATCH ENABLE}}$ must be driven in conjunction with LATCH ENABLE for the AD96687.
$\overline{\text{LATCH ENABLE}}$	– In the "compare" mode (logic LOW), the output will track changes at the input of the comparator. In the "latch" mode (logic HIGH), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. LATCH ENABLE must be driven in conjunction with $\overline{\text{LATCH ENABLE}}$ for the AD96687.
$-V_S$	– Negative supply terminal, nominally −5.2V.
Q	– One of two complementary outputs. Q will be at logic HIGH if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ (AD96687 only) for additional information.
$\overline{Q}$	– One of two complementary outputs. $\overline{Q}$ will be at logic LOW if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ (AD96687 only) for additional information.
GROUND 1	– One of two grounds, but primarily associated with the digital ground. Both grounds should be connected together near the comparator.
GROUND 2	– One of two grounds, but primarily associated with the analog ground. Both grounds should be connected together near the comparator.

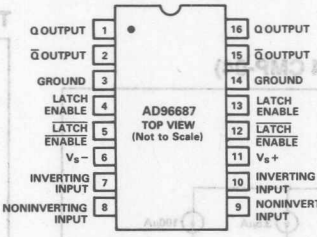
12

PIN DESIGNATIONS

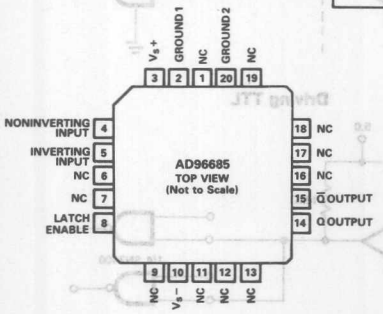
AD96685BQ/TQ/BR



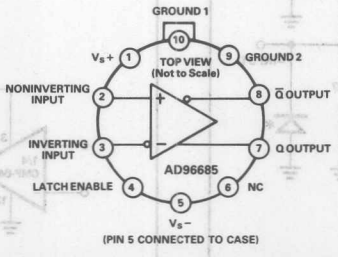
AD96687BQ/TQ/BR



AD96685TE/BP

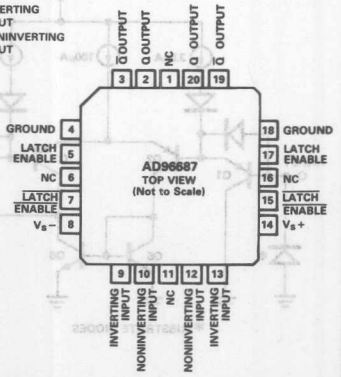


AD96685BH/TH



(PIN 5 CONNECTED TO CASE)

AD96687TE/BP



FEATURES

- **High Gain ..... 200V/mV Typ**
- **Single or Dual Supply Operation**
- **Input Voltage Range Includes Ground**
- **Low Power Consumption (1.5mW/Comparator)**
- **Low Input Bias Current ..... 100nA Max**
- **Low Input Offset Current ..... 10nA Max**
- **Low Offset Voltage ..... 1mV Max**
- **Low Output Saturation Voltage ..... 250mV @ 4mA**
- **Logic Output Compatible with TTL, DTL, ECL, MOS and CMOS**
- **Directly Replaces LM139/239/339 Comparators**
- **Available in Die Form**

GENERAL DESCRIPTION

Four precision independent comparators comprise the CMP-04. Performance highlights include a very low offset voltage, low output saturation voltage and high gain in a single supply design. The input voltage range includes ground for single supply operation and V– for split supplies. A low power supply current of 2mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

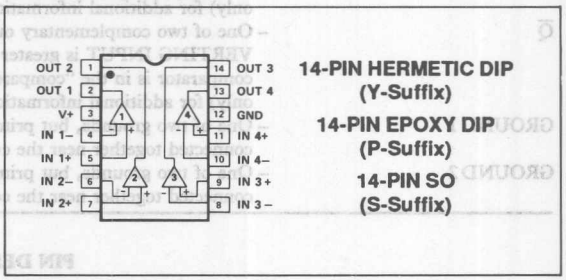
ORDERING INFORMATION †

T_A = +25°C	PACKAGE			
V_{OS} (mV)	CERDIP 14-PIN	PLASTIC 14-PIN	SO 14-PIN	OPERATING TEMPERATURE RANGE
1	CMP04BY*	–	–	MIL
1	CMP04FY	CMP04FP	CMP04FS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

PIN CONNECTIONS

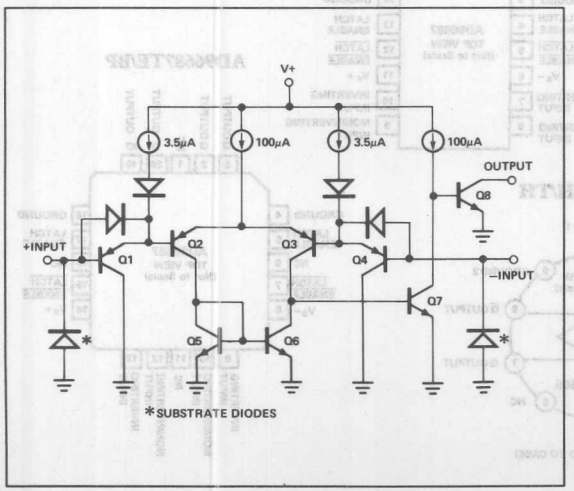


14-PIN HERMETIC DIP (Y-Suffix)

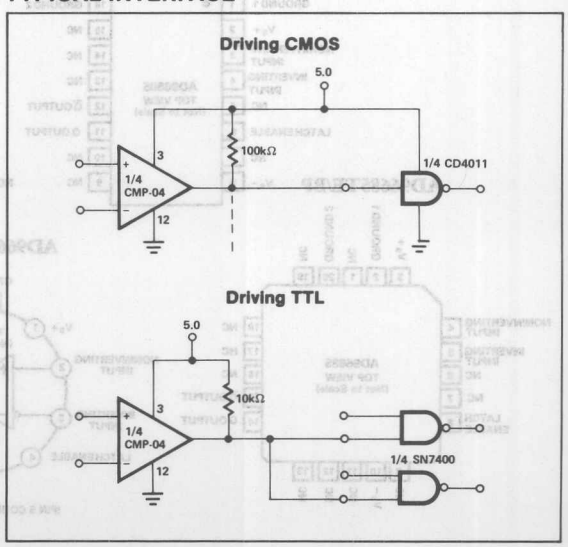
14-PIN EPOXY DIP (P-Suffix)

14-PIN SO (S-Suffix)

SIMPLIFIED SCHEMATIC (1/4 CMP-04)



TYPICAL INTERFACE



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... 36V or ±18V
Differential Input Voltage ..... $36V_{DC}$
Input Voltage ..... –0.3V to +36V
Operating Temperature Range
CMP-04FY ..... –40°C to +85°C
CMP-04BY ..... –55°C to +125°C
CMP-04FP, FS ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
P-Suffix) ..... –65°C to +125°C
Input Current (V_{IN} < –3.0V) 50mA
Output Short-Circuit to GND ..... Continuous
Lead Temperature (Soldering, 60 sec) ..... 300°C

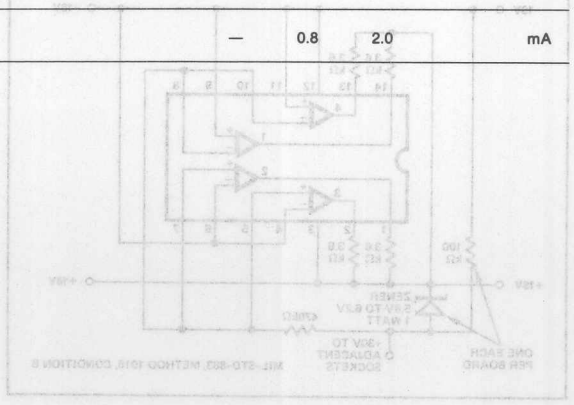
PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Z)	110	26	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SO (S)	120	36	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V+ = +5V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04B/F MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	R_S = 0Ω, R_L = 5.1kΩ V_O = 1.4V, (Note 1)	—	0.4	1	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ R_L = 5.1kΩ V_O = 1.4V	—	2	10	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$	—	25	100	nA
Voltage Gain	A_V	$R_L \geq$ 15kΩ, V+ = 15V, (Note 5)	80	200	—	V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing V_{REF} = 1.4V, (Note 4) V_{RL} = 5V, R_L = 5.1kΩ	—	300	—	ns
Small-Signal Response Time	t_r	V_{IN} = 100mV Step, (Note 4) 5mV Overdrive V_{RL} = 5V, R_L = 5.1kΩ	—	1.3	—	µs
Input Voltage Range	CMVR	(Note 2)	0	—	V+ –1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	80	100	—	dB
Power Supply Rejection Ratio	PSRR	V+ = +5V to 18V, (Note 5)	80	100	—	dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq$ 1V, $V_{IN}(+)$ = 0, $I_{SINK} \leq$ 4mA	—	250	400	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq$ 1V, $V_{IN}(+)$ = 0, $V_O \leq$ 1.5V	6	16	—	mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq$ 1V, $V_{IN}(-)$ = 0, V_O = 30V	—	0.1	100	nA
Supply Current	I+	R_L = ∞, All Comps V+ = 30V	—	0.8	2.0	mA

NOTES:
1. At output switch point, V_O = 1.4V, R_S = 0Ω with V+ from 5V; and over the full input common-mode range (0V to V+ – 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ – 1.5V, but either or both inputs can go to +30V without damage.
3. $R_L \geq$ 15kΩ, V+ = 15V, V_{CM} = 1.5V to 13.5V.
4. Sample tested.
5. Guaranteed by design.



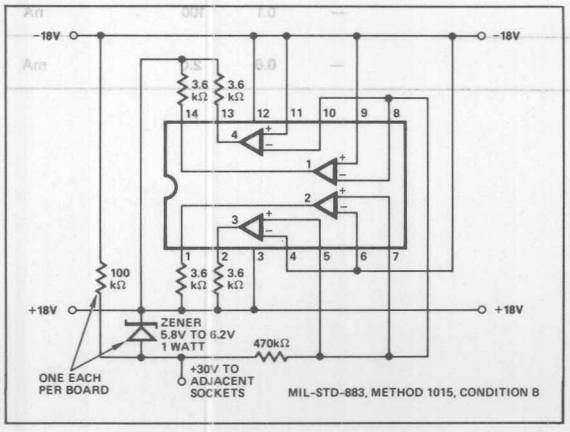
ELECTRICAL CHARACTERISTICS at V+ = +5V, −55°C ≤ T_A ≤ +125°C for CMP-04BY, −40°C ≤ T_A ≤ +85°C for CMP-04FY/FP/FS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04B/F (Note 3) MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	R_S = 0Ω, R_L = 5.1kΩ V_O = 1.4V, (Note 1)	—	1	2	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ R_L = 5.1kΩ V_O = 1.4V	—	4	20	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$	—	40	200	nA
Voltage Gain	A_V	R_L ≥ 15kΩ, V+ = 15V, (Note 5)	70	125	—	V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing V_{REF} = 1.4V, (Note 4) V_{RL} = 5V, R_L = 5.1kΩ	—	300	—	ns
Small-Signal Response Time	t_r	V_{IN} = 100mV Step, (Note 4) 5mV Overdrive V_{RL} = 5V, R_L = 5.1kΩ	—	1.3	—	µs
Input Voltage Range	CMVR	(Note 2)	0	—	V+ −1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	60	100	—	dB
Power Supply Rejection Ratio	PSRR	V+ = +5V to 18V	80	100	—	dB
Saturation Voltage	V_{OL}	$V_{IN}(-)$ ≥ 1V, $V_{IN}(+)$ = 0, I_{SINK} ≤ 4mA	—	250	700	mV
Output Sink Current	I_{SINK}	$V_{IN}(-)$ ≥ 1V, $V_{IN}(+)$ = 0, V_O ≤ 1.5V	5	16	—	mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+)$ ≥ 1V, $V_{IN}(-)$ = 0, V_O = 30V	—	0.1	200	nA
Supply Current	I+	R_L = ∞, All Comps V+ = 30V	—	1.2	3.0	mA

NOTES:

1. At output switch point, V_O = 1.4V, R_S = 0Ω with V+ from 5V; and over the full input common-mode range (0V to V+ − 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to +30V without damage.
3. R_L ≥ 15kΩ, V+ = 15V, V_{CM} = 1.5V to 13.5V.
4. Sample tested.
5. Guaranteed by design.

BURN-IN CIRCUIT



Matched Transistors
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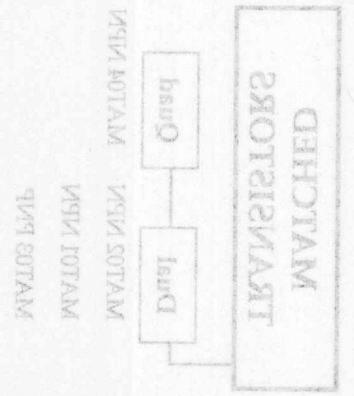
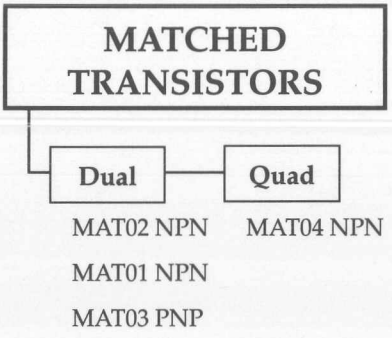
MAT02 – Low Noise, Matched Dual Monolithic Transistor	13–7
MAT03 – Low Noise, Matched Dual PNP Transistor	13–10
MAT04 – Matched Monolithic Quad Transistor	13–13



Selection Tree — Matched Transistors



Selection Guide—Matched Transistors

Model	Type	V_{OS} Max μV	TCV_{OS} Max μV/°C	hFE Min[1]	ΔhFE max %	en max nV/√Hz[2]	Package Options[3]	Temp Ranges[4]	Comments	Page[5]
MAT01	**Dual NPN**	**100**	**0.5**	**500**	**3**	**7.5**	**Q**	**M/**	**Low Cost**	**13–5**
MAT02	**Dual NPN**	**50**	**0.1**	**500**	**2**	**1**	**N**	**I, M/**	**Low Noise, Low r_{BE}**	**13–7**
MAT03	**Dual PNP**	**100**	**0.5**	**100**	**2**	**1**	**N**	**I, M/**	**Low Noise**	**13–10**
MAT04	**Quad NPN**	**200**	**1**	**300**	**2**	**2.5**	**N**	**I, M/**	**Low Cost**	**13–13**
SSM2210	Dual NPN	200	1	300	5	1	P	I	Low Cost, Audio	D
SSM2220	Dual PNP	200	1	80	6	1	R	I	Low Cost, Audio	D

[1]I_C = 1 mA
[2]$f_C \geq 100$ Hz
[3]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[4]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[5]D = Data Sheet. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Selection Guide—Matched Transistors

Model	Type	V_{os} Max μV	TCV$_{os}$ Max $\mu V/°C$	h_{FE} Min[1]	Δh_{FE} max %	C_{ob} max pF	Package Options[2]	Temp Ranges[3]	Comments	Page[4]
MAT01	Dual NPN	100	0.5	500	3	7.5	D	M	Low Cost	13-5
MAT02	Dual NPN	50	0.1	500	2	1	N	I, M	Low Noise, Low r_{bb}	13-7
MAT03	Dual PNP	100	0.5	100	2	1	N	I, M	Low Noise	13-10
MAT04	Quad NPN	300	1	300	2	2.5	N	I, M	Low Cost	13-13
SSM2210	Dual NPN	200	1	300	5	1	P	I	Low Cost, Audio	D
SSM2220	Dual PNP	200	1	80	6	1	R	I	Low Cost, Audio	D

I_C = 1 mA

$^{*}f_C \geq 100$ Hz

[1] Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic J-Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; S = SSOP—Shrink Small Outline Package; T = Thin Quad Flatpack; ST = Thin Quad Flatpack—Thin Small Outline Package; W = Hermetic Ceramic SOIC; Y = Shrink-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.

[2] Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, –40°C to +85°C (Some older products –25°C to +85°C); M = Military, –55°C to +125°C. If a device has military grade, the M designation will be followed by \ to indicate /883B, /Dsc, /JAN, /LCC, or /Proc.

[3] = Data Sheet. All letter codes refer to this volume.

Additional Type Data about Information in this volume.

ANALOG DEVICES

Matched Monolithic Dual Transistor

MAT01

FEATURES

- Low V_{OS} (V_{BE} Match) ..... 40μV Typ
  100μV Max
- Low TCV_{OS} ..... 0.5μV/° C Max
- High h_{FE} ..... 500 Min
- Excellent h_{FE} Linearity from 10nA to 10mA
- Low Noise Voltage ..... 0.23μV_{p-p} — 0.1Hz to 10Hz
- High Breakdown ..... 45V Min
- Available in Die Form

ORDERING INFORMATION†

T_A = 25° C V_{OS} MAX (mV)	PACKAGE	OPERATING TEMPERATURE RANGE
0.1	MAT01AH*	MIL
0.5	MAT01GH	MIL

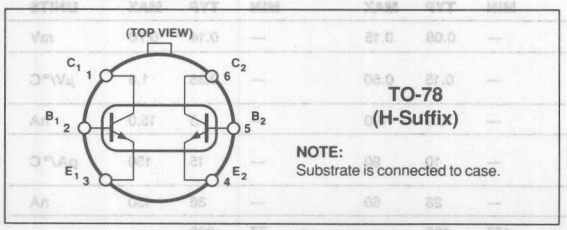
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The MAT-01 is a monolithic dual NPN transistor. An exclusive Silicon Nitride "Triple-Passivation" process provides excellent stability of critical parameters over both temperature and time. Matching characteristics include offset voltage of 40μV, temperature drift of 0.15μV/° C, and h_{FE} matching of 0.7%. Very high h_{FE} is provided over a six decade range of collector current, including an exceptional h_{FE} of 590 at a collector current of only 10nA. The high gain at low collector current makes the MAT-01 ideal for use in low-power, low-level input stages.

PIN CONNECTIONS



TO-78
(H-Suffix)

NOTE:
Substrate is connected to case.

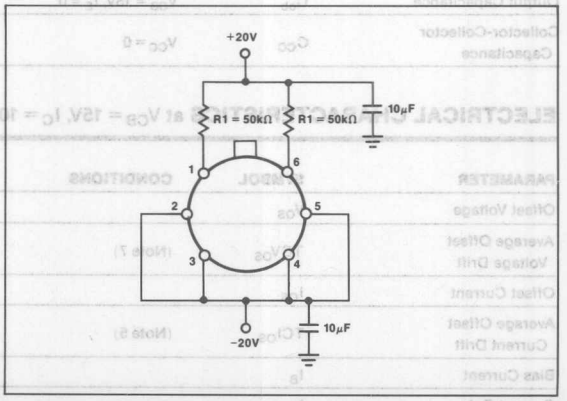
ABSOLUTE MAXIMUM RATINGS (Note 4)

Collector-Base Voltage (BV_{CBO})	
MAT-01AH, GH, N	45V
Collector-Emitter Voltage (BV_{CEO})	
MAT-01AH, GH, N	45V
Collector-Collector Voltage (BV_{CC})	
MAT-01AH, GH, N	45V
Emitter-Emitter Voltage (BV_{EE})	
MAT-01AH, GH, N	45V
Emitter-Base Voltage (BV_{EBO}) (Note 1)	5V
Collector Current (I_C)	25mA
Emitter Current (I_E)	25mA
Total Power Dissipation	
Case Temperature ≤ 40° C (Note 2)	1.8W
Ambient Temperature ≤ 70° C (Note 3)	500mW
Operating Ambient Temperature	−55° C to +125° C
Operating Junction Temperature	−55° C to +150° C
Storage Temperature	−65° C to +150° C
Lead Temperature (Soldering, 60 sec)	300° C
DICE Junction Temperature	−65° C to +150° C

NOTES:

1. Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure BV_{EBO} greater than the 5V rating shown.
2. Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4mW/° C for case temperatures above 40° C.
3. Rating applies to applications not using heat sinking; device in free air only. Derate linearly at 6.3mW/° C for ambient temperatures above 70° C.
4. Absolute maximum ratings apply to both DICE and packaged devices.

BURN-IN CIRCUIT



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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Breakdown Voltage	BV_{CEO}	$I_C = 100\mu A$	45	—	—	45	—	—	V
Offset Voltage	V_{OS}		—	0.04	0.1	—	0.10	0.5	mV
Offset Voltage Stability									
First Month	V_{OS}/Time	(Note 1)	—	2.0	—	—	2.0	—	μV/Mo
Long-Term		(Note 2)	—	0.2	—	—	0.2	—	
Offset Current	I_{OS}		—	0.1	0.6	—	0.2	3.2	nA
Bias Current	I_B		—	13	20	—	18	40	nA
Current Gain	h_{FE}	$I_C = 10nA$	—	590	—	—	430	—	
		$I_C = 10\mu A$	500	770	—	250	560	—	
		$I_C = 10mA$	—	840	—	—	610	—	
Current Gain Match	Δh_{FE}	$I_C = 10\mu A$	—	0.7	3.0	—	1.0	8.0	%
		$100nA \le I_C \le 10mA$	—	0.8	—	—	1.2	—	
Low Frequency Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.23	0.4	—	0.23	0.4	μV_{p-p}
Broadband Noise Voltage	e_{nRMS}	1Hz to 10kHz	—	0.60	—	—	0.60	—	μV_{RMS}
Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 3)	—	7.0	9.0	—	7.0	9.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 3)	—	6.1	7.6	—	6.1	7.6	
		$f_O = 1000Hz$ (Note 3)	—	6.0	7.5	—	6.0	7.5	
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \le V_{CB} \le 30V$	—	0.5	3.0	—	0.8	8.0	μV/V
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	$0 \le V_{CB} \le 30V$	—	2	15	—	3	70	pA/V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 30V$, $I_E = 0$ (Note 4)	—	15	50	—	25	200	pA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 30V$, $V_{BE} = 0$ (Notes 4, 6)	—	50	200	—	90	400	pA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = 30V$, (Note 6)	—	20	200	—	30	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 0.1mA$, $I_C = 1mA$	—	0.12	0.20	—	0.12	0.25	V
		$I_B = 1mA$, $I_C = 10mA$	—	0.8	—	—	0.8	—	
Gain-Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 10mA$	—	450	—	—	450	—	MHz
Output Capacitance	C_{ob}	$V_{CB} = 15V$, $I_E = 0$	—	2.8	—	—	2.8	—	pF
Collector-Collector Capacitance	C_{CC}	$V_{CC} = 0$	—	8.5	—	—	8.5	—	pF

ELECTRICAL CHARACTERISTICS at $V_{CB} = 15V$, $I_C = 10\mu A$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

			MAT-01AH			MAT-01GH			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}		—	0.06	0.15	—	0.14	0.70	mV
Average Offset Voltage Drift	TCV_{OS}	(Note 7)	—	0.15	0.50	—	0.35	1.8	μV/°C
Offset Current	I_{OS}		—	0.9	8.0	—	1.5	15.0	nA
Average Offset Current Drift	TCI_{OS}	(Note 5)	—	10	90	—	15	150	pA/°C
Bias Current	I_B		—	28	60	—	36	130	nA
Current Gain	h_{FE}		167	400	—	77	300	—	
Collector-Base Leakage Current	I_{CBO}	$T_A = 125°C$, $V_{CB} = 30V$, $I_E = 0$ (Note 4)	—	15	80	—	25	200	nA
Collector-Emitter Leakage Current	I_{CES}	$T_A = 125°C$, $V_{CE} = 30V$, $V_{BE} = 0$ (Notes 4, 6)	—	50	300	—	90	400	nA
Collector-Collector Leakage Current	I_{CC}	$T_A = 125°C$, $V_{CC} = 30V$ (Note 6)	—	30	200	—	50	400	nA

Low Noise, Matched Dual Monolithic Transistor

MAT02

FEATURES

- **Low Offset Voltage ..... 50μV Max**
- **Low Noise Voltage at 100Hz, 1mA ... 1.0nV/√Hz Max**
- **High Gain (h_{FE}) ..... 500 Min at I_C = 1mA**
  ..... 300 Min at I_C = 1μA
- **Excellent Log Conformance ..... $r_{BE} \simeq 0.3\Omega$**
- **Low Offset Voltage Drift ..... 0.1μV/° C Max**
- **Improved Direct Replacement for LM194/394**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE TO-78	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
50	MAT02AH*	–	MIL
50	MAT02EH	–	IND
150	–	MAT02BRC/883	MIL
150	MAT02FH	–	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

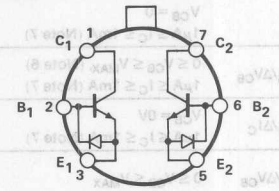
The design of the MAT-02 series of NPN dual monolithic transistors is optimized for very low noise, low drift, and low r_{BE}. Precision Monolithics' exclusive Silicon Nitride "Triple-Passivation" process stabilizes the critical device parameters over wide ranges of temperature and elapsed time. Also, the high current gain (h_{FE}) of the MAT-02 is maintained over a wide range of collector current. Exceptional characteristics of the MAT-02 include offset voltage of 50μV max (A/E grades) and 150μV max (B/F grades). Device performance is specified over the full military temperature range as well as at 25° C.

Input protection diodes are provided across the emitter-base junctions to prevent degradation of the device characteristics due to reverse-biased emitter current. The substrate is clamped to the most negative emitter by the parasitic isolation junction created by the protection diodes. This results in complete isolation between the transistors.

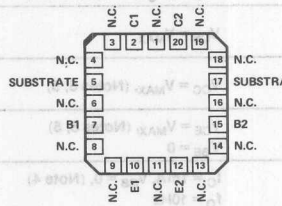
The MAT-02 should be used in any application where low noise is a priority. The MAT-02 can be used as an input stage to make an amplifier with noise voltage of less than 1.0nV/√Hz at 100Hz. Other applications, such as log/anti-log circuits, may use the excellent logging conformity of the MAT-02. Typical bulk resistance is only 0.3Ω to 0.4Ω. The MAT-02 electrical characteristics approach those of an ideal transistor when operated over a collector current range of 1μA to 10mA. For applications requiring multiple devices see MAT-04 Quad Matched Transistor data sheet.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PIN CONNECTIONS



TO-78
(H-Suffix)



MAT-02BRC/883
20-LEAD LCC
(RC-Suffix)

NOTE: Substrate is connected to case on TO-78 package. Substrate is normally connected to the most negative circuit potential, but can be floated.

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ABSOLUTE MAXIMUM RATINGS (Note 3)

Collector-Base Voltage (BV_{CBO})	40V
Collector-Emitter Voltage (BV_{CEO})	40V
Collector-Collector Voltage (BV_{CC})	40V
Emitter-Emitter Voltage (BV_{EE})	40V
Collector Current (I_C)	20mA
Emitter Current (I_E)	20mA
Total Power Dissipation	
Case Temperature ≤40°C (Note 1)	1.8W
Ambient Temperature ≤70°C (Note 2)	500mW
Operating Temperature Range	
MAT-02A, B	–55°C to +125°C
MAT-02E, F	–25°C to +85°C
Operating Junction Temperature	–55°C to +150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C
Junction Temperature	–65°C to +150°C

NOTES:

1. Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4mW/° C for case temperature above 40° C.
2. Rating applies to applications not using heat sinking; device in free air only. Derate linearly at 6.3mW/° C for ambient temperature above 70° C.
3. Absolute maximum ratings apply to both DICE and packaged devices.

MAT02

ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.

			MAT-02A/E			MAT-02B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Current Gain	h_{FE}	I_C = 1mA (Note 1)	500	605	—	400	605	—	
		I_C = 100μA	500	590	—	400	590	—	
		I_C = 10μA	400	550	—	300	550	—	
		I_C = 1μA	300	485	—	200	485	—	
Current Gain Match	Δh_{FE}	10μA ≤ I_C ≤ 1mA, (Note 2)	—	0.5	2	—	0.5	4	%
Offset Voltage	V_{OS}	V_{CB} = 0 1μA ≤ I_C ≤ 1mA (Note 7)	—	10	50	—	80	150	μV
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ V_{MAX}, (Note 6) 1μA ≤ I_C ≤ 1mA (Note 7)	—	10	25	—	10	50	μV
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0V 1μA ≤ I_C ≤ 1mA (Note 7)	—	5	25	—	5	50	μV
Offset Current Change vs V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ V_{MAX}	—	30	70	—	30	70	pA/V
Bulk Resistance	r_{BE}	10μA ≤ I_C ≤ 10mA (Note 3)	—	0.3	0.5	—	0.3	0.5	Ω
Collector-Base Leakage Current	I_{CBO}	V_{CB} = V_{MAX}	—	25	200	—	25	400	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = V_{MAX}, (Notes 3, 5)	—	35	200	—	35	400	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = V_{MAX}, (Notes 3, 5) V_{BE} = 0	—	35	200	—	35	400	pA
Noise Voltage Density	e_n	I_C = 1mA, V_{CB} = 0, (Note 4) f_O = 10Hz	—	1.6	2	—	1.6	3	nV/√Hz
		f_O = 100Hz	—	0.9	1	—	0.9	2	
		f_O = 1kHz	—	0.85	1	—	0.85	2	
		f_O = 10kHz	—	0.85	1	—	0.85	2	
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA I_B = 100μA	—	0.05	0.1	—	0.05	0.2	V
Input Bias Current	I_B	I_C = 10μA	—	—	25	—	—	34	nA
Input Offset Current	I_{OS}	I_C = 10μA	—	—	0.6	—	—	1.3	nA
Breakdown Voltage	BV_{CEO}		40	—	—	40	—	—	V
Gain-Bandwidth Product	f_T	I_C = 10mA, V_{CE} = 10V	—	200	—	—	200	—	MHz
Output Capacitance	C_{OB}	V_{CB} = 15V, I_E = 0	—	23	—	—	23	—	pF
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	—	35	—	—	35	—	pF

NOTES:

1. Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector currents.
2. Current Gain Match (Δh_{FE}) is defined as:

$$\Delta h_{FE} = \frac{100\ (\Delta I_B)\ (h_{FE}\ \text{min})}{I_C}$$

3. Guaranteed by design.
4. Sample tested.
5. I_{CC} and I_{CES} are verified by measurement of I_{CBO}.
6. This is the maximum change in V_{OS} as V_{CB} is swept from 0V to 40V.
7. Measured at I_C = 10μA and guaranteed by design over the specified range of I_C.

PARAMETER	SYMBOL	CONDITIONS	MAT-02E MIN	MAT-02E TYP	MAT-02E MAX	MAT-02F MIN	MAT-02F TYP	MAT-02F MAX	UNITS
Offset Voltage	V_{OS}	$V_{CB} = 0$ $1\mu A \le I_C \le 1mA$ (Note 5)	—	—	70	—	—	220	μV
Average Offset Voltage Drift	TCV_{OS}	$10\mu A \le I_C \le 1mA$, $0 \le V_{CB} \le V_{MAX}$, (Note 1) V_{OS} Trimmed to Zero, (Note 3)	— —	0.08 0.03	0.3 0.1	— —	0.08 0.03	1 0.3	$\mu V/°C$
Input Offset Current	I_{OS}	$I_C = 10\mu A$	—	—	8	—	—	13	nA
Input Offset Current Drift	TCI_{OS}	$I_C = 10\mu A$, (Note 4)	—	40	90	—	40	150	$pA/°C$
Input Bias Current	I_B	$I_C = 10\mu A$	—	—	45	—	—	50	nA
Current Gain	h_{FE}	$I_C = 1mA$, (Note 2) $I_C = 100\mu A$ $I_C = 10\mu A$ $I_C = 1\mu A$	325 275 225 200	— — — —	— — — —	300 250 200 150	— — — —	— — — —	
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$	—	2	—	—	3	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = V_{MAX}$, $V_{BE} = 0$	—	3	—	—	4	—	nA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = V_{MAX}$	—	3	—	—	4	—	nA

ELECTRICAL CHARACTERISTICS $V_{CB} = 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02A MIN	MAT-02A TYP	MAT-02A MAX	MAT-02B MIN	MAT-02B TYP	MAT-02B MAX	UNITS
Offset Voltage	V_{OS}	$V_{CB} = 0$ $1\mu A \le I_C \le 1mA$ (Note 5)	—	—	80	—	—	250	μV
Average Offset Voltage Drift	TCV_{OS}	$10\mu A \le I_C \le 1mA$, $0 \le V_{CB} \le V_{MAX}$, (Note 1) V_{OS} Trimmed to Zero, (Note 3)	— —	0.08 0.03	0.3 0.1	— —	0.08 0.03	1 0.3	$\mu V/°C$
Input Offset Current	I_{OS}	$I_C = 10\mu A$	—	—	9	—	—	15	nA
Input Offset Current Drift	TCI_{OS}	$I_C = 10\mu A$, (Note 4)	—	40	90	—	40	150	$pA/°C$
Input Bias Current	I_B	$I_C = 10\mu A$	—	—	60	—	—	70	nA
Current Gain	h_{FE}	$I_C = 1mA$, (Note 2) $I_C = 100\ \mu A$ $I_C = 10\mu A$ $I_C = 1\mu A$	275 225 175 150	— — — —	— — — —	250 200 150 100	— — — —	— — — —	
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$ $T_A = 125°C$	—	15	—	—	25	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = V_{MAX}$, $V_{BE} = 0$ $T_A = 125°C$	—	50	—	—	50	—	nA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = V_{MAX}$ $T_A = 125°C$	—	30	—	—	40	—	nA

NOTES:

1. Guaranteed by V_{OS} test ($TCV_{OS} \simeq \frac{V_{OS}}{T}$ for $V_{OS} \ll V_{BE}$) T = 298k for $T_A = 25°C$.
2. Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector current.
3. The initial zero offset voltage is established by adjusting the ratio of I_{C1} to I_{C2} at $T_A = 25°C$. This ratio must be held to 0.003% over the entire temperature range. Measurements are taken at the temperature extremes and 25°C.
4. Guaranteed by design.
5. Measured at $I_C = 10\mu A$ and guaranteed by design over the specified range of I_C.

Low Noise, Matched Dual PNP Transistor

MAT03

FEATURES

- Dual Matched PNP Transistor
- Low Offset Voltage ..... 100μV Max
- Low Noise ..... 1nV/√Hz @ 1kHz Max
- High Gain ..... 100 Min
- High Gain Bandwidth ..... 190MHz Typ
- Tight Gain Matching ..... 3% Max
- Excellent Logarithmic Conformance ..... $r_{BE} \simeq 0.3\Omega$ Typ
- Available in Die Form

ORDERING INFORMATION†

T_A = +25°C V_{OS} MAX (μV)	PACKAGE TO-78	PACKAGE LCC	OPERATING TEMPERATURE RANGE
100	MAT03AH*	MAT03ARC/883	MIL
100	MAT03EH	—	XIND
200	MAT03FH	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

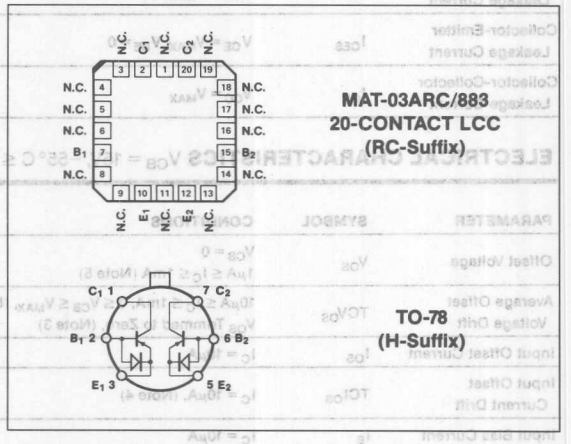
† Burn-in is available on industrial temperature range parts.

GENERAL DESCRIPTION

The MAT-03 dual monolithic PNP transistor offers excellent parametric matching and high frequency performance. Low noise characteristics (1nV/√Hz Max @ 1kHz), high bandwidth (190MHz typical), and low offset voltage (100μV Max), makes the MAT-03 an excellent choice for demanding preamplifier applications. Tight current gain matching (3% Max mismatch) and high current gain (100 Min), over a wide range of collector current, makes the MAT-03 an excellent choice for current mirrors. A low value of bulk resistance (typically 0.3Ω) also makes the MAT-03 an ideal component for applications requiring accurate logarithmic conformance.

Each transistor is individually tested to data sheet specifications. Device performance is guaranteed at 25°C and over the extended industrial and military temperature ranges. To insure the long-term stability of the matching parameters, internal protection diodes across the base-emitter junction clamp any reverse base-emitter junction potential. This prevents a base-emitter breakdown condition which can result in degradation of gain and matching performance due to excessive breakdown current.

PIN CONNECTIONS



MAT-03ARC/883
20-CONTACT LCC
(RC-Suffix)

TO-78
(H-Suffix)

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Collector-Base Voltage (BV_{CBO}) 36V
Collector-Emitter Voltage (BV_{CEO}) 36V
Collector-Collector Voltage (BV_{CC}) 36V
Emitter-Emitter Voltage (BV_{EE}) 36V
Collector Current (I_C) 20mA
Emitter Current (I_E) 20mA
Total Power Dissipation
Ambient Temperature ≤ 70°C (Note 2) 500mW
Operating Temperature Range
MAT-03A ..... −55°C to +125°C
MAT-03E/F ..... −40°C to +85°C
Operating Junction Temperature ..... −55°C to +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... −65°C to +150°C

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged devices.
2. Rating applies to TO-78 not using a heat sink, and LCC; devices in free air only. For TO-78, derate linearly at 6.3mW/°C above 70°C ambient temperature; for LCC, derate at 7.8mW/°C.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, unless otherwise noted.

			MAT-03A			MAT-03E			MAT-03F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Current Gain (Note 1)	h_{FE}	V_{CB} = 0V, −36V I_C = 1mA	100	165	—	100	165	—	80	165	—	
		I_C = 100μA	90	150	—	90	150	—	70	150	—	
		I_C = 10μA	80	120	—	80	120	—	60	120	—	
Current Gain Matching (Note 2)	Δh_{FE}	I_C = 100μA, V_{CB} = 0V	—	0.5	3	—	0.5	3	—	0.5	6	%
Offset Voltage (Note 3)	V_{OS}	V_{CB} = 0V, I_C = 100μA	—	40	100	—	40	100	—	40	200	μV
Offset Voltage Change vs Collector Voltage	$\Delta V_{OS}/\Delta V_{CB}$	I_C = 100μA V_{CB_1} = 0V V_{CB_2} = −36V	—	11	150	—	11	150	—	11	200	μV
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0V I_{C_1} = 10μA, I_{C_2} = 1mA	—	12	50	—	12	50	—	12	75	μV
Bulk Resistance	r_{BE}	V_{CB} = 0V, 10μA ≤ I_C ≤ 1mA	—	0.3	0.75	—	0.3	0.75	—	0.3	0.75	Ω
Offset Current	I_{OS}	I_C = 100μA, V_{CB} = 0V	—	6	35	—	6	35	—	6	45	nA
Collector-Base Leakage Current	I_{CB_0}	V_{CB} = −36V = V_{MAX}	—	50	200	—	50	200	—	50	400	pA
Noise Voltage Density (Note 4)	e_N	I_C = 1mA, V_{CB} = 0 f_O = 10Hz	—	0.8	2	—	0.8	—	—	0.8	—	nV/√Hz
		f_O = 100Hz	—	0.7	1	—	0.7	—	—	0.7	—	
		f_O = 1kHz	—	0.7	1	—	0.7	—	—	0.7	—	
		f_O = 10kHz	—	0.7	1	—	0.7	—	—	0.7	—	
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA, I_B = 100μA	—	0.025	0.1	—	0.025	0.1	—	0.025	0.1	V

NOTES:
1. Current gain is measured at collector-base voltages (V_{CB}) swept from 0 to V_{MAX} at indicated collector current. Typicals are measured at V_{CB} = 0V.
2. Current gain matching (Δh_{FE}) is defined as:

$$\Delta h_{FE} = \frac{100\ (\Delta I_B)\ h_{FE}\ (MIN)}{I_C}$$

3. Offset voltage is defined as:
$V_{OS} = V_{BE_1} - V_{BE_2}$,
where V_{OS} is the differential voltage for

$$I_{C_1} = I_{C_2}: V_{OS} = V_{BE_1} - V_{BE_2} = \frac{KT}{q} \ln\left(\frac{I_{C_1}}{I_{C_2}}\right).$$

4. Sample tested. Noise tested and specified as equivalent input voltage for each transistor.

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PARAMETER	SYMBOL	CONDITIONS	MAT-03A MIN	MAT-03A TYP	MAT-03A MAX	UNITS
Current Gain	h_{FE}	V_{CB} = 0V, −36V I_C = 1mA I_C = 100μA I_C = 10μA	70 60 50	110 100 85	— — —	
Offset Voltage	V_{OS}	I_C = 100μA, V_{CB} = 0V	—	40	150	μV
Offset Voltage Drift (Note 1)	TCV_{OS}	I_C = 100μA, V_{CB} = 0V	—	0.3	0.5	μV/°C
Offset Current	I_{OS}	I_C = 100μA, V_{CB} = 0V	—	15	85	nA
Breakdown Voltage	BV_{CEO}		36	54	—	V

NOTE:
1. Guaranteed by V_{OS} test ($TCV_{OS} = V_{OS}/T$ for $V_{OS} \ll V_{BE}$) where T = 298° K for T_A = 25°C.

ELECTRICAL CHARACTERISTICS at −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-03E MIN	MAT-03E TYP	MAT-03E MAX	MAT-03F MIN	MAT-03F TYP	MAT-03F MAX	UNITS
Current Gain	h_{FE}	V_{CB} = 0V, −36V I_C = 1mA I_C = 100μA I_C = 10μA	70 60 50	120 105 90	— — —	60 50 40	120 105 90	— — —	
Offset Voltage	V_{OS}	I_C = 100μA, V_{CB} = 0V	—	30	135	—	30	265	μV
Offset Voltage Drift (Note 1)	TCV_{OS}	I_C = 100μA, V_{CB} = 0V	—	0.3	0.5	—	0.3	1.0	μV/°C
Offset Current	I_{OS}	I_C = 100μA, V_{CB} = 0V	—	10	85	—	10	200	nA
Breakdown Voltage	BV_{CEO}		36	—	—	36	—	—	V

NOTE:
1. Guaranteed by V_{OS} test ($TCV_{OS} = V_{OS}/T$ for $V_{OS} \ll V_{BE}$) where T = 298° K for T_A = 25°C.

FEATURES

- Low Offset Voltage ..... 200µV Max
- High Current Gain ..... 400 Min
- Excellent Current Gain Match ..... 2% Max
- Low Noise Voltage at 100Hz, 1mA ..... 2.5nV/ Hz Max
- Excellent Log Conformance ..... rBE = 0.6Ω Max
- Matching Guaranteed for All Transistors
- Available in Die Form

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (µV)	PACKAGE CERDIP 14-PIN	PACKAGE PLASTIC 14-PIN	OPERATING TEMPERATURE RANGE
200	MAT04AY*	—	MIL
200	MAT04EY	—	IND
400	MAT04BY*	—	MIL
400	MAT04FY	MAT04FP	XIND
400	—	MAT04FS††	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

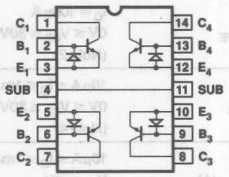
GENERAL DESCRIPTION

The MAT-04 is a quad monolithic NPN transistor that offers excellent parametric matching for precision amplifier and non-linear circuit applications. Performance characteristics of the MAT-04 include high gain (400 minimum) over a wide range of collector current, low noise (2.5nV/$\sqrt{Hz}$ maximum at 100Hz, I_C = 1 mA) and excellent logarithmic conformance. The MAT-04 also features a low offset voltage of 200µV and tight current gain matching, to within 2%. Each transistor of the MAT-04 is individually tested to data sheet specifications. For matching parameters (offset voltage, input offset current, and gain match), each of the dual transistor combinations are verified to meet stated limits. Device performance is guaranteed at 25°C and over the industrial and military temperature ranges.

The long-term stability of matching parameters is guaranteed by the protection diodes across the base-emitter junction of each transistor. These diodes prevent degradation of beta and matching characteristics due to reverse bias base-emitter current.

The superior logarithmic conformance and accurate matching characteristics of the MAT-04 makes it an excellent choice for use in log and antilog circuits. The MAT-04 is an ideal choice in applications where low noise and high gain are required.

PIN CONNECTIONS



14-PIN CERDIP (Y-Suffix)

14-PIN PLASTIC DIP (P-Suffix)

14-PIN SO (S-Suffix)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Collector-Base Voltage (BV_{CBO}) 40V
Collector-Emitter Voltage (BV_{CEO}) 40V
Collector-Collector Voltage (BV_{CC}) 40V
Emitter-Emitter Voltage (BV_{EE}) 40V
Collector Current 30mA
Emitter Current 30mA
Substrate (Pin-4 to Pin-11) Current 30mA
Operating Temperature Range
MAT-04AY, BY ..... –55°C TO +125°C
MAT-04EY ..... –25°C TO +85°C
MAT-04FY,FP,FS ..... –40°C to +85°C
Storage Temperature
Y Package ..... –65°C to +150°C
P Package ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin CERDIP (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SO (S)	120	36	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ELECTRICAL CHARACTERISTICS at T_A = 25°C unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}, Δh_{FE}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

			MAT-04A/E			MAT-04B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Current Gain	h_{FE}	10µA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 1)	400	800	—	300	600	—	
Current Gain Match	Δh_{FE}	I_C = 100µA 0V ≤ V_{CB} ≤ 30V (Note 2)	—	0.5	2	—	1	4	%
Offset Voltage	V_{OS}	10µA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 4)	—	50	200	—	100	400	µV
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	10µA ≤ I_C ≤ 1mA V_{CB} = 0V (Note 4)	—	5	25	—	10	50	µV
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	10µA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 4)	—	50	100	—	100	200	µV
Bulk Emitter Resistance	r_{BE}	10µA ≤ I_C ≤ 1mA V_{CB} = 0V (Note 5)	—	0.4	0.6	—	0.4	0.6	Ω
Input Bias Current	I_B	I_C = 100µA 0V ≤ V_{CB} ≤ 30V	—	125	250	—	165	330	nA
Input Offset Current	I_{OS}	I_C = 100µA V_{CB} = 0V	—	0.6	5	—	2	13	nA
Breakdown Voltage	BV_{CEO}	I_C = 10µA	40	—	—	40	—	—	V
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 100µA I_C = 1mA	—	0.03	0.06	—	0.03	0.06	V
Collector-Base Leakage Current	I_{CBO}	V_{CB} = 40V	—	5	—	—	5	—	pA
Noise Voltage Density	e_n	V_{CB} = 0V f_O = 10Hz	—	2	3	—	2	4	nV/√Hz
		I_C = 1mA f_O = 100Hz	—	1.8	2.5	—	1.8	3	
		(Note 3) f_O = 1kHz	—	1.8	2.5	—	1.8	3	
Gain Bandwidth Product	f_T	I_C = 1mA V_{CE} = 10V	—	300	—	—	300	—	MHz
Output Capacitance	C_{OBO}	V_{CB} = 15V I_E = 0 f = 1MHz	—	10	—	—	10	—	pF
Input Capacitance	C_{EBO}	V_{BE} = 0V I_C = 0 f = 1MHz	—	40	—	—	40	—	pF

NOTES:

1. Current gain measured at I_C = 10µA, 100µA and 1mA.
2. Current gain match is defined as: $\Delta h_{FE} = \frac{100\,(\Delta I_B)\,(h_{FE}\,\text{min})}{I_C}$
3. Sample tested.
4. Measured at I_C = 10µA and guaranteed by design over the specified range of I_C.
5. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $-25°C \le T_A \le +85°C$ for MAT-04E, $-40°C \le T_A \le +85°C$ for MAT-04F, unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04E MIN	MAT-04E TYP	MAT-04E MAX	MAT-04F MIN	MAT-04F TYP	MAT-04F MAX	UNITS
Current Gain	h_{FE}	$10\mu A \le I_C \le 1mA$ $0V \le V_{CB} \le 30V$ (Note 1)	225	625	—	200	500	—	
Offset Voltage	V_{OS}	$10\mu A \le I_C \le 1mA$ $0V \le V_{CB} \le 30V$ (Note 3)	—	60	260	—	120	520	μV
Average Offset Voltage Drift	TCV_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$ (Note 2)	—	0.2	1	—	0.4	2	μV/°C
Input Bias Current	I_B	$I_C = 100\mu A$ $0V \le V_{CB} \le 30V$	—	160	445	—	200	500	nA
Input Offset Current	I_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	4	20	—	8	40	nA
Average Offset Current Drift	TCI_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	50	—	—	100	—	pA/°C
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu A$	40	—	—	40	—	—	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40V$	—	0.5	—	—	0.5	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 40V$	—	5	—	—	5	—	nA
Collector-Substrate Leakage Current	I_{CS}	$V_{CS} = 40V$	—	0.7	—	—	0.7	—	nA

ELECTRICAL CHARACTERISTICS at $-55°C \le T_A \le 125°C$ unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

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PARAMETER	SYMBOL	CONDITIONS	MAT-04A MIN	MAT-04A TYP	MAT-04A MAX	MAT-04B MIN	MAT-04B TYP	MAT-04B MAX	UNITS
Current Gain	h_{FE}	$10\mu A \le I_C \le 1mA$ $0V \le V_{CB} \le 30V$ (Note 1)	175	475	—	125	425	—	
Offset Voltage	V_{OS}	$10\mu A \le I_C \le 1mA$ $0V \le V_{CB} \le 30V$ (Note 3)	—	70	300	—	140	600	μV
Average Offset Voltage Drift	TCV_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$ (Note 2)	—	0.2	1	—	0.4	2	μV/°C
Input Bias Current	I_B	$I_C = 100\mu A$ $0V \le V_{CB} \le 30V$	—	210	570	—	235	800	nA
Input Offset Current	I_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	6	30	—	12	60	nA
Average Offset Current Drift	TCI_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	50	—	—	100	—	pA/°C
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu A$	40	—	—	40	—	—	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40V$	—	5	—	—	5	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 40V$	—	100	—	—	100	—	nA
Collector-Substrate Leakage Current	I_{CS}	$V_{CS} = 40V$	—	7	—	—	7	—	nA

NOTES:
1. Current gain measured at $I_C = 10\mu A$, $100\mu A$ and 1mA.
2. Guaranteed by V_{OS} test ($TCV_{OS} \le V_{OS}/T$ for $V_{OS} << V_{BE}$) T = 298°K for $T_A = 25°C$.
3. Measured at $I_C = 10\mu A$ and guaranteed by design over the specified range of I_C.

ELECTRICAL CHARACTERISTICS at $-55°C \leq T_A \leq 125°C$ unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}) each dual transistor combination is verified to meet stated limits. All tests made at ambient unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04E			MAT-04F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	h_{FE}	$10\mu A \leq I_C \leq 1mA$ $0V \leq V_{CB} \leq 30V$ (Note 1)	228	825	—	200	600	—	
Offset Voltage	V_{OS}	$10\mu A \leq I_C \leq 1mA$ $0V \leq V_{CB} \leq 30V$ (Note 3)	—	60	250	—	125	320	μV
Average Offset Voltage Drift	TCV_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$ (Note 2)	—	0.2	1	—	0.4	2	$\mu V/°C$
Input Bias Current	I_B	$I_C = 100\mu A$ $0V \leq V_{CB} \leq 30V$	—	160	445	—	270	700	nA
Input Offset Current	I_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	4	20	—	8	40	nA
Average Offset Current Drift	TCI_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	50	—	—	100	—	$nA/°C$
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu A$	40	—	—	40	—	—	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40V$	—	0.5	—	—	0.5	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 40V$	—	5	—	—	5	—	nA
Collector-Substrate Leakage Current	I_{CS}	$V_{CS} = 40V$	—	0.7	—	—	0.7	—	nA

ELECTRICAL CHARACTERISTICS at $-55°C \leq T_A \leq 125°C$ unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}) each dual transistor combination is verified to meet stated limits. All tests made at ambient unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04A			MAT-04B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	h_{FE}	$10\mu A \leq I_C \leq 1mA$ $0V \leq V_{CB} \leq 30V$ (Note 1)	778	4750	—	125	425	—	
Offset Voltage	V_{OS}	$10\mu A \leq I_C \leq 1mA$ $0V \leq V_{CB} \leq 30V$ (Note 3)	—	20	200	—	140	800	μV
Average Offset Voltage Drift	TCV_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$ (Note 2)	—	0.2	1	—	0.4	2	$\mu V/°C$
Input Bias Current	I_B	$I_C = 100\mu A$ $0V \leq V_{CB} \leq 30V$	—	240	670	—	2.15	800	nA
Input Offset Current	I_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	6	30	—	12	60	nA
Average Offset Current Drift	TCI_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	80	—	—	320	—	$pA/°C$
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu A$	40	—	—	40	—	—	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40V$	—	5	—	—	5	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 40V$	—	100	—	—	100	—	nA
Collector-Substrate Leakage Current	I_{CS}	$V_{CS} = 40V$	—	7	—	—	7	—	nA

NOTES:
1. Current gain measured at $I_C = 10\mu A$, $100\mu A$ and $1mA$.
2. Guaranteed by V_{OS} test ($TCV_{OS} \approx V_{OS}/T$ for $V_{OS} << V_{OS}$) $T = 298°K$ for $T_A = 25°C$.
3. Measured at $I_C = 10\mu A$ and guaranteed by design over the specified range of I_C.

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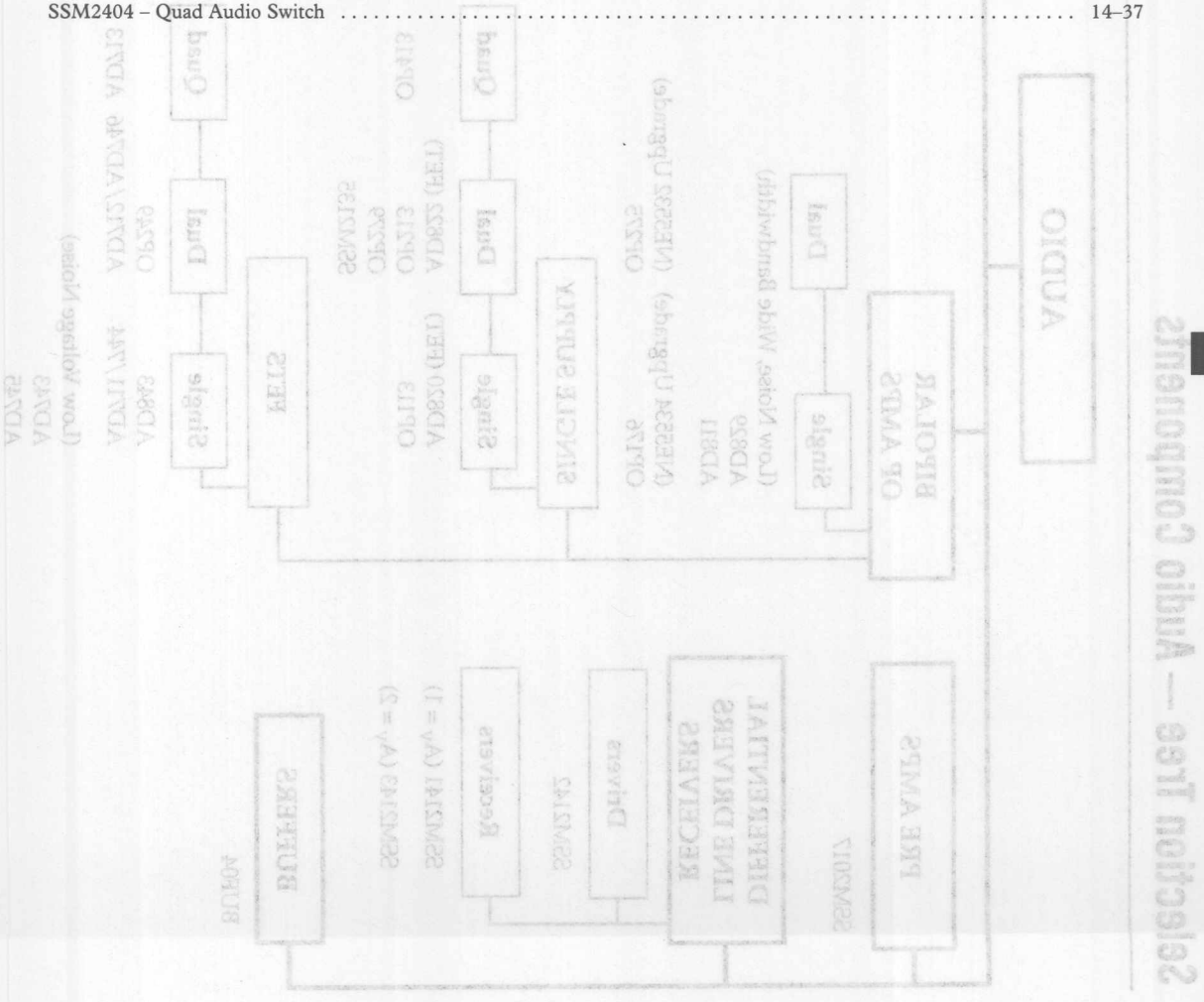

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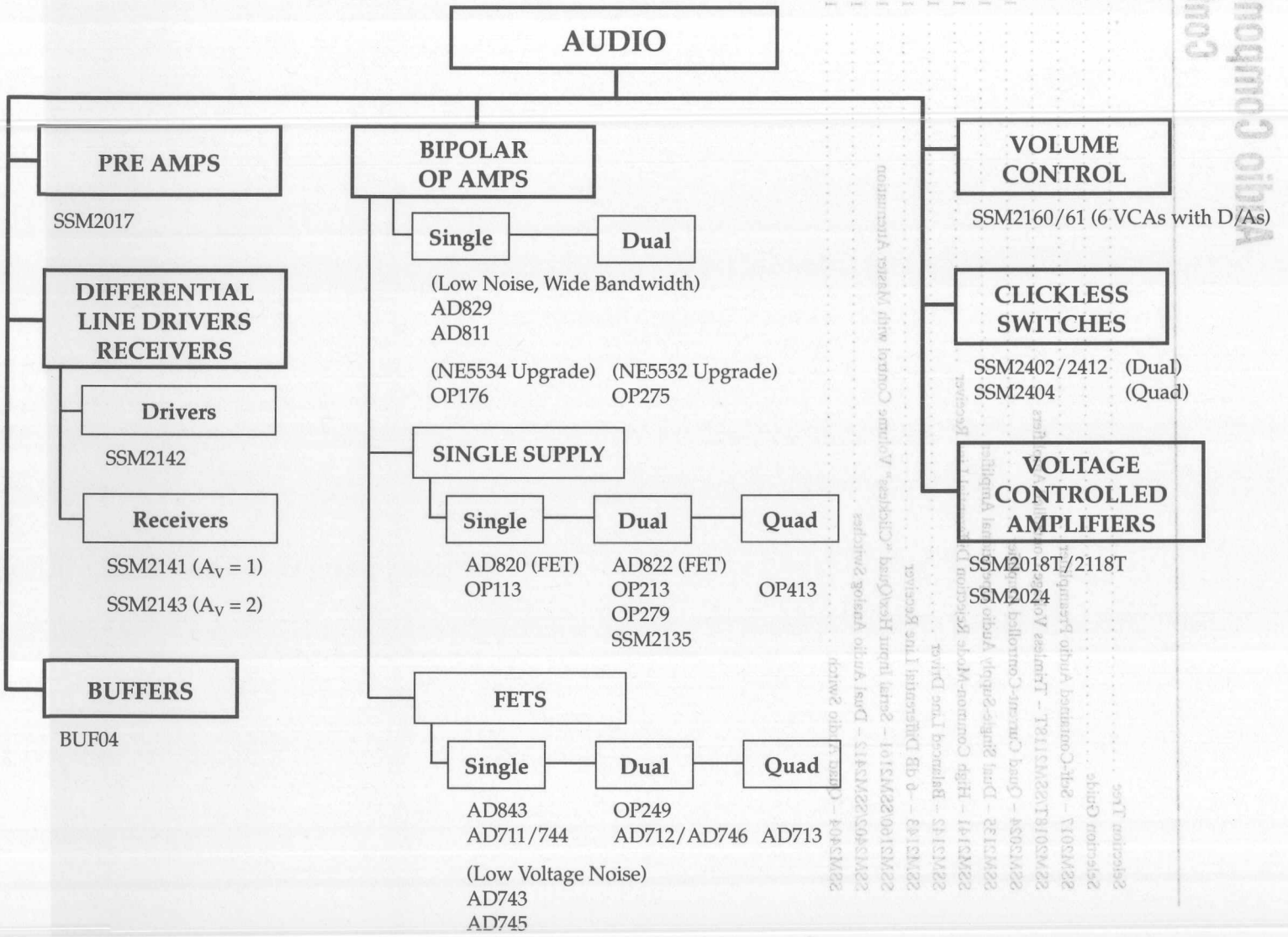
Selection Tree — Audio Components



Selection Guides—Audio Components

Amplifiers

Model	Function	en nV/√Hz 20 kHz BW	THD+N @ 1 kHz	BW MHz	Package Option[1]	Temp Ranges[2]	Comments	Page
SSM2017	Audio Preamplifier	0.95	0.005%	4.0	N, R	I	Low Noise, 8-Pin DIP, High Gain	14–5
SSM2135	Dual Audio Op Amp	5.2	0.001%	3.5	N, R	I	+5 V Supply, 8-Pin DIP, High Output	14–14
SSM2141	Differential Line Receiver	22.0	0.001%	3	N, R	I	High CMRR, Drives 600 Ω	14–24
SSM2142	Balanced Line Driver	117.0	0.006%	—	N, Q, R	I	10 V RMS into 600 Ω, High Cap Load	14–26
SSM2143	Differential Line Receiver	23.6	0.0006%	7	N, R	I	Gain = 1/2 or 2, High CMRR	14–28

Volume Control/Voltage-Controlled Amplifiers

Model	Function	Dynamic Range dB	THD %	BW MHz	Package Option[1]	Temp Ranges[2]	Comments	Page
SSM2018T	Voltage Out VCA	117	0.006	0.7	N, R	I	Trimless, 140 dB Gain Range	14–8
SSM2118T	Diff. Current Out VCA	140	0.006	14.0	N, R	I	Direct Output Summing	14–8
SSM2024	Quad Current-Controlled VCA	82	0.3	—	N	C	Low Feedthrough, Class A	14–12
SSM2160	Hex Digital Volume Control	100	0.008	—	N, R	I	"Clickless" Control, Master Attenuator	14–30
SSM2161	Quad Digital Volume Control	100	0.008	—	N, R	I	Low Crosstalk, Adjustable Step	14–30

"Clickless" Audio Switches

Model	Function	THD %	Switch Time ms	Ron Ω	Signal Range V	Package Option[1]	Temp Ranges[2]	Comments	Page
SSM2402	Dual SPST Switch	0.003	10.0	60	±14.2	N, R	I	Break-Before-Make, Low Distortion	14–34
SSM2404	Quad SPST Switch	0.008	8.0	28	±12.0	N, R	I	Single Supply, Low Crosstalk	14–37
SSM2412	Dual SPST Switch	0.003	3.5	60	±14.2	N, R	I	Higher Speed, Low Noise	14–34

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_{J}$ for JAN, $_{D}$ for SMD, and $_{S}$ for space level.
Boldface Type: Data sheet information in this volume.

Selection Guides—Audio Components

Amplifiers

Model	Function	en nV/√Hz 20 kHz BW	THD+N @ 1 kHz	BW MHz	Package Option[1]	Temp Ranges[2]	Comments
SSM2017	Audio Preamplifier	0.95	0.0056%	4.0	N, R	I	Low Noise, 8-Pin DIP, High Gain
SSM2135	Dual Audio Op Amp	5.2	0.0019%	3.5	N, R	I	+5 V Supply, 8-Pin DIP, High Outp
SSM2141	Differential Line Receiver	22.0	0.0019%	3	N, R	I	High CMRR, Drives 600 Ω
SSM2142	Balanced Line Driver	117.0	0.0095%	—	N, Q, R	I	10 V RMS into 600 Ω, High Op Le
SSM2143	Differential Line Receiver	25.6	0.0095%	7	N, R	I	Gain = 1/2 or 2, High CMRR

Volume Control/Voltage-Controlled Amplifiers

Model	Function	Dynamic Range dB	THD %	BW MHz	Package Option[1]	Temp Ranges[2]	Comments
SSM2018T	Voltage Out VCA	117	0.006	0.7	N, R	I	Trimless, 140 dB Gain Range
SSM2181T	DBL Current Out VCA	140	0.006	14.0	N, R	I	Direct Output Summing
SSM2024	Quad Current-Controlled VCA	82	0.3	—	N	C	Low Feedthrough, Class A
SSM2160	Hex Digital Volume Control	100	0.008	—	N, R	I	"Clickless" Control, Master Attenua
SSM2161	Quad Digital Volume Control	100	0.008	—	N, R	I	Low Crosstalk, Adjustable Step

"Clickless" Audio Switches

Model	Function	THD %	Switch Time ms	Ron Ω	Signal Range V	Package Option[1]	Temp Ranges[2]	Comments
SSM2402	Dual SPST Switch	0.003	10.0	60	±14.2	N, R	I	Break-Before-Make, Low Distort
SSM2404	Quad SPST Switch	0.008	8.0	25	±12.0	N, R	I	Single Supply, Low Crosstalk
SSM2412	Dual SPST Switch	0.003	3.5	60	±14.2	N, R	I	Higher Speed, Low Noise

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; P = Ceramic Flatpack; Q = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ce
M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Pack
Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Le
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, –40°C to +85°C (Some older products – 25°C to +85°C); M = Military, –55°C to +125°C. If a device has military grade c
prepcreature designator will be followed by /to indicate 883B, 1 for JAN, D for SMD, and 8 for space level.
Rolative Types Data sheet information in this volume.

FEATURES

- Excellent Noise Performance: 950 pV/$\sqrt{Hz}$ or 1.5 dB Noise Figure
- Ultralow THD: <0.01% @ G = 100 Over the Full Audio Band
- Wide Bandwidth: 1 MHz @ G = 100
- High Slew Rate: 17 V/μs typ
- Unity Gain Stable
- True Differential Inputs
- Subaudio 1/f Noise Corner
- 8-Pin Mini-DIP with Only One External Component Required
- Very Low Cost
- Extended Temperature Range: −40°C to +85°C

APPLICATIONS

- Audio Mix Consoles
- Intercom/Paging Systems
- Two-Way Radio
- Sonar
- Digital Audio Systems

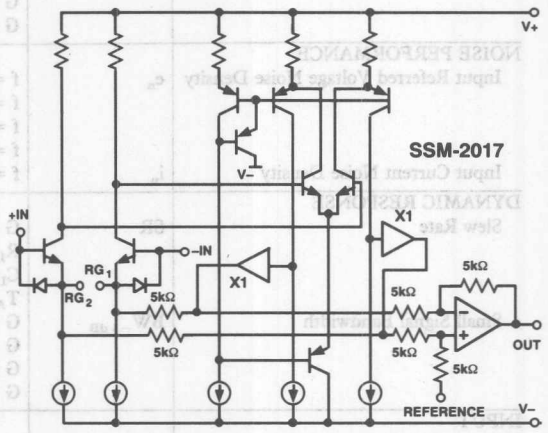
GENERAL DESCRIPTION

The SSM-2017 is a latest generation audio preamplifier combining SSM preamplifier design expertise with advanced processing. The result is excellent audio performance from a self-contained 8-pin mini-DIP device, requiring only one external gain set resistor or potentiometer. The SSM-2017 is further enhanced by its unity gain stability.

Key specifications include ultralow noise (1.5 dB noise figure) and THD (<0.01% at G = 100), complemented by wide bandwidth and high slew rate.

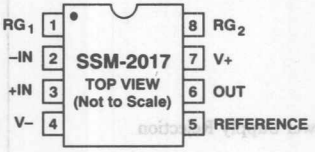
Applications for this low cost device include microphone preamplifiers and bus summing amplifiers in professional and consumer audio equipment, sonar, and other applications requiring a low noise instrumentation amplifier with high gain capability.

FUNCTIONAL BLOCK DIAGRAM

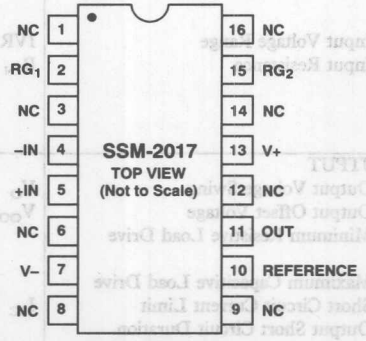


PIN CONNECTIONS

Epoxy Mini-DIP (P Suffix)



16-Pin Wide Body SOL (S Suffix)



NC = NO CONNECT

14

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SSM2017—SPECIFICATIONS

(V_S = ±15 V and −40°C ≤ T_A ≤ +85°C, unless otherwise specified. Typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DISTORTION PERFORMANCE		T_A = +25°C V_O = 7 V_{RMS} R_L = 5 kΩ				
Total Harmonic Distortion Plus Noise	THD+N	G = 1000, f = 1 kHz		0.012		%
		G = 100, f = 1 kHz		0.005		%
		G = 10, f = 1 kHz		0.004		%
		G = 1, f = 1 kHz		0.008		%
NOISE PERFORMANCE						
Input Referred Voltage Noise Density	e_n	f = 1 kHz, G = 1000		0.95		$nV/\sqrt{Hz}$
		f = 1 kHz; G = 100		1.95		$nV/\sqrt{Hz}$
		f = 1 kHz; G = 10		11.83		$nV/\sqrt{Hz}$
		f = 1 kHz; G = 1		107.14		$nV/\sqrt{Hz}$
Input Current Noise Density	i_n	f = 1 kHz, G = 1000		2		$pA/\sqrt{Hz}$
DYNAMIC RESPONSE						
Slew Rate	SR	G = 10 R_L = 4.7 kΩ C_L = 50 pF T_A = +25°C	10	17		V/µs
Small Signal Bandwidth	$BW_{-3\ dB}$	G = 1000		200		kHz
		G = 100		1000		kHz
		G = 10		2000		kHz
		G = 1		4000		kHz
INPUT						
Input Offset Voltage	V_{IOS}			0.1	1.2	mV
Input Bias Current	I_B	V_{CM} = 0 V		6	25	µA
Input Offset Current	I_{OS}	V_{CM} = 0 V		±0.002	±2.5	µA
Common-Mode Rejection	CMR	V_{CM} = ±8 V				
		G = 1000	80	112		dB
		G = 100	60	92		dB
		G = 10	40	74		dB
		G = 1, T_A = +25°C	26	54		dB
		G = 1, T_A = −40°C to +85°C	20	54		dB
Power Supply Rejection	PSR	V_S = ±6 V to ±18 V				
		G = 1000	80	124		dB
		G = 100	60	118		dB
		G = 10	40	101		dB
		G = 1	26	82		dB
Input Voltage Range	IVR		±8			V
Input Resistance	R_{IN}	Differential, G = 1000		1		MΩ
		G = 1		30		MΩ
		Common Mode, G = 1000		5.3		MΩ
		G = 1		7.1		MΩ
OUTPUT						
Output Voltage Swing	V_O	R_L = 2 kΩ; T_A = +25°C	±11.0	±12.3		V
Output Offset Voltage	V_{OOS}			−40	500	mV
Minimum Resistive Load Drive		T_A = +25°C		2		kΩ
		T_A = −40°C to +85°C		4.7		kΩ
Maximum Capacitive Load Drive				50		pF
Short Circuit Current Limit	I_{SC}	Output-to-Ground Short		±50		mA
Output Short Circuit Duration					10	sec
GAIN						
Gain Accuracy	$R_G = \frac{10\ k\Omega}{G-1}$	T_A = +25°C				
		R_G = 10 Ω, G = 1000		0.25	1	dB
		R_G = 101 Ω, G = 100		0.20	1	dB
		R_G = 1.1 kΩ, G = 10		0.20	1	dB
		R_G = ∞, G = 1		0.05	0.5	dB
Maximum Gain	G			70		dB

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
REFERENCE INPUT						
Input Resistance				10		kΩ
Voltage Range				±8		V
Gain to Output				1		V/V
POWER SUPPLY						
Supply Voltage Range	V_S		±6		±22	V
Supply Current	I_{SY}	V_{CM} = 0 V, R_L = ∞		±10.6	±14.0	mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±22 V
Input Voltage . . . . . Supply Voltage
Output Short Circuit Duration . . . . . 10 sec
Storage Temperature Range (P, Z Packages) . −65°C to +150°C
Junction Temperature (T_J) . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C
Operating Temperature Range . . . . . −40°C to +85°C
Thermal Resistance[1]
8-Pin Hermetic DIP (Z): θ_{JA} = 134; θ_{JC} = 12 . . . . . °C/W
8-Pin Plastic DIP (P): θ_{JA} = 96; θ_{JC} = 37 . . . . . °C/W
16-Pin SOIC (S): θ_{JA} = 92; θ_{JC} = 27 . . . . . °C/W

NOTE
[1]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ORDERING GUIDE

Model	Temperature Range[1]	Package Description	Package Option[2]
SSM2017P	−40°C to +85°C	8-Pin Plastic DIP	N-8
SSM2017S	−40°C to +85°C	16-Lead SOL	R-16

[1]XIND = −40°C to +85°C.
[2]For outline information see Package Information section.

Typical Performance Characteristics

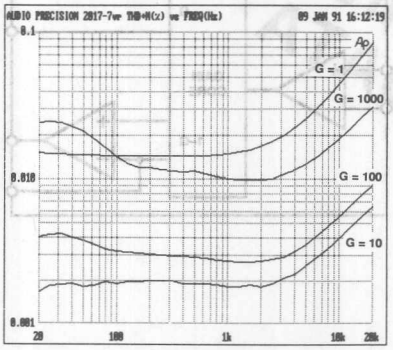


Figure 1. Typical THD+Noise at G = 1, 10, 100, 1000; V_O = 7 V_{RMS}, V_S = ±15 V, R_L = 5 kΩ; T_A = +25°C*

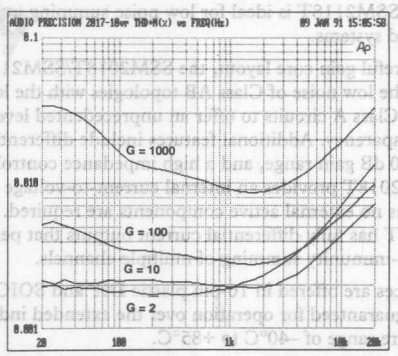
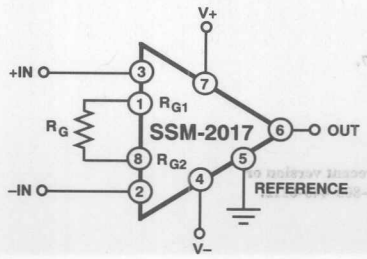


Figure 2. Typical THD+Noise at G = 2, 10, 100, 1000; V_O = 10 V_{RMS}, V_S = ±18 V, R_L = 5 kΩ; T_A = +25°C*

*80 kHz low-pass filter used for Figures 1–2.



$$G = \frac{V_{OUT}}{(+IN) - (-IN)} = \left(\frac{10k\Omega}{R_G}\right) + 1$$

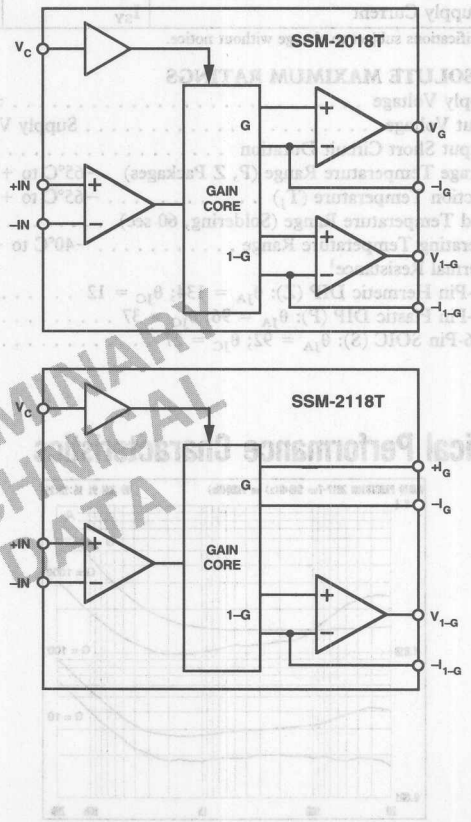
Basic Circuit Connections

Trimless Voltage Controlled Amplifiers

SSM2018T/SSM2118T*

FEATURES
117 dB Dynamic Range
0.006% Typical THD+N (@ 1 kHz, Unity Gain)
140 dB Gain Range
No External Trimming Required
Differential Inputs
Complementary Gain Outputs
Buffered Control Port
I–V Converter On-Chip (SSM2018T)
Differential Current Outputs (SSM2118T)
Low External Parts Count
Low Cost

FUNCTIONAL BLOCK DIAGRAMS



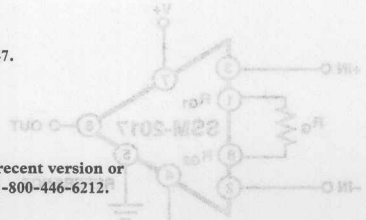
PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The SSM2018T and SSM2118T represent continuing evolution of the Frey Operational Voltage Element (OVCE) topology that permits flexibility in the design of high performance volume control systems. Voltage (SSM2018T) and differential current (SSM2118T) output versions are offered, both laser-trimmed for gain core symmetry and offset. As a result, the SSM2018T is the first professional audio quality VCA to offer trimless operation. The SSM2118T is ideal for low noise summing in large VCA based systems.

Due to careful gain core layout, the SSM2018T/SSM2118T combine the low noise of Class AB topologies with the low distortion of Class A circuits to offer an unprecedented level of sonic transparency. Additional features include differential inputs, a 140 dB gain range, and a high impedance control port. The SSM2018T provides an internal current-to-voltage converter; thus no external active components are required. The SSM2118T has fully differential current outputs that permit high noise-immunity summing of multiple channels.

Both devices are offered in 16-pin plastic DIP and SOIC packages and guaranteed for operation over the extended industrial temperature range of –40°C to +85°C.



***Protected by U.S. Patent Nos. 4,471,320 and 4,560,947.**

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This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

[V_S = ±15 V, A_V = 0 dB, R_L = 100 kΩ, f = 1 kHz, 0 dBu = 0.775 V rms, simple VCA application circuit with 18 kΩ resistors, $-V_{IN}$ floating, and Class AB gain core bias (R_B = 150 kΩ), −40°C < T_A < +85°C, unless otherwise noted. Typical specifications apply at T_A = +25°C.]

Parameter	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE[1]					
Noise	V_{IN} = GND, 20 kHz Bandwidth		–95	–93	dBu
Headroom	Clip Point = 1% THD+N		+22		dBu
Total Harmonic Distortion plus Noise	2nd and 3rd Harmonics Only (+25°C to +85°C)				
	A_V = 0 dB, V_{IN} = +10 dBu		0.006	0.025	%
	A_V = +20 dB, V_{IN} = –10 dBu		0.013	0.014	%
	A_V = –20 dB, V_{IN} = +10 dBu		0.013	0.04	%
INPUT AMPLIFIER					
Bias Current	V_{CM} = 0 V		0.25	1	µA
Offset Voltage	V_{CM} = 0 V		1	15	mV
Offset Current	V_{CM} = 0 V		10	100	nA
Input Impedance			4		MΩ
Common-Mode Range			±13		V
Gain Bandwidth	VCA Configuration		0.7		MHz
	VCP Configuration		14		MHz
Slew Rate			10		V/µs
OUTPUT AMPLIFIER (SSM2018T)					
Offset Voltage	V_{IN} = 0 V, V_C = +4 V		1.0	15	mV
Output Voltage Swing	I_{OUT} = 1.5 mA				
	Positive	+10	+13		V
	Negative	–10	+14		V
Minimum Load Resistance	For Full Output Swing		9		kΩ
CONTROL PORT					
Bias Current			0.36	1	µA
Input Impedance			1		MΩ
Gain Constant	Device Powered in Socket > 60 sec		–30		mV/dB
Gain Constant Temperature Coefficient			–3500		ppm/°C
Control Feedthrough	+10 dB to –40 dB Gain Range		±1	±4	mV
Maximum Attenuation	V_C = +4 V		100		dB
POWER SUPPLIES					
Supply Voltage Range		±5		±18	V
Supply Current			11	15	mA
Power Supply Rejection Ratio			80		dB

NOTES

[1]SSM2118T tested and characterized using OP275 as current-to-voltage converter.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Input Voltage	$\pm V_S$
Operating Temperature Range	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Junction Temperature (T_J)	+150°C
Lead Temperature (Soldering, 60 sec)	+300°C

THERMAL CHARACTERISTICS

Thermal Resistance[2]

16-Pin Plastic DIP

θ_{JA}	76°C/W
θ_{JC}	33°C/W

16-Pin SOIC

θ_{JA}	92°C/W
θ_{JC}	27°C/W

TRANSISTOR COUNT

Number of Transistors

SSM2018T	125
SSM2118T	108

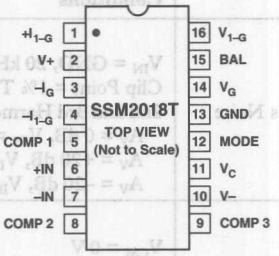
ESD RATINGS

883 (Human Body) Model	500 V
EIAJ Model	100 V

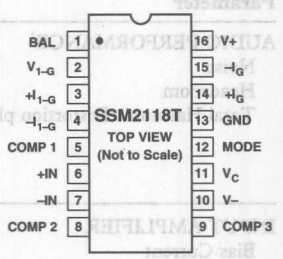
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP and device soldered in circuit board for SOIC package.

and SOL



and SOL



ORDERING GUIDE

Model	Temperature Range	Package Option*
SSM2018TN	–40°C to +85°C	N-16
SSM2018TR	–40°C to +85°C	R-16
SSM2118TN	–40°C to +85°C	N-16
SSM2118TR	–40°C to +85°C	R-16

*N = Plastic DIP; R = SOL. For outline information see Package Information section.

PRELIMINARY TECHNICAL DATA

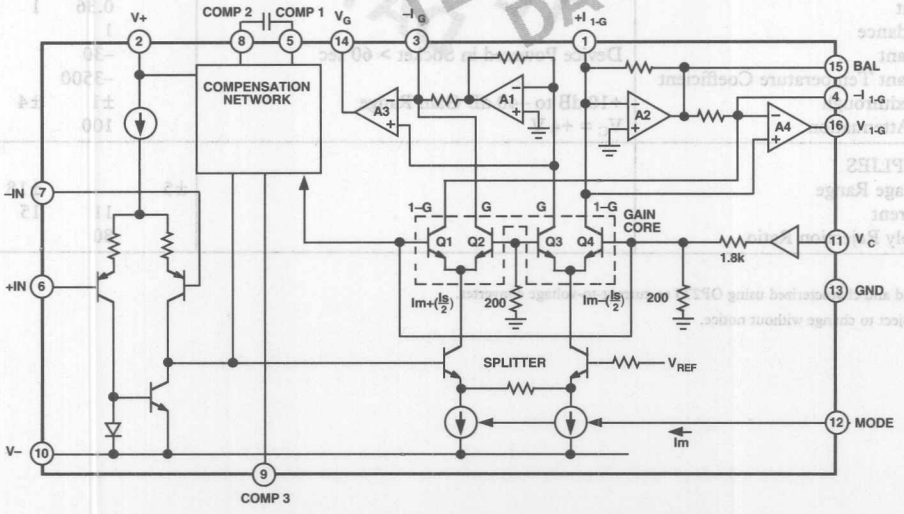


Figure 1. SSM2018T Detailed Functional Block Diagram

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2018T/SSM2118T features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

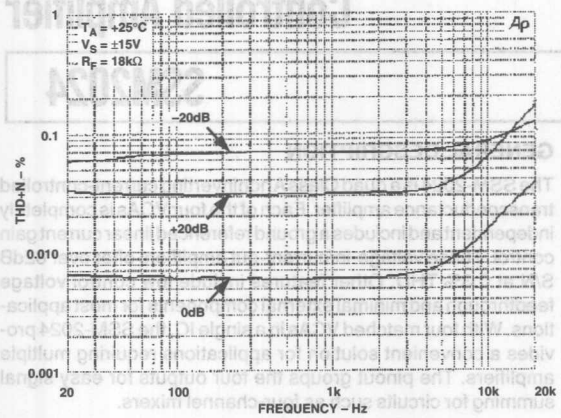


Figure 2. SSM2018T THD+N vs. Frequency (80 kHz Low-Pass Filter; for A_V = 0 dB, V_{IN} = 1 V rms; for A_V = +20 dB, V_{IN} = 0.1 V rms; for A_V = –20 dB, V_{IN} = 10 V rms)

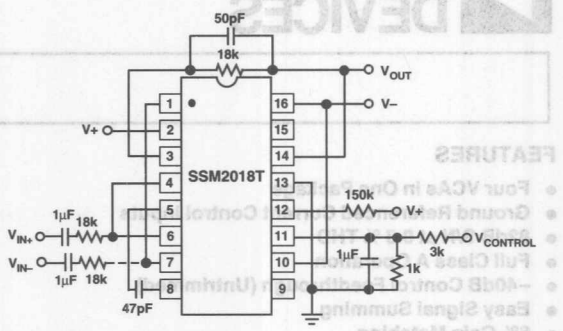
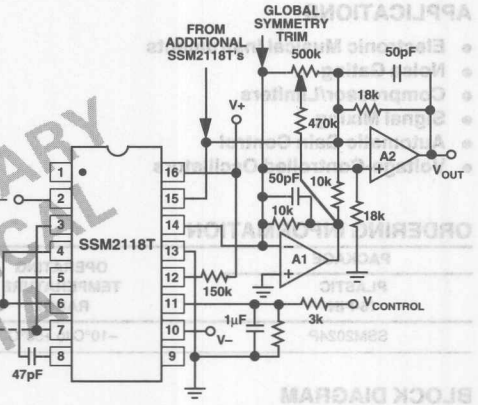


Figure 3. SSM2018T Typical Application Circuit



PRELIMINARY TECHNICAL DATA

Figure 5. SSM2118T Typical Application Circuit

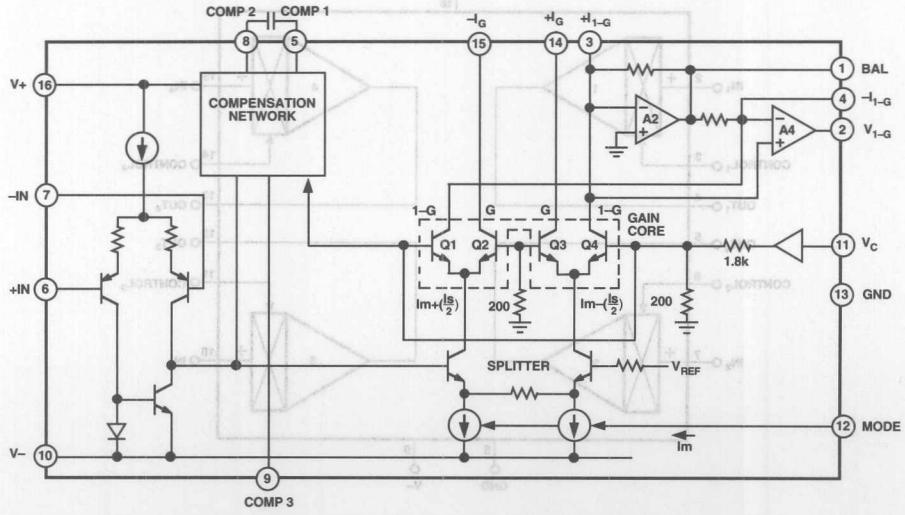


Figure 4. SSM2118T Detailed Functional Diagram

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Quad Current-Controlled Amplifier

SSM2024

FEATURES

- Four VCAs in One Package
- Ground Referenced Current Control Inputs
- 82dB S/N at 0.3 % THD
- Full Class A Operation
- –40dB Control Feedthrough (Untrimmed)
- Easy Signal Summing
- 6% Gain Matching

APPLICATIONS

- Electronic Musical Instruments
- Noise Gating
- Compressor/Limiters
- Signal Mixing
- Automatic Gain Control
- Voltage-Controlled Oscillators

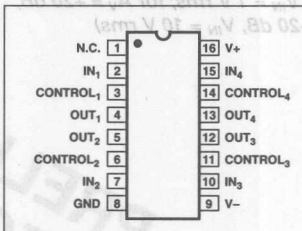
ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	
SSM2024P	–10°C to +50°C

GENERAL DESCRIPTION

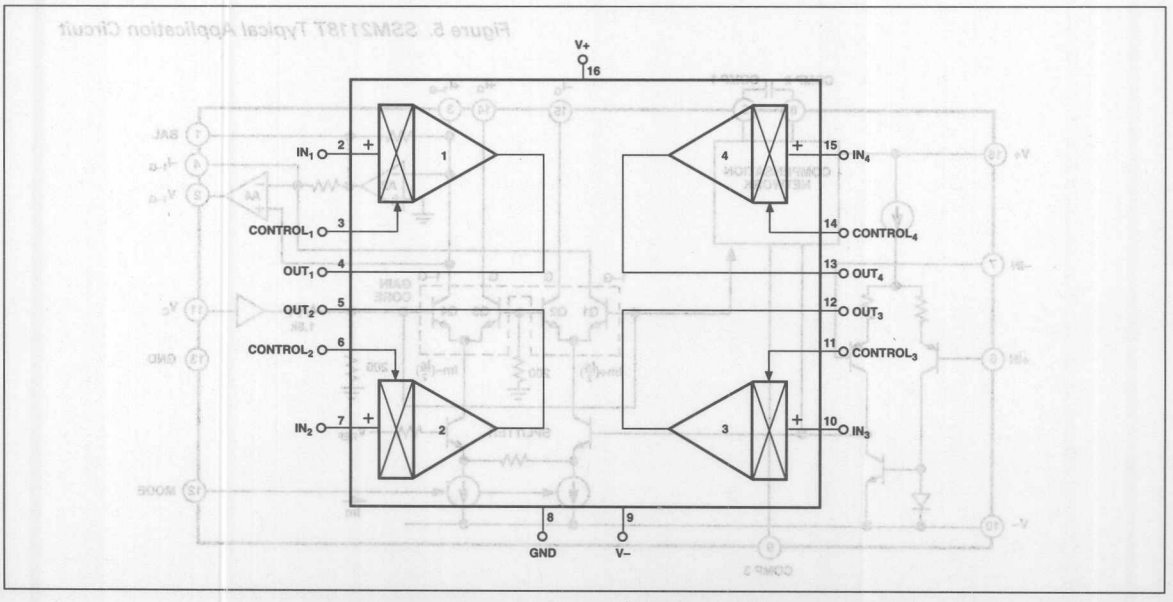
The SSM-2024 is a quad Class A noninverting current-controlled transconductance amplifier. Each of the four VCAs is completely independent and includes a ground referenced linear current gain control. These voltage-in/current-out amplifiers offer over 82dB S/N at 0.3% THD. Other features include low control voltage feedthrough and minimal external components for most applications. With four matched VCAs in a single IC, the SSM-2024 provides a convenient solution for applications requiring multiple amplifiers. The pinout groups the four outputs for easy signal summing for circuits such as four-channel mixers.

PIN CONNECTIONS



16-PIN PLASTIC DIP
(P-Suffix)

BLOCK DIAGRAM



The SSM-2024 is mask work protected under the Semiconductor Chip Protection Act of 1983.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 36V or ±18V
Junction Temperature ..... +150°C
Operating Temperature Range ..... –10 to +50°C
Storage Temperature Range ..... –65 to +150°C
Maximum Current into Any Pin 10mA
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
14-Pin Plastic DIP (P)	90	47	°C/W

NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			SSM-2024			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Current	$+I_{SY}$	I_{CON} (1-4) = 0 V_S = ±15V I_{CON} (1-4) = 0 V_S = ±16.5V	0.95 1.05	1.40 1.55	1.85 2.05	mA
Negative Supply Current	$-I_{SY}$	I_{CON} (1-4) = 0 V_S = ±15V I_{CON} (1-4) = 0 V_S = ±16.5V	1.05 1.20	1.55 1.65	2.05 2.25	mA
Gain	G	I_{CON} (1-4) = ±500µA	3842	4085	4330	µmhos
Gain Matching	ΔG	I_{CON} (1-4) = ±500µA	–	–	±6	%
Input Offset Voltage	V_{OS}	V_{IN} = 0V I_{CON} (1-4) = ±500µA I_{CON} (1-4) = +250µA	–	±.4	±1.3	mV
Change in Offset Voltage	ΔV_{OS}	+2.5µA ≤ I_{CON} (1-4) ≤ +250µA +250nA ≤ I_{CON} (1-4) ≤ +250µA	– –	±100 ±250	±840 ±840	µV
Output Leakage	I_{OL}	I_{CON} (1-4) = 0	–	0.1	±5	nA
Control Rejection (Untrimmed)	CVR	I_{CON} (1-4) = 500µA V_{IN} (1-4) = 40mV_{P-P}	30	41.5	–	dB
Signal-to-Noise	S/N	V_{IN} (1-4) = 40mV_{P-P}	–	82	–	dB
Distortion	THD	V_{IN} (1-4) = 40mV_{P-P}	–	0.3	–	%
Threshold Input Control Voltage	V_{TCI}	I_{OUT} (1-4) = 0	+160	–	+220	mV

NOTE: Specifications subject to change; consult latest data sheet.

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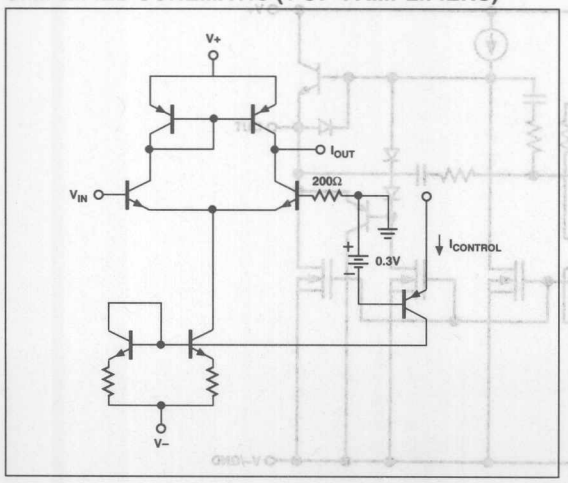
SIMPLIFIED SCHEMATIC (1 OF 4 AMPLIFIERS)



FEATURES

Excellent Sonic Characteristics
High Output Drive Capability
5.2 nV/$\sqrt{Hz}$ Equivalent Input Noise @ 1 kHz
0.001% THD+N (V_O = 2.5 V p-p @ 1 kHz)
3.5 MHz Gain Bandwidth
Unity-Gain Stable
Low Cost

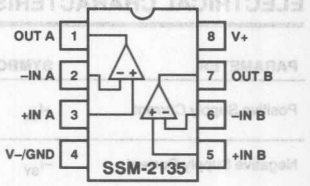
APPLICATIONS

Multimedia Audio Systems
Microphone Preamplifier
Headphone Driver
Differential Line Receiver
Balanced Line Driver
Audio ADC Input Buffer
Audio DAC I-V Converter and Filter
Pseudo-Ground Generator

PIN CONNECTIONS

8-Lead Narrow-Body SOIC (S Suffix)

8-Lead Epoxy DIP (P Suffix)



GENERAL DESCRIPTION

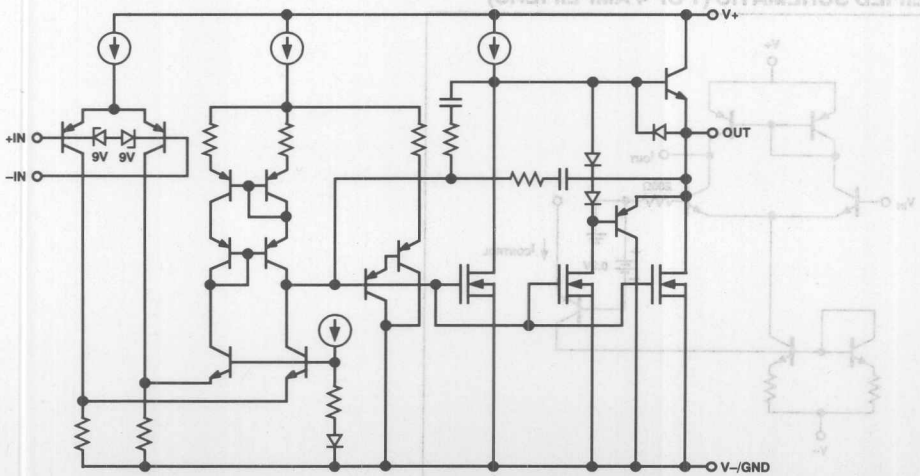
The SSM-2135 Dual Audio Operational Amplifier permits excellent performance in portable or low power audio systems, with an operating supply range of +4 V to +36 V or ±2 V to ±18 V. The unity gain stable device has very low voltage noise of 4.7 nV/$\sqrt{Hz}$, and total harmonic distortion plus noise below 0.01% over normal signal levels and loads. Such characteristics are enhanced by wide output swing and load drive capability. A unique output stage* permits output swing approaching the rail under moderate load conditions. Under severe loading, the SSM-2135 still maintains a wide output swing with ultralow distortion.

Particularly well suited for computer audio systems and portable digital audio units, the SSM-2135 can perform preamplification, headphone and speaker driving, and balanced line driving and receiving. Additionally, the device is ideal for input signal conditioning in single-supply sigma-delta analog-to-digital converter subsystems such as the AD1878/AD1879.

The SSM-2135 is available in 8-pin plastic DIP and SOIC packages, and is guaranteed for operation over the extended industrial temperature range of −40°C to +85°C.

*Protected by U. S. Patent No. 5,146,181.

FUNCTIONAL BLOCK DIAGRAM



SPECIFICATIONS

(V_S = +5 V, −40°C < T_A < +85°C unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		5.2		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.5		pA/√Hz
Signal-To-Noise Ratio	SNR	20 Hz to 20 kHz, 0 dBu = 0.775 V rms		121		dBu
Headroom	HR	Clip Point = 1% THD+N, f = 1 kHz, R_L = 10 kΩ		5.3		dBu
Total Harmonic Distortion	THD+N	A_V = +1, V_O = 1 V p-p, f = 1 kHz, 80 kHz LPF				
		R_L = 10 kΩ		0.003		%
		R_L = 32 Ω		0.005		%
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, T_A = +25°C	0.6	0.9		V/μs
Gain Bandwidth Product	GBW			3.5		MHz
Settling Time	t_S	to 0.1%, 2 V Step		5.8		μs
INPUT CHARACTERISTICS						
Input Voltage Range	V_{CM}		0		+4.0	V
Input Offset Voltage	V_{OS}	V_{OUT} = 2 V		0.2	2.0	mV
Input Bias Current	I_B	V_{CM} = 0 V, V_{OUT} = 2 V		300	750	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V, V_{OUT} = 2 V			50	nA
Differential Input Impedance	Z_{IN}			4		MΩ
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 4 V, f = dc	87	112		dB
Large Signal Voltage Gain	A_{VO}	0.01 V ≤ V_{OUT} ≤ 3.9 V, R_L = 600 Ω	2			V/μV
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 100 kΩ	4.1			V
		R_L = 600 Ω	3.9			V
Output Voltage Swing Low	V_{OL}	R_L = 100 kΩ			3.5	mV
		R_L = 600 Ω			3.0	mV
Short Circuit Current Limit	I_{SC}			±30		mA
POWER SUPPLY						
Supply Voltage Range	V_S	Single Supply	+4		+36	V
		Dual Supply	±2		±18	V
Power Supply Rejection Ratio	PSRR	V_S = +4 V to +6 V, f = dc	90	120		dB
Supply Current	I_{SY}	V_{OUT} = 2.0 V, No Load				
		V_S = +5 V		2.8	4.0	mA
		V_S = ±18 V		3.7	5.0	mA

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- Single Supply . . . . . +36 V
- Dual Supply . . . . . ±18 V

Input Voltage . . . . . ±V_S
Differential Input Voltage . . . . . 10 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . −40°C to +85°C
Junction Temperature Range (T_J) . . . . . −65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

ESD RATINGS

883 (Human Body) Model . . . . . 1 kV
EIAJ Model . . . . . 175 V

THERMAL CHARACTERISTICS

Thermal Resistance[1]		
8-Pin Plastic DIP	θ_{JA}	103°C/W
	θ_{JC}	43°C/W
8-Pin SOIC	θ_{JA}	158°C/W
	θ_{JC}	43°C/W

[1]θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP and device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
SSM2135P	−40°C to +85°C	8-Pin Plastic DIP	N-8
SSM2135S	−40°C to +85°C	8-Pin Narrow Body	SO-8

*For outline information see Package Information section.

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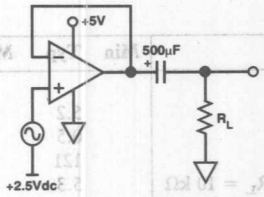

Figure 1. Test Circuit for Figures 2–4

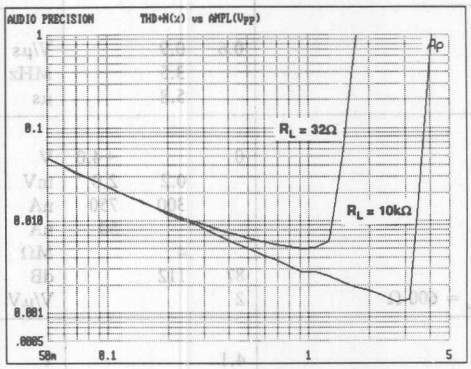

Figure 2. THD+N vs. Amplitude (See Test Circuit; A_V = +1, V_S = +5 V, f = 1 kHz, with 80 kHz Low-Pass Filter)

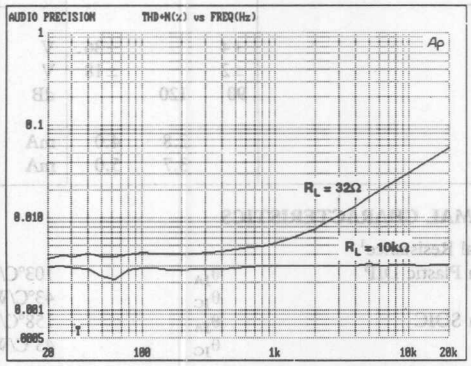

Figure 3. THD+N vs. Frequency (See Test Circuit; A_V = +1, V_{IN} = 1 V p-p, with 80 kHz Low-Pass Filter)

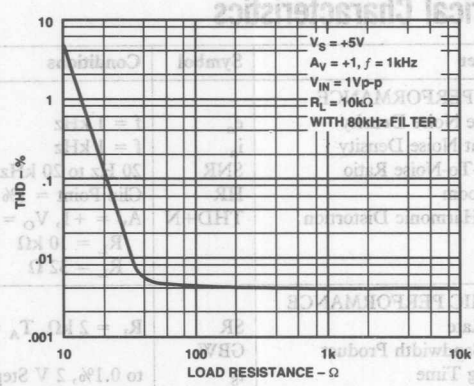

Figure 4. THD+N vs. Load (See Test Circuit)

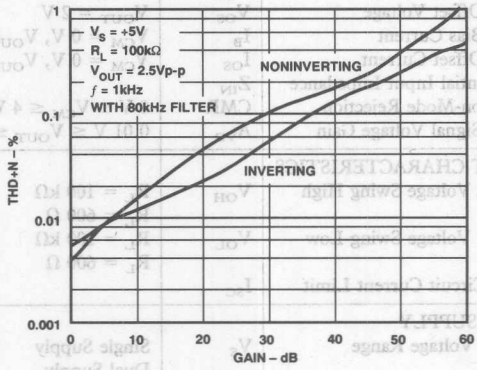

Figure 5. THD+N vs. Gain

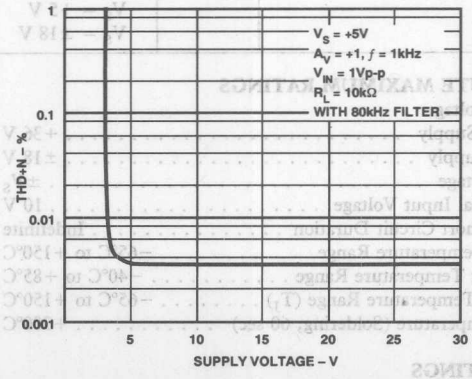

Figure 6. THD+N vs. Supply Voltage

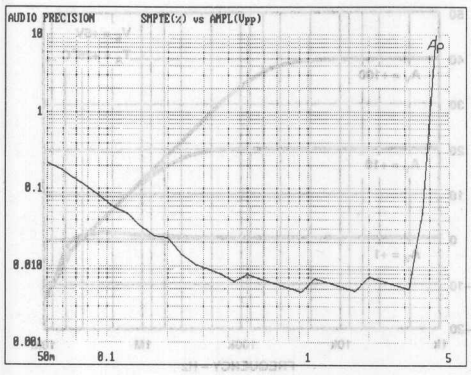

Figure 7. SMPTE Intermodulation Distortion (A_V = +1, V_S = +5 V, f = 1 kHz, R_L = 10 kΩ)

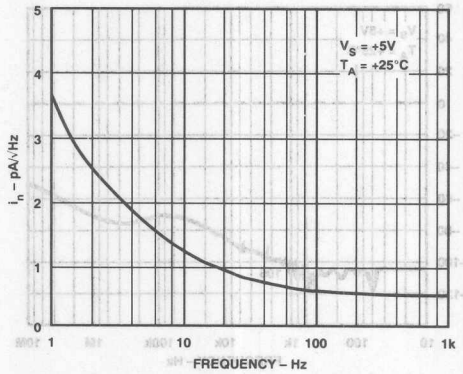

Figure 10. Current Noise Density vs. Frequency

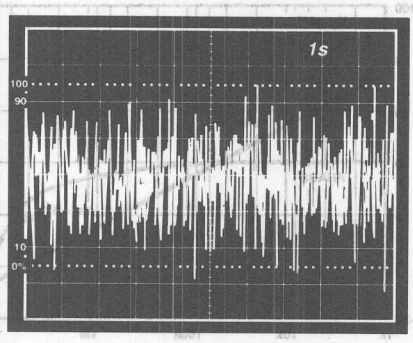

Figure 8. Input Voltage Noise (20 nV/div)

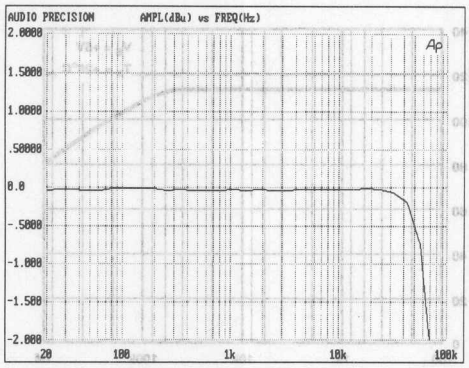

Figure 11. Frequency Response (A_V = +1, V_S = +5 V, V_{IN} = 1 V p-p, R_L = 10 kΩ)

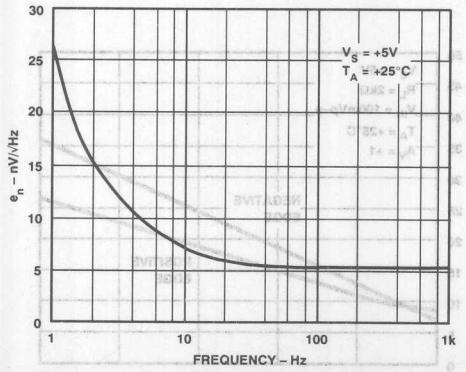

Figure 9. Voltage Noise Density vs. Frequency

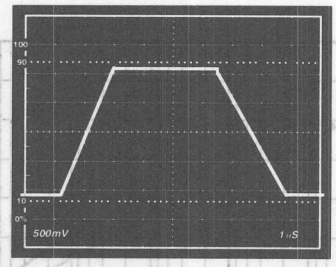

Figure 12. Square Wave Response (V_S = +5 V, A_V = +1, R_L = ∞)

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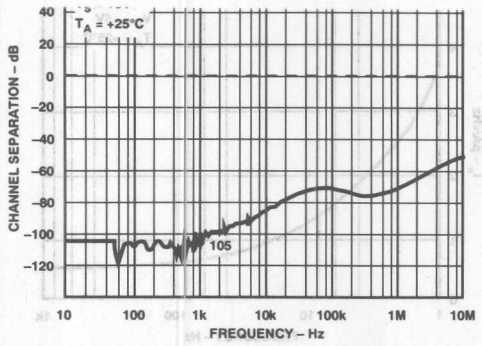

Figure 13. Crosstalk vs. Frequency (R_L = 10 kΩ)

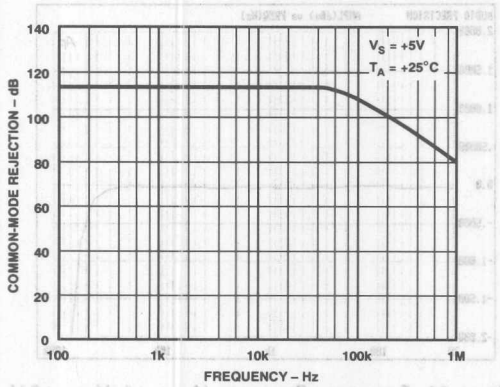

Figure 14. Common-Mode Rejection vs. Frequency

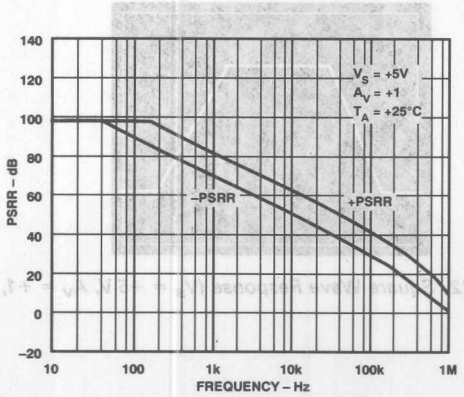

Figure 15. Power Supply Rejection vs. Frequency

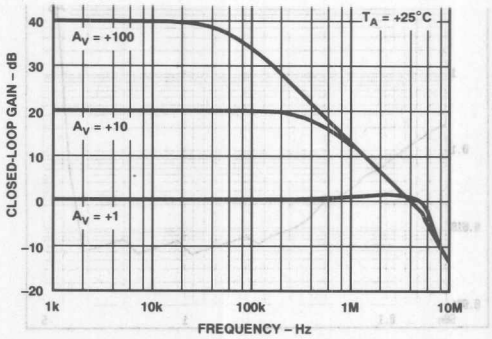

Figure 16. Closed-Loop Gain vs. Frequency

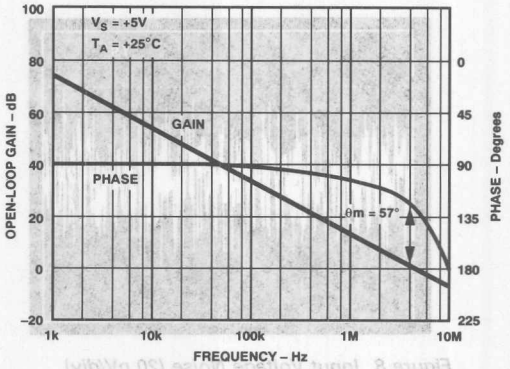

Figure 17. Open-Loop Gain and Phase vs. Frequency

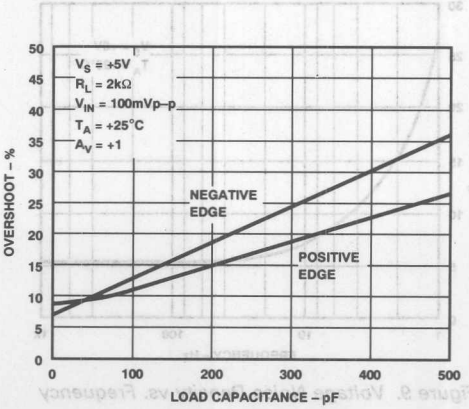

Figure 18. Small Signal Overshoot vs. Load Capacitance

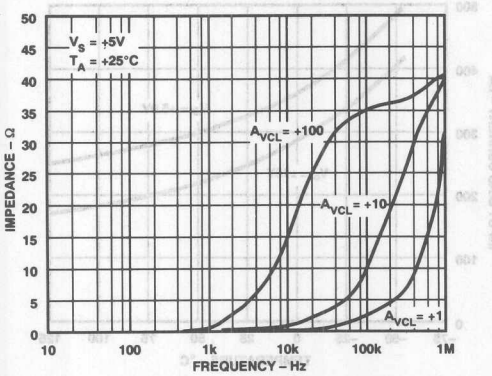

Figure 19. Output Impedance vs. Frequency

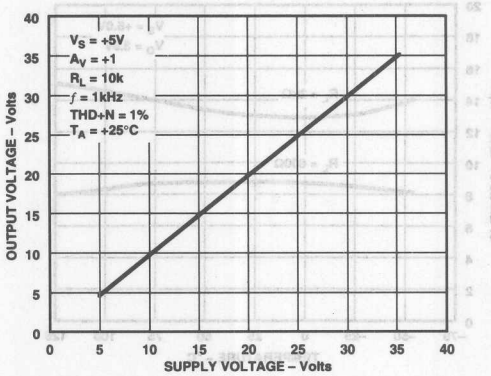

Figure 22. Output Swing vs. Supply Voltage

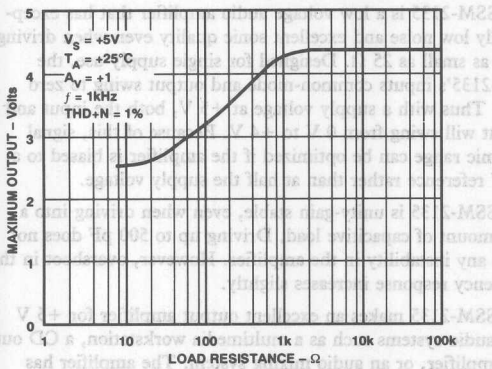

Figure 20. Maximum Output Voltage vs. Load Resistance

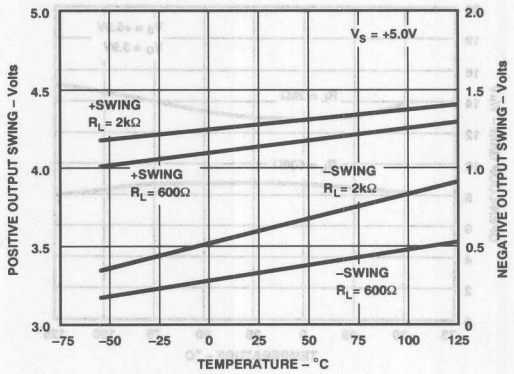

Figure 23. Output Swing vs. Temperature and Load

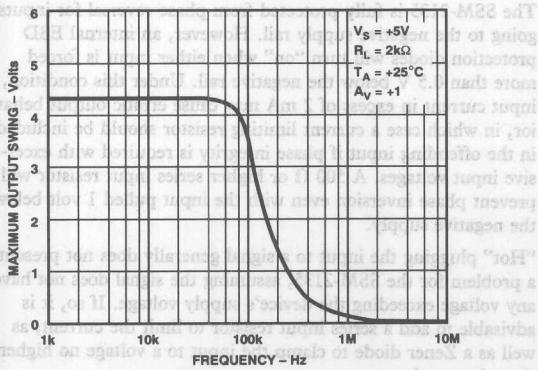

Figure 21. Maximum Output Swing vs. Frequency

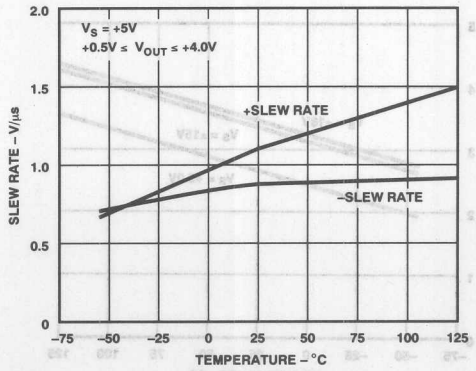

Figure 24. Slew Rate vs. Temperature

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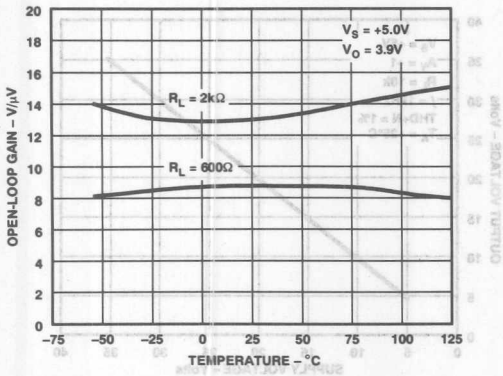

Figure 25. Open-Loop Gain vs. Temperature

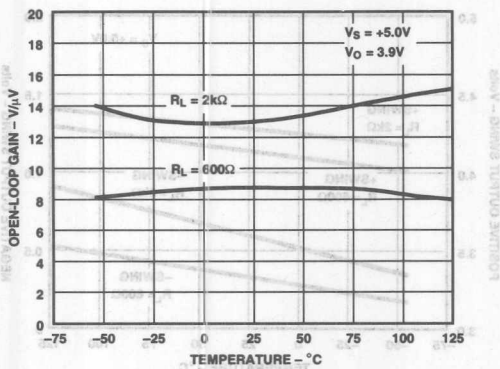

Figure 26. Gain Bandwidth Product and Phase Margin vs. Temperature

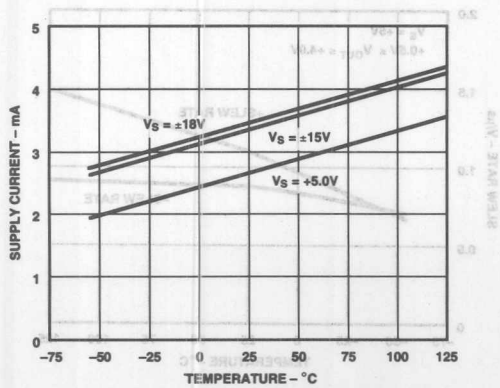

Figure 27. Supply Current vs. Temperature

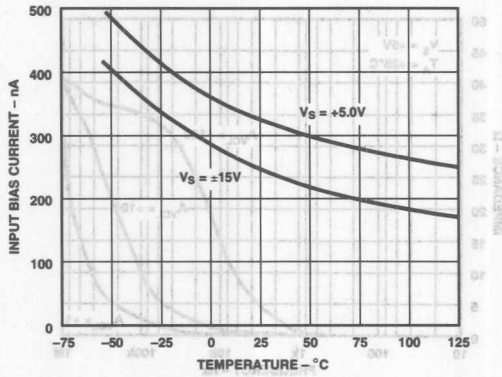

Figure 28. Input Bias Current vs. Temperature

APPLICATION INFORMATION

The SSM-2135 is a low voltage audio amplifier that has exceptionally low noise and excellent sonic quality even when driving loads as small as 25 Ω. Designed for single supply use, the SSM-2135's inputs common-mode and output swing to zero volts. Thus with a supply voltage at +5 V, both the input and output will swing from 0 V to +4 V. Because of this, signal dynamic range can be optimized if the amplifier is biased to a +2 V reference rather than at half the supply voltage.

The SSM-2135 is unity-gain stable, even when driving into a fair amount of capacitive load. Driving up to 500 pF does not cause any instability in the amplifier. However, overshoot in the frequency response increases slightly.

The SSM-2135 makes an excellent output amplifier for +5 V only audio systems such as a multimedia workstation, a CD output amplifier, or an audio mixing system. The amplifier has large output swing even at this supply voltage because it is designed to swing to the negative rail. In addition, it easily drives load impedances as low as 25 Ω with low distortion.

The SSM-2135 is fully protected from phase reversal for inputs going to the negative supply rail. However, an internal ESD protection diodes will turn "on" when either input is forced more than 0.5 V below the negative rail. Under this condition, input current in excess of 2 mA may cause erratic output behavior, in which case a current limiting resistor should be included in the offending input if phase integrity is required with excessive input voltages. A 500 Ω or higher series input resistor will prevent phase inversion even with the input pulled 1 volt below the negative supply.

"Hot" plugging the input to a signal generally does not present a problem for the SSM-2135, assuming the signal does not have any voltage exceeding the device's supply voltage. If so, it is advisable to add a series input resistor to limit the current, as well as a Zener diode to clamp the input to a voltage no higher than the supply.

APPLICATION CIRCUITS

A Low Noise Stereo Headphone Driver Amplifier

Figure 29 shows the SSM-2135 used in a stereo headphone driver for multimedia applications with the AD1848, a 16-bit stereo codec. The SSM-2135 is equally well suited for the serial-bused AD1849 stereo codec. The headphone's impedance can be as low as 25 Ω, which covers most commercially available high fidelity headphones. Although the amplifier can operate at up to ±18 V supply, it is just as efficient powered by a single +5 V. At this voltage, the amplifier has sufficient output drive to deliver distortion-free sound to a low impedance headphone.

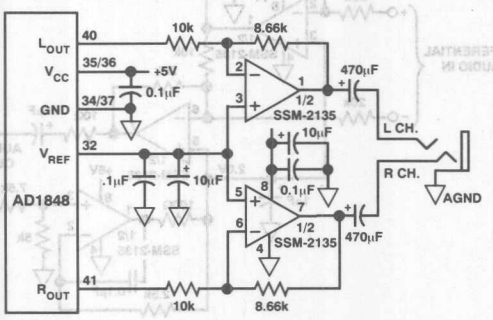

Figure 29. A Stereo Headphone Driver for Multimedia Sound Codec

Figure 30 shows the total harmonic distortion characteristics versus frequency driving into a 32 Ω load, which is a very typical impedance for a high quality stereo headphone. The SSM-2135 has excellent power supply rejection, and as a result, is tolerant of poorly regulated supplies. However, for best sonic quality, the power supply should be well regulated and heavily bypassed to minimize supply modulation under heavy loads. A minimum of 10 μF bypass is recommended.

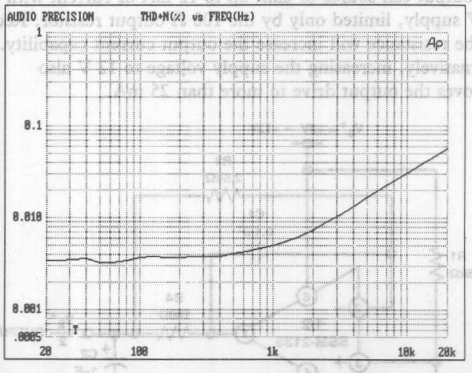

Figure 30. Headphone Driver THD+N vs. Frequency into a 32 Ω Load (V_S = +5 V, with 80 kHz Low-Pass Filter)

A Low Noise Microphone Preamplifier

The SSM-2135's 4.7 nV/$\sqrt{Hz}$ input noise in conjunction with low distortion makes it an ideal device for amplifying low level signals such as those produced by microphones. Figure 31 illustrates a stereo microphone input circuit feeding a multimedia sound codec. As shown, the gain is set at 100 (40 dB), although it can be set to other gains depending on the microphone output levels. Figure 32 shows the preamplifier's harmonic distortion performance with 1 V rms output while operating from a single +5 V supply.

The SSM-2135 is biased to 2.25 V by the V_{REF} pin of the AD1848 codec. The same voltage is buffered by the 2N4124 transistor to provide "phantom power" to the microphone. A typical electret condenser microphone with an impedance range of 100 Ω to 1 kΩ works well with the circuit. This power booster circuit may be omitted for dynamic microphone elements.

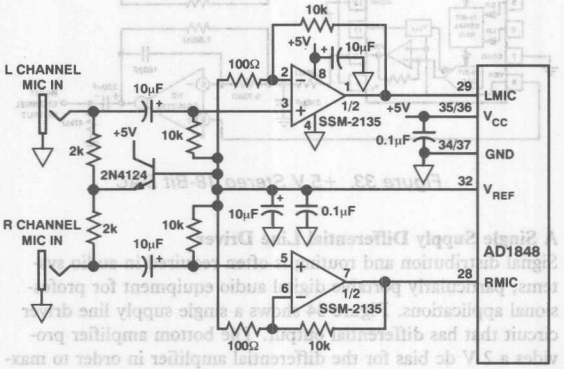

Figure 31. Low Noise Microphone Preamp for Multimedia Sound Codec

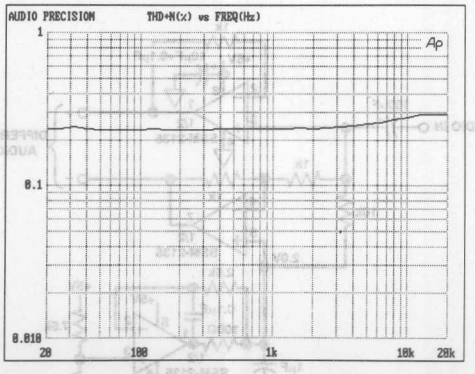

Figure 32. MIC Preamp THD+N Performance (V_S = +5 V, A_V = 40 dB, V_{OUT} = 1 V rms, with 80 kHz Low-Pass Filter)

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amplifier for audio D/A converters because of its low noise and distortion. Figure 33 shows the implementation of an 18-Bit stereo DAC channel. The output amplifier also provides low-pass filtering for smoothing the oversampled audio signal. The filter's cutoff frequency is set at 22.5 kHz and it has a maximally flat response from dc to 20 kHz.

As mentioned above, the amplifier's outputs can drive directly into a stereo headphone that has impedance as low as 25 Ω with no additional buffering required.

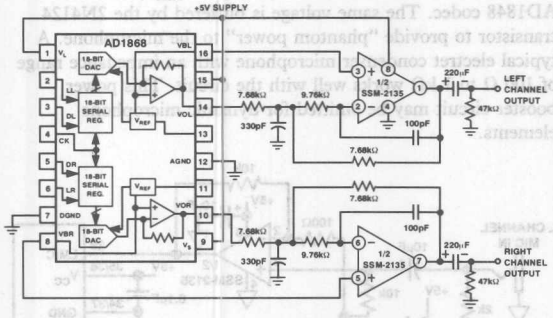

Figure 33. +5 V Stereo 18-Bit DAC

A Single Supply Differential Line Driver

Signal distribution and routing is often required in audio systems, particularly portable digital audio equipment for professional applications. Figure 34 shows a single supply line driver circuit that has differential output. The bottom amplifier provides a 2 V dc bias for the differential amplifier in order to maximize the output swing range. The amplifier can output a maximum of 0.8 V rms signal with a +5 V supply. It is capable of driving into 600 Ω line termination at a reduced output amplitude.

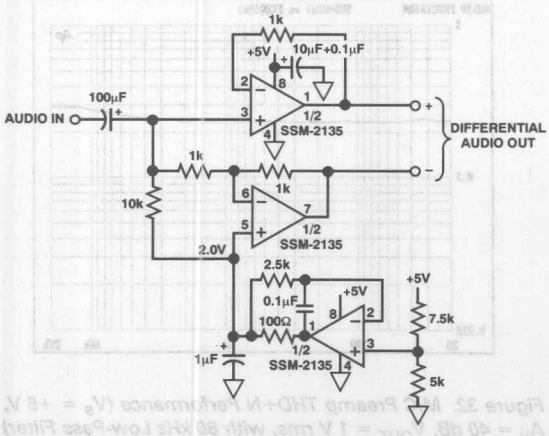

Figure 34. Single Supply Differential Line Driver

achieved using the circuit in Figure 35. Unlike a difference amplifier (a subtractor), the circuit has a true balanced input impedance regardless of input drive levels. That is, each input always presents a 20 kΩ impedance to the source. For best common-mode rejection performance, all resistors around the differential amplifier must be very well matched. Best results can be achieved using a 10 kΩ precision resistor network.

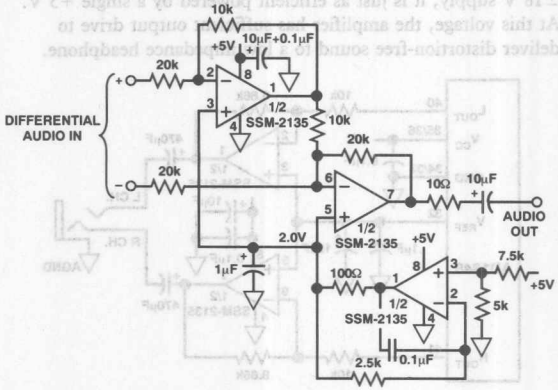

Figure 35. Single Supply Balanced Differential Line Receiver

A Pseudo-Reference Voltage Generator

For single supply circuits, a reference voltage source is often required for biasing purposes or signal offsetting purposes. The circuit in Figure 36 provides a supply splitter function with low output impedance. The 1 μF output capacitor serves as a charge reservoir to handle a sudden surge in demand by the load as well as providing a low ac impedance to it. The 0.1 μF feedback capacitor compensates the amplifier in the presence of a heavy capacitive load, maintaining stability.

The output can source or sink up to 12 mA of current with +5 V supply, limited only by the 100 Ω output resistor. Reducing the resistance will increase the output current capability. Alternatively, increasing the supply voltage to 12 V also improves the output drive to more than 25 mA.

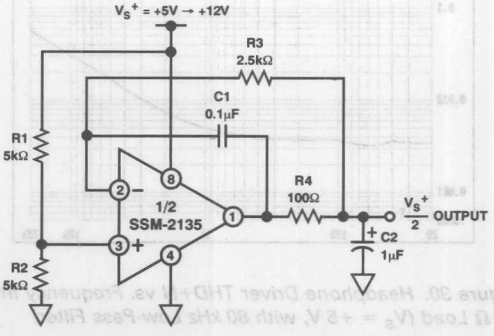

Figure 36. Pseudo-Reference Generator

D/A converter, the SSM-2135 makes for an efficient audio attenuator, as shown in Figure 37. The circuit works off a single +5 V supply. The DAC's are biased to a 2 V reference level which is sufficient to keep the DAC's internal R-2R ladder switches operating properly. This voltage is also the optimal midpoint of the SSM-2135's common-mode and output swing range. With the circuit as shown, the maximum input and output swing is 1.25 V rms. Total harmonic distortion measures a respectable 0.01% at 1 kHz and 0.1% at 20 kHz. The frequency response at any attenuation level is flat to 20 kHz.

Each DAC can be controlled independently via the 8-bit parallel data bus. The attenuation level is linearly controlled by the binary weighting of the digital data input. Total attenuation ranges from 0 dB to −48 dB.

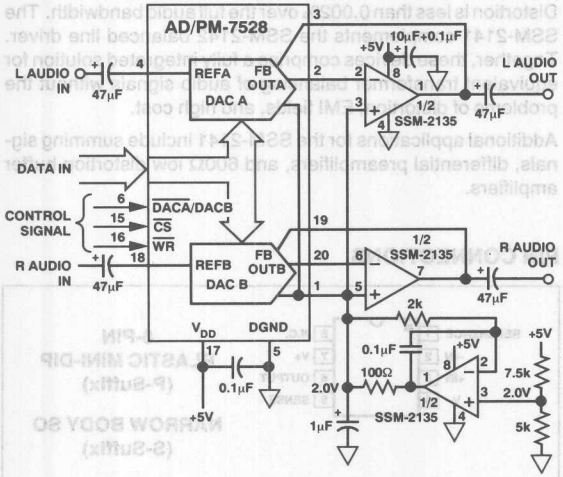

Figure 37. Digital Volume Control

function. Similar biasing is used. With an 8-bit bus, the AD7111 provides an 88.5 dB attenuation range. Each bit resolves a 0.375 dB attenuation. Refer to AD7111 data sheet for attenuation levels for each input code.

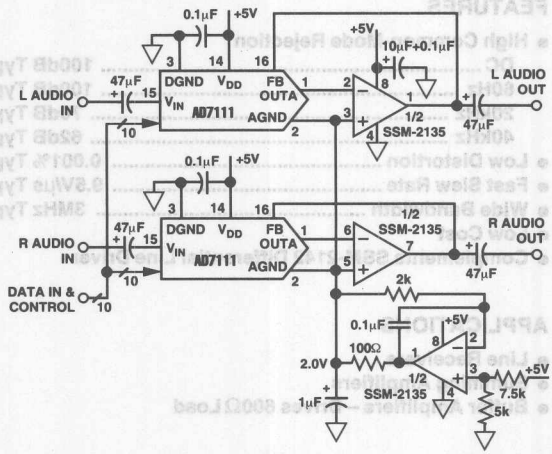

Figure 38. Single Supply Logarithmic Volume Control

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High Common-Mode Rejection Differential Line Receiver

SSM2141

FEATURES

- **High Common-Mode Rejection**
  - **DC ..... 100dB Typ**
  - **60Hz ..... 100dB Typ**
  - **20kHz ..... 70dB Typ**
  - **40kHz ..... 62dB Typ**
- **Low Distortion ..... 0.001% Typ**
- **Fast Slew Rate ..... 9.5V/µs Typ**
- **Wide Bandwidth ..... 3MHz Typ**
- **Low Cost**
- **Complements SSM-2142 Differential Line Driver**

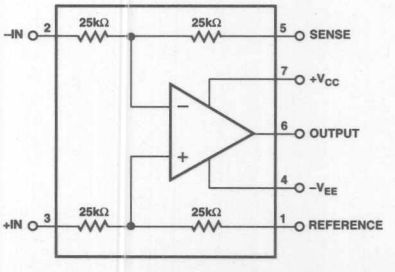
APPLICATIONS

- **Line Receivers**
- **Summing Amplifiers**
- **Buffer Amplifiers – Drives 600Ω Load**

ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	NARROW BODY SO 8-PIN	
SSM2141P	SSM2141S	XIND (–40°C ≤ T_A ≤ +85°C)

FUNCTIONAL DIAGRAM



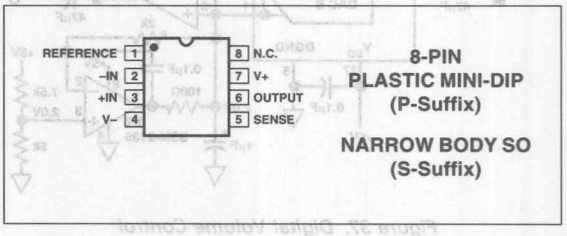
GENERAL DESCRIPTION

The SSM-2141 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of noise immunity and optimum common-mode rejection. The SSM-2141 typically achieves 100dB of common-mode rejection (CMR), whereas implementing an op amp with four off-the-shelf precision resistors will typically achieve only 40dB of CMR – inadequate for high-performance audio.

The SSM-2141 achieves low distortion performance by maintaining a large slew rate of 9.5V/µs and high open-loop gain. Distortion is less than 0.002% over the full audio bandwidth. The SSM-2141 complements the SSM-2142 balanced line driver. Together, these devices comprise a fully integrated solution for equivalent transformer balancing of audio signals without the problems of distortion, EMI fields, and high cost.

Additional applications for the SSM-2141 include summing signals, differential preamplifiers, and 600Ω low distortion buffer amplifiers.

PIN CONNECTIONS



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage (Note 1) ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P Package ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... +150°C
Operating Temperature Range ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	103	43	°C/W

NOTES:
1. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±18V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2141 MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}	V_{CM} = 0V	–1000	25	1000	µV
Gain Error		No Load, V_{IN} = ±10V, R_S = 0Ω	–	0.001	0.01	%
Input Voltage Range	IVR	(Note 1)	±10	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±10V	80	100	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	–	0.7	15	µV/V
Output Swing	V_O	R_L = 2kΩ	±13	±14.7	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted To Ground	+45/–15	–	–	mA
Small-Signal Bandwidth (–3dB)	BW	R_L = 2kΩ	–	3	–	MHz
Slew Rate	SR	R_L = 2kΩ	6	9.5	–	V/µs
Total Harmonic Distortion	THD	R_L = 100kΩ	–	0.001	–	%
		R_L = 600Ω	–	0.01	–	
Capacitive Load Drive Capability	C_L	No Oscillation	–	300	–	pF
Supply Current	I_{SY}	No Load	–	2.5	3.5	mA

NOTE:
1. Input voltage range guaranteed by CMR test.

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ELECTRICAL CHARACTERISTICS at V_S = ±18V, –40°C ≤ T_A ≤ +85°C.

PARAMETER	SYMBOL	CONDITIONS	SSM-2141 MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}	V_{CM} = 0V	–2500	200	2500	µV
Gain Error		No Load, V_{IN} = ±10V, R_S = 0Ω	–	0.002	0.02	%
Input Voltage Range	IVR	(Note 1)	±10	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±10V	75	90	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	–	1.0	20	µV/V
Output Swing	V_O	R_L = 2kΩ	±13	±14.7	–	V
Slew Rate	SR	R_L = 2kΩ	–	9.5	–	V/µs
Supply Current	I_{SY}	No Load	–	2.6	4.0	mA

NOTE:
1. Input voltage range guaranteed by CMR test.

ANALOG DEVICES

Balanced Line Driver

SSM2142

FEATURES

- Transformer-Like Balanced Output
- Drives 10 V RMS Into a 600 Ω Load
- Stable When Driving Large Capacitive Loads and Long Cables
- Low Distortion
  - 0.006% typ 20 Hz-20 kHz, 10 V RMS into 600 Ω
- High Slew Rate
  - 15 V/μs typ
- Low Gain Error
  - (Differential or Single-Ended); 0.7% typ
- Outputs Short-Circuit Protected
- Available In Space-Saving 8-Pin Mini-DIP Package
- Low Cost

APPLICATIONS

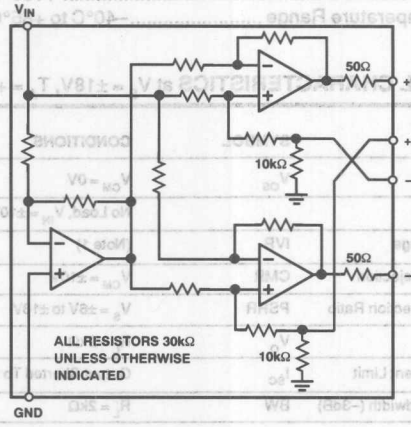
- Audio Mix Consoles
- Distribution Amplifiers
- Graphic and Parametric Equalizers
- Dynamic Range Processors
- Digital Effects Processors
- Telecommunications Systems
- Industrial Instrumentation
- Hi-Fi Equipment

GENERAL DESCRIPTION

The SSM-2142 is an integrated differential-output buffer amplifier that converts a single-ended input signal to a balanced output signal pair with high output drive. By utilizing low noise thermally matched thin film resistors and high slew rate amplifiers, the SSM-2142 helps maintain the sonic quality of audio systems by eliminating power line hum, RF interference, voltage drops, and other externally generated noise commonly encountered with long audio cable runs. Excellent rejection of common-mode noise and offset errors is achieved by laser trimming of the onboard resistors, assuring high gain accuracy. The carefully designed output stage of the SSM-2142 is capable of driving difficult loads, yielding low-distortion performance despite extremely long cables or loads as low as 600 Ω, and is stable over a wide range of operating conditions.

Based on a cross-coupled, electronically balanced topology, the SSM-2142 mimics the performance of fully balanced transformer-based solutions for line driving. However, the SSM-2142 maintains lower distortion and occupies much less board space than transformers while achieving comparable common-mode rejection performance with reduced parts count.

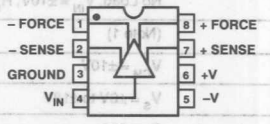
FUNCTIONAL BLOCK DIAGRAM



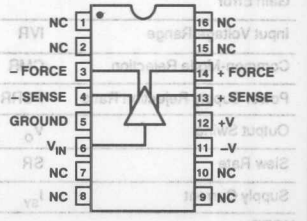
The SSM-2142 in tandem with the SSM-2141 differential receiver establishes a complete, reliable solution for driving and receiving audio signals over long cables. The SSM-2141 features an Input Common-Mode Rejection Ratio of 100 dB at 60 Hz. Specifications demonstrating the performance of this typical system are included in the data sheet.

PIN CONNECTIONS

8-Pin Plastic DIP
(P Suffix)
8-Pin Cerdip
(Z Suffix)



16-Pin
Wide Body SOL
(S Suffix)



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SPECIFICATIONS

(V_S = ±18 V, −40°C ≤ T_A ≤ +85°C, operating in differential mode unless indicated otherwise. Typical characteristics apply to operation at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT IMPEDANCE	Z_{IN}			10		kΩ
INPUT CURRENT	I_{IN}	V_{IN} = ±7.071 V		±750	±900	μA
GAIN, DIFFERENTIAL			5.8	5.98		dB
GAIN, SINGLE-ENDED		Single-Ended Mode	5.7	5.94		dB
GAIN ERROR, DIFFERENTIAL		R_L = 600 Ω		0.7	2	%
POWER SUPPLY REJECTION RATIO STATIC	PSRR	V_S = ±13 V to ±18 V	60	80		dB
OUTPUT COMMON-MODE REJECTION	OCMR	See Test Circuit; f = 1 kHz	−38	−45		dB
OUTPUT SIGNAL BALANCE RATIO	SBR	See Test Circuit; f = 1 kHz	−35	−40		dB
TOTAL HARMONIC DISTORTION Plus Noise	THD+N	20 Hz to 20 kHz, V_O = 10 V rms, R_L = 600 Ω		0.006		%
SIGNAL-TO-NOISE RATIO	SNR	V_{IN} = 0 V		−93.4		dBu
HEADROOM	HR	CLIP Level = 10.5 V rms		+93.4		dBu
SLEW RATE	SR			15		V/μs
OUTPUT COMMON-MODE VOLTAGE OFFSET[1]	V_{OOS}	R_L = 600 Ω	−250	25	250	mV
DIFFERENTIAL OUTPUT VOLTAGE OFFSET	V_{OOD}	R_L = 600 Ω	−50	15	50	mV
DIFFERENTIAL OUTPUT VOLTAGE SWING		V_{IN} = ±7.071 V	±13.8	±14.14		V
OUTPUT IMPEDANCE	Z_O		45	50	55	Ω
SUPPLY CURRENT	I_{SY}	Unloaded, V_{IN} = 0 V		5.5	7.0	mA
OUTPUT CURRENT, SHORT CIRCUIT	I_{SC}		60	70		mA

NOTE
[1]Output common-mode offset voltage can be removed by inserting dc blocking capacitors in the sense lines. See the Applications Information.
Specifications subject to change without notice.

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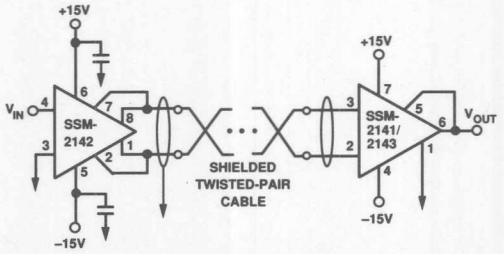
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±18 V
Storage Temperature . . . . . −60°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C
Junction Temperature . . . . . +150°C
Operating Temperature Range . . . . . −40°C to +85°C
Output Short Circuit Duration (Both Outputs) . . . . . Indefinite

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



Typical Application of the SSM-2142 and SSM-2141

ORDERING GUIDE

Model	Operating Temperature Range	Package Description	Package Option[1]
SSM2142P	−40°C to +85°C	Plastic DIP	N-8
SSM2142Z	−40°C to +85°C	Cerdip	Q-8
SSM2142S[2]	−40°C to +85°C	SOL	R-16

NOTES
[1]For outline information see Package Information section.
[2]For availability of SOIC package, contact your local sales office.

SSM2143

FEATURES

High Common-Mode Rejection
- **DC: 90 dB typ**
- **60 Hz: 90 dB typ**
- **20 kHz: 85 dB typ**

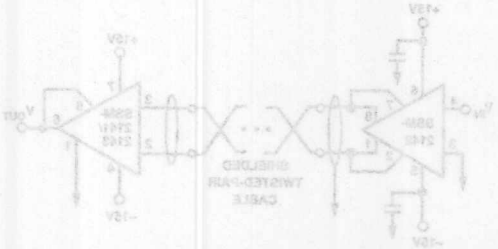
Ultralow THD: 0.0006% typ @ 1 kHz
Fast Slew Rate: 10 V/μs typ
Wide Bandwidth: 7 MHz typ (G = 1/2)
Two Gain Levels Available: G = 1/2 or 2
Low Cost

GENERAL DESCRIPTION

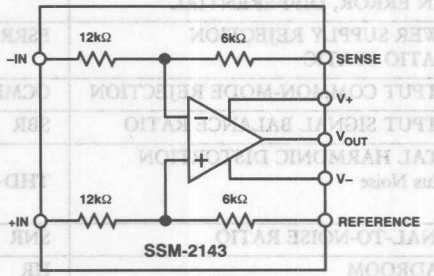
The SSM-2143 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of immunity from common-mode noise. The device provides a typical 90 dB of common-mode rejection (CMR), which is achieved by laser trimming of resistances to better than 0.005%.

Additional features of the device include a slew rate of 10 V/μs and wide bandwidth. Total harmonic distortion (THD) is less than 0.004% over the full audio band, even while driving low impedance loads. The SSM-2143 input stage is designed to handle input signals as large as +28 dBu at G = 1/2. Although primarily intended for G = 1/2 applications, a gain of 2 can be realized by reversing the +IN/−IN and SENSE/REFERENCE connections.

When configured for a gain of 1/2, the SSM-2143 and SSM-2142 Balanced Line Driver provide a fully integrated, unity gain solution to driving audio signals over long cable runs.

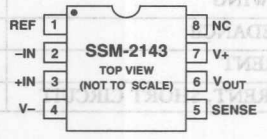


FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS

Epoxy Mini-DIP (P Suffix)
and
SOIC (S Suffix)



NC = NO CONNECT

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SPECIFICATIONS (V_S = ±15 V, −40°C ≤ T_A ≤ +85°C, G = 1/2 unless otherwise specified)

Signal-to-Noise Ratio	SNR	0 dBu = 0.775 V rms, 20 kHz BW, RTI		−107.3		dBu
Headroom	HR	Clip Point = 1% THD+N		+28.0		dBu
DYNAMIC RESPONSE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 200 pF	6	10		V/μs
Small Signal Bandwidth	$BW_{-3\ dB}$	R_L = 2 kΩ, C_L = 200 pF				
		G = 1/2		7		MHz
		G = 2		3.5		MHz
INPUT						
Input Offset Voltage	V_{IOS}	V_{CM} = 0 V, RTI, G = 2	−1.2	0.05	+1.2	mV
Common-Mode Rejection	CMR	V_{CM} = ±10 V, RTO				
		f = dc	70	90		dB
		f = 60 Hz		90		dB
		f = 20 kHz		85		dB
		f = 400 kHz		60		dB
Power Supply Rejection	PSR	V_S = ±6 V to ±18 V	90	110		dB
Input Voltage Range	IVR	Common Mode		±15		V
		Differential		±28		V
OUTPUT						
Output Voltage Swing	V_O	R_L = 2 kΩ	±13	±14		V
Minimum Resistive Load Drive				2		kΩ
Maximum Capacitive Load Drive				300		pF
Short Circuit Current Limit	I_{SC}			+45, −20		mA
GAIN						
Gain Accuracy			−0.1	0.03	0.1	%
REFERENCE INPUT						
Input Resistance				18		kΩ
Voltage Range				±10		V
POWER SUPPLY						
Supply Voltage Range	V_S		±6		±18	V
Supply Current	I_{SY}	V_{CM} = 0 V, R_L = ∞		±2.7	±4.0	mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Common-Mode Input Voltage . . . . . ±22 V
Differential Input Voltage . . . . . ±44 V
Output Short Circuit Duration . . . . . Continuous
Operating Temperature Range . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature (Tj) . . . . . +150°C
Lead Temperature (Soldering, 60 sec.) . . . . . +300°C
Thermal Resistance
8-Pin Plastic DIP (P): θ_{JA} = 103, θ_{JC} = 43 . . . . . °C/W
8-Pin SOIC (S): θ_{JA} = 150, θ_{JC} = 43 . . . . . °C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
SSM2143P	−40°C to +85°C	8-Pin Plastic DIP	N-8
SSM2143S	−40°C to +85°C	8-Pin SOIC	SO-8

*For outline information see Package Information section.

14

Serial Input Hex/Quad "Clickless" Volume Control with Master Attenuation

SSM2160/SSM2161

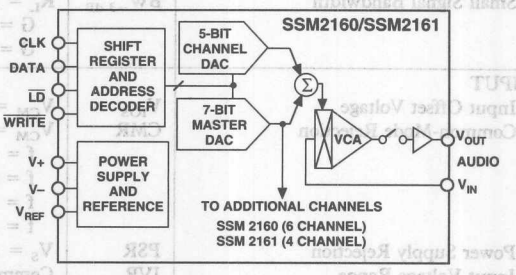
FEATURES

- Digitally-Controlled "Clickless" Level Adjustment
  - SSM2160: Six Channels
  - SSM2161: Four Channels
- Master Control Has 128 1 dB Steps
- Each Channel Has 32 1 dB Steps Plus Mute
- Step Sizes Can Be Changed Using External Resistors
- High Gain Accuracy
- 100 dB Gain Range
- Excellent Audio Characteristics:
  - –100 dBu SNR (0 dBu = 0.775 V rms, V_S = ±5 V)
  - +10 dBu Headroom (V_S = ±5 V)
  - 0.008% THD+N (@ 1 kHz, V_{IN} = –10 dBu, Unity Gain)
  - –80 dB Crosstalk (@ 1 kHz)
- Single or Dual Supply Operation
- 24-Pin Plastic DIP and SOIC Packages (SSM2160)
- 20-Pin Plastic DIP and SOIC Packages (SSM2161)

APPLICATIONS

- Dolby* Pro-Logic Master Volume Control
- Home THX† System
- DSP Soundfield Processors
- Automotive Audio Systems
- HDTV Audio Systems

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The SSM2160 and SSM2161 allow digital control of volume for six and four channels, respectively, with a master level control. In order to avoid "clicking," the device uses high performance voltage controlled amplifiers (VCAs) for the audio signal path. The VCA control port effectively isolates DAC charge injection from the audio path, which is the major contributor to clicking in resistor-ladder type attenuators. Each channel is controlled by a dedicated 5-bit DAC, providing 32 steps of adjustment, plus mute. In addition, a master 7-bit DAC feeds every control port, with 128 steps. Therefore, a balance can be achieved among all channels over a 32-step range, and the master control allows adjustment over its entire range while maintaining the desired channel-to-channel balance. Step sizes are defaulted to 1 dB, but channel sizes can be increased or master sizes decreased by the addition of external resistors. Approximately 80 dB of attenuation and up to 20 dB of gain is possible.

The SSM2160/SSM2161 can operate either single or dual supply, with a total supply voltage range of 8 V to 36 V. An on-chip voltage reference is provided for single-supply applications.

*Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.
†Home THX is a registered trademark of Lucasfilm, Ltd.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (V_S = ±5 V, A_V = 0 dB, 0 dBu = 0.775 V rms, V_{IN} = –10 dBu, f_{AUDIO} = 1 kHz, f_{CLK} = 250 kHz, R_L = 100 kΩ, –40°C < T_A < +85°C, unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Parameter	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE					
Noise	V_{IN} = GND, 20 kHz Bandwidth		–100	TBD	dBu
Headroom	Clip Point = 1% THD+N		+10		dBu
Total Harmonic Distortion Plus Noise	2nd and 3rd Harmonics Only				
	A_V = 0 dB		0.008	TBD	%
	A_V = –20 dB		0.02	TBD	%
	A_V = 0 dB, V_{IN} = +10 dBu		0.8	1.0	%
Channel Separation	Any Channel to Another		80		dB
ANALOG INPUT					
Input Offset Voltage			10		mV
Input Impedance			14		kΩ
GAIN CONTROL ELEMENTS					
Default Step Size—Master	A_VMASTER = 0 dB to –60 dB	TBD	1.0	TBD	dB
Default Step Size—Channel	A_VCHANNEL = 0 dB to +20 dB	TBD	1.0	TBD	dB
Gain Error	Relative to Same Channel				
	A_VMASTER = 0 dB			0.25	dB
	A_VMASTER = –20 dB			0.25	dB
	A_VMASTER = –40 dB			1	dB
	A_VMASTER = –60 dB			2	dB
Gain Match Error	Channel-to-Channel; Same Level Setting				
	A_VMASTER = 0 dB			0.25	dB
	A_VMASTER = –20 dB			0.25	dB
	A_VMASTER = –20 dB, A_VCH = +20 dB			0.25	dB
	A_VMASTER = –40 dB			1	dB
	A_VMASTER = –60 dB			2	dB
Mute Attenuation			–105		dB
ANALOG OUTPUT					
Output Impedance			TBD		Ω
Mute Output Impedance			TBD		Ω
Output Sink Current			TBD		mA
Minimum Resistive Load Drive			TBD		Ω
Maximum Capacitive Drive			TBD		pF
Offset Voltage	Channel Muted		20		mV
CONTROL SECTION					
Logic Input LO				0.8	V
Logic Input HI		2.0			V
Logic Input Current	Logic LO or HI		1		µA
Maximum Clock Frequency		1	2		MHz
Timing Characteristics	See Timing Diagram				
REFERENCE					
Output Voltage	V_S = +10 V (Single Supply)	4.9	5.0	5.1	V
Output Impedance			TBD		Ω
Load Regulation	–10 mA ≤ I_L ≤ +10 mA		0.1		%
POWER SUPPLIES					
Supply Voltage Range	Dual Supply	±4		±15	V
	Single Supply	+8		+30	V
Supply Current	Positive		TBD	TBD	mA
	Negative		20	30	mA
Power Supply Rejection Ratio	Dual Supply		TBD		dB

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Dual Supply ..... ±18 V
Single Supply ..... +36 V
Analog Input Voltage ..... $\pm V_S$
Logic Input Voltage ..... $\pm V_S$
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

THERMAL CHARACTERISTICS

Thermal Resistance[2]

24-Pin Plastic DIP (SSM2160)
θ_{JA} ..... TBD°C/W
θ_{JC} ..... TBD°C/W

24-Pin SOIC (SSM2160)
θ_{JA} ..... TBD°C/W
θ_{JC} ..... TBD°C/W

20-Pin Plastic DIP (SSM2161)
θ_{JA} ..... TBD°C/W
θ_{JC} ..... TBD°C/W

20-Pin SOIC (SSM2161)
θ_{JA} ..... TBD°C/W
θ_{JC} ..... TBD°C/W

TRANSISTOR COUNT

Number of Transistors ..... TBD

ESD RATINGS

883 (Human Body) Model ..... TBD kV
EIAJ Model ..... TBD V

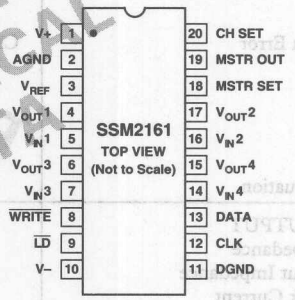
NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP and device soldered in circuit board for SOIC package.

SSM2161 PIN CONFIGURATION

20-Lead Plastic DIP and SOIC



PRELIMINARY TECHNICAL DATA

ORDERING GUIDE

Model	Temperature Range	Package Option*
SSM2160N	–40°C to +85°C	N-24
SSM2160R	–40°C to +85°C	R-24
SSM2161N	–40°C to +85°C	N-20
SSM2161R	–40°C to +85°C	R-20

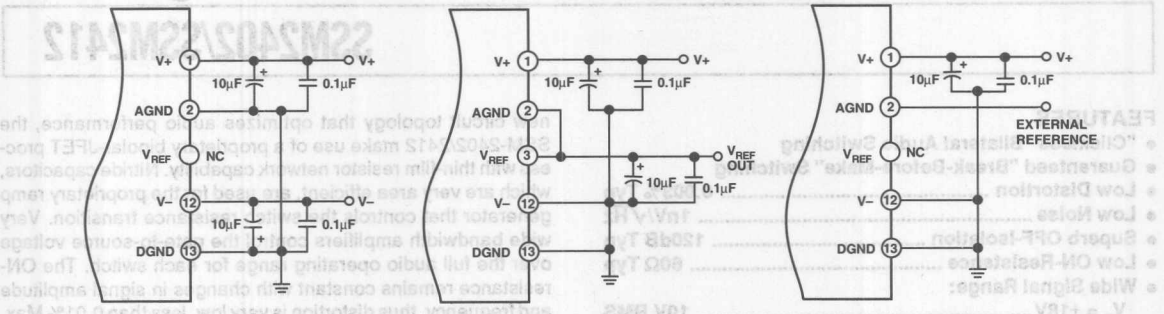
*N = Plastic DIP; R = SOIC. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2160/SSM2161 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

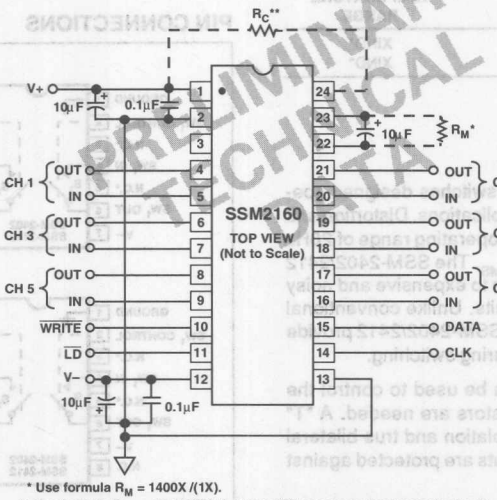
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SSM2160 POWER SUPPLY CONNECTIONS



Dual Supply *Single Supply* *Single Supply Using External Reference*

TYPICAL APPLICATION CIRCUIT (DUAL SUPPLY)



* Use formula R_M = 1400X /(1X).

** Use formula R_{CH} = 44-20X/(X-1), where "X" equals desired step size in dB.

PRELIMINARY TECHNICAL DATA

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This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Dual Audio Analog Switches

SSM2402/SSM2412

FEATURES

- "Clickless" Bilateral Audio Switching
- Guaranteed "Break-Before-Make" Switching
- Low Distortion ..... 0.003% Typ
- Low Noise ..... 1nV/√Hz
- Superb OFF-Isolation ..... 120dB Typ
- Low ON-Resistance ..... 60Ω Typ
- Wide Signal Range:
  V_S = ±18V ..... 10V RMS
- Wide Power Supply Range ..... ±20V Max
- Available in Dice Form

ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 14-PIN	SOL 16-PIN	
SSM2402P	SSM2402S	XIND*
SSM2412P	SSM2412S	XIND*

*XIND = –40°C to +85°C

GENERAL DESCRIPTION

The SSM-2402/2412 are dual analog switches designed specifically for high-performance audio applications. Distortion and noise are negligible over the full audio operating range of 20Hz to 20kHz at signal levels of up to $10V_{RMS}$. The SSM-2402/2412 offer a monolithic integrated alternative to expensive and noisy relays or complex discrete JFET circuits. Unlike conventional general-purpose CMOS switches, the SSM-2402/2412 provide superb fidelity without audio "clicks" during switching.

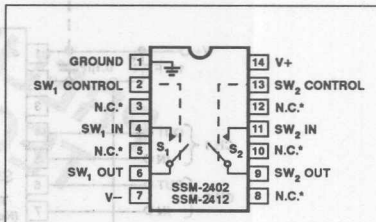
Conventional TTL or CMOS logic can be used to control the switch state. No external pull-up resistors are needed. A "T" configuration provides superb OFF-isolation and true bilateral operation. The analog inputs and outputs are protected against overload and overvoltage.

An important feature is the guaranteed "break-before-make" for all units, even IC-to-IC. In large systems with multiple switching channels, all separate switching units must open before any switch goes into the ON-state. With the SSM-2402/2412, you can be certain that multiple circuits will all break-before-make.

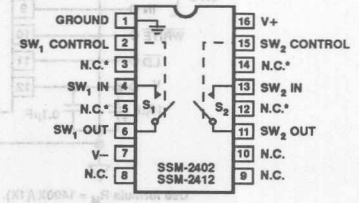
The SSM-2402/2412 represent a significant step forward in audio switching technology. Distortion and switching noise are significantly reduced in the new SSM-2402/2412 bipolar-JFET switches relative to CMOS switching technology. Based on a new circuit topology that optimizes audio performance, the SSM-2402/2412 make use of a proprietary bipolar-JFET process with thin-film resistor network capability. Nitride capacitors, which are very area efficient, are used for the proprietary ramp generator that controls the switch resistance transition. Very wide bandwidth amplifiers control the gate-to-source voltage over the full audio operating range for each switch. The ON-resistance remains constant with changes in signal amplitude and frequency, thus distortion is very low, less than 0.01% Max.

The SSM-2402 is the first analog switch truly optimized for high-performance audio applications. For broadcasting and other switching applications which require a faster switching time, we recommend the SSM-2412 – a dual analog switch with one-third of the switching time of the SSM-2402.

PIN CONNECTIONS



14-PIN PLASTIC DIP (P-Suffix)



16-PIN SOL (S-Suffix)

* GUARD PINS FOR INPUT/OUTPUT ISOLATION (GROUND FOR BEST PERFORMANCE)

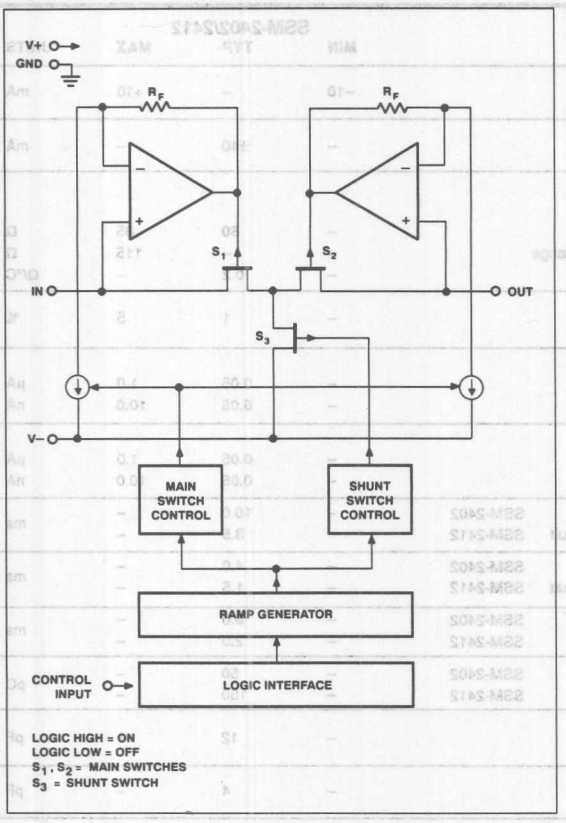
CONTROL LOGIC

Logic In	Switch State
0	OFF
1	ON

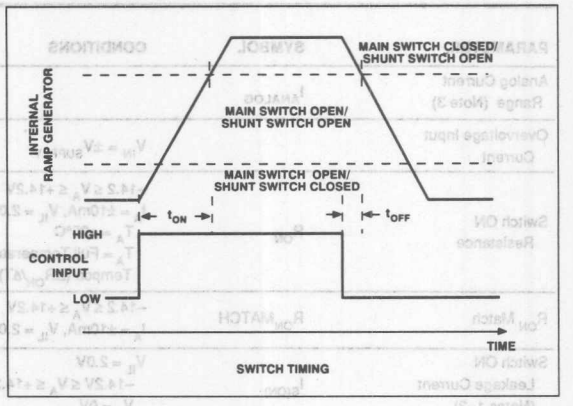
Logic "0" ≤ 0.8V
Logic "1" ≥ 2.0V

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

FUNCTIONAL DIAGRAM



TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range ..... –40°C to +85°C
Operating Supply Voltage Range ..... ±20V
Analog Input Voltage Range
Continuous ..... V– +3.5V ≤ V_A ≤ V+ –3.5V
Maximum Current Through Switch 20mA
Logic Input Voltage Range ..... V+ Supply to –2V
V+ Supply to Ground ..... +36V
V– Supply to Ground ..... –20V
V_A to V– Supply ..... +36V

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

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ELECTRICAL CHARACTERISTICS at V_S = ±18V, R_L = OPEN, and –40°C ≤ T_A ≤ +85°C, unless otherwise noted.
All specifications, tables, graphs, and application data apply to both the SSM-2402 and SSM-2412, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2402/2412 MIN	TYP	MAX	UNITS
Positive Supply Current	$+I_{SY}$	V_{IL} = 0.8V, 2.0V (Note 1)	–	6.0	7.5	mA
Negative Supply Current	$-I_{SY}$	V_{IL} = 0.8V, 2.0V (Note 1)	–	4.8	6.0	mA
Ground Current	I_{GND}	V_{IL} = 0.8V, 2.0V (Note 1)	–	0.6	1.5	mA
Digital Input High	V_{INH}	T_A = Full Temperature Range	2.0	–	–	V
Digital Input Low	V_{INL}	T_A = Full Temperature Range	–	–	0.8	V
Logic Input Current	I_{LOGIC}	V_{IN} = 0 to 15V (Note 2)	–	1.0	5.0	µA
Analog Voltage Range (Note 3)	V_{ANALOG}		–14.2	–	+14.2	V

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Current Range (Note 3)	I_{ANALOG}			–10	–	+10	mA
Overvoltage Input Current		$V_{IN} = \pm V_{SUPPLY}$		–	±40	–	mA
Switch ON Resistance	R_{ON}	$-14.2 \le V_A \le +14.2V$ $I_A = \pm 10mA$, $V_{IL} = 2.0V$ $T_A = +25°C$ T_A = Full Temperature Range Tempco ($\Delta R_{ON}/\Delta T$)		– – –	60 – 0.2	85 115 –	Ω Ω Ω/°C
R_{ON} Match	R_{ON}MATCH	$-14.2 \le V_A \le +14.2V$ $I_A = \pm 10mA$, $V_{IL} = 2.0V$		–	1	5	%
Switch ON Leakage Current (Notes 1, 2)	$I_{S(ON)}$	$V_{IL} = 2.0V$ $-14.2V \le V_A \le +14.2V$ $V_A = 0V$		– –	0.05 0.05	1.0 10.0	µA nA
Switch OFF Leakage Current (Notes 1, 2)	$I_{S(OFF)}$	$V_{IL} = 0.8V$ $-14.2V \le V_A \le +14.2V$ $V_A = 0V$		– –	0.05 0.05	1.0 10.0	µA nA
Turn-On Time (Note 4)	t_{ON}	$V_A = +10V$, $R_L = 2k\Omega$ $T_A = +25°C$, See Test Circuit	SSM-2402 SSM-2412	– –	10.0 3.5	– –	ms
Turn-Off Time (Note 5)	t_{OFF}	$V_A = +10V$, $R_L = 2k\Omega$ $T_A = +25°C$, See Test Circuit	SSM-2402 SSM-2412	– –	4.0 1.5	– –	ms
Break-Before-Make Time Delay (Note 6)	$t_{OFF} - t_{ON}$	$T_A = +25°C$	SSM-2402 SSM-2412	– –	6.0 2.0	– –	ms
Charge Injection	Q	$T_A = +25°C$	SSM-2402 SSM-2412	– –	50 150	– –	pC
ON-State Input Capacitance	$CS_{(ON)}$	$V_A = 1V_{RMS}$ f = 5kHz, $T_A = +25°C$		–	12	–	pF
OFF-State Input Capacitance	$CS_{(OFF)}$	$V_A = 1V_{RMS}$ f = 5kHz, $T_A = +25°C$		–	4	–	pF
OFF Isolation	$I_{SO(OFF)}$	$V_A = 10V_{RMS}$, 20Hz to 20kHz $T_A = +25°C$, See Test Circuit		–	120	–	dB
Channel-to-Channel Crosstalk	C_T	$V_A = 10V_{RMS}$, 20Hz to 20kHz $T_A = +25°C$		–	96	–	dB
Total Harmonic Distortion (Note 7)	THD	0 to $10V_{RMS}$, 20Hz to 20kHz $T_A = +25°C$, $R_L = 5k\Omega$		–	0.003	0.01	%
Spectral Noise Density	e_n	20Hz to 20kHz $T_A = +25°C$		–	1	–	$nV/\sqrt{Hz}$
Wideband Noise Density	$e_{n\,p\text{-}p}$	20Hz to 20kHz $T_A = +25°C$		–	0.2	–	$\mu V_{p\text{-}p}$

NOTES:

1. "V_{IL}" is the Logic Control Input.
2. Current tested at $V_{IN} = 0V$. This is the worst case condition.
3. Guaranteed by R_{ON} test condition.
4. Turn-ON Time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the final value.
5. Turn-OFF time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the initial value.
6. Switch is guaranteed by design to provide break-before-make operation.
7. THD guaranteed by design and dynamic R_{ON} testing.

ANALOG DEVICES

Quad Audio Switch

SSM2404

FEATURES

- "Clickless" Bilateral Audio Switching
- Four SPST Switches in a 20-Pin Package
- Ultralow THD+N: 0.0008% @ 1 kHz (2 V rms, R_L = 100 kΩ)
- Low Charge Injection: 35 pC typ
- High OFF Isolation: −100 dB typ (R_L = 10 kΩ @ 1 kHz)
- Low Crosstalk: −94 dB typ (R_L = 10 kΩ @ 1 kHz)
- Low ON Resistance: 28 Ω typ
- Low Supply Current: 900 µA typ
- Single or Dual Supply Operation: +11 V to +24 V or ±5.5 V to ±12 V
- Guaranteed Break-Before-Make
- TTL and CMOS Compatible Logic Inputs
- Low Cost-Per-Switch

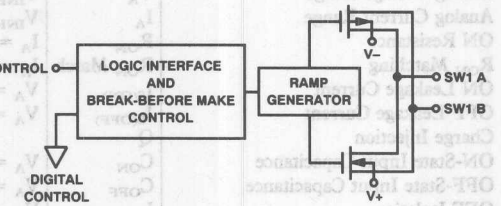
GENERAL DESCRIPTION

The SSM-2404 integrates four SPST analog switches in a single 20-pin package. Developed specifically for high performance audio applications, distortion and noise are negligible over the full operating range of 20 Hz to 20 kHz. With very low charge injection of 35 pC, "clickless" audio switching is possible, even under the most demanding conditions.

Switch control is realized by conventional TTL or CMOS logic. Guaranteed "break-before-make" operation assures that all switches in a large system will open before any switch reaches the ON state.

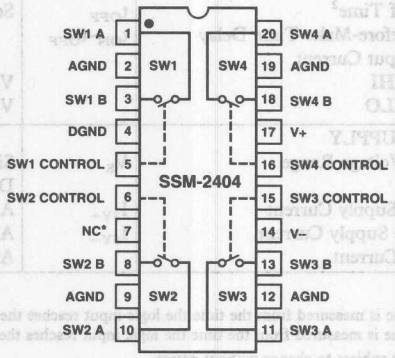
Single or dual supply operation is possible. Additional features include −100 dB OFF isolation, −94 dB crosstalk and 28 Ω ON resistance. Optional current-mode switching permits an extended signal-handling range. Although optimized for large load impedances, the SSM-2404 maintains good audio performance even under low load impedance conditions.

BLOCK DIAGRAM OF ONE SWITCH CHANNEL



PIN CONNECTIONS

Epoxy Mini-DIP (P-Suffix) and SOIC (S-Suffix)



NC = NO CONNECT

*CONNECT TO ANALOG GROUND FOR BEST NOISE ISOLATION

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SSM2404—SPECIFICATIONS

(V_S = ±12 V, T_A = +25°C, unless otherwise specified. Typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD+N	@ 1 kHz, with 80 kHz Filter, R_L = 100 kΩ, V_{IN} = 2 V rms		0.0008		%
Spectral Noise Density	e_n	20 Hz to 20 kHz		0.8		nV/√Hz
Wideband Noise Density	e_n p–p	20 Hz to 20 kHz		0.6		μV p–p
ANALOG SIGNAL SECTION						
Analog Voltage Range	V_A	V_{INH} = 2.4 V, I_A = ±2 mA		±12		V
Analog Current Range	I_A	V_{INH} = 2.4 V, V_A = 0 V		±10		mA
ON Resistance	R_{ON}	I_A = ±10 mA, V_A = ±10 V dc		28	45	Ω
R_{ON} Matching	R_{ON} Match	I_A = ±10 mA, V_A = 0 V		1		%
ON Leakage Current	$I_{S(ON)}$	V_A = ±10 V	−20	0.1	+20	nA
OFF Leakage Current	$I_{S(OFF)}$	V_A = ±10 V	−20	0.1	+20	nA
Charge Injection	Q			35		pC
ON-State Input Capacitance	C_{ON}	V_A = 5 V rms		31		pF
OFF-State Input Capacitance	C_{OFF}	V_A = 5 V rms		17		pF
OFF Isolation	$I_{SO(OFF)}$	V_A = 50 mV rms, f = 1 kHz, R_L = 10 kΩ		−100		dB
Channel-to-Channel Crosstalk	C_T	V_A = 50 mV rms, f = 1 kHz, R_L = 10 kΩ		−94		dB
CONTROL SECTION						
Digital Input High	V_{INH}	DGND = 0 V	2.4		V_S	V
Digital Input Low	V_{INL}	DGND = 0 V	0		0.8	V
Turn-On Time[1]	t_{ON}	See Test Circuit		8	50	ms
Turn-Off Time[2]	t_{OFF}	See Test Circuit		5	30	ms
Break-Before-Make Time Delay	t_{ON}–t_{OFF}			3	20	ms
Logic Input Current						
Logic HI		V_{INH} = 2.4 V	−1000	1.3	+1000	nA
Logic LO		V_{INL} = 0.8 V	−1000	1.0	+1000	nA
POWER SUPPLY						
Supply Voltage Range	V_S	Single Supply	+11		+24	V
		Dual Supply	±5.5		±12	V
Positive Supply Current	I_{SY+}	All Channels On		0.9	5	mA
Negative Supply Current	I_{SY-}	All Channels On	−1.5	−0.6		mA
Ground Current		All Channels On	−2.0	−0.3		mA

NOTES

[1]Turn-on time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the final value.

[2]Turn-off time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the initial value.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- Single Supply . . . . . +27 V
- Dual Supply . . . . . ±13.5 V

Analog Input Voltage (V_A) . . . . . V_S

Logic Input Voltage ($V_{INL/INH}$) . . . . . V_S

Maximum Current Through Any Switch . . . . . 20 mA

Operating Temperature Range . . . . . −40°C to +85°C

Storage Temperature Range . . . . . −65°C to +150°C

Junction Temperature (T_J) . . . . . +150°C

Lead Temperature (Soldering, 60 sec) . . . . . +300°C

Thermal Resistance[1]
- 20-Pin Plastic DIP (P): θ_{JA} = 74, θ_{JC} = 32 . . . . . °C/W
- 20-Pin SOIC (S): θ_{JA} = 90, θ_{JC} = 27 . . . . . °C/W

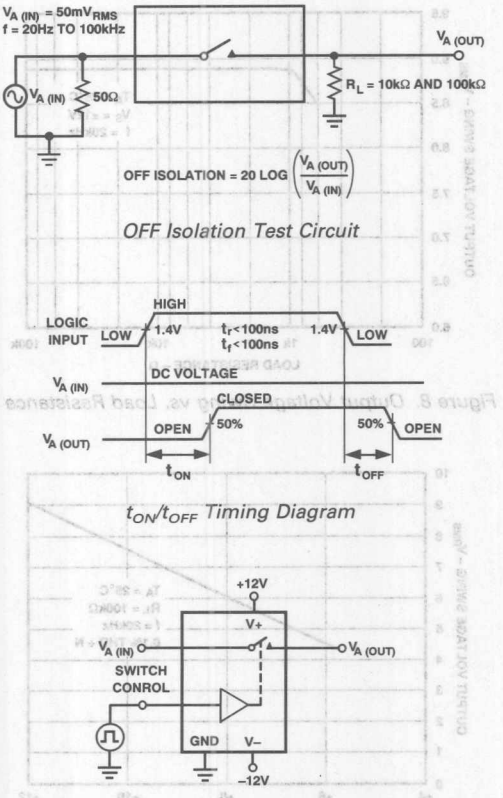
NOTE

[1]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package.

ORDERING GUIDE

Model	Operating Temperature Range	Package	Package Option*
SSM2404P	−40°C to +85°C	20-Pin Plastic DIP	N-20
SSM2404S	−40°C to +85°C	20-Pin SOIC	R-20

*N = Plastic DIP, R = SOIC. For outline information see Package Information section.



Test Circuit for t_{ON}/t_{OFF} Timing Specification, t_{ON}/t_{OFF} Switching Response, and ON/OFF Transition Photos

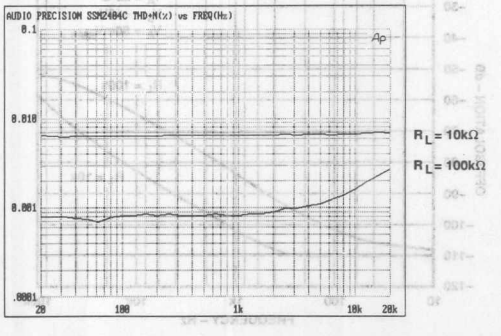


Figure 1. THD+N vs. Frequency (V_S = ±12 V, V_A = 2 V rms, with 80 kHz Filter)

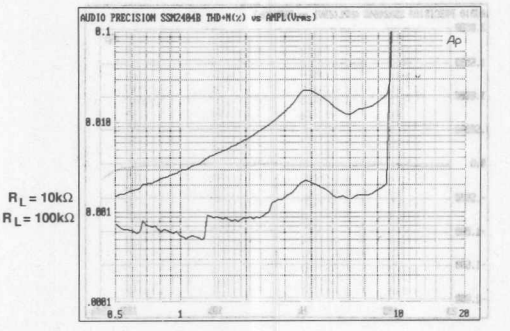


Figure 2. Headroom (V_S = ±12 V, f = 1kHz, with 80 kHz Filter)

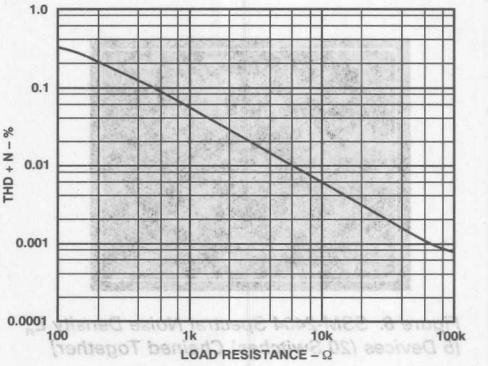


Figure 3. THD+N vs. Load (V_S =±12 V, V_A = 2 V rms, f = 1 kHz, with 80 kHz Filter)

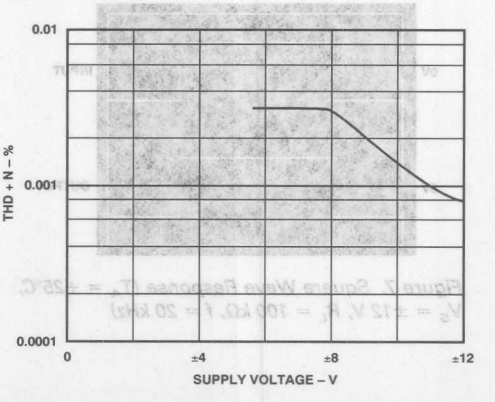


Figure 4. THD+N vs. Supply Voltage (V_A = 2 V rms, f = 1 kHz, R_L = 100 kΩ, with 80 kHz Filter)

14

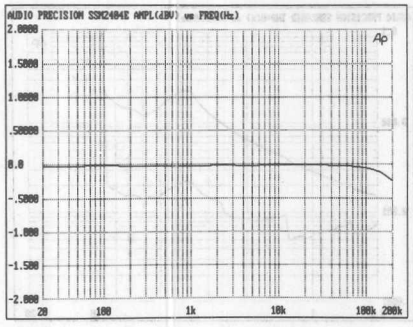


Figure 5. Frequency Response (V_S = ±12 V, V_A = 1 V rms, R_L = 100 kΩ)

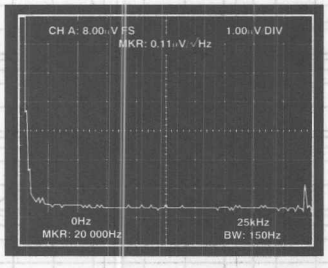


Figure 6. SSM-2404 Spectral Noise Density E_n [5 Devices (20 Switches) Chained Together]

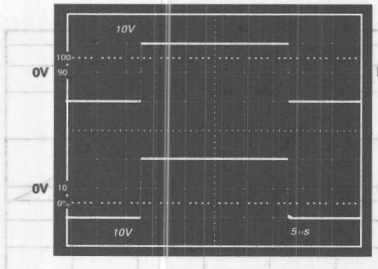


Figure 7. Square Wave Response (T_A = +25°C, V_S = ±12 V, R_L = 100 kΩ, f = 20 kHz)

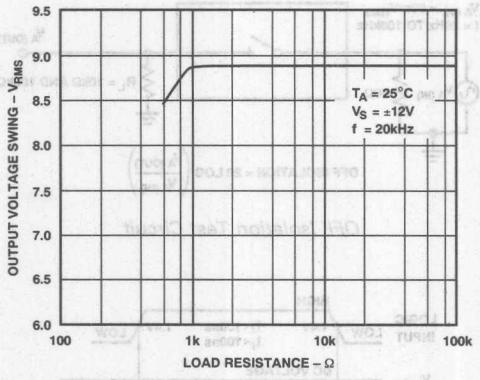


Figure 8. Output Voltage Swing vs. Load Resistance

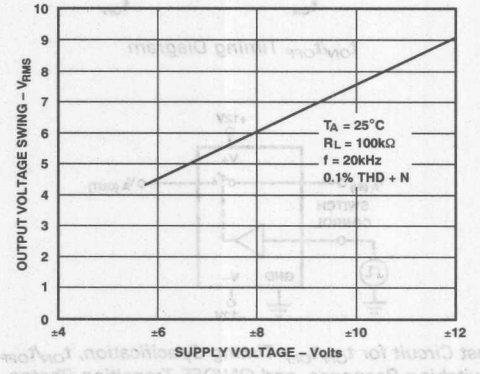


Figure 9. Output Voltage Swing vs. Supply Voltage

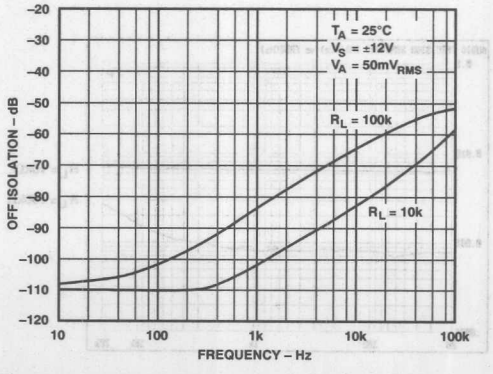


Figure 10. OFF-Isolation vs. Frequency

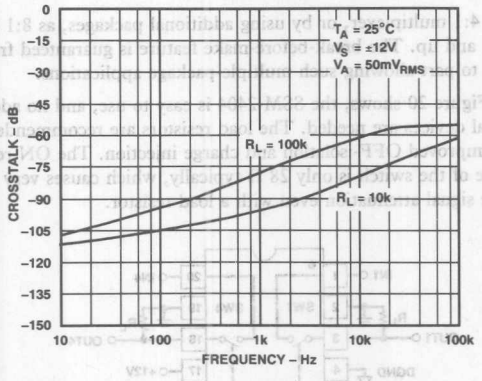


Figure 11. Channel-to-Channel Crosstalk vs. Frequency (Worst-Case Conditions, as Measured Between Switches 1 and 4, or 2 and 3)

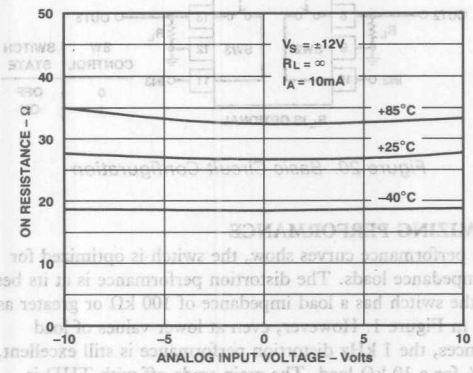


Figure 12. ON Resistance vs. Analog Voltage

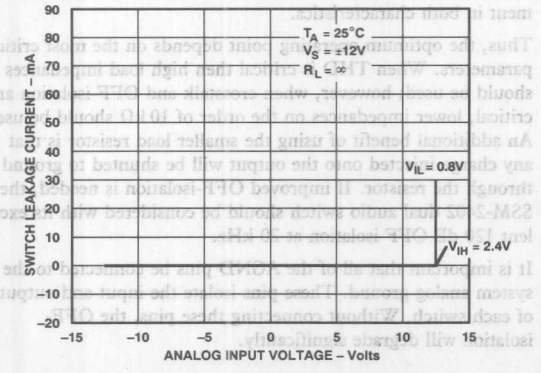


Figure 13. Overvoltage Characteristics

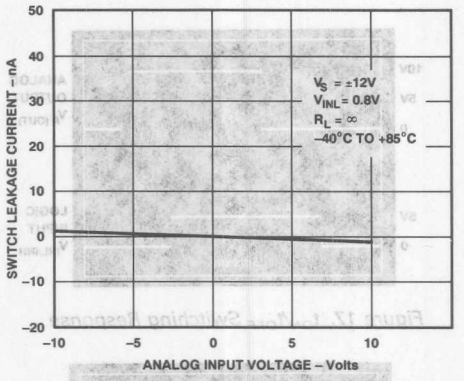


Figure 14. Leakage Current vs. Analog Voltage

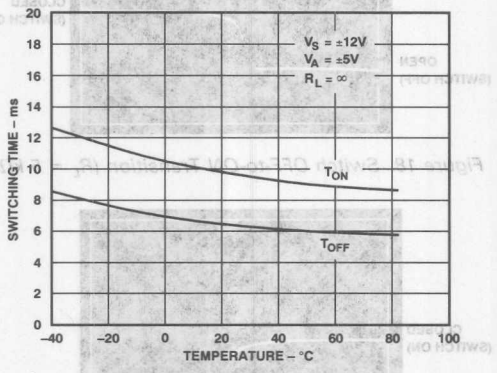


Figure 15. Switching Time vs. Temperature

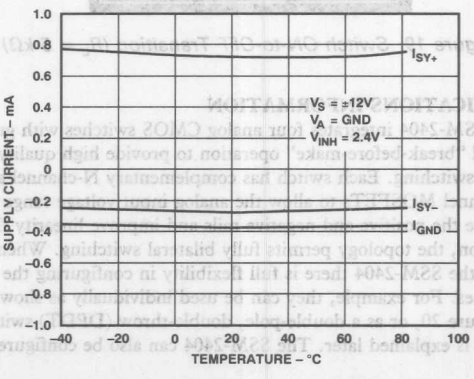


Figure 16. Supply Current vs. Temperature

14

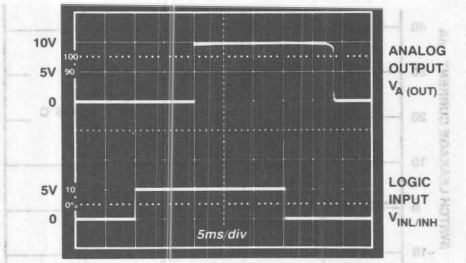


Figure 17. t_{ON}/t_{OFF} Switching Response

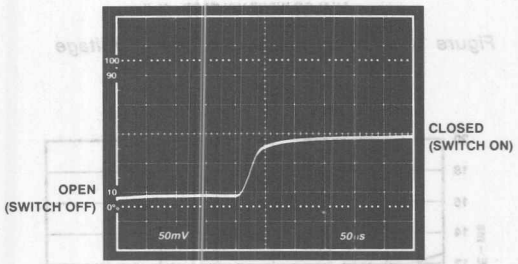


Figure 18. Switch OFF-to-ON Transition (R_L = 5 kΩ)

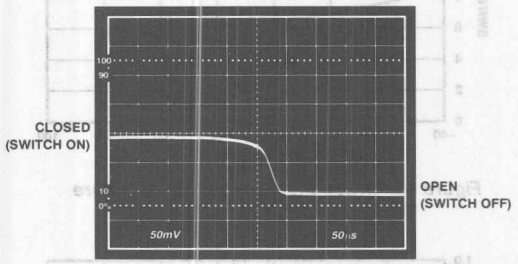


Figure 19. Switch ON-to-OFF Transition (R_L = 5 kΩ)

APPLICATIONS INFORMATION

The SSM-2404 integrates four analog CMOS switches with guaranteed "break-before-make" operation to provide high quality audio switching. Each switch has complementary N-channel and P-channel MOSFETs to allow the analog input voltage range to include the positive and negative rails and improve linearity. In addition, the topology permits fully bilateral switching. When using the SSM-2404 there is full flexibility in configuring the switches. For example, they can be used individually as shown in Figure 20, or as a double-pole, double-throw (DPDT) switch, which is explained later. The SSM-2404 can also be configured 16:1 and up. The break-before-make feature is guaranteed from part to part allowing such multiple-package applications.

As Figure 20 shows, the SSM-2404 is easy to use, and no additional devices are needed. The load resistors are recommended for improved OFF-isolation and charge injection. The ON resistance of the switch is only 28 Ω typically, which causes very little signal attenuation even with a load resistor.

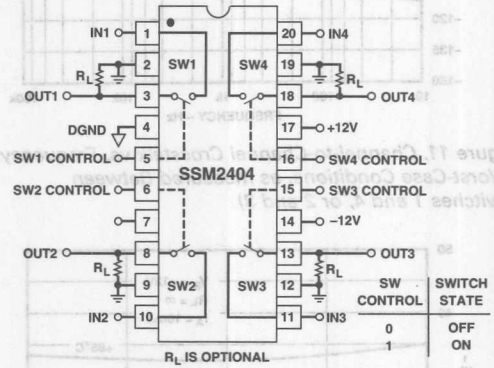


Figure 20. Basic Circuit Configuration

OPTIMIZING PERFORMANCE

As the performance curves show, the switch is optimized for high impedance loads. The distortion performance is at its best when the switch has a load impedance of 100 kΩ or greater as shown in Figure 1. However, even at lower values of load resistances, the 1 kHz distortion performance is still excellent, 0.006% for a 10 kΩ load. The main trade-off with THD is OFF-isolation and crosstalk. This is shown in Figures 10 and 11, again with two different load conditions. As these graphs show, the 10 kΩ load yields approximately a 16 dB improvement in both characteristics.

Thus, the optimum operating point depends on the most critical parameters. When THD is critical then high load impedances should be used; however, when crosstalk and OFF-isolation are critical, lower impedances on the order of 10 kΩ should be used. An additional benefit of using the smaller load resistor is that any charge injected onto the output will be shunted to ground through the resistor. If improved OFF-isolation is needed, the SSM-2402 dual audio switch should be considered with its excellent 120 dB OFF-isolation at 20 kHz.

It is important that all of the AGND pins be connected to the system analog ground. These pins isolate the input and output of each switch. Without connecting these pins, the OFF-isolation will degrade significantly.

DETAILED SWITCH OPERATION

A simplified circuit schematic with the functional sections is shown in Figure 21. The TTL interface has an internally regulated 5 V to ensure TTL logic levels regardless of the supply voltage. The logic threshold is with respect to the DGND pin, which can be offset. For example, if DGND is connected to the negative supply, then the SSM-2404 will operate with negative rail logic. The interface shifts the control logic down to the negative supply and inverts it to drive N1.

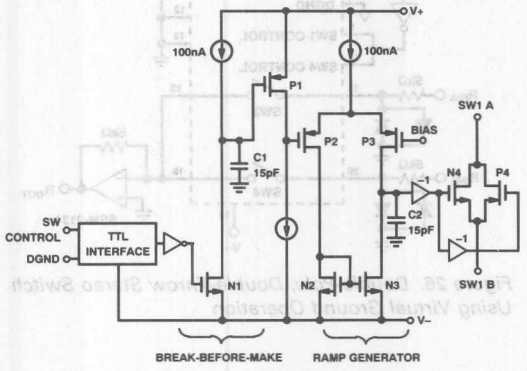


Figure 21. Simplified Schematic

N1 in combination with C1 and the 100 nA current source provides the break-before-make operation of the switch. When the switch is on, N1 is off and C1 is charged up to the positive rail. However, when the SW CONTROL is turned off, then the gate of N1 is pulled high. This turns N1 on, providing a low impedance path to quickly discharge C1 to the negative rail, which quickly "breaks" the switch. On the other hand, when the SW CONTROL goes high again, the gate of N1 is pulled low, turning it off. This leaves C1 to be slowly charged up to the positive rail by the 100 nA current source. The difference in the discharge and charging times ensures break-before-make operation, even from device to device.

The voltage on C1 is inverted by P1 to drive the ramp generator differential pair, consisting of P2, P3 and N2, N3. This differential pair steers the 100 nA of tail current to either charge or discharge C2. As discussed above, when the switch is on, C1 is charged up to the positive rail. P1 inverts this, putting a low voltage equivalent to the negative supply on the gate of P2. The BIAS voltage is approximately equal to the midpoint of the two supply voltages. Thus, when P2 is pulled down, it is turned on and P3 is off. All of the 100 nA flows through N2 and is mirrored by N3. Thus, the 100 nA discharges C2 through N3. When C2 is pulled low, the inverter turns N4 on by pulling its gate high, and the second inverter turns P4 on. To turn the switch off the gate of P2 is pulled above the BIAS so that all 100 nA charges C2 through P3. This is then inverted to turn off N4 and P4.

The internal ramp has rise and fall times on the order of a few milliseconds which is sped-up by the inverters. As the gate voltages of N4 and P4 are changing, the ON resistance of each switch is ramping from its OFF state to 28 Ω and vice versa. The actual rise and fall times are shown in Figures 18 and 19 for a 5 kΩ load. These times are significantly slower than typical switches, minimizing the SSM-2404's charge injection and giving it "clickless" performance.

DOUBLE-POLE DOUBLE-THROW SWITCH

The SSM-2404 is ideal as a one-chip solution for a stereo switch. The schematic in Figure 22 shows the typical configuration. This circuit will select one of two stereo sources, channel A or B. The switch controls for the left and right input of each channel are tied together so that both will be turned on or off simultaneously. An inverter is inserted between the channel A and B controls so that only one logic signal is needed. The outputs can be configured many different ways, such as an inverting or noninverting amplifier stage, and the 10 kΩ load resistors are added to improve the OFF-isolation. The performance of this stereo switch is equivalent to each individual switch, yielding a high quality audio switch that is virtually transparent to the signal.

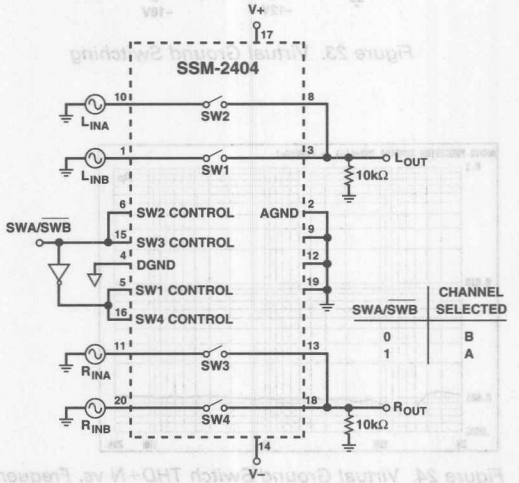


Figure 22. Double-Pole, Double-Throw Stereo Switch

VIRTUAL GROUND SWITCHING

The SSM-2404 was built on a CMOS process with a 24 V operating limit for the total supply voltage across the part. This leads to a corresponding limit on the analog voltage range. However, to achieve larger signal swings, the SSM-2404 should be configured in the virtual ground mode. As shown in Figure 23, the output of the SSM-2404 is connected to the inverting input of an amplifier. Since the noninverting input is grounded, the SSM-2404 will also be biased at ground, and large voltage swings on the circuit's input will not significantly change the voltage on the switch. The only limitation is that the current through the switch needs to be less than ±10 mA, and the voltage range is limited only by the op amp and its supply voltages.

The circuit was tested with an SSM-2131 high slew rate audio amplifier and the results are shown in Figures 24 and 25. This configuration yields excellent THD performance that is primarily determined by the amplifier. Also, the headroom is now +24 dBu (0 dBu = 0.775 V rms), which is due to the amplifier's output voltage swing. Thus, even though the SSM-2404 has a ±12 V limitation on its supplies, it can be used in systems with much higher voltage ranges. For example, the double-pole double-throw switch from Figure 22 can be reconfigured in the virtual ground mode to allow higher voltage swings, as shown in Figure 26. This application realizes the excellent performance of Figures 24 and 25 while providing a low cost switching solution.

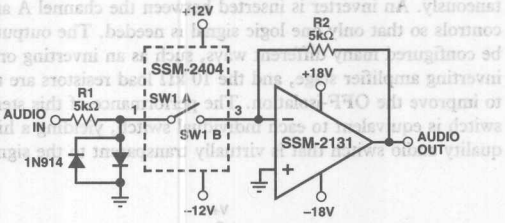


Figure 23. Virtual Ground Switching

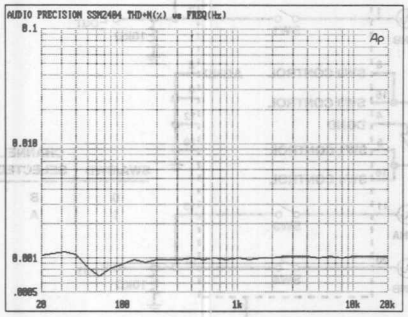


Figure 24. Virtual Ground Switch THD+N vs. Frequency (V_S = ±12 V, V_A = 2 V rms, with 80 kHz Filter)

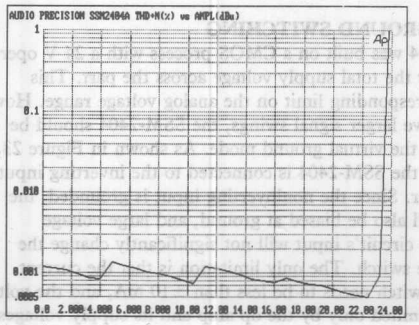


Figure 25. Virtual Ground Switch Headroom (V_S = ±12 V for SSM-2404; V_S = ±18 V for Op Amp, f = 1 kHz, with 80 kHz Filter)

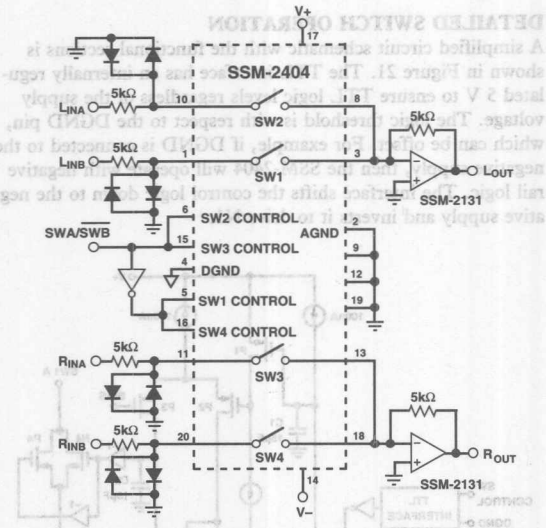


Figure 26. Double-Pole, Double-Throw Stereo Switch Using Virtual Ground Operation

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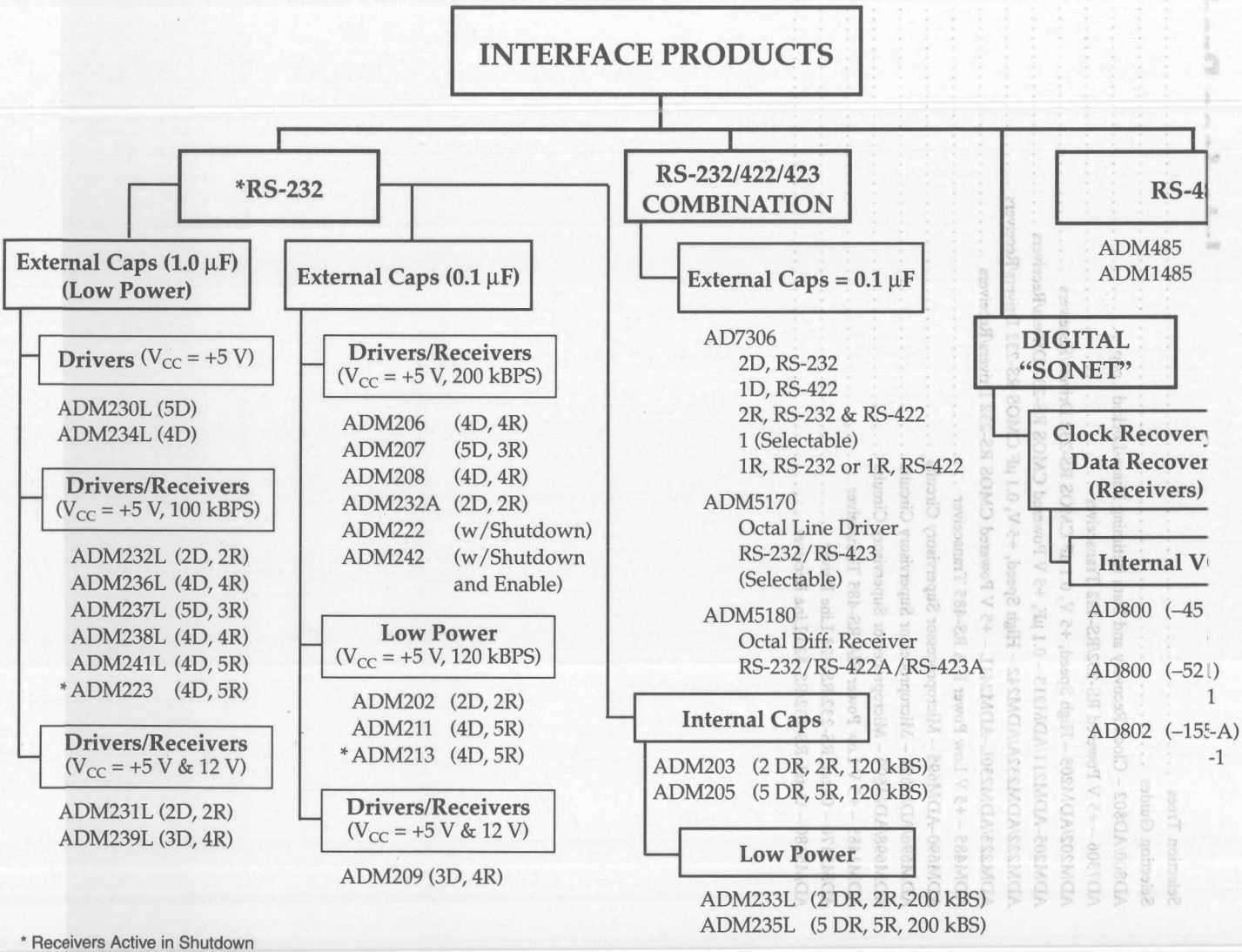
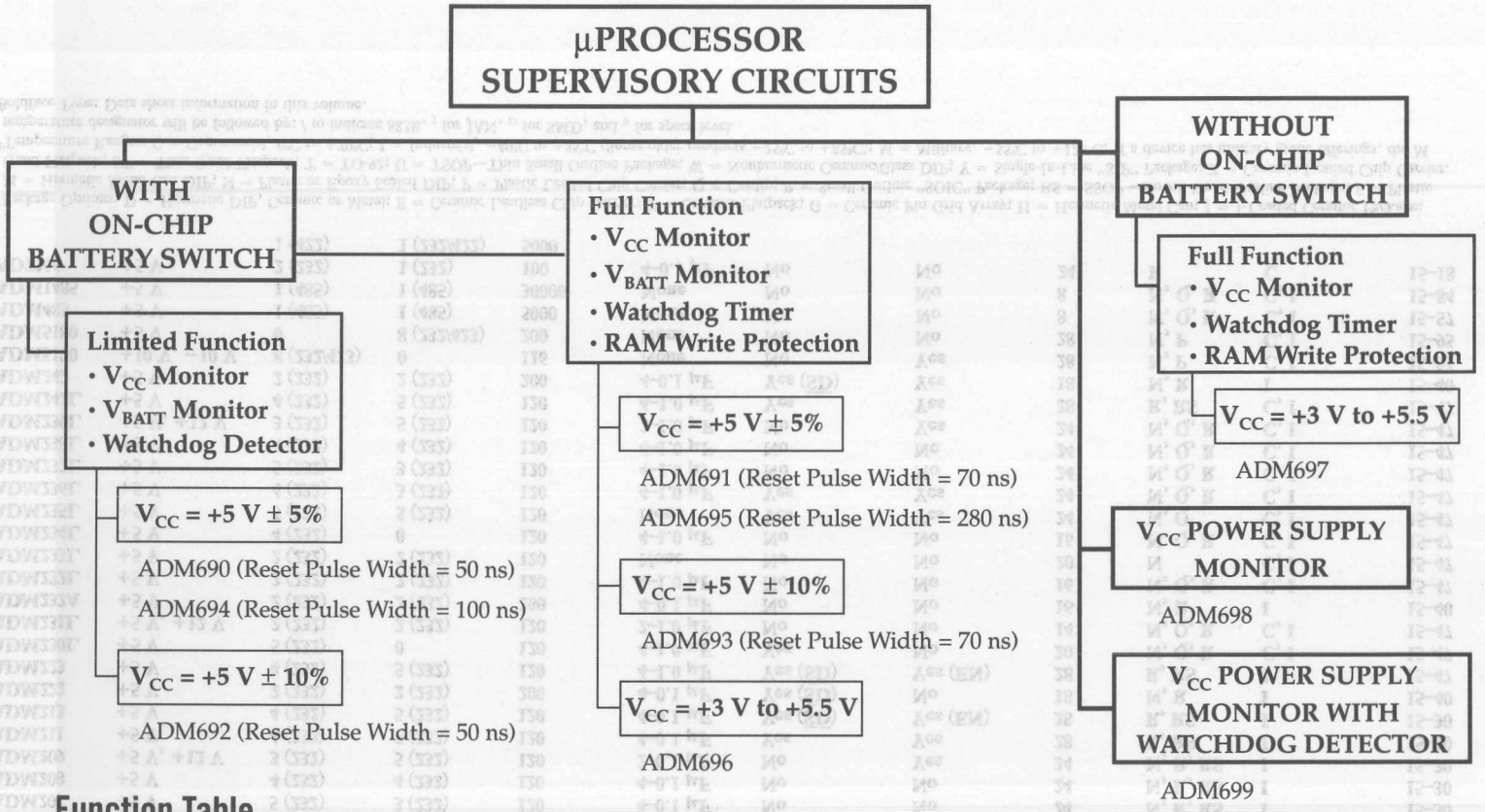
Selection Trees — Interface Products



* Receivers Active in Shutdown



Function Table

ADM690–ADM699 Functions	ADM690	ADM691	ADM692	ADM693	ADM694	ADM695	ADM696	ADM697	ADM698	ADM699
Fixed Power Up/Down Reset	✓	✓	✓	✓	✓	✓			✓	✓
Variable Power Up/Down Reset							✓	✓		
Battery Backup Switching	✓	✓	✓	✓	✓	✓	✓			
Watchdog Timer	✓	✓	✓	✓	✓	✓	✓	✓		✓
Power Failing Warning	✓	✓	✓	✓	✓	✓	✓	✓		
Write Protect		✓		✓		✓		✓		

Selection Guides—Interface Products

Line Drivers/Receivers

Model	Power Supply	No. of Drivers	No. of Receivers	Data Rate kB/S	External Capacitors	Low Power Shutdown SD	TTL Three-State $\overline{EN}$	No. of Pins	Package Options[1]	Temperature Ranges[2]	Page
ADM202	+5 V	2 (232)	2 (232)	120	4–0.1 μF	No	No	16	N, R	C	15–26
ADM203	+5 V	2 (232)	2 (232)	120	None	No	No	20	N	C	15–26
ADM205	+5 V	5 (232)	5 (232)	120	None	Yes	Yes	24	N	I	15–30
ADM206	+5 V	4 (232)	3 (232)	120	4–0.1 μF	Yes	Yes	24	N, R, RS	I	15–30
ADM207	+5 V	5 (232)	3 (232)	120	4–0.1 μF	No	No	24	N, R, RS	I	15–30
ADM208	+5 V	4 (232)	4 (232)	120	4–0.1 μF	No	No	24	N, R, RS	I	15–30
ADM209	+5 V, +12 V	3 (232)	5 (232)	120	2–0.1 μF	No	Yes	24	N, R, RS	I	15–30
ADM211	+5 V	4 (232)	5 (232)	120	4–0.1 μF	Yes	Yes	28	R, RS	I	15–30
ADM213	+5 V	4 (232)	5 (232)	120	4–0.1 μF	Yes ($\overline{SD}$)	Yes (EN)	28	R, RS	I	15–30
ADM222	+5 V	2 (232)	2 (232)	200	4–0.1 μF	Yes ($\overline{SD}$)	No	18	N, R	I	15–40
ADM223	+5 V	4 (232)	5 (232)	120	4–1.0 μF	Yes ($\overline{SD}$)	Yes (EN)	28	R, RS	I	15–47
ADM230L	+5 V	5 (232)	0	120	4–1.0 μF	Yes	No	20	N, Q, R	C, I	15–47
ADM231L	+5 V, +12 V	2 (232)	2 (232)	120	2–1.0 μF	No	No	14	N, Q, R	C, I	15–47
ADM232A	+5 V	2 (232)	2 (232)	200	4–0.1 μF	No	No	16	N, R	I	15–40
ADM232L	+5 V	2 (232)	2 (232)	120	4–1.0 μF	No	No	16	N, Q, R	C, I	15–47
ADM233L	+5 V	2 (232)	2 (232)	120	None	No	No	20	N	C, I	15–47
ADM234L	+5 V	4 (232)	0	120	4–1.0 μF	No	No	16	N, Q, R	C, I	15–47
ADM235L	+5 V	5 (232)	5 (232)	120	None	Yes	Yes	24	N, Q	C, I	15–47
ADM236L	+5 V	4 (232)	3 (232)	120	4–1.0 μF	Yes	Yes	24	N, Q, R	C, I	15–47
ADM237L	+5 V	5 (232)	3 (232)	120	4–1.0 μF	No	No	24	N, Q, R	C, I	15–47
ADM238L	+5 V	4 (232)	4 (232)	120	4–1.0 μF	No	No	24	N, Q, R	C, I	15–47
ADM239L	+5 V, +12 V	3 (232)	5 (232)	120	2–1.0 μF	No	Yes	24	N, Q, R	C, I	15–47
ADM241L	+5 V	4 (232)	5 (232)	120	4–1.0 μF	Yes	Yes	28	R, RS	C, I	15–47
ADM242	+5 V	2 (232)	2 (232)	200	4–0.1 μF	Yes ($\overline{SD}$)	Yes	18	N, R	I	15–40
ADM5170	+10 V, −10 V	8 (232/423)	0	116	None	No	Yes	28	N, P	C, I	15–91
ADM5180	+5 V	0	8 (232/423)	200	None	No	No	28	N, P	C, I	15–95
ADM485	+5 V	1 (485)	1 (485)	5000	None	No	No	8	N, Q, R	C, I	15–57
ADM1485	+5 V	1 (485)	1 (485)	30000	None	No	No	8	N, Q, R	C, I	15–84
AD7306	+5 V	2 (232)	1 (232)	100	4–0.1 μF	No	No	24	R	C	15–18
		1 (422)	1 (232/422)	5000							

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_{J}$ for JAN, $_{D}$ for SMD, and $_{S}$ for space level.
Boldface Type: Data sheet information in this volume.

Clock Recovery Circuits

Model	Description	Frequency	Package Options[1]	Temp Ranges[2]	Page	Comments
AD800-45	**Clock Recovery and Data Retiming Phase Locked Loop**	**44.736 MHz DS-3**	**Q**	**I**	**15–7**	**5 V Supply, 10K ECL Compatible**
AD800-52	**Clock Recovery and Data Retiming Phase Locked Loop**	**51.84 MHz STS-1**	**R**	**I**	**15–7**	**5 V Supply, 10K ECL Compatible**
AD800-155	**Clock Recovery and Data Retiming Phase Locked Loop**	**155.52 MHz STS-3 or STM-1**	**R**	**C**	**15–7**	**5 V Supply, 10K ECL Compatible**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_{J}$ for JAN, $_{D}$ for SMD, and $_{S}$ for space level.
Boldface Type: Data sheet information in this volume.

Clock Recovery and Data Retiming Phase-Locked Loop

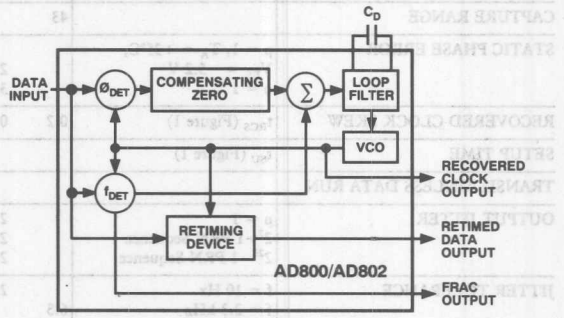
AD800/AD802*

FEATURES

Standard Products
- **44.736 Mbps—DS-3**
- **51.84 Mbps—STS-1**
- **155.52 Mbps—STS-3 or STM-1**

Accepts NRZ Data, No Preamble Required
Recovered Clock and Retimed Data Outputs
Phase-Locked Loop Type Clock Recovery—No Crystal Required
Random Jitter: 20° Peak-to-Peak
Pattern Jitter: Virtually Eliminated
10KH ECL Compatible
Single Supply Operation: −5.2 V or +5 V
Wide Operating Temperature Range: −40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD800 and AD802 employ a second order phase-locked loop architecture to perform clock recovery and data retiming on Non-Return to Zero, NRZ, data. This architecture is capable of supporting data rates between 20 Mbps and 160 Mbps. The products described here have been defined to work with standard telecommunications bit rates. 45 Mbps DS-3 and 52 Mbps STS-1 are supported by the AD800-45 and AD800-52 respectively. 155 Mbps STS-3 or STM-1 are supported by the AD802-155.

Unlike other PLL-based clock recovery circuits, these devices do not require a preamble or an external VCXO to lock onto input data. The circuit acquires frequency and phase lock using two control loops. The frequency acquisition control loop initially acquires the clock frequency of the input data. The phase-lock loop then acquires the phase of the input data, and ensures that the phase of the output signals track changes in the phase of the input data. The loop damping of the circuit is dependent on the value of a user selected capacitor; this defines jitter peaking performance and impacts acquisition time. The devices exhibit 0.08 dB jitter peaking, and acquire lock on random or scrambled data within 4×10^5 bit periods when using a damping factor of 5.

During the process of acquisition the frequency detector provides a Frequency Acquisition (FRAC) signal which indicates that the device has not yet locked onto the input data. This signal is a series of pulses which occur at the points of cycle slip between the input data and the synthesized clock signal. Once the circuit has acquired frequency lock no pulses occur at the FRAC output.

The inclusion of a precisely trimmed VCO in the device eliminates the need for external components for setting center frequency, and the need for trimming of those components. The VCO provides a clock output within ±20% of the device center frequency in the absence of input data.

The AD800 and AD802 exhibit virtually no pattern jitter, due to the performance of the patented phase detector. Total loop jitter is 20° peak-to-peak. Jitter bandwidth is dictated by mask programmable fractional loop bandwidth. The AD800, used for data rates < 90 Mbps, has been designed with a nominal loop bandwidth of 0.1% of the center frequency. The AD802, used for data rates in excess of 90 Mbps, has a loop bandwidth of 0.08% of center frequency.

All of the devices operate with a single +5 V or −5.2 V supply.

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***Protected by U.S. Patent No. 5,027,085.**

AD800/AD802—SPECIFICATIONS (V_{EE} = V_{MIN} to V_{MAX}, V_{CC} = GND, T_A = T_{MIN} to T_{MAX}, Loop Damping Factor = 5, unless otherwise noted)

Parameter[1]	Condition	AD800-45BQ Min	AD800-45BQ Typ	AD800-45BQ Max	AD800-52BR Min	AD800-52BR Typ	AD800-52BR Max	AD802-155KR/BR Min	AD802-155KR/BR Typ	AD802-155KR/BR Max	Units
NOMINAL CENTER FREQUENCY			44.736			51.84			155.52		MHz
OPERATING TEMPERATURE RANGE (T_{MIN} to T_{MAX})	K Grade							0		70	°C
	B Grade	−40		85	−40		85	−40		85	°C
TRACKING RANGE		43		45.5	49		53	155		156	Mbps
CAPTURE RANGE		43		45.5	49		53	155		156	Mbps
STATIC PHASE ERROR	ρ = 1, T_A = +25°C, V_{EE} = −5.2 V		2	10		2	10		14	30	Degrees
	ρ = 1		3	11.5		3	11.5		18	37	Degrees
RECOVERED CLOCK SKEW	t_{RCS} (Figure 1)	0.2	0.6	1	0.2	0.6	1	0.2	0.8	1	ns
SETUP TIME	t_{SU} (Figure 1)							2.06	2.37		ns
TRANSITIONLESS DATA RUN				240			240			240	Bit Periods
OUTPUT JITTER	ρ = 1		2			2			3.5		Degrees rms
	2^7−1 PRN Sequence		2.5	4.7		2.5	4.7		5.4	9.7	Degrees rms
	2^{23}−1 PRN Sequence		2.5	4.7		2.5	4.7		5.4	9.7	Degrees rms
JITTER TOLERANCE	f = 10 Hz		2,500			2,500			3,000		Unit Intervals
	f = 2.3 kHz	6.5									Unit Intervals
	f = 30 kHz	0.47									Unit Intervals
	f = 1 MHz	0.47									Unit Intervals
	f = 30 Hz				830						Unit Intervals
	f = 300 Hz				83						Unit Intervals
	f = 2 kHz				7.4						Unit Intervals
	f = 20 kHz				0.47						Unit Intervals
	f = 6.5 kHz							2.0	7.6		Unit Intervals
	f = 65 kHz							0.26	0.9		Unit Intervals
JITTER TRANSFER											
Damping Factor Capacitor, C_D											
ζ = 1, Nominal			8.2			6.8			2.2		nF
ζ = 5, Nominal			0.22			0.15			0.047		μF
ζ = 10, Nominal			0.82			0.68			0.22		μF
Peaking											
ζ = 1, Nominal	T_A = +25°C, V_{EE} = −5.2 V		2			2			2		dB
ζ = 5, Nominal	T_A = +25°C, V_{EE} = −5.2 V		0.08			0.08			0.08		dB
ζ = 10, Nominal	T_A = +25°C, V_{EE} = −5.2 V		0.02			0.02			0.02		dB
Bandwidth			45			52			130		kHz
ACQUISITION TIME											
ρ = 1/2	ζ = 1		1×10^4			1×10^4			1.5×10^4		Bit Periods
T_A = +25°C	ζ = 5		3×10^5	8×10^5		3×10^5	8×10^5		4×10^5	8×10^5	Bit Periods
V_{EE} = −5.2 V	ζ = 10		8×10^5			8×10^5			1.4×10^6		Bit Periods
POWER SUPPLY											
Voltage (V_{MIN} to V_{MAX})	T_A = +25°C	−4.5	−5.2	−5.5	−4.5	−5.2	−5.5	−4.5	−5.2	−5.5	Volts
Current	T_A = +25°C, V_{EE} = −5.2 V		125	170		125	170		140	180	mA
				180			180			205	mA
INPUT VOLTAGE LEVELS	T_A = +25°C										
Input Logic High, V_{IH}		−1.084		−0.72	−1.084		−0.72	−1.084		−0.72	Volts
Input Logic Low, V_{IH}		−1.95		−1.594	−1.95		−1.594	−1.95		−1.594	Volts
OUTPUT VOLTAGE LEVELS	T_A = +25°C										
Output Logic High, V_{OH}		−1.084		−0.72	−1.084		−0.72	−1.084		−0.72	Volts
Output Logic Low, V_{OL}		−1.95		−1.60	−1.95		−1.60	−1.95		−1.60	Volts
INPUT CURRENT LEVELS	T_A = +25°C										
Input Logic High, I_{IH}				125			125			125	μA
Input Logic Low, I_{IL}				80			80			80	μA
OUTPUT SLEW TIMES	T_A = +25°C										
Rise Time (t_R)	20%–80%		0.75	1.5		0.75	1.5		0.75	1.5	ns
Fall Time (t_F)	80%–20%		0.75	1.5		0.75	1.5		0.75	1.5	ns
SYMMETRY	ρ = 1/2, T_A = +25°C										
Recovered Clock Output	V_{EE} = −5.2 V	45		55	45		55	45		55	%

NOTES

[1]Refer to Glossary for parameter definition.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . −6 V
Input Voltage (Pin 16 or Pin 17 to V_{CC}) . . . . V_{EE} to +300 mV
Maximum Junction Temperature
SOIC Package . . . . . +150°C
Ceramic DIP Package . . . . . +175°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C
ESD Rating
AD800 . . . . . 1500 V
AD802 . . . . . 1000 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to an absolute maximum rating condition for an extended period may adversely affect device reliability.

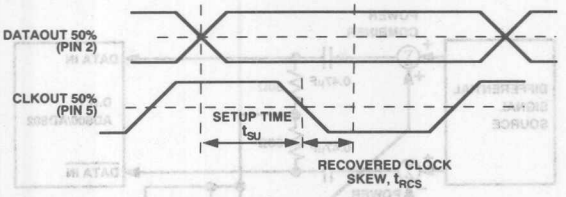

Figure 1. Recovered Clock Skew and Setup (See Previous Page)

PIN DESCRIPTIONS

Number	Mnemonic	Description
1	$\overline{\text{DATAOUT}}$	Differential Retimed Data Output
2	DATAOUT	Differential Retimed Data Output
3	V_{CC2}	Digital Ground
4	$\overline{\text{CLKOUT}}$	Differential Recovered Clock Output
5	CLKOUT	Differential Recovered Clock Output
6	V_{EE}	Digital V_{EE}
7	V_{EE}	Digital V_{EE}
8	V_{CC1}	Digital Ground
9	AV_{EE}	Analog V_{EE}
10	ASUBST	Analog Substrate
11	CF_2	Loop Damping Capacitor Input
12	CF_1	Loop Damping Capacitor Input
13	AV_{CC}	Analog Ground
14	V_{CC1}	Digital Ground
15	V_{EE}	Digital V_{EE}
16	DATAIN	Differential Data Input
17	$\overline{\text{DATAIN}}$	Differential Data Input
18	SUBST	Digital Substrate
19	$\overline{\text{FRAC}}$	Differential Frequency Acquisition Indicator Output
20	FRAC	Differential Frequency Acquisition Indicator Output

THERMAL CHARACTERISTICS

	θ_{JC}	θ_{JA}
SOIC Package	22°C/W	75°C/W
Cerdip Package	25°C/W	90°C/W

Use of a heatsink may be required depending on operating environment.

GLOSSARY

Maximum and Minimum Specifications
Maximum and minimum specifications result from statistical analyses of measurements on multiple devices and multiple test systems. Typical specifications indicate mean measurements. Maximum and minimum specifications are calculated by adding or subtracting an appropriate guardband from the typical specification. Device-to-device performance variation and test system-to-test system variation contribute to each guardband.

Nominal Center Frequency
This is the frequency that the VCO will operate at with no input signal present and the loop damping capacitor, C_D, shorted.

Tracking Range
This is the range of input data rates over which the PLL will remain in lock.

Capture Range
This is the range of input data rates over which the PLL can acquire lock.

Static Phase Error
This is the steady-state phase difference, in degrees, between the recovered clock sampling edge and the optimum sampling instant, which is assumed to be halfway between the rising and falling edges of a data bit. Gate delays between the signals that define static phase error, and IC input and output signals prohibit direct measurement of static phase error.

Data Transition Density, ρ
This is a measure of the number of data transitions, from "0" to "1" and from "1" to "0," over many clock periods. ρ is the ratio ($0 \le \rho \le 1$) of data transitions to clock periods.

Jitter
This is the dynamic displacement of digital signal edges from their long term average positions, measured in degrees rms, or Unit Intervals (UI). Jitter on the input data can cause dynamic phase errors on the recovered clock sampling edge. Jitter on the recovered clock causes jitter on the retimed data.

Output Jitter
This is the jitter on the retimed data, in degrees rms, due to a specific pattern or some psuedo-random input data sequence (PRN Sequence).

Jitter Tolerance
Jitter tolerance is a measure of the PLL's ability to track a jittery input data signal. Jitter on the input data is best thought of as phase modulation, and is usually specified in unit intervals.

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ORDERING GUIDE

Device	Center Frequency	Fractional Loop Bandwidth	Description	Operating Temperature	Package Option*
AD800-45BQ	44.736 MHz	0.1%	20-Pin Cerdip	−40°C to +85°C	Q-20
AD800-52BR	51.84 MHz	0.1%	20-Pin Plastic SOIC	−40°C to +85°C	R-20
AD802-155BR	155.52 MHz	0.08%	20-Pin Plastic SOIC	−40°C to +85°C	R-20
AD802-155KR	155.52 MHz	0.08%	20-Pin Plastic SOIC	0°C to +70°C	R-20

*For outline information see Package Information section.

the input jitter, some modulation signal must be generated at the output of the phase detector (see Figure 21). The modulation output from the phase detector can only be produced by a phase error between the data input and the clock input. Hence, the PLL can never perfectly track jittered data. However, the magnitude of the phase error depends on the gain around the loop. At low frequencies the integrator provides very high gain, and thus very large jitter can be tracked with small phase errors between input data and recovered clock. At frequencies closer to the loop bandwidth, the gain of the integrator is much smaller, and thus less input jitter can be tolerated. The PLL data output will have a bit error rate less than 1×10^{-10} when in lock and retiming input data that has the specified jitter applied to it.

Jitter Transfer
The PLL exhibits a low-pass filter response to jitter applied to its input data.

Bandwidth
This describes the frequency at which the PLL attenuates sinusoidal input jitter by 3 dB.

Peaking
This describes the maximum jitter gain of the PLL in dB.

Damping Factor, ζ
ζ describes how the PLL will track an input signal with a phase step. A greater value of ζ corresponds to less overshoot in the PLL response to a phase step. ζ is a standard constant in second order feedback systems.

Acquisition Time
This is the transient time, measured in bit periods, required for the PLL to lock on input data from its free-running state.

time equals the time that the clock signal is greater than the midpoint between its "0" level and its "1" level.

Bit Error Rate vs. Signal-to-Noise Ratio
The AD800 and AD802 were designed to operate with standard ECL signal levels at the data input. Although not recommended, smaller input signals are tolerable. Figure 8, 14, and 20 show the bit error rate performance versus input signal-to-noise ratio for input signal amplitudes of full 900 mV ECL, and decreased amplitudes of 80 mV and 20 mV. Wideband amplitude noise is summed with the data signals as shown in Figure 2. The full ECL and 80 mV signals give virtually indistinguishable results. The 20 mV signals also provide adequate performance when in lock, but signal acquisition may be impaired.

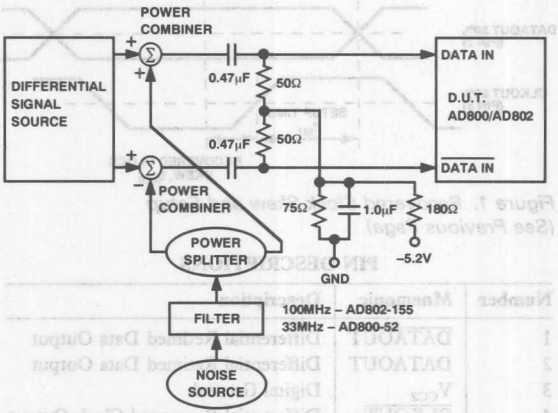

Figure 2. Bit Error Rate vs. Signal-to-Noise Ratio Test: Block Diagram

USING THE AD800 AND THE AD802 SERIES

Ground Planes
Use of one ground plane for connections to both analog and digital grounds is recommended. Output signal sensitivity to power supply noise (PECL configuration, Figure 22) is less using one ground plane than when using separate analog and digital ground planes.

Power Supply Connections
Use of a 10 μF tantalum capacitor between V_{EE} and ground is recommended.

Use of 0.1 μF ceramic capacitors between IC power supply or substrate pins and ground is recommended. Power supply decoupling should take place as close to the IC as possible. Refer to schematics, Figure 22 and Figure 26, for advised connections.

Sensitivity of IC output signals (PECL configuration, Figure 22) to high frequency power supply noise (at 2× the nominal data rate) can be reduced through the connection of signals AV_{CC} and V_{CC1}, and the addition of a bypass network. The type of bypass network to consider depends on the noise tolerance required. The more complex bypass network schemes tolerate greater power supply noise levels. Refer to Figures 23 and 24 for bypassing schemes and power supply sensitivity curves.

Transmission Lines
Use of 50 Ω transmission lines are recommended for DATAIN, CLKOUT, DATAOUT, and FRAC signals.

Terminations
Termination resistors should be used for DATAIN, CLKOUT, DATAOUT, and FRAC signals. Metal, thick film, 1% tolerance resistors are recommended. Termination resistors for the DATAIN signals should be placed as close as possible to the DATAIN pins.

Connections form V_{EE} to lead resistors for DATAIN, DATAOUT, FRAC, and CLKOUT signals should be individual, not daisy chained. This will avoid crosstalk on these signals.

Loop Damping Capacitor, C_D
A ceramic capacitor may be used for the loop damping capacitor.

Input Buffer
Use of an input buffer, such as a 10H116 Line Receiver IC, is suggested for an application where the DATAIN signals do not come directly from an ECL gate, or where noise immunity on the DATAIN signals is an issue.

Typical Characteristics

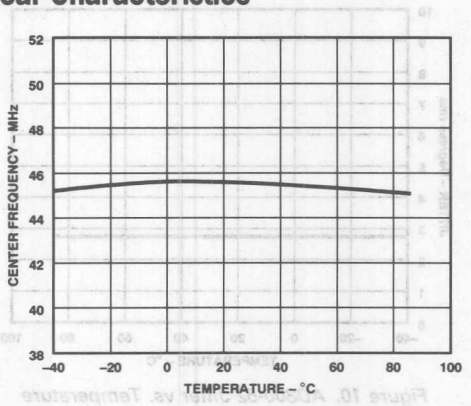

Figure 3. AD800-45 Center Frequency vs. Temperature

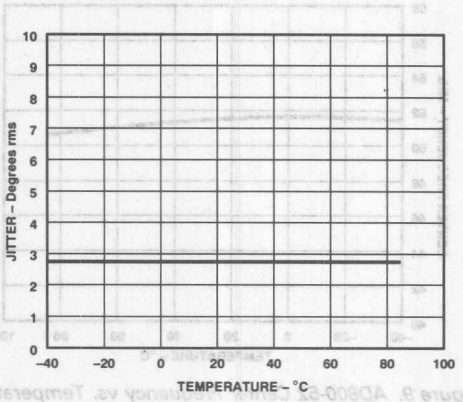

Figure 4. AD800-45 Jitter vs. Temperature

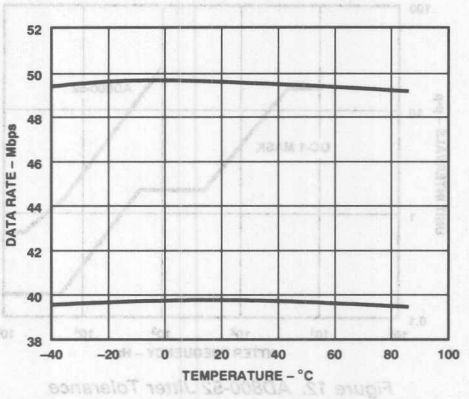

Figure 5. AD800-45 Capture and Tracking Range vs. Temperature

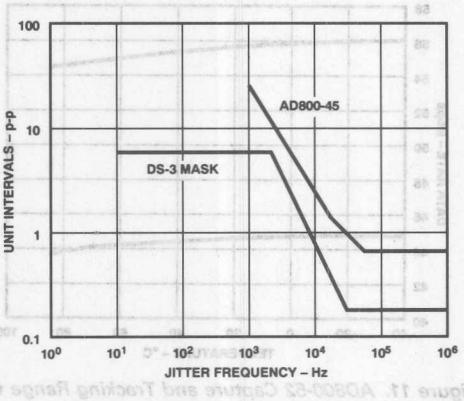

Figure 6. AD800-45 Jitter Tolerance

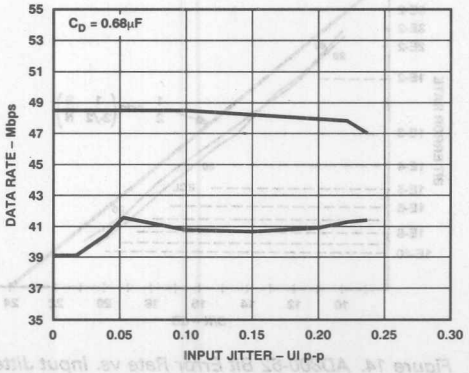

Figure 7. AD800-45 Acquisition Range vs. Input Jitter

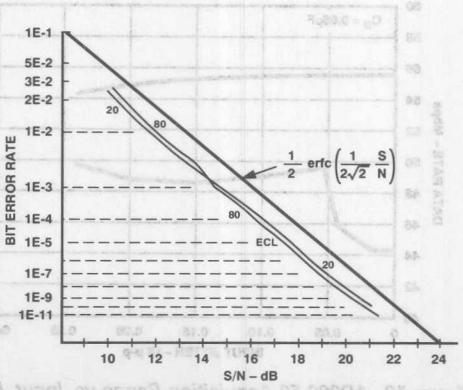

Figure 8. AD800-45 Bit Error Rate vs. Input Jitter

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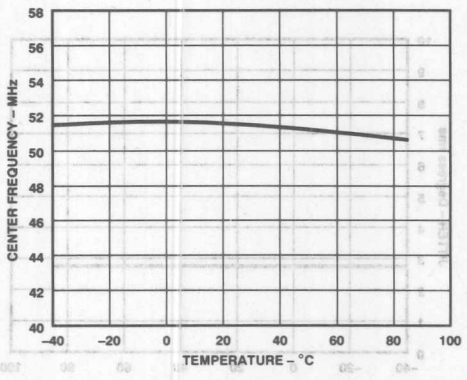

Figure 9. AD800-52 Center Frequency vs. Temperature

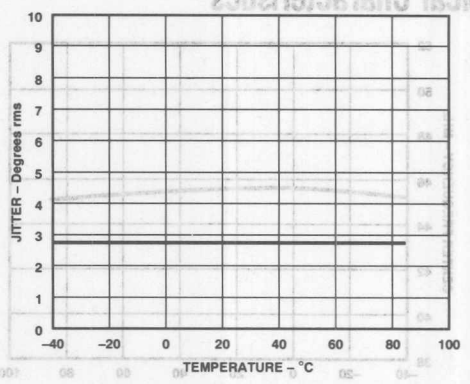

Figure 10. AD800-52 Jitter vs. Temperature

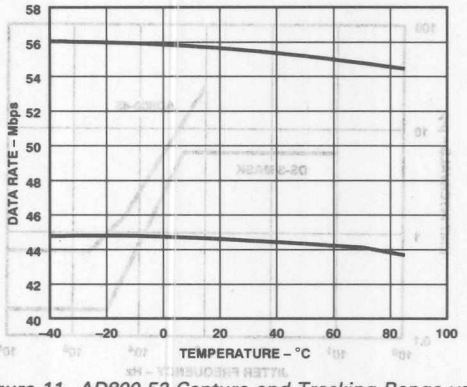

Figure 11. AD800-52 Capture and Tracking Range vs. Temperature

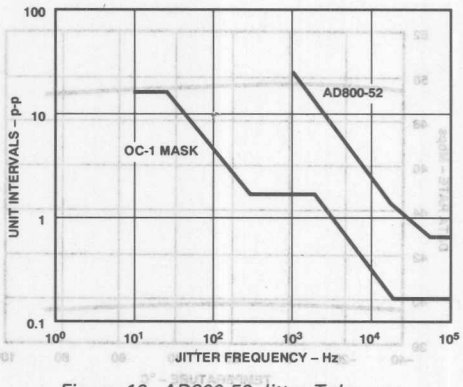

Figure 12. AD800-52 Jitter Tolerance

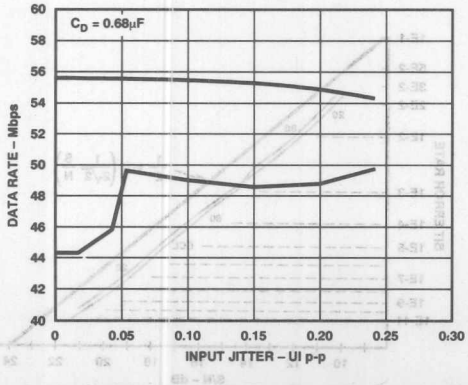

Figure 13. AD800-52 Acquisition Range vs. Input Jitter

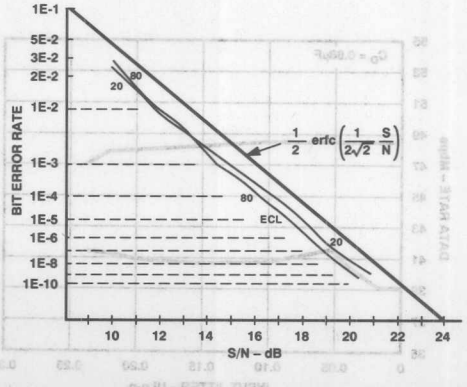

Figure 14. AD800-52 Bit Error Rate vs. Input Jitter

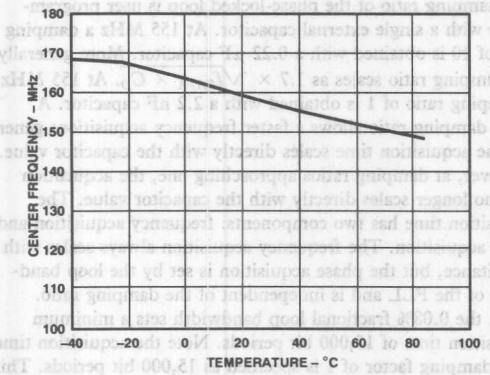

Figure 15. AD802-155 Center Frequency vs. Temperature

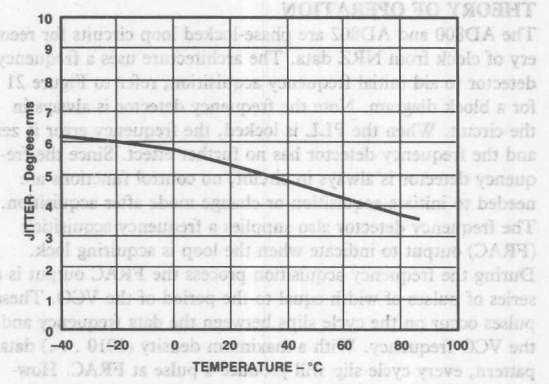

Figure 16. AD802-155 Output Jitter vs. Temperature

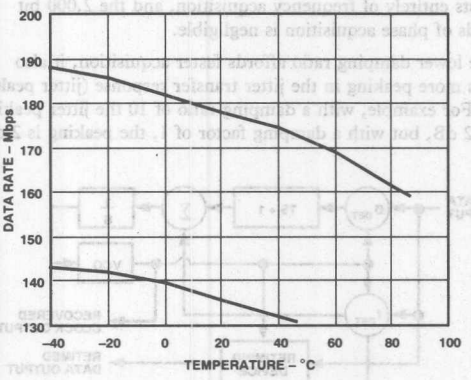

Figure 17. AD802-155 Capture Range, Tracking Range vs. Temperature

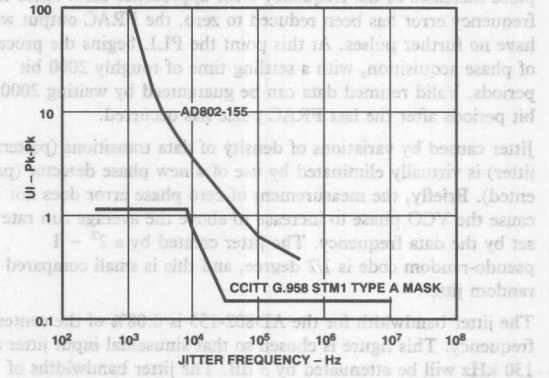

Figure 18. AD802-155 Jitter Tolerance

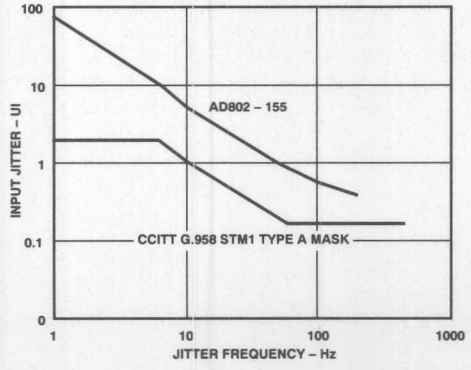

Figure 19. AD802-155 Minimum Acquisition Range vs. Jitter Frequency, T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}

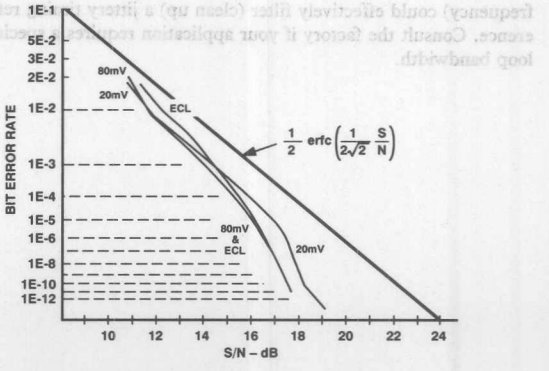

Figure 20. AD802-155 Bit Error Rate vs. Input Jitter

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THEORY OF OPERATION

The AD800 and AD802 are phase-locked loop circuits for recovery of clock from NRZ data. The architecture uses a frequency detector to aid initial frequency acquisition, refer to Figure 21 for a block diagram. Note the frequency detector is always in the circuit. When the PLL is locked, the frequency error is zero and the frequency detector has no further effect. Since the frequency detector is always in circuit, no control functions are needed to initiate acquisition or change mode after acquisition. The frequency detector also supplies a frequency acquisition (FRAC) output to indicate when the loop is acquiring lock. During the frequency acquisition process the FRAC output is a series of pulses of width equal to the period of the VCO. These pulses occur on the cycle slips between the data frequency and the VCO frequency. With a maximum density (1010 . . .) data pattern, every cycle slip will produce a pulse at FRAC. However, with random data, not every cycle slip produces a pulse. The density of pulses at FRAC increases with the density of data transitions. The probability that a cycle slip will produce a pulse increases as the frequency error approaches zero. After the frequency error has been reduced to zero, the FRAC output will have no further pulses. At this point the PLL begins the process of phase acquisition, with a settling time of roughly 2000 bit periods. Valid retimed data can be guaranteed by waiting 2000 bit periods after the last FRAC pulse has occurred.

Jitter caused by variations of density of data transitions (pattern jitter) is virtually eliminated by use of a new phase detector (patented). Briefly, the measurement of zero phase error does not cause the VCO phase to increase to above the average run rate set by the data frequency. The jitter created by a $2^7 - 1$ pseudo-random code is 1/2 degree, and this is small compared to random jitter.

The jitter bandwidth for the AD802-155 is 0.08% of the center frequency. This figure is chosen so that sinusoidal input jitter at 130 kHz will be attenuated by 3 dB. The jitter bandwidths of the AD800-45 and AD800-52 are 0.1% of the respective center frequencies. The jitter bandwidth of the AD800 or the AD802 is mask programmable from 0.01% to 1% of the center frequency. A device with a very low loop bandwidth (0.01% of the center frequency) could effectively filter (clean up) a jittery timing reference. Consult the factory if your application requires a special loop bandwidth.

The damping ratio of the phase-locked loop is user programmable with a single external capacitor. At 155 MHz a damping ratio of 10 is obtained with a 0.22 μF capacitor. More generally, the damping ratio scales as $1.7 \times \sqrt{f_{DATA} \times C_D}$. At 155 MHz a damping ratio of 1 is obtained with a 2.2 nF capacitor. A lower damping ratio allows a faster frequency acquisition; generally the acquisition time scales directly with the capacitor value. However, at damping ratios approaching one, the acquisition time no longer scales directly with the capacitor value. The acquisition time has two components: frequency acquisition and phase acquisition. The frequency acquisition always scales with capacitance, but the phase acquisition is set by the loop bandwidth of the PLL and is independent of the damping ratio. Thus, the 0.08% fractional loop bandwidth sets a minimum acquisition time of 15,000 bit periods. Note the acquisition time for a damping factor of 1 is specified as 15,000 bit periods. This comprises 13,000 bit periods for frequency acquisition and 2,000 periods for phase acquisition. Compare this to the 400,000 bit periods acquisition time specified for a damping ratio of 5; this consists entirely of frequency acquisition, and the 2,000 bit periods of phase acquisition is negligible.

While lower damping ratio affords faster acquisition, it also allows more peaking in the jitter transfer response (jitter peaking). For example, with a damping ratio of 10 the jitter peaking is 0.02 dB, but with a damping factor of 1, the peaking is 2 dB.

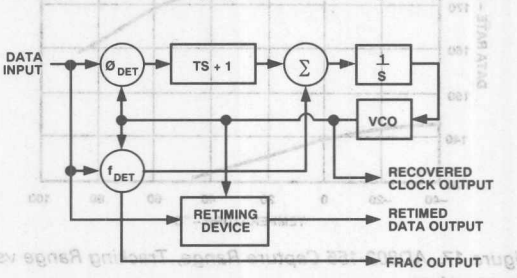
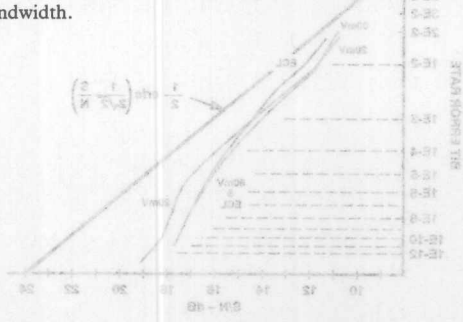
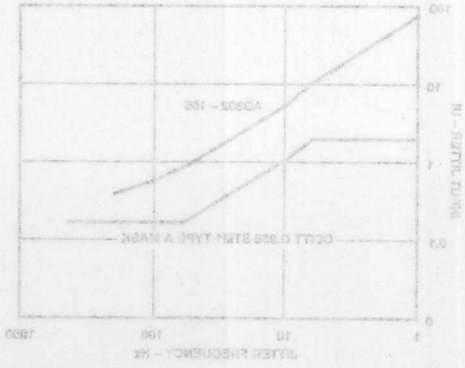


Figure 21. AD800 and AD802 Block Diagram





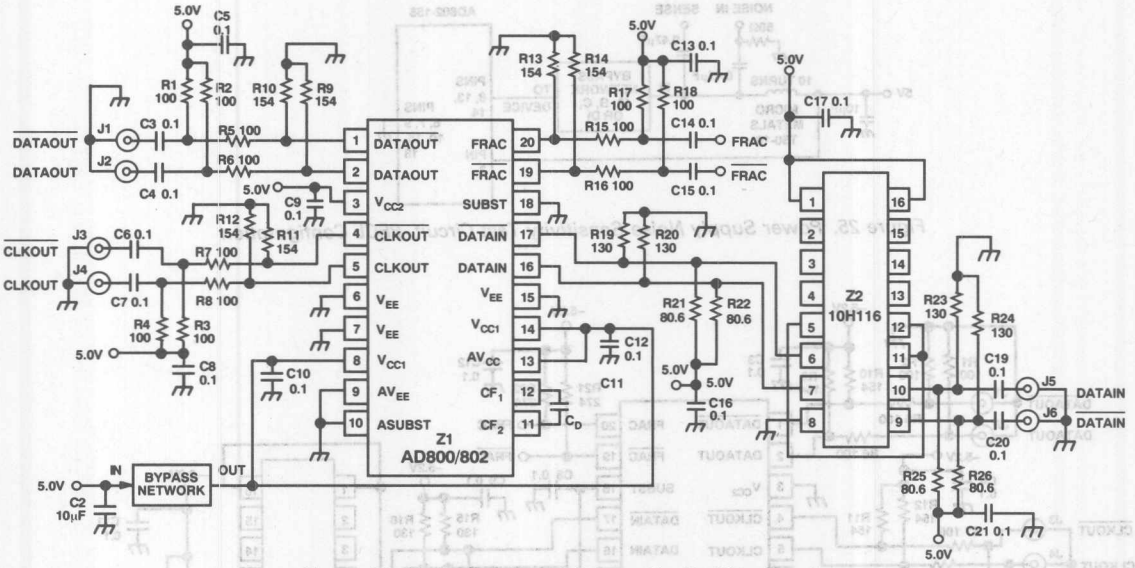


Figure 22. Evaluation Board Schematic, Positive Supply

Table I. Evaluation Board, Positive Supply: Components List

Reference Designator	Description	Quantity
R1–8, R15–18	Resistor, 100 Ω, 1%	12
R9–14	Resistor, 154 Ω, 1%	6
R19, 20, 23, 24	Resistor, 130 Ω, 1%	4
R21, 22, 25, 26	Resistor, 80.6 Ω, 1%	4
C_D	Capacitor, Loop Damping (See Specifications Page)	1
C2	Capacitor, 10 μF, Tantalum	1
C3–C21	Capacitor, 0.1 μF, Ceramic Chip	17
Z1	AD800/AD802	1
Z2	10H116, ECL Line Receiver	1

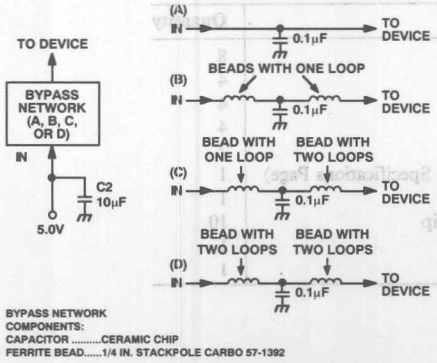


Figure 23. Bypass Network Schemes

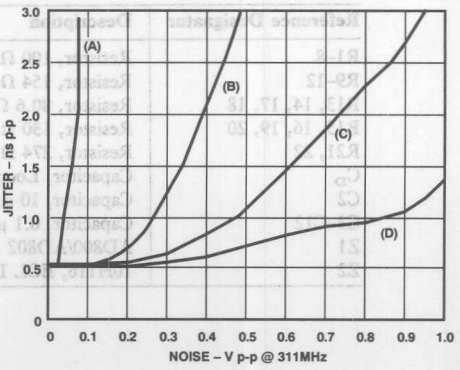


Figure 24. AD802-155 Output Jitter vs. Supply Noise (PECL Configuration)

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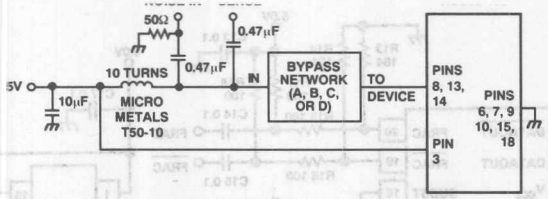

Figure 25. Power Supply Noise Sensitivity Test Circuit, PECL Configuration

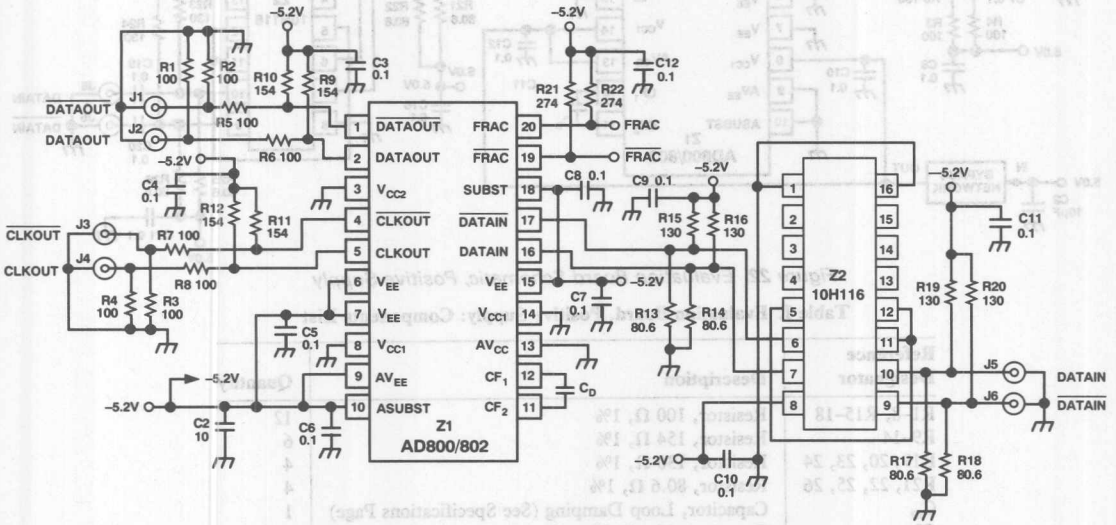

Figure 26. Evaluation Board Schematic, Negative Supply

Table II. Evaluation Board, Negative Supply: Components List

Reference Designator	Description	Quantity
R1–8	Resistor, 100 Ω, 1%	8
R9–12	Resistor, 154 Ω, 1%	4
R13, 14, 17, 18	Resistor, 80.6 Ω, 1%	4
R15, 16, 19, 20	Resistor, 130 Ω, 1%	4
R21, 22	Resistor, 274 Ω, 1%	2
C_D	Capacitor, Loop Damping (See Specifications Page)	1
C2	Capacitor, 10 μF, Tantalum	1
C3–C12	Capacitor, 0.1 μF, Ceramic Chip	10
Z1	AD800/AD802	1
Z2	10H116, ECL Line Receiver	1

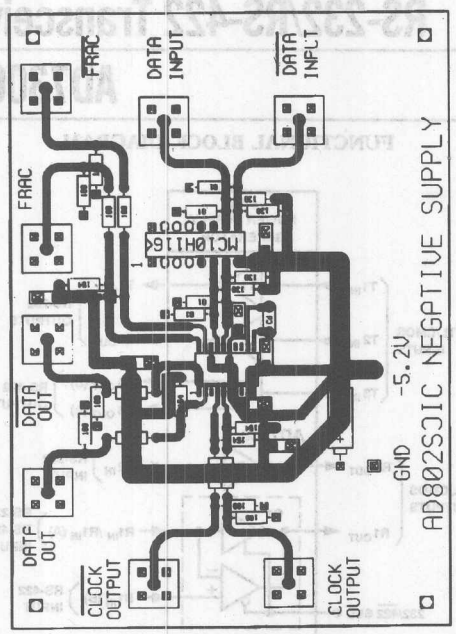

Figure 27. Negative Supply Configuration: Component Side (Top Layer)

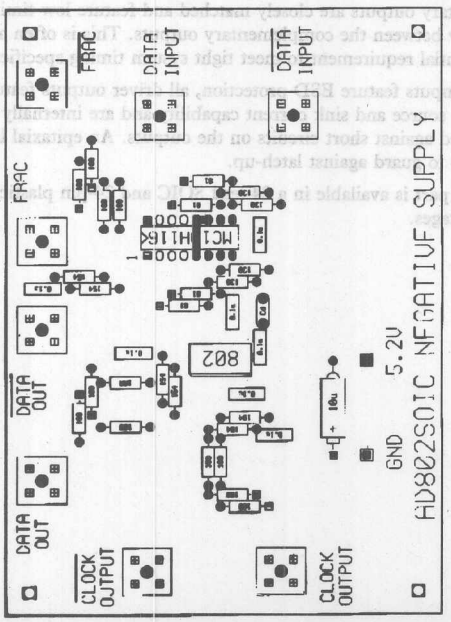

Figure 28. Negative Supply Configuration: Solder Side

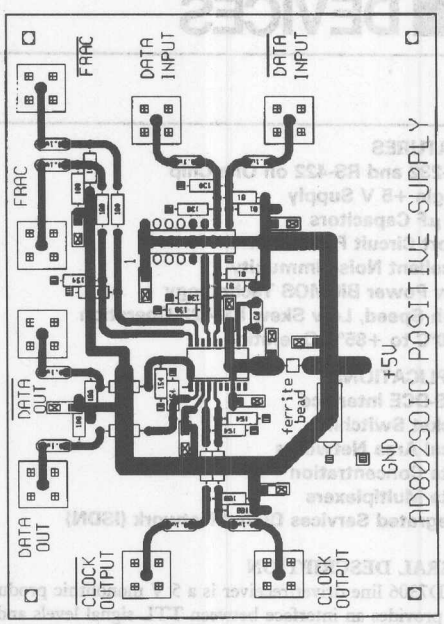

Figure 29. Positive Supply Configuration: Component Side (Top Layer)

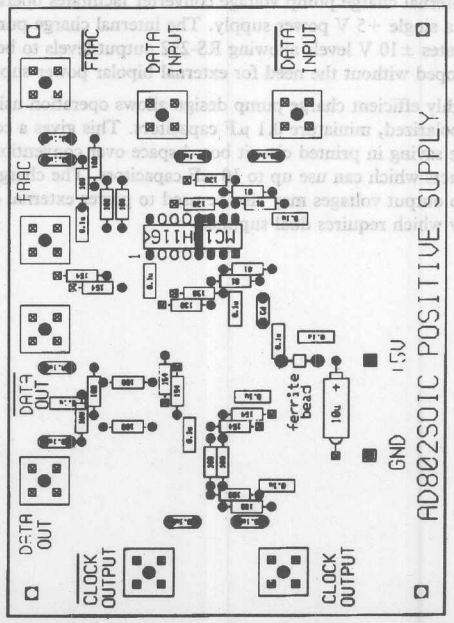

Figure 30. Positive Supply Configuration: Solder Side

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+5 V Powered RS-232/RS-422 Transceiver

AD7306

FEATURES
RS-232 and RS-422 on One Chip
Single +5 V Supply
0.1 μF Capacitors
Short Circuit Protection
Excellent Noise Immunity
Low Power BiCMOS Technology
High Speed, Low Skew RS-422 Operation
−40°C to +85°C Operation

APPLICATIONS
DTE-DCE Interface
Packet Switching
Local Area Networks
Data Concentration
Data Multiplexers
Integrated Services Digital Network (ISDN)

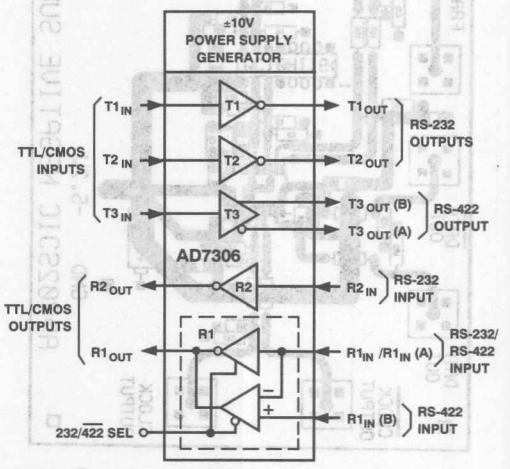
GENERAL DESCRIPTION

The AD7306 line driver/receiver is a 5 V monolithic product which provides an interface between TTL signal levels and dual standard EIA RS-232/RS-422 signal levels. The part contains two RS-232 drivers, one RS-422 driver, one RS-232 receiver, and one receiver path which can be configured either as RS-232 or as RS-422.

An internal charge pump voltage converter facilitates operation from a single +5 V power supply. The internal charge pump generates ±10 V levels allowing RS-232 output levels to be developed without the need for external bipolar power supplies.

A highly efficient charge pump design allows operation using non polarized, miniature 0.1 μF capacitors. This gives a considerable saving in printed circuit board space over conventional products which can use up to 10 μF capacitors. The charge pump output voltages may also be used to power external circuitry which requires dual supplies.

FUNCTIONAL BLOCK DIAGRAM



The RS-232 channels are suitable for communications rates up to 100 kHz and the RS-422 channels are suitable for high speed communications up to 5 MHz. The RS-422 transmitter complementary outputs are closely matched and feature low timing skew between the complementary outputs. This is often an essential requirement to meet tight system timing specifications.

All inputs feature ESD protection, all driver outputs feature high source and sink current capability and are internally protected against short circuits on the outputs. An epitaxial layer is used to guard against latch-up.

The part is available in a 24-lead SOIC and 24-pin plastic DIP packages.

SPECIFICATIONS (V_{CC} = +5 V ± 5%, C1 = C2 = C3 = C4 = 0.1 µF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
RS-232 DRIVER					
TTL Input Logic Low, V_{INL}			0.8	V	
TTL Input Logic High, V_{INH}	2.0			V	
Input Logic Current		0.1	±10	µA	V_{IN} = 0 V to V_{CC}
RS-232 High Level Output Voltage	5.0	7.3		V	R_L = 3 kΩ
RS-232 Low Level Output Voltage	−5.0	−6.5		V	R_L = 3 kΩ
Output Short Circuit Current	±5	±12		mA	V_{OUT} = 0 V, T_A = 0°C to +70°C
Slew Rate	8	20	30	V/µs	C_L = 50 pF, R_L = 3 kΩ
		4		V/µs	C_L = 2500 pF, R_L = 3 kΩ
Output Resistance (Powered Down)	300	10M		Ω	V_{CC} = 0 V, V_{OUT} = ±3 V
RS-232 RECEIVER					
Input Voltage Range	−15		+15	V	
RS-232 Input Threshold Low	0.8	1.3		V	
RS-232 Input Threshold High		1.7	2.4	V	
RS-232 Input Hysteresis	0.1	0.4	1.0	V	
RS-232 Input Resistance	3	5	7	kΩ	
TTL Output Voltage Low, V_{OL}		0.2	0.4	V	I_{OUT} = +4 mA
TTL Output Voltage High, V_{OH}	3.5	4.8		V	I_{OUT} = −4 mA
RS-422 DRIVER					
TTL Input Logic Low, V_{INL}			0.8	V	
TTL Input Logic High, V_{INH}	2.0			V	
Logic Input Current		0.1	±10	µA	V_{IN} = 0 V to V_{CC}
Differential Output Voltage			5.0	V	V_{CC} = 5 V, R_L Diff = ∞; Figure 3
	2			V	R_L Diff = 100 Ω; Figure 3
Common-Mode Output Voltage			3	V	
$\Delta\|V_{OUT}\|$ for Complementary O/P States			0.2	V	R_L Diff = 100 Ω
Output Short Circuit Current	35		150	mA	0 V ≤ V_{CMR} ≤ +7 V
RS-422 RECEIVER					
Common-Mode Voltage Range			±7	V	Typical RS-422 Input Voltage <5 V
Differential Input Threshold Voltage	−0.2		+0.2	V	
Input Voltage Hysteresis		70		mV	V_{CM} = 0 V
Input Resistance	3	5	7	kΩ	
TTL Output Voltage Low, V_{OL}		0.2	0.4	V	I_{OUT} = +4.0 mA
TTL Output Voltage High, V_{OH}	3.5	4.8		V	I_{OUT} = −4.0 mA
232/$\overline{422}$ SEL Input					
Input Logic Low, V_{INL}			0.8	V	
Input Logic High, V_{INH}	2.0			V	
Logic Input Current		0.1	±10	µA	V_{IN} = 0 V to V_{CC}
POWER SUPPLY CURRENT					
I_{CC}		10	15	mA	Outputs Unloaded
CHARGE PUMP VOLTAGE GENERATOR					
V+ Output Voltage		9		V	RS-232 Output Unloaded; See Typical Performance Curves
V− Output Voltage		−9		V	RS-232 Outputs Unloaded; See Typical Performance Curves
Generator Rise Time		200		µs	

Specifications subject to change without notice.

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TIMING SPECIFICATIONS (V_{CC} = +5 V ± 5%, C_1 – C_2 – C_3 – C_4 = 0.1 μF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Typ	Max	Units	Test Conditions/Comments
RS-422 Driver				
Propagation Delay Input to Output T_{PLH}, T_{PHL}	35	100	ns	R_L Diff = 100 Ω, C_{L1} = C_{L2} = 100 pF, Figures 2 & 4
RS-422 O/P to $\overline{O/P}$ T_{SKEW}	2	10	ns	R_L Diff = 100 Ω, C_{L1} = C_{L2} = 100 pF, Figures 2 & 4
Driver Rise/Fall Time T_R, T_F	15	40	ns	R_L Diff = 100 Ω, C_{L1} = C_{L2} = 100 pF, Figures 2 & 4
RS-422 Receiver				
Propagation Delay Input to Output T_{PLH}, T_{PHL}	70	200	ns	C_L = 15 pF. Figure 5
RS-232/RS-422 Enable				
RS-232 Disable to RS-422 Enable T_{EN1}	70	200	ns	Figure 6
RS-422 Disable to RS-232 Enable T_{EN2}	70	200	ns	Figure 6
Transmission Rate (RS-422)	5		MHz	
RS-232 Receiver				
Propagation Delay Input to Output	1000		ns	
Transmission Rate (RS-232)	100		kHz	C_L = 50 pF
	20		kHz	C_L = 2.5 nF

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{CC} . . . . . +7 V
V+ . . . . . (V_{CC} −0.3 V) to +13.2 V
V− . . . . . +0.3 V to −13.2 V
Inputs
$T1_{IN}$, $T2_{IN}$ . . . . . V− to V+
$T3_{IN}$ . . . . . −0.3 V to V+
$R1_{IN}$ A/B, $R2_{IN}$ . . . . . −25 V to +25 V
232/$\overline{422}$ SEL . . . . . −0.3 V to V+
Outputs
$T1_{OUT}$, $T2_{OUT}$ . . . . . −15 V to +15 V
$T3_{OUT}$(A), (B) . . . . . −0.3 V to +7 V
$R1_{OUT}$, $R2_{OUT}$ . . . . . −0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
T_{OUT} . . . . . Continuous
Power Dissipation
Small Outline . . . . . 650 mW
DIP . . . . . 650 mW
Operating Temperature Range
Commercial (J Version) . . . . . 0°C to +70°C
Industrial (A Version) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

CAUTION

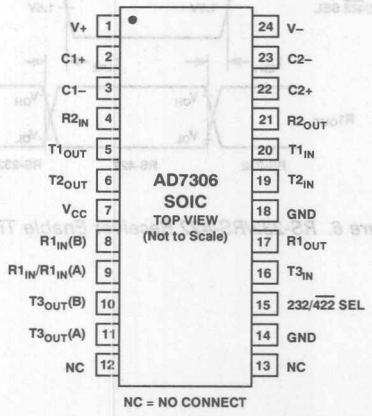
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7306 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

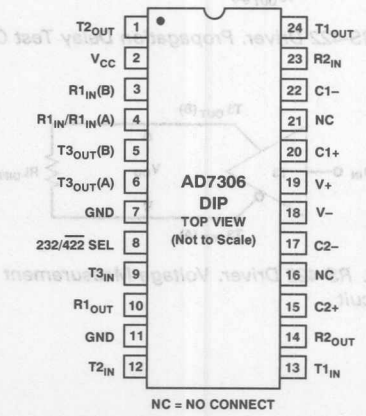
Model	Temperature Range	Package Description	Package Option*
AD7306JR	0°C to +70°C	24-Lead SOIC	R-24
AD7306JN	0°C to +70°C	24-Pin DIP	N-24
AD7306AR	−40°C to +85°C	24-Lead SOIC	R-24
AD7306AN	−40°C to +85°C	24-Pin DIP	N-24

*For outline information see Package Information section.

SOIC Pin	DIP Pin	Mnemonic	Function
1	19	V+	Internally Generated Positive Supply (+9 V nominal). A 0.1 μF capacitor must be connected between this pin and GND.
2, 3	20, 22	C1+, C1−	External Capacitor 1 Terminals. A 0.1 μF capacitor must be connected between these pins.
4	23	$R2_{IN}$	RS-232 Receiver R2 Input. This input accepts RS-232 input voltages.
5	24	$T1_{OUT}$	RS-232 Transmitter (Driver) T1 Output (Typically ±7.5 V).
6	1	$T2_{OUT}$	RS-232 Transmitter (Driver) T2 Output (Typically ±7.5 V).
7	2	V_{CC}	Power Supply Input (5 V ± 5%).
8	3	$R1_{IN}$ (B)	RS-422 Receiver R1, Differential Input B.
9	4	$R1_{IN}/R1_{IN}$ (A)	Receiver R1 Input. May be configured to accept either single ended RS-232 levels or differential RS-422 levels. It is configured using the 232/$\overline{422}$ SEL pin.
10	5	$T3_{OUT}$ (B)	RS-422 Transmitter (Driver) T3, Differential Output B.
11	6	$T3_{OUT}$ (A)	RS-232 Transmitter (Driver) T3, Differential Output A.
12, 13	16, 21	NC	No Connect Pins.
14, 18	7, 11	GND	Ground Pin. Must be connected to 0 V.
15	8	232/$\overline{422}$ SEL	Select Input. This input configures Receiver R1 to accept either RS-232 or RS-422 signal levels. A Logic 1 on this input selects 232 operation while a Logic 0 selects 422 operation.
16	9	$T3_{IN}$	TTL/CMOS Input to the RS-422 Transmitter T3.
17	10	$R1_{OUT}$	TTL/CMOS Output from Receiver R1.
19	12	$T2_{IN}$	TTL/CMOS Input to RS-232 Transmitter T2.
20	13	$T1_{IN}$	TTL/CMOS Input to RS-232 Transmitter T1.
21	14	$R2_{OUT}$	TTL/CMOS Output from Receiver R2.
22, 23	15, 17	C2+, C2−	External Capacitor 2 Terminals. A 0.1 μF capacitor must be connected between these pins.
24	18	V−	Internally Generated Negative Supply (−9 V nominal). A 0.1 μF capacitor must be connected between this pin and GND



SOIC Pin Configuration



DIP Pin Configuration

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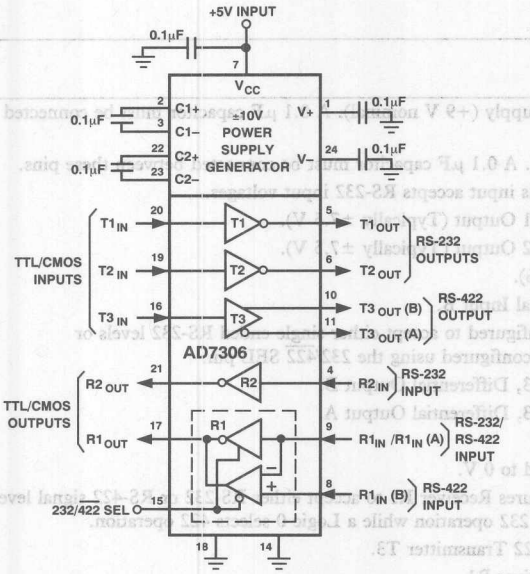

Figure 1. AD7306 Application Circuit (SOIC Package)

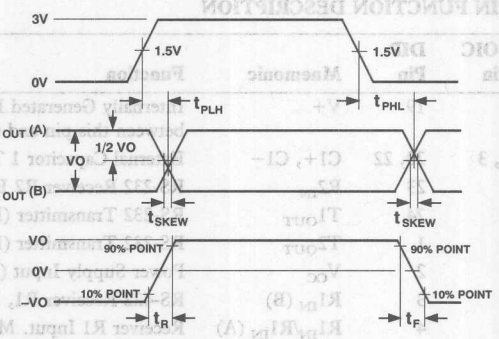

Figure 4. RS-422 Driver. Propagation Delay, Rise/Fall Timing

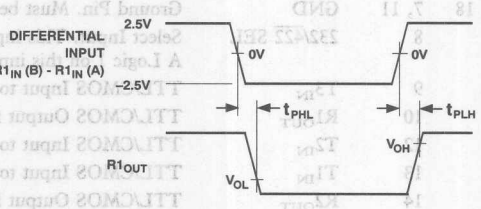

Figure 5. RS-422 Receiver Timing

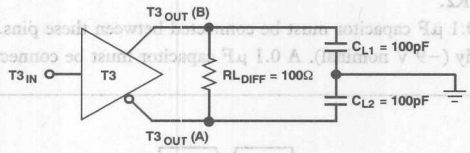

Figure 2. RS-422 Driver. Propagation Delay Test Circuit

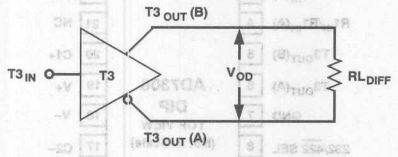

Figure 3. RS-422 Driver. Voltage Measurement Test Circuit

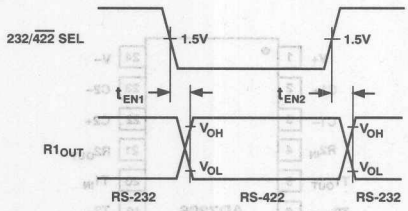

Figure 6. RS-232/RS-422 Receiver Enable Timing

GENERAL DESCRIPTION

The AD7306 drivers/receivers provide an interface which is compatible with RS-232/RS-422 standard interfaces. As both standards are widely accepted it is often necessary to provide an interface which is compatible with both. The AD7306 is ideally suited to this type of application as both standards may be met using a single package. This part contains two RS-232 drivers, one RS-422 driver, one RS-232 receiver, and one receiver path which can be configured as either RS-232 or RS-422. This receiver is configured using the 232/$\overline{422}$ SEL pin.

This part also contains an internal charge pump voltage converter which facilitates operation using a single +5 V power supply.

Charge Pump DC-DC Voltage Generator

The charge pump voltage generator uses a switched capacitor technique to develop ±10 V levels from an input +5 V supply. A highly efficient charge pump design coupled with a high frequency internal oscillator permit operation using four 0.1 μF capacitors.

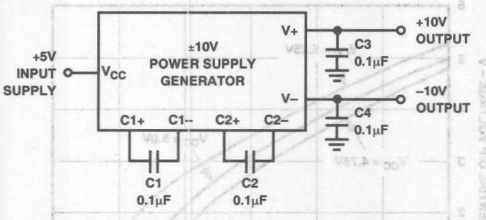

Figure 7. Charge Pump Voltage Generator

Capacitors C1 and C2 act as charge storage capacitors while C3 and C4 provide output smoothing. For correct operation all four capacitors must be included. Either polarized or nonpolarized capacitors may be used for C1–C4. If a polarized type is used, then the correct polarity should be observed. This may be ignored with nonpolarized type capacitors.

The charge pump output voltages, V+ and V−, are used internally to power the RS-232 transmitters. This permits RS-232 output levels to be developed on the RS-232 transmitter outputs. The charge pump output voltages may also be used to power external circuitry if the current requirements are small. Please refer to the Typical Performance Characteristics.

The generator rise time after power up is 200 μs typical. This time is necessary to completely charge the storage capacitors in the charge pump. Therefore, RS-232 data transmission should not be initiated until this time has elapsed after switch on. This will ensure that valid data is always transmitted.

RS-232 Drivers

The RS-232 drivers in the AD7306 meet the EIA RS-232 specifications. The drivers are inverting level shifters which convert TTL/CMOS levels into RS-232 output levels. The input switching threshold is typically 1.3 V. With a typical RS-232 load, the output levels are ±7.5 V. Under worst case load conditions, the drivers are guaranteed to provide ±5 V which meets the minimum RS-232 requirement. The output slew rate is internally limited to <30 V/μs without the need for an external slew-limiting capacitor. Short circuit protection is also provided which prevents damage in the event of output fault conditions. Active current limiting is used which limits the output short circuit current to less than 12 mA in the event of an output fault. This type of current limiting does not degrade the output voltage swing under normal loading conditions as would be the case with conventional passive limiting.

The powered-down output impedance is typically 10 MΩ. This is considerably larger than the 300 Ω minimum value required by the RS-232 specification. It provides additional protection under fault conditions where another powered-up transmitter output is inadvertently shorted to the powered-down device.

RS-232 Receivers

The receivers are inverting level shifters which accept RS-232 input levels (±3 V to ±15 V) and translates them into 5 V TTL/CMOS levels. The input switching thresholds are 0.8 V minimum and 2.4 V maximum which are well within the RS-232 requirement of ±3 V. Internal 5 kΩ pull-down resistors to GND are provided on the receiver inputs. This ensures that an unconnected input will be interpreted as a low level giving a Logic "1" on the TTL/CMOS output. Excellent noise immunity is achieved by the use of hysteresis and internal filtering circuitry. The filter rejects noise glitches of up to 0.5 μs in duration.

RS-422 Driver

The RS-422 driver on the AD7306 accepts a TTL/CMOS input and translates it into a differential RS-422 level signal. The input switching threshold is typically 1.3 V. The unloaded output differential voltage is typically ±5 V (see Typical Performance Characteristics). Short circuit protection is provided on the output which limits the current to less than 150 mA.

RS-422 Receiver

The RS-422 receiver on the AD7306 accepts a differential input signal and translates it into a TTL/CMOS output level. The input resistance on both differential inputs is 5 kΩ typical. With the receiver inputs unconnected (floating), internal biasing ensures that the receiver output is a Logic "1."

Excellent noise immunity and high transmission speed is achieved using the differential configuration.

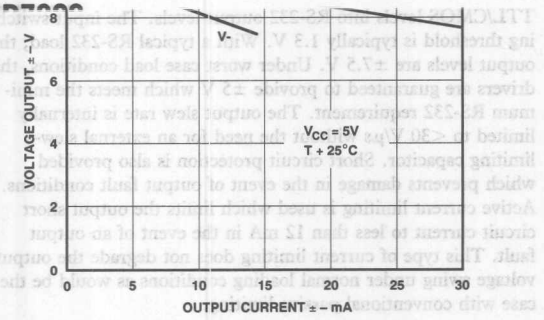

Figure 8. V+ and V– Voltage vs. Current

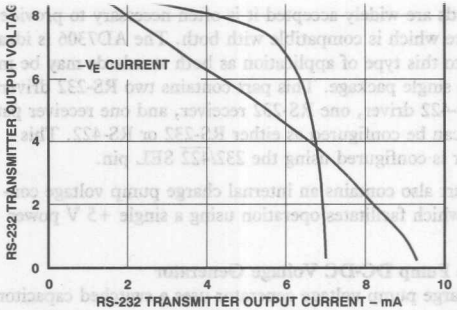

Figure 11. RS-232 Driver Output Voltage vs. Current

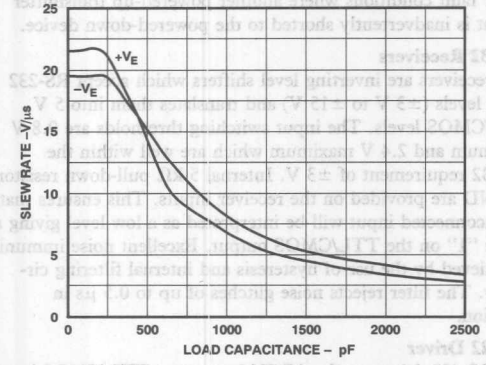

Figure 9. RS-232 Driver Slew Rate vs. Load Capacitance

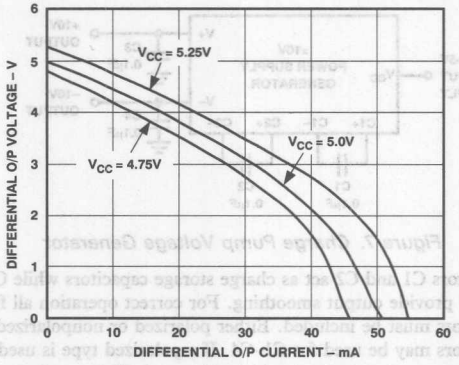

Figure 12. RS-422 Driver Output Current vs. Output Voltage

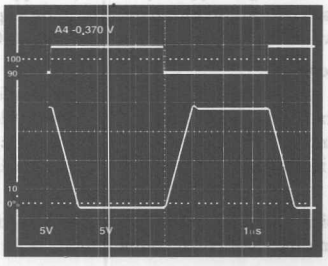

Figure 10. RS-232 Driver; R_L = 5 kΩ, C_L = 50 pF

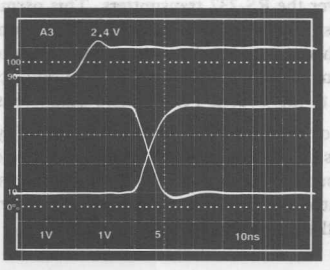

Figure 13. RS-422 Driver; R_{LDIFF} = 100 Ω, C_{L1} = C_{L2} = 100 pF

Single-Ended Data Transmission

Single-ended interfaces are used for low speed, short distance communications such as from a computer terminal to a printer. A single line is used to carry the signal. Various standards have been developed to standardize the communication link, the most popular of these being the RS-232. The RS-232 standard was introduced in 1962 by the EIA and has been widely used throughout the industry. The standard has been revised several times, and the current revision is known as EIA-232E. The RS-232 standard is suitable for single-ended data transmission at relatively slow data rates over short distances. A typical RS-232 interface is shown in Figure 14.

Figure 14. Single-Ended RS-232 Interface

Differential Data Transmission

When transmitting at high data rates, over long distances and through noisy environments, single-ended data transmission is often inadequate. In this type of application, differential data transmission offers superior performance. Differential transmission uses two signal lines to transmit data. It rejects ground shifts and is insensitive to noise signals which appear as common mode voltages on the transmission lines. To accommodate faster data communication, the differential RS-422 standard was developed. Therefore, it can be used to reliably transmit data at higher speeds and over longer distances than single-ended transmission. A typical RS-422 interface is shown in Figure 15.

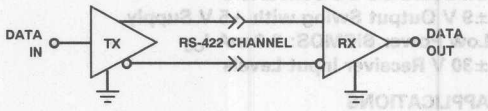

Figure 15. Differential RS-422 Interface

Table I. Comparison of RS-232 and RS-422 Interface Standards

Specification	EIA-232E	RS-422
Transmission Type	Single-Ended	Differential
Maximum Data Rate	20 kB/s	10 MB/s
Maximum Cable Length	Load Dependent	4000 ft
Minimum Driver Output Voltage	±5 V	±1.5 V
Slew Rate	30 V/μs max	–
Receiver Input Resistance	3 kΩ to 7 kΩ	4 kΩ min
Receiver Input Sensitivity	±3 V	±200 mV
Receiver Input Voltage Range	±15 V	±7 V
No. of Drivers per Line	1	1
No. of Receivers per Line	1	10

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High Speed, +5 V, 0.1 μF CMOS RS-232 Drivers/Receivers

ADM202/ADM203

FEATURES

120 kB Transmission Rate
ADM202: Small (0.1 μF) Charge Pump Capacitors
ADM203: No External Capacitors Required
Single 5 V Power Supply
Meets EIA-232-E and V.28 Specifications
Two Drivers and Two Receivers
On-board DC-DC Converters
±9 V Output Swing with +5 V Supply
Low Power BiCMOS: 2.0 mA I_{CC}
±30 V Receiver Input Levels

APPLICATIONS

Computers
Peripherals
Modems
Printers
Instruments

GENERAL DESCRIPTION

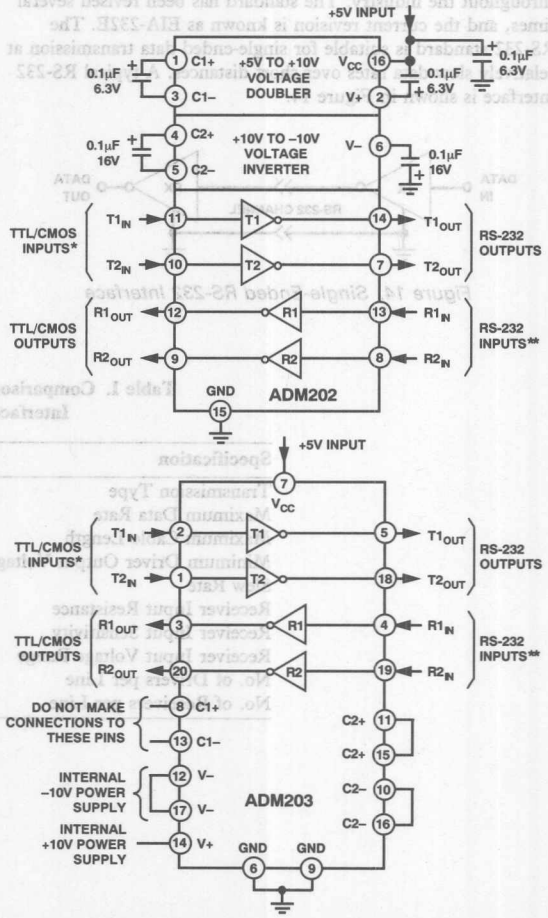
The ADM202/ADM203 is a two-channel RS-232 line driver/receiver pair designed to operate from a single +5 V power supply. A highly efficient on-chip charge pump design permits RS-232 levels to be developed using charge pump capacitors as small as 0.1 μF. The capacitors are internal to the package on the ADM203 so no external capacitors are required. These converters generate ±10 V RS-232 output levels.

The ADM202/ADM203 meets or exceeds the EIA-232-E and V.28 specifications. Fast driver slew rates permit operation up to 120 kB while high drive currents allows for extended cable lengths.

An epitaxial BiCMOS construction minimizes power consumption to 10 mW and also guards against latch-up. Overvoltage protection is provided allowing the receiver inputs to withstand continuous voltages in excess of ±30 V. In addition, all pins contain ESD protection to levels greater than 2 kV.

The ADM202 is available in 16-lead DIP and both narrow and wide SOIC packages. The ADM203 is available in a 20-pin DIP package.

FUNCTIONAL BLOCK DIAGRAMS



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (V_{CC} = +5 V ±10%, (ADM202 C1–C4 = 0.1 µF). All Specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Output Voltage Swing	±5	±9		V	V_{CC} = 5 V ± 5%, $T1_{OUT}$, $T2_{OUT}$ Loaded with 3 kΩ to GND
Output Voltage Swing	±5	±9		V	V_{CC} = 5 V ± 10%, T_A = +25°C, $T1_{OUT}$, $T2_{OUT}$ Loaded with 3 kΩ to GND
V_{CC} Power Supply Current		1.5	2	mA	No Load, $T1_{IN}$, $T2_{IN}$ = V_{CC}
		3.0	4	mA	No Load, $T1_{IN}$, $T2_{IN}$ = GND
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}
Input Logic Threshold High, V_{INH}	2.0			V	T_{IN}
Logic Pull-Up Current		10	25	µA	T_{IN} = 0 V
RS-232 Input Voltage Range	−30		+30	V	
RS-232 Input Threshold Low	0.8	1.2		V	
RS-232 Input Threshold High		1.7	2.4	V	
RS-232 Input Hysteresis	0.2	0.5	1.0	V	
RS-232 Input Resistance	3	5	7	kΩ	
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 1.6 mA
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = −1.0 mA
Propagation Delay		0.5	5	µs	RS-232 to TTL
Instantaneous Slew Rate[1]		25	30	V/µs	C_L = 10 pF, R_L = 3-7 kΩ, T_A = +25°C
Transition Region Slew Rate		5		V/µs	R_L = 3 kΩ, C_L = 2500 pF Measured from +3 V to −3 V or −3 V to +3 V
Baud Rate	120			kB	R_L = 3 kΩ, C_L = 1 nF
Output Resistance	300			Ω	V_{CC} = V+ = V− = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±10	±60	mA	

NOTE
[1]Sample tested to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} . . . . . +6 V
V+ . . . . . (V_{CC} − 0.3 V) to +14 V
V− . . . . . +0.3 V to −14 V
Input Voltages
  T_{IN} . . . . . −0.3 V to (V_{CC} + 0.3 V)
  R_{IN} . . . . . ±30 V
Output Voltages
  T_{OUT} . . . . . (V+, +0.3 V) to (V−, − 0.3 V)
  R_{OUT} . . . . . −0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
  T_{OUT} . . . . . Continuous
Power Dissipation
  N-16 DIP . . . . . 470 mW
  R-16N SOIC . . . . . 600 mW
  R-16W SOIC . . . . . 500 mW
  N-20 DIP . . . . . 890 mW
Thermal Impedance
  N-16 DIP . . . . . 135°C/W
  R-16N SOIC . . . . . 105°C/W
  R-16W SOIC . . . . . 105°C/W
  N-20 DIP . . . . . 125°C/W
Operating Temperature Range
  Commercial (J Version) . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature Soldering
  Vapor Phase (60 sec) . . . . . +215°C
  Infrared (15 sec) . . . . . +220°C
ESD Rating . . . . . >2000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM202JN	0°C to +70°C	N-16
ADM202JRN	0°C to +70°C	R-16N
ADM202JRW	0°C to +70°C	R-16W
ADM203JN	0°C to +70°C	N-20

*For outline information see Package Information section.

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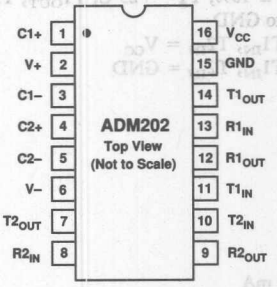
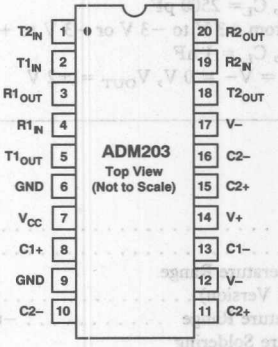
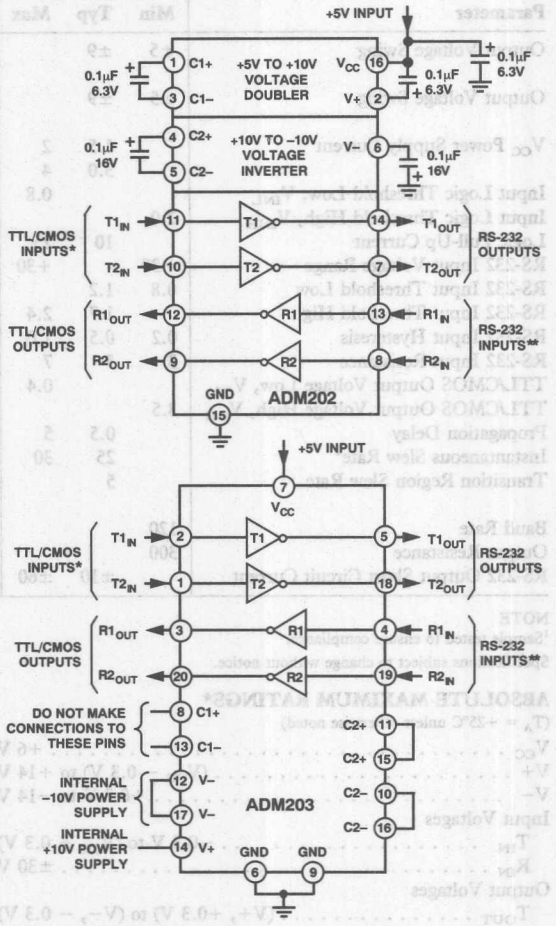
PIN CONFIGURATIONS

DIP/SOIC



DIP





*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 1. Typical Operating Circuits

PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power Supply Input 5 V ± 10%.
V+	Internally Generated Positive Supply (+10 V nominal).
V−	Internally Generated Negative Supply (−10 V nominal).
GND	Ground Pin. Must be connected to 0 V.
C1+	ADM202 External Capacitor, (+ terminal) is connected to this pin. ADM203: The capacitor is connected internally and no external capacitor is required.
C1−	ADM202 External Capacitor, (− terminal) is connected to this pin. ADM203: The capacitor is connected internally and no external capacitor is required.
C2+	ADM202 External Capacitor, (+ terminal) is connected to this pin. ADM203: The capacitor is connected internally and no external capacitor is required.
C2−	ADM202 External Capacitor, (− terminal) is connected to this pin. ADM203: The capacitor is connected internally and no external capacitor is required.
T_{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V_{CC} is connected on each input.
T_{OUT}	Transmitter (Driver) Outputs. These are RS-232 levels (typically ±10 V).

R_{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each of these inputs.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.

GENERAL INFORMATION

The ADM202/ADM203 is an RS-232 drivers/receivers designed to solve interface problems by meeting the EIA-232E specifications while using a single digital +5 V supply. The EIA standard requires transmitters that will deliver ±5 V minimum on the transmission channel and receivers that can accept signal levels down to ±3 V. The parts achieve this by integrating step up voltage converters and level shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation to an absolute minimum.

The ADM203 uses internal capacitors and, therefore, no external capacitors are required.

The ADM202 contains an internal voltage doubler and a voltage inverter which generates ±10 V from the +5 V input. External 0.1 μF capacitors are required for the internal voltage converter.

The ADM202/ADM203 is a modification, enhancement and improvement to the AD230–AD241 family and derivatives thereof. It is essentially plug-in compatible and does not have materially different applications.

CIRCUIT DESCRIPTION

The internal circuitry consists of three main sections. These are

(a) A Charge Pump Voltage Converter

(b) RS-232 to TTL/CMOS Receivers

(c) TTL/CMOS to RS-232 Transmitters

Charge Pump DC-DC Voltage Converter

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a ±10 V supply from the input 5 V level. This is done in two stages using a switched capacitor technique as illustrated below. First, the 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The 10 V level is then inverted to generate −10 V using C2 as the storage element.

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors C1 and C2 may also be reduced at the expense of higher output impedance on the V+ and V− supplies. On the ADM203, all capacitors C1 to C4 are molded into the package.

The V+ and V− supplies may also be used to power external circuitry if the current requirements are small.

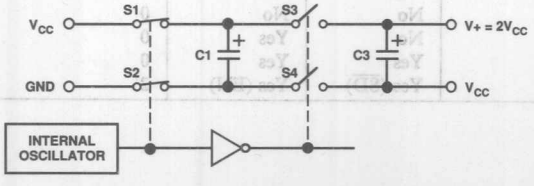


Figure 2. Charge Pump Voltage Doubler

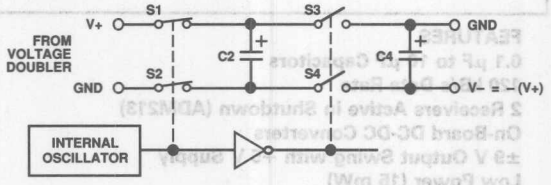


Figure 3. Charge Pump Voltage Inverter

Transmitter (Driver) Section

The drivers convert TTL/CMOS input levels into EIA-232-E output levels. With V_{CC} = +5 V and driving a typical EIA-232-E load, the output voltage swing is ±9 V. Even under worst case conditions the drivers are guaranteed to meet the ±5 V EIA-232-E minimum requirement.

The input threshold levels are both TTL and CMOS compatible with the switching threshold set at $V_{CC}/4$. With a nominal V_{CC} = 5 V the switching threshold is 1.25 V typical. Unused inputs may be left unconnected, as an internal 400 kΩ pull-up resistor pulls them high forcing the outputs into a low state.

As required by the EIA-232-E standard the slew rate is limited to less than 30 V/μs without the need for an external slew limiting capacitor and the output impedance in the power-off state is greater than 300 Ω.

Receiver Section

The receivers are inverting level shifters that accept EIA-232-E input levels (±5 V to ±15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum which are well within the ±3 V EIA-232 requirement. The low level threshold is deliberately positive as it ensures that an unconnected input will be interpreted as a low level.

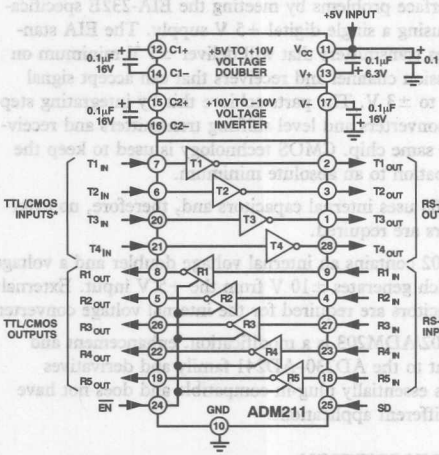
The receivers have Schmitt trigger input with a hysteresis level of 0.5 V. This ensures error free reception both for noisy inputs and for inputs with slow transition times.

15

FEATURES
- 0.1 μF to 10 μF Capacitors
- 120 kB/s Data Rate
- 2 Receivers Active in Shutdown (ADM213)
- On-Board DC-DC Converters
- ±9 V Output Swing with +5 V Supply
- Low Power (15 mW)
- Low Power Shutdown ≤5 μW
- ±30 V Receiver Input Levels
- Latch-Up FREE
- Plug-In Upgrade for MAX205-211/213

APPLICATIONS
- Computers
- Peripherals
- Modems
- Printers
- Instruments

TYPICAL OPERATING CIRCUIT



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**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

GENERAL DESCRIPTION

The ADM2xx family of line drivers/receivers is intended for all EIA-232-E and V.28 communications interfaces, especially in applications where ±12 V is not available. The ADM205, ADM206, ADM211 and ADM213 feature a low power shutdown mode which reduces power dissipation to less than 5 μW making them ideally suited for battery powered equipment. The ADM205 does not require any external components and is particularly useful in applications where printed circuit board space is critical. The ADM213 has an active-low shutdown and an active-high receiver enable control. Two receivers of the ADM213 remain active during shutdown. This feature is useful for ring indicator monitoring.

All members of the ADM2xx family, except the ADM209, include two internal charge pump voltage converters which allow operation from a single +5 V supply. These converters convert the +5 V input power to the ±10 V required for RS-232 output levels. The ADM209 is designed to operate from +5 V and +12 V supplies. An internal +12 V to −12 V charge pump voltage converter generates the −12 V supply.

Table I. Selection Table

Part Number	Power Supply Voltage	No. of RS-232 Drivers	No. of RS-232 Receivers	External Capacitors	Low Power Shutdown (SD)	TTL Three-State $\overline{EN}$	No. of Receivers Active in Shutdown
ADM205	+5 V	5	5	None	Yes	Yes	0
ADM206	+5 V	4	3	4	Yes	Yes	0
ADM207	+5 V	5	3	4	No	No	0
ADM208	+5 V	4	4	4	No	No	0
ADM209	+5 V & +9 V to +13.2 V	3	5	2	No	Yes	0
ADM211	+5 V	4	5	4	Yes	Yes	0
ADM213	+5 V	4	5	4	Yes ($\overline{SD}$)	Yes (EN)	2

SPECIFICATIONS

V_{CC} = +5 V ± 10% (206, 207, 208, 209, 211, 213); V_{CC} = +5 V ± 5% (ADM205); V+ = +9 V to +13.2 V (ADM209); C1–C4 = 0.1 µF Ceramic. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Output Voltage Swing	±5	±9		Volts	All Transmitter Outputs Loaded with 3 kΩ to Ground
V_{CC} Power Supply Current		3	7	mA	No Load, ADM206, ADM211, ADM213
		5	9	mA	No Load, ADM205, ADM207, ADM208
		0.4	1	mA	No Load, ADM209
V+ Power Supply Current		3.5	5	mA	No Load, V+ = 12 V ADM209 Only
Shutdown Supply Current		1	5	µA	
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$
Input Logic Threshold High, V_{INH}	2.0			V	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$
Logic Pull-Up Current		10	25	µA	T_{IN} = 0 V
RS-232 Input Voltage Range	−30		+30	V	
RS-232 Input Threshold Low	0.8	1.2		V	
RS-232 Input Threshold High		1.7	2.4	V	
RS-232 Input Hysteresis	0.2	0.5	1.0	V	
RS-232 Input Resistance	3	5	7	kΩ	
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 1.6 mA
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = −1.0 mA
TTL/CMOS Output Leakage Current		0.05	±5	µA	$\overline{EN}$ = V_{CC}, EN = 0 V, 0 V ≤ R_{OUT} ≤ V_{CC}
Output Enable Time (T_{EN})		115		ns	ADM205, ADM206, ADM209, ADM211 (Figure 25. C_L = 150 pF)
Output Disable Time (T_{DIS})		165		ns	ADM205, ADM206, ADM209, ADM211 (Figure 25. R_L = 1 kΩ)
Propagation Delay		0.5	5	µs	RS-232 to TTL
Instantaneous Slew Rate[1]		25	30	V/µs	C_L = 10 pF, R_L = 3-7 kΩ, T_A = +25°C
Transition Region Slew Rate	3	6		V/µs	R_L = 3 kΩ, C_L = 2500 pF Measured from +3 V to −3 V or −3 V to +3 V
Output Resistance	300			Ω	V_{CC} = V+ = V− = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±12	±60	mA	

NOTE
[1]Sample tested to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} . . . . . −0.3 V to +6 V
V+ . . . . . (V_{CC} − 0.3 V) to +14 V
V− . . . . . +0.3 V to −14 V
Input Voltages
  T_{IN} . . . . . −0.3 V to (V_{CC} + 0.3 V)
  R_{IN} . . . . . ±30 V
Output Voltages
  T_{OUT} . . . . . (V+, + 0.3 V) to (V−, − 0.3 V)
  R_{OUT} . . . . . −0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
  T_{OUT} . . . . . Continuous
Power Dissipation
  N-24 DIP (Derate 13.5 mW/°C above +70°C) . . . . 1000 mW
  N-24A DIP (Derate 13.5 mW/°C above +70°C) . . . 500 mW
  R-24 SOIC (Derate 12 mW/°C above +70°C) . . . . . 850 mW
  R-28 SOIC (Derate 12.5 mW/°C above +70°C) . . . . 900 mW
  RS-28 SSOP (Derate 10 mW/°C above +70°C) . . . . 900 mW
  Q-24 Cerdip (Derate 12.5 mW/°C above +70°C) . . 1000 mW
  D-24 Ceramic (Derate 20 mW/°C above +70°C) . . 1000 mW

Thermal Impedance, θ_{JA}
  N-24 DIP . . . . . 120°C/W
  N-24A DIP . . . . . 110°C/W
  R-24 SOIC . . . . . 85°C/W
  R-28 SOIC . . . . . 80°C/W
  RS-28 SSOP . . . . . 100°C/W
  Q-14 Cerdip . . . . . 105°C/W
  Q-16 Cerdip . . . . . 100°C/W
  Q-20 Cerdip . . . . . 100°C/W
  Q-24 Cerdip . . . . . 55°C/W
  D-24 Ceramic . . . . . 50°C/W
Operating Temperature Range
  Industrial (A Version) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature, Soldering . . . . . +300°C
  Vapour Phase (60 sec) . . . . . +215°C
  Infrared (15 sec) . . . . . +220°C
ESD Rating . . . . . > 2000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*	Model	Temperature Range	Package Option*	Model	Temperature Range	Package Option*
ADM205			**ADM206**			**ADM207**		
ADM205AN	−40°C to +85°C	N-24A	ADM206AN	−40°C to +85°C	N-24	ADM207AN	−40°C to +85°C	N-24
			ADM206AR	−40°C to +85°C	R-24	ADM207AR	−40°C to +85°C	R-24
			ADM206ARS	−40°C to +85°C	RS-24	ADM207ARS	−40°C to +85°C	RS-24
ADM208			**ADM209**			**ADM211**		
ADM208AN	−40°C to +85°C	N-24	ADM209AN	−40°C to +85°C	N-24	ADM211AR	−40°C to +85°C	R-28
ADM208AR	−40°C to +85°C	R-24	ADM209AR	−40°C to +85°C	R-24	ADM211ARS	−40°C to +85°C	RS-28
ADM208ARS	−40°C to +85°C	RS-24	ADM209ARS	−40°C to +85°C	RS-24			
ADM213								
ADM213AR	−40°C to +85°C	R-28						
ADM213ARS	−40°C to +85°C	RS-28						

*N = Plastic DIP; R = Small Outline IC (SOIC); RS = Small Shrink Outline Package (SSOP). For outline information see Package Information section.

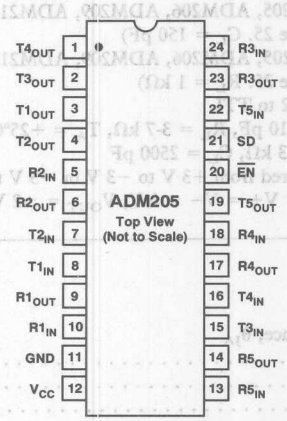

Figure 1. ADM205 DIP Pin Configuration

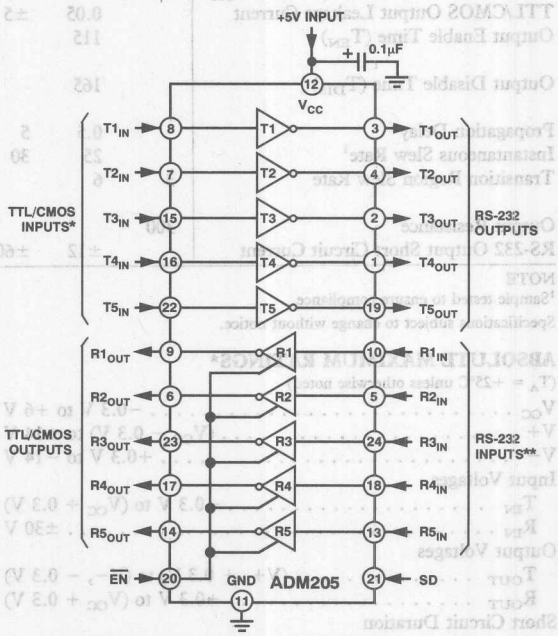

Figure 2. ADM205 Typical Operating Circuit

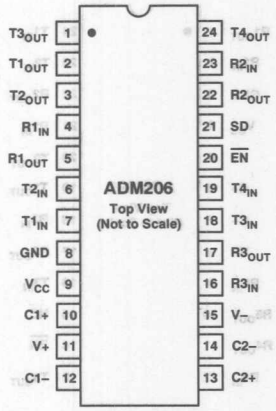

Figure 3. ADM206 DIP/SOIC/SSOP Pin Configuration

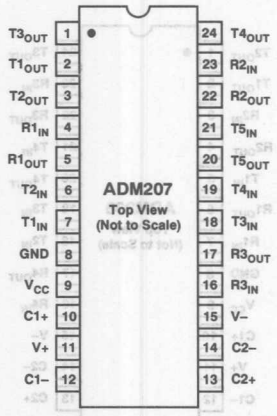

Figure 5. ADM207 DIP/SOIC/SSOP Pin Configuration

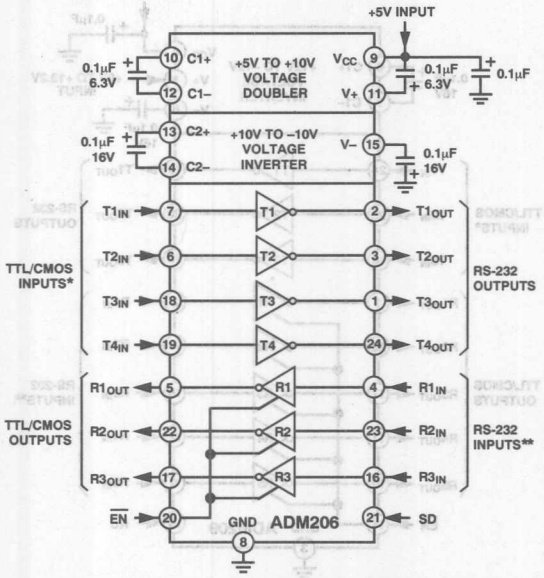

Figure 4. ADM206 Typical Operating Circuit

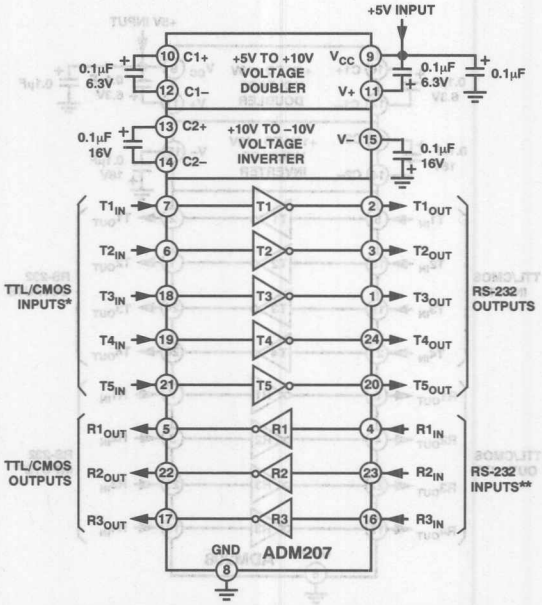

Figure 6. ADM207 Typical Operating Circuit

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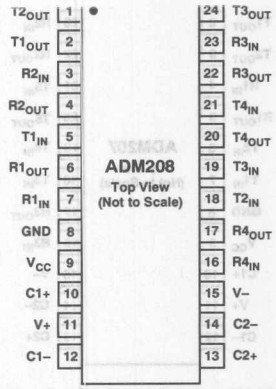


Figure 7. ADM208 DIP/SOIC/SSOP Pin Configuration

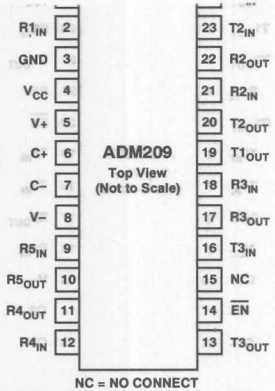
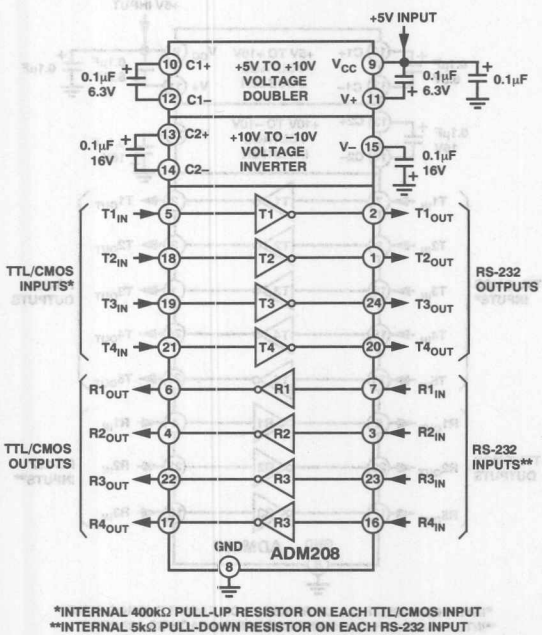
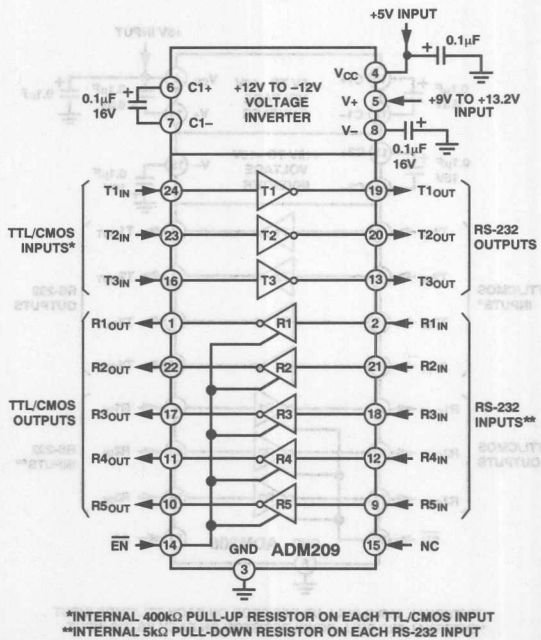


Figure 9. ADM209 DIP/SOIC/SSOP Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 8. ADM208 Typical Operating Circuit



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 10. ADM209 Typical Operating Circuit

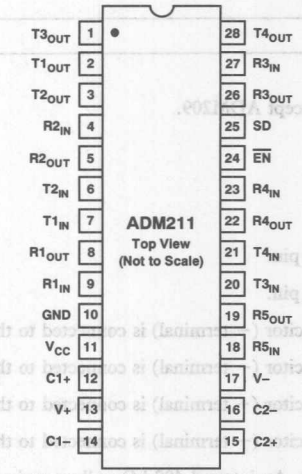


Figure 11. ADM211 SOIC/SSOP Pin Configuration

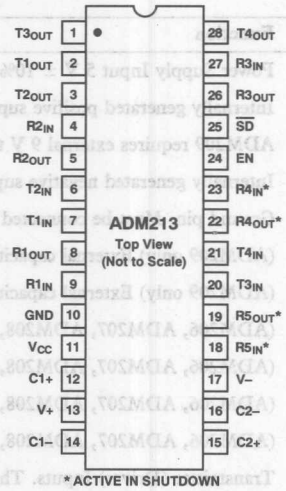


Figure 13. ADM213 SOIC/SSOP Pin Configuration

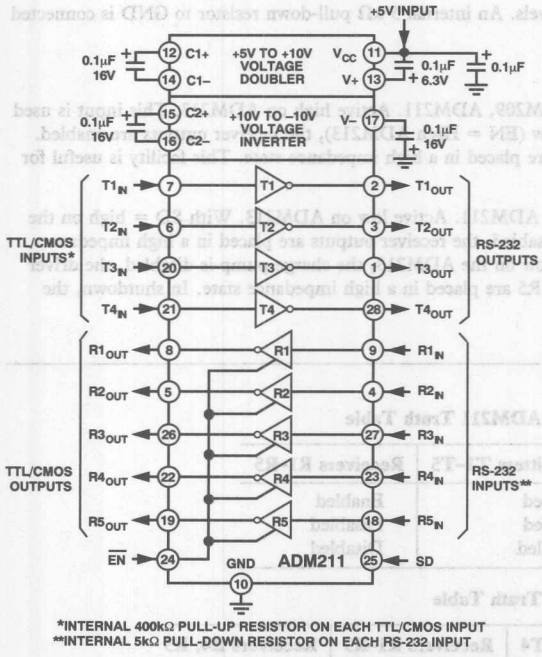


Figure 12. ADM211 Typical Operating Circuit

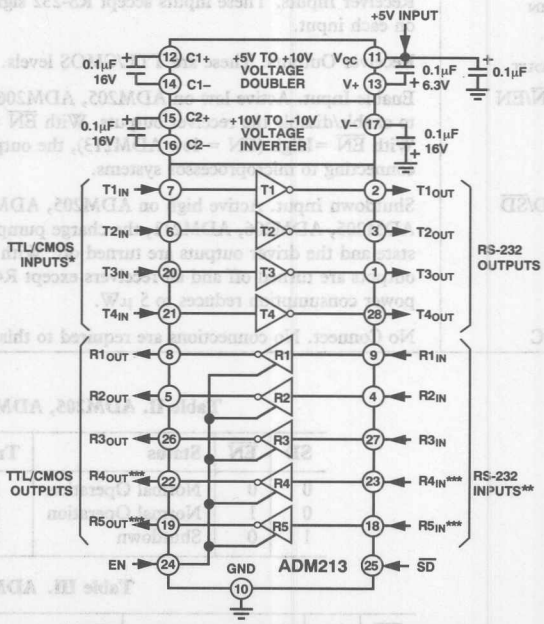


Figure 14. ADM213 Typical Operating Circuit

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PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power Supply Input 5 V ± 10% (+5 V ± 5% ADM205).
V+	Internally generated positive supply (+10 V nominal) on all parts except ADM209. ADM209 requires external 9 V to 13.2 V supply.
V−	Internally generated negative supply (−10 V nominal).
GND	Ground pin. Must be connected to 0 V.
C+	(ADM209 only) External capacitor (+ terminal) is connected to this pin.
C−	(ADM209 only) External capacitor (− terminal) is connected to this pin.
C1+	(ADM206, ADM207, ADM208, ADM211, ADM213) External capacitor (+ terminal) is connected to this pin.
C1−	(ADM206, ADM207, ADM208, ADM211, ADM213) External capacitor (− terminal) is connected to this pin.
C2+	(ADM206, ADM207, ADM208, ADM211, ADM213) External capacitor (+ terminal) is connected to this pin.
C2−	(ADM206, ADM207, ADM208, ADM211, ADM213) External capacitor (− terminal) is connected to this pin.
T_{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V_{CC} is connected on each input.
T_{OUT}	Transmitter (Driver) Outputs. These are RS-232 levels (typically ±10 V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$/EN	Enable Input. Active low on ADM205, ADM206, ADM209, ADM211. Active high on ADM213. This input is used to enable/disable the receiver outputs. With $\overline{EN}$ = Low (EN = High ADM213), the receiver outputs are enabled. With $\overline{EN}$ =High (EN = low ADM213), the outputs are placed in a high impedance state. This facility is useful for connecting to microprocessor systems.
SD/$\overline{SD}$	Shutdown Input. Active high on ADM205, ADM206, ADM211. Active low on ADM213. With SD = high on the ADM205, ADM206, ADM211, the charge pump is disabled, the receiver outputs are placed in a high impedance state and the driver outputs are turned off. With $\overline{SD}$ low on the ADM213, the charge pump is disabled, the driver outputs are turned off and all receivers except R4 and R5 are placed in a high impedance state. In shutdown, the power consumption reduces to 5 μW.
NC	No Connect. No connections are required to this pin.

Table II. ADM205, ADM206, ADM211 Truth Table

SD	$\overline{EN}$	Status	Transmitters T1–T5	Receivers R1–R5
0	0	Normal Operation	Enabled	Enabled
0	1	Normal Operation	Enabled	Disabled
1	0	Shutdown	Disabled	Disabled

Table III. ADM213 Truth Table

$\overline{SD}$	EN	Status	Transmitters T1–T4	Receivers R1–R3	Receivers R4, R5
0	0	Shutdown	Disabled	Disabled	Disabled
0	1	Shutdown	Disabled	Disabled	Enabled
1	0	Normal Operation	Enabled	Disabled	Disabled
1	1	Normal Operation	Enabled	Enabled	Enabled

Typical Performance Characteristics

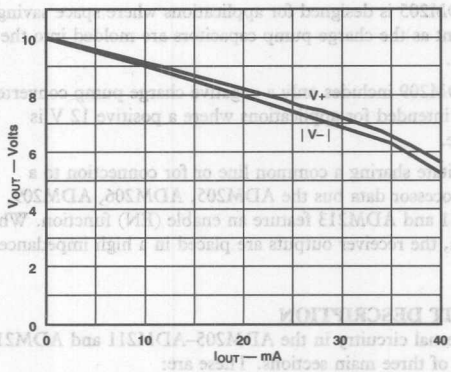

Figure 15. Charge Pump V+, V– vs. Current

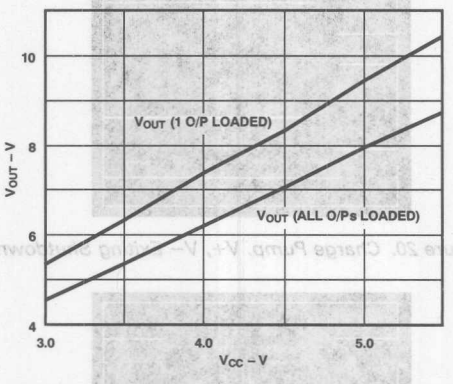

Figure 17. Transmitter Output Voltage vs. V_{CC}

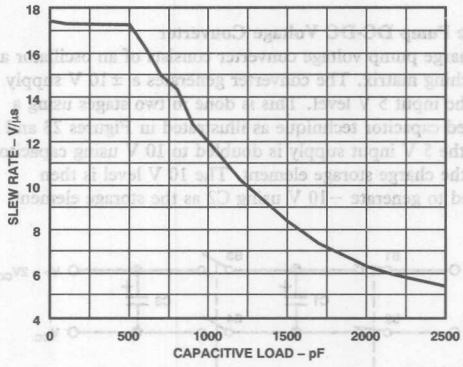

Figure 16. Transmitter Slew Rate vs. Load Capacitance

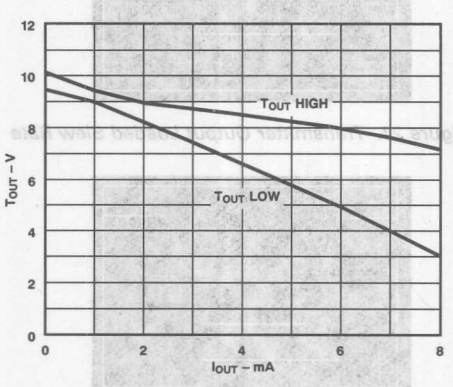

Figure 18. Transmitter Output Voltage vs. Current

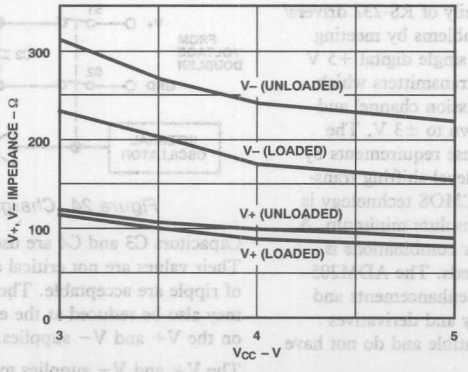

Figure 19. Charge Pump Impedance vs. V_{CC}

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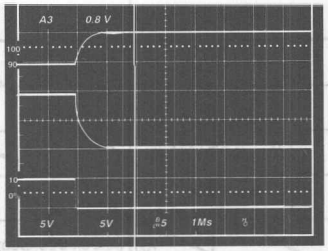


Figure 20. Charge Pump, V+, V− Exiting Shutdown

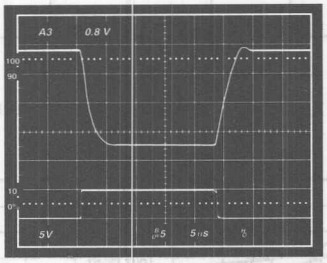


Figure 21. Transmitter Output Loaded Slew Rate

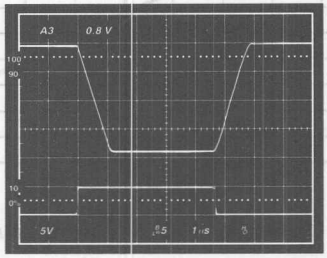


Figure 22. Transmitter Output Unloaded Slew Rate

GENERAL INFORMATION

The ADM205–ADM211 and ADM213 family of RS-232 drivers/receivers are designed to solve interface problems by meeting the EIA-232-E specifications while using a single digital +5 V supply. The EIA-232-E standard requires transmitters which will deliver ±5 V minimum on the transmission channel and receivers which can accept signal levels down to ±3 V. The ADM205–ADM211 and ADM213 meet these requirements by integrating step up voltage converters and level shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation to an absolute minimum. A comprehensive range of transmitter/receiver combinations is available to cover most communications needs. The ADM205–ADM211 and ADM213 are modifications, enhancements and improvements to the AD230–AD241 family and derivatives thereof. They are essentially plug-in compatible and do not have materially different applications.

The ADM205, ADM206, ADM211, and ADM213 are particularly useful in battery powered systems as they feature a low

than 5 µW.

The ADM205 is designed for applications where space saving is important as the charge pump capacitors are molded into the package.

The ADM209 includes only a negative charge pump converter and are intended for applications where a positive 12 V is available.

To facilitate sharing a common line or for connection to a microprocessor data bus the ADM205, ADM206, ADM209, ADM211 and ADM213 feature an enable ($\overline{EN}$) function. When disabled, the receiver outputs are placed in a high impedance state.

CIRCUIT DESCRIPTION

The internal circuitry in the ADM205–ADM211 and ADM213 consists of three main sections. These are:

(a) A charge pump voltage converter
(b) RS-232 to TTL/CMOS receivers
(c) TTL/CMOS to RS-232 transmitters

Charge Pump DC-DC Voltage Converter

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a ±10 V supply from the input 5 V level. This is done in two stages using a switched capacitor technique as illustrated in Figures 23 and 24. First, the 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The 10 V level is then inverted to generate −10 V using C2 as the storage element.

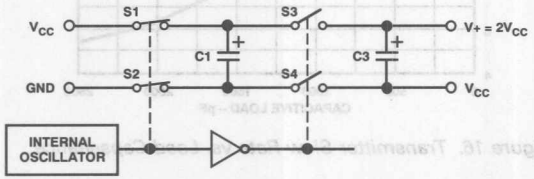


Figure 23. Charge-Pump Voltage Doubler

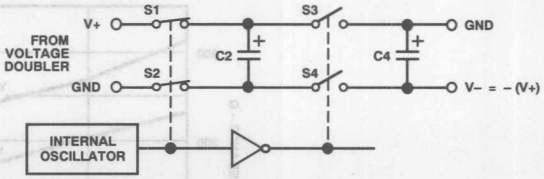


Figure 24. Charge-Pump Voltage Inverter

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors C1 and C2 may also be reduced at the expense of higher output impedance on the V+ and V− supplies.

The V+ and V− supplies may also be used to power external circuitry if the current requirements are small.

Transmitter (Driver) Section

The drivers convert TTL/CMOS input levels into EIA-232-E output levels. With V_{CC} = +5 V and driving a typical EIA-232-E load, the output voltage swing is ±9 V. Even under worst case conditions the drivers are guaranteed to meet the ±5 V EIA-232-E minimum requirement.

The input threshold levels are both TTL and CMOS compatible with the switching threshold set at $V_{CC}/4$. With a nominal V_{CC} = 5 V the switching threshold is 1.25 V typical. Unused inputs may be left unconnected, as an internal 400 kΩ pull-up resistor pulls them high forcing the outputs into a low state.

As required by the EIA-232-E standard, the slew rate is limited to less than 30 V/μs without the need for an external slew limiting capacitor and the output impedance in the power-off state is greater than 300 Ω.

Receiver Section

The receivers are inverting level shifters which accept EIA-232-E input levels (±5 V to ±15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum which are well within the ±3 V EIA-232-E requirement. The low level threshold is deliberately positive as it ensures that an unconnected input will be interpreted as a low level.

The receivers have Schmitt trigger inputs with a hysteresis level of 0.5 V. This ensures error-free reception for both noisy inputs and for inputs with slow transition times.

Shutdown (SD)

The ADM205, ADM206, ADM211 and ADM213 feature a control input which may be used to disable the part and reduce the power consumption to less than 5 μW. This is very useful in battery operated systems. During shutdown the charge pump is turned off, the transmitters are disabled and all receivers except R4 and R5 on the ADM213 are put into a high-impedance disabled state. Receivers R4 and R5 on the ADM213 remain enabled during shutdown. This feature allows monitoring external activity such as ring indicator monitoring while the device is in a low power shutdown mode. The shutdown control input is active high on all parts except the ADM213 where it is active low. Refer to Tables II and III.

Enable Input

The ADM205, ADM209, ADM211, and ADM213 feature an enable input used to enable or disable the receiver outputs. The enable input is active low on the ADM205, ADM209, ADM211 and active-high on the ADM213. Refer to Tables II and III. When disabled, all receiver outputs are placed in a high impedance state. This function allows the outputs to be connected directly to a microprocessor data bus. It can also be used to allow receivers from different devices to share a common data line. The timing diagram for the enable function is shown in Figure 25.

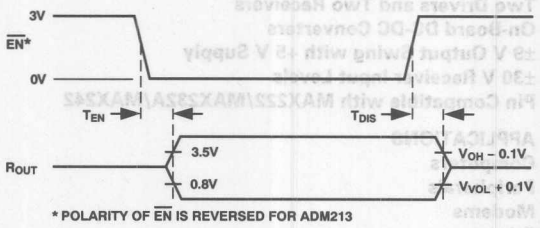


Figure 25. Enable Timing

APPLICATION HINTS

Driving Long Cables

In accordance with the EIA-232-E standard, long cables are permissible provided that the total load capacitance does not exceed 2500 pF. For longer cables which do exceed this, then it is possible to trade off baud rate vs. cable length. Large load capacitances cause a reduction in slew rate, and hence the maximum transmission baud rate is decreased. The ADM205–ADM211 and ADM213 are designed so that the slew rate reduction with increasing load capacitance is minimized.

For the receivers, it is important that a high level of noise immunity be inbuilt so that slow rise and fall times do not cause multiple output transitions as the signal passes slowly through the transition region. The ADM205–ADM211 and ADM213 have 0.5 V of hysteresis to guard against this. This ensures that, even in noisy environments, error-free reception can be achieved.

High Baud Rate Operation

The ADM205–ADM211 and ADM213 feature high slew rates permitting data transmission at rates well in excess of the EIA-232-E specification. The drivers maintain ±5 V signal levels at data rates up to 120-kB/s under worst-case loading conditions.

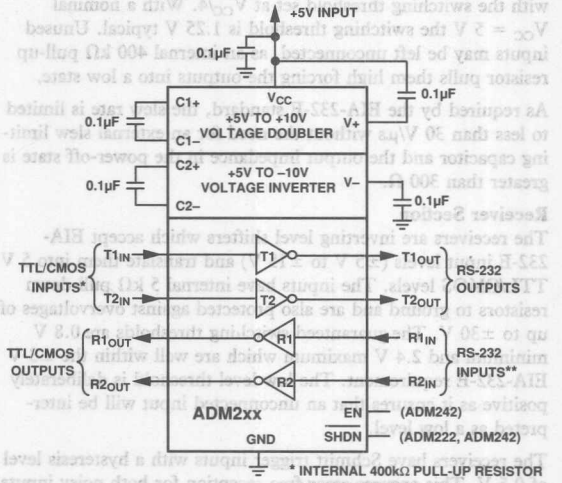
High Speed, +5 V, 0.1 µF CMOS RS-232 Drivers/Receivers

ADM222/ADM232A/ADM242*

FEATURES
200 kB/s Transmission Rate
Small (0.1 µF) Charge Pump Capacitors
Single 5 V Power Supply
Meets All EIA-232-E and V.28 Specifications
Two Drivers and Two Receivers
On-Board DC-DC Converters
±9 V Output Swing with +5 V Supply
±30 V Receiver Input Levels
Pin Compatible with MAX222/MAX232A/MAX242

APPLICATIONS
Computers
Peripherals
Modems
Printers
Instruments

FUNCTIONAL BLOCK DIAGRAM



* INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/MOS INPUT

** INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

GENERAL DESCRIPTION

The ADM222, ADM232A, ADM242 are a family of high speed RS-232 line drivers/receivers offering transmission rates up to 200 kB/s. Operating from a single +5 V power supply, a highly efficient on-chip charge pump using small (0.1 µF) external capacitors allows RS-232 bipolar levels to be developed. Two RS-232 drivers and two RS-232 receivers are provided on each device.

The devices are fabricated on BiCMOS, an advanced mixed technology process which combines low power CMOS with high speed bipolar circuitry. This allows for transmission rates up to 200 kB/s yet minimizes the quiescent power supply current to under 5 mA.

The ADM232A is a pin-compatible, high speed upgrade for the AD232 and for the ADM232L. It is available in 16-pin DIP and in both narrow and wide surface mount (SOIC) packages.

The ADM222 contains an additional shutdown ($\overline{\text{SHDN}}$) function which may be used to disable the device thereby reducing the supply current to 0.1 µA. During shutdown, all transmit/receive functions are disabled. The ADM222 is available in 18-pin DIP and in a wide surface mount (SOIC) package.

The ADM242 combines both shutdown ($\overline{\text{SHDN}}$) and enable ($\overline{\text{EN}}$) functions. The shutdown function reduces the supply curent to 0.1 mA. During shutdown, the transmitters are disabled but the receivers continue to operate normally. The enable function allows the receiver outputs to be disabled thereby facilitating sharing a common bus. The ADM242 is available in 18-pin DIP and in a wide surface mount (SOIC) package.

***Protected by U.S. Patent No. 5,237,209.**

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM222AN	–40°C to +85°C	N-18
ADM222AR	–40°C to +85°C	R-18W
ADM232AAN	–40°C to +85°C	N-16
ADM232AARN	–40°C to +85°C	R-16N
ADM232AARW	–40°C to +85°C	R-16W
ADM242AN	–40°C to +85°C	N-18
ADM242AR	–40°C to +85°C	R-18W

*For outline information see Package Information section.

SPECIFICATIONS (V_{CC} = +5 V ± 10%, C1–C4 = 0.1 µF; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
RS-232 TRANSMITTERS					
Output Voltage Swing	±5	±9		V	All Transmitter Outputs Loaded with 3 kΩ to Ground
Input Logic Threshold Low, V_{INL}		1.4	0.8	V	T_{IN}
Input Logic Threshold High, V_{INH}	2.0	1.4		V	T_{IN}
Logic Pullup Current		5	40	µA	T_{IN} = 0 V
Data Rate	200			kB/s	
Output Resistance	300			Ω	V_{CC} = V+ = V– = 0 V, V_{OUT} = ±2 V
Output Short Circuit Current (Instantaneous)	±7	±22		mA	
RS-232 RECEIVERS					
RS-232 Input Voltage Range	–30		+30	V	
RS-232 Input Threshold Low	0.8	1.3		V	
RS-232 Input Threshold High		1.8	2.4	V	
RS-232 Input Hysteresis	0.2	0.5	1.0	V	V_{CC} = 5 V
RS-232 Input Resistance	3	5	7	kΩ	
TTL/CMOS Output Voltage Low, V_{OL}		0.2	0.4	V	I_{OUT} = 3.2 mA
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = –1.0 mA
TTL/CMOS Output Short-Circuit Current	–2	–10		mA	Source Current (V_{OUT} = GND)
TTL/CMOS Output Short-Circuit Current	10	30		mA	Sink Current (V_{OUT} = V_{CC})
TTL/CMOS Output Leakage Current		±0.05	±10	µA	$\overline{SHDN}$ = GND/$\overline{EN}$ = V_{CC} 0 V ≤ V_{OUT} ≤ V_{CC}
$\overline{EN}$ Input Threshold Low, V_{INL}		1.4	0.8	V	
$\overline{EN}$ Input Threshold High, V_{INH}	2.0	1.4		V	
POWER SUPPLY					
Power Supply Current		4	8	mA	No Load
		15		mA	3 kΩ Load on Both Outputs
Shutdown Power Supply Current		0.1	10	µA	
$\overline{SHDN}$ Input Leakage Current			±1	µA	
$\overline{SHDN}$ Input Threshold Low, V_{INL}		1.4	0.8	V	
$\overline{SHDN}$ Input Threshold High, V_{INH}	2.0	1.4		V	
AC CHARACTERISTICS					
Transition Region Slew Rate	6	12	30	V/µs	C_L = 50 pF to 2500 pF, R_L = 3 kΩ to 7 kΩ Measured from +3 V to –3 V or –3 V to +3 V
Transmitter Propagation Delay TTL to RS-232		0.7	3.5	µs	t_{PHLT}
		0.7	3.5	µs	t_{PLHT}
Receiver Propagation Delay RS-232 to TTL		0.2	0.5	µs	t_{PHLR}
		0.3	0.5	µs	t_{PLHR}
Receiver Output Enable Time		125	500	ns	t_{ER}
Receiver Output Disable Time		160	500	ns	t_{DR}
Transmitter Output Enable Time		250		µs	$\overline{SHDN}$ Goes high
Transmitter Output Disable Time		3.5		µs	$\overline{SHDN}$ Goes low
Transmitter + to – Propagation Delay Difference		300		ns	
Receiver + to – Propagation Delay Difference		100		ns	

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} ..... +6 V
V+ ..... (V_{CC} – 0.3 V) to +13 V
V– ..... +0.3 V to –13 V
Input Voltages
T_{IN} ..... –0.3 V to (V_{CC} + 0.3 V)
R_{IN} ..... ±30 V
Output Voltages
T_{OUT} ..... (V+, +0.3 V) to (V–, –0.3 V)
R_{OUT} ..... –0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
T_{OUT} ..... Continuous
Power Dissipation N-16 ..... 400 mW
(Derate 7.5 mW/°C above +70°C)
θ_{JA}, Thermal Impedance ..... 80°C/W
Power Dissipation R-16N ..... 400 mW
(Derate 7 mW/°C above +70°C)
θ_{JA}, Thermal Impedance ..... 80°C/W
Power Dissipation R-16W ..... 400 mW
(Derate 7 mW/°C above +70°C)
θ_{JA}, Thermal Impedance ..... 80°C/W
Power Dissipation N-18 ..... 400 mW
(Derate 7 mW/°C above +70°C)
θ_{JA}, Thermal Impedance ..... 80°C/W
Power Dissipation R-18W ..... 400 mW
(Derate 7 mW/°C above +70°C)
θ_{JA}, Thermal Impedance ..... 80°C/W
Operating Temperature Range
Industrial (A Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Test Circuits

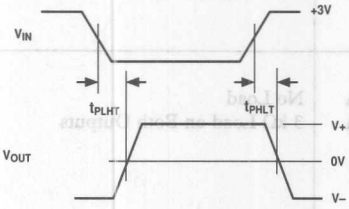


Figure 1. Transmitter Propagation Delay Timing

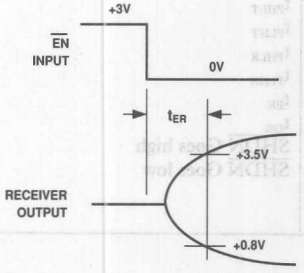


Figure 2. Receiver Enable Timing

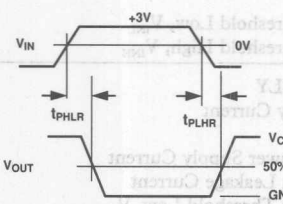


Figure 3. Receiver Propagation Delay Timing

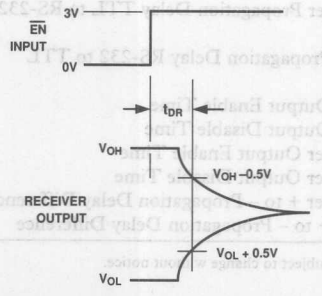


Figure 4. Receiver Disable Timing

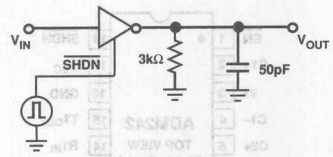


Figure 5. Shutdown Test Circuit

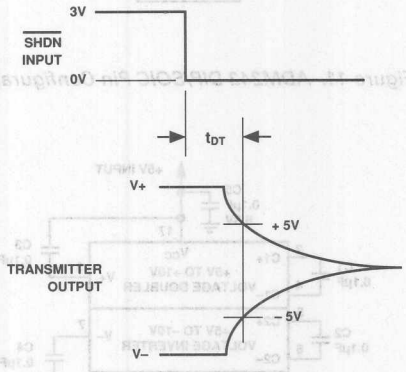


Figure 6. Transmitter Shutdown Disable Timing

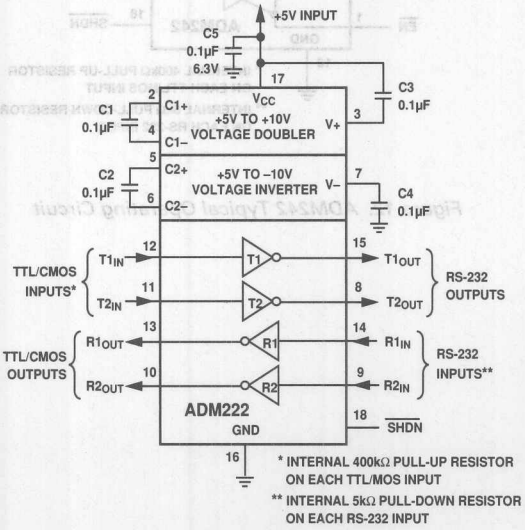


Figure 7. ADM222 Typical Operating Circuit

PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power Supply Input, +5 V ± 10%.
V+	Internally generated positive supply (+10 V nominal).
V–	Internally generated negative supply (–10 V nominal).
GND	Ground Pin. Must be connected to 0 V.
C1+	External capacitor 1, (+ terminal) is connected to this pin.
C1–	External capacitor 1, (– terminal) is connected to this pin.
C2+	External capacitor 2, (+ terminal) is connected to this pin.
C2–	External capacitor 2, (– terminal) is connected to this pin.
T_{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V_{CC} is connected on each input.
T_{OUT}	Transmitter (Driver) Outputs. These are RS-232 levels (typically ±9 V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each of these inputs.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
NC	No Connect. No connections are required to this pin.
$\overline{EN}$	(ADM242 Only) Active Low Digital Input. May be used to enable or disable (three-state) both receiver outputs.
$\overline{SHDN}$	(ADM222 & ADM242) Active Low Digital Input. May be used to disable the device so that the power consumption is minimized. On the ADM222 all drivers and receivers are disabled. On the ADM242 the drivers are disabled but the receivers remain enabled.

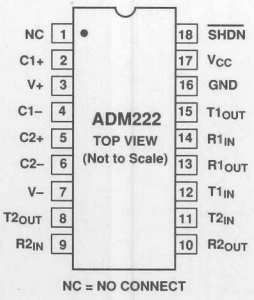


Figure 8. ADM222 DIP & SOIC Pin Configurations

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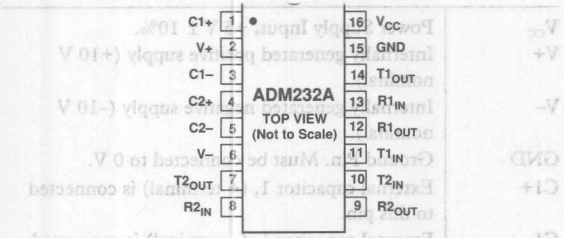


Figure 9. ADM232A DIP/SOIC Pin Configuration

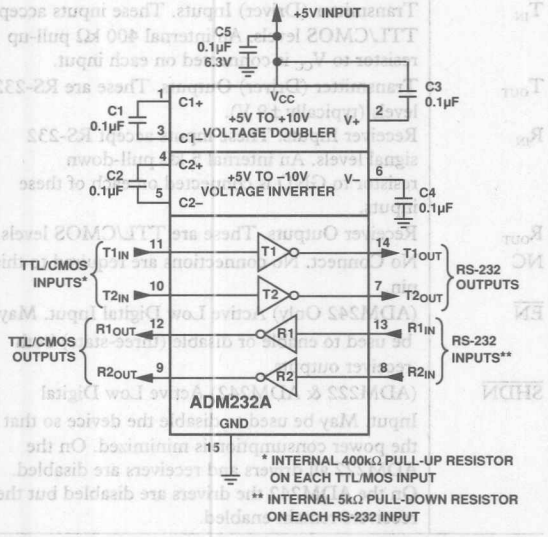


Figure 10. ADM232A Typical Operating Circuit

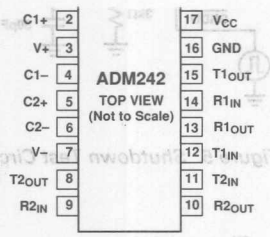


Figure 11. ADM242 DIP/SOIC Pin Configuration

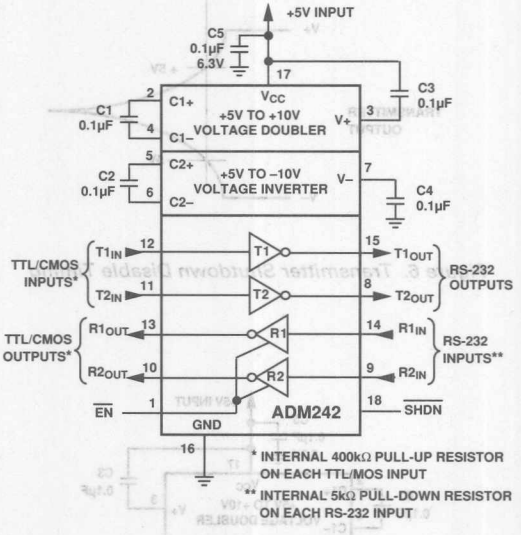


Figure 12. ADM242 Typical Operating Circuit

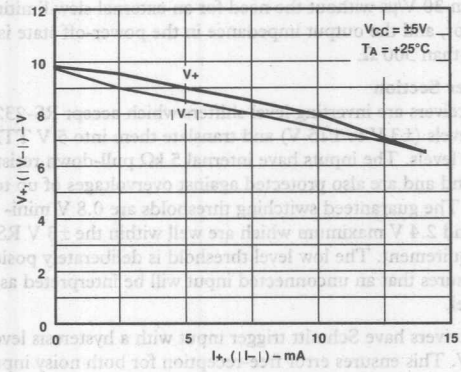


Figure 13. Charge Pump V+, V– vs. Current

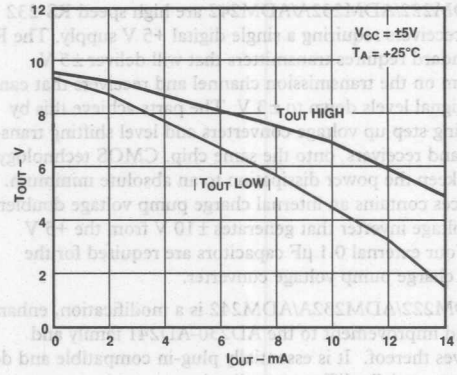


Figure 16. Transmitter Output Voltage vs. Current

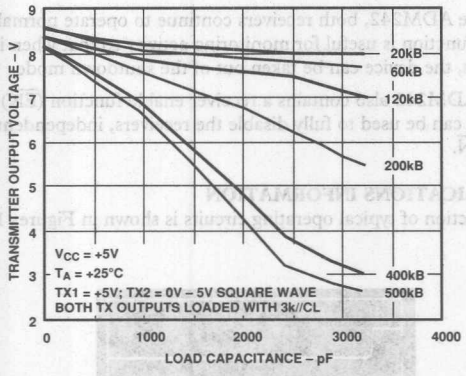


Figure 14. Transmitter Baud Rate vs. Load Capacitance

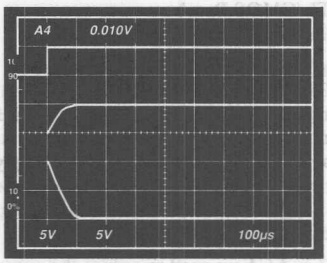


Figure 17. Charge Pump V+, V– Exiting Shutdown

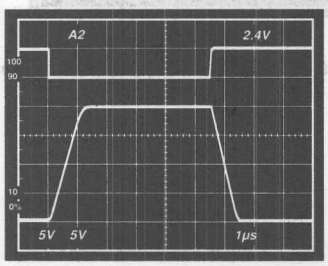


Figure 15. Transmitter Unloaded Slew Rate

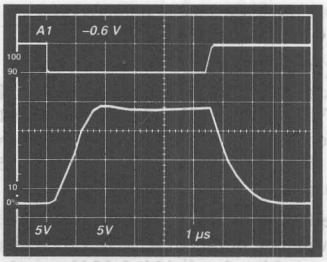


Figure 18. Transmitter Fully Loaded Slew Rate

15

GENERAL INFORMATION

The ADM222/ADM232A/ADM242 are high speed RS-232 drivers/receivers requiring a single digital +5 V supply. The RS-232 standard requires transmitters that will deliver ±5 V minimum on the transmission channel and receivers that can accept signal levels down to ±3 V. The parts achieve this by integrating step up voltage converters and level shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation to an absolute minimum. All devices contains an internal charge pump voltage doubler and a voltage inverter that generates ±10 V from the +5 V input. Four external 0.1 µF capacitors are required for the internal charge pump voltage converter.

The ADM222/ADM232A/ADM242 is a modification, enhancement and improvement to the AD230-AD241 family and derivatives thereof. It is essentially plug-in compatible and does not have materially different applications.

CIRCUIT DESCRIPTION

The internal circuitry consists of four main sections. These are:

A Charge Pump Voltage Converter
TTL/CMOS to RS-232 Transmitters
RS-232 to TTL/CMOS Receivers
Enable and Shutdown Functions.

Charge Pump DC-DC Voltage Converter

The Charge Pump Voltage converter consists of an oscillator and a switching matrix. The converter generates a ±10 V supply from the input 5 V level. This is done in two stages using a switched capacitor technique. The 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The –10 V level is also generated from the input 5 V supply using C1 and C2 as the storage elements.

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors C1 and C2 may also be reduced at the expense of higher output impedance on the V+ and V– supplies.

The V+ and V– supplies may also be used to power external circuitry if the current requirements are small. Please refer to the typical performance characteristics which shows the V+, V– output voltage vs. current.

In the shutdown mode the charge pump is disabled and V+ decays to V_{CC} while V– decays to 0 V.

Transmitter (Driver) Section

The Drivers convert TTL/CMOS input levels into RS-232 output levels. With V_{CC} = +5 V and driving a typical RS-232 load, the output voltage swing is ±9 V. Even under worst case conditions the drivers are guaranteed to meet the ±5 V RS-232 minimum requirement.

The input threshold levels are both TTL and CMOS compatible with the switching threshold set at $V_{CC}/4$. With a nominal V_{CC} = 5 V the switching threshold is 1.25 V typical. Unused inputs may be left unconnected, as an internal 400 kΩ pull- up resistor pulls them high forcing the outputs into a low state.

As required by the RS-232 standard, the slew rate is limited to less than 30 V/µs without the need for an external slew limiting capacitor, and the output impedance in the power-off state is greater than 300 Ω.

Receiver Section

The receivers are inverting level shifters which accept RS-232 input levels (±3 V to ±15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum which are well within the ±3 V RS-232 requirement. The low level threshold is deliberately positive as it ensures that an unconnected input will be interpreted as a low level.

The receivers have Schmitt trigger input with a hysteresis level of 0.5 V. This ensures error free-reception for both noisy inputs and for inputs with slow transition times

Enable and Shutdown Functions

On the ADM222, both receivers are fully disabled during shutdown.

On the ADM242, both receivers continue to operate normally. This function is useful for monitoring activity so that when it occurs, the device can be taken out of the shutdown mode.

The ADM242 also contains a receiver enable function ($\overline{EN}$) which can be used to fully disable the receivers, independent of $\overline{SHDN}$.

APPLICATIONS INFORMATION

A selection of typical operating circuits is shown in Figures 13 to 19.

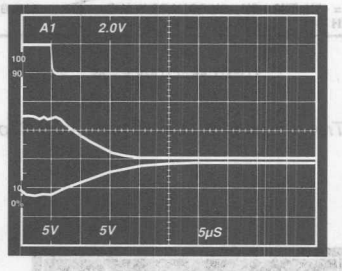


Figure 19. Transmitter Output Disable Timing

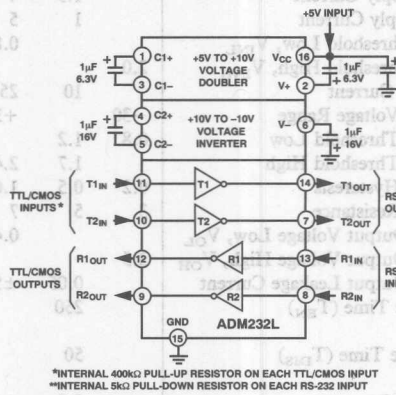
+5 V Powered CMOS RS-232 Drivers/Receivers

ADM223/ADM230L–ADM241L

FEATURES
- Single 5 V Power Supply
- Meets All EIA-232-E and V.28 Specifications
- 120 kB/s Data Rate
- On-Board DC-DC Converters
- ±9 V Output Swing with +5 V Supply
- Small 1 μF Capacitors
- Low Power Shutdown ≤1 μA
- Receivers Active in Shutdown (ADM223)
- ESD > 2 kV
- ±30 V Receiver Input Levels
- Latch-Up FREE
- Plug-In Upgrade for MAX223/230-241
- Plug-In Upgrade for AD230–AD241

APPLICATIONS
- Computers
- Peripherals
- Modems
- Printers
- Instruments

ADM232L TYPICAL OPERATING CIRCUIT



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

GENERAL DESCRIPTION

The ADM2xx family of line drivers/receivers is intended for all EIA-232-E and V.28 communications interfaces, especially in applications where ±12 V is not available. The ADM223, ADM230L, ADM235L, ADM236L and ADM241L feature a low power shutdown mode which reduces power dissipation to less than 5 μW making them ideally suited for battery powered equipment. Two receivers remain enabled during shutdown on the ADM223. The ADM233L and ADM235L do not require any external components and are particularly useful in applications where printed circuit board space is critical.

All members of the ADM230L family, except the ADM231L and the ADM239L, include two internal charge pump voltage converters which allow operation from a single +5 V supply. These converters convert the +5 V input power to the ±10 V required for RS-232 output levels. The ADM231L and ADM239L are designed to operate from +5 V and +12 V supplies. An internal +12 V to −12 V charge pump voltage converter generates the −12 V supply.

The ADM2xxL is an enhanced upgrade for the AD2xx family featuring lower power consumption, faster slew rate and operation with smaller (1 μF) capacitors.

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Table I. Selection Table

Part Number	Power Supply Voltage	No. of RS-232 Drivers	No. of RS-232 Receivers	External Capacitors	Low Power Shutdown (SD)	TTL Three-State $\overline{EN}$	No. of Pins
ADM223	+5 V	4	5	4	Yes ($\overline{SD}$)	Yes ($\overline{EN}$)	28
ADM230L	+5 V	5	0	4	Yes	No	20
ADM231L	+5 V & +7.5 V to +13.2 V	2	2	2	No	No	14
ADM232L	+5 V	2	2	4	No	No	16
ADM233L	+5 V	2	2	None	No	No	20
ADM234L	+5 V	4	0	4	No	No	16
ADM235L	+5 V	5	5	None	Yes	Yes	24
ADM236L	+5 V	4	3	4	Yes	Yes	24
ADM237L	+5 V	5	3	4	No	No	24
ADM238L	+5 V	4	4	4	No	No	24
ADM239L	+5 V & +7.5 V to +13.2 V	3	5	2	No	Yes	24
ADM241L	+5 V	4	5	4	Yes	Yes	28

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Output Voltage Swing	±5	±9		Volts	All Transmitter Outputs Loaded with 3 kΩ to Ground
V_{CC} Power Supply Current		2	3.0	mA	No Load, All T_{INS} = V_{CC} (except ADM223)
		3.5	6	mA	No Load, All T_{INS} = GND
		0.4	1	mA	ADM231L, ADM239L
V+ Power Supply Current		1.5	4	mA	No Load, V+ = 12 V ADM231L & ADM239L Only
Shutdown Supply Current		1	5	μA	
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$
Input Logic Threshold High, V_{INH}	2.0			V	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$
Logic Pull-Up Current		10	25	μA	T_{IN} = 0 V
RS-232 Input Voltage Range	−30		+30	V	
RS-232 Input Threshold Low	0.8	1.2		V	
RS-232 Input Threshold High		1.7	2.4	V	
RS-232 Input Hysteresis	0.2	0.5	1.0	V	
RS-232 Input Resistance	3	5	7	kΩ	
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = −1.0 mA
TTL/CMOS Output Leakage Current		0.05	±5	μA	$\overline{EN}$ = V_{CC}, 0 V ≤ R_{OUT} ≤ V_{CC}
Output Enable Time (T_{EN})		250		ns	ADM223, ADM235L, ADM236L, ADM239L, ADM241L (Figure 25. C_L = 150 pF)
Output Disable Time (T_{DIS})		50		ns	ADM223, ADM235L, ADM236L, ADM239L, ADM241L (Figure 25. R_L = 1 kΩ)
Propagation Delay		0.5		μs	RS-232 to TTL
Instantaneous Slew Rate[1]		25	30	V/μs	C_L = 10 pF, R_L = 3-7 kΩ, T_A = +25°C
Transition Region Slew Rate		5		V/μs	R_L = 3 kΩ, C_L = 2500 pF Measured from +3 V to −3 V or −3 V to +3 V
Output Resistance	300			Ω	V_{CC} = V+ = V− = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±10		mA	

NOTE
[1]Sample tested to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{CC} . . . . . −0.3 V to +6 V
V+ . . . . . (V_{CC} − 0.3 V) to +14 V
V− . . . . . +0.3 V to −14 V
Input Voltages
T_{IN} . . . . . −0.3 V to (V_{CC} + 0.3 V)
R_{IN} . . . . . ±30 V
Output Voltages
T_{OUT} . . . . . (V+, + 0.3 V) to (V−, − 0.3 V)
R_{OUT} . . . . . −0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
T_{OUT} . . . . . Continuous
Power Dissipation
N-14 DIP (Derate 10 mW/°C above +70°C) . . . . . 800 mW
N-16 DIP (Derate 10.5 mW/°C above +70°C) . . . . 840 mW
N-20 DIP (Derate 11 mW/°C above +70°C) . . . . . 890 mW
N-24 DIP (Derate 13.5 mW/°C above +70°C) . . . . 1000 mW
N-24A DIP (Derate 13.5 mW/°C above +70°C) . . . 500 mW
R-16 SOIC (Derate 9 mW/°C above +70°C) . . . . . 760 mW
R-20 SOIC (Derate 9.5 mW/°C above +70°C) . . . . 800 mW
R-24 SOIC (Derate 12 mW/°C above +70°C) . . . . . 850 mW
R-28 SOIC (Derate 12.5 mW/°C above +70°C) . . . . 900 mW
RS-28 SSOP (Derate 10 mW/°C above +70°C) . . . . 900 mW
Q-14 Cerdip (Derate 10 mW/°C above +70°C) . . . . 720 mW
Q-16 Cerdip (Derate 10 mW/°C above +70°C) . . . . 800 mW
Q-20 Cerdip (Derate 11.2 mW/°C above +70°C) . . . 890 mW
Q-24 Cerdip (Derate 12.5 mW/°C above +70°C) . . 1000 mW
D-24 Ceramic (Derate 20 mW/°C above +70°C) . . 1000 mW

Thermal Impedance, θ_{JA}
N-14 DIP . . . . . 140°C/W
N-16 DIP . . . . . 135°C/W
N-20 DIP . . . . . 125°C/W
N-24 DIP . . . . . 120°C/W
N-24A DIP . . . . . 110°C/W
R-16 SOIC . . . . . 105°C/W
R-20 SOIC . . . . . 105°C/W
R-24 SOIC . . . . . 85°C/W
R-28 SOIC . . . . . 80°C/W
RS-28 SSOP . . . . . 100°C/W
Q-14 Cerdip . . . . . 105°C/W
Q-16 Cerdip . . . . . 100°C/W
Q-20 Cerdip . . . . . 100°C/W
Q-24 Cerdip . . . . . 55°C/W
D-24 Ceramic . . . . . 50°C/W
Operating Temperature Range
Commercial (J Version) . . . . . 0 to +70°C
Industrial (A Version) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature, Soldering . . . . . +300°C
Vapour Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
ESD Rating . . . . . >2000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Model	Temperature Range	Package Option*	Model	Temperature Range	Package Option*	Model	Temperature Range	Package Option*
ADM223			**ADM230L**			**ADM231L**		
ADM223AR	−40°C to +85°C	R-28	ADM230LJN	0°C to +70°C	N-20	ADM231LJN	0°C to +70°C	N-14
ADM223ARS	−40°C to +85°C	RS-28	ADM230LJR	0°C to +70°C	R-20	ADM231LJR	0°C to +70°C	R-16
			ADM230LAN	−40°C to +85°C	N-20	ADM231LAN	−40°C to +85°C	N-14
			ADM230LAR	−40°C to +85°C	R-20	ADM231LAR	−40°C to +85°C	R-16
			ADM230LAQ	−40°C to +85°C	Q-20	ADM231LAQ	−40°C to +85°C	Q-14
ADM232L			**ADM233L**			**ADM234L**		
ADM232LJN	0°C to +70°C	N-16	ADM233LJN	0°C to +70°C	N-20	ADM234LJN	0°C to +70°C	N-16
ADM232LJR	0°C to +70°C	R-16	ADM233LAN	−40°C to +85°C	N-20	ADM234LJR	0°C to +70°C	R-16
ADM232LAN	−40°C to +85°C	N-16				ADM234LAN	−40°C to +85°C	N-16
ADM232LAR	−40°C to +85°C	R-16				ADM234LAR	−40°C to +85°C	R-16
ADM232LAQ	−40°C to +85°C	Q-16				ADM234LAQ	−40°C to +85°C	Q-16
ADM235L			**ADM236L**			**ADM237L**		
ADM235LJN	0°C to +70°C	N-24A	ADM236LJN	0°C to +70°C	N-24	ADM237LJN	0°C to +70°C	N-24
ADM235LAN	−40°C to +85°C	N-24A	ADM236LJR	0°C to +70°C	R-24	ADM237LJR	0°C to +70°C	R-24
ADM235LAQ	−40°C to +85°C	D-24	ADM236LAN	−40°C to +85°C	N-24	ADM237LAN	−40°C to +85°C	N-24
			ADM236LAR	−40°C to +85°C	R-24	ADM237LAR	−40°C to +85°C	R-24
			ADM236LAQ	−40°C to +85°C	Q-24	ADM237LAQ	−40°C to +85°C	Q-24
ADM238L			**ADM239L**			**ADM241L**		
ADM238LJN	0°C to +70°C	N-24	ADM239LJN	0°C to +70°C	N-24	ADM241LJR	0°C to +70°C	R-28
ADM238LJR	0°C to +70°C	R-24	ADM239LJR	0°C to +70°C	R-24	ADM241LAR	−40°C to +85°C	R-28
ADM238LAN	−40°C to +85°C	N-24	ADM239LAN	−40°C to +85°C	N-24	ADM241LJRS	0°C to +70°C	RS-28
ADM238LAR	−40°C to +85°C	R-24	ADM239LAR	−40°C to +85°C	R-24	ADM241LARS	−40°C to +85°C	RS-28
ADM238LAQ	−40°C to +85°C	Q-24	ADM239LAQ	−40°C to +85°C	Q-24			

*D = Ceramic DIP; N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC); RS = Small Shrink Outline Package (SSOP).

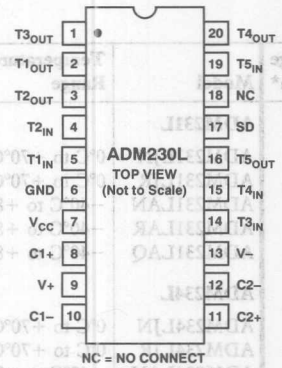


Figure 1. ADM230L DIP/SOIC Pin Configuration

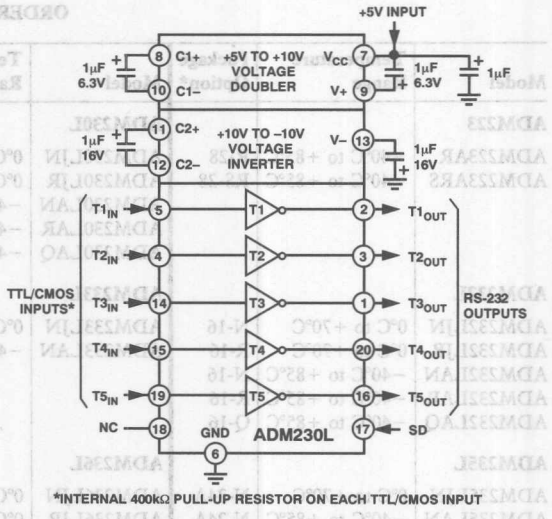
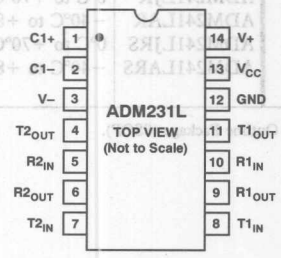


Figure 2. ADM230L Typical Operating Circuit

DIP



SOIC

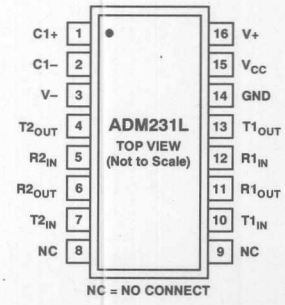


Figure 3. ADM231L DIP & SOIC Pin Configurations

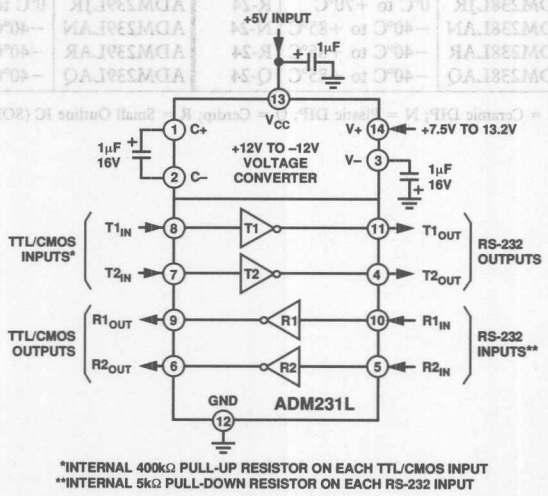


Figure 4. ADM231L Typical Operating Circuit (DIP Pinout)

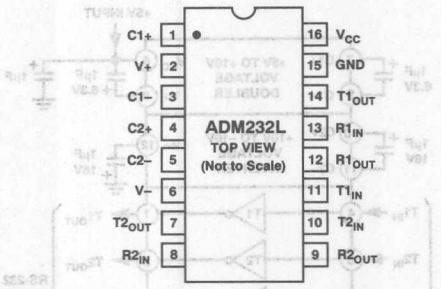
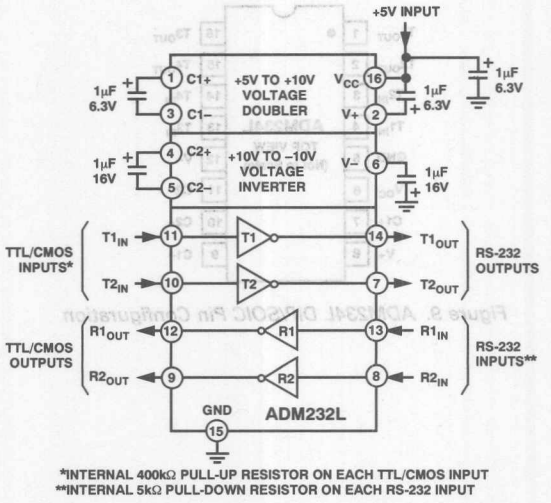


Figure 5. ADM232L DIP/SOIC Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 6. ADM232L Typical Operating Circuit

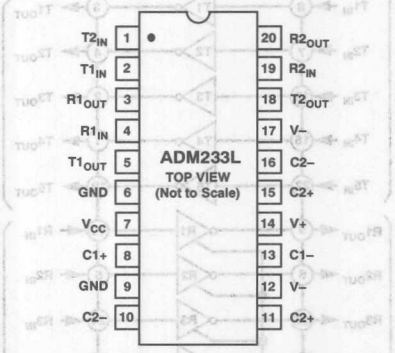
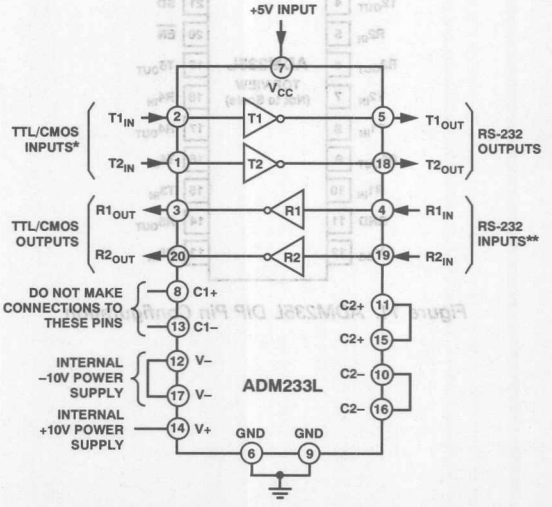


Figure 7. ADM233L DIP Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 8. ADM233L Typical Operating Circuit

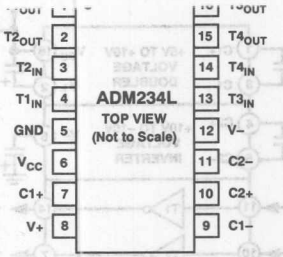


Figure 9. ADM234L DIP/SOIC Pin Configuration

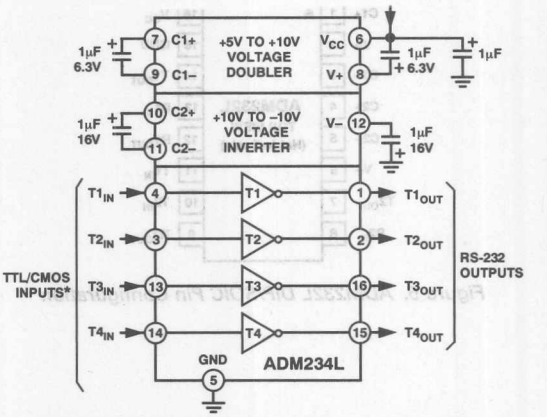


Figure 10. ADM234L Typical Operating Circuit

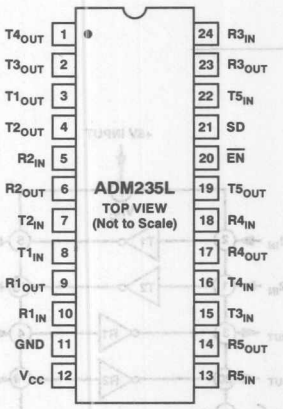


Figure 11. ADM235L DIP Pin Configuration

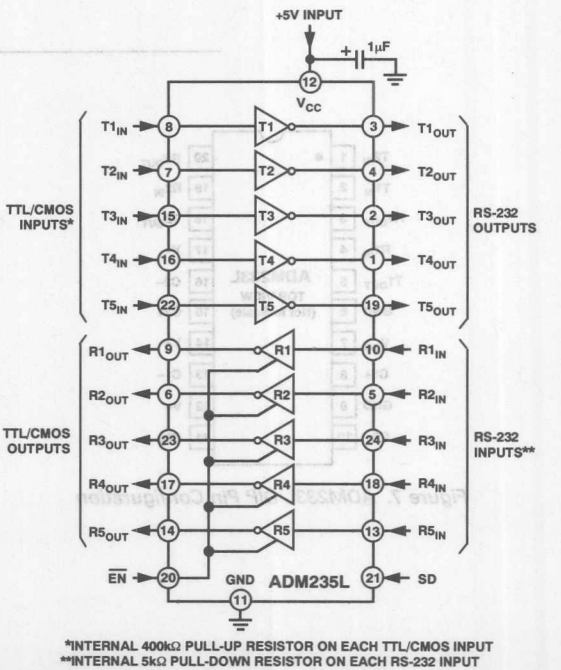


Figure 12. ADM235L Typical Operating Circuit

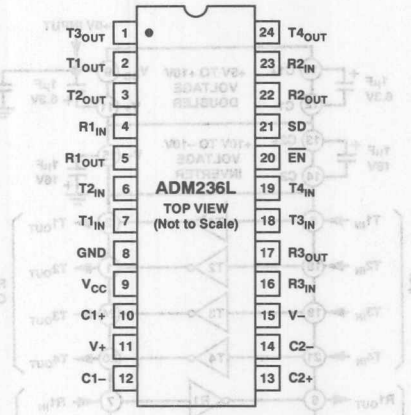


Figure 13. ADM236L DIP/SOIC Pin Configuration

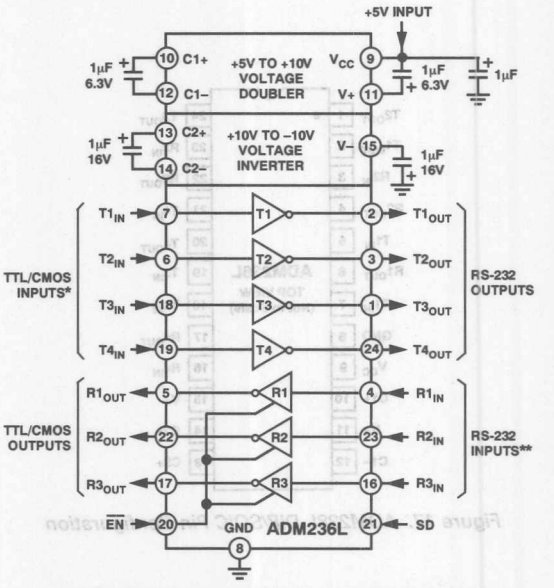


Figure 14. ADM236L Typical Operating Circuit

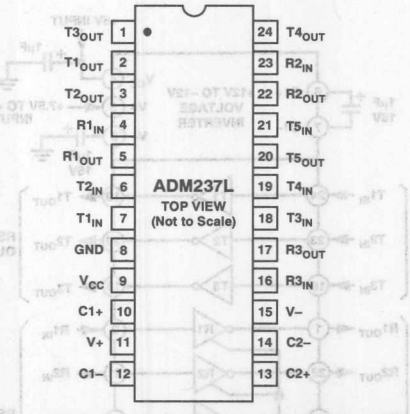


Figure 15. ADM237L DIP/SOIC Pin Configuration

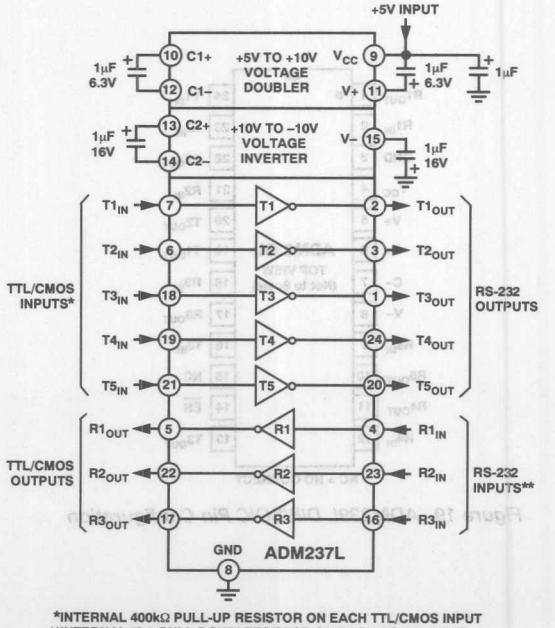


Figure 16. ADM237L Typical Operating Circuit

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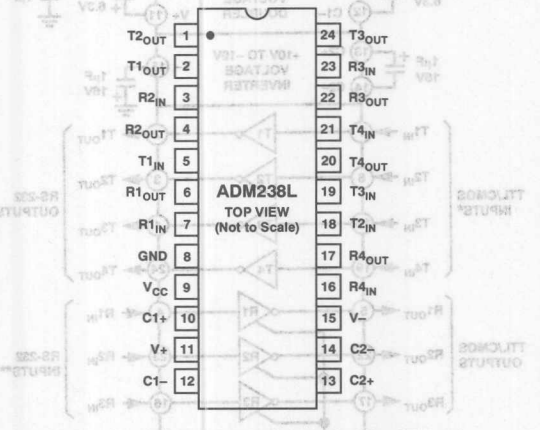
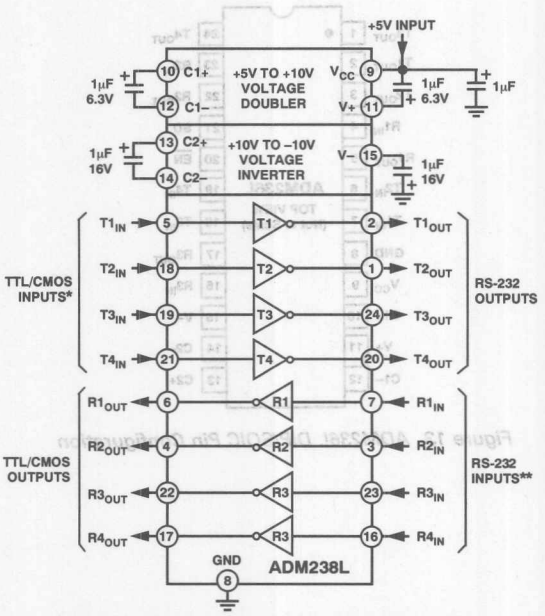


Figure 17. ADM238L DIP/SOIC Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 18. ADM238L Typical Operating Circuit

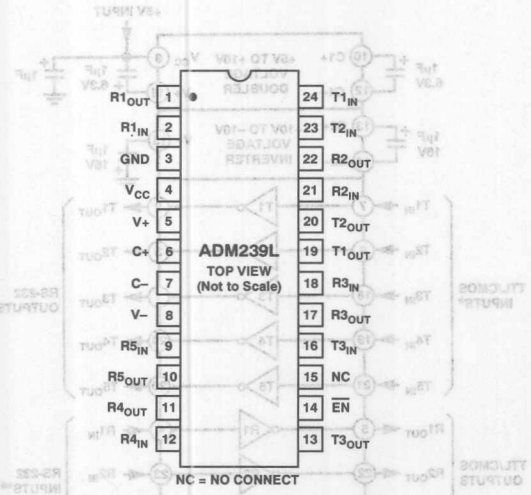
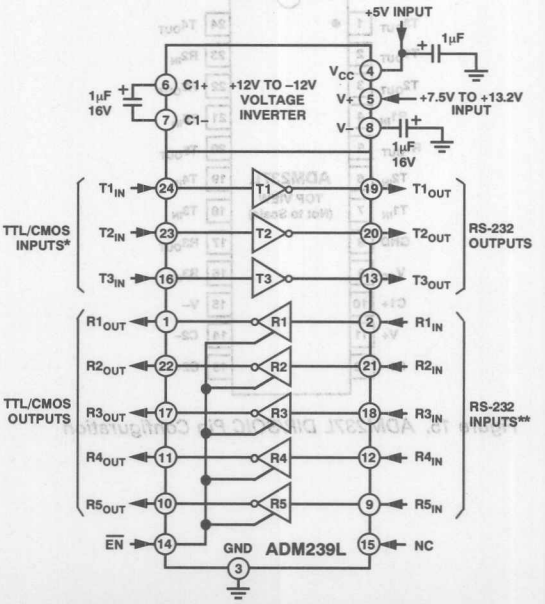


Figure 19. ADM239L DIP/SOIC Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 20. ADM239L Typical Operating Circuit

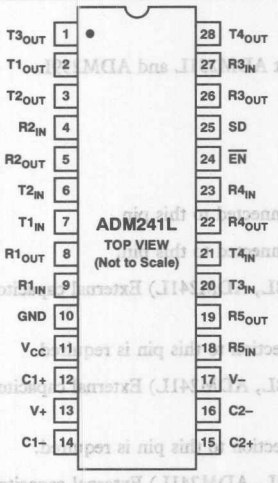


Figure 21. ADM241L SOIC/SSOP Pin Configuration

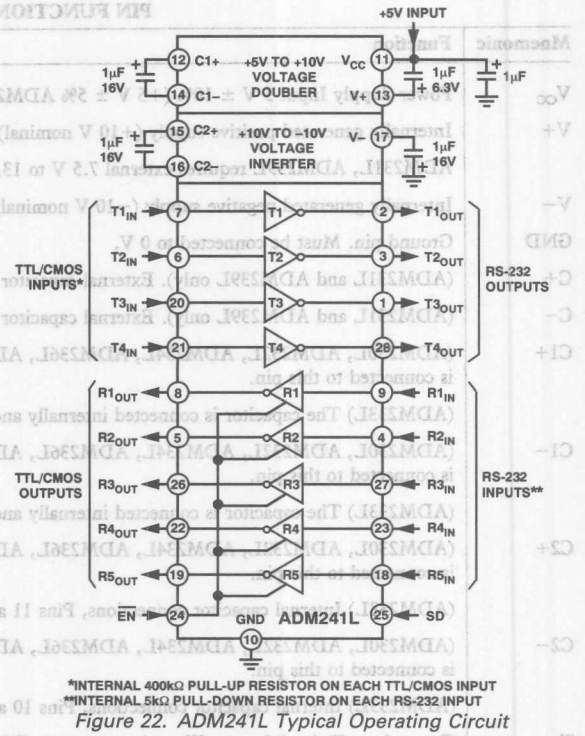


Figure 22. ADM241L Typical Operating Circuit

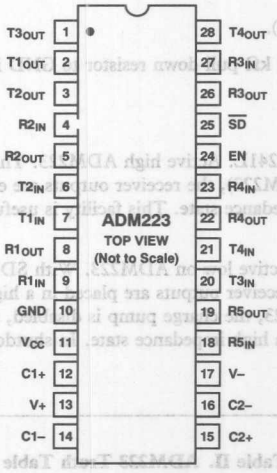


Figure 23. ADM223 SOIC/SSOP Pin Configuration

SD	EN	Status	T1–T4	R1–R3	R4, R5
0	0	Shutdown	Disabled	Disabled	Disabled
0	1	Shutdown	Disabled	Disabled	Enabled
1	0	Normal Operation	Enabled	Disabled	Disabled
1	1	Normal Operation	Enabled	Enabled	Enabled

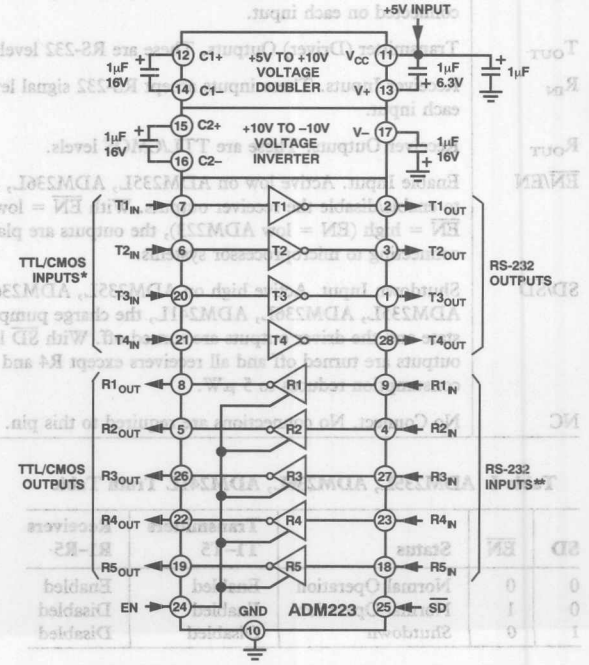


Figure 24. ADM223 Typical Operating Circuit

V_{CC}	Power Supply Input 5 V ± 10% (+5 V ± 5% ADM233L, ADM235L).
V+	Internally generated positive supply (+10 V nominal) on all parts except ADM231L and ADM239L. ADM231L, ADM239L requires external 7.5 V to 13.2 V supply.
V−	Internally generated negative supply (−10 V nominal).
GND	Ground pin. Must be connected to 0 V.
C+	(ADM231L and ADM239L only). External capacitor (+ terminal) is connected to this pin.
C−	(ADM231L and ADM239L only). External capacitor (− terminal) is connected to this pin.
C1+	(ADM230L, ADM232L, ADM234L, ADM236L, ADM237L, ADM238L, ADM241L) External capacitor (+ terminal) is connected to this pin. (ADM233L) The capacitor is connected internally and no external connection to this pin is required.
C1−	(ADM230L, ADM232L, ADM234L, ADM236L, ADM237L, ADM238L, ADM241L) External capacitor (− terminal) is connected to this pin. (ADM233L) The capacitor is connected internally and no external connection to this pin is required.
C2+	(ADM230L, ADM232L, ADM234L, ADM236L, ADM237L, ADM238L, ADM241L) External capacitor (+ terminal) is connected to this pin. (ADM233L) Internal capacitor connections, Pins 11 and 15 must be connected together.
C2−	(ADM230L, ADM232L, ADM234L, ADM236L, ADM237L, ADM238L, ADM241L) External capacitor (− terminal) is connected to this pin. (ADM233L) Internal capacitor connections, Pins 10 and 16 must be connected together.
T_{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V_{CC} is connected on each input.
T_{OUT}	Transmitter (Driver) Outputs. These are RS-232 levels (typically ±10 V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$/EN	Enable Input. Active low on ADM235L, ADM236L, ADM239L, ADM241L. Active high ADM223. This input is used to enable/disable the receiver outputs. With $\overline{EN}$ = low (EN = high ADM223), the receiver outputs are enabled. With $\overline{EN}$ = high (EN = low ADM223), the outputs are placed in a high impedance state. This facility is useful for connecting to microprocessor systems.
SD/$\overline{SD}$	Shutdown Input. Active high on ADM235L, ADM236L, ADM241L. Active low on ADM223. With SD = high on the ADM235L, ADM236L, ADM241L, the charge pump is disabled, the receiver outputs are placed in a high impedance state and the driver outputs are turned off. With $\overline{SD}$ low on the ADM223, the charge pump is disabled, the driver outputs are turned off and all receivers except R4 and R5 are placed in a high impedance state. In shutdown, the power consumption reduces to 5 μW.
NC	No Connect. No connections are required to this pin.

Table I. ADM235L, ADM236L, ADM241L Truth Table

SD	$\overline{EN}$	Status	Transmitters T1–T5	Receivers R1–R5
0	0	Normal Operation	Enabled	Enabled
0	1	Normal Operation	Enabled	Disabled
1	0	Shutdown	Disabled	Disabled

Table II. ADM223 Truth Table

$\overline{SD}$	EN	Status	Transmitters T1–T4	Receivers R1–R3	Receivers R4, R5
0	0	Shutdown	Disabled	Disabled	Disabled
0	1	Shutdown	Disabled	Disabled	Enabled
1	0	Normal Operation	Enabled	Disabled	Disabled
1	1	Normal Operation	Enabled	Enabled	Enabled

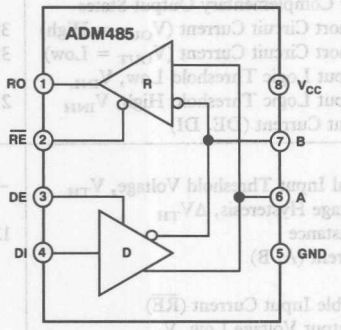
+5 V Low Power EIA RS-485 Transceiver

ADM485

FEATURES
- Meets EIA RS-485 Standard
- 5 Mb/s Data Rate
- Single +5 V Supply
- −7 V to +12 V Bus Common-Mode Range
- High Speed, Low Power BiCMOS
- Thermal Shutdown Protection
- Short Circuit Protection
- Zero Skew Driver
- Driver Propagation Delay: 10 ns
- Receiver Propagation Delay: 25 ns
- High Z Outputs with Power Off
- Superior Upgrade for LTC485

APPLICATIONS
- Low Power RS-485 Systems
- DTE-DCE Interface
- Packet Switching
- Local Area Networks
- Data Concentration
- Data Multiplexers
- Integrated Services Digital Network (ISDN)

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The ADM485 is a differential line transceiver suitable for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced data transmission and complies with both EIA Standards RS-485 and RS-422. The part contains a differential line driver and a differential line receiver. Both the driver and the receiver may be enabled independently. When disabled, the outputs are tristated.

The ADM485 operates from a single +5 V power supply. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if during fault conditions a significant temperature increase is detected in the internal driver circuitry.

Up to 32 transceivers may be connected simultaneously on a bus, but only one driver should be enabled at any time. It is important therefore that the remaining disabled drivers do not load the bus. To ensure this, the ADM485 driver features high output impedance when disabled and also when powered down. This minimizes the loading effect when the transceiver is not being utilized. The high impedance driver output is maintained over the entire common-mode voltage range from −7 V to +12 V.

The receiver contains a fail safe feature which results in a logic high output state if the inputs are unconnected (floating).

The ADM485 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology. All inputs and outputs contain protection against ESD; all driver outputs feature high source and sink current capability. An epitaxial layer is used to guard against latch-up.

The ADM485 features extremely fast switching speeds. Minimal driver propagation delays permit transmission at data rates up to 5 Mbits/s while low skew minimizes EMI interference.

The part is fully specified over the commercial and industrial temperature range and is available in an 8-pin DIL/ SOIC package.

ADM485—SPECIFICATIONS (V_{CC} = +5 V ± 5%. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}			5.0	V	R = ∞, Figure 1
	2.0		5.0	V	V_{CC} = 5 V, R = 50 Ω (RS422), Figure 1
	1.5		5.0	V	R = 27 Ω (RS485), Figure 1
V_{OD3}	1.5		5.0	V	V_{TST} = −7 V to +12 V, Figure 2
$\Delta\|V_{OD}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, Figure 1
Common-Mode Output Voltage V_{OC}			3	V	R = 27 Ω or 50 Ω, Figure 1
$\Delta\|V_{OC}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω
Output Short Circuit Current (V_{OUT} = High)	35		250	mA	−7 V ≤ V_O ≤ +12 V
Output Short Circuit Current (V_{OUT} = Low)	35		250	mA	−7 V ≤ V_O ≤ +12 V
CMOS Input Logic Threshold Low, V_{INL}			0.8	V	
CMOS Input Logic Threshold High, V_{INH}	2.0			V	
Logic Input Current (DE, DI)			±1.0	μA	
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	−0.2		+0.2	V	−7 V ≤ V_{CM} ≤ +12 V
Input Voltage Hysteresis, ΔV_{TH}		70		mV	V_{CM} = 0 V
Input Resistance	12			kΩ	−7 V ≤ V_{CM} ≤ +12 V
Input Current (A, B)			+1	mA	V_{IN} = 12 V
			−0.8	mA	V_{IN} = −7 V
Logic Enable Input Current ($\overline{RE}$)			±1	μA	
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = +4.0 mA
CMOS Output Voltage High, V_{OH}	4.0			V	I_{OUT} = −4.0 mA
Short Circuit Output Current	7		85	mA	V_{OUT} = GND or V_{CC}
Tristate Output Leakage Current			±1.0	μA	0.4 V ≤ V_{OUT} ≤ +2.4 V
POWER SUPPLY CURRENT					
I_{CC} (Outputs Enabled)		1.35	2.2	mA	Outputs Unloaded, Digital Inputs = GND or V_{CC}
I_{CC} (Outputs Disabled)		0.7	1	mA	Outputs Unloaded, Digital Inputs = GND or V_{CC}

Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{CC} = +5 V ± 5%. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/ Comments
DRIVER					
Propagation Delay Input to Output T_{PLH}, T_{PHL}	2	10	15	ns	R_L Diff = 54 Ω C_{L1} = C_{L2} = 100 pF, Figure 3
Driver O/P to $\overline{O/P}$ T_{SKEW}		0	5	ns	R_L Diff = 54 Ω C_{L1} = C_{L2} = 100 pF, Figure 3
Driver Rise/Fall Time T_R, T_F		2	10	ns	R_L Diff = 54 Ω C_{L1} = C_{L2} = 100 pF, Figure 3
Driver Enable to Output Valid		10	25	ns	
Driver Disable Timing		10	25	ns	
RECEIVER					
Propagation Delay Input to Output T_{PLH}, T_{PHL}	18	25	40	ns	C_L = 15 pF, Figure 5
Skew $\|T_{PLH}-T_{PHL}\|$		0	5	ns	
Receiver Enable T_{EN1}		15	25	ns	Figure 6
Receiver Disable T_{EN2}		15	25	ns	Figure 6

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{CC} . . . . . +7 V
Inputs
Driver Input (DI) . . . . . −0.3 V to V_{CC} + 0.3 V
Control Inputs (DE, RE) . . . . . −0.3 V to V_{CC} + 0.3 V
Receiver Inputs (A, B) . . . . . −14 V to +14 V
Outputs
Driver Outputs . . . . . −14 V to +14 V
Receiver Output . . . . . −0.5 V to V_{CC} + 0.5 V
Power Dissipation 8-Pin DIP . . . . . 500 mW
θ_{JA}, Thermal Impedance . . . . . +130°C/W
Power Dissipation 8-Pin SOIC . . . . . 450 mW
θ_{JA}, Thermal Impedance . . . . . +170°C/W
Power Dissipation 8-Pin Cerdip . . . . . 500 mW
θ_{JA}, Thermal Impedance . . . . . +125°C/W
Operating Temperature Range
Commercial (J Version) . . . . . 0°C to +70°C
Industrial (A Version) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Vapour Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

Table I. Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
X	0	X	Z	Z

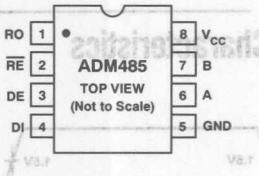
Table II. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2 V	1
0	0	≤ −0.2 V	0
0	0	Inputs Open	1
1	0	X	Z

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1	RO	Receiver Output. When enabled if A > B by 200 mV, then RO = High. If A < B by 200 mV, then RO = Low.
2	$\overline{RE}$	Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state.
3	DE	Driver Output Enable. A high level enables the driver differential outputs, A and B. A low level places it in a high impedance state.
4	DI	Driver Input. When the driver is enabled a logic Low on DI forces A low and B high while a logic High on DI forces A high and B low.
5	GND	Ground Connection, 0 V.
6	A	Noninverting Receiver Input A/Driver Output A.
7	B	Inverting Receiver Input B/Driver Output B.
8	V_{CC}	Power Supply, 5 V ± 5%.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM485JN	0°C to +70°C	N-8
ADM485JR	0°C to +70°C	R-8
ADM485AN	−40°C to +85°C	N-8
ADM485AR	−40°C to +85°C	R-8
ADM485AQ	−40°C to +85°C	Q-8

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM485 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Test Circuits

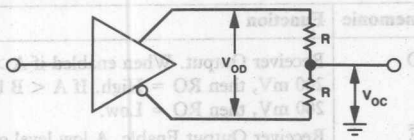


Figure 1. Driver Voltage Measurement Test Circuit

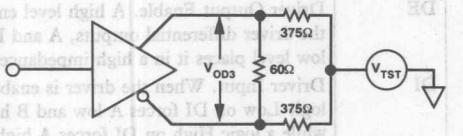


Figure 2. Driver Voltage Measurement Test Circuit 2

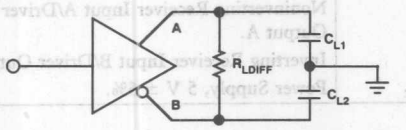


Figure 3. Driver Propagation Delay Test Circuit

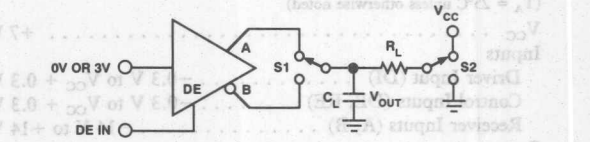


Figure 4. Driver Enable/Disable Test Circuit

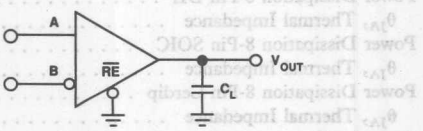


Figure 5. Receiver Propagation Delay Test Circuit

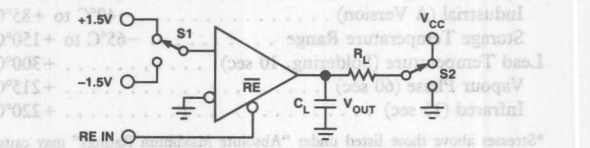


Figure 6. Receiver Enable/Disable Test Circuit

Switching Characteristics

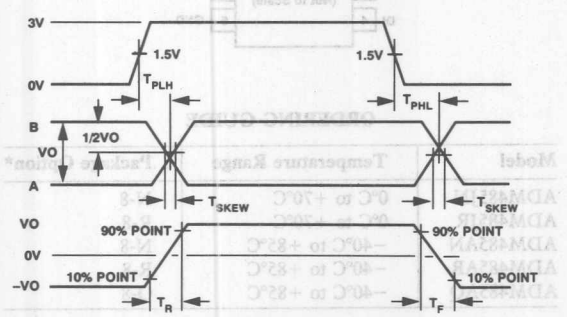


Figure 7. Driver Propagation Delay, Rise/Fall Timing

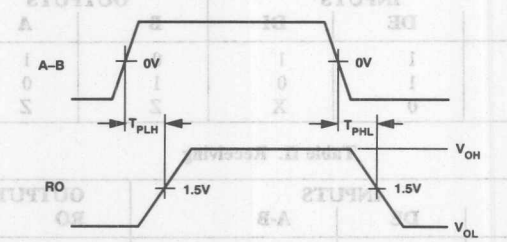


Figure 9. Receiver Propagation Delay

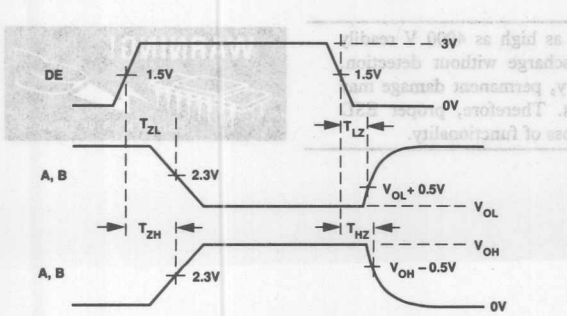


Figure 8. Driver Enable/Disable Timing

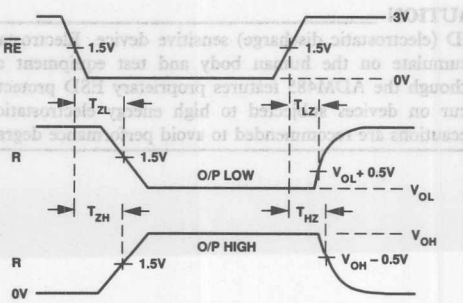


Figure 10. Receiver Enable/Disable Timing

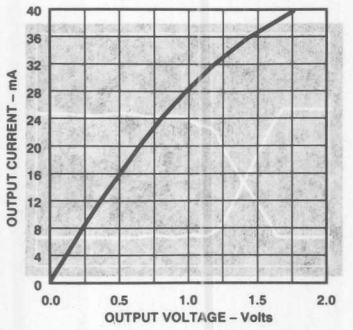


Figure 11. Receiver Output Low Voltage vs. Output Current

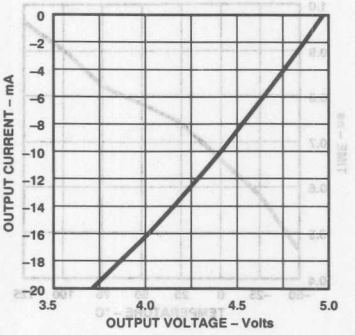


Figure 12. Receiver Output High Voltage vs. Output Current

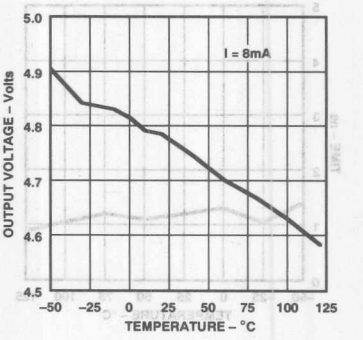


Figure 13. Receiver Output High Voltage vs. Temperature

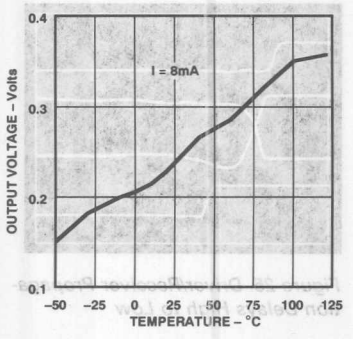


Figure 14. Receiver Output Low Voltage vs. Temperature

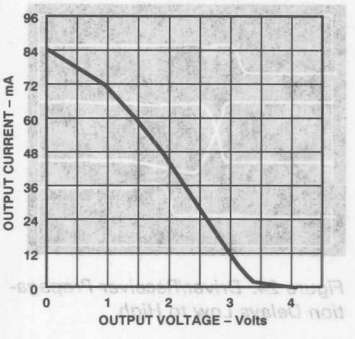


Figure 15. Driver Differential Output Voltage vs. Output Current

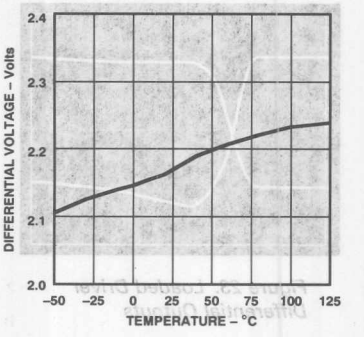


Figure 16. Driver Differential Output Voltage vs. Temperature, R_L = 54 Ω

15

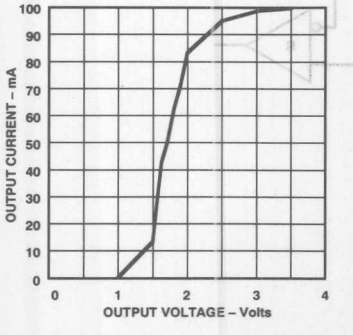


Figure 17. Driver Output Low Voltage vs. Output Current

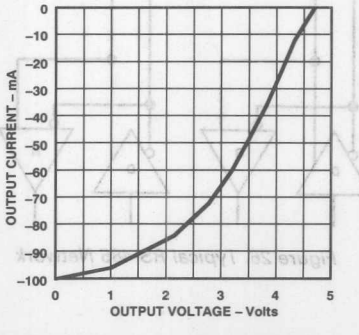


Figure 18. Driver Output High Voltage vs. Output Current

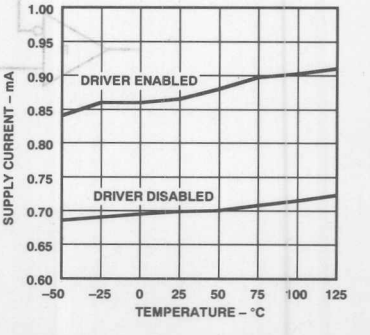


Figure 19. Supply Current vs. Temperature

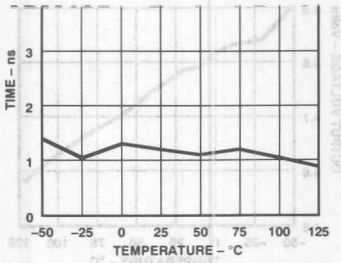


Figure 20. Receiver t_{PLH}–t_{PHL} vs. Temperature

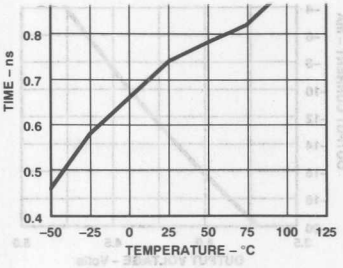


Figure 21. Driver Skew vs. Temperature

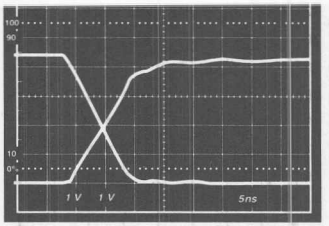


Figure 22. Unloaded Driver Differential Outputs

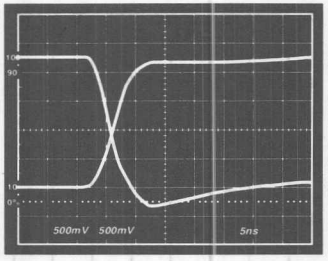


Figure 23. Loaded Driver Differential Outputs

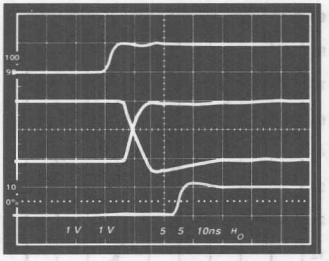


Figure 24. Driver/Receiver Propagation Delays Low to High

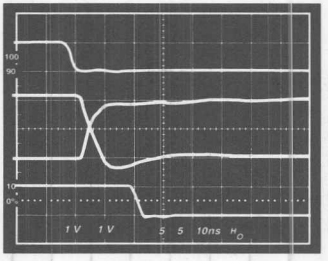


Figure 25. Driver/Receiver Propagation Delays High to Low

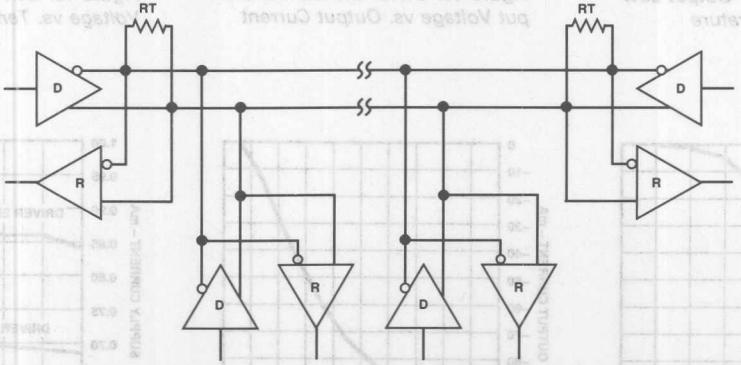


Figure 26. Typical RS-485 Network

APPLICATIONS INFORMATION

Differential Data Transmission

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals which appear as common-mode voltages on the line. There are two main standards approved by the Electronics Industries Association (EIA) which specify the electrical characteristics of transceivers used in differential data transmission.

The RS-422 standard specifies data rates up to 10 MBaud and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.

In order to cater for true multipoint communications, the RS-485 standard was defined. This standard meets or exceeds all the requirements of RS-422 but also allows for up to 32 drivers and 32 receivers to be connected to a single bus. An extended common-mode range of −7 V to +12 V is defined. The most significant difference between RS-422 and RS-485 is the fact that the drivers may be disabled thereby allowing more than one (32 in fact) to be connected to a single line. Only one driver should be enabled at time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

Cable and Data Rate

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby, reducing the effective inductance of the pair.

The ADM485 is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 26. An RS-485 transmission line can have as many as 32 transceivers on the bus. Only one driver can transmit at a particular time but multiple receivers may be enabled simultaneously.

As with any transmission line, it is important that reflections are minimized. This may be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

Thermal Shutdown

The ADM485 contains thermal shutdown circuitry which protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature and disables the driver outputs. The thermal sensing circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at 140°C.

Propagation Delay

The ADM485 features very low propagation delay ensuring maximum baud rate operation. The driver is well balanced ensuring distortion free transmission.

Another important specification is a measure of the skew between the complementary outputs. Excessive skew impairs the noise immunity of the system and increases the amount of electromagnetic interference (EMI).

Receiver Open-Circuit Fail Safe

The receiver input includes a fail-safe feature which guarantees a logic high on the receiver when the inputs are open circuit or floating.

Table III. Comparison of RS-422 and RS-485 Interface Standards

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Cable Length	4000 ft.	4000 ft.
Minimum Driver Output Voltage	±2 V	±1.5 V
Driver Load Impedance	100 Ω	54 Ω
Receiver Input Resistance	4 kΩ min	12 kΩ min
Receiver Input Sensitivity	±200 mV	±200 mV
Receiver Input Voltage Range	−7 V to +7 V	−7 V to +12 V
No of Drivers/Receivers Per Line	1/10	32/32

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Microprocessor Supervisory Circuits

ADM690–ADM695

FEATURES

Superior Upgrade for MAX690–MAX695
Specified Over Temperature
Low Power Consumption (5 mW)
Precision Voltage Monitor
Reset Assertion Down to 1 V V_{CC}
Low Switch On-Resistance 1.5 Ω Normal, 20 Ω in Backup
High Current Drive (100 mA)
Watchdog Timer—100 ms, 1.6 s, or Adjustable
600 nA Standby Current
Automatic Battery Backup Power Switching
Extremely Fast Gating of Chip Enable Signals (5 ns)
Voltage Monitor for Power Fail

APPLICATIONS

Microprocessor Systems
Computers
Controllers
Intelligent Instruments
Automotive Systems

GENERAL DESCRIPTION

The ADM690–ADM695 family of supervisory circuits offers complete single chip solutions for power supply monitoring and battery control functions in microprocessor systems. These functions include μP reset, backup battery switchover, watchdog timer, CMOS RAM write protection, and power failure warning. The complete family provides a variety of configurations to satisfy most microprocessor system requirements.

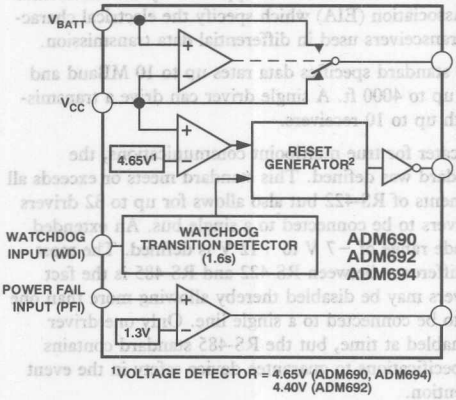
The ADM690, ADM692 and ADM694 are available in 8-pin DIP packages and provide:

1. Power-on reset output during power-up, power-down and brownout conditions. The RESET output remains operational with V_{CC} as low as 1 V.
2. Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic.
3. A reset pulse if the optional watchdog timer has not been toggled within a specified time.
4. A 1.3 V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5 V.

The ADM691, ADM693 and ADM695 are available in 16-pin DIP and small outline packages and provide three additional functions:

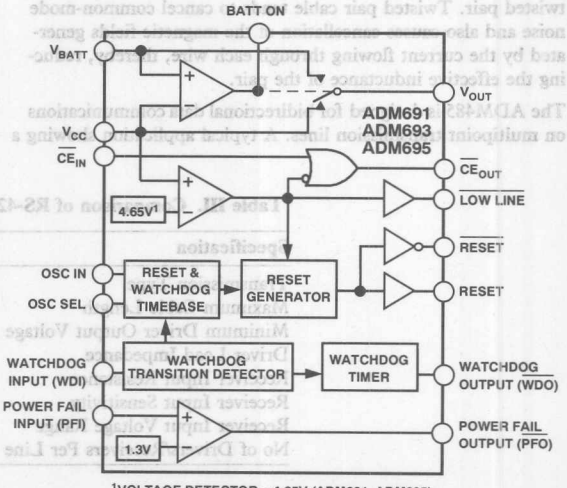
1. Write protection of CMOS RAM or EEPROM.
2. Adjustable reset and watchdog timeout periods.
3. Separate watchdog timeout, backup battery switchover, and low V_{CC} status outputs.

FUNCTIONAL BLOCK DIAGRAMS



¹VOLTAGE DETECTOR = 4.65V (ADM690, ADM694)
4.40V (ADM692)

²RESET PULSE WIDTH = 50ms (ADM690, ADM692)
200ms (ADM694)



¹VOLTAGE DETECTOR = 4.65V (ADM691, ADM695)
4.40V (ADM693)

The ADM690–ADM695 family is fabricated using an advanced epitaxial CMOS process combining low power consumption (5 mW), extremely fast Chip Enable gating (5 ns) and high reliability. RESET assertion is guaranteed with V_{CC} as low as 1 V. In addition, the power switching circuitry is designed for minimal voltage drop thereby permitting increased output current drive of up to 100 mA without the need for an external pass transistor.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (V_{CC} = Full Operating Range, V_{BATT} = +2.8 V, T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
BATTERY BACKUP SWITCHING					
V_{CC} Operating Voltage Range					
ADM690, ADM691, ADM694, ADM695	4.75		5.5	V	
ADM692, ADM693	4.5		5.5	V	
V_{BATT} Operating Voltage Range					
ADM690, ADM691, ADM694, ADM695	2.0		4.25	V	
ADM692, ADM693	2.0		4.0	V	
V_{OUT} Output Voltage	V_{CC} – 0.05	V_{CC} – 0.025		V	I_{OUT} = 1 mA
	V_{CC} – 0.5	V_{CC} – 0.25		V	I_{OUT} ≤ 100 mA
V_{OUT} in Battery Backup Mode	V_{BATT} – 0.05	V_{BATT} – 0.02		V	I_{OUT} = 250 µA, V_{CC} < V_{BATT} – 0.2 V
Supply Current (Excludes I_{OUT})		1	1.95	mA	I_{OUT} = 100 mA
Supply Current in Battery Backup Mode		0.6	1	µA	V_{CC} = 0 V, V_{BATT} = 2.8 V
Battery Standby Current					5.5 V > V_{CC} > V_{BATT} + 0.2 V
(+ = Discharge, – = Charge)	–0.1		+0.02	µA	T_A = +25°C
	–1.0		+0.02	µA	
Battery Switchover Threshold		70		mV	Power Up
V_{CC} – V_{BATT}		50		mV	Power Down
Battery Switchover Hysteresis		20		mV	
BATT ON Output Voltage			0.3	V	I_{SINK} = 3.2 mA
BATT ON Output Short Circuit Current		35		mA	BATT ON = V_{OUT} = 4.5 V Sink Current
	0.5	1	25	µA	BATT ON = 0 V Source Current
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold					
ADM690, ADM691, ADM694, ADM695	4.5	4.65	4.73	V	
ADM692, ADM693	4.25	4.4	4.48	V	
Reset Threshold Hysteresis		40		mV	
Reset Timeout Delay					
ADM690, ADM691, ADM692, ADM693	35	50	70	ms	OSC SEL = HIGH, V_{CC} = 5 V, T_A = +25°C
ADM694, ADM695	140	200	280	ms	OSC SEL = HIGH, V_{CC} = 5 V, T_A = +25°C
Watchdog Timeout Period, Internal Oscillator	1.0	1.6	2.25	s	Long Period, V_{CC} = 5 V, T_A = +25°C
	70	100	140	ms	Short Period, V_{CC} = 5 V, T_A = +25°C
Watchdog Timeout Period, External Clock	3840		4097	Cycles	Long Period
	768		1025	Cycles	Short Period
Minimum WDI Input Pulse Width	50			ns	V_{IL} = 0.4, V_{IH} = 3.5 V
$\overline{\text{RESET}}$ Output Voltage @ V_{CC} = +1 V		4	200	mV	I_{SINK} = 10 µA, V_{CC} = 1 V
RESET, LOW LINE Output Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 4.25 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
RESET, $\overline{\text{WDO}}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 5 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 4.25 V
Output Short Circuit Source Current	1	3	25	µA	
Output Short Circuit Sink Current		25		mA	
WDI Input Threshold					V_{CC} = 5 V[1]
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		20	50	µA	WDI = V_{OUT}, T_A = +25°C
	–50	–15		µA	WDI = 0 V, T_A = +25°C
POWER FAIL DETECTOR					
PFI Input Threshold	1.25	1.3	1.35	V	V_{CC} = +5 V
PFI Input Current	–25	±0.01	+25	nA	
$\overline{\text{PFO}}$ Output Voltage			0.4	V	I_{SINK} = 3.2 mA
	3.5			V	I_{SOURCE} = 1 µA
$\overline{\text{PFO}}$ Short Circuit Source Current	1	3	25	µA	PFI = Low, $\overline{\text{PFO}}$ = 0 V
$\overline{\text{PFO}}$ Short Circuit Sink Current		25		mA	PFI = High, $\overline{\text{PFO}}$ = V_{OUT}
CHIP ENABLE GATING					
$\overline{CE}_{IN}$ Threshold			0.8	V	V_{IL}
	3.0			V	V_{IH}
$\overline{CE}_{IN}$ Pull-Up Current		3		µA	
$\overline{CE}_{OUT}$ Output Voltage			0.4	V	I_{SINK} = 3.2 mA
	V_{OUT} – 1.5			V	I_{SOURCE} = 3.0 mA
	V_{OUT} – 0.05			V	I_{SOURCE} = 1 µA, V_{CC} = 0 V
$\overline{CE}$ Propagation Delay		5	9	ns	

OSC IN Input Current		±2		µA	
OSC SEL Input Pull-Up Current		5		µA	
OSC IN Frequency Range	0		250	kHz	OSC SEL = 0 V
OSC IN Frequency with External Capacitor		4		kHz	OSC SEL = 0 V, C_{OSC} = 47 pF

NOTE
[1]WDI is a three level input which is internally biased to 38% of V_{CC} and has an input impedance of approximately 125 kΩ.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} . . . . . −0.3 V to +6 V
V_{BATT} . . . . . −0.3 V to +6 V
All Other Inputs . . . . . −0.3 V to V_{OUT} + 0.5 V
Input Current
  V_{CC} . . . . . 200 mA
  V_{BATT} . . . . . 50 mA
  GND . . . . . 20 mA
Digital Output Current . . . . . 20 mA
Power Dissipation, N-8 DIP . . . . . 400 mW
  θ_{JA} Thermal Impedance . . . . . 120°C/W
Power Dissipation, Q-8 DIP . . . . . 500 mW
  θ_{JA} Thermal Impedance . . . . . 125°C/W
Power Dissipation, N-16 DIP . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 135°C/W
Power Dissipation, Q-16 DIP . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 100°C/W
Power Dissipation, R-16 SOIC . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 110°C/W
Operating Temperature Range
  Industrial (A Version) . . . . . −40°C to +85°C
  Extended (S Version) . . . . . −55°C to +125°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
  Vapor Phase (60 secs) . . . . . +215°C
  Infrared (15 secs) . . . . . +220°C
Storage Temperature Range . . . . . −65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM690AN	−40°C to +85°C	N-8
ADM690AQ	−40°C to +85°C	Q-8
ADM690SQ	−55°C to +125°C	Q-8
ADM691AN	−40°C to +85°C	N-16
ADM691AR	−40°C to +85°C	R-16
ADM691AQ	−40°C to +85°C	Q-16
ADM691SQ	−55°C to +125°C	Q-16
ADM692AN	−40°C to +85°C	N-8
ADM692AQ	−40°C to +85°C	Q-8
ADM692SQ	−55°C to +125°C	Q-8
ADM693AN	−40°C to +85°C	N-16
ADM693AR	−40°C to +85°C	R-16
ADM693AQ	−40°C to +85°C	Q-16
ADM693SQ	−55°C to +125°C	Q-16
ADM694AN	−40°C to +85°C	N-8
ADM694AQ	−40°C to +85°C	Q-8
ADM694SQ	−55°C to +125°C	Q-8
ADM695AN	−40°C to +85°C	N-16
ADM695AR	−40°C to +85°C	R-16
ADM695AQ	−40°C to +85°C	Q-16
ADM695SQ	−55°C to +125°C	Q-16

*For outline information see Package Information section.

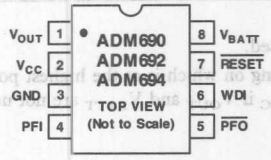
CAUTION

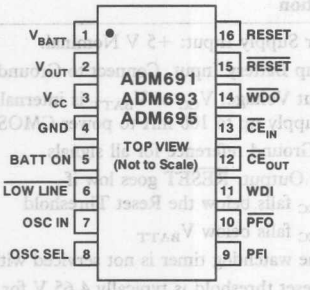
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM690–ADM695 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power Supply Input: +5 V Nominal.
V_{BATT}	Backup Battery Input. Connect to Ground if a backup battery is not used.
V_{OUT}	Output Voltage, V_{CC} or V_{BATT} is internally switched to V_{OUT} depending on which is at the highest potential. V_{OUT} can supply up to 100 mA to power CMOS RAM. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	0 V. Ground reference for all signals.
$\overline{\text{RESET}}$	Logic Output. $\overline{\text{RESET}}$ goes low if 1. V_{CC} falls below the Reset Threshold 2. V_{CC} falls below V_{BATT} 3. The watchdog timer is not serviced within its timeout period. The reset threshold is typically 4.65 V for the ADM690/ADM691/ADM694/ADM695 and 4.4 V for the ADM692 and ADM693. $\overline{\text{RESET}}$ remains low for 50 ms (ADM690/ADM691/ADM692/ADM693) or 200 ms (ADM694/ADM695) after V_{CC} returns above the threshold. $\overline{\text{RESET}}$ also goes low for 50 (200) ms if the watchdog timer is enabled but not serviced within its timeout period. The $\overline{\text{RESET}}$ pulse width can be adjusted on the ADM691/ADM693/ADM695 as shown in Table I. The $\overline{\text{RESET}}$ output has an internal 3 μA pull up, and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pull-up resistor.
WDI	Watchdog Input. WDI is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{\text{RESET}}$ pulses low and WDO goes low. The timer resets with each transition on the WDI line. The watchdog timer may be disabled if WDI is left floating or is driven to midsupply.
PFI	Power Fail Input. PFI is the noninverting input to the Power Fail Comparator When PFI is less than 1.3 V, $\overline{\text{PFO}}$ goes low. Connect PFI to GND or V_{OUT} when not used.
$\overline{\text{PFO}}$	Power Fail Output. $\overline{\text{PFO}}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3 V. The comparator is turned off and $\overline{\text{PFO}}$ goes low when V_{CC} is below V_{BATT}.
$\overline{\text{CE}}_{IN}$	Logic Input. The input to the $\overline{\text{CE}}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{\text{CE}}_{OUT}$	Logic Output. $\overline{\text{CE}}_{OUT}$ is a gated version of the $\overline{\text{CE}}_{IN}$ signal. $\overline{\text{CE}}_{OUT}$ tracks $\overline{\text{CE}}_{IN}$ when V_{CC} is above the reset threshold. If V_{CC} is below the reset threshold, $\overline{\text{CE}}_{OUT}$ is forced high. See Figures 5 and 6.
BATT ON	Logic Output. BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 35 mA and can directly drive the base of an external PNP transistor to increase the output current above the 100 mA rating of V_{OUT}.
$\overline{\text{LOW LINE}}$	Logic Output. $\overline{\text{LOW LINE}}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold.
RESET	Logic Output. RESET is an active high output. It is the inverse of $\overline{\text{RESET}}$.
OSC SEL	Logic Oscillator Select Input. When OSC SEL is unconnected (floating) or driven high, the internal oscillator sets the reset active time and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3 μA internal pull up, (see Table I).
OSC IN	Oscillator Logic Input. With OSC SEL low, OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND. This sets both the reset active pulse timing and the watchdog timeout period (see Table I and Figure 4). With OSC SEL high or floating, the internal oscillator is enabled and the reset active time is fixed at 50 ms typ. (ADM691/93) or 200 ms typ (ADM695). In this mode the OSC IN pin selects between fast (100 ms) and slow (1.6 s) watchdog timeout periods. In both modes, the timeout period immediately after a reset is 1.6 s typical.
$\overline{\text{WDO}}$	Logic Output. The Watchdog Output, $\overline{\text{WDO}}$, goes low if WDI remains either high or low for longer than the watchdog timeout period. $\overline{\text{WDO}}$ is set high by the next transition at WDI. If WDI is unconnected or at midsupply, the watchdog timer is disabled and $\overline{\text{WDO}}$ remains high. $\overline{\text{WDO}}$ also goes high when $\overline{\text{LOW LINE}}$ goes low.

PIN CONFIGURATIONS





PRODUCT SELECTION GUIDE

Part Number	Nominal Reset Time	Nominal V_{CC} Reset Threshold	Nominal Watchdog Timeout Period	Battery Backup Switching	Base Drive Ext PNP	Chip Enable Signals
ADM690	50 ms	4.65 V	1.6 s	Yes	No	No
ADM691	50 ms or ADJ	4.65 V	100 ms, 1.6 s, ADJ	Yes	Yes	Yes
ADM692	50 ms	4.4 V	1.6 s	Yes	No	No
ADM693	50 ms or ADJ	4.4 V	100 ms, 1.6 s, ADJ	Yes	Yes	Yes
ADM694	200 ms	4.65 V	1.6 s	Yes	No	No
ADM695	200 ms or ADJ	4.65 V	100 ms, 1.6 s, ADJ	Yes	Yes	Yes

CIRCUIT INFORMATION

Battery Switchover Section

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50 mV higher than V_{BATT} as V_{CC} falls, and when V_{CC} is 70 mV greater than V_{BATT} as V_{CC} rises. This 20 mV of hysteresis prevents repeated rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

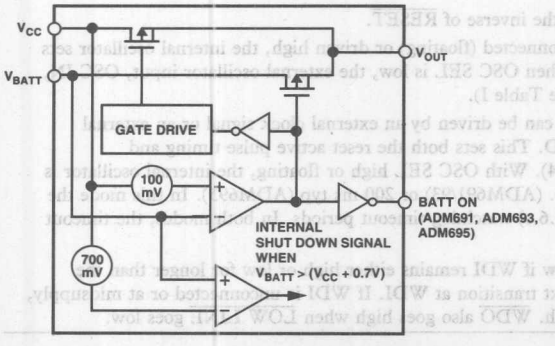


Figure 1. Battery Switchover Schematic

During normal operation with V_{CC} higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via an internal PMOS transistor switch. This switch has a typical on-resistance of 1.5 Ω and can supply up to 100 mA at the V_{OUT} terminal. V_{OUT} is normally used to drive a RAM memory bank which may require instantaneous currents of greater than 100 mA. If this is the case then a bypass capacitor should be connected to V_{OUT}. The capacitor will provide the peak current transients to the RAM. A capacitance value of 0.1 μF or greater may be used.

If the continuous output current requirement at V_{OUT} exceeds 100 mA or if a lower V_{CC}–V_{OUT} voltage differential is desired, an external PNP pass transistor may be connected in parallel with the internal transistor. The BATT ON output (ADM691/ADM693/ADM695) can directly drive the base of the external transistor.

A 20 Ω MOSFET switch connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery back up of CMOS RAM or other low power CMOS circuitry. The supply current in battery back up is typically 0.6 μA.

The ADM690/ADM691/ADM694/ADM695 operates with battery voltages from 2.0 V to 4.25 V and the ADM692/ADM693 operates with battery voltages from 2.0 V to 4.0 V. High value capacitors, either standard electrolytic or the farad size double layer capacitors, can also be used for short-term memory back up. A small charging current of typically 10 nA (0.1 μA max) flows out of the V_{BATT} terminal. This current is useful for maintaining rechargeable batteries in a fully charged condition. This extends the life of the back up battery by compensating for its self discharge current. Also note that this current poses no problem when lithium batteries are used for back up since the maximum charging current (0.1 μA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, V_{BATT} should be connected to GND and V_{OUT} should be connected to V_{CC}.

POWER FAIL $\overline{\text{RESET}}$ OUTPUT

$\overline{\text{RESET}}$ is an active low output which provides a $\overline{\text{RESET}}$ signal to the Microprocessor whenever V_{CC} is at an invalid level. When V_{CC} falls below the reset threshold the $\overline{\text{RESET}}$ output is forced low. The nominal reset voltage threshold is 4.65 V (ADM690/ADM691/ADM694/ADM695) or 4.4 V (ADM692/ADM693).

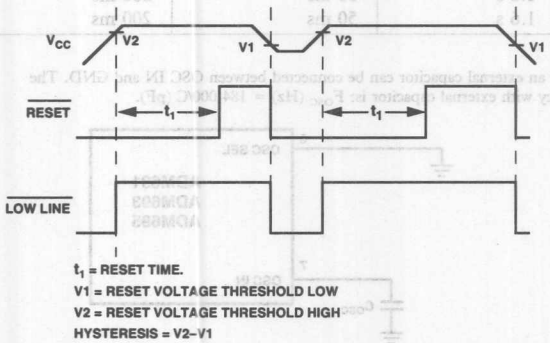


Figure 2. Power Fail Reset Timing

On power-up $\overline{\text{RESET}}$ will remain low for 50 ms (200 ms for ADM694 and ADM695) after V_{CC} rises above the appropriate reset threshold. This allows time for the power supply and microprocessor to stabilize. On power-down, the $\overline{\text{RESET}}$ output remains low with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition.

This $\overline{\text{RESET}}$ active time is adjustable on the ADM691/ADM693/ADM695 by using an external oscillator or by connecting an external capacitor to the OSC IN pin. Refer to Table I and Figure 4.

The guaranteed minimum and maximum thresholds of the ADM690/ADM691/ADM694/ADM695 are 4.5 V and 4.73 V, while the guaranteed thresholds of the ADM692/ADM693 are 4.25 V and 4.48 V. The ADM690/ADM691/ADM694/ADM695 is, therefore, compatible with 5 V supplies with a +10%, −5% tolerance while the ADM692/ADM693 is compatible with 5 V ± 10% supplies. The reset threshold comparator has approximately 50 mV of hysteresis. The response time of the reset voltage comparator is less than 1 µs. If glitches are present on the V_{CC} line which could cause spurious reset pulses, then V_{CC} should be decoupled close to the device.

In addition to $\overline{\text{RESET}}$ the ADM691/ADM693/ADM695 contain an active high RESET output. This is the complement of $\overline{\text{RESET}}$ and is intended for processors requiring an active high RESET signal.

Watchdog Timer $\overline{\text{RESET}}$

The watchdog timer circuit monitors the activity of the microprocessor in order to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the Watchdog Input (WDI) line. If this line is not toggled within the selected timeout period, a $\overline{\text{RESET}}$ pulse is generated. The nominal watchdog timeout period is preset at 1.6 seconds on the ADM690/ADM692/ADM694. The ADM691/ADM693/ADM695 may be configured for either a fixed "short" 100 ms or a "long" 1.6 second timeout period or for an adjustable timeout period. If the "short" period is selected, some systems may be unable to service the watchdog timer immediately after a reset, so the ADM691/ADM693/ADM695 automatically selects the "long" timeout period directly after a reset is issued. The watchdog timer is restarted at the end of reset, whether the reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold.

The normal (short) timeout period becomes effective following the first transition of WDI after $\overline{\text{RESET}}$ has gone inactive. The watchdog timeout period restarts with each transition on the WDI pin. To ensure that the watchdog timer does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum timeout period. If WDI remains permanently either high or low, reset pulses will be issued after each "long" timeout period (1.6 s). The watchdog monitor can be deactivated by floating the Watchdog Input (WDI) or by connecting it to midsupply.

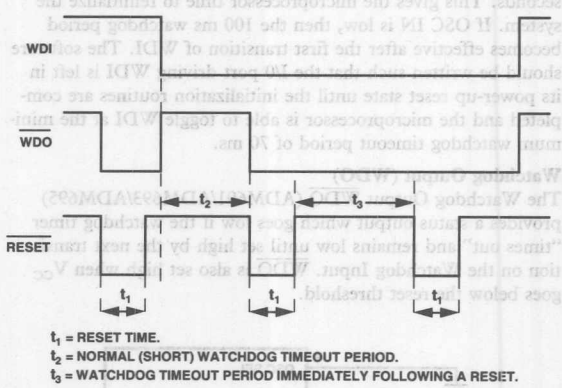


Figure 3. Watchdog Timeout Period and Reset Active Time

15

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Active Period	
		Normal	Immediately After Reset	ADM691/ADM693	ADM695
Low	External Clock Input	1024 CLKS	4096 CLKS	512 CLKS	2048 CLKS
Low	External Capacitor	400 ms × C/47 pF	1.6 s × C/47 pF	200 ms × C/47 pF	800 ms × C/47 pF
Floating or High	Low	100 ms	1.6 s	50 ms	200 ms
Floating or High	Floating or High	1.6 s	1.6 s	50 ms	200 ms

NOTE
With the OSC SEL pin low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24 kHz. The nominal oscillator frequency with external capacitor is: F_{OSC} (Hz) = 184,000/C (pF).

The watchdog timeout period is fixed at 1.6 seconds, and the reset pulse width is fixed at 50 ms on the ADM690/ADM692. On the ADM694 the watchdog timeout period is also 1.6 seconds but the reset pulse width is fixed at 200 ms. The ADM691/ADM693/ADM695 allow these times to be adjusted as shown in Table I. Figure 4 shows the various oscillator configurations which can be used to adjust the reset pulse width and watchdog timeout period.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100 ms watchdog timeout periods. With OSC IN connected high or floating, the 1.6 second timeout period is selected; while with it connected low, the 100 ms timeout period is selected. In either case, immediately after a reset, the timeout period is 1.6 seconds. This gives the microprocessor time to reinitialize the system. If OSC IN is low, then the 100 ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/0 port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70 ms.

Watchdog Output (WDO)

The Watchdog Output $\overline{WDO}$ (ADM691/ADM693/ADM695) provides a status output which goes low if the watchdog timer "times out" and remains low until set high by the next transition on the Watchdog Input. $\overline{WDO}$ is also set high when V_{CC} goes below the reset threshold.

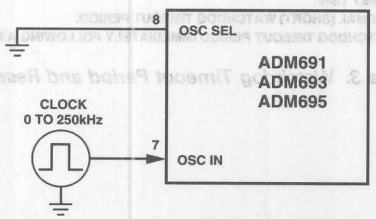


Figure 4a. External Clock Source

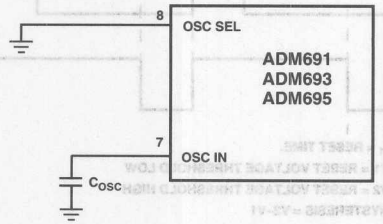


Figure 4b. External Capacitor

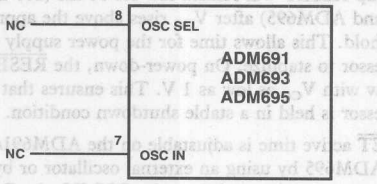


Figure 4c. Internal Oscillator (1.6 Second Watchdog)

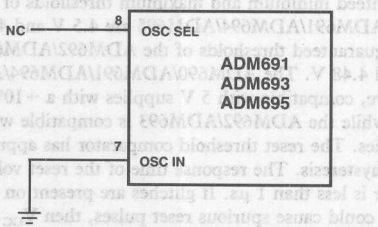


Figure 4d. Internal Oscillator (100 ms Watchdog)

$\overline{CE}$ Gating and RAM Write Protection (ADM691/ADM693/ADM695)

The ADM691/ADM693/ADM695 products include memory protection circuitry which ensures the integrity of data in memory by preventing write operations when V_{CC} is at an invalid level. There are two additional pins, $\overline{CE}_{IN}$ and $\overline{CE}_{OUT}$, which may be used to control the Chip Enable or Write inputs of CMOS RAM. When V_{CC} is present, $\overline{CE}_{OUT}$ is a buffered replica of $\overline{CE}_{IN}$, with a 5 ns propagation delay. When V_{CC} falls below the reset voltage threshold or V_{BATT}, an internal gate forces $\overline{CE}_{OUT}$ high, independent of $\overline{CE}_{IN}$.

$\overline{CE}_{OUT}$ typically drives the $\overline{CE}$, $\overline{CS}$, or write input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{CE}_{OUT}$ to drive the store or write inputs.

If the 5 ns typical propagation delay of $\overline{CE}_{OUT}$ is excessive, connect $\overline{CE}_{IN}$ to GND and use the resulting $\overline{CE}_{OUT}$ to control a high speed external logic gate.

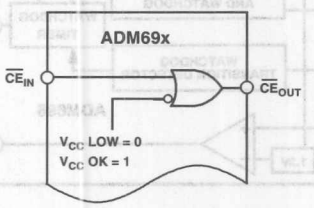


Figure 5. Chip Enable Gating

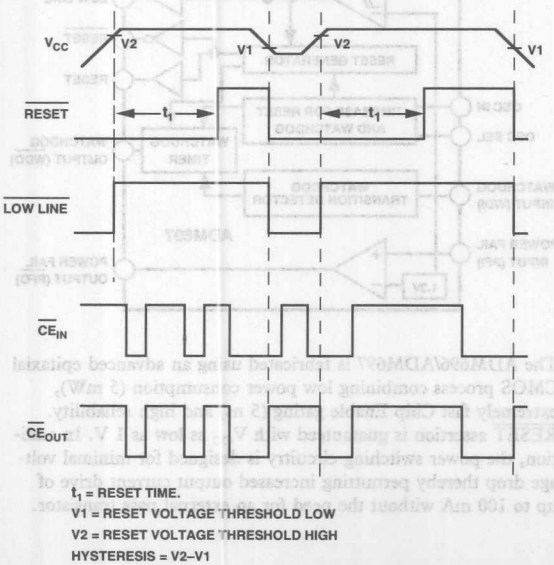


Figure 6. Chip Enable Timing

Power Fail Warning Comparator

An additional comparator is provided for early warning of failure in the microprocessor's power supply. The Power Fail Input (PFI) is compared to an internal +1.3 V reference. The Power Fail Output ($\overline{PFO}$) goes low when the voltage at PFI is less than 1.3 V. Typically PFI is driven by an external voltage divider which senses either the unregulated dc input to the system's 5 V regulator or the regulated 5 V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3 V several milliseconds before the +5 V power supply falls below the reset threshold. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM and the shut down procedure executed before power is lost.

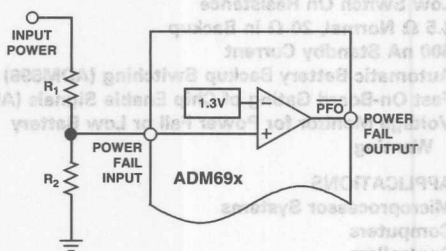


Figure 7. Power Fail Comparator

Table II. Input and Output Status In Battery Backup Mode

Signal	Status
V_{OUT}	V_{OUT} is connected to V_{BATT} via an internal PMOS switch.
$\overline{RESET}$	Logic low.
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low.
BATT ON	Logic high. The open circuit voltage is equal to V_{OUT}.
WDI	WDI is ignored. It is internally disconnected from the internal pull-up resistor and does not source or sink current as long as its input voltage is between GND and V_{OUT} The input voltage does not affect supply current.
$\overline{WDO}$	Logic high. The open circuit voltage is equal to V_{OUT}.
PFI	The Power Fail Comparator is turned off and has no effect on the Power Fail Output.
$\overline{PFO}$	Logic low.
$\overline{CE}_{IN}$	$\overline{CE}_{IN}$ is ignored. It is internally disconnected from its internal pull-up and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{CE}_{OUT}$	Logic high. The open circuit voltage is equal to V_{OUT}.
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.

15

ANALOG DEVICES

Microprocessor Supervisory Circuits

ADM696/ADM697

FEATURES

- Superior Upgrade for MAX696/MAX697
- Specified Over Temperature
- Adjustable Low Line Voltage Monitor
- Power OK/Reset Time Delay
- Reset Assertion Down to 1 V V_{CC}
- Watchdog Timer—100 ms, 1.6 s, or Adjustable
- Low Switch On Resistance
- 1.5 Ω Normal, 20 Ω in Backup
- 600 nA Standby Current
- Automatic Battery Backup Switching (ADM696)
- Fast On-Board Gating of Chip Enable Signals (ADM697)
- Voltage Monitor for Power Fail or Low Battery Warning

APPLICATIONS

- Microprocessor Systems
- Computers
- Controllers
- Intelligent Instruments
- Automotive Systems
- Critical μP Power Monitoring

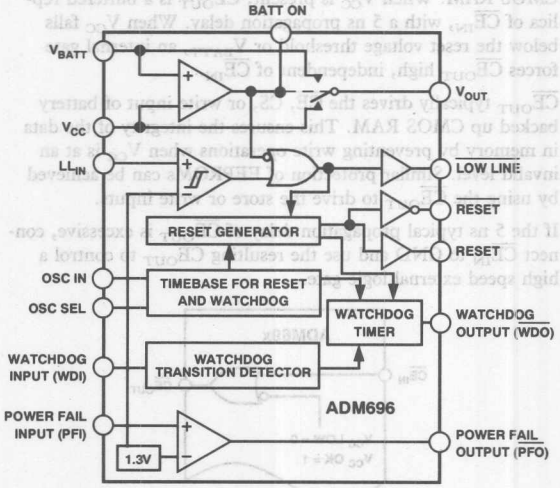
GENERAL DESCRIPTION

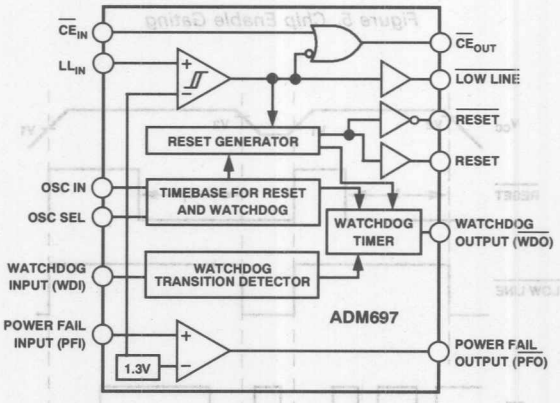
The ADM696/ADM697 supervisory circuits offer complete single chip solutions for power supply monitoring and battery control functions in microprocessor systems. These functions include μP reset, backup-battery switchover, watchdog timer, CMOS RAM write protection, and power failure warning.

The ADM696/ADM697 are available in 16-pin DIP and small outline packages and provide the following functions:

1. Power-On Reset output during power-up, power-down and brownout conditions. The RESET voltage threshold is adjustable using an external voltage divider. The $\overline{\text{RESET}}$ output remains operational with V_{CC} as low as 1 V.
2. A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
3. Separate watchdog timeout and low line status outputs.
4. Adjustable reset and watchdog timeout periods.
5. A 1.3 V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than V_{CC}.
6. Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic (ADM696).
7. Write protection of CMOS RAM or EEPROM (ADM697).

FUNCTIONAL BLOCK DIAGRAMS





The ADM696/ADM697 is fabricated using an advanced epitaxial CMOS process combining low power consumption (5 mW), extremely fast Chip Enable gating (5 ns) and high reliability. $\overline{\text{RESET}}$ assertion is guaranteed with V_{CC} as low as 1 V. In addition, the power switching circuitry is designed for minimal voltage drop thereby permitting increased output current drive of up to 100 mA without the need for an external pass transistor.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (V_{CC} = Full Operating Range, V_{BATT} = +2.8 V, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V_{CC} Operating Voltage Range	3.0		5.5	V	
V_{BATT} Operating Voltage Range	2.0		V_{CC} – 0.3	V	
BATTERY BACKUP SWITCHING (ADM696)					
V_{OUT} Output Voltage	V_{CC} – 0.05	V_{CC} – 0.025		V	I_{OUT} = 1 mA
	V_{CC} – 0.5	V_{CC} – 0.25		V	I_{OUT} ≤ 100 mA
V_{OUT} in Battery Backup Mode	V_{BATT} – 0.05	V_{BATT} – 0.02		V	I_{OUT} = 250 µA, V_{CC} < V_{BATT} – 0.2 V
Supply Current (excludes I_{OUT})		1	1.95	mA	I_{OUT} = 100 mA
Supply Current in Battery Backup Mode		0.6	1	µA	V_{CC} = 0 V, V_{BATT} = 2.8 V
Battery Standby Current					5.5 V > V_{CC} > V_{BATT} + 0.2 V
(+ = Discharge, – = Charge)	–0.1		+0.02	µA	T_A = +25°C
	–1		+0.02	µA	
Battery Switchover Threshold		70		mV	Power-Up
V_{CC} – V_{BATT}		50		mV	Power-Down
Battery Switchover Hysteresis		20		mV	
BATT ON Output Voltage			0.4	V	I_{SINK} = 1.6 mA
BATT ON Output Short Circuit Current		7		mA	BATT ON = V_{OUT} = 2.4 V Sink Current
	0.5	1	25	µA	BATT ON = V_{OUT}, V_{CC} = 0 V, Source Current
RESET AND WATCHDOG TIMER					
Low Line Threshold (LL_{IN})	1.25	1.3	1.35	V	V_{CC} = +5 V, +3 V
Reset Timeout Delay	35	50	70	ms	OSC SEL = HIGH, V_{CC} = 5 V, T_A = +25°C
Watchdog Timeout Period, Internal Oscillator	1.0	1.6	2.25	s	Long Period, V_{CC} = 5 V, T_A = +25°C
	70	100	140	ms	Short Period, V_{CC} = 5 V, T_A = +25°C
Watchdog Timeout Period, External Clock	4032		4097	Cycles	Long Period
	960		1025	Cycles	Short Period
Minimum WDI Input Pulse Width	50			ns	V_{IL} = 0.4, V_{IH} = 3.5 V, V_{CC} = 5 V
$\overline{RESET}$ Output Voltage @ V_{CC} = +1 V		4	200	mV	I_{SINK} = 10 µA, V_{CC} = 1 V
RESET, $\overline{RESET}$ Output Voltage			0.4	V	I_{SINK} = 400 µA, V_{CC} = 2 V, V_{BATT} = 0 V
			0.4	V	I_{SINK} = 1.6 mA, 3 V < V_{CC} < 5.5 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
$\overline{LOW\ LINE}$, $\overline{WDO}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA,
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
Output Short Circuit Source Current	1	3	25	µA	
WDI Input Threshold					V_{CC} = 5 V[1]
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		20	50	µA	WDI = V_{OUT}, (V_{CC}) T_A = +25°C
	–50	–15		µA	WDI = 0 V, T_A = +25°C
POWER FAIL DETECTOR					
PFI Input Threshold	1.2	1.3	1.4	V	V_{CC} = +3 V, +5 V
PFI–LL_{IN} Threshold Difference	–50	±15	+50	mV	V_{CC} = +3 V, +5 V
PFI Input Current	–25	±0.01	+25	nA	
LL_{IN} Input Current	–50	±0.01	+50	nA	
$\overline{PFO}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
$\overline{PFO}$ Short Circuit Source Current	1	3	25	µA	PFI = Low, $\overline{PFO}$ = 0 V
CHIP ENABLE GATING (ADM697)					
$\overline{CE}_{IN}$ Threshold			0.8	V	V_{IL}
	3.0			V	V_{IH}, V_{CC} = 5 V
$\overline{CE}_{IN}$ Pullup Current		3		µA	
$\overline{CE}_{OUT}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA
	V_{CC} – 0.5			V	I_{SOURCE} = 800 µA
$\overline{CE}$ Propagation Delay		5	25	ns	
OSCILLATOR					
OSC IN Input Current		±2		µA	
OSC SEL Input Pullup Current		5		µA	
OSC IN Frequency Range	0		250	kHz	OSC SEL = 0 V
OSC IN Frequency with Ext. Capacitor		4		kHz	OSC SEL = 0 V, C_{OSC} = 47 pF

NOTE

[1]WDI is a three-level input which is internally biased to 38% of V_{CC} and has an input impedance of approximately 125 kΩ.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} . . . . . −0.3 V to +6 V
V_{BATT} . . . . . −0.3 V to +6 V
All Other Inputs . . . . . −0.3 V to V_{OUT} + 0.5 V
Input Current
  V_{CC} . . . . . 200 mA
  V_{BATT} . . . . . 50 mA
  GND . . . . . 20 mA
Digital Output Current . . . . . 20 mA
Power Dissipation, N-16 DIP . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 135°C/W
Power Dissipation, Q-16 DIP . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 100°C/W
Power Dissipation, R-16 SOIC . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 110°C/W
Operating Temperature Range
  Industrial (A Version) . . . . . −40°C to +85°C
  Extended (S Version) . . . . . −55°C to +125°C
Lead Temperature (Soldering, 10 s) . . . . . +300°C
  Vapor Phase (60 s) . . . . . +215°C
  Infrared (15 s) . . . . . +220°C
Storage Temperature Range . . . . . −65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

CAUTION

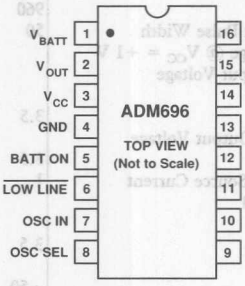
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD696/ADM697 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

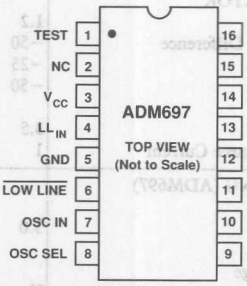
ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM696AN	−40°C to +85°C	N-16
ADM696AR	−40°C to +85°C	R-16
ADM696AQ	−40°C to +85°C	Q-16
ADM696SQ	−55°C to +125°C	Q-16
ADM697AN	−40°C to +85°C	N-16
ADM697AR	−40°C to +85°C	R-16
ADM697AQ	−40°C to +85°C	Q-16
ADM697SQ	−55°C to +125°C	Q-16

*For outline information see Package Information section.

PIN CONFIGURATIONS





PIN FUNCTION DESCRIPTION

Mnemonic	Pin No. ADM696	Pin No. ADM697	Function
V_{CC}	3	3	Power Supply Input +3 V to +5 V.
V_{BATT}	1	–	Backup Battery Input. Connect to Ground if a backup battery is not used.
V_{OUT}	2	–	Output Voltage, V_{CC} or V_{BATT} is internally switched to V_{OUT} depending on which is at the highest potential. V_{OUT} can supply up to 100 mA to power CMOS RAM. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	4	5	0 V. Ground reference for all signals.
$\overline{RESET}$	15	15	Logic Output. $\overline{RESET}$ goes low whenever LL_{IN} falls below 1.3 V or when V_{CC} falls below the V_{BATT} input voltage. $\overline{RESET}$ remains low for 50 ms after LL_{IN} goes above 1.3 V, $\overline{RESET}$ also goes low for 50 ms if the watchdog timer is enabled but not serviced within its timeout period. The $\overline{RESET}$ pulse width can be adjusted as shown in Table I.
WDI	11	11	Watchdog Input, WDI is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The timer resets with each transition at the WDI input. The watchdog timer is disabled when WDI is left floating or is driven to midsupply.
PFI	9	9	Power Fail Input. PFI is the noninverting input to the Power Fail Comparator when PFI is less than 1.3 V, PFO goes low. Connect PFI to GND or V_{OUT} when not used. See Figure 1.
$\overline{PFO}$	10	10	Power Fail Output. $\overline{PFO}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3 V. The comparator is turned off and $\overline{PFO}$ goes low when V_{CC} is below V_{BATT}.
$\overline{CE}_{IN}$	–	13	Logic Input. The input to the CE gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{CE}_{OUT}$	–	12	Logic Output. $\overline{CE}_{OUT}$ is a gated version of the $\overline{CE}_{IN}$ signal. $\overline{CE}_{OUT}$ tracks $\overline{CE}_{IN}$ when LL_{IN} is above 1.3 V. If LL_{IN} is below 1.3 V, $\overline{CE}_{OUT}$ is forced high.
BATT ON	5	–	Logic Output. BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 7 mA and can directly drive the base of an external PNP transistor to increase the output current above the 100 mA rating of V_{OUT}.
$\overline{LOW\ LINE}$	6	6	Logic Output. $\overline{LOW\ LINE}$ goes low when LL_{IN} falls below 1.3 V. It returns high as soon as LL_{IN} rises above 1.3 V
RESET	16	16	Logic Output. RESET is an active high output. It is the inverse of $\overline{RESET}$.
OSC SEL	8	8	Logic Oscillator Select Input. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3 μA internal pullup. See Table I and Figure 4.
OSC IN	7	7	Logic Oscillator Input. When OSC SEL is low, OSC IN can be driven by an external clock to adjust both the reset delay and the watchdog timeout period. The timing can also be adjusted by connecting an external capacitor to this pin. See Table I and Figure 4. When OSC SEL is high or floating, OSC IN selects between fast and slow watchdog timeout periods.
$\overline{WDO}$	14	14	Logic Output. The Watchdog Output, $\overline{WDO}$, goes low if WDI remains either high or low for longer than the watchdog timeout period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at midsupply, $\overline{WDO}$ remains high. $\overline{WDO}$ also goes high when $\overline{LOW\ LINE}$ goes low.
NC	12	2	No Connect. It should be left open.
LL_{IN}	13	4	Voltage Sensing Input. The voltage on the low line input, LLIN, is compared with a 1.3 V reference voltage. This input is normally used to monitor the power supply voltage. The output of the comparator generates a $\overline{LOW\ LINE}$ output signal. It also generates a RESET/$\overline{RESET}$ output.
TEST	–	1	This is a special test pin using during device manufacture. It should be connected to GND.

CIRCUIT INFORMATION

Battery-Switchover Section (ADM696)

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50 mV higher than V_{BATT} as V_{CC} falls, and when V_{CC} is 70 mV greater than V_{BATT} as V_{CC} rises. This 20 mV of hysteresis prevents repeated rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

During normal operation with V_{CC} higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via an internal PMOS transistor switch. This switch has a typical on resistance of 1.5 Ω and can supply up to 100 mA at the V_{OUT} terminal. V_{OUT} is normally used to drive a RAM memory bank which may require instantaneous currents of greater than 100 mA. If this is the case, then a bypass capacitor should be connected to V_{OUT}. The capacitor will provide the peak current transients to the RAM. A capacitance value of 0.1 µF or greater may be used.

If the continuous output current requirement at V_{OUT} exceeds 100 mA or if a lower V_{CC}–V_{OUT} voltage differential is desired, an external PNP pass transistor may be connected in parallel with the internal transistor. The BATT ON output can directly drive the base of the external transistor.

A 20 Ω MOSFET switch connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. The supply current in battery backup is typically 0.6 µA.

The ADM696 operates with battery voltages from 2.0 V to V_{CC} −0.3 V). High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term memory backup. A small charging current of typically 10 nA (0.1 µA max) flows out of the V_{BATT} terminal. This current is useful for maintaining rechargeable batteries in a fully charged condition. This extends the life of the backup battery by compensating for its self discharge current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum charging current (0.1 µA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, V_{BATT} should be connected to GND and V_{OUT} should be connected to V_{CC}.

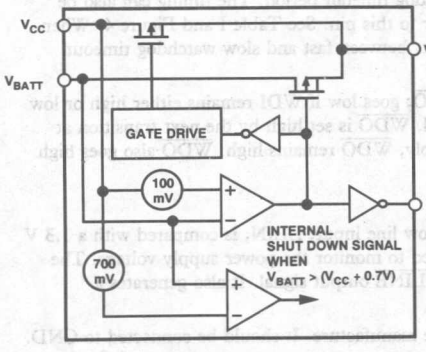


Figure 1. Battery Switchover Schematic

Low Line $\overline{\text{RESET}}$ OUTPUT

$\overline{\text{RESET}}$ is an active low output which provides a $\overline{\text{RESET}}$ signal to the microprocessor whenever the Low Line Input (LL_{IN}) is below 1.3 V. The LL_{IN} input is normally used to monitor the power supply voltage. An internal timer holds $\overline{\text{RESET}}$ low for 50ms after the voltage on LL_{IN} rises above 1.3 V. This is intended as a power-on $\overline{\text{RESET}}$ signal for the processor. It allows time for the power supply and microprocessor to stabilize. On power-down, the $\overline{\text{RESET}}$ output remains low with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition.

The LL_{IN} comparator has approximately 12 mV of hysteresis for enhanced noise immunity.

In addition to $\overline{\text{RESET}}$, an active high RESET output is also available. This is the complement of $\overline{\text{RESET}}$ and is useful for processors requiring an active high RESET.

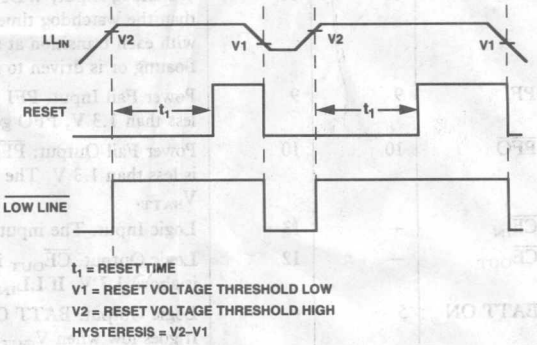


Figure 2. Power-Fail Reset Timing

Watchdog Timer $\overline{\text{RESET}}$

The watchdog timer circuit monitors the activity of the microprocessor in order to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the Watchdog Input (WDI) line. If this line is not toggled within the selected timeout period, a $\overline{\text{RESET}}$ pulse is generated. The ADM696/ADM697 may be configured for either a fixed "short" 100 ms or a "long" 1.6 second timeout period or for an adjustable timeout period. If the "short" period is selected some systems may be unable to service the watchdog timer immediately after a reset, so a "long" timeout is automatically initiated directly after a reset is issued. The watchdog timer is restarted at the end of Reset, whether the Reset was caused by lack of activity on WDI or by LL_{IN} falling below the reset threshold.

The normal (short) timeout period becomes effective following the first transition of WDI after $\overline{\text{RESET}}$ has gone inactive. The watchdog timeout period restarts with each transition on the WDI pin. To ensure that the watchdog timer does not time out, either a high-to-low or low-to high transition on the WDI pin must occur at or less than the minimum timeout period. If WDI remains permanently either high or low, reset pulses will be issued after each timeout period (1.6 s). The watchdog monitor can be deactivated by floating the Watchdog Input (WDI) or by connecting it to midsupply.

Table I. ADM696, ADM697 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Active Period
		Normal	Immediately After Reset	
Low	External Clock Input	1024 CLKS	4096 CLKS	512 CLKS
Low	External Capacitor	400 ms × C/47 pF	1.6 s × C/47 pF	200 ms × C/47 pF
Floating or High	Low	100 ms	1.6 s	50 ms
Floating or High	Floating or High	1.6 s	1.6 s	50 ms

NOTE
With the OSC SEL pin low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24 kHz. The nominal oscillator frequency with external capacitor is: F_{OSC} (Hz) = 184,000/C (pF).

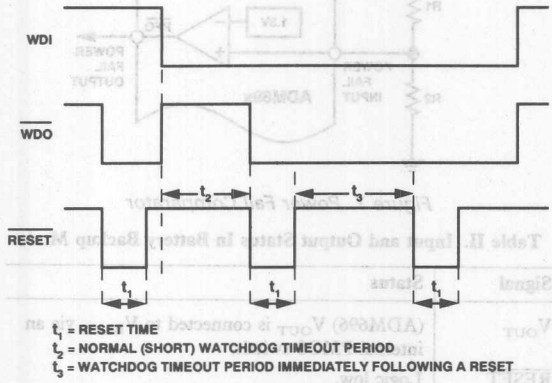


Figure 3. Watchdog Timeout Period and Reset Active Time

The watchdog timeout period defaults to 1.6 s and the reset pulse width defaults to 50 ms but these times to be adjusted as shown in Table I. Figure 4 shows the various oscillator configurations which can be used to adjust the reset pulse width and watchdog timeout period.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100 ms watchdog timeout periods. In either case, immediately after a reset the timeout period is 1.6 s. This gives the microprocessor time to reinitialize the system. If OSC IN is low, then the 100 ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70 ms.

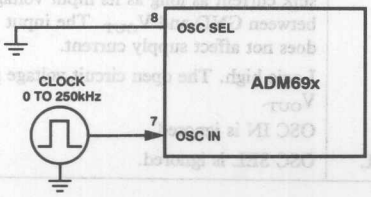


Figure 4a. External Clock Source

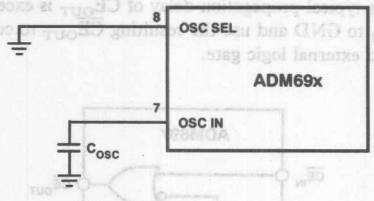


Figure 4b. External Capacitor

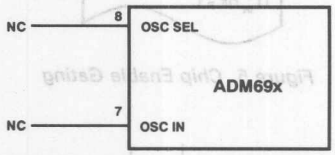


Figure 4c. Internal Oscillator (1.6 s Watchdog)

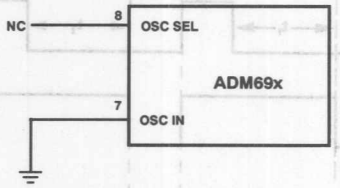


Figure 4d. Internal Oscillator (100 ms Watchdog)

Watchdog Output ($\overline{WDO}$)
The Watchdog Output $\overline{WDO}$ provides a status output which goes low if the watchdog timer "times out" and remains low until set high by the next transition on the watchdog input. $\overline{WDO}$ is also set high when LL_{IN} goes below the reset threshold.

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CE Gating and RAM Write Protection (ADM697)
The ADM697 contains memory protection circuitry which ensures the integrity of data in memory by preventing write operations when LL_{IN} is below the threshold voltage. When LL_{IN} is greater than 1.3 V, $\overline{CE}_{OUT}$ is a buffered replica of $\overline{CE}_{IN}$, with a 5 ns propagation delay. When LL_{IN} falls below the 1.3 V threshold, an internal gate forces $\overline{CE}_{OUT}$ high, independent of $\overline{CE}_{IN}$.

$\overline{CE}_{OUT}$ typically drives the CE, CS, or Write input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level.

If the 5 ns typical propagation delay of $\overline{CE}_{OUT}$ is excessive, connect $\overline{CE}_{IN}$ to GND and use the resulting $\overline{CE}_{OUT}$ to control a high speed external logic gate.

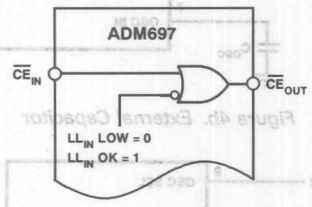


Figure 5. Chip Enable Gating

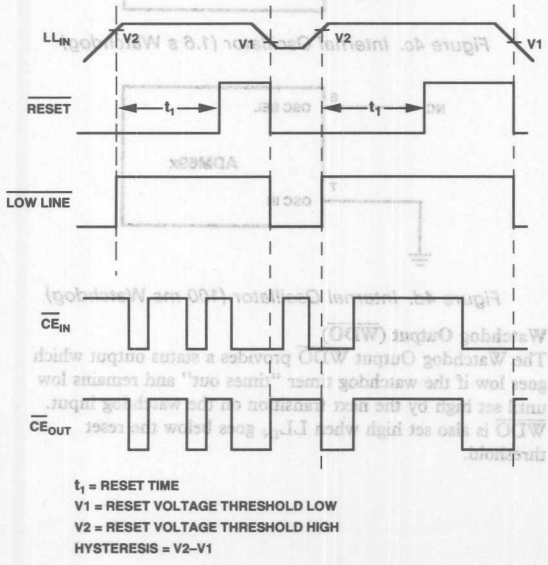


Figure 6. Chip Enable Timing

Power Fail Warning Comparator
An additional comparator is provided for early warning of failure in the microprocessor's power supply. The Power Fail Input (PFI) is compared to an internal +1.3 V reference. The Power Fail Output ($\overline{PFO}$) goes low when the voltage at PFI is less than 1.3 V. Typically PFI is driven by an external voltage divider which senses either the unregulated dc input to the system's 5 V regulator or the regulated 5 V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3 V several milliseconds before the +5 V power supply falls below the reset threshold. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM and the shut-down procedure executed before power is lost.

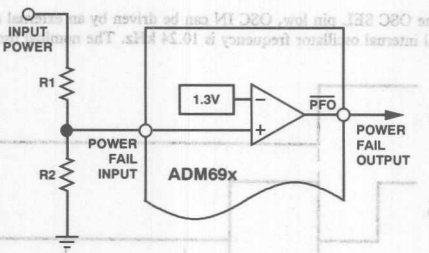


Figure 7. Power Fail Comparator

Table II. Input and Output Status In Battery Backup Mode

Signal	Status
V_{OUT}	(ADM696) V_{OUT} is connected to V_{BATT} via an internal PMOS switch.
$\overline{RESET}$	Logic low.
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low.
BATT ON	(ADM696) Logic high. The open circuit voltage is equal to V_{OUT}.
WDI	WDI is ignored. It is internally disconnected from the internal pullup resistor and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{WDO}$	Logic high. The open circuit voltage is equal to V_{OUT}.
PFI	The Power Fail Comparator is turned off and has no effect on the Power Fail Output.
$\overline{PFO}$	Logic low.
$\overline{CE}_{IN}$	$\overline{CE}_{IN}$ is ignored. It is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{CE}_{OUT}$	Logic high. The open circuit voltage is equal to V_{OUT}.
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.

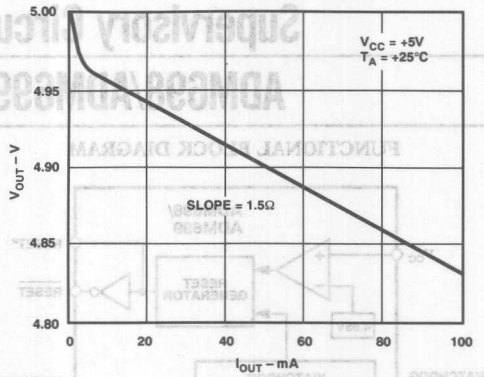


Figure 8. V_{OUT} vs. I_{OUT} Normal Operation

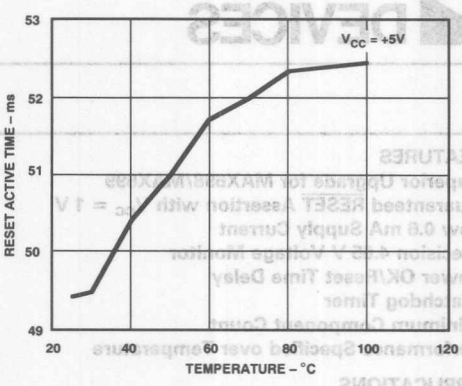


Figure 11. RESET Active Time vs. Temperature

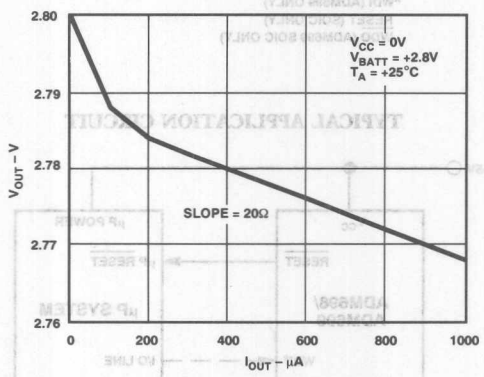


Figure 9. V_{OUT} vs. Battery Backup

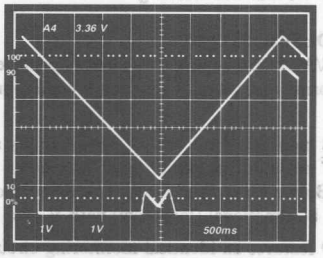


Figure 12. RESET Output Voltage vs. Supply Voltage

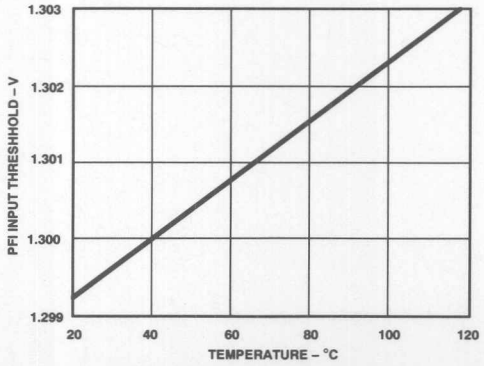


Figure 10. PFI Input Threshold vs. Temperature

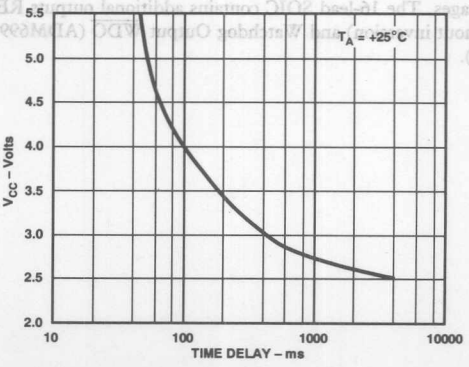


Figure 13. $\overline{RESET}$ Timeout Delay vs. V_{CC}

15

FEATURES

Superior Upgrade for MAX698/MAX699
Guaranteed $\overline{\text{RESET}}$ Assertion with V_{CC} = 1 V
Low 0.6 mA Supply Current
Precision 4.65 V Voltage Monitor
Power OK/Reset Time Delay
Watchdog Timer
Minimum Component Count
Performance Specified over Temperature

APPLICATIONS

Microprocessor Systems
Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

GENERAL DESCRIPTION

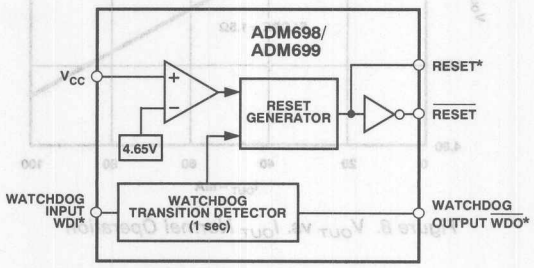
The ADM698/ADM699 supervisory circuits provide power supply monitoring and watchdog timing for microprocessor systems.

The ADM698 monitors the 5 V V_{CC} power supply and generates a $\overline{\text{RESET}}$ pulse during power up, power down and during low voltage "Brown Out" conditions. The $\overline{\text{RESET}}$ output is guaranteed to be functional (logic low) with V_{CC} as low as 1 V.

The ADM699 features an identical monitoring circuit as in the ADM698 plus an additional watchdog timer input to monitor microprocessor activity. The $\overline{\text{RESET}}$ output is forced low if the watchdog input is not toggled within the 1 second watchdog timeout period.

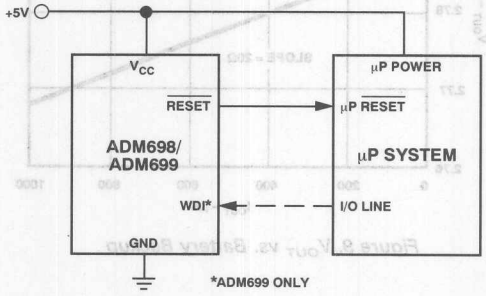
Both parts are available in 8-pin plastic DIP and 16-lead SOIC packages. The 16-lead SOIC contains additional outputs RESET (without inversion) and Watchdog Output $\overline{\text{WDO}}$ (ADM699 only).

FUNCTIONAL BLOCK DIAGRAM



*WDI (ADM699 ONLY)
RESET (SOIC ONLY)
WDO (ADM699 SOIC ONLY)

TYPICAL APPLICATION CIRCUIT



*ADM699 ONLY

SPECIFICATIONS (V_{CC} = +5 V ± 10%, T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V_{CC} Operating Voltage Range	3.0		5.5	V	
Supply Current		0.6	1.95	mA	
Power-Down Reset Assertion	4.5	4.65	4.73	V	
Power-Up Reset Deassertion			4.73	V	
Reset Threshold Hysteresis		40		mV	
Reset Active Time	140	200	280	ms	T_A = +25°C, V_{CC} = +5 V
Watchdog Timeout Period (ADM699)	1.0	1.6	2.25	s	T_A = +25°C, V_{CC} = +5 V
Minimum WDI Input Pulse Width	50			ns	V_{IL} = 0.4, V_{IH} = 3.5 V
$\overline{\text{RESET}}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 4.4 V
$\overline{\text{RESET}}$ Output Voltage (V_{CC} = 1 V)		4	200	mV	I_{SINK} = 10 µA, V_{CC} = 1.0 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
RESET and $\overline{\text{WDO}}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 5 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 4.4 V
$\overline{\text{RESET}}$ Output Short Circuit Current		25		mA	Output Sink Current
WDI Input Threshold (ADM699)					
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		20	50	µA	WDI = V_{CC}, T_A = +25°C
	−50	−20		µA	WDI = 0 V, T_A = +25°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} . . . . . −0.3 V to +6 V
All Other Inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Power Dissipation 8-Pin DIP . . . . . 500 mW
  θ_{JA}, Thermal Impedance . . . . . +120°C/W
Power Dissipation 16-Pin SOIC . . . . . 375 mW
  θ_{JA}, Thermal Impedance . . . . . +110°C/W
Power Dissipation 8-Pin Cerdip . . . . . 500 mW
  θ_{JA}, Thermal Impedance . . . . . +125°C/W
Operating Temperature Range
  Industrial (A Version) . . . . . −40°C to +85°C
  Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
  Vapor Phase (60 secs) . . . . . +215°C
  Infrared (15 secs) . . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM698AN	−40°C to +85°C	N-8
ADM698AR	−40°C to +85°C	R-16
ADM698AQ	−40°C to +85°C	Q-8
ADM698SQ	−55°C to +125°C	Q-8
ADM699AN	−40°C to +85°C	N-8
ADM699AR	−40°C to +85°C	R-16
ADM699AQ	−40°C to +85°C	Q-8
ADM699SQ	−55°C to +125°C	Q-8

*For outline information see Package Information section.

15

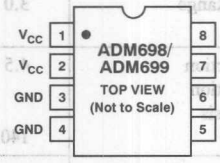
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM698/ADM699 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

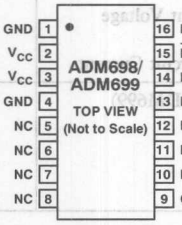
Mnemonic	Function
V_{CC}	+5 V Power Supply Input.
GND	0 V. Ground reference for all signals.
$\overline{\text{RESET}}$	Logic Output. $\overline{\text{RESET}}$ goes low whenever V_{CC} falls below the reset voltage threshold (4.65 V typ). $\overline{\text{RESET}}$ remains low for a minimum of 140 ms after V_{CC} returns to 5 V. $\overline{\text{RESET}}$ also goes low for a minimum of 140 ms if the watchdog timer is enabled but not serviced within its timeout period.
WDI	Watchdog Input. WDI is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{\text{RESET}}$ pulses low and $\overline{\text{WDO}}$ goes low. The timer resets with each transition on the WDI line. The watchdog timer may be disabled if WDI is left floating or is driven to midsupply.
RESET	(SOIC packages only) Logic Output. RESET is an active high output. It is the inverse of $\overline{\text{RESET}}$.
$\overline{\text{WDO}}$	(SOIC ADM699 only) Logic Output. The Watchdog Output, $\overline{\text{WDO}}$, goes low if WDI remains either high or low for longer than the watchdog timeout period. $\overline{\text{WDO}}$ is set high by the next transition at WDI. If WDI is unconnected or at midsupply, the watchdog timer is disabled and $\overline{\text{WDO}}$ remains high.

PIN CONFIGURATION (DIP)



*( ) ADM699 ONLY

PIN CONFIGURATION (SOIC)



*( ) ADM699 ONLY

TYPICAL PERFORMANCE CURVES

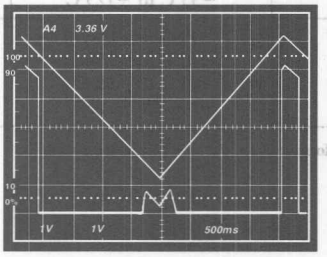


Figure 1. RESET Output Voltage vs. V_{CC}

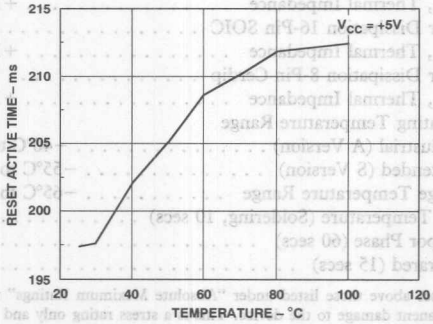


Figure 2. RESET Active Time vs. Temperature

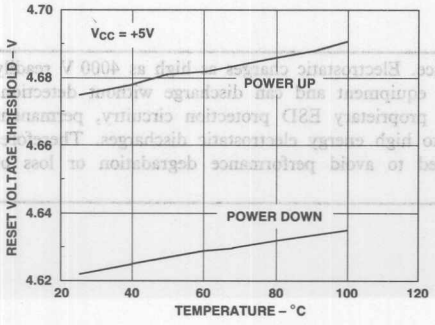


Figure 3. RESET Voltage Threshold vs. Temperature

CIRCUIT INFORMATION

Power Fail RESET

A precision voltage detector monitors V_{CC} and generates a $\overline{RESET}$ output to hold the microprocessor's Reset line low when V_{CC} falls below the reset threshold (4.65 V) (see Figure 4). The reset voltage threshold is set to accommodate a 5% variation on V_{CC}. The voltage detector has 40 mV hysteresis to ensure that glitches on V_{CC} do not activate the $\overline{RESET}$ output.

On power up, an internal monostable holds $\overline{RESET}$ low for 140 ms after V_{CC} rises above the reset threshold. This allows the power supply to stabilize on power up and also prevents repeated toggling of $\overline{RESET}$ even if the 5 V power drops out and recovers with each power line cycle. In order to prevent mistriggering due to transient voltage spikes, it is recommended that a 0.1 μF capacitor be connected at the V_{CC} pin.

The $\overline{RESET}$ output is guaranteed to remain low with V_{CC} as low as 1 V. This holds the microprocessor in a stable shutdown condition as the power supply comes up.

On the 16-lead SOIC package, an active high RESET output is also provided. This is the complement of $\overline{RESET}$ and is intended for microprocessors requiring an active high signal.

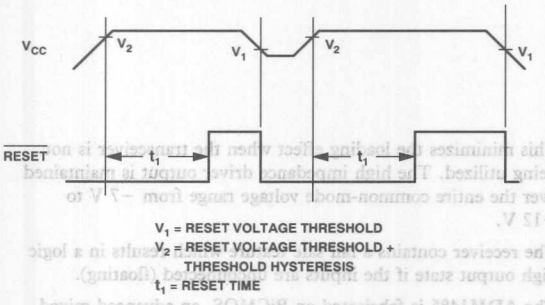


Figure 4. Watchdog Timeout Period vs. Temperature

Watchdog Timer (ADM699 Only)

The watchdog timer input (WDI) monitors an I/O line from the μP system. The μP must toggle this input once every 1.6 seconds to verify correct software execution. Failure to toggle the line indicates that the μP system is not correctly executing its program and may be tied up in an endless loop. If this happens, a reset pulse is generated to initialize the processor.

The WDI input is a three level input and will recognize a low-to- high or a high-to-low transition on its input. The watchdog timer is reset by each WDI transition and then begins its time-out period. If the WDI pin remains either high or low, reset pulses will be issued every 1.6 seconds typically. If the watchdog timer is not needed, the WDI input should be left floating.

The Watchdog Output ($\overline{WDO}$) (SOIC package Only) provides watchdog status information. It is driven low if WDI is not toggled within the watchdog timeout period. It goes high at the next WDI transition. It is also set high when V_{CC} falls below the reset threshold.

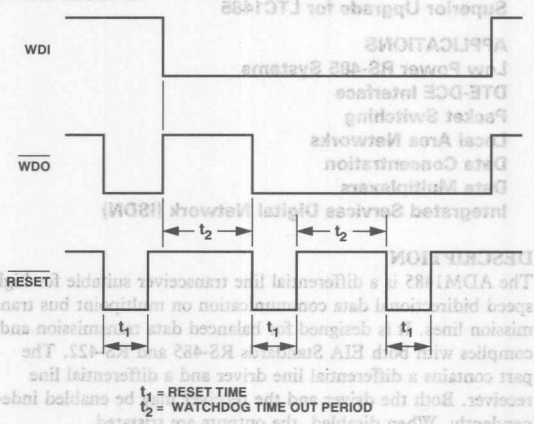


Figure 5. Watchdog Timeout Period and Reset Active Time

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ADM1485

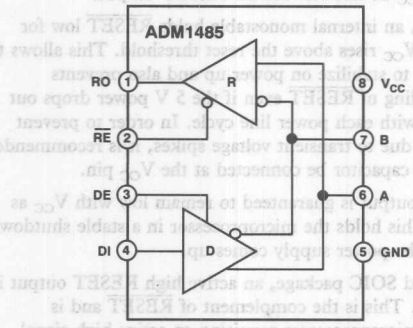
FEATURES

Meets EIA RS-485 Standard
30 Mb/s Data Rate
Single +5 V Supply
−7 V to +12 V Bus Common-Mode Range
High Speed, Low Power BiCMOS
Thermal Shutdown Protection
Short Circuit Protection
Zero Skew Driver
Driver Propagation Delay: 10 ns
Receiver Propagation Delay: 25 ns
High Z Outputs with Power Off
Superior Upgrade for LTC1485

APPLICATIONS

Low Power RS-485 Systems
DTE-DCE Interface
Packet Switching
Local Area Networks
Data Concentration
Data Multiplexers
Integrated Services Digital Network (ISDN)

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The ADM1485 is a differential line transceiver suitable for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced data transmission and complies with both EIA Standards RS-485 and RS-422. The part contains a differential line driver and a differential line receiver. Both the driver and the receiver may be enabled independently. When disabled, the outputs are tristated.

The ADM1485 operates from a single +5 V power supply. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if during fault conditions a significant temperature increase is detected in the internal driver circuitry.

Up to 32 transceivers may be connected simultaneously on a bus, but only one driver should be enabled at any time. It is important therefore that the remaining disabled drivers do not load the bus. To ensure this, the ADM1485 driver features high output impedance when disabled and also when powered down. This minimizes the loading effect when the transceiver is not being utilized. The high impedance driver output is maintained over the entire common-mode voltage range from −7 V to +12 V.

The receiver contains a fail safe feature which results in a logic high output state if the inputs are unconnected (floating).

The ADM1485 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology. All inputs and outputs contain protection against ESD; all driver outputs feature high source and sink current capability. An epitaxial layer is used to guard against latch-up.

The ADM1485 features extremely fast switching speeds. Minimal driver propagation delays permit transmission at data rates up to 30 Mbits/s while low skew minimizes EMI interference.

The part is fully specified over the commercial and industrial temperature range and is available in an 8-pin DIL/ SOIC package.

SPECIFICATIONS (V_{CC} = +5 V ± 5%. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}			5.0	V	R = ∞, Figure 1
	2.0		5.0	V	V_{CC} = 5 V, R = 50 Ω (RS-422), Figure 1
	1.5		5.0	V	R = 27 Ω (RS-485), Figure 1
V_{OD3}	1.5		5.0	V	V_{TST} = −7 V to +12 V, Figure 2
$\Delta\|V_{OD}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, Figure 1
Common-Mode Output Voltage V_{OC}			3	V	R = 27 Ω or 50 Ω, Figure 1
$\Delta\|V_{OC}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω
Output Short Circuit Current (V_{OUT} = High)	35		250	mA	−7 V ≤ V_O ≤ +12 V
Output Short Circuit Current (V_{OUT} = Low)	35		250	mA	−7 V ≤ V_O ≤ +12 V
CMOS Input Logic Threshold Low, V_{INL}			0.8	V	
CMOS Input Logic Threshold High, V_{INH}	2.0			V	
Logic Input Current (DE, DI)			±1.0	μA	
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	−0.2		+0.2	V	−7 V ≤ V_{CM} ≤ +12 V
Input Voltage Hysteresis, ΔV_{TH}		70		mV	V_{CM} = 0 V
Input Resistance	12			kΩ	−7 V ≤ V_{CM} ≤ +12 V
Input Current (A, B)			+1	mA	V_{IN} = 12 V
			−0.8	mA	V_{IN} = −7 V
Logic Enable Input Current ($\overline{RE}$)			±1	μA	
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = +4.0 mA
CMOS Output Voltage High, V_{OH}	4.0			V	I_{OUT} = −4.0 mA
Short Circuit Output Current	7		85	mA	V_{OUT} = GND or V_{CC}
Tristate Output Leakage Current			±1.0	μA	0.4 V ≤ V_{OUT} ≤ +2.4 V
POWER SUPPLY CURRENT					
I_{CC} (Outputs Enabled)		1.35	2.2	mA	Outputs Unloaded, Digital Inputs = GND or V_{CC}
I_{CC} (Outputs Disabled)		0.7	1	mA	Outputs Unloaded, Digital Inputs = GND or V_{CC}

Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{CC} = +5 V ± 5%. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/ Comments
DRIVER					
Propagation Delay Input to Output T_{PLH}, T_{PHL}	2	10	15	ns	R_L Diff = 54 Ω C_{L1} = C_{L2} = 100 pF, Figure 3
Driver O/P to $\overline{O/P}$ T_{SKEW}		0	5	ns	R_L Diff = 54 Ω C_{L1} = C_{L2} = 100 pF, Figure 3
Driver Rise/Fall Time T_R, T_F		2	10	ns	R_L Diff = 54 Ω C_{L1} = C_{L2} = 100 pF, Figure 3
Driver Enable to Output Valid		10	25	ns	
Driver Disable Timing		10	25	ns	
RECEIVER					
Propagation Delay Input to Output T_{PLH}, T_{PHL}	18	25	40	ns	C_L = 15 pF, Figure 5
Skew $\|T_{PLH}-T_{PHL}\|$		0	5	ns	
Receiver Enable T_{EN1}		15	25	ns	Figure 6
Receiver Disable T_{EN2}		15	25	ns	Figure 6

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{CC} . . . . . +7 V
Inputs
Driver Input (DI) . . . . . −0.3 V to V_{CC} + 0.3 V
Control Inputs (DE, RE) . . . . . −0.3 V to V_{CC} + 0.3 V
Receiver Inputs (A, B) . . . . . −14 V to +14 V
Outputs
Driver Outputs . . . . . −14 V to +14 V
Receiver Output . . . . . −0.5 V to V_{CC} + 0.5 V
Power Dissipation 8-Pin DIP . . . . . 500 mW
θ_{JA}, Thermal Impedance . . . . . +130°C/W
Power Dissipation 8-Pin SOIC . . . . . 450 mW
θ_{JA}, Thermal Impedance . . . . . +170°C/W
Power Dissipation 8-Pin Cerdip . . . . . 500 mW
θ_{JA}, Thermal Impedance . . . . . +125°C/W
Operating Temperature Range
Commercial (J Version) . . . . . 0°C to +70°C
Industrial (A Version) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Vapour Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

Table I. Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
X	0	X	Z	Z

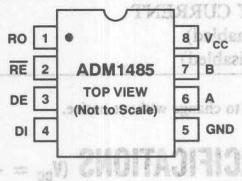
Table II. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2 V	1
0	0	≤ −0.2 V	0
0	0	Inputs Open	1
1	0	X	Z

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1	RO	Receiver Output. When enabled if A > B by 200 mV, then RO = High. If A < B by 200 mV, then RO = Low.
2	$\overline{RE}$	Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state.
3	DE	Driver Output Enable. A high level enables the driver differential outputs, A and B. A low level places it in a high impedance state.
4	DI	Driver Input. When the driver is enabled a logic Low on DI forces A low and B high while a logic High on DI forces A high and B low.
5	GND	Ground Connection, 0 V.
6	A	Noninverting Receiver Input A/Driver Output A.
7	B	Inverting Receiver Input B/Driver Output B.
8	V_{CC}	Power Supply, 5 V ± 5%.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM1485JN	0°C to +70°C	N-8
ADM1485JR	0°C to +70°C	R-8
ADM1485AN	−40°C to +85°C	N-8
ADM1485AR	−40°C to +85°C	R-8
ADM1485AQ	−40°C to +85°C	Q-8

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM1485 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Test Circuits

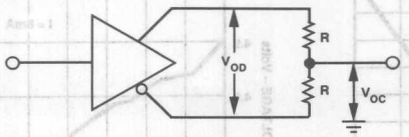


Figure 1. Driver Voltage Measurement Test Circuit

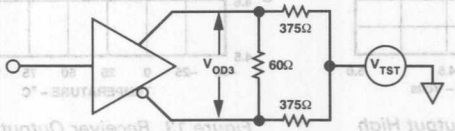


Figure 2. Driver Voltage Measurement Test Circuit 2

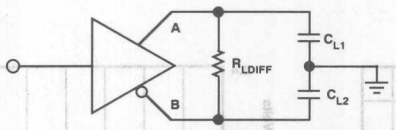


Figure 3. Driver Propagation Delay Test Circuit

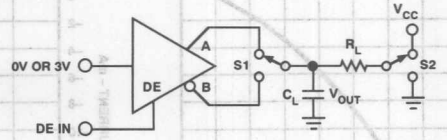


Figure 4. Driver Enable/Disable Test Circuit

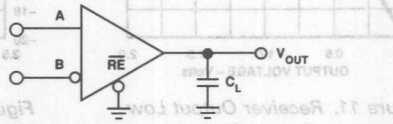


Figure 5. Receiver Propagation Delay Test Circuit

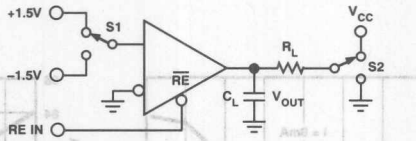


Figure 6. Receiver Enable/Disable Test Circuit

Switching Characteristics

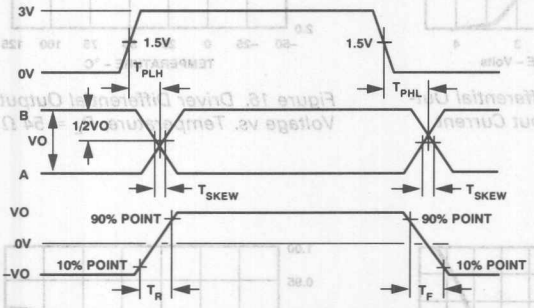


Figure 7. Driver Propagation Delay, Rise/Fall Timing

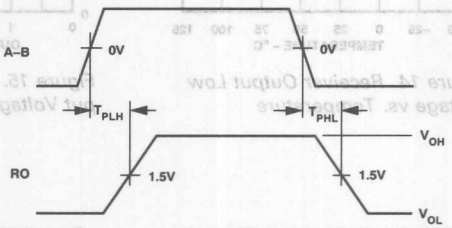


Figure 9. Receiver Propagation Delay

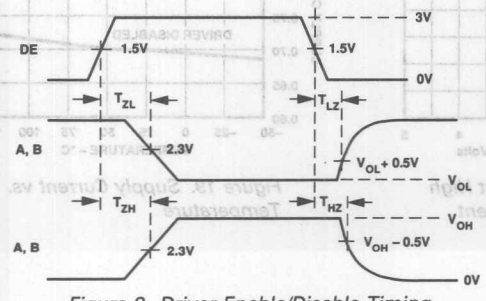


Figure 8. Driver Enable/Disable Timing

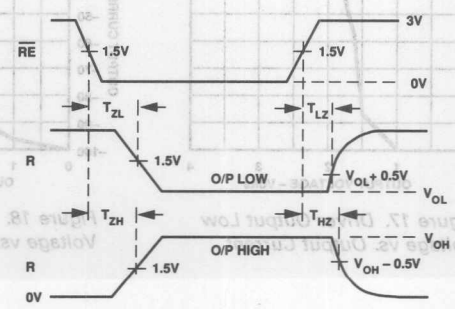


Figure 10. Receiver Enable/Disable Timing

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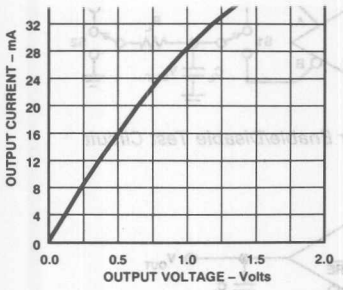

Figure 11. Receiver Output Low Voltage vs. Output Current

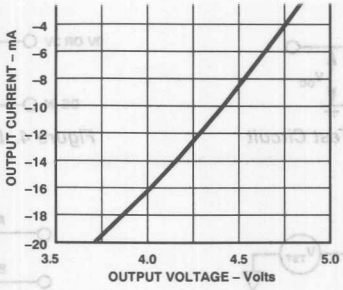

Figure 12. Receiver Output High Voltage vs. Output Current

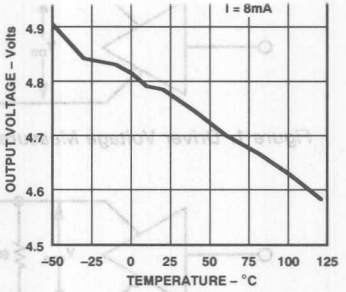

Figure 13. Receiver Output High Voltage vs. Temperature

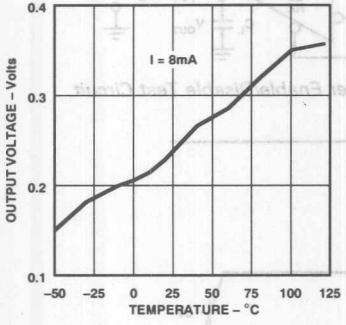

Figure 14. Receiver Output Low Voltage vs. Temperature

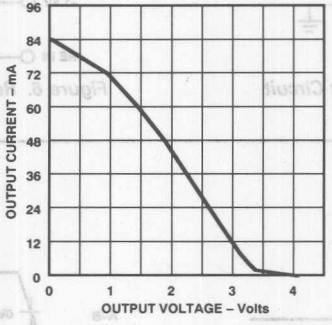

Figure 15. Driver Differential Output Voltage vs. Output Current

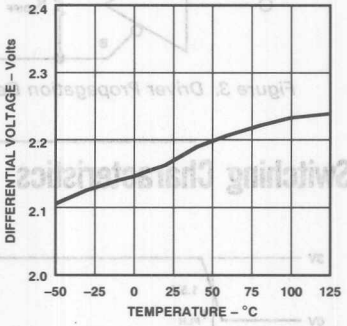

Figure 16. Driver Differential Output Voltage vs. Temperature, R_L = 54 Ω

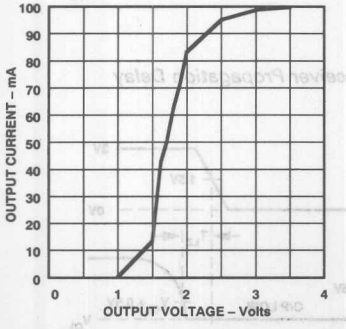

Figure 17. Driver Output Low Voltage vs. Output Current

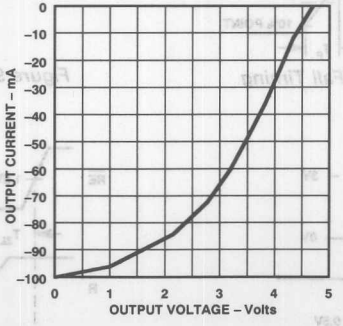

Figure 18. Driver Output High Voltage vs. Output Current

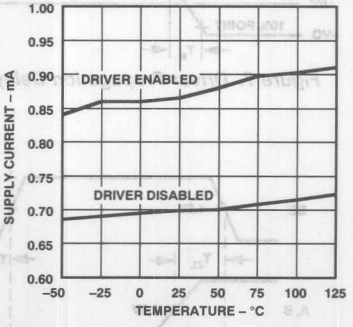

Figure 19. Supply Current vs. Temperature

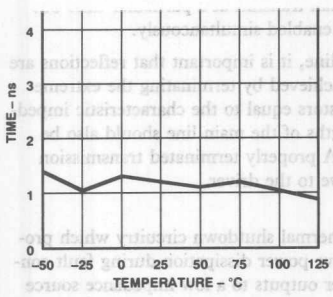

Figure 20. Receiver t_{PLH}–t_{PHL} vs. Temperature

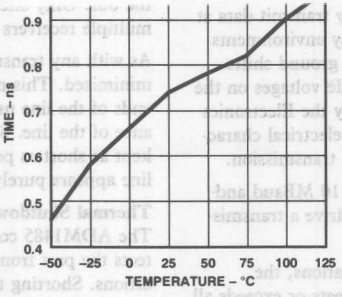

Figure 21. Driver Skew vs. Temperature

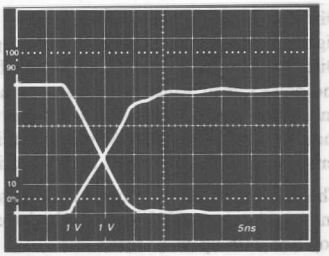

Figure 22. Unloaded Driver Differential Outputs

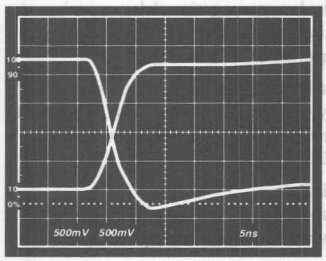

Figure 23. Loaded Driver Differential Outputs

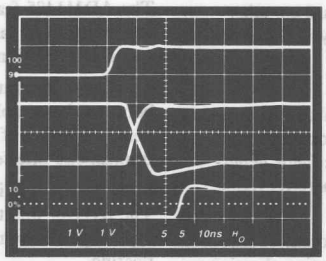

Figure 24. Driver/Receiver Propagation Delays Low to High

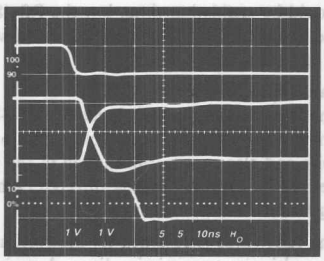

Figure 25. Driver/Receiver Propagation Delays High to Low

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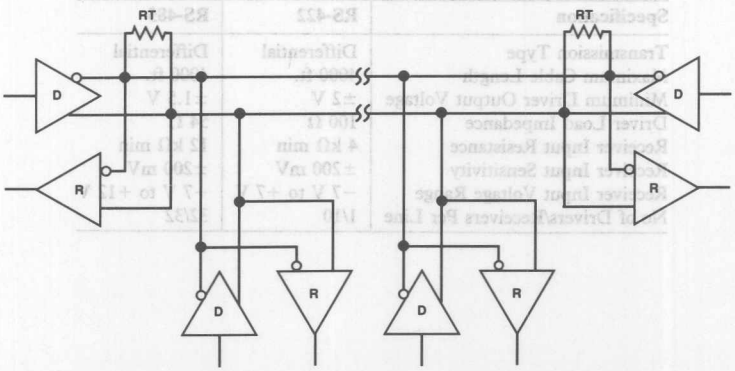


Figure 26. Typical RS-485 Network

APPLICATIONS INFORMATION

Differential Data Transmission

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals which appear as common-mode voltages on the line. There are two main standards approved by the Electronics Industries Association (EIA) which specify the electrical characteristics of transceivers used in differential data transmission.

The RS-422 standard specifies data rates up to 10 MBaud and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.

In order to cater for true multipoint communications, the RS-485 standard was defined. This standard meets or exceeds all the requirements of RS-422 but also allows for up to 32 drivers and 32 receivers to be connected to a single bus. An extended common-mode range of −7 V to +12 V is defined. The most significant difference between RS-422 and RS-485 is the fact that the drivers may be disabled thereby allowing more than one (32 in fact) to be connected to a single line. Only one driver should be enabled at time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

Cable and Data Rate

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby, reducing the effective inductance of the pair.

The ADM1485 is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 26. An RS-485 transmission line can have as many as 32 transceivers on the bus. Only one driver can transmit at a particular time but multiple receivers may be enabled simultaneously.

As with any transmission line, it is important that reflections are minimized. This may be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

Thermal Shutdown

The ADM1485 contains thermal shutdown circuitry which protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature and disables the driver outputs. The thermal sensing circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at 140°C.

Propagation Delay

The ADM1485 features very low propagation delay ensuring maximum baud rate operation. The driver is well balanced ensuring distortion free transmission.

Another important specification is a measure of the skew between the complementary outputs. Excessive skew impairs the noise immunity of the system and increases the amount of electromagnetic interference (EMI).

Receiver Open-Circuit Fail Safe

The receiver input includes a fail-safe feature which guarantees a logic high on the receiver when the inputs are open circuit or floating.

Table III. Comparison of RS-422 and RS-485 Interface Standards

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Cable Length	4000 ft.	4000 ft.
Minimum Driver Output Voltage	±2 V	±1.5 V
Driver Load Impedance	100 Ω	54 Ω
Receiver Input Resistance	4 kΩ min	12 kΩ min
Receiver Input Sensitivity	±200 mV	±200 mV
Receiver Input Voltage Range	−7 V to +7 V	−7 V to +12 V
No of Drivers/Receivers Per Line	1/10	32/32

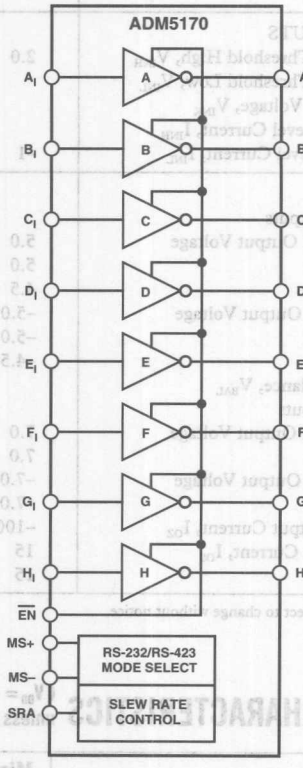
Octal, RS-232/RS-423 Line Driver

ADM5170

FEATURES
- Eight Single Ended Line Drivers in One Package
- Meets EIA Standard RS-232E, RS-423A and CCITT V.10/X.26
- Resistor Programmable Slew Rate
- Wide Supply Voltage Range
- Low Power CMOS
- 3-State Outputs
- TTL/CMOS Compatible Inputs
- Output Short Circuit Protection
- Available in 28-Pin DIP/PLCC
- Low Power Replacement for UC5170C

APPLICATIONS
- High Speed Communication
- Computer I-O Ports Peripherals
- High Speed Modems
- Printers
- Logic Level Translation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM5170 is an octal line driver suitable for digital communication systems with data rates up to 116 kB/s. Input TTL or CMOS signal levels are inverted and translated into either EIA RS-232E or RS-423A signal levels depending on the status of the Mode Select inputs MS+ and MS–. With both Mode Select inputs at GND, RS-423 operation is selected while with MS+ connected to V_{DD} and MS– connected to V_{SS}, RS-232 operation is selected.

The output slew rates may be controlled using an external resistor connected between the SRA (Slew Rate Adjust) pin and GND. Resistor values between 2 kΩ and 10 kΩ may be selected giving a slew rate which can be adjusted from 10 V/µs to 2.2 V/µs. This adjustment of the slew rate allows tailoring of the output characteristics to suit the interface cable being used.

The outputs may be disabled using the $\overline{EN}$ (Enable Input). This feature permits sharing of a common output line.

The ADM5170 is fabricated on an advanced CMOS process featuring low power consumption. In the disabled state the power consumption reduces from 500 mW to 40 mW. The ADM5170 is available in both 28-pin DIP and 28-lead PLCC packages.

Truth Table

Inputs $\overline{EN}$	Data	Outputs EIA RS-232E[1]	RS-423A
0	0	(V_{DD} – 3 V)	5 V to 6 V
0	1	(V_{SS} – 3 V)	–5 V to –6 V
1	X	High Z	High Z

[1]Minimum Output Level

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ADM5170–SPECIFICATIONS

(V_{DD} = +10 V ± 10%, V_{SS} = –10 V ± 10% V, MS+ = MS– = 0 V, R_{SRA} = 10 kΩ. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD} Range	9		15	V	
V_{SS} Range	–9		–15	V	
I_{DD} (Disabled)		2	4	mA	$\overline{EN}$ = High,
I_{DD} (Enabled)		25	36	mA	R_L = ∞, $\overline{EN}$ = 0 V
I_{SS} (Disabled)		–2	–4	mA	$\overline{EN}$ = High
I_{SS} (Enabled)		–23	–36	mA	R_L = ∞, $\overline{EN}$ = 0 V
DIGITAL INPUTS					
Input Logic Threshold High, V_{INH}	2.0			V	
Input Logic Threshold Low, V_{INL}			0.8	V	
Input Clamp Voltage, V_{INK}		–1.1	–1.8	V	I_{IN} = –15 mA
Input High Level Current, I_{INH}			1	µA	V_{INH} = 2.4 V
Input Low Level Current, I_{INL}	–1			µA	V_{INL} = 0.4 V
OUTPUTS					
RS-423A Outputs					$\overline{EN}$ = 0.8 V, MS+ = MS– = 0 V
High Level Output Voltage	5.0	5.3	6.0	V	R_L = ∞, V_{IN} = 0.8 V
	5.0	5.3	6.0	V	R_L = 3 kΩ, V_{IN} = 0.8 V
	4.5	5.2	6.0	V	R_L = 450 Ω, V_{IN} = 0.8 V
Low Level Output Voltage	–5.0	–5.3	–6.0	V	R_L = ∞, V_{IN} = 2.0 V
	–5.0	–5.6	–6.0	V	R_L = 3 kΩ, V_{IN} = 2.0 V
	–4.5	–5.4	–6.0	V	R_L = 450 Ω, V_{IN} = 2.0 V
Output Balance, V_{BAL}		0.05	0.4	V	R_L = 450 Ω, V_{BAL} = V_{OH} – V_{OL}
RS-232 Outputs					$\overline{EN}$ = 0.8 V, MS+ = V_{DD}, MS– = V_{SS}
High Level Output Voltage	7.0	7.6	V_{DD}	V	R_L = ∞, V_{IN} = 0.8 V
	7.0	7.6	V_{DD}	V	R_L = 3 kΩ, V_{IN} = 0.8 V
Low Level Output Voltage	–7.0	–7.7	V_{SS}	V	R_L = ∞, V_{IN} = 2.0 V
	–7.0	–7.7	V_{SS}	V	R_L = 3 kΩ, V_{IN} = 2.0 V
Off-State Output Current, I_{OZ}	–100		100	µA	$\overline{EN}$ = 2.0 V, V_O = ±6 V, V_{DD} = 15 V, V_{SS} = –15 V
Short Circuit Current, I_{OS}	15	50	100	mA	V_{IN} = 0 V, $\overline{EN}$ = 0 V
	15	40	100	mA	V_{IN} = 5 V, $\overline{EN}$ = 0 V

Specifications subject to change without notice.

TIMING CHARACTERISTICS

(V_{DD} = +10 V ± 10%, V_{SS} = –10 V ± 10%, MS+ = MS– = 0 V. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Output Slew Rate	6.65	10	14	V/µs	Fig 1, Fig 2. R_{SRA} = 2 kΩ, R_L = 450 Ω, C_L = 50 pF Rising/Falling Edge, t_R, t_F
Output Slew Rate	1.33	2.0	3	V/µs	Fig 1, Fig 2. R_{SRA} = 10 kΩ, R_L = 450 Ω, C_L = 50 pF Rising/Falling Edge, t_R , t_F
Output to Hi-Z Propagation Delay (Disable)		0.3	1.0	µs	Fig 1, Fig 3. R_{SRA} = 10 kΩ, R_L = 450 Ω, C_L = 50 pF t_{HZ}
		0.5	1.0	µs	t_{LZ}
Hi-Z to Valid Output Propagation Delay (Enable)		6.0	15	µs	Fig 1, Fig 3. R_{SRA} = 10 kΩ, R_L = 450Ω, C_L = 50 pF t_{ZH}
		7.0	15	µs	t_{ZL}

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{DD} . . . . . +15 V
V_{SS} . . . . . –15 V
Input Voltages
V_{IN} . . . . . –0.3 to (V_{DD} + 0.3 V)
Ouput Voltages
V_{OUT} . . . . . –12 V to +12 V
Output Short Circuit Duration . . . . . Continuous
Power Dissipation Plastic DIP . . . . . 1250 mW
(Derate at 12.5 mW/°C above +50°C)
θ_{JA}, Thermal Impedance . . . . . 75°C/W
Power Dissipation PLCC . . . . . 1000 mW
(Derate at 10 mW/°C above +50°C)
θ_{JA}, Thermal Impedance . . . . . 80°C/W
Operating Temperature Range
Commercial (J Version) . . . . . 0°C to +70°C
Industrial (A Version) . . . . . –40°C to +85°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C
Vapour Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM5170JN	0°C to +70°C	N-28
ADM5170AN	–40°C to +85°C	N-28
ADM5170JP	0°C to +70°C	P-28A
ADM5170AP	–40°C to +85°C	P-28A

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM5170 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

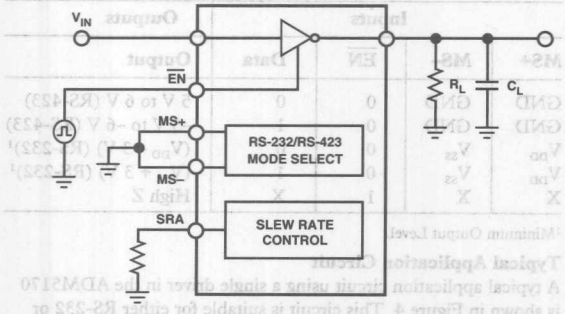


Figure 1. Timing Test Circuit

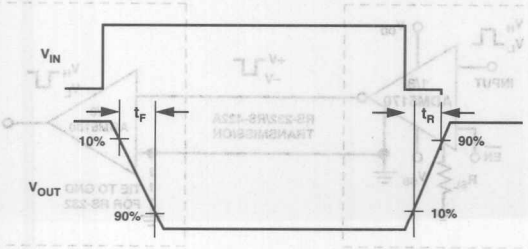


Figure 2. Rise/Fall Timing Waveforms

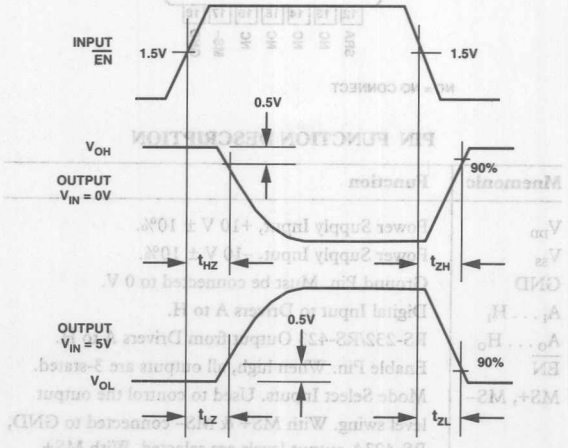


Figure 3. Enable/Disable Timing Waveforms

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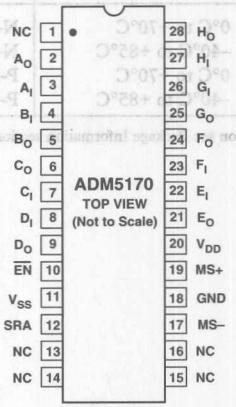
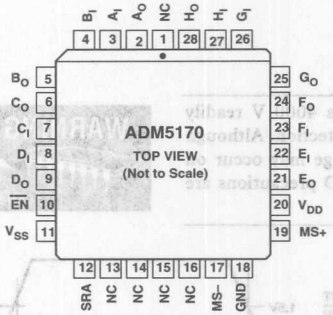
DIP



NC = NO CONNECT

PLCC



NC = NO CONNECT

PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{DD}	Power Supply Input, +10 V ± 10%.
V_{SS}	Power Supply Input, –10 V ± 10%.
GND	Ground Pin. Must be connected to 0 V.
$A_I \ldots H_I$	Digital Input to Drivers A to H.
$A_O \ldots H_O$	RS-232/RS-423 Output from Drivers A to H.
$\overline{EN}$	Enable Pin. When high, all outputs are 3-stated.
MS+, MS–	Mode Select Inputs. Used to control the output level swing. With MS+ & MS– connected to GND, RS-423A output levels are selected. With MS+ connected to V_{DD} and MS– connected to V_{SS}, RS-232 output levels are developed.
SRA	Slew Rate Adjust Input. An external resistor (2 kΩ to 10 kΩ) connected between this pin and GND is used to control the Output Slew Rate (10 V/µs to 2.2 V/µs).

connected between the SRA pin and GND. The slew rate is approximately.

$$Slew\ Rate\ (V/\mu s) = 20/R_{SRA}\ (k\Omega)$$

Resistors between 2 kΩ and 10 kΩ may be used providing a slew rate which may be varied from 10 V/µs to 2.2 V/µs. Figure 5 in the Typical Performance Characteristics section shows how the slew rate varies with R_{SRA} while Figure 8 shows how the transition time (10% to 90%) varies with R_{SRA}. Waveshaping of the output allows the user to control the level of interference (near-end crosstalk) which may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rate are given in the EIA RS-423A specifications.

Maximum Data Rate (kB/s) = 300/t (for rates from 1 kB/s to 100 kB/s).

$$Cable\ Length\ (feet) = 100\ X\ t\ (Max\ Length = 4000\ ft.)$$

where t is the transition time (in µs) for the output to swing from 10% to 90% of its steady state values. The absolute maximum data rate is 100 kB/s and the maximum cable length is limited to 4000 ft.

Output Mode Programming

The ADM5170 has two programmable output modes which provide different output voltage levels. The low output mode meets the specifications of EIA standards RS-423A while the high output mode meets the RS-232 specifications. The high output mode provides greater output swings and is suitable for driving lines where higher attenuation levels must be tolerated. This mode is selected by connecting the mode select pins to the supplies, MS+ to V_{DD} and MS– to V_{SS}. The low output mode is selected by connecting both mode select pins MS+ and MS– to GND. This mode provides a controlled output swing with lower output levels.

Inputs				Outputs
MS+	MS–	$\overline{EN}$	Data	Output
GND	GND	0	0	5 V to 6 V (RS-423)
GND	GND	0	1	–5 V to –6 V (RS-423)
V_{DD}	V_{SS}	0	0	(V_{DD} – 3 V) (RS-232)[1]
V_{DD}	V_{SS}	0	1	(V_{SS} + 3 V) (RS-232)[1]
X	X	1	X	High Z

[1]Minimum Output Level.

Typical Application Circuit

A typical application circuit using a single driver in the ADM5170 is shown in Figure 4. This circuit is suitable for either RS-232 or RS-423 communication. An ADM5180 octal receiver is used to translate the signal back to CMOS logic level at the receiving end.

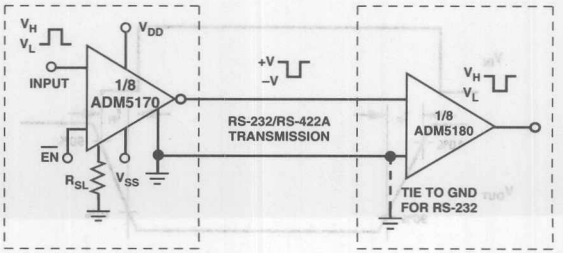


Figure 4. RS-232/RS-423A Typical Application Circuit

Octal, RS-232/RS-423 Line Receiver

ADM5180

FEATURES

Eight Differential Line Receivers in One Package
Meets EIA Standard EIA-232E, 423A, 422A and CCITT V.10, V.11, V.28
Single +5 V Supply
Differential Inputs Withstand ±25 V
Internal Hysteresis
Low Power CMOS –3.5 mA Supply Current
TTL/CMOS Compatible Outputs
Available in 28-Pin DIP and PLCC Packages
Low Power Replacement for UC5180C/NE5180

APPLICATIONS

High Speed Communication
Computer I-O Ports
Peripherals
High Speed Modems
Printers
Logic Level Translation

GENERAL DESCRIPTION

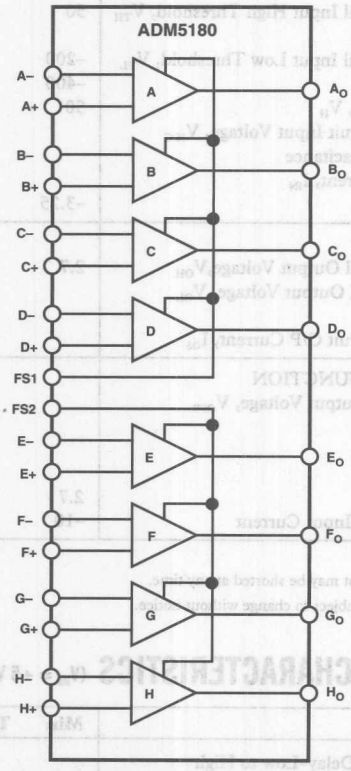
The ADM5180 is an octal differential line receiver suitable for a wide range of digital communication systems with data rates up to 200 kB/s. Input signals conforming to EIA Standards 232-E, 422A and CCITT V.10, V.11, V.28, X.26, and X.27 are accepted and translated into TTL /CMOS output signal levels.

The ADM5180 is a superior upgrade for the UC5180C and the NE5180. It is fabricated on an advanced BiCMOS process, allowing high speed bipolar circuitry to be combined with low power CMOS. This minimizes the power consumption to less than 25 mW.

A failsafe function ensures a known output state under a variety of input fault conditions as defined in RS-422A and RS-423A. The failsafe function is controlled by FS1 and FS2. Each controls four receivers. With FS = Low and a fault condition the output is forced low while if FS = High, the output is forced high.

The device is available in both 28-pin DIP and 28-lead PLCC packages.

FUNCTIONAL BLOCK DIAGRAM



Truth Table

Differential Input (+) - (–)	Failsafe Input FS1, FS2	Receiver Logic Output
>200 mV	X	H
<–200 mV	X	L
O/C	L	L
S/C	L	L
O/C	H	H
S/C	H	H

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ADM5180–SPECIFICATIONS (V_{DD} = +5 V ± 5%, Input Common-Mode Range = ±7 V. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD}	4.75		5.25	V	
I_{DD}		3.5	5	mA	
INPUTS					
Input Resistance, R_{IN}	3		7	kΩ	3 V ≤ |V_{IN}| ≤ 25 V
Differential Input High Threshold, V_{TH}	50		200	mV	R_S = 0 Ω, V_{OUT} = 2.7 V, I_{OUT} = –440 μA, See Figure 1
			400	mV	R_S = 500 Ω, V_{OUT} = 2.7 V, I_{OUT} = –440 μA, See Figure 1
Differential Input Low Threshold, V_{TL}	–200		–50	mV	R_S = 0 Ω, V_{OUT} = 0.45 V, I_{OUT} = 8 mA, See Figure 1
	–400			mV	R_S = 500 Ω, V_{OUT} = 0.45 V, I_{OUT} = 8 mA, See Figure 1
Hysteresis, V_H	50		140	mV	FS1, FS2 = 0 V or V_{DD}, See Figure 1
Open Circuit Input Voltage, V_{IOC}			60	mV	
Input Capacitance			20	pF	
Input Current, I_{IN}			3.25	mA	V_{IN} = +10 V
	–3.25			mA	V_{IN} = –10 V
OUTPUTS					
High Level Output Voltage, V_{OH}	2.7			V	V_{ID} = 1.0 V, I_{OUT} = –440 μA
Low Level Output Voltage , V_{OL}			0.4	V	V_{ID} = –1.0 V, I_{OUT} = 4 mA
			0.45	V	V_{ID} = –1.0 V, I_{OUT} = 8 mA, T_A = 0°C to +70°C
Short Circuit O/P Current, I_{OS}			100	mA	Note 1
FAILSAFE FUNCTION					
Failsafe Output Voltage, V_{OFS}					Inputs Open or Shorted Together or One Input Open and One Grounded
			0.40	V	0 ≤ I_{OUT} ≤ 4 mA; FS1, FS2 = 0 V
			0.45	V	0 ≤ I_{OUT} ≤ 8 mA, T_A = 0°C to +70°C; FS1, FS2 = 0 V
	2.7			V	0 ≥ I_{OUT} ≥ –400 μA; FS1, FS2 = V_{DD}
FS1, FS2 Input Current	–10		+10	μA	

NOTE
[1]Only one output may be shorted at any time.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = +5 V ± 5%. All Specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Propagation Delay–Low to High			550	ns	C_L = 50 pF, V_{IN} = ±500 mV
Propagation Delay–High to Low			550	ns	C_L = 50 pF, V_{IN} = ±500 mV
Acceptable Input Frequency			0.1	MHz	Unused Input Grounded, V_{IN} = ±200 mV
Rejectable Input Frequency	5.5			MHz	Unused Input Grounded, V_{IN} = ±500 mW

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted)

V_{DD} ..... +7 V
Common-Mode Input Voltage ..... +15 V
Differential Input Voltage ..... +25 V
Failsafe Voltage ..... –0.3 V to V_{CC}
Output Short Circuit Duration ..... Continuous[2]
Power Dissipation Plastic DIP ..... 1250 mW
(Derate at 12.5 mW/°C Above +50°C)
θ_{JA}, Thermal Impedance ..... 75°C/W
Power Dissipation PLCC ..... 1000 mW
(Derate at 12.5 mW/°C Above +50°C)
θ_{JA}, Thermal Impedance ..... +80°C/W
Operating Temperature Range
Commercial (J Version) ..... 0°C to +70°C
Industrial (A Version) ..... –40°C to +80°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Vapour Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

NOTES
[1]This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.
[2]Only one output should be shorted at any time.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM5180 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

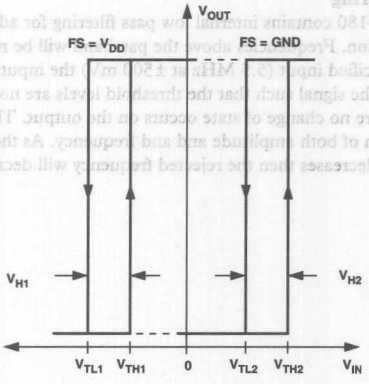

Figure 1. V_{TL}, V_{TH}, V_H Definition

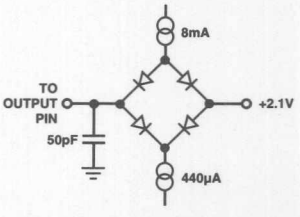

Figure 2. Timing Test Load

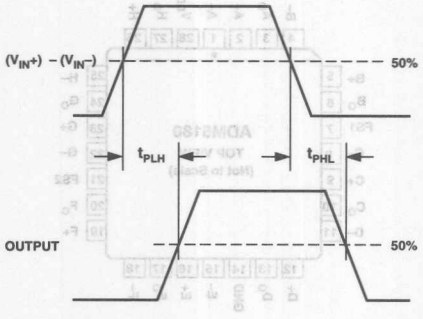

Figure 3. Timing Waveform

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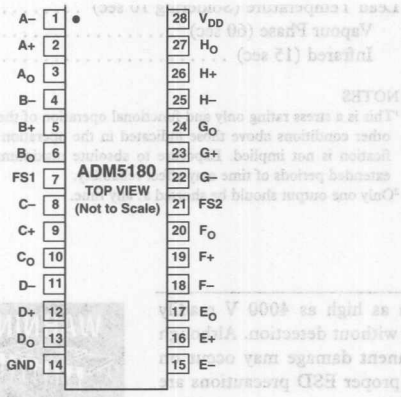
ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM5180JN	0°C to +70°C	N-28
ADM5180AN	–40°C to +85°C	N-28
ADM5180JP	0°C to +70°C	P-28A
ADM5180AP	–40°C to +85°C	P-28A

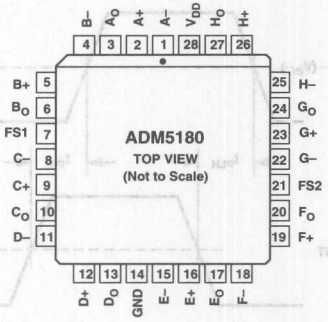
*For outline information see Package Information section.



input fault conditions as defined in RS-422A and RS-423A standards. The fault conditions are (1) Driver in power-off condition, (2) Receiver not interconnected with Driver, (3) Open-circuited interconnecting cable, and (4) Short-circuited interconnecting cable. If any of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The failsafe level is programmed using the failsafe (FS) input. There are two failsafe inputs, FS1 and FS2 which each control four receivers. FSI controls receivers A . . . D and FS2 controls receivers E . . . H. A connection to V_{DD} on the failsafe input sets the output high under fault conditions while a connection to GND sets the output low.

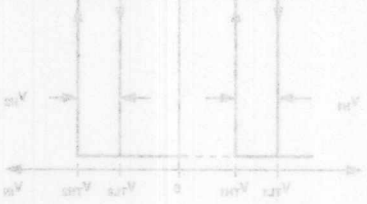
FS1, FS2	Output During Fault Condition
V_{DD}	High
GND	Low

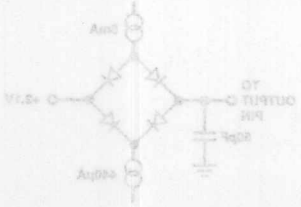
PLCC



Input Filtering

The ADM5180 contains internal low pass filtering for additional noise rejection. Frequencies above the passband will be rejected. For the specified input (5.5 MHz at ±500 mV) the input stage attenuates the signal such that the threshold levels are not reached and therefore no change of state occurs on the output. The filtering is a function of both amplitude and and frequency. As the signal amplitude decreases then the rejected frequency will decrease.





PIN DESCRIPTION

Mnemonic	Function
V_{DD}	Power Supply Input, 5 V ± 5%.
GND	Ground Pin. Must be connected to 0 V.
A+ . . . H+	Noninverting Input to Differential Receivers A to H.
A– . . . H–	Inverting Input to Differential Receivers A to H.
A_O . . . H_O	Receiver Outputs A to H.
FS1	A through D and FS2 controls receivers E through H.
FS2	Failsafe Control Inputs. FS1 controls receivers A through D and FS2 control Receiver E through H.

Motion Control Products
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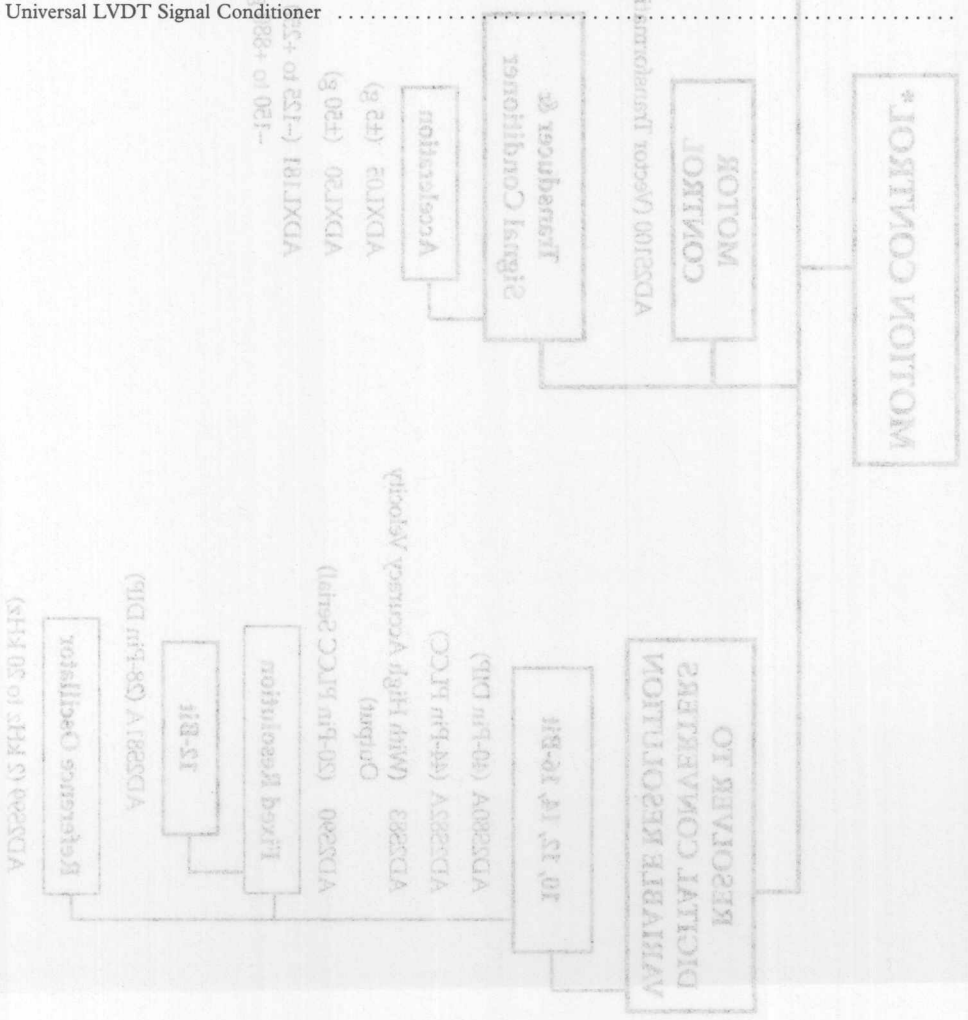
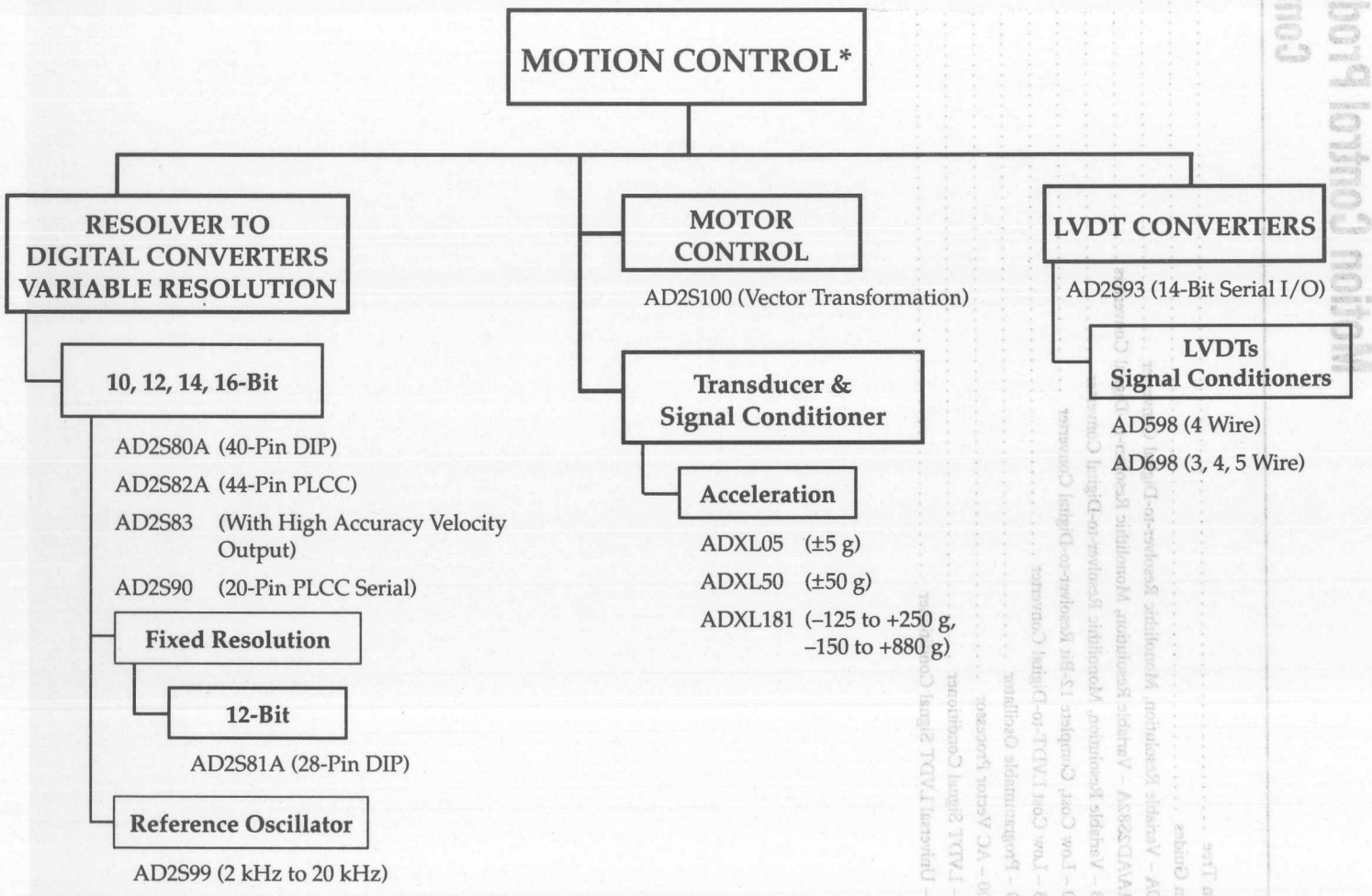


Selection Tree — Motion Control



*All Products are Monolithic

Selection Guides—Motion Control Products

Digital-to-Synchro and Resolver Converters

Model	Res Bits	Output Format[1]	Accuracy arc mins	Load Driving Capability	Reference Frequency Options Hz	Reference Input Volt Options V rms	Signal Output Volt Options V rms	Transformer Output Isolations	Package Options[2]	Temp Ranges[3]	Page[4]	Comments
DRC1745	14	R[5]	±1, ±2, ±3	2.0VA[6]	dc→2600	0→3.4	0→6.8	Use Ext. STM 1680 and STM 1683 Transformer	M	M	CI 3–107	Digital-to-Resolver Converter with Int. 2 VA Power Amplifier. Optional Int. TransZorb† Protection. 2 Byte Latched Inputs
AD2S65	14	R	±2, ±4[7]	–	dc→2600	0→3.4	0→6.8	–	M	C, M	CI 3–35	Digital-to-Resolver Converter. Autonulling (AN) Option
DRC1746	16	R[5]	±1, ±2, ±3	2.0VA[6]	dc→2600	0→3.4	0→6.8	Use Ext. STM 1680 and STM 1683 Transformer	M	M	CI 3–107	16-Bit Version of DRC1745
AD2S66	16	R	±1, ±2, ±4[7]	–	dc→2600	0→3.4	0→6.8	–	M	C, M	CI 3–35	Digital-to-Resolver Converter. Autonulling (AN) Option

Motor Control

Model	Description	Package Options[2]	Temp Range[3]	Page[4]	Comments
AD2S100	**AC Vector Controller**	**P**	**I**	**16–51**	Vector Coordinate Transformation, 15 arc min, 2 μs Settling Time

Synchro/Resolver Support Components

Model	Description	Package Options[2]	Temp Ranges[3]	Page[4]	Comments
AD2S99	**Programmable Sine Wave Oscillator**	**P**	**I**	**16–48**	**2 kHz–20 kHz Freq., Transducer Output Phase Locking**
AD2S75	Signal and Reference Isolation for AD2S80/81/82	M	C, M	CI 3–43	56–20,000 Hz Freq, 11.8–115 V rms Ref, 11.8/26/90 V rms Input
OSC1758	Hybrid Sine/Cosine Power Oscillator	M	C, M	CI 3–117	0.0–10 kHz Frequency Range[6], In-phase and Quadrature Outputs, 1.5 W Output Power

LVDT Signal Conditioners

Model	Description	Package Options[2]	Temp Ranges[3]	Page[4]	Comments
AD598	**Single Chip LVDT Driver/Amplifier**	**D, R**	**C, I**	**16–63**	**20 Hz–20 kHz, Phase Insensitive, High Accuracy**
AD698	**Single Chip 4-Wire LVDT Driver/Amplifier**	**P, Q**	**I, M**	**16–67**	**Improved Performance, Multiple Configurations**

[1]S = Synchro; R = Resolver.
[2]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[3]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[4]CI = *Data Converter Reference Manual, Volume I*. All other entries refer to this volume.
[5]Synchro format output with external output transformer STM1683.
[6]Can be used with pulsating power supply for reduced dissipation.
[7]Depends on option.
Boldface Type: Data sheet information in this volume.
†TransZorb is a trademark of General Semiconductor Industries, Inc.

Selection Guides—Motion Control Products

Synchro, Resolver, Inductosyn† and LVDT-to-Digital Converters

Model	Res Bits	Input Format[1]	Accuracy arc mins	Tracking Rate Options revs/sec[2]	Reference Frequency Options Hz	Input Isol	Package Options[3]	Temp Ranges[4]	Page[5]	Comments
SDC/RDC1741	12	S, R	±15.3	18	400, 2.6 k	Yes	M	C, M	CI 3–119	Tristate, Latched Output Internal Transformer Isolatio
SDC/RDC1742	12	S, R	±8.5	18	400, 2.6 k	Yes	M	C, M	CI 3–119	Tristate, Latched Output Internal Transformer Isolatio
AD2S81A[6]	**12**	**I, R**	**±30[7]**	**260**	**400→20 k**	**No**	**D**	**C**	**16–11**	**Monolithic, User Selectable Characteristics, High Tracki Quality Velocity Output, Cla**
SDC/RDC1740	14	S, R	±5.3	27	400, 2.6 k	Yes	M	C, M	CI 3–119	Tristate, Latched Output Internal Transformer Isolatio
AD2S80A[6]	**16, 14, 12, 10[8]**	**I, R**	**±2, ±4, ±8**	**1040[9]**	**50–20 k**	**No**	**D, E**	**C, I, M/D**	**16–7**	**Monolithic, User Selectable Characteristics and Resoluti Tracking Rate and Quality V Output**
AD2S82A[6]	**16, 14, 12, 10[8]**	**I, R**	**±2, ±4, ±8**	**1040[9]**	**50–20 k**	**No**	**P**	**C**	**16–11**	**Monolithic, User Selectable Characteristics and Resoluti Tracking Rate and Quality V Output**
AD2S83	**16, 14, 12, 10[8]**	**I, R**	**±8**	**1040[9]**	**50–20 k**	**No**	**P**	**I**	**16–15**	**Monolithic, User Selectable Dynamic Characteristics and Resolution. High Tracking R ±0.15% Linearity Velocity O**
AD2S34	14	R	±2.6, ±4.0	20, 48	0.4, 2.6, 4.0 k	No	Z	M	CI 3–7	Dual Channel Resolver-to-Dig Converter with On-Board Osc
AD2S46	16	S, R	±1.3, ±2.6	12	0.4→2.6 k	No	D	M	CI 3–23	16-Bit Resolver/Synchro-to- Digital Converter, 1.3 arc min

Model	Res Bits	Input Format[1]	Accuracy arc mins	Tracking Rate Options revs/sec[2]	Reference Frequency Options Hz	Input Isol	Package Options[3]	Temp Ranges[4]	Page[5]	Comments
AD2S44	14	S, R	±2.6,[10] ±4.0, ±5.2	20	0.4→2.6 k	No	M	M	CI 3–15	Dual Channel Resolver/ Synchro-to-Digital Converter with Loss of Track Detection
AD2S90	**12**	**I, R**	**±8**	**375**	**2.0→10.0 k**	**No**	**P**	**C, I**	**16–27**	Low Cost RDC, Incremental Encoder and Absolute Position Output
AD2S93	**14**	**LVDT**	**0.1, 0.05%**	**TBD**	**2.0–10.0 k**	**No**	**P**	**I**	**16–37**	14-Bit LVDT-to-Digital Converter

[1]S = Synchro; R = Resolver; I = Inductosyn.
[2]In general, higher reference frequency options have higher tracking rates.
[3]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[4]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[5]CI = *Data Converter Reference Manual, Volume I*. All other entries refer to this volume.
[6]Die Revision.
[7]Consult data sheet.
[8]Resolution is user selectable.
[9]Depends on resolution selected.
[10]±2.6 arc min only available over 0°C to +70°C.
Boldface Type: Data sheet information in this volume.
†Inductosyn is a registered trademark of Farrand Industries, Inc.

Variable Resolution, Monolithic Resolver-to-Digital Converter

AD2S80A

FEATURES

Monolithic (BiMOS II) Tracking R/D Converter
40-Pin DIP Package
44-Pin LCC Package
10-, 12-, 14- and 16-Bit Resolution Set by User
Ratiometric Conversion
Low Power Consumption: 300 mW typ
Dynamic Performance Set by User
High Max Tracking Rate 1040 RPS (10 Bits)
Velocity Output
Industrial Temperature Range Versions
Military Temperature Range Versions
ESD Class 2 Protection (2,000 V min)
/883 B Parts Available

APPLICATIONS

DC Brushless and AC Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control
Military Servo Control

GENERAL DESCRIPTION

The AD2S80A is a monolithic 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter contained in a 40-pin DIP or 44-pin LCC ceramic package. It is manufactured on a BiMOS II process that combines the advantages of CMOS logic and bipolar high accuracy linear circuits on the same chip.

The converter allows users *to select their own resolution and dynamic performance with external components*. This allows the users great flexibility in defining the converter that best suits their system requirements. The converter allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

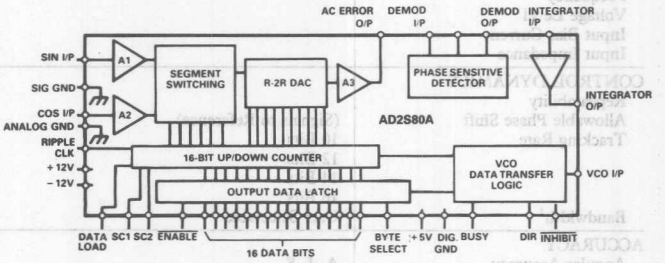
The AD2S80A converts resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high-noise immunity and tolerance of lead length when the converter is remote from the resolver.

The 10-, 12-, 14- or 16-bit output word is in a three-state digital logic available in 2 bytes on the 16 output data lines. BYTE SELECT, $\overline{\text{ENABLE}}$ and $\overline{\text{INHIBIT}}$ pins ensure easy data transfer to 8- and 16-bit data buses, and outputs are provided to allow for cycle or pitch counting in external counters.

An analog signal proportional to velocity is also available and can be used to replace a tachogenerator.

The AD2S80A operates over 50 Hz to 20,000 Hz reference frequency.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

Monolithic. A one chip solution reduces the package size required and increases the reliability.

Resolution Set by User. Two control pins are used to select the resolution of the AD2S80A to be 10, 12, 14 or 16 bits allowing the user to use the AD2S80A with the optimum resolution for each application.

Ratiometric Tracking Conversion. Conversion technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and tolerance to harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low cost preferred value resistors and capacitors, and the component values are easy to select using the simple instructions given.

Velocity Output. An analog signal proportional to velocity is available and is linear to typically one percent. This can be used in place of a velocity transducer in many applications to provide loop stabilization in servo controls and velocity feedback data.

Low Power Consumption. Typically only 300 mW.

Military Product. The AD2S80A is available processed in accordance with MIL-STD-883B, Class B.

MODELS AVAILABLE

Information on the models available is given in the section "Ordering Guide."

16

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD2S80A—SPECIFICATIONS (typical at +25°C unless otherwise noted)

Parameter	Conditions	AD2S80A Min	Typ	Max	Units
SIGNAL INPUTS					
Frequency		50		20,000	Hz
Voltage Level		1.8	2.0	2.2	V rms
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
Maximum Voltage				8	V pk
REFERENCE INPUT					
Frequency		50		20,000	Hz
Voltage Level		1.0		8.0	V pk
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
CONTROL DYNAMICS					
Repeatability				1	LSB
Allowable Phase Shift	(Signals to Reference)	−10		+10	Degrees
Tracking Rate	10 Bits			1040	rps
	12 Bits			260	rps
	14 Bits			65	rps
	16 Bits			16.25	rps
Bandwidth[1]	User Selectable				
ACCURACY					
Angular Accuracy	A, J, S			**±8 +1 LSB**	arc min
	B, K, T			**±4 +1 LSB**	arc min
	L, U			**±2 +1 LSB**	arc min
Monotonicity	Guaranteed Monotonic				
Missing Codes (16-Bit Resolution)	A, B, J, K, S, T			**4**	Codes
	L, U			**1**	Code
VELOCITY SIGNAL					
Linearity	Over Full Range		±1	**±3**	% FSD
Reversion Error			±1	±2	% FSD
DC Zero Offset[2]				**6**	mV
DC Zero Offset Tempco			−22		μV/°C
Gain Scaling Accuracy				±10	% FSD
Output Voltage	1 mA Load	±8	±9	±10.5	V
Dynamic Ripple	Mean Value			1.5	% rms O/P
Output Load				1.0	kΩ
INPUT/OUTPUT PROTECTION					
Analog Inputs	Overvoltage Protection		±8		V
Analog Outputs	Short Circuit O/P Protection	±5.6	±8	±10.4	mA
DIGITAL POSITION					
Resolution	10, 12, 14, and 16				
Output Format	Bidirectional Natural Binary				
Load				**3**	LSTTL
$\overline{\text{INHIBIT}}$[3]					
Sense	Logic LO to Inhibit				
Time to Stable Data				600	ns
$\overline{\text{ENABLE}}$[3]	Logic LO Enables Position Output. Logic HI Outputs				
ENABLE Time	in High Impedance State	35		110	ns
BYTE SELECT[3]					
Sense					
Logic HI	MS Byte DB1–DB8, LS Byte DB9–DB16				
Logic LO	LS Byte DB1–DB8, LS Byte DB9–DB16				
Time to Data Available		60		140	ns
SHORT CYCLE INPUTS	Internally Pulled High (100 kΩ to $+V_S$)				
SC1 SC2					
0 0	10 Bit				
0 1	12 Bit				
1 0	14 Bit				
1 1	16 Bit				
DATA LOAD					
Sense	Internally Pulled High (100 kΩ) to $+V_S$. Logic LO Allows Data to be Loaded into the Counters from the Data Lines		150	300	ns
BUSY[3]					
Sense	Logic HI When Position O/P Changing				
Width		**200**		**600**	ns
Load	Use Additional Pull-Up			1	LSTTL

Parameter	Conditions	AD2S80A Min	Typ	Max	Units
DIRECTION[3]					
Sense	Logic HI Counting Up Logic LO Counting Down				
Max Load				3	LSTTL
RIPPLE CLOCK[3]					
Sense	Logic HI; All 1s to All 0s; All 0s to all 1s				
Width	Dependent on Input Velocity	300			
Reset	Before Next Busy				
Load				3	LSTTL
DIGITAL INPUTS					
High Voltage, V_{IH}	$\overline{\text{INHIBIT}}$, ENABLE DB1–DB16, Byte Select $\pm V_S = \pm 10.8$ V, $V_L = 5.0$ V	2.0			V
Low Voltage, V_{IL}	$\overline{\text{INHIBIT}}$, ENABLE DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.0$ V			0.8	V
DIGITAL INPUTS					
High Current, I_{IH}	$\overline{\text{INHIBIT}}$, ENABLE DB1–DB16 $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			±100	µA
Low Current, I_{IL}	$\overline{\text{INHIBIT}}$, ENABLE DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			±100	µA
DIGITAL INPUTS					
Low Voltage, V_{IL}	ENABLE = HI SC1, SC2, Data Load $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			1.0	V
Low Current, I_{IL}	ENABLE = HI SC1, SC2, Data Load $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			−400	µA
DIGITAL OUTPUTS					
High Voltage, V_{OH}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 4.5$ V $I_{OH} = 100$ µA	2.4			V
Low Voltage, V_{OL}	DB1– DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $I_{OL} = 1.2$ mA			0.4	V
THREE STATE LEAKAGE	DB1–DB16 Only				
Current I_L	$\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V, $V_{OL} = 0$ V			±100	µA
	$\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V, $V_{OH} = 5.0$ V			±100	µA
POWER SUPPLIES					
Voltage Levels					
$+V_S$		+10.8		+13.2	V
$-V_S$		−10.8		−13.2	V
$+V_L$		+5		+13.2	V
Current					
$\pm I_S$	$\pm V_S$ @ ±12 V		±12	±23	mA
$\pm I_S$	$\pm V_S$ @ ±13.2 V		±19	±30	mA
$\pm I_L$	$+V_L$ @ ±5.0 V		±0.5	±1.5	mA

NOTES
[1]Refers to small signal bandwidth.
[2]Output offset dependent on value for R6.
[3]Refer to timing diagram.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.

ESD SENSITIVITY

The AD2S80A features an input protection circuit consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charges Device Model).

The AD2S80A is ESD protection Class II (2000 V min). Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices *ESD Prevention Manual.*

16

AD2S80A

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_S$, $-V_S$) . . . . . ±12 V dc ±10%
Power Supply Voltage V_L . . . . . +5 V dc ±10%
Analog Input Voltage (SIN and COS) . . . . . 2 V rms ±10%
Analog Input Voltage (REF) . . . . . 1 V to 8 V peak
Signal and Reference Harmonic Distortion . . . . . 10% (max)
Phase Shift Between Signal and Reference . ±10 Degrees (max)
Ambient Operating Temperature Range
  Commercial (JD, KD, LD) . . . . . 0°C to +70°C
  Industrial (AD, BD) . . . . . −40°C to +85°C
  Extended (SD, SE, TD, TE, UD, UE) . . . −55°C to +125°C

ABSOLUTE MAXIMUM RATINGS[1] (with respect to GND)

$+V_S$[2] . . . . . +14 V dc
$-V_S$ . . . . . −14 V dc
$+V_L$ . . . . . $+V_S$
Reference . . . . . +14 V to $-V_S$
SIN . . . . . +14 V to $-V_S$
COS . . . . . +14 V to $-V_S$
Any Logical Input . . . . . −0.4 V dc to $+V_L$ dc
Demodulator Input . . . . . +14 V to $-V_S$
Integrator Input . . . . . +14 V to $-V_S$
VCO Input . . . . . +14 V to $-V_S$
Power Dissipation . . . . . 860 mW
Operating Temperature
  Commercial (JD, KD, LD) . . . . . 0°C to +70°C
  Industrial (AD, BD) . . . . . −40°C to +85°C
  Extended (SD, SE, TD, TE, UD, UE) . . . −55°C to +125°C
θ_{JC}[3] (40-Pin DIP 883 Parts Only) . . . . . 11°C/W
θ_{JC}[3] (44-Pin LCC 883 Parts Only) . . . . . 10°C/W
Storage Temperature (All Grades) . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

CAUTION:

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
3. With reference to Appendix C of MIL-M-38510.

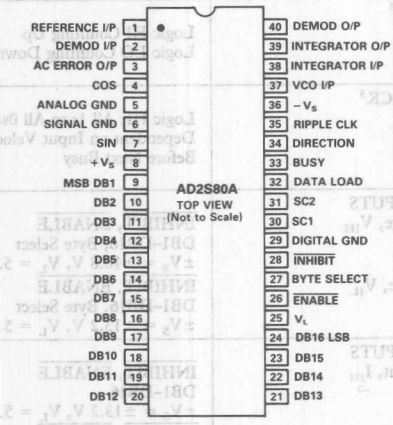
ORDERING GUIDE

Model	Operating Temperature Range	Accuracy	Package Option*
AD2S80AJD	0°C to +70°C	8 arc min	D-40
AD2S80AKD	0°C to +70°C	4 arc min	D-40
AD2S80ALD	0°C to +70°C	2 arc min	D-40
AD2S80AAD	−40°C to +85°C	8 arc min	D-40
AD2S80ABD	−40°C to +85°C	4 arc min	D-40
AD2S80ASD	−55°C to +125°C	8 arc min	D-40
AD2S80ATD	−55°C to +125°C	4 arc min	D-40
AD2S80AUD	−55°C to +125°C	2 arc min	D-40
AD2S80ASE	−55°C to +125°C	8 arc min	E-44A
AD2S80ATE	−55°C to +125°C	4 arc min	E-44A
AD2S80AUE	−55°C to +125°C	2 arc min	E-44A
AD2S80ASD/883B	−55°C to +125°C	8 arc min	D-40
AD2S80ATD/883B	−55°C to +125°C	4 arc min	D-40
AD2S80ASE/883B	−55°C to +125°C	8 arc min	E-44A
AD2S80ATE/883B	−55°C to +125°C	4 arc min	E-44A

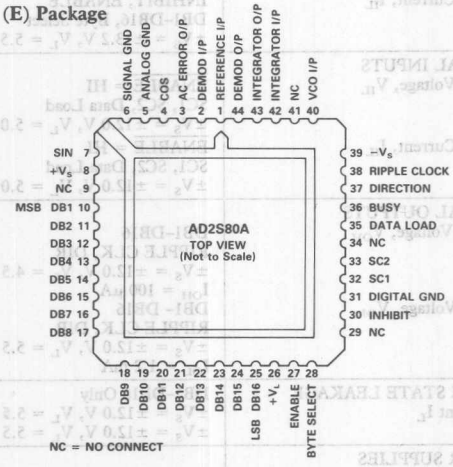
*D = Ceramic DIP Package; E = Leadless Ceramic Chip Carrier Package.
For outline information see Package Information section.

AD2S80A PIN CONFIGURATIONS

DIP (D) Package



LCC (E) Package



PIN DESIGNATIONS

MNEMONIC	DESCRIPTION
REFERENCE I/P	REFERENCE SIGNAL INPUT
DEMOD I/P	DEMODULATOR INPUT
AC ERROR O/P	RATIO MULTIPLIER OUTPUT
COS	COSINE INPUT
ANALOG GROUND	POWER GROUND
SIGNAL GROUND	RESOLVER SIGNAL GROUND
SIN	SINE INPUT
$+V_S$	POSITIVE POWER SUPPLY
DB1–DB16	PARALLEL OUTPUT DATA
V_L	LOGIC POWER SUPPLY
$\overline{\text{ENABLE}}$	LOGIC HI-OUTPUT DATA IN HIGH IMPEDANCE STATE, LOGIC LO PRESENTS DATA TO THE OUTPUT LATCHES.
BYTE SELECT	LOGIC HI-MOST SIGNIFICANT BYTE TO DB1–DB8 LOGIC LO-LEAST SIGNIFICANT BYTE TO DB1–DB8.
$\overline{\text{INHIBIT}}$	LOGIC LO INHIBITS DATA TRANSFER TO OUTPUT LATCHES.
DIGITAL GROUND	DIGITAL GROUND
SC1–SC2	SELECT CONVERTER RESOLUTION
DATA LOAD	LOGIC LO DB1–D16 INPUTS LOGIC HI DB1–D16 OUTPUTS
BUSY	CONVERTER BUSY, DATA NOT VALID WHILE BUSY HI
DIRECTION	LOGIC STATE DEFINES DIRECTION OF INPUT SIGNAL ROTATION
RIPPLE CLOCK	POSITIVE PULSE WHEN CONVERTER OUTPUT CHANGES FROM 1S TO ALL 0S OR VICE VERSA
$-V_S$	NEGATIVE POWER SUPPLY
VCO I/P	VCO INPUT
INTEGRATOR I/P	INTEGRATOR INPUT
INTEGRATOR O/P	INTEGRATOR OUTPUT
DEMOD O/P	DEMODULATOR OUTPUT

Variable Resolution, Monolithic Resolver-to-Digital Converters

AD2S81A/AD2S82A

FEATURES
Monolithic (BiMOS II) Tracking R/D Converter
Ratiometric Conversion
Low Power Consumption: 300 mW typ
Dynamic Performance Set by User
Velocity Output
ESD Class 2 Protection (2,000 V min)

AD2S81A
28-Pin DIP Package
Low Cost

AD2S82A
44-Pin PLCC Package
10-, 12-, 14- and 16-Bit Resolution Set by User
High Max Tracking Rate 1040 RPS (10 Bits)
VCO Output (Inter LSB Output)
Data Complement Facility

APPLICATIONS
DC Brushless and AC Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control

GENERAL DESCRIPTION

The AD2S82A is a monolithic 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter contained in a 44-pin J leaded PLCC package. Two extra functions are provided in the new surface mount package – COMPLEMENT and VCO output.

The AD2S81A is a monolithic 12-bit fixed resolution tracking resolver-to-digital converter packaged in a 28-pin DIP.

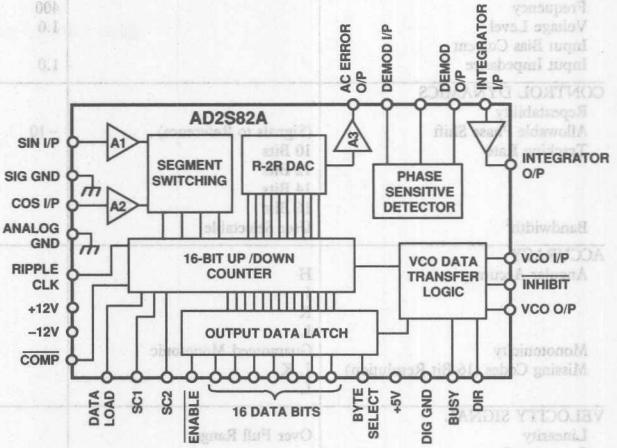
The converters allow users to *select their own dynamic performance with external components*. This allows the users great flexibility in defining the converter that best suits their system requirements. The AD2S82A allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

The AD2S81A and AD2S82A convert resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high-noise immunity and tolerance of lead length when the converter is remote from the resolver.

The output word is in a three-state digital logic form available in 2 bytes on the 16 output data lines for the AD2S82A and on 8 output data lines for the AD2S81A. BYTE SELECT, $\overline{\text{ENABLE}}$ and $\overline{\text{INHIBIT}}$ pins ensure easy data transfer to 8- and 16-bit data buses, and outputs are provided to allow for cycle or pitch counting in external counters.

An analog signal proportional to velocity is also available and can be used to replace a tachogenerator.

AD2S82A FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

Monolithic. A one-chip solution reduces the package size required and increases the reliability.

Resolution Set by User. Two control pins are used to select the resolution of the AD2S82A to be 10, 12, 14 or 16 bits allowing the user to use the AD2S82A with the optimum resolution for each application.

Ratiometric Tracking Conversion. Conversion technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and tolerance to harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low cost, preferred value resistors and capacitors, and the component values are easy to select using the simple instructions given.

Velocity Output. An analog signal proportional to velocity is available and is linear to typically one percent. This can be used in place of a velocity transducer in many applications to provide loop stabilization in servo controls and velocity feedback data.

Low Power Consumption. Typically only 300 mW.

MODELS AVAILABLE

Information on the models available is given in the section "Ordering Information."

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD2S81A/AD2S82A—SPECIFICATIONS (typical at +25°C unless otherwise noted)

Parameter	Conditions	AD2S81A Min	AD2S81A Typ	AD2S81A Max	AD2S82A Min	AD2S82A Typ	AD2S82A Max	Units
SIGNAL INPUTS								
Frequency		400		20,000	50		20,000	Hz
Voltage Level		1.8	2.0	2.2		*		V rms
Input Bias Current			60	150		*		nA
Input Impedance		1.0				*		MΩ
Maximum Voltage				±8		*		V pk
REFERENCE INPUT								
Frequency		400		20,000	50		20,000	Hz
Voltage Level		1.0		8.0		*		V pk
Input Bias Current			60	150		*		nA
Input Impedance		1.0				*		MΩ
CONTROL DYNAMICS								
Repeatability				1			1	LSB
Allowable Phase Shift	(Signals to Reference)	−10		+10		*		Degrees
Tracking Rate	10 Bits						1040	rps
	12 Bits			260			260	rps
	14 Bits						65	rps
	16 Bits						16.25	rps
Bandwidth[1]	User Selectable							
ACCURACY								
Angular Accuracy	H						±22 + 1 LSB	arc min
	J			±30 +1 LSB			±8 + 1 LSB	arc min
	K						±4 + 1 LSB	arc min
	L						±2 + 1 LSB	arc min
Monotonicity	Guaranteed Monotonic							
Missing Codes (16-Bit Resolution)	J, K						4	Codes
	L						1	Code
VELOCITY SIGNAL								
Linearity	Over Full Range		±1	±3		*		% FSD
Reversion Error				±2		*		% FSD
DC Zero Offset[2]				6		*		mV
DC Zero Offset Tempco			−22			*		μV/°C
Gain Scaling Accuracy				±10		*		% FSD
Output Voltage	1 mA Load	±8	±9	±10.5		*		V
Dynamic Ripple	Mean Value			1.5		*		% rms O/P
Output Load				1.0		*		kΩ
INPUT/OUTPUT PROTECTION								
Analog Inputs	Overvoltage Protection		±8			*		V
Analog Outputs	Short Circuit O/P Protection	±5.6	±8	±10.4		*		mA
DIGITAL POSITION								
Resolution	10, 12, 14, and 16							
Output Format	Bidirectional Natural Binary							
Load				3		*		LSTTL
$\overline{\text{INHIBIT}}$[3]								
Sense	Logic LO to Inhibit							
Time to Stable Data				600		*		ns
$\overline{\text{ENABLE}}$[3]	Logic LO Enables Position Output. Logic HI Outputs in High Impedance State							
$\overline{\text{ENABLE}}$/Disable Time		35		110		*		ns
BYTE SELECT[3]								
Sense								
Logic HI	MS Byte DB1–DB8, (LS Byte DB9–DB16)[4]							
Logic LO	LS Byte DB1–DB8, (LS Byte DB9–DB16)[4]							
Time to Data Available		60		140		*		ns
SHORT CYCLE INPUTS[4]	Internally Pulled High (100 kΩ) to $+V_S$							
SC1 SC2								
0 0	10 Bit							
0 1	12 Bit							
1 0	14 Bit							
1 1	16 Bit							
DATA LOAD[4]								
Sense	Internally Pulled High (100 kΩ) to $+V_S$; Logic LO Allows Data to Be Loaded into the Counters from the Data Lines					150	300	ns

Parameter	Conditions	AD2S81A Min	AD2S81A Typ	AD2S81A Max	AD2S82A Min	AD2S82A Typ	AD2S82A Max	Units
COMPLEMENT[4]	Internally Pulled High (100 kΩ) to $+V_S$; Logic LO to Activate; No Connect for Normal Operation							
BUSY[3]								
Sense	Logic HI When Position O/P Changing							
Width		200		600		*		ns
Load	Use Additional Pull-Up			1		*		LSTTL
DIRECTION[3]								
Sense	Logic HI Counting Up Logic LO Counting Down							
Max Load				3		*		LSTTL
RIPPLE CLOCK[3]								
Sense	Logic HI, All 1s to All 0s All 0s to All 1s							
Width	Dependent On Input Velocity	300				*		
Reset	Before Next Busy							
Load				3		*		LSTTL
DIGITAL INPUTS								
High Voltage, V_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 10.8$ V, $V_L = 5.0$ V	2.0				*		V
Low Voltage, V_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.0$ V			0.8		*		V
DIGITAL INPUTS								
High Current, I_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16 $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			±100		*		µA
Low Current, I_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			±100		*		µA
DIGITAL INPUTS								
Low Voltage, V_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, Data Load $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			1.0		*		V
Low Current, I_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, Data Load $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			−400		*		µA
DIGITAL OUTPUTS								
High Voltage, V_{OH}	DB1–DB16; RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 4.5$ V $I_{OH} = 100$ µA	2.4				*		V
Low Voltage, V_{OL}	DB1–DB16, RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $I_{OL} = 1.2$ mA			0.4		*		V
THREE-STATE LEAKAGE	DB1–DB16 Only							
Current I_L	$+V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OL} = 0$ V			±100		*		µA
	$+V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OH} = 5.0$ V			±100		*		µA
POWER SUPPLIES								
Voltage Levels								
$+V_S$		+10.8		+13.2		*		V
$-V_S$		−10.8		−13.2		*		V
$+V_L$		+5		+13.2		*		V
Current								
$+I_S$	$\pm V_S$ @ ±12 V		±12	±23		*		mA
$+I_S$	$\pm V_S$ @ ±13.2 V		±19	±30		*		mA
$+I_L$	$\pm V_L$ @ ±5.0 V		±0.5	±1.5		*		mA

NOTES
[1]Refers to small signal bandwidth.
[2]Output offset dependent on value for R6.
[3]Refer to timing diagram.
[4]AD2S82A only.
*Specifications same as AD2S81A.
Specifications subject to change without notice.
All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.

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Power Supply Voltage ($+V_S$ to $-V_S$) . . . . . ±12 V dc ±10%
Power Supply Voltage V_L . . . . . +5 V dc ±10%
Analog Input Voltage (SIN and COS) . . . . . 2 V rms ±10%
Analog Input Voltage (REF) . . . . . 1 V to 8 V peak
Signal and Reference Harmonic Distortion . . . . . 10% (max)
Phase Shift Between Signal and Reference . ±10 Degrees (max)
Ambient Operating Temperature
Commercial (JD, HP, JP, KP, LP) . . . . . 0°C to +70°C

PIN DESIGNATIONS

MNEMONIC	DESCRIPTION
REFERENCE I/P	REFERENCE SIGNAL INPUT
DEMOD I/P	DEMODULATOR INPUT
AC ERROR O/P	RATIO MULTIPLIER OUTPUT
COS I/P	COSINE INPUT
ANALOG GROUND	POWER GROUND
SIGNAL GROUND	RESOLVER SIGNAL GROUND
SIN I/P	SINE INPUT
$+V_S$	POSITIVE POWER SUPPLY
DB1–DB16	PARALLEL OUTPUT DATA
V_L	LOGIC POWER SUPPLY
$\overline{\text{ENABLE}}$	LOGIC HI–OUTPUT DATA IN HIGH IMPEDANCE STATE, LOGIC, LO PRESENTS DATA TO THE OUTPUT LATCHES.
BYTE SELECT	LOGIC HI–MOST SIGNIFICANT BYTE TO DB1–DB8 LOGIC LO–LEAST SIGNIFICANT BYTE TO DB1–DB8.
$\overline{\text{INHIBIT}}$	LOGIC LO INHIBITS DATA TRANSFER TO OUTPUT LATCHES.
DIGITAL GROUND	DIGITAL GROUND
SC1–SC2*	SELECT CONVERTER RESOLUTION
DATA LOAD*	LOGIC LO DB1–D16 INPUTS LOGIC HI DB1–D16 OUTPUTS
BUSY	CONVERTER BUSY, DATA NOT VALID WHILE BUSY HI
DIRECTION	LOGIC STATE DEFINES DIRECTION OF INPUT SIGNAL ROTATION
RIPPLE CLOCK	POSITIVE PULSE WHEN CONVERTER OUTPUT CHANGES FROM 1S TO ALL 0S OR VICA VERSA
$-V_S$	NEGATIVE POWER SUPPLY
VCO I/P	VCO INPUT
INTEGRATOR I/P	INTEGRATOR INPUT
INTEGRATOR O/P	INTEGRATOR OUTPUT
DEMOD O/P	DEMODULATOR OUTPUT
$\overline{\text{COMPLEMENT}}$*	ACTIVE LOGIC LO
VCO O/P*	VCO OUTPUT

*AD2S82A ONLY.

ORDERING GUIDE

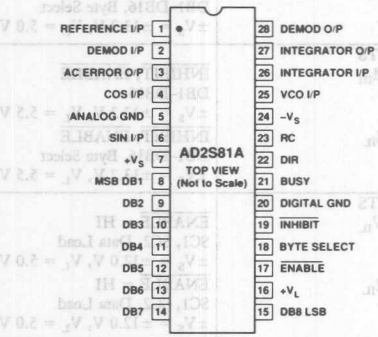
	Accuracy	Operating Temperature Range	Package Option*
AD2S81AJD	30 arc min	0°C to +70°C	D-28
AD2S82AHP	22 arc min	0°C to +70°C	P-44A
AD2S82AJP	8 arc min	0°C to +70°C	P-44A
AD2S82AKP	4 arc min	0°C to +70°C	P-44A
AD2S82ALP	2 arc min	0°C to +70°C	P-44A

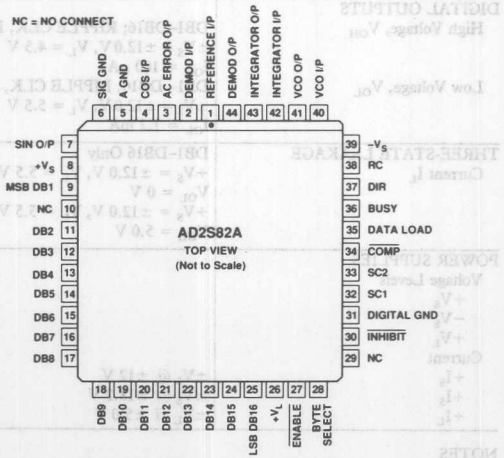
*D = Ceramic DIP Package; P = Plastic Leaded Chip Carrier (PLCC) Package. For outline information see Package Information section.

$+V_S$ . . . . . +14 V dc
$-V_S$ . . . . . −14 V dc
$+V_L$ . . . . . $+V_S$
Reference . . . . . +14 V to $-V_S$
SIN . . . . . +14 V to $-V_S$
COS . . . . . +14 V to $-V_S$
Any Logical Input . . . . . −0.4 V dc to $+V_L$ dc
Demodulator Input . . . . . +14 V to $-V_S$
Integrator Input . . . . . +14 V to $-V_S$
VCO Input . . . . . +14 V to $-V_S$
Power Dissipation . . . . . 860 mW
Operating Temperature
Commercial (JD, HP, JP, KP, LP) . . . . . 0°C to +70°C
Storage Temperature (All Grades) . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

CAUTION:
1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

PIN CONFIGURATIONS





CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although devices feature proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper precautions are recommended to avoid any performance degradation or loss of functionality.

Variable Resolution, Monolithic Resolver-to-Digital Converter

AD2S83

FEATURES
- Monolithic Tracking R/D Converter
- High Accuracy Velocity Output
- High Max Tracking Rate 1040 RPS (10 Bits)
- 44-Pin PLCC Package
- 10-, 12-, 14- or 16-Bit Resolution Set by User
- Ratiometric Conversion
- Stabilized Velocity Reference
- Dynamic Performance Set by User
- Industrial Temperature Range Versions

APPLICATIONS
- DC and AC Servo Motor Control
- Process Control
- Numerical Control of Machine Tools
- Robotics
- Axis Control

GENERAL DESCRIPTION

The AD2S83 is a monolithic 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter contained in a 44-pin PLCC package. It is manufactured on Analog Devices' BiMOS II process that combines the advantages of CMOS logic and bipolar high accuracy linear circuits on the same chip.

The converter allows users *to select their own resolution and dynamic performance with external components*. This allows the users great flexibility in defining the converter that best suits their system requirements. The converter allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

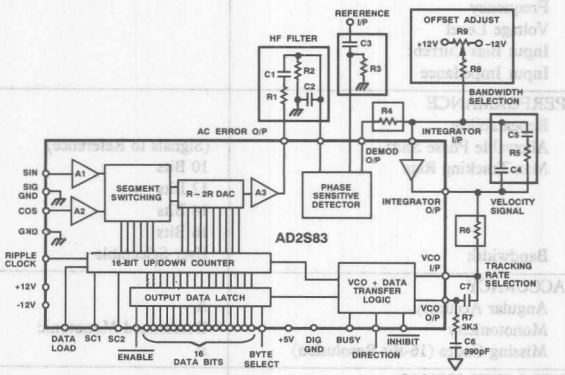
The AD2S83 converts resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high noise immunity and tolerance of long leads allowing the converter to be located remote from the resolver.

The position output from the converter is presented via 3-state output pins which can be configured for operations with 8- or 16-bit bus. BYTE SELECT, ENABLE and INHIBIT pins ensure easy data transfer to 8- and 16-bit data bus, and outputs are provided to allow for cycle or pitch counting in external counters.

A precise analog signal proportional to velocity is also available and will replace a tachogenerator.

The AD2S83 operates over reference frequencies in the range 0 Hz to 20,000 Hz.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

High Accuracy Velocity Output. A precision analog velocity signal with a typical linearity of ±0.1% and reversion error less than ±0.3% is generated by the AD2S83. The provision of this signal removes the need for mechanical tachogenerators used in servo systems to provide loop stabilization and speed control.

Monolithic. A one-chip solution reduces the package size and increases the reliability.

Resolution Set by User. Two control pins are used to select the resolution of the AD2S83 to be 10, 12, 14 or 16 bits allowing the user to use the AD2S83 with the optimum resolution for each application.

Ratiometric Tracking Conversion. This technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and tolerance to harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low cost, preferred value resistors and capacitors, and the component values are easy to select using the free component selection software design aid.

MODELS AVAILABLE

Information on the models available is given in the section "Ordering Information."

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD2S83—SPECIFICATIONS ($\pm V_S$ = ±12 V dc ± 5%; V_L = +5 V dc ± 10%; T_A = −40°C to +85°C)

Parameter	Conditions	AD2S83J Min	Typ	Max	Units
SIGNAL INPUTS (SIN, COS)					
Frequency[1]		0		20,000	Hz
Voltage Level		1.8	2.0	2.2	V rms
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
REFERENCE INPUT (REF)					
Frequency		0		20,000	Hz
Voltage Level		1.0		8.0	V pk
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
PERFORMANCE					
Repeatability				1	LSB
Allowable Phase Shift	(Signals to Reference)	−10		+10	Degrees
Max Tracking Rate	10 Bits	1040			rps
	12 Bits	260			rps
	14 Bits	65			rps
	16 Bits	16.25			rps
Bandwidth	User Selectable				
ACCURACY					
Angular Accuracy	A			**±8 +1 LSB**	arc min
Monotonicity	Guaranteed Monotonic				
Missing Codes (16-Bit Resolution)	A			4	Codes
VELOCITY SIGNAL					
Linearity[2, 3, 4]	VCO Rate 0–500 kHz		±0.1	**±0.25**	%
	VCO Rate 500 kHz–1000 kHz		±0.25	**±1.0**	%
Reversion Error			±0.3	**±1.0**	% Output
DC Zero Offset[5]			±3		mV
Gain Scaling Accuracy			±1.5	**±3**	% FSR
Output Voltage	1 mA Load	±8			V
Dynamic Ripple	Mean Value			1.0	% rms O/P
INPUT/OUTPUT PROTECTION					
Analog Inputs	Overvoltage Protection		±8		V
Analog Outputs	Short Circuit O/P Protection	±5.6	±8	±10.4	mA
DIGITAL POSITION					
Resolution	10, 12, 14, and 16				Bits
Output Format	Bidirectional Natural Binary				
Load				3	LSTTL
$\overline{\text{INHIBIT}}$[6]					
Sense	Logic LO to $\overline{\text{INHIBIT}}$				
Time to Stable Data		240	390	490	ns
$\overline{\text{ENABLE}}$[6]	Logic LO Enables Position Output Logic HI Outputs in High				
$\overline{\text{ENABLE}}$[6]/Disable Time	Impedance State	35		110	ns
BYTE SELECT[6]					
Sense					
Logic HI	MS Byte DB1–DB8				
Logic LO	LS Byte DB1–DB8				
Time to Data Available		60		140	ns
SHORT CYCLE INPUTS	Internally Pulled High via 100 kΩ 100 kΩ to $+V_S$				
SC1 SC2					
0 0	10-Bit Resolution				
0 1	12-Bit Resolution				
1 0	14-Bit Resolution				
1 1	16-Bit Resolution				
$\overline{\text{COMPLEMENT}}$	Internally Pulled High via 100 kΩ to $+V_S$. Logic LO to Activate; No Connect for Normal Operation				

Parameter	Conditions	AD2S83 Min	Typ	Max	Units
$\overline{\text{DATA LOAD}}$ Sense	Internally Pulled High via 100 kΩ to $+V_S$. Logic LO Allows Data to be Loaded into the Counters from the Data Lines		150	300	ns
BUSY[6, 7] Sense	Logic HI When Position O/P Changing				
Width		200		350	ns
Load	Use Additional Pull-Up (See Figure 2)			1	LSTTL
DIRECTION[6] Sense	Logic HI Counting Up Logic LO Counting Down				
Max Load				3	LSTTL
RIPPLE CLOCK[6] Sense	Logic HI All 1s to All 0s All 0s to All 1s				
Width	Dependent on Input Velocity	300			ns
Reset	Before Next Busy				
Load				3	LSTTL
DIGITAL INPUTS Input High Voltage, V_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 11.4$ V, $V_L = 5.0$ V	2.0			V
Input Low Voltage, V_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 12.6$ V, $V_L = 5.0$ V			0.8	V
DIGITAL INPUTS Input High Current, I_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16 $\pm V_S = \pm 12.6$ V, $V_L = 5.5$ V			±100	μA
Input Low Current, I_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 12.6$ V, $V_L = 5.5$ V			±100	μA
DIGITAL INPUTS Low Voltage, V_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, $\overline{\text{DATA LOAD}}$ $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			1.0	V
Low Current, I_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, $\overline{\text{DATA LOAD}}$ $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			−400	μA
DIGITAL OUTPUTS High Voltage, V_{OH}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 4.5$ V $I_{OH} = 100$ μA	2.4			V
Low Voltage, V_{OL}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $I_{OL} = 1.2$ mA			0.4	V

NOTES
[1]Angular accuracy is not guaranteed <50 Hz reference frequency.
[2]Linearity Derates from 500 kHz–1000 kHz @ 0.0017%/kHz.
[3]Refer to Definition of Linearity, "The AD2S83 as a Silicon Tachogenerator."
[4]Worst case reversion error at temperature extremes.
[5]Velocity output offset dependent on value for R6.
[6]Refer to timing diagram.
[7]Busy pulse guaranteed up to a VCO rate of 900 kHz.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.
Specifications subject to change without notice.

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	V_{OL} = 0 V $\pm V_S$ = ±12.0 V, V_L = 5.5 V V_{OH} = 5.0 V			**±20**	µA
RATIO MULTIPLIER					
AC Error Output Scaling	10 Bit		177.6		mV/Bit
	12 Bit		44.4		mV/Bit
	14 Bit		11.1		mV/Bit
	16 Bit		2.775		mV/Bit
PHASE SENSITIVE DETECTOR					
Output Offset Voltage				**12**	mV
Gain					
In Phase	w.r.t. REF	−0.882	−0.9	−0.918	V rms/V dc
In Quadrature	w.r.t. REF			±0.02	V rms/V dc
Input Bias Current			60	**150**	nA
Input Impedance		1.0			MΩ
Input Voltage				±8	V
INTEGRATOR					
Open-Loop Gain	At 10 kHz	57	60	63	dB
Dead Zone Current (Hysteresis)		**90**	100	**110**	nA/LSB
Input Offset Voltage			1	5	mV
Input Bias Current			60	**150**	nA
Output Voltage Range		**±8**			V
VCO					
Maximum Rate		1.1			MHz
VCO Rate	+ve DIR	**8.25**	8.50	**8.75**	kHz/µA
	−ve DIR	**8.25**	8.50	**8.75**	kHz/µA
VCO Power Supply Sensitivity					
Rate	$+V_S$			+0.5	%/V
	$-V_S$			−0.5	%/V
Input Offset Voltage			3		mV
Input Bias Current			12	**50**	nA
Input Bias Current Tempco			+0.22		nA/°C
Linearity of Absolute Rate					
0 kHz–500 kHz			±0.1	**±0.15**	%
500 kHz–1000 kHz			±0.15	**±1.0**	%
Reversion Error			±0.3	**±0.5**	% Output
POWER SUPPLIES					
Voltage Levels					
$+V_S$		+11.4		+12.6	V
$-V_S$		−11.4		−12.6	V
$+V_L$		+4.5	+5	$+V_S$	V
Current					
$\pm I_S$	$\pm V_S$ @ ±12 V		±12	**±23**	mA
$\pm I_S$	$\pm V_S$ @ ±12.6 V		±19	**±30**	mA
$\pm I_L$	$+V_L$ @ ±5.0 V		±0.5	**±1.5**	mA

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Accuracy	Option*
AD2S83AP	−40°C to +85°C	8 arc min	P-44A

*P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS[1] (with respect to GND)

$+V_S$[2] . . . . . +13 V dc
$-V_S$[2] . . . . . −13 V dc
$+V_L$ . . . . . $+V_S$
Reference . . . . . +13 V to $-V_S$
SIN . . . . . +13 V to $-V_S$
COS . . . . . +13 V to $-V_S$
Any Logic Input . . . . . −0.4 V dc to $+V_L$ dc
Demodulator Input . . . . . +13 V to $-V_S$
Integrator Input . . . . . +13 V to $-V_S$
VCO Input . . . . . +13 V to $-V_S$
Power Dissipation . . . . . 800 mW
Operating Temperature
Industrial (AP) . . . . . −40°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

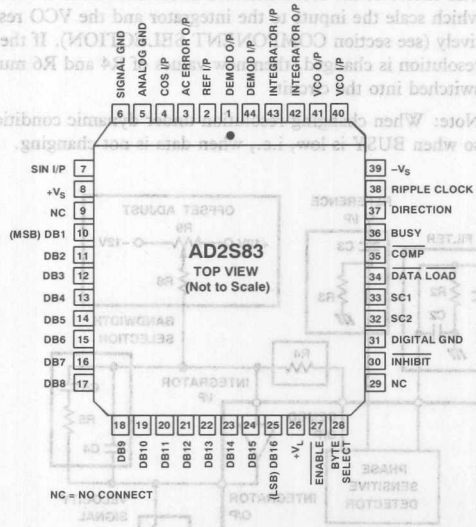
CAUTION:

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_S$, $-V_S$) . . . . . ±12 V dc ± 5%
Power Supply Voltage V_L . . . . . +5 V dc ± 10%
Analog Input Voltage (SIN and COS) . . . . . 2 V rms ± 10%
Analog Input Voltage (REF) . . . . . 1 V to 8 V peak
Signal and Reference Harmonic Distortion . . . . . 10% (max)
Phase Shift Between Signal and Reference . . . . . ±10 Degrees (max)
Ambient Operating Temperature Range
Industrial (AP) . . . . . −40°C to +85°C

PIN CONFIGURATION



PIN DESIGNATIONS

Pin Nos.	Mnemonic	Description
1	DEMOD O/P	Demodulator Output
2	REFERENCE I/P	Reference Signal Input
3	AC ERROR O/P	Ratio Multiplier Output
4	COS	Cosine Input
5	ANALOG GND	Power Ground
6	SIGNAL GND	Resolver Signal Ground
7	SIN	Sine Input
8	$+V_S$	Positive Power Supply
10–25	DB 1–DB 16	Parallel Output Data
26	$+V_L$	Logic Power Supply
27	$\overline{\text{ENABLE}}$	Logic HI–Output Data Pins in High Impedance State Logic LO–Presents Active Data to the Output Pins
28	BYTE SELECT	Logic HI–Most Significant Byte to DB1–DB8 Logic LO–Least Significant Byte to DB1–DB8
30	$\overline{\text{INHIBIT}}$	Logic LO Inhibits Data Transfer to Output Latches
31	DIGITAL GND	Digital Ground
32, 33	SC2–SC1	Select Converter Resolution
34	$\overline{\text{DATA LOAD}}$	Logic LO DB1–DB16 Inputs Logic HI DB1–DB16 Outputs
35	$\overline{\text{COMPLEMENT}}$	Active Logic LO
36	BUSY	Converter Busy, Data not Valid While Busy HI
37	DIRECTION	Logic State Defines Direction of Input Signal Rotation
38	RIPPLE CLOCK	Positive Pulse When Converter Output Changes from 1s to All 0s or Vice Versa
39	$-V_S$	Negative Power Supply
40	VCO I/P	VCO Input
41	VCO O/P	VCO Output
42	INTEGRATOR O/P	Integrator Output
43	INTEGRATOR I/P	Integrator Input
44	DEMOD I/P	Demodulator Input

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ESD SENSITIVITY

The AD2S83 features an input protection circuit consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charges Device Model).

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices *ESD Prevention Manual.*

Bit Weight Table

Binary Bits (N)	Resolution (N^N)	Degrees /Bit	Minutes /Bit	Seconds /Bit
0	1	360.0	21600.0	1296000.0
1	2	180.0	10800.0	648000.0
2	4	90.0	5400.0	324000.0
3	8	45.0	2700.0	162000.0
4	16	22.5	1350.0	81000.0
5	32	11.25	675.0	40500.0
6	64	5.625	337.5	20250.0
7	128	2.8125	168.75	10125.0
8	256	1.40625	84.375	5062.5
9	512	0.703125	42.1875	2531.25
10	1024	0.3515625	21.09375	1265.625
11	2048	0.1757813	10.546875	632.8125
12	4096	0.0878906	5.273438	316.40625
13	8192	0.0439453	2.636719	158.20313
14	16384	0.0219727	1.318359	79.10156
15	32768	0.0109836	0.659180	39.55078
16	65536	0.0054932	0.329590	19.77539
17	131072	0.0027466	0.164795	9.88770
18	262144	0.0013733	0.082397	4.94385

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be +12 V dc and −12 V dc and must not be reversed. The voltage applied to V_L can be +5 V dc to $+V_S$.

It is recommended that decoupling capacitors are connected in parallel between the power lines $+V_S$, $-V_S$ and ANALOG GROUND adjacent to the converter. Recommended values are 100 nF (ceramic) and 10 μF (tantalum). Also capacitors of 100 nF and 10 μF should be connected between $+V_L$ and DIGITAL GROUND adjacent to the converter.

When more than one converter is used on a card, separate decoupling capacitors should be used for each converter.

The resolver signal connections should be made to the SIN and COS inputs, REFERENCE INPUT and SIGNAL GROUND as shown in Figure 10 and described in section "CONNECTING THE RESOLVER."

The two signal ground wires from the resolver should be joined at the SIGNAL GROUND pin of the converter to minimize the coupling between the sine and cosine signals. For this reason it is also recommended that the resolver is connected using individually screened twisted pair cables with the sine, cosine and reference signals twisted separately.

SIGNAL GROUND and ANALOG GROUND are connected internally. ANALOG GROUND and DIGITAL GROUND must be connected externally and as close to the converter as possible.

The external components required should be connected as shown in Figure 1.

CONVERTER RESOLUTION

Two major areas of the AD2S83 specification can be selected by the user to optimize the total system performance. The resolution of the digital output is set by the logic state of the inputs SC1 and SC2 to be 10, 12, 14 or 16 bits; and the dynamic characteristics of bandwidth and tracking rate are selected by the choice of external components.

The choice of the resolution will affect the values of R4 and R6 which scale the inputs to the integrator and the VCO respectively (see section COMPONENT SELECTION). If the resolution is changed, then new values of R4 and R6 must be switched into the circuit.

Note: When changing resolution under dynamic conditions, do so when BUSY is low, i.e., when data is not changing.

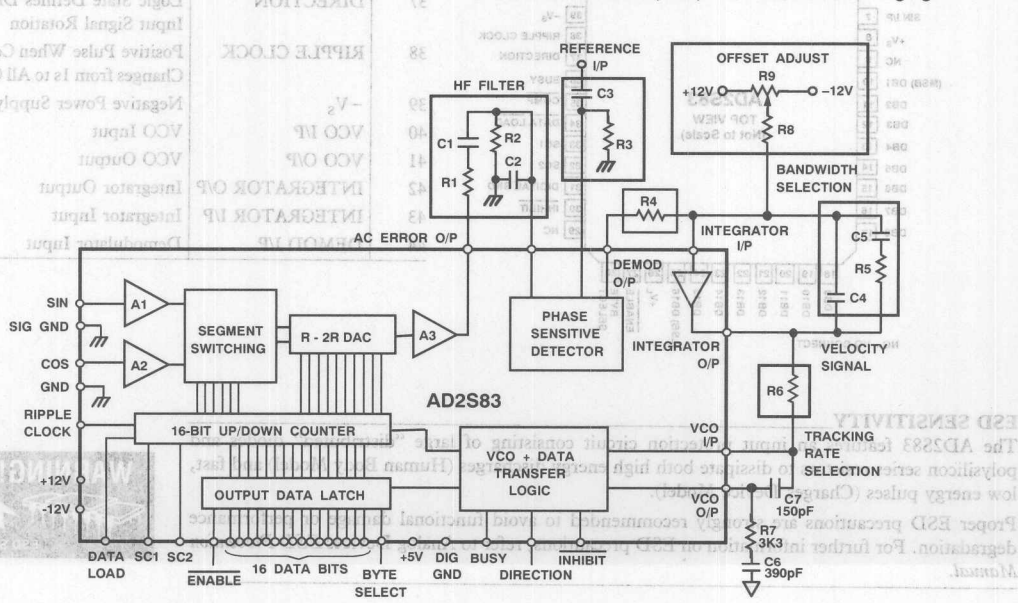


Figure 1. Connection Diagram

CONVERTER OPERATION

When connected in a circuit such as shown in Figure 10, the AD2S83 operates as a tracking resolver-to-digital converter. The output will automatically follow the input for speeds up to the selected maximum tracking rate. No convert command is necessary as the conversion is automatically initiated by each LSB increment, or decrement, of the input. Each LSB change of the converter initiates a BUSY pulse.

The AD2S83 is remarkably tolerant of input amplitude and frequency variation because the conversion depends only on the ratio of the input signals. Consequently there is no need for accurate, stable oscillator to produce the reference signal. The inclusion of the phase sensitive detector in the conversion loop ensures high immunity to signals that are not phase or frequency coherent or are in quadrature with the reference signal.

SIGNAL CONDITIONING

The amplitude of the SINE and COSINE signal inputs should be maintained within 10% of the nominal values if full performance is required from the velocity signal.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a loss in accuracy due to internal overload. Reducing levels will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3 LSB. At this level the repeatability will also degrade to 2 LSB and the dynamic response will also change, since the dynamic characteristics are proportional to the signal level.

The AD2S83 will not be damaged if the signal inputs are applied to the converter without the power supplies and/or the reference.

REFERENCE INPUT

The amplitude of the reference signal applied to the converter's input is not critical, but care should be taken to ensure it is kept within the recommended operating limits.

The AD2S83 will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

HARMONIC DISTORTION

The amount of harmonic distortion allowable on the signal and reference lines is 10%.

Square waveforms can be used but the input levels should be adjusted so that the average value is 1.9 V rms. (For example, a square wave should be 1.9 V peak.) Triangular and sawtooth waveforms should have a amplitude of 2 V rms.

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

POSITION OUTPUT

The resolver shaft position is represented at the converter output by a natural binary parallel digital word. As the digital position output of the converter passes through the major carries, i.e., all "1s" to all "0s" or the inverse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is always valid in advance of a RIPPLE CLOCK pulse and, as it is internally latched, only changing state (1 LSB min change in input) with a corresponding change in direction.

Both the RIPPLE CLOCK pulse and the DIRECTION data are unaffected by the application of the $\overline{\text{INHIBIT}}$. The static positional accuracy quoted is the worst case error that can occur over the full operating temperature excluding the effects of offset signals at the INTEGRATOR INPUT (which can be trimmed out – see Figure 1), and with the following conditions: input signal amplitudes are within 10% of the nominal; phase shift between signal and reference is less than 10 degrees.

These operating conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the AD2S83 can be used well outside these operating conditions providing the above points are observed.

VELOCITY SIGNAL

The tracking converter technique generates an internal signal at the output of the integrator (INTEGRATOR OUTPUT) that is proportional to the rate of change of the input angle. This is a dc analog output referred to as the VELOCITY signal.

It is recommended that the velocity output be buffered.

The sense is positive for an increasing angular input and negative for decreasing angular input. The full-scale velocity output is ±8 V dc. The output velocity scaling and tracking rate are a function of the resolution of the converter; this is summarized below.

Res	Max Tracking Rate (rps)	Nominal Scaling (rps/V dc)
10	1040	130
12	260	32.5
14	65	8.125
16	16.25	2.03

(Velocity O/P = ±8 V dc nominal)

The output velocity can be suitably scaled and used to replace a conventional DC tachogenerator. For more detailed information see "AD2S83 as a Silicon Tachogenerator" section.

DC ERROR SIGNAL

The signal at the output of the phase sensitive detector (DEMODULATOR OUTPUT) is the signal to be nulled by the tracking loop and is, therefore, proportional to the error between the input angle and the output digital angle. As the converter is a Type 2 servo loop, the demodulator output signal will increase if the output fails to track the input for any reason. This is an indication that the input has exceeded the maximum tracking rate of the converter or, due to some internal or external malfunction, the converter is unable to reach a null. By connecting two external comparators, this voltage can be used as a "built-in-test."

components for the converter in order to achieve the required bandwidth and tracking rate. In all cases the nearest "preferred value" component should be used, and a 5% tolerance will not degrade the overall performance of the converter. Care should be taken that the resistors and capacitors will function over the required operating temperature range. The components should be connected as shown in Figure 1.

Free PC compatible software is available to help users select the optimum component values for the AD2S83, and display the transfer gain, phase and small step response.

For more detailed information and explanation, see section "CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE."

1. HF Filter (R1, R2, C1, C2)
   The function of the HF filter is to remove any dc offset and to reduce the amount of noise present on the signal inputs to the AD2S83, reaching the Phase Sensitive Detector and affecting the outputs. R1 and C2 may be omitted – in which case R2 = R3 and C1 = C3, calculated below – but their use is particularly recommended if noise from switch mode power supplies and brushless motor drive is present.
   Values should be chosen so that
   $$15\ k\Omega \le R1 = R2 \le 56\ k\Omega$$
   $$C1 = C2 = \frac{1}{2\ \pi\ R1\ f_{REF}}$$
   and f_{REF} = Reference frequency (Hz)
   This filter gives an attenuation of 3 times at the input to the phase sensitive detector.
2. Gain Scaling Resistor (R4) (See Phase Sensitive Demodulator Section)
   If R1, C2 are fitted then:
   $$R4 = \frac{E_{DC}}{100 \times 10^{-9}} \times \frac{1}{3}\ \Omega$$
   where 100×10^{-9} = current/LSB
   If R1, C2 are not fitted then:
   $$R4 = \frac{E_{DC}}{100 \times 10^{-9}}\ \Omega$$
   where E_{DC} = 160×10^{-3} for 10 bits resolution
   = 40×10^{-3} for 12 bits
   = 10×10^{-3} for 14 bits
   = 2.5×10^{-3} for 16 bits
   = Scaling of the DC ERROR in volts/LSB
3. AC Coupling of Reference Input (R3, C3)
   Select R3 and C3 so that there is no significant phase shift at the reference frequency. That is,
   $$R3 = 100\ k\Omega$$
   $$C3 > \frac{1}{R3 \times f_{REF}}\ F$$
   with R3 in Ω.
4. Maximum Tracking Rate (R6)
   The VCO input resistor R6 sets the maximum tracking rate of the converter and hence the velocity scaling as at the max tracking rate, the velocity output will be 8 V.
   remembered that the linearity of the velocity output is specified across 0 kHz–500 kHz and 500 kHz–1000 kHz. The following conversion can be used to determine the corresponding rps:
   $$rps = \frac{VCO\ Rate\ (Hz)}{2^N}$$
   Note that "T" must not exceed the maximum tracking rate or 1/16 of the reference frequency.
   $$R6 = \frac{6.81 \times 10^{10}}{T \times n}\ \Omega$$
   where n = bits per revolution
   = 1,024 for 10 bits resolution
   = 4,096 for 12 bits
   = 16,384 for 14 bits
   = 65,536 for 16 bits
5. Closed-Loop Bandwidth Selection (C4, C5, R5)
   a. Choose the closed-loop bandwidth (f_{BW}) required ensuring that the ratio of reference frequency to bandwidth does not exceed the following guidelines:

Resolution	Ratio of Reference Frequency/Bandwidth
10	2.5 : 1
12	4 : 1
14	6 : 1
16	7.5 : 1

   Typical values may be 100 Hz for a 400 Hz reference frequency and 500 Hz to 1000 Hz for a 5 kHz reference frequency.
   b. Select C4 so that
   $$C4 = \frac{21}{R6 \times f_{BW}^2}\ F$$
   with R6 in Ω and f_{BW} in Hz selected above.
   c. C5 is given by
   $$C5 = 5 \times C4$$
   d. R5 is given by
   $$R5 = \frac{4}{2 \times \pi \times f_{BW} \times C5}\ \Omega$$
6. VCO Phase Compensation
   The following values of C6 and R7 should be connected as close as possible to the VCO output, Pin 41.
   $$C6 = 390\ pF,\ R7 = 3.3\ k\Omega$$
7. VCO Optimization
   To optimize the performance of the VCO a capacitor, C7, should be placed across the VCO input and output, Pins 40 and 41.
   $$C7 = 150\ pF$$
8. Offset Adjust
   Offsets and bias currents at the integrator input can cause an additional positional offset at the output of the converter of 1 arc minute typical, 5.3 arc minutes maximum. If this can be tolerated, then R8 and R9 can be omitted from the circuit.
   If fitted, the following values of R8 and R9 should be used:
   $$R8 = 4.7\ M\Omega,\ R9 = 1\ M\Omega\ potentiometer$$

To adjust the zero offset, ensure the resolver is disconnected and all the external components are fitted. Connect the COS pin to the REFERENCE INPUT and the SIN pin to the SIGNAL GROUND and with the power and reference applied, adjust the potentiometer to give all "0s" on the digital output bits.

The potentiometer may be replaced with select on test resistors if preferred.

DATA TRANSFER

To transfer data the $\overline{\text{INHIBIT}}$ input should be used. The data will be valid 490 ns after the application of a logic "LO" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied and allows time for an active BUSY to clear. By using the $\overline{\text{ENABLE}}$ input the two bytes of data can be transferred after which the $\overline{\text{INHIBIT}}$ should be returned to a logic "HI" state to enable the output latches to be updated.

BUSY Output

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses at TTL levels. A BUSY pulse is initiated each time the input moves by the analog equivalent of one LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

$\overline{\text{ENABLE}}$ Input

The $\overline{\text{ENABLE}}$ input determines the state of the output data. A logic "HI" maintains the output data pins in the high impedance condition, and the application of a logic "LO" presents the data in the latches at the output pins. The operation of the $\overline{\text{ENABLE}}$ has no effect on the conversion process.

BYTE SELECT Input

The BYTE SELECT input selects the byte of the position data to be presented at the data output pins DB1 to DB8. The least significant byte will be presented on data output pins DB9 to DB16 (with the $\overline{\text{ENABLE}}$ input taken to a logic "LO") regardless of the state of the BYTE SELECT pin. Note that when the AD2S83 is used with a resolution less than 16 bits the unused data lines are pulled to a logic "LO." A logic "HI" on the BYTE SELECT input will present the eight most significant data bits on data output pins DB1 through DB8. A logic "LO" will present the least significant byte on data outputs 1 to 8, i.e., data outputs 1 to 8 will duplicate data outputs 9 to 16.

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

RIPPLE CLOCK

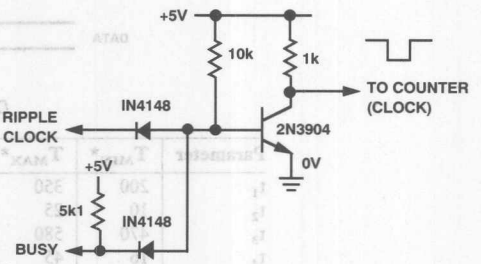
As the output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a positive going edge on the RIPPLE CLOCK (RC) output is initiated indicating that a revolution, or a pitch, of the input has been completed.

The minimum pulse width of the ripple clock is 300 ns. RIPPLE CLOCK is normally set high before a BUSY pulse and resets before the next positive going edge of the next busy pulse.

The only exception to this is when DIR changes while the RIPPLE CLOCK is high. Resetting of the RIPPLE clock will only occur if the DIR remains stable for two consecutive positive BUSY pulse edges.

If the AD2S83 is being used in a pitch and revolution counting application, the ripple and busy will need to be gated to prevent false decrement or increment (see Figure 2).

RIPPLE CLOCK is unaffected by $\overline{\text{INHIBIT}}$.



NOTE: DO NOT USE ABOVE CCT WHEN $\overline{\text{INHIBIT}}$ IS LOW.

Figure 2. Diode Transistor Logic Nand Gate

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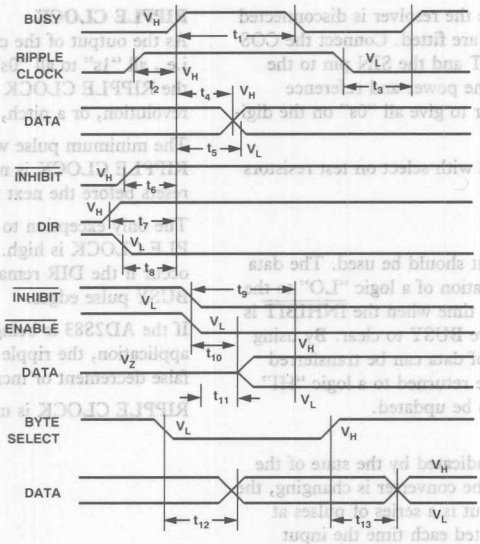

Digital Timing

Parameter	T_{MIN}*	T_{MAX}*	Condition
t_1	200	350	BUSY WIDTH V_H–V_H
t_2	10	25	RIPPLE CLOCK V_H to BUSY V_H
t_3	470	580	RIPPLE CLOCK V_L to Next BUSY V_H
t_4	16	45	BUSY V_H to DATA V_H
t_5	3	25	BUSY V_H to DATA V_L
t_6	70	140	$\overline{\text{INHIBIT}}$ V_H to BUSY V_H
t_7	485	625	MIN DIR V_H to BUSY V_H
t_8	515	670	MIN DIR V_H to BUSY V_H
t_9	–	490	$\overline{\text{INHIBIT}}$ V_L to DATA STABLE
t_{10}	40	110	$\overline{\text{ENABLE}}$ V_L to DATA V_H
t_{11}	35	110	$\overline{\text{ENABLE}}$ V_L to DATA V_L
t_{12}	60	140	BYTE SELECT V_L to DATA STABLE
t_{13}	60	125	BYTE SELECT V_H to DATA STABLE

*ns

DIRECTION Output

The DIRECTION (DIR) output indicates the direction of the input rotation. Any change in the state of DIR precedes the corresponding BUSY, DATA and RIPPLE CLOCK updates. DIR can be considered as an asynchronous output and can make multiple changes in state between two consecutive LSB update cycles. This occurs when the direction of rotation of the input changes but the magnitude of the rotation is less than 1 LSB.

$\overline{\text{COMPLEMENT}}$

The $\overline{\text{COMPLEMENT}}$ input is an active low input and is internally pulled to $+V_S$ via 100 kΩ.

Strobing $\overline{\text{DATA LOAD}}$ and $\overline{\text{COMPLEMENT}}$ pins to logic LO will set the logic HI bits of the AD2S83 counter to a LO state. Those bits of the applied data which are logic LO will not change the corresponding bits in the AD2S83 counter.

For Example:

Initial Counter State	1 0 1 0 1
Applied Data Word	1 1 0 0 0
Counter State after $\overline{\text{DATA LOAD}}$	1 1 0 0 0
Initial Counter State	1 0 1 0 1
Applied Data Word	1 1 0 0 0
Counter State after $\overline{\text{DATA LOAD}}$ and Complement	0 0 1 0 1

In order to read the counter following a $\overline{\text{DATA LOAD}}$, the procedure below should be followed:

1. Place Outputs in high impedance state ($\overline{\text{ENABLE}}$ = HI).
2. Present data to pins.
3. Pull $\overline{\text{DATA LOAD}}$ and $\overline{\text{COMPLEMENT}}$ pins to ground.
4. Wait 100 ns.
5. Remove data from pins.
6. Remove outputs from high impedance state ($\overline{\text{ENABLE}}$ = LO).
7. Read outputs.

VELOCITY ERRORS

Some "ripple" or noise will always be present in the velocity signal. Velocity signal ripple is caused by, or related to, the following parameters. The resulting effects are generally additive. This means diagnosis needs to be an iterative process in order to define the source of the error.

1.0 Reference Frequency
A ripple content at the reference frequency is superimposed on the velocity signal output. The amplitude depends on the loop bandwidth. This error is a function of a dc offset at the input to Phase Sensitive Demodulator (PSD).

2.0 Resolver Inaccuracies
Impedance mismatch occur in the sine and cosine windings of the resolver. These give rise to differential phase shift between the sine and cosine inputs to the RDC and variations in the resolver output amplitudes.

2.1 Sine and Cosine Amplitude Mismatch —
This is normally identified by the presence of asymmetrical ripple voltages.

2.2 Differential Phase Shift between the Sine and Cosine Inputs
The frequency of this ripple is usually twice the input velocity, and the amplitude is proportional to the magnitude of the velocity signal. The phase shift is normally induced through the connections from the resolver to the converter. Maintaining equal lengths of screened twisted pair cable from the resolver to the AD2S83 will reduce the effects of resistive imbalance, and therefore, reduce differential phase shift.

3.0 LSB Update Ripple
LSB update noise occurs as the resolver rotates and the digital outputs of the RDC are updated. For a correctly scaled loop, this ripple component has a magnitude of approximately 2 mV peak at 16-bit resolution.

3.1 Ripple due to the LSB rate given by:

$$\text{LSB rate} = N \times \text{Reference Frequency}$$

The PSD generates sums and differences of all its component input frequencies, so when the LSB update rate is an multiple of the reference frequency, a beat frequency is generated. The magnitude of this ripple is a function of the LSB weighting, i.e., ripple is less at 16 bits.

4.0 Torque Ripple
Torque ripple is a phenomenon associated with motors. An ac motor naturally exhibits a sinusoidal back emf. In an ideal system the current fed to the motor should, in order to cancel, also be sinusoidal. In practice the current is often trapezoidal. Consequently, the output torque from the motor will not be smooth and torque ripple is created. If the loading on a motor is constant, the velocity of the motor shaft will vary as a result of the cyclic variation of motor torque. The variation in velocity then appears on the velocity output as ripple. This is not an error but a true velocity variation in the system.

Offset Errors

The limiting factor in the measuring of low or "creep" speeds is the level of dc offset present at zero velocity. The zero velocity dc offset at the output of the AD2S83 is a function of the input bias current to the VCO and the value for the input resistor R6. See "Circuit Functions and Dynamic Performance VCO."

The offset can be minimized by reducing the maximum tracking rate so reducing the value for R6. Offset is a function of tracking rate and therefore resolution; the dc offset is lowest at 16 bits. To increase the dynamic range of the velocity dynamic resolution switching can be employed. (Contact MCG Applications for more information.)

CONNECTING THE RESOLVER

The recommended connection circuit is shown in Figure 10.

In cases where the reference phase relative to the input signals from the resolver requires adjustment, this can be easily achieved by varying the value of the resistor R2 of the HF filter (see Figure 1).

Assume that R1 = R2 = R and C1 = C2 = C

and Reference Frequency $= \dfrac{1}{2\pi RC}$.

By altering the value of R2, the phase of the reference relative to the input signals will change in an approximately linear manner for phase shifts of up to 10 degrees.

Increasing R2 by 10% introduces a phase lag of 2 degrees. Decreasing R2 by 10% introduces a phase lead of 2 degrees.

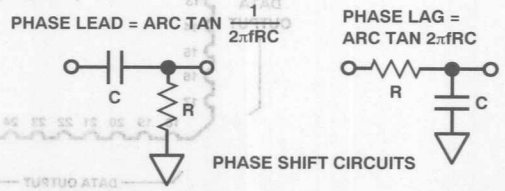

Figure 9. Phase Shift Circuits

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TYPICAL CIRCUIT CONFIGURATION

Figure 10 shows a typical circuit configuration for the AD2S83 with 12-bit resolution. Values of the external components have been chosen for a reference frequency of 5 kHz and a maximum tracking rate of 260 rps with a bandwidth of 520 Hz. Placing the values for R4, R6, C4 and C5 in the equation for K_A gives a value of 2.7×10^6. The resistors are 0.125 W, 5% tolerance preferred values. The capacitors are 100 V ceramic, 10% tolerance components.

For signal and reference voltages greater than 2 V rms a simple voltage divider circuit of resistors can be used to generate the correct signal level at the converter. Care should be taken to ensure that the ratios of the resistors between the sine signal line and ground and the cosine signal line and ground are the same. Any difference will result in an additional position error.

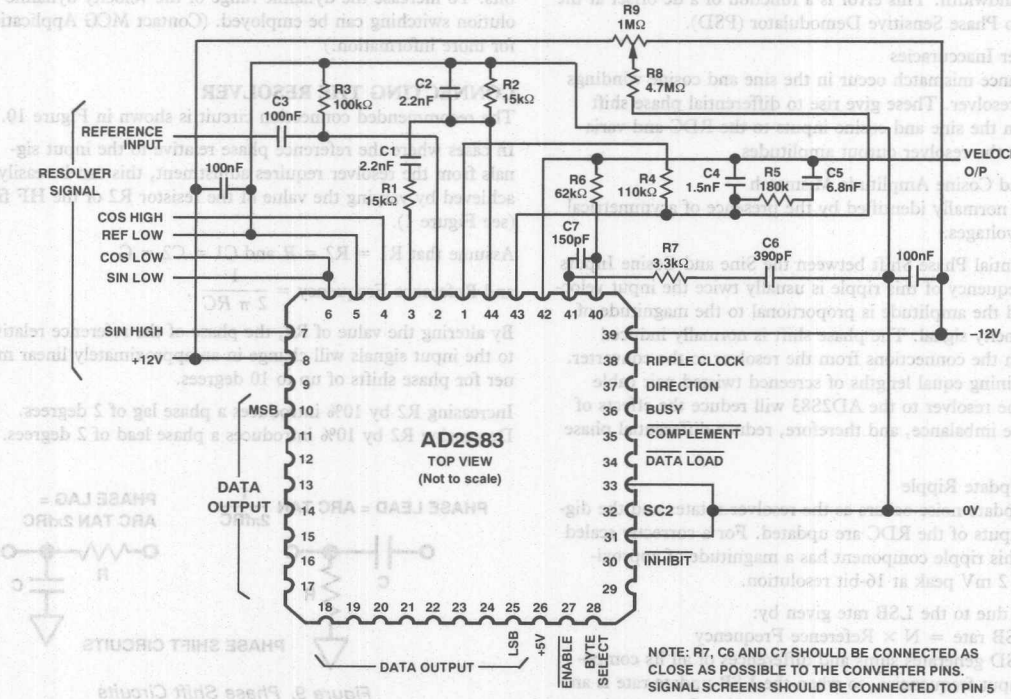


Figure 10. Typical Circuit Configuration

Low Cost, Complete 12-Bit Resolver-to-Digital Converter

AD2S90

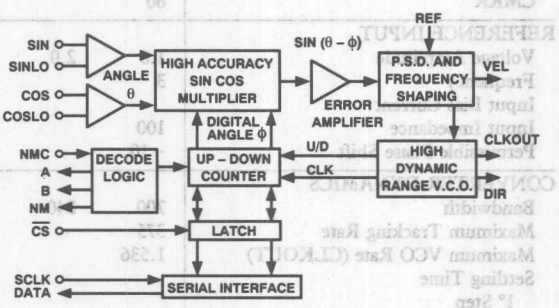
FEATURES

Complete Monolithic Resolver-to-Digital Converter
Incremental Encoder Emulation (1024-Line)
Absolute Serial Data (12-Bit)
Differential Inputs
12-Bit Resolution
Industrial Temperature Range
20-Pin PLCC
Low Power (50 mW)

APPLICATIONS

Industrial Motor Control
Servo Motor Control
Industrial Gauging
Encoder Emulation
Automotive Motion Sensing and Control
Factory Automation
Limit Switching

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S90 is a complete 12-bit resolution tracking resolver-to-digital converter. No external components are required to operate the device.

The converter accepts 2 V rms ± 10% input signals in the range 3–20 kHz on the SIN, COS and REF inputs. A Type II servo loop is employed to track the inputs and convert the input SIN and COS information into a digital representation of the input angle. The bandwidth of the converter is set internally at 1 kHz. The maximum tracking rate is 375 rps at 12-bit resolution.

Angular position output information is available in two forms, absolute serial binary and incremental A quad B.

The absolute serial binary output is 12-bit (1 in 4096). The data output pin is high impedance when Chip Select $\overline{CS}$ is logic HI. This allows the connection of multiple converters onto a common bus. Absolute angular information in serial pure binary form is accessed by $\overline{CS}$ followed by the application of an external clock (SCLK) with a maximum rate of 2 MHz.

The encoder emulation outputs A, B and NM continuously produce signals equivalent to a 1024 line encoder. When decoded this corresponds to 12-bits resolution. Three common north marker pulse widths are selected via a single pin (NMC).

An analog velocity output signal provides a representation of velocity from a rotating resolver shaft travelling in either a clockwise or counterclockwise direction.

The AD2S90 operates on a ±5 V dc ± 5% power supplies and is fabricated on Analog Devices' Linear Compatible CMOS process (LC^2MOS). LC^2MOS is a mixed technology process that combines precision bipolar circuits with low power CMOS logic circuits.

PRODUCT HIGHLIGHTS

Complete Resolver–Digital Interface. The AD2S90 provides the complete solution for digitizing resolver signals (12-bit resolution) without the need for external components.

Dual Format Position Data. Incremental encoder emulation in standard A QUAD B format with selectable North Marker width. Absolute serial 12-bit angular binary position data accessed via simple 3-wire interface.

Single High Accuracy Grade in Low Cost Package. ±10.6 arc minutes of angular accuracy available in a 20-pin PLCC.

Low Power. Typically 50 mW power consumption.

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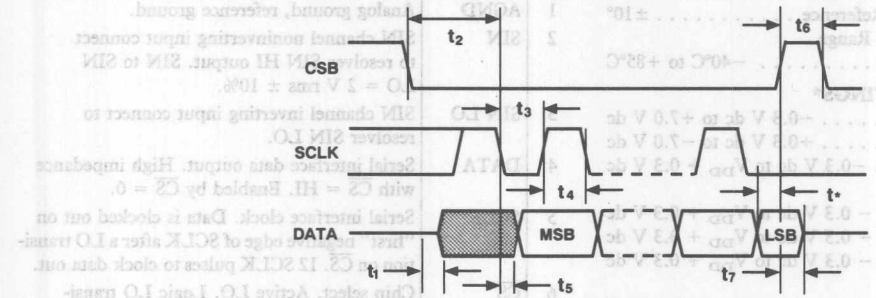
Voltage Amplitude	1.8	2.0	2.2	V rms	Differential SIN to SIN LO, COS to COS LO
Frequency	3		20	kHz	
Input Bias Current			100	nA	V_{IN} = 2 ± 10% V rms
Input Impedance	1.0			MΩ	V_{IN} = 2 ± 10% V rms
Common-Mode Volts[1]			100	mV peak	CMV @ SINLO, COSLO w.r.t.
CMRR	60			dB	AGND @ 10 kHz
REFERENCE INPUT					
Voltage Amplitude	1.8	2.0	3.35	V rms	
Frequency	3		20	kHz	
Input Bias Current			100	nA	
Input Impedance	100			kΩ	
Permissible Phase Shift	−10		+10	Degrees	Relative to SIN, COS Inputs
CONVERTER DYNAMICS					
Bandwidth	700	840	1000	Hz	
Maximum Tracking Rate	375			rps	
Maximum VCO Rate (CLKOUT)	1.536			MHz	
Settling Time					
1° Step			7	ms	
179° Step			20	ms	
ACCURACY					
Angular Accuracy[2]			±10.6 +1 LSB	arc min	
Repeatability[3]			1	LSB	
VELOCITY OUTPUT					
Scaling	127.5	150	172.5	rps/V dc	
Output Voltage at max rps	±2.17		±2.875	V dc	
Load Drive Capability			±250	μA	V_{OUT} = ±2.5 V dc
LOGIC INPUTS SCLK, $\overline{CS}$					
Input High Voltage (V_{INH})	3.5			V dc	V_{DD} = +5 V dc, V_{SS} = −5 V dc
Input Low Voltage (V_{INL})			1.5	V dc	V_{DD} = +5 V dc, V_{SS} = −5 V dc
Input Current (I_{IN})			10	μA	
Input Capacitance			10	pF	
LOGIC OUTPUTS DATA, A, B,[4] NM, CLKOUT, DIR					V_{DD} = +5 V dc, V_{SS} = −5 V dc
Output High Voltage	4.0			V dc	I_{OH} = 1 mA
Output Low Voltage			1.0	V dc	I_{OL} = 1 mA
			0.4	V dc	I_{OL} = 400 μA
SERIAL CLOCK (SCLK)					
SCLK Input Rate			2	MHz	1:1 Mark Space Ratio
NORTH MARKER CONTROL (NMC)					
90°	+4.75	+5.0	+5.25	V dc	North Marker Width Relative to
180°	−0.75	DGND	+0.75	V dc	to "A" Cycle
360°	−4.75	−5.0	−5.25	V dc	
POWER SUPPLIES					
V_{DD}	+4.75	+5.00	+5.25	V dc	
V_{SS}	−4.75	−5.00	−5.25	V dc	
I_{DD}			7	mA	
I_{SS}			9	mA	

NOTES
[1]If the tolerance on signal inputs = ±5%, then CMV = 200 mV.
[2]1 LSB = 5.3 arc minute.
[3]Specified at constant temperature.
[4]Output load drive capability.
Specifications subject to change without notice.

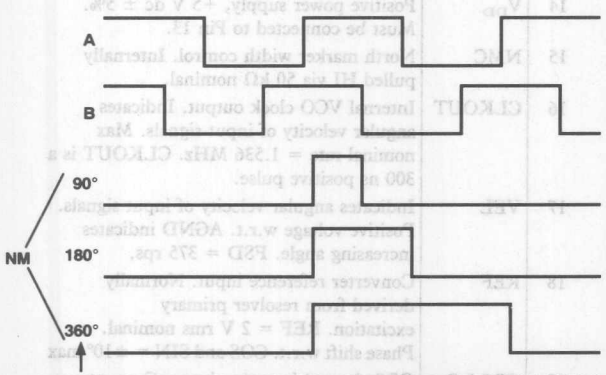


* THE MINIMUM ACCESS TIME: USER DEPENDENT

Serial Interface

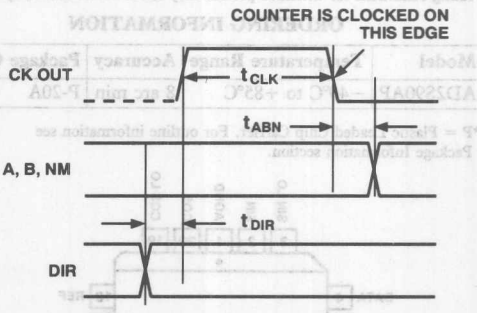
Parameter	AD2S90	Units	Test Conditions/Notes
t_1	150	ns max	$\overline{CS}$ to DATA Enable
t_2[1]	600	ns min	$\overline{CS}$ to 1st SCLK Negative Edge
t_3	250	ns min	SCLK Low Pulse
t_4	250	ns min	SCLK High Pulse
t_5	100	ns max	SCLK Negative Edge to DATA Valid
t_6	600	ns min	$\overline{CS}$ High Pulse Width
t_7	150	ns max	$\overline{CS}$ High to DATA High Z (Bus Relinquish)

[1]SCLK can only be applied after t_2 has elapsed.



NUMBER OF DEGREES REFERS TO WIDTH RELATIVE TO " A " CYCLE

Incremental Encoder



DIR/CLKOUT/AB and NM Timing

Parameter	AD2S90 Min	AD2S90 Max	Units	Test Conditions/Notes
t_{DIR}		200	ns	DIR to CLKOUT Positive Edge
t_{CLK}	250	400	ns	CLKOUT Pulse Width
t_{ABN}		250	ns	CLKOUT Negative Edge to A, B & NM Transition

NOTES

[1]Timing data are not 100% production tested. Sample tested at +25°C only to ensure conformance to data sheet limits. Logic output timing tests carried out using 10 pF, 100 kΩ load.

[2]Capacitance of data pin in high impedance state = 15 pF.

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RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage (V_{DD}–V_{SS}) . . . . . ±5 V dc ± 5%
Analog Input Voltage (SIN, COS & REF) . . . 2 V rms ± 10%
Signal and Reference Harmonic Distortion 10%
Phase Shift between Signal and Reference . . . . . ±10°
Ambient Operating Temperature Range
Industrial (AP) . . . . . −40°C to +85°C

ABSOLUTE MAXIMUM RATINGS*

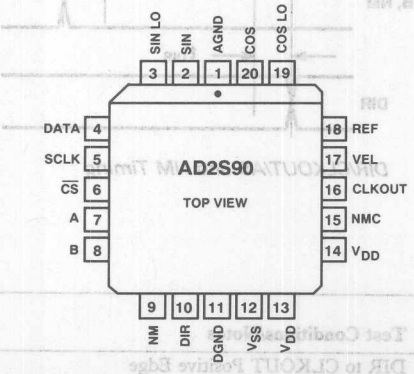
V_{DD} to AGND . . . . . −0.3 V dc to +7.0 V dc
V_{SS} to AGND . . . . . +0.3 V dc to −7.0 V dc
AGND to DGND . . . . . −0.3 V dc to V_{DD} + 0.3 V dc
Analog Inputs to AGND
REF . . . . . V_{SS} − 0.3 V dc to V_{DD} + 0.3 V dc
SIN, SIN LO . . . . . V_{SS} − 0.3 V dc to V_{DD} + 0.3 V dc
COS, COS LO . . . . . V_{SS} − 0.3 V dc to V_{DD} + 0.3 V dc
Analog Output to AGND
VEL . . . . . V_{SS} to V_{DD}
Digital Inputs to DGND, CSB,
SCLK, RES . . . . . −0.3 V dc to V_{DD} + 0.3 V dc
Digital Outputs to DGND, NM, A, B,
DIR, CLKOUT DATA . . . . −0.3 V dc to V_{DD} + 0.3 V dc
Operating Temperature Range
Industrial (AP) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 secs) . . . . . 300°C
Power Dissipation to +75°C . . . . . 300 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Model	Temperature Range	Accuracy	Package Option*
AD2S90AP	−40°C to +85°C	8 arc min	P-20A

*P = Plastic Leaded Chip Carrier. For outline information see Package Information section.



PIN DESCRIPTIONS

Pin No.	Mnemonic	Function
1	AGND	Analog ground, reference ground.
2	SIN	SIN channel noninverting input connect to resolver SIN HI output. SIN to SIN LO = 2 V rms ± 10%.
3	SIN LO	SIN channel inverting input connect to resolver SIN LO.
4	DATA	Serial interface data output. High impedance with $\overline{CS}$ = HI. Enabled by $\overline{CS}$ = 0.
5	SCLK	Serial interface clock. Data is clocked out on "first" negative edge of SCLK after a LO transition on $\overline{CS}$. 12 SCLK pulses to clock data out.
6	$\overline{CS}$	Chip select. Active LO. Logic LO transition enables DATA output.
7	A	Encoder A output. A leads B for increasing angular rotation.
8	B	Encoder B output.
9	NM	Encoder North Marker emulation output. Pulse triggered as code passes through zero. Three common pulse widths available.
10	DIR	Indicates direction of rotation of input. Logic HI = increasing angular rotation. Logic LO = decreasing angular rotation.
11	DGND	Digital power ground return.
12	V_{SS}	Negative power supply, −5 V dc ± 5%.
13	V_{DD}	Positive power supply, +5 V dc ± 5%.
14	V_{DD}	Positive power supply, +5 V dc ± 5%. Must be connected to Pin 13.
15	NMC	North marker width control. Internally pulled HI via 50 kΩ nominal.
16	CLKOUT	Internal VCO clock output. Indicates angular velocity of input signals. Max nominal rate = 1.536 MHz. CLKOUT is a 300 ns positive pulse.
17	VEL	Indicates angular velocity of input signals. Positive voltage w.r.t. AGND indicates increasing angle. FSD = 375 rps.
18	REF	Converter reference input. Normally derived from resolver primary excitation. REF = 2 V rms nominal. Phase shift w.r.t. COS and SIN = ±10° max
19	COS LO	COS channel inverting input. Connect to resolver COS LO.
20	COS	COS channel noninverting input. Connect to resolver COS HI output. COS = 2 V rms ± 10%.

ESD SENSITIVITY

The AD2S90 features an input protection circuit consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charges Device Model).

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices *ESD Prevention Manual.*

RESOLVER FORMAT SIGNALS

A resolver is a rotating transformer which has two stator windings and one rotor winding. The stator windings are displaced mechanically by 90° (see Figure 1). The rotor is excited with an ac reference. The amplitude of subsequent coupling onto the stator windings is a function of the position of the rotor (shaft) relative to the stator. The resolver, therefore, produces two output voltages (S3–S1, S2–S4) modulated by the SINE and COSINE of shaft angle. Resolver format signals refer to the signals derived from the output of a resolver. Equation 1 illustrates the output form.

$$S3\text{–}S1 = E_O\ SIN\ \omega t \cdot SIN\theta$$
$$S2\text{–}S4 = E_O\ SIN\ \omega t \cdot COS\theta \quad (1)$$

where: θ = shaft angle
$SIN\ \omega t$ = rotor excitation frequency
E_O = rotor excitation amplitude

Principle of Operation

The AD2S90 operates on a Type 2 tracking closed-loop principle. The output continually tracks the position of the resolver without the need for external convert and wait states. As the transducer moves through a position equivalent to the least significant bit weighting, the output is updated by one LSB.

On the AD2S90, CLKOUT updates corresponding to one LSB increment. If we assume that the current word state of the up-down counter is ϕ, S3–S1 is multiplied by COS ϕ and S2–S4 is multiplied by SIN ϕ to give:

$$E_O\ SIN\ \omega t \cdot SIN\ \theta\ COS\phi$$
$$E_O\ SIN\ \omega t \cdot COS\ \theta\ SIN\phi \quad (2)$$

An error amplifier subtracts these signals giving:

$$E_O\ SIN\ \theta \cdot (SIN\ \theta\ COS\ \phi – COS\ \theta\ SIN\ \phi)$$

or

$$E_O\ SIN\ \omega t \cdot SIN\ (\theta–\phi) \quad (3)$$

where $(\theta–\phi)$ = angular error

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null sin $(\theta–\phi)$. When this is accomplished the word state of the up/down counter, ϕ, equals within the rated accuracy of the converter, the resolver shaft angle θ.

For more information on the operation of the converter, see Circuit Dynamics section.

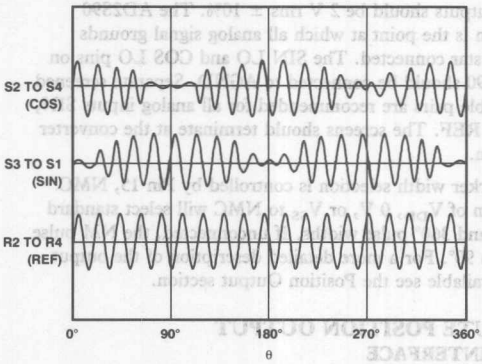


Figure 1. Electrical and Physical Resolver Representation

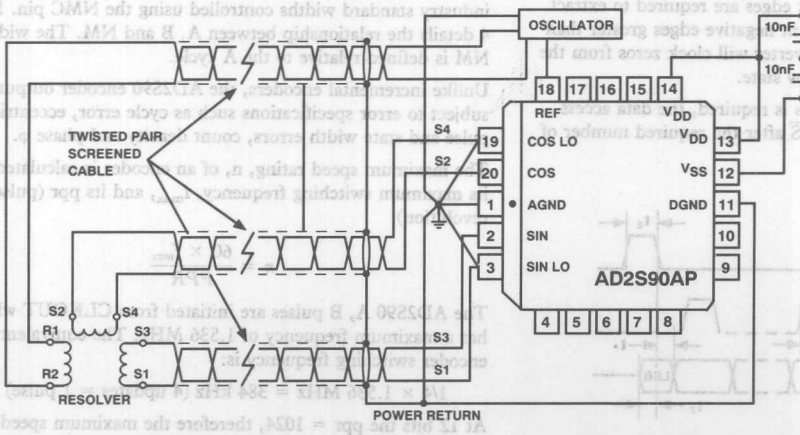


Figure 2. Connecting the AD2S90 to a Resolver

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Refer to Figure 2. Positive power supply V_{DD} = +5 V dc ± 5% should be connected to Pin 13 & Pin 14 and negative power supply V_{SS} = −5 V dc ± 5% to Pin 12. **Reversal of these power supplies will destroy the device.** S3 (SIN) and S2 (COS) from the resolver should be connected to the SIN and COS pins of the converter. S1 (SIN) and S4 (COS) from the resolver should be connected to the SINLO and COSLO pins of the converter. The maximum signal level of either the SIN or COS resolver outputs should be 2 V rms ± 10%. The AD2S90 AGND pin is the point at which all analog signal grounds should be star connected. The SIN LO and COS LO pins on the AD2S90 should be connected to AGND. Separate screened twisted cable pairs are recommended for all analog inputs SIN, COS, and REF. The screens should terminate at the converter AGND pin.

North marker width selection is controlled by Pin 15, NMC. Application of V_{DD}, 0 V, or V_{SS} to NMC will select standard 90°, 180° and 360° pulse widths. If unconnected, the NM pulse defaults to 90°. For a more detailed description of the output formats available see the Position Output section.

ABSOLUTE POSITION OUTPUT

SERIAL INTERFACE

Absolute angular position is represented by serial binary data and is extracted via a three wire interface, DATA, $\overline{CS}$ and SCLK. The DATA output is held in a high impedance state when $\overline{CS}$ is HI.

Upon the application of a Logic LO to the $\overline{CS}$ pin, the DATA output is enabled and the current angular information is transferred from the counters to the serial interface. Data is retrieved by applying an external clock to the SCLK pin. The maximum data rate of the SCLK is 2 MHz. To ensure secure data retrieval it is important to note that SCLK should not be applied until a minimum period of 600 ns after the application of a Logic LO to $\overline{CS}$. Data is then clocked out, MSB first, on successive negative edges of the SCLK; 12 clock edges are required to extract the full 12 bits of data. Subsequent negative edges greater than the defined resolution of the converter will clock zeros from the data output if $\overline{CS}$ remains in a low state.

If a resolution of less than 12 bits is required, the data access can be terminated by releasing $\overline{CS}$ after the required number of bits have been read.

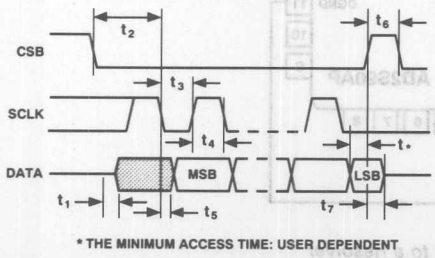

Figure 3. Serial Read Cycle

$\overline{CS}$ can be released a minimum of 100 ns after the last negative edge. If the user is reading data continuously, $\overline{CS}$ can be reapplied a minimum of 250 ns after it is released (see Figure 3).

Max RD Time = [600 + (12 × 500) + 600 + 100] = 7.50 µs.

INCREMENTAL ENCODER OUTPUTS

The incremental encoder emulation outputs A, B and NM are free running and are always valid, providing that valid resolver format input signals are applied to the converter.

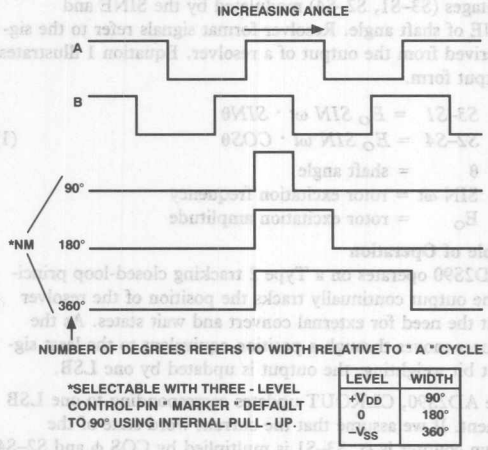

Figure 4. A, B & NM Timing

The AD2S90 emulates a 1024-line encoder. Relating this to converter resolution means one revolution produces 1024 A, B pulses. A leads B for increasing angular rotation. The addition of the DIR output negates the need for external A and B direction decode logic. DIR is HI for increasing angular rotation.

The north marker pulse is generated as the absolute angular position passes through zero. The AD2S90 supports the three industry standard widths controlled using the NMC pin. Figure 4 details the relationship between A, B and NM. The width of NM is defined relative to the A cycle.

Unlike incremental encoders, the AD2S90 encoder output is not subject to error specifications such as cycle error, eccentricity, pulse and state width errors, count density and phase φ.

The maximum speed rating, n, of an encoder is calculated from its maximum switching frequency, f_{max}, and its ppr (pulses per revolution).

$$n = \frac{60 \times f_{max}}{PPR}$$

The AD2S90 A, B pulses are initiated from CLKOUT which has a maximum frequency of 1.536 MHz. The equivalent encoder switching frequency is:

1/4 × 1.536 MHz = 384 kHz (4 updates = 1 pulse)

At 12 bits the ppr = 1024, therefore the maximum speed, n, of the AD2S90 is:

$$n = \frac{60 \times 384000}{1024} = 22500\ rpm$$

This compares favorably with encoder specifications where f_{max} is specified from 20 kHz (photo diodes) to 125 kHz (laser based)

solution to replace optical encoders directly without the need to change or upgrade existing application software.

VELOCITY OUTPUT

The analog velocity output VEL is scaled to produce 150 rps/V dc ± 15%. The sense is positive V dc for increasing angular rotation. VEL can drive a maximum load combination of 10 kΩ and 30 pF. The internal velocity scaling is fixed.

POSITION CONTROL

The rotor movement of dc or ac motors used for servo control is monitored at all times. Feedback transducers used for this purpose detect either relative position in the case of an incremental encoder or absolute position and velocity using a resolver. An incremental encoder only measures change in position not actual position.

Closed Loop Control Systems

The primary demand for a change in position must take into account the magnitude of that change and the associated acceleration and velocity characteristics of the servo system. This is necessary to avoid "hunting" due to over- or underdamping of the control employed.

A position loop needs both actual and demand position information. Algorithms consisting of proportional, integral and derivative control (PID) may be implemented to control the velocity profile.

A simplified position loop is shown in Figure 5.

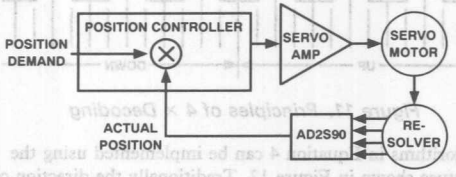

Figure 5. Position Loop

MOTION CONTROL PROCESSES

Advanced VLSI designs mean that silicon system blocks are now available to achieve high performance motion control in servo systems.

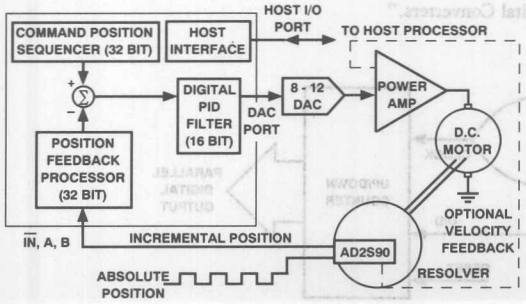

Figure 6. Practical Implementation of the AD2S90

zoidal velocity profile via the I/O port.

As can be seen from Figure 6 encoder position feedback information is used. This is a popular format and one which the AD2S90 emulates thereby facilitating the replacement of encoders with an AD2S90 and a resolver. However, major benefits can be realized by adopting the resolver principle as opposed to the incremental technique.

Incremental feedback based systems normally carry out a periodic check between the position demanded by the controller and the increment position count. This requires software and hardware comparisons and battery backup in the case of power failure. If there is a supply failure and the drive system moves, unless all parts of the system are backed up, a reset to a known datum point needs to take place. This can be extremely hazardous in many applications. The AD2S90 gets round this problem by supplying an absolute position serial data stream upon request, thus removing the need to reset to a known datum.

DSP Interfacing

The AD2S90 serial output is ideally suited for interfacing to DSP configured microprocessors. Figures 7 to 10 illustrate how to configure the AD2S90 for serial interfacing to the DSP. In all cases the AD2S90 is configured for 12-bit operation.

ADSP-2105 Interfacing

Figure 7 shows the AD2S90 interfaced to an ADSP-2105. The on-chip serial port of the ADSP-2105 is used in alternate framing receive mode with internal framing (internally inverted) and internal serial clock generation (externally inverted) options selected. In this mode the ADSP-2105 provides a $\overline{CS}$ and a serial clock to the AD2S90. The serial clock is inverted to prevent timing errors as a result of both the AD2S90 and ADSP-2105 clock data on the negative edge of SCLK. The first data bit is void; 12-bits of significant data then follow on each consecutive negative edge of the clock. Data is clocked from the AD2S90 into the data receive register of the ADSP-2105. This is internally set to 13 bit (12 bits and one "dummy" bit) when 13 bits are received. The serial port automatically generates an internal processor interrupt. This allows the ADSP-2105 to read 12 significant bits at once and continue processing.

The ADSP-2101, ADSP-2102, ADSP-2111 and 21msp50 can all interface to the AD2S90 with similar interface circuitry.

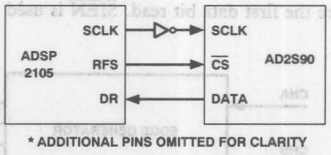

Figure 7. ADSP-2105/AD2S90 Serial Interface

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TMS32020 Interfacing

Figure 8 shows the serial interface between the AD2S90 and the TMS32020. The interface is configured in alternate internal framing, external clock (externally inverted) mode. Sixteen bits of data are clocked from the AD2S90 into the data receive register (DDR) of the TMS32020. The DRR is fixed at 16 bits. To obtain the 12-significant bits, the processor needs to execute three right shifts. (First bit read is void, the last three will be zeros). When 16 bits have been received by the TMS32020, it generates an internal interrupt to read the data from the DRR.

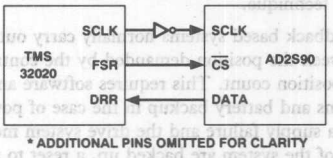

Figure 8. TMS32020/AD2S90 Serial Interface

DSP56000 Interface

Figure 9 shows a serial interface between the AD2S90 and the DSP56000. The DSP in configured for normal mode synchronous operation with gated clock with SCK and SCI as outputs. SCI is applied to $\overline{CS}$.

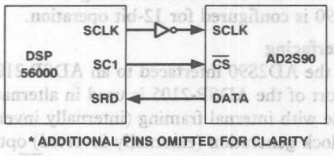

Figure 9. DSP56000/AD2S90 Serial Interface

The DSP56000 assumes valid data on the first falling edge of SCK. SCK is inverted to ensure that the valid data is clocked in after one leading bit. The receive data shift register (SRD) is set for a 13-bit word.

When this register has received 13 bits of data, it generates an internal interrupt on the DSP56000 to read the 12-bits of significant data from the register.

NEC7720 Interface

Figure 10 shows the serial interface between the NEC7720 and the AD2S90. The NEC7720 expects data on the rising edge of its SCK output, and therefore unlike the previous interfaces no inverter is required to clock data into the SI register. There is no need to ignore the first data bit read. $\overline{SIEN}$ is used to Chip Select the AD2S90 and frame the data. The SI register is fixed at 16 bits, therefore, to obtain the 12-significant bits the processor needs to execute four right shifts. Once the NEC7720 has read 16 bits, an internal interrupt is generated to read the internal contents of the SI register.

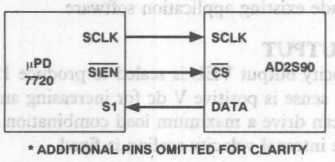

Figure 10. μPD7720/AD2S90 Serial Interface

EDGE TRIGGERED 4 × DECODING LOGIC

In most data acquisition or control systems the A, B incremental outputs must be decoded into absolute information, normally a parallel word, before they can be utilized effectively.

To decode the A, B outputs on the AD2S90 the user must implement a 4 × decoding architecture. The principle states that one A, B cycle represents 4 LSB weighted increments of the converter (see Equation 4).

$$Up = (\uparrow A) \cdot B + (\downarrow A) \cdot B + (\uparrow B) \cdot A + (\downarrow B) \cdot A$$

$$Down = (\uparrow A) \cdot B + (\uparrow A) \cdot B + (\uparrow B) \cdot A + (\downarrow B) \cdot A \quad (4)$$

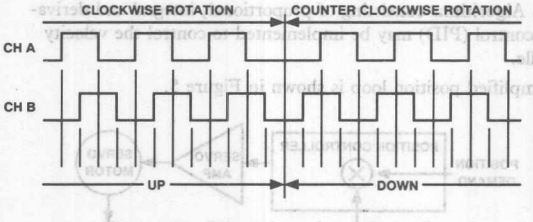

Figure 11. Principles of 4 × Decoding

The algorithms in Equation 4 can be implemented using the architecture shown in Figure 12. Traditionally the direction of the shaft is decoded by determining whether A leads B. The AD2S90 removes the need to derive direction by supplying a direction output state which can be fed straight into the up-down counter.

For further information on this topic please refer to the application note "Circuit Applications of the AD2S90 Resolver-to-Digital Converters."

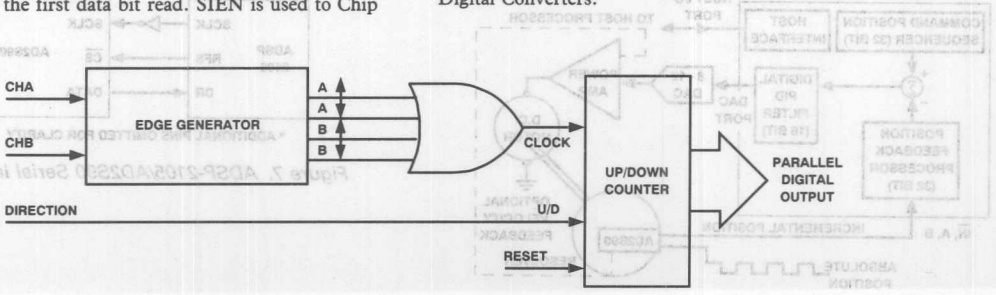

Figure 12. 4 × Decoding Incremental to Parallel Conversion

REMOTE MULTIPLE SENSOR INTERFACING

The DATA output of the AD2S90 is held in a high impedance state until $\overline{CS}$ is taken LO. This allows a user to operate the AD2S90 in an application with more than one converter connected on the same line. Figure 13 shows four resolvers interfaced to four AD2S90s. Excitation for the resolvers is provided locally by an oscillator.

SCLK, DATA and two address lines are fed down low loss cables suitable for communication links. The two address lines are decoded locally into $\overline{CS}$ for the individual converters. Data is received and transmitted using transmitters and receivers.

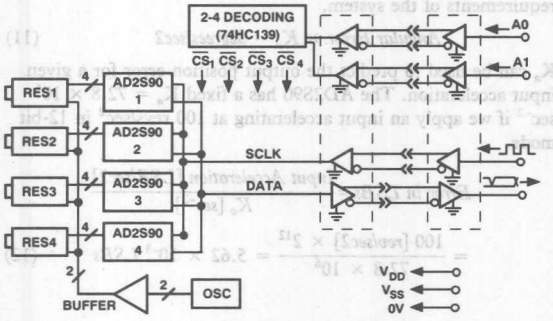

Figure 13. Remote Sensor Interfacing

CIRCUIT DYNAMICS/ERROR SOURCES

Transfer Function

The AD2S90 operates as a Type 2 tracking servo loop. An integrator and VCO/counter perform the two integrations inherent in a Type 2 loop.

The overall system response of the AD2S90 is that of a unity gain second order low-pass filter, with the angle of the resolver as the input and the digital position data as the output. Figure 14 illustrates the AD2S90 system diagram.

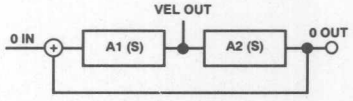

Figure 14. AD2S90 Transfer Function

The open loop transfer function is given by;

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_1 K_2}{s^2} \frac{(1 + st_1)}{1 + st_2} \quad (5)$$

where:

$$A_1(s) = \frac{K_1}{s} \frac{1 + st_1}{1 + st_2} \qquad t_1 = 1.0\ \text{ms} \qquad t_2 = 90\ \mu\text{s} \quad (6)$$

$$A_2(s) = \frac{K_2}{s} \qquad K_1 = 364\text{s}^{-2} \qquad K_2 = 200{,}000\text{s}^{-2} \quad (7)$$

The AD2S90 acceleration constant is given by:

$$K_a = K_1 \cdot K_2 = 72.8 \times 10^6\ \text{sec}^{-2} \quad (8)$$

The AD2S90's design has been optimized with a critically damped response. The closed-loop transfer function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + st_1}{1 + st_1 + \frac{s_2}{K_1 K_2} + \frac{s_3\, t_2}{K_1 K_2}} \quad (9)$$

The normalized gain and phase diagrams are given in Figures 15 and 16.

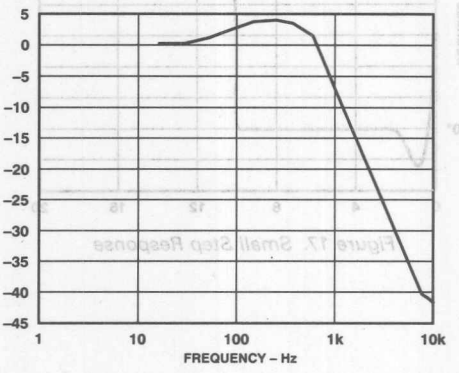

Figure 15. AD2S90 Gain Plot

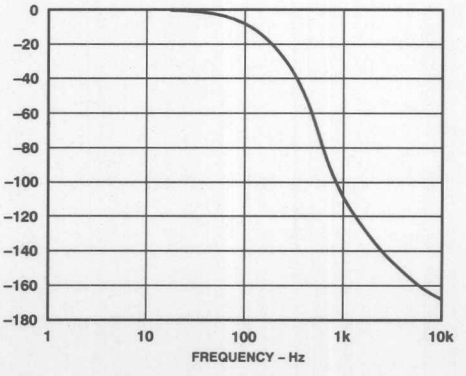

Figure 16. AD2S90 Phase Plot

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The small step response is given in Figure 17, and is the time taken for the converter to settled to within 1 LSB.

ts = 7.00 ms (12-bit resolution)

The large step response (steps>20°) applies when the error voltage will exceed the linear range of the converter. Typically it will take three times longer to reach the first peak for a 179° step.

In response to a velocity step [VELOUT/(dθ/dt)] the velocity output will exhibit the same response characteristics as outlined above.

Figure 17. Small Step Response

SOURCES OF ERROR

Acceleration Error

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{Input\ Acceleration}{Error\ in\ Output\ Angle} \quad (10)$$

The numerator and denominator's units must be consistent. *K_a does not define maximum input acceleration,* only the error due to its acceleration. The maximum acceleration allowable before the converter loses track is dependent on the angular accuracy requirements of the system.

$$Angular\ Error \times K_a = degrees/sec2 \quad (11)$$

K_a can be used to predict the output position error for a given input acceleration. The AD2S90 has a fixed $K_a = 72.8 \times 10^6$ sec^{-2} if we apply an input accelerating at 100 revs/sec^2 in 12-bit mode.

$$Error\ in\ LSBs = \frac{Input\ Acceleration\ [LSB/sec2]}{K_a\ [sec^{-2}]}$$

$$= \frac{100\ [rev/sec2] \times 2^{12}}{72.8 \times 10^6} = 5.62 \times 10^{-3}\ LSBs \quad (12)$$

ANALOG DEVICES

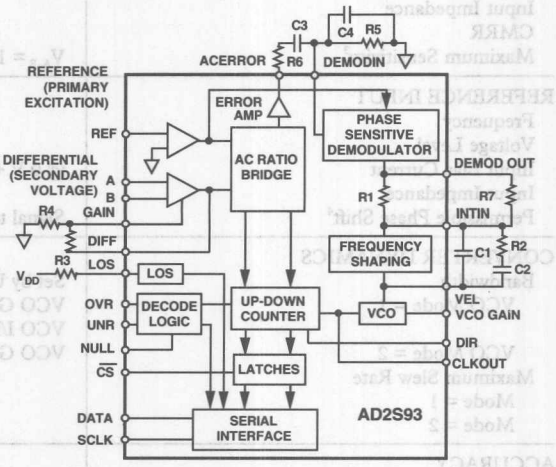
Low Cost LVDT-to-Digital Converter

AD2S93

FEATURES
Full Function Monolithic LVDT-to-Digital Converter
Absolute Serial Data Output
Uncommitted Differential Input
Repeatability
Remote Diagnostics
14-Bit Resolution
Industrial Temperature Range
28-Pin PLCC
Low Power

APPLICATIONS
Industrial Gauging
Industrial Process Control
Linear Positioning Systems
Linear Actuator Control
Automotive Motion Sensing and Control
Torque Sensing Conditioner
AC Strain Gages Conditioning
Avionics

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S93 is a complete 14-bit resolution tracking LVDT-to-digital converter. A Type II tracking loop is employed to track the A–B input and produce a digital output equal to (A–B)/(REF/2), where REF is a fixed amplitude ac reference phase coherent with the A–B input. This allows the measurement of any 2-, 3-, 4- and 5-wire LVDT or linear amplitude modulated input. The operating frequency range is from 360 Hz to 10 kHz with user definable bandwidth set externally within a range of 45 Hz to 1250 Hz.

The AD2S93 has a 16-bit serial output. The MSB (LOS), read first, indicates a loss of the signal A, B, or reference inputs to the converter or transducer. The second and third MSBs are flags indicating whether [–REF/2 (UNR) ≤ A–B ≤ +REF/2 (OVR]) is outside the linear operating range of the converter. The displacement data is presented as 13-bit offset binary giving a ±12-bit operating range. LOS, OVR and UNR are pinned out on the device, in addition a NULL flag is available which is set when (A–B) = 0.

Absolute displacement information is accessed when $\overline{CS}$ is taken LO followed by the application of an external clock (SCLK) with a maximum rate of 2 MHz. Data is read MSB first. When $\overline{CS}$ is high the DATA output is high impedance; this allows daisy chaining of more than one converter onto a common bus.

The A, B differential input allows the user to scale the A, B inputs between 1 and 10. This enables the user to accurately set up the inputs matching the REF input to the DIFF output. The DIFF output is the resultant A–B. The AD2S93 operates using ±5 V ± 5% power supplies and is fabricated on Analog Devices' linear compatible CMOS process (LC^{2}MOS). The (LC^{2}MOS) is a mixed technology process that combines precision bipolar circuits with low power logic.

PRODUCT HIGHLIGHTS

Complete LVDT-to-Digital Interface. The AD2S93 provides the complete solution for digitizing LVDT signals to 14-bit resolution.

Serial 16-Bit Output Data. One 16-bit read from the AD2S93 determines input signal continuity (LOS), over and underrange detection and 13 bits of offset binary displacement information.

High Accuracy Grade in Low Cost Package. 0.05% and 0.1% integral linearity over the full –40°C to +85°C operating temperature range.

Uncommitted Differential Input. Allows configuration of 2-, 3-, 4- and 5-wire LVDTs.

Multiple Converter Interfacing. High impedance data output and a simple three-wire interface reduces cabling and eliminates bus contention.

Low Power. 70 mW power consumption (typ).

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AD2S93 SPECIFICATIONS (V_{DD} = +5 V ± 5%; V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, T_A = –40°C to +85°C

Max Voltage Level[1]		0.8	1.0	1.2	V rms
Nominal Full Scale[2]			1.0		V rms
Input Bias Current	@ +25°C			1.1	µA
Input Impedance			1.0		MΩ
CMRR			57		dB
Maximum Sensitivity[3]	V_{A-B} = 1 V rms, G = 1		342		µV pk/LSB
REFERENCE INPUT					
Frequency		0.36		10	kHz
Voltage Level		1.8	2.0	2.2	V rms
Input Bias Current	@ 0 V +25°C			1	µA
Input Impedance			1.0		MΩ
Permissible Phase Shift[4]	Signal to Reference	–10		+10	Degrees
CONVERTER DYNAMICS					
Bandwidth	Set by User				
VCO Mode = 1	VCO Gain Connected to VCO I/P	500		1250	Hz
VCO Mode = 2	VCO Gain No Connect	45		500	Hz
Maximum Slew Rate					
Mode = 1			2400	3000	LSB/ms
Mode = 2			800	1000	LSB/ms
ACCURACY					
Integral Linearity	AP			0.1	% FSD
	BP			0.05	% FSD
Differential Linearity	AP			<2	LSB
	BP			<1	LSB
Repeatability				±1	LSB
Zero Position Offset	AP @ +25°C	–3		3	LSB
	BP @ +25°C	–1		1	LSB
	AP @ –40°C to +85°C	–4		4	LSB
	BP @ –40°C to +85°C	–2		2	LSB
Gain Error				±0.7	% FS
VELOCITY OUTPUT					
Max Output Voltage	Denotes Max Input Speed			±4.0	V dc
Load Drive Capability				±250	µA
LOGIC INPUTS SCLK, $\overline{CS}$					
Input High Voltage V_{INH}		3.5			V dc
Input Low Voltage V_{INL}				1.5	V dc
Input Current I_{IN}				500	nA
Input Capacitance			10		pF
LOGIC OUTPUTS					
OVR, UNR, NULL, DATA, A, B CLKOUT DIR					
Output High Voltage	@ 1 mA	4.0			V dc
Output Low Voltage	@ 1 mA			1.0	V dc
LOS OUTPUT	Open Drain Output				
	Pull-Up to +V_{DD} via 12 kΩ			400	µA
Drive Capability					
Signal Threshold (A-B)		0.1		0.2	V rms
REF Threshold			0.22		V rms
Timeout Threshold				50	ms

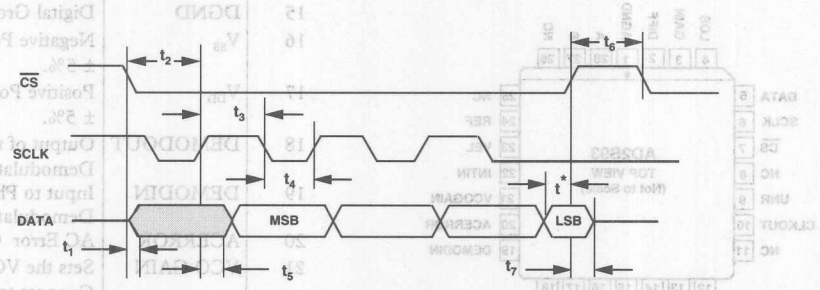
Parameter	Test Conditions	Min	Typ	Max	Units
SERIAL CLOCK (SCLK)					
SCK Input Rate				2	MHz
Maximum Read Rate (16 Bits)	Continuous			9.2	µs
POWER SUPPLY					
I_{DD}		5	7	10	mA
I_{SS}		5	7	10	mA

NOTES
[1]The signal input voltage maximum should always be set at 10% less than the reference input.
[2]Nominal + FS = $V_{A-B} = V_{REF}/2$, FS = $-V_{A-B} = V_{REF}/2$
[3]With G = 10; Sensitivity 34.2 µV pk/LSB
[4]Phase shift cause gain errors. "See Phase Shift and Quadrative Effects."
Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = +5 V ± 5%, AGND = DGND = 0 V, T_A = –40°C to +85°C unless otherwise noted)

Parameter	AD2S93	Units	Test Conditions
t_1[1]	150	ns max	$\overline{CS}$ to DATA Enable
t_2	600	ns min	$\overline{CS}$ to 1st SCLK Positive Edge
t_3	250	ns min	SCLK High Pulse
t_4	250	ns min	SCLK Low Pulse
t_5	100	ns max	SCLK Positive Edge to DATA Valid
t_6	600	ns min	$\overline{CS}$ High Pulse Width
t_7	150	ns max	$\overline{CS}$ High to DATA High Z (Bus Relinquish)

NOTE
[1]SCLK can only be applied after t_2 has elapsed.



t* = THE MINIMUM ACCESS TIME: USER DEPENDENT
TOTAL MAX READ TIME = $t_2 + 16.(t_3 + t_4) + t_7$
TOTAL MAX READ TIME = 600 +16 (250 + 250) + 150 ns
TOTAL MAX READ TIME = 600 + 8000 + 150 ns
TOTAL MAX READ TIME = 8.750 µs (SINGLE READ ONLY)

Timing Diagram

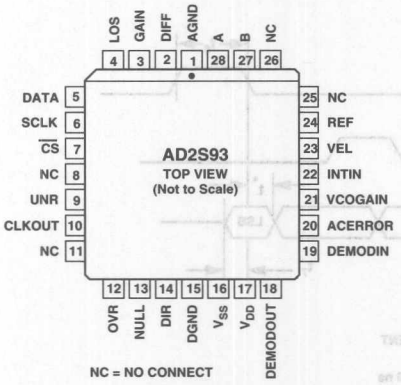
RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage (V_{DD}–V_{SS}) ..... ±5 V dc ± 5%
Analog Input Voltage (A, B) ..... 1 V rms ± 10%
Analog Reference Input (REF) ..... 2 V rms ± 10%
Signal and Reference Harmonic Distortion ..... <10%
Operating Temperature Range
Industrial (AP, BP) ..... –40°C to +85°C

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND ..... –0.3 V dc to + 7.0 V dc
V_{SS} to AGND ..... +0.3 V dc to – 7.0 V dc
AGND to DGND ..... –0.3 V dc to V_{DD} + 0.3 V dc
Analog Inputs to AGND REF .... V_{SS} – 0.3 V to V_{DD} + 0.3 V
A, B ..... V_{SS} – 0.3 V to V_{DD} + 0.3 V
Analog Output to AGND VEL ..... V_{SS} to V_{DD}
Digital Inputs to DGND
$\overline{CS}$, SCLK ..... –0.3 V to V_{DD} + 0.3 V
Digital Outputs to DGND
NULL, DIR, CLKOUT, DATA .... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A, B) ..... –40°C to +85°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Power Dissipation to +75°C ..... +100 mW
Derates above +75°C by ..... 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



ORDERING GUIDE

Model	Temperature Range	Linearity	Package Option*
AD2S93AP	–40°C to +85°C	0.1%	P-28A
AD2S93BP	–40°C to +85°C	0.05%	P-28A

*For outline information see Package Information section.

PIN DESIGNATIONS

Pin No.	Mnemonic	Description
1	AGND	Analog Ground.
2	DIFF	Output of Signal Input Preamplifier.
3	GAIN	Connect GAIN Pin to DIFF for nominal × 1. Gains greater than 1 can be resistively scaled. Do not leave unconnected.
4	LOS	Denotes A or B lines loss of connection and/or loss of reference to transducer or converter.
5	DATA	16-bit serial data output 13 bits of absolute position information plus overrange and underrange plus LOS.
6	SCLK	Serial Clock. Maximum rate = 2 MHz.
7	$\overline{CS}$	Chip Select. Loads serial interface with current positional information and enable output.
9, 12	UNR, OVR	Two pins that denote whether the input signals are underrange or overrange.
10	CLKOUT	Updates every LSB.
13	NULL	Denotes Null Position.
14	DIR	Indicates direction. DIR is HI for positive displacement and LO for negative displacement.
15	DGND	Digital Ground.
16	V_{SS}	Negative Power Supply –5.0 V dc ± 5%.
17	V_{DD}	Positive Power Supply +5.0 V dc ± 5%.
18	DEMODOUT	Output of the Phase Sensitive Demodulator.
19	DEMODIN	Input to Phase Sensitive Demodulator.
20	ACERROR	AC Error Output.
21	VCO GAIN	Sets the VCO gain internally. Connect to VEL for 2400 LSB/s. Disconnect for 800 LSB/s.
22	INTIN	Determines system dynamics connect C and RC (serial) parallel combination across INTIN and VEL to determine loop dynamics.
23	VEL	Analog Velocity Output.
24	REF	Single ended input for fixed amplitude reference.
27, 28	B, A	Uncommitted differential inputs for the A, B signal inputs.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD2S93 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

GLOSSARY OF TERMS

INTEGRAL LINEARITY

Integral linearity deviation as a percent of full scale. A 0.1% deviation is equivalent to 8-LSB change on the output.

Gain

The converter gain is the maximum variation in the ratio of A–B/REF/2 to the maximum digital input.

Output Offset

The output offset is the digital output code when the analog input signal A–B = 0.

Overrange (OVR)

OVR goes high when A–B is in phase with REF and larger than REF/2.

Underrange (UNR)

UNR goes high when A–B is out of phase with REF and larger than REF/2.

PRINCIPLE OF OPERATION

The AD2S93 is based on a Type 2 tracking closed-loop principle. The output tracks the position of the LVDT without the need for external convert and wait states. As the transducer moves through a position equivalent to the least significant bit weighting, the output is updated by one LSB. On the AD2S93, CLKOUT updates corresponding to one LSB increment. Figure 1 illustrates the principle of operation.

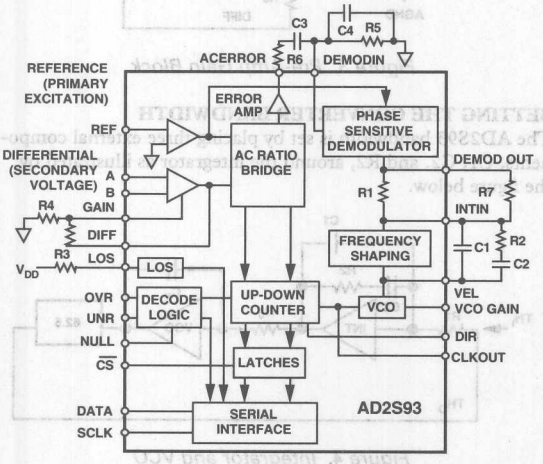


Figure 1. Functional Block Diagram

Because the conversion depends on the ratio of the input signals (ratiometric ac bridge), the AD2S93 is remarkably tolerant of input amplitude and frequency. This, combined with the definable Type 2 tracking closed-loop guarantees the AD2S93's repeatability for a given input. A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null the output of the ACERROR. When this is accomplished the word state of the up/down counter equals within the rated accuracy of the converter, the LVDT position output.

For more information on the operation of the converter, see "Circuit Dynamics" section.

DATA FORMAT

OPERATING RANGE

The AD2S93 operating range is defined in Figure 2. The linearity and specified operating range of the converter is the central two 12-bit quadrants through zero. The corresponding input relationship is $-REF/2 \le A-B \le +REF/2$, ($\pm$ is used to denote phase coherency). The sign bit is low for inputs with A–B in phase with REF. The two remaining 12-bit quadrants are used to denote over (OVR) and underrange (UNR). OVR goes high when A–B is in phase with REF and larger than REF/2. UNR goes high when A–B is out of phase with REF and larger than REF/2. LOS is an open drain output which pulls high when A and/or B are removed or REF is removed (see "Inbuilt Diagnostics"), or A + B is less than 100 mV.

SCALING THE INPUTS

In order to match the LVDT output to the AD2S93 output, the inputs to the AD2S93 need to be scaled. The operating range is illustrated in Figure 2. The AD2S93 operates across ±12-bit range where the remaining 12-bit quadrants are used to denote overrange and underrange. The output position word is a function of the ratio between A–B and V_{REF} (see Figure 2) where:

$$\pm FSR = \frac{(A-B)}{V_{REF}/2}$$

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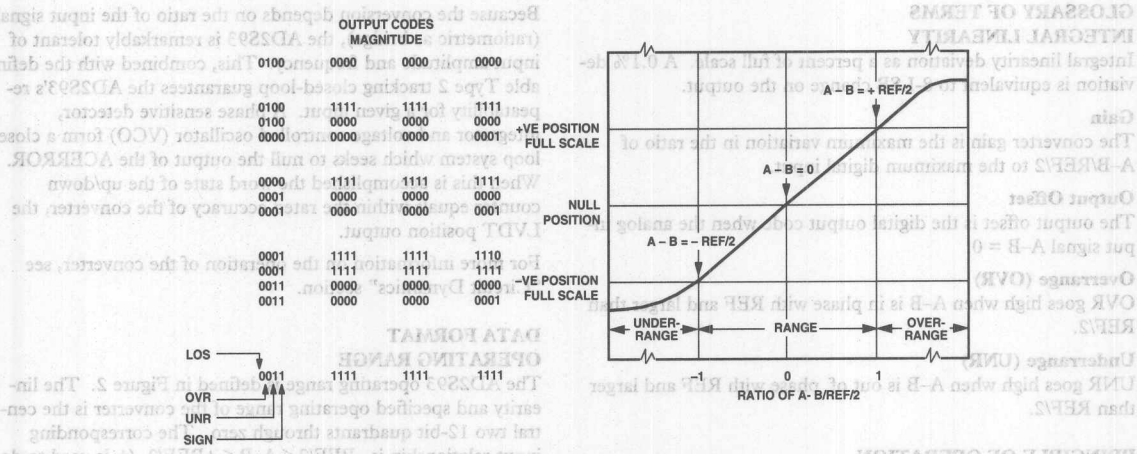

Figure 2. Output Code Format

If the maximum operating stroke of an LVDT yielded a 1 V rms A–B output, the weighting of the LVDT to AD2S93 digital output would be:

$$\frac{\textit{Input Signal Full Scale}}{\textit{Full-Scale Operating Range}\ (\pm 2^{12})}$$

$$\frac{1 \times 2\sqrt{2}}{2^{13}}$$

$$\textit{Input Scaling} = 345\ \mu V/LSB$$

This can be equated directly to the LVDT sensitivity specification in mm/v/v.

Note: The overrange and underrange quadrants can be utilized by decoding the overrange and underrange MSBs and decoding the 12 magnitude bits. This will increase the operating range of the AD2S93 accordingly. However, if the input A–B > V_{REF} then the converter will lose track of the input and will only regain track when the input signal returns to within the operating range of the converter.

INPUT GAIN

Since the transformation ratio of an LVDT or RVDT from excitation voltage to signal voltage can be 1:0.15, provision for gain scaling has been provided. The gain can, therefore, be selected to ensure that the full-scale output of converter represents the maximum stroke position of the transducer.

The gain setting is accomplished by connecting Pin 2, (DIFF) and Pin 3 (GAIN) together (unity gain) or connecting two resistors as shown in Figure 3.

The gain of the input stage is calculated using the following equation:

$$\frac{DIFF(A-B)}{(A-B)\ IN} = 1 + \frac{R_3}{R_4}$$

e.g., For a gain of 5, R3 = 12 kΩ, R4 = 3 kΩ
For a gain of 10, R3 = 18 kΩ, R4 = 2 kΩ

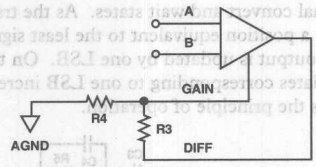

Figure 3. Pre-Amp Gain Block

SETTING THE CONVERTER BANDWIDTH

The AD2S93 bandwidth is set by placing three external components, C1, C2, and R2, around the integrator as illustrated by the figure below.

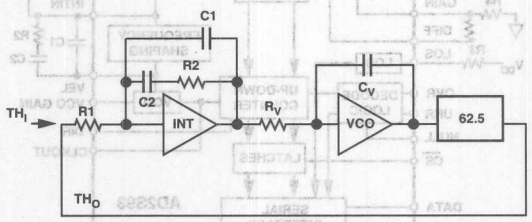

Figure 4. Integrator and VCO

Before the bandwidth can be set, the corresponding VCO gain setting must be determined. The VCO gain is directly related to the slew rate of the converter. This is set internally to two different rates defined internally by R_V.

Typical converter slew rates are defined below,

$G\ (1) = 2400\ LSB/ms–Mode\ 1$
$G\ (2) = 800\ LSB/ms–Mode\ 2$

Calculation of the component values for the bandwidth is detailed below. For more detailed information on component value selection for the AD2S93, please consult the "Passive Component Selection and Dynamic Modeling Software for the AD2S93 LVDT-to-Digital Converter."

VCO Gain G (1) Mode 1

The available bandwidth with this option is from 0.5 kHz to 1.25 kHz.

$$F_{REF} > 8 \times Fo$$
$$C1 = 1/(800 \times Fo^2)$$
$$C2 = 8 \times C1$$
$$R2 = 45 \times Fo$$

Where F_{REF} is the reference frequency, Fo is the closed-loop 3 dB point.

VCO Gain G (2) Mode 2

The available bandwidth with this option is from 45 Hz to 500 Hz.

$$F_{REF} > 8 \times Fo$$
$$C1 = 1/(2400 \times Fo^2)$$
$$C2 = 8\ C1$$
$$R2 = 45 \times Fo$$

Where F_{REF} is the reference frequency, Fo is the closed-loop 3 dB point.

INTERFACING TO THE AD2S93 (SEE "TIMING CHARACTERISTICS")

The absolute position information is extracted via a three-wire interface, DATA, CS and SCLK. The DATA output is held in a high impedance state when CS is high.

Upon the application of logic low to the CS pin, the DATA is enabled and the current position information is transferred from the counters to the serial interface. Data is retrieved by applying an external clock to the SCLK pin. The maximum data rate of the SCLK is 2 MHz. To ensure secure data retrieval, it is important to note that SCLK should not be applied until a minimum period of 600 ns after the application of logic low to CS. Data is then clocked out on successive positive edges of SCLK: 16 clock edges are required to extract the entire data word. Subsequent positive edges greater than the defined resolution of the converter will clock zeros from the data output if CS remains in a low state. The format of the data read is shown in Table I.

Table I.

	DB0	DB1	DB2	DB3	DATA DB4–D15 MSB LSB
Function	LOS	OVR	UNR	SIGN	MAGNITUDE

If less than the full 16-bit word is required, then the data read can be terminated by releasing CS after the required number of bits have been read.

CS can be released a minimum of 100 ns after the last positive edge. If the user is reading data continuously, CS can be reapplied after a minimum of 600 ns after it is released. The minimum repetitive read time of the same converter is given by (16 bits read @ 2 MHz). Min RD Time = [600 + (16 × 500) + 600] = 9.2 µs.

IN-BUILT DIAGNOSTICS

The first three bits read from the serial interface preceding the sign and magnitude data can be used to determine whether the data is valid or not. Over and underrange (OVR, UNR) denote the two extremes of the LVDT stroke where linearity of the LVDT may degrade. Loss of signal LOS is an open drain output which pulls high (12 kΩ pull up) when one of the following conditions is satisfied:

1. A and/or B is disconnected.
2. REF is disconnected.

Note: LOS has a response time of 50 ms max to the conditions stated above, see "Specifications."

CONNECTING THE CONVERTER

Positive power supply V_{DD} = +5 V dc ± 5% should be connected to Pin 17 and negative power supply V_{SS} = –5 V dc ± 5% to Pin 16. *Reversal of these power supplies will destroy this device.* For LVDT connections to the converter please refer to Figures 5 through 7. On all connections, the maximum input reference signal V_{REF} = 2.0 V rms ± 10%. To operate within the standard operating range, A–B should not exceed 1.0 V rms ± 10%. The AD2S93 AGND point is the point at which all analog signal grounds should be connected. Ground returns from the LVDT should be connected to AGND. The AD2S93 DGND pin should be connected to the AD2S93 AGND pin. Ancillary Digital circuitry must be connected to the Star Point and not to the AD2S93 AGND pin.

In all cases, the AD2S93 has been configured with the following dynamics.

Reference Frequency	*5 kHz*
3 dB Bandwidth	*625 Hz*

Vco Gain is set in MODE 1 where VCO GAIN is connected to VEL.

Using the procedure described in "setting the converter bandwidth" the following preferred values (E12 series) were calculated:

$$C1 = 3.3\ nF$$
$$C2 = 27\ nF$$
$$R2 = 27\ k\Omega$$

CALCULATING HF FILTER (C3, C4, R5, R6)

$$15\ k\Omega \le R5 = R6 \le 56\ k\Omega$$

$$C3 = C4 = \frac{1}{2\pi\ R5\ F_{REF}}$$

So, C3 = 1 nF, R5 = R6 = 33 kΩ, C4 = 1 nF and in all cases R7 = 15 kΩ.

Half-Bridge Type LVDT Connection

In this method of connection, it is necessary to add two additional bridge completion resistors R_C and R_C, in order to derive a reference for the AD2S93. In selecting the bridge completion resistor, it is important to remember that mismatch between R_{C1} and R_{C2} will cause nonzero errors at null. If two LVDTs are being used for differential measurements, the resistors can be replaced by the second LVDT.

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Three- or Four-Wire LVDT Connection

In this method of connection, shown in Figure 6, the converters digital output is proportional to the ratio:

$$\frac{(A-B)}{(A+B)/2}$$

where A and B are the individual LVDT secondary output voltages. Inspection of Figure 6 should demonstrate why this relationship is true. (A–B) is simply the voltage across the series connected secondaries of the LVDT and is applied to the A, B input to the converter. (A + B)/2 is effectively the average of the two secondary voltages as computed by the balanced bridge completion resistors and the grounding of the secondary center-tap.

Note: This method of connection is appropriate only for where (A + B) is a constant, independent of LVDT position. Any lack of constancy in (A + B) will be reflected as an additional non-linearity in the output. It is up to the user to determine if (A + B) is sufficiently constant over the particular stroke length employed.

This method will usually restrict the usable LVDT range to half of its full range. The restriction can be eliminated, however, by attenuating DIFF by a factor of 2 or increasing V_{REF} by a factor of 2. This connection method has the tremendous advantage of being insensitive to temperature related phase shifts and excitation oscillator instability effects usually associated with more conventional LVDT conversion systems.

As in the case of the half-bridge type LVDT connection, R_{C1} and R_{C2} are the bridge completion resistors and are matched to a degree sufficient to ensure that the digital output representing the null position does not vary from the LVDT's natural null position. If null adjustment is required, a potentiometer can be used in place of the common connection between the two resistors.

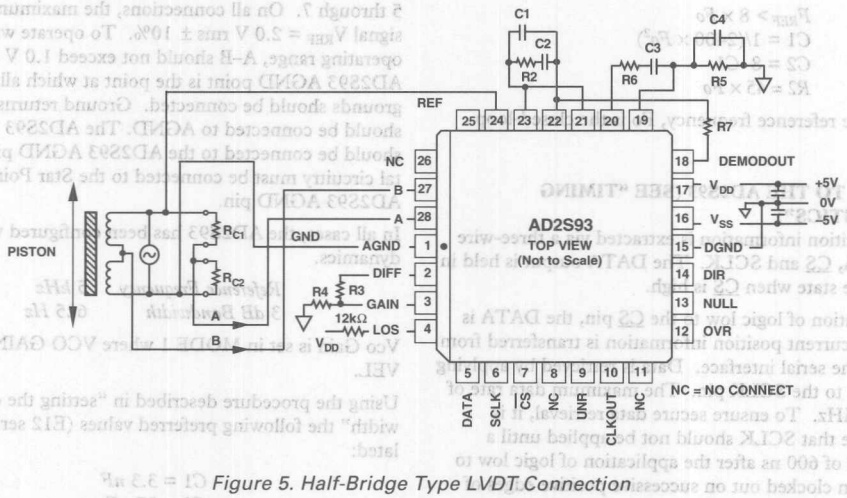

Figure 5. Half-Bridge Type LVDT Connection

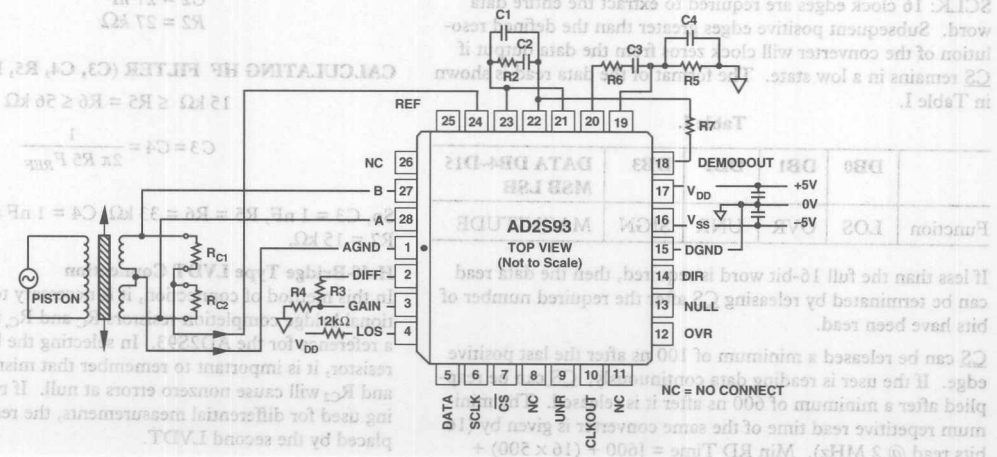

Figure 6. Three- or Four-Wire LVDT Connection

Two-Wire LVDT Connection

This method should be used in cases where the sum of the LVDT secondary output voltages (A + B) is not constant with LVDT displacement over the desired stroke length. This method of connection, shown in Figure 7, still maintains the ratiometric operation and the insensitivity to variations in reference amplitude and frequency. However, the phase shift between V_{REF} and V1 should be minimized to maintain accuracy (see Section "PHASE SHIFT AND QUADRATURE EFFECTS"). Suggested phase compensation circuits are shown in Figure 7.

PHASE SHIFT AND QUADRATURE EFFECTS

Reference to signal phase shift can be high in LVDTs, sometimes in the order of 70 degrees. If the converter is connected as in Figures 5 and 6, any effects due to this phase shift are minimized. This connection method, therefore, provides outstanding benefits.

The additional gain error caused by reference to signal phase shifts is given by:

$$(1 - \cos\theta) \times 100\% \text{ of FSR}$$

where

θ = *phase shift between* V_{REF} *and DIFF.*

When the phase shift between V_{REF} and V1 is zero, additional quadrature on the signal will have no effect on the converter. This is another benefit of the conversion method. For example, when a REF lags (A–B) by approximately 10°, the gain error is approximately 1%. When (A–B) lags REF by approximately 10°, the gain error is approximately 2%.

REMOTE MULTIPLE SENSOR INTERFACING

The DATA output of the AD2S93 is held in a high impedance state until $\overline{CS}$ is taken LO. This allows a user to operate the AD2S93 in an application with more than one converter connected on the same line. Figure 8 shows four LVDTs interfaced to four AD2S93s. Excitation for the LVDT is provided locally by an oscillator.

SCLK, DATA and two address lines are fed down low loss cables suitable for communication links. The two address lines are decoded locally into $\overline{CS}$ for the individual converters. Data is received and transmitted using transmitters and receivers.

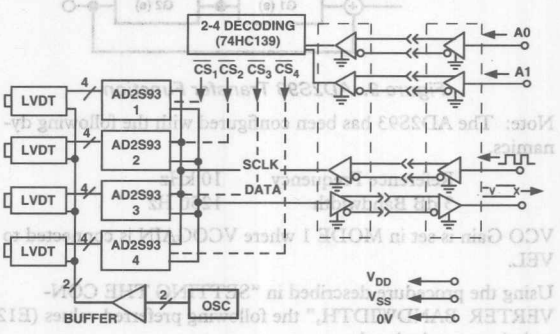

Figure 8. Remote Sensor Interface

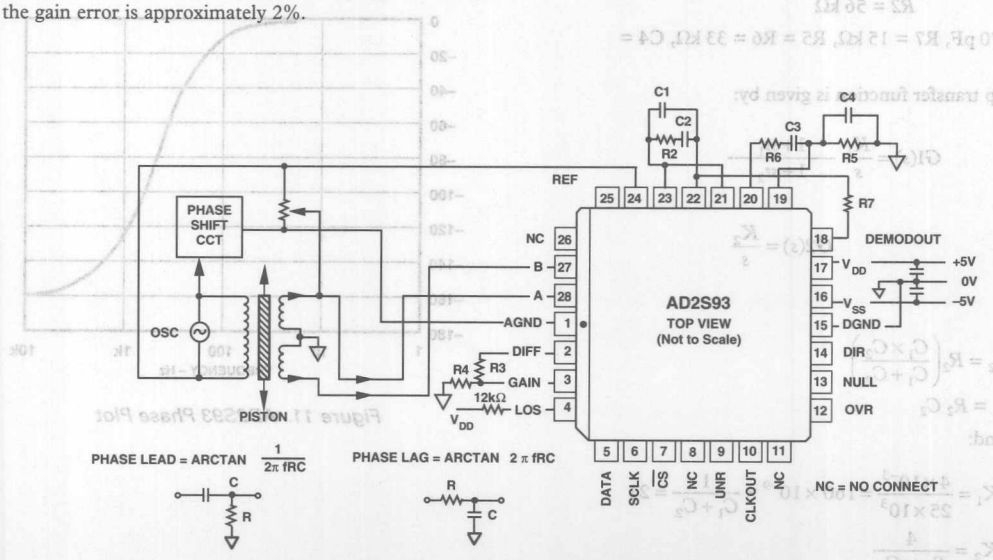

Figure 7. Two-Wire LVDT Connection

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grator and VCO/counter perform the two integrations inherent in a Type 2 loop.

The overall system response of the AD2S93 is that of a unity gain second order low-pass filter, with the position of the LVDT as the input and the digital position data as the output. Figure 9 illustrates the AD2S93 system diagram.

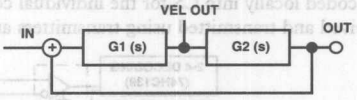

Figure 9. AD2S93 Transfer Function

Note: The AD2S93 has been configured with the following dynamics.

Reference Frequency	10 kHz
3 dB Bandwidth	1250 Hz

VCO Gain is set in MODE 1 where VCOGAIN is connected to VEL.

Using the procedure described in "SETTING THE CONVERTER BANDWIDTH," the following preferred values (E12 series) were calculated:

$C1 = 820$ pF
$C2 = 6.8$ nF
$R2 = 56$ kΩ

C3 = C4 = 470 pF, R7 = 15 kΩ, R5 = R6 = 33 kΩ, C4 = 470 pF

The open-loop transfer function is given by:

$$G1(s) = \frac{K_1}{s}\,\frac{1+st_1}{1+st_2}$$

$$G2(s) = \frac{K_2}{s}$$

where:

$$t_2 = R_2\left(\frac{C_1 \times C_2}{C_1 + C_2}\right)$$

$t_1 = R_2\,C_2$

and:

$$K_1 = \frac{4\times10^{-3}}{25\times10^{3}} = 160\times10^{-9} \times \frac{1}{C_1+C_2} = 21$$

$$K_2 = \frac{4}{R_V \times C_V}$$

Note A_2 has two values depending on which mode is being used

$K_{2\ (MODE1)} = 640 \times 10^3$
$K_{2\ (MODE2)} = 160 \times 10^3$

The AD2S93 acceleration constant is given by:

$$K_a = K_1 \times K_2$$

Therefore in the example given,

$$K_a = K_1 \times K_2 = 21 \times 640 \times 10^3 = 13.44 \times 10^6\ s^{-2}$$

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{\dfrac{1+st_1}{1+st_1+\dfrac{s_2}{K_1K_2}+\dfrac{s_3t_2}{K_1K_2}}}{\dfrac{\theta_{OUT}}{\theta_{IN}} = \dfrac{K_1K_2}{s^2}\,\dfrac{(1+st_1)}{1+st_2}}$$

The normalized gain and phase diagrams are given in Figures 10 and 11 with a bandwidth of 1.25 kHz.

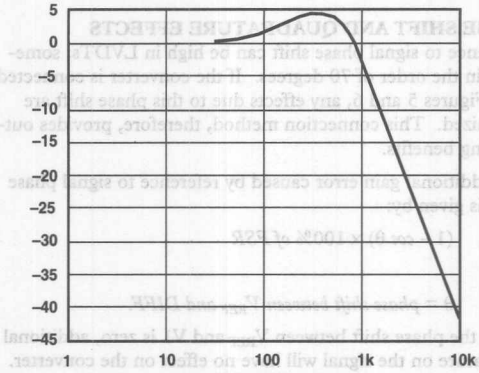

Figure 10. AD2S93 Gain Plot

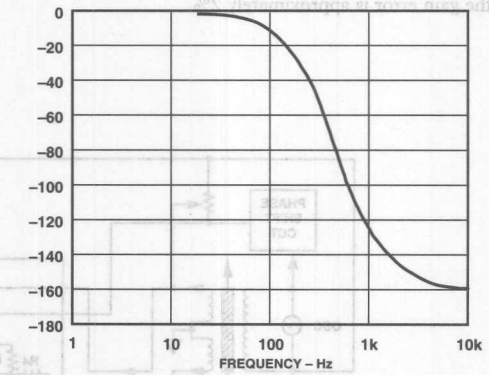

Figure 11. AD2S93 Phase Plot

The small step response is given in Figure 12, and is the time taken for the converter to settled to within 1 LSB.

$$ts = 7\ ms\ (14\text{-}bit\ resolution)$$

The large step response (steps >5% of FSR) applies when the error voltage will exceed the linear range of the converter. Typically it will take three times longer to reach the first peak FSR.

In response to a velocity step [VELOUT/(dθ/dt)] the velocity output will exhibit the same response characteristics as outlined above.

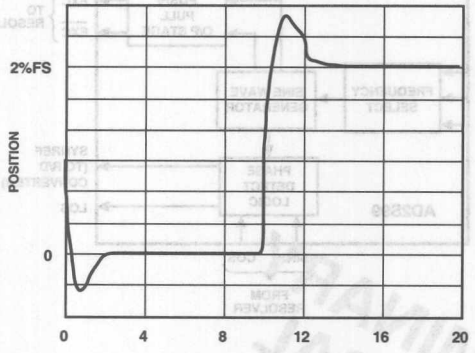

Figure 12. Small Step Response

SOURCES OF ERROR

ACCELERATION ERROR

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{input\ acceleration}{position}$$

The numerator and denominator's units must be consistent. *K_a does not define maximum input acceleration,* only the error due to its acceleration. The maximum acceleration allowable before the converter loses track is dependent on the positional accuracy requirement of the system.

$$Position\ Error \times K_a = LSB/sec^2$$

K_a can be used to predict the output position error for a given input acceleration. The AD2S93 in the example has a $K_a = 13.44 \times 10^6\ sec^{-2}$ if we apply an input accelerating at $100 \times 2^{14}\ LSB/sec^2$.

$$Error\ in\ LSBs = \frac{input\ acceleration\left[LSB/sec^2\right]}{K_a\left[sec^{-2}\right]}$$

$$= \frac{100 \times 2^{14}}{13.44 \times 10^6} = 0.12\ LSBs$$

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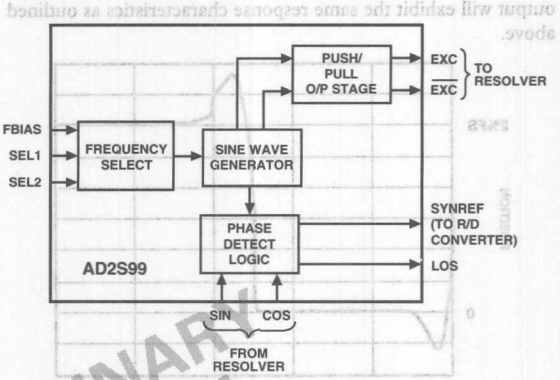
Programmable Oscillator

AD2S99

FEATURES
Programmable Sinusoidal Oscillator
Synthesized Synchronous Reference Output
Programmable Output Frequency Range: 2 kHz – 20 kHz
Wide Power Supply Range
"Loss-of-Signal" Indicator
20-Pin PLCC Package
Low Cost

APPLICATIONS
Primary Excitation of:
Resolvers
Synchros
LVDTs
RVDTs
Pressure Transducers
Load Cells
Inductosyns
AC Bridges

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD2S99 is a programmable sinusoidal oscillator available in a 20-pin PLCC package, with an operating temperature range of –40°C to +85°C.

The AD2S99 provides a sine wave excitation output for resolvers and a wide variety of ac transducers. The AD2S99 also provides a synthesized reference output signal which is phase locked to the Sin and Cos inputs of the AD2S99. These inputs are provided by the secondary windings of a resolver. The synthesized reference eliminates the need for preset phase shift circuits and allows synchronous demodulation schemes such as type II tracking converters to be implemented without additional calibration of the total system.

By providing a Synchronous Reference output, the AD2S99 eliminates the temperature dependent phase shifts found with inductive transducers, and their resultant errors.

The AD2S99 requires only one external resistor for operation. The AD2S99 is manufactured on a LC^2MOS process that combines high density, low power CMOS logic with bipolar linear circuitry.

PRODUCT HIGHLIGHTS

Dynamic Phase Compensation

The AD2S99 dynamically compensates for any phase variation in the transducer by phase locking the outputs of the transducer to the synthesized reference output of the AD2S99.

Programmable Frequency

The oscillator frequency is easily programmed to 2 kHz, 5 kHz, 10 kHz or 20 kHz by using the frequency select pins.

Loss of Signal Pin

The "LOS" output indicates a signal failure if both the sensor outputs feeding back to the AD2S99 are lost.

Wide Power Supply Range

The AD2S99 operates over the ±5 V to ±15 V power supply range.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SPECIFICATIONS (V_S = ±4.75 V to ±15.75 V @ –40°C to +85°C unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
FREQUENCY OUTPUT RANGE					SEL1 SEL2
2 kHz		2000		Hz	V_{SS} V_{SS}
5 kHz		5000		Hz	V_{SS} GND
10 kHz		10000		Hz	GND V_{SS}
20 kHz		20000		Hz	GND GND
ACCURACY					
Frequency			±10	%	AP Grade @ +25°C
			±20	%	AP Grade –40°C to +85°C
			±5	%	BP Grade @ +25°C
			±10	%	BP Grade –40°C to +85°C
Amplitude		±3	±10	%	AP Grade @ +25°C
			±20	%	AP Grade –40°C to +85°C
		±3	±5	%	BP Grade @ +25°C
			±10	%	BP Grade –40°C to +85°C
Power Supply Rejection Ratio		0.002		V p-p/V	Output Variation as Function of Change in Power Supply Voltage
EXCITATION OUTPUT					Square Wave
EXC, $\overline{EXC}$		2		V rms	R_{LOAD} = 145 Ω to GND
SYNREF		±3		V rms	C_{LOAD} = 1000 pF
OUTPUT DRIVE CAPABILITY					
EXC, $\overline{EXC}$					
Current Drive			±8	mA p-p	V_{SS} = –5 V, V_{DD} = +5 V
			±20	mA p-p	V_{SS} = –15 V, V_{DD} = +15 V
Capacitive Drive			1000	pF	
PHASE LOCK RANGE					
SIN Input to REF Output	–45		+45	Degrees	
Additional Phase Delay					
AP Grade			±10	Degrees	
BP Grade			±5	Degrees	
LOS Detector Threshold	0.5		0.7	V rms	
TOTAL HARMONIC DISTORTION					
EXC, $\overline{EXC}$					
AP Grade			–25	dB	@ 2 kHz
BP Grade			–30	dB	R_{LOAD} = 145 Ω to GND
					C_{LOAD} = 1000 pF
FREQUENCY SELECT INPUTS					
SEL1, SEL2[1]	V_{SS}		AGND	V dc	
LOS OUTPUT					
Output Low Voltage			0.4	V dc	I_{OL} = 400 µA
Output High Voltage	V_{DD} – 0.4			V dc	50 kΩ Pull Up to V_{DD} (Open Drain Output)
POWER SUPPLIES					
Supply Currents	+4.75		+15.75	V dc	V_{DD} = +15.75 V, V_{SS} = –15.75 V
	–4.75		–15.75	V dc	V_{DD} = +4.75 V, V_{SS} = –4.75 V
TEMPERATURE RANGE					
	–40		+85	°C	Operating
	–65		+150	°C	Storage

NOTES
[1]Frequency select pins SEL1 and SEL2 must be connected to appropriate voltage levels before power is applied.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage (V_{DD} to V_{SS}) . . . . . ±4.75 V to ±15.75 V
Analog Input Voltage (SIN and COS) . . . . . 2 V rms ±10%
Frequency Select (SEL1 and SEL2) . . . . . V_{SS} to AGND
Operating Temperature Range . . . . . –40°C to +85°C

ABSOLUTE MAXIMUM RATINGS*

V_{DD} . . . . . +16.5 V
V_{SS} . . . . . –16.5 V
Operating Temperature . . . . . –40°C to +85°C
Storage Temperature . . . . . –65°C to +150°C
Analog Input Voltages (SIN and COS) . . . . . V_{SS} – 0.3 V
. . . . . to V_{DD} + 0.3 V
Frequency Select (SEL1, SEL2) . . . . . V_{SS} – 0.4 V
. . . . . to AGND + 0.4 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD2S99?P	–40°C to +85°C	P-20A

*For outline information see Package Information section.

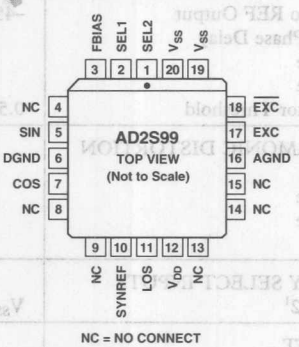
PIN DESIGNATIONS

Pin No.	Mnemonic	Description
1	SEL2	Frequency Select 2
2	SEL1	Frequency Select 1
3	FBIAS	External Freq. Adjust Pin
5	SIN	Resolver Output SIN
6*	DGND	Digital Ground
7	COS	Resolver Output COS
10	SYNREF	Synthesized Reference Output
11	LOS	Indicates When Both the SIN and COS Are Below the Threshold.
12	V_{DD}	Positive Power Supply
16*	AGND	Analog Ground
17	EXC	Resolver Reference (Plus)
18	$\overline{EXC}$	Resolver Reference (Minus)
19*	V_{SS}	Negative Power Supply
20*	V_{SS}	Negative Power Supply

*Note: Pins 6 and 16 must be connected together and Pins 19 and 20 must be connected together.

PRELIMINARY TECHNICAL DATA

PIN CONFIGURATION



NC = NO CONNECT

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD2S99 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

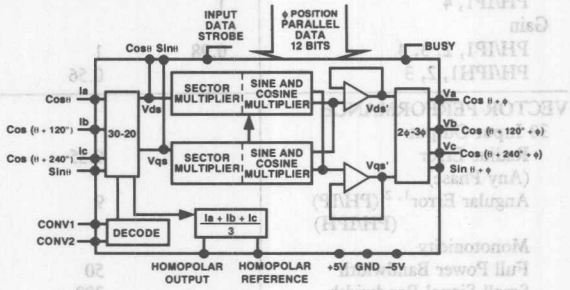
FEATURES

Complete Vector Coordinate Transformation on Silicon
Mixed Signal Data Acquisition
Three-Phase 120° and Orthogonal 90° Signal Transformation
Three-Phase Balance Diagnostic—Homopolar Output

APPLICATIONS

AC Induction and DC Permanent Magnet Motor Control
HVAC, Pump, Fan Control
Material Handling
Robotics
Spindle Drives
Gyroscopes
Dryers
Washing Machines
Electric Cars
Actuators
Three-Phase Power Measurement
Digital-to-Resolver & Synchro Conversion

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S100 performs the vector rotation of three phase 120 degree or two-phase 90 degree sine and cosine signals by transferring these inputs into a new reference frame which is controlled by the digital input angle ϕ. Two transforms are included in the AD2S100. The first is the Clarke transform which computes the sine and cosine orthogonal components of a three phase input. These signals represent real and imaginary components which then form the input to the Park transform. The Park transform relates the angle of the input signals to a reference frame controlled by the digital input port. The digital input is a 12-bit parallel binary representation.

If the input current signals are represented by Vds and Vqs, respectively, where Vds and Vqs are the real and imaginary components, then the transformation can be described as follows:

$$Vds' = Vds\ Cos\phi - Vqs\ Sin\phi$$
$$Vqs' = Vds\ Sin\phi + Vqs\ Cos\phi$$

Where Vds' and Vqs' are the output of the Park transform and $Sin\phi$, and $Cos\phi$ are the values internally derived by the AD2S100 from the binary digital data.

The input section of the device can be configured to accept either three-phase inputs, two-phase inputs of a three-phase system, or two 90 degree input signals. The homopolar output detects the imbalance of a three-phase input only. Under normal conditions, this output will be zero.

The digital input section will accept a resolution of up to 12 bits (AD2S100). An input data strobe signal is required to synchronize the position data and load this information into the device counters. A busy output is provided to identify the conversion status of the AD2S100. The busy period represents the conversion time of the vector rotation.

Two analog output formats are available. A two-phase rotated output facilitates multiple rotation blocks. Three phase format signals are available for use with a PWM inverter.

PRODUCT HIGHLIGHTS

Hardware Peripheral for Standard Microcontrollers and DSP Systems
The AD2S100 removes the time consuming cartesian transformations from digital processors and benchmarks a speed improvement of 30:1 on standard 20 MHz processors. AD2S100 transformation time = 2 μs (typ).

Field Orientated Control of AC and DC Brushless Motors
The AD2S100 accommodates all the necessary functions to provide a hardware solution for ac vector control of induction motors and dc brushless motors.

Three-Phase Imbalance Detection
The AD2S100 can be used to sense overcurrent situations or imbalances in a three-phase system via the homopolar output.

Resolver to Digital Converter Interface
The AD2S100 provides general purpose interface for position sensors used in the application of dc brushless and ac induction motor control.

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AD2S100—SPECIFICATIONS (V_{DD} = +5 V ± 5%; V_{SS} = −5 V ± 5% AGND = DGND = 0 V; T_A = −40°C to +85°C unless otherwise noted)

Parameter	Min	Typ	Max	Units	Conditions
SIGNAL INPUTS					
PH/IP1, 2, 3, 4 Voltage Level		±2.8	±3.3	V p-p	DC to 50 kHz
PH/IPH1, 2, 3 Voltage Level			±4.25	V p-p	DC to 50 kHz
Input Impedance					
PH/IP1, 2, 3	7.5	10		kΩ	
PH/IPH1, 2, 3	13.5	18		kΩ	
PH/IP1, 4	1			MΩ	Mode 1 Only (2 Phase) Sin & Cos
Gain					
PH/IP1, 2, 3, 4	0.98	1	1.02		
PH/IPH1, 2, 3		0.56			
VECTOR PERFORMANCE					
3θ Input-Output					
Radius Error (Any Phase)		0.35	0.7	%	DC to 600 Hz
Angular Error[1, 2] (PH/IP)		9	18	arc min	DC to 600 Hz
(PH/IPH)			24	arc min	DC to 600 Hz
Monotonicity					Guaranteed Monotonic
Full Power Bandwidth		50		kHz	
Small Signal Bandwidth		200		kHz	
ANALOG SIGNAL OUTPUTS					
PH/OP1, 2, 3, 4					PH/IP, PH/IPH INPUTS
Output Voltage[3]		±2.8	±3.3	V p-p	DC to 50 kHz
Offset Voltage		2	5	mV	Inputs = 0 V
Slew Rate		2		V/μs	
Small Signal Step Response		1		μs	1° Input to Settle to ±1 LSB (Input to Output)
Output Resistance		15		Ω	
Output Drive Current	3.0	4.0		mA	Outputs to AGND
Resistive Load	2			kΩ	
Capacitive Load		50		pF	
STROBE					
Write	100			ns	Positive Pulse
Max Update Rate		366		kHz	
BUSY					
Pulse Width		1.7	2.5	μs	Conversion in Process
V_{OH}	4			V dc	I_{OH} = 0.5 mA
V_{OL}			1	V dc	I_{OL} = 0.5 mA
DIGITAL INPUTS					
DB1–DB12					
V_{IH}	3.5			V dc	
V_{IL}			1.5	V dc	
Input Current, I_{IN}			±10	μA	
Input Capacitance, C_{IN}		10		pF	
CONVERT MODE					
(CONV1, CONV2)					
V_{IH}	3.5			V dc	
V_{IL}			1.5	V dc	Internal 50 kΩ Pull-Up Resistor
Input Current			100	μA	
Input Capacitance		10		pF	
CONVERT LOGIC					
CONV1 CONV2					
NO CONNECT DGND					2-Phase Orthogonal with 2 Inputs Nominal Input Level
DGND V_{DD}					3-Phase (0°, 120°, 240°) with 3 Inputs Nominal/High Input Level
V_{DD} V_{DD}					3-Phase (0°, 120°, 240°) with 2 Inputs Nominal Input Level

Parameter	Min	Typ	Max	Units	Conditions
HOMOPOLAR OUTPUT					
HPOP–Output					
V_{OH}	4			V dc	I_{OH} = 0.5 mA
V_{OL}			1	V dc	I_{OL} = 0.5 mA
HPREF–REFERENCE		0.5		V dc	Homopolar Output–Internal I_{SOURCE} = 25 μA and 20 kΩ to AGND
HPFILT–FILTER		100		kΩ	Internal Resistor with External Capacitor = 220 nF
POWER SUPPLY					
V_{DD}	4.75	5	5.25	V dc	
V_{SS}	−5.25	−5	−4.75	V dc	
I_{DD}		4	10	mA	Quiescent Current
I_{SS}		4	10	mA	Quiescent Current

NOTES
[1]Angular accuracy includes offsets and gain errors. Stationary digital input and maximum analog frequency inputs.
[2]Included in the angular error is an allowance for the additional error caused by the phase delay as a function of the input frequency. For example if f_{INPUT} = 600 Hz, the contribution to the error due to phase delay in 650 ns × f_{INPUT} × 60 × 360 = 8.4 arc minutes.
[3]Output subject to input voltage and gain.
Specifications in **boldface** are production tested.
Specifications subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_{DD}$, $-V_{SS}$) . . . . . ±5 V dc ± 5%
Analog Input Voltage (PH/IP1, 2, 3, 4) . . . . . 2 V rms ± 10%
Analog Input Voltage (PH/IPH1, 2, 3) . . . . . 3 V rms ± 10%
Ambient Operating Temperature
Industrial (AP) . . . . . −40°C to +85°C

ORDERING GUIDE

Model	Temperature Temperature Range	Accuracy	Package Option*
AD2S100AP	−40°C to +85°C	18 arc min	P-44A

*P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

V_{DD} to AGND . . . . . −0.3 V to +7 V dc
V_{SS} to AGND . . . . . +0.3 V to −7 V dc
AGND to DGND . . . . . ±0.3 V dc
Analog Input Voltage to AGND . . . . . V_{SS} to V_{DD}
Digital Input Voltage to DGND . . −0.3 V to V_{DD} + 0.3 V dc
Digital Output Voltage to DGND . . −0.3 V to V_{DD} + 0.3 V dc
Analog Output Voltage to AGND
. . . . . V_{SS} − 0.3 V to V_{DD} + 0.3 V dc
Analog Output Load Condition (PH/OP1, 2, 3, 4
SINθ, COSθ) . . . . . 2 kΩ
Power Dissipation . . . . . 60 mW
Operating Temperature
Industrial (AP) . . . . . −40°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

CAUTION

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_{DD}$ and $-V_{SS}$ pins.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD2S100 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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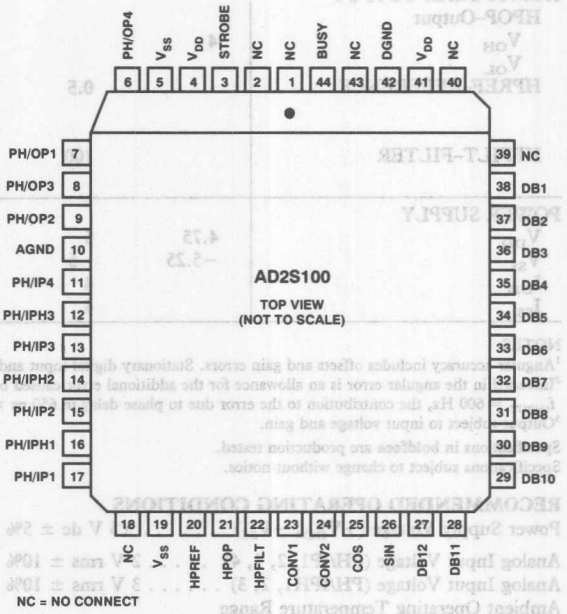
Pin	Mnemonic	Description
3	STROBE	Start Conversion
4	V_{DD}	Positive Power Supply
5	V_{SS}	Negative Power Supply
6	PH/OP4	Sin ($\theta + \phi$)
7	PH/OP1	Cos ($\theta + \phi$)
8	PH/OP3	Cos ($\theta + 240° + \phi$)
9	PH/OP2	Cos ($\theta + 120° + \phi$)
10	AGND	Analog Ground
11	PH/IP4	Sin θ Input
12	PH/IPH3	High Level Cos ($\theta + 240°$) Input
13	PH/IP3	Cos ($\theta + 240°$) Input
14	PH/IPH2	High Level Cos ($\theta + 120°$) Input
15	PH/IP2	Cos ($\theta + 120°$) Input
16	PH/IPH1	High Level Cos θ Input
17	PH/IP1	Cos (θ) Input
19	V_{SS}	Negative Power Supply
20	HPREF	Homopolar Reference
21	HPOP	Homopolar Output
22	HPFILT	Homopolar Filter
23	CONV1	Select Input Format (3 Phase/3 Wire, Sin θ
24	CONV2	Cos θ/Input, 3 Phase/2 Wire)
25	COS	Cos Output
26	SIN	Sin Output
27	DB12	(DB1 = MSB DB12 = LSB
38	DB1	Parallel Input Data)
41	V_{DD}	Positive Power Supply
42	DGND	Digital Ground
44	BUSY	Conversion in Progress



NOTES

Signal Inputs PH/IP and PH/IPH on Pin Nos. 11 through 17.

1. 90° orthogonal signals = Sin θ, Cos θ (Resolver) = PH/IP4 and PH/IP1.
2. Three phase, 120°, three wire signals
   = Cos θ, Cos (θ + 120°), Cos (θ + 240°).
   = PH/IP1, PH/IP2, PH/IP3
   High Level = PH/IPH1, PH/IPH2, PH/IPH3.
3. Three Phase, 120°, two wire signals = Cos (θ + 120°), Cos (θ + 240°) = PH/IP2, PH/IP3.

In all cases where any of the input Pins 11 through 17 are not used, they must be left unconnected.

drives is that the magnitude and position of the rotating air-gap rotor flux be known. This is normally carried out by measuring the rotor position via a position sensor and establishing a rotor reference frame that can be related to stator current coordinates.

To generate a flux component in the rotor, stator current is applied. A build-up of rotor flux is concluded which must be maintained by controlling the stator current, i_{ds}, parallel to the rotor flux. The rotor flux current component is the magnetizing current, i_{mr}.

Torque is generated by applying a current component which is perpendicular to the magnetizing current. This current is normally called the torque generating current, i_{qs}.

To orient and control both the torque and flux stator current vectors a coordinate transformation is carried out to establish a new reference frame related to the rotor. This complex calculation is carried out by the AD2S100 vector processor.

To expand upon the vector operator a description of a single vector rotation is of assistance. If it is considered that the moduli of a vector is OP and that through the movement of rotor position by ϕ, we require the new position of this vector it can be deduced as follows:

Let original vector OP = A (Cos θ + jSIN θ) where A is a constant;

so if, $OQ = \text{OP } e^{j\phi}$ (1)

and: $e^{j\phi} = \text{Cos } \phi + j\text{Sin } \phi$

$$OQ = A\,(Cos\,(\theta + \phi) + j\,Sin\,(\theta + \phi))$$
$$= A\,[Cos\,\theta\,Cos\,\phi - Sin\,\theta\,Sin\,\phi + jSin\,\theta\,Cos\,\phi + jCos\,\theta\,Sin\,\phi]$$
$$= A\,[(Cos\,\theta + jSin\,\theta)\,(Cos\,\phi + jSin\,\phi)] \quad (2)$$

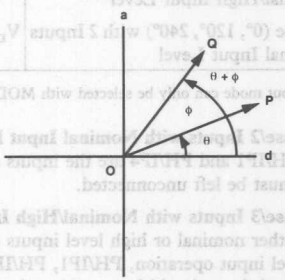


Figure 1. Vector Rotation in Polar Coordinate

The complex stator current vector can be represented as $i_s = i_{as} + ai_{bs} + a^2 i_{cs}$ where $a = e^{\frac{j2\pi}{3}}$ and $a^2 = e^{\frac{j4\pi}{3}}$. This can be replaced by rectangular coordinates as

$$i_s = i_{ds} + ji_{qs} \quad (3)$$

In this equation i_{ds} and i_{qs} represent the equivalent of a two-phase stator winding which establishes the same magnitude of MMF in a three-phase system. These inputs can be seen after the three-phase to two-phase transformation in the AD2S100 block diagram. Equation (3) therefore represents a three-phase to two-phase conversion.

now rotated by the operator $e^{j\phi}$, where $e^{j\phi} = \text{Cos } \phi + j\text{Sin } \phi$.

Here the term vector rotator comes into play where the stator current vector can be represented in rotor-based coordinates or visa versa.

The AD2S100 uses $e^{j\phi}$ as the core operator. Here ϕ represents the digital position angle which rotates as the rotor moves. In terms of the mathematical function, it rotates the orthogonal i_{ds} and i_{qs} components as follows:

$$i_{ds}' + ji_{qs}' = (I_{ds} + jI_{qs})\,e^{j\phi}$$

where i_{ds}', i_{qs}' = stator currents in the rotor reference frame. And

$$e^{j\phi} = Cos\,\phi + jSin\,\phi$$
$$= (I_{ds} + jI_{qs})(Cos\,\phi + jSin\,\phi)$$

The output from the AD2S100 takes the form of:

$$i_{ds}' = I_{ds}\,Cos\,\phi - I_{qs}\,Sin\,\phi$$
$$i_{qs}' = I_{ds}\,Sin\,\phi + I_{qs}\,Cos\,\phi$$

The matrix equation is:

$$\begin{bmatrix} i_{ds}' \\ i_{qs}' \end{bmatrix} = \begin{bmatrix} Cos\,\phi & -Sin\,\phi \\ Sin\,\phi & Cos\,\phi \end{bmatrix} \begin{bmatrix} I_{ds} \\ I_{qs} \end{bmatrix}$$

and it is shown in Figure 2.

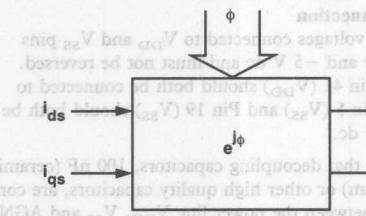


Figure 2. AD2S100 Vector Rotation Operation

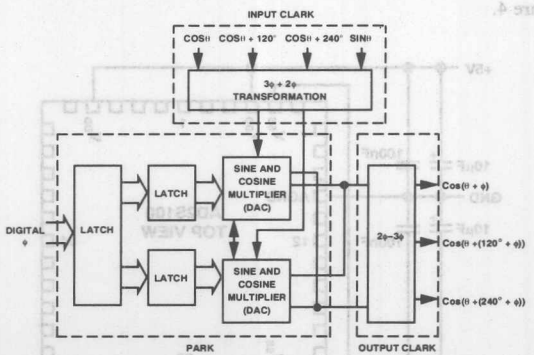


Figure 3. Converter Operation Diagram

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CONVERTER OPERATION

The architecture of the AD2S100 is illustrated in Figure 3. The AD2S100 is configured in the forward transformation which rotates the rotor frame coordinates to the stator frame.

Forward Rotation

In this configuration the 3ϕ–2ϕ Clark is bypassed, and inputs are fed directly into the quadrature (PH/IP4) and direct (PH/IP1) inputs to the Park transform, $e^{i\phi}$, where ϕ is defined by the AD2S100's digital input. Position data, ϕ, is loaded into the input latch on the positive edge of the strobe pulse. (For detail on the timing, please refer to the "timing diagram.") The negative edge of the strobe signifies that conversion has commenced. A busy pulse is subsequently produced as data is passed from the input latches to the Sin and Cos multipliers. During the loading of the multiplier, the busy pulse remains high to ensure simultaneous setting of ϕ in both the Sin and Cos registers.

The negative edge of the busy pulse signifies that the multipliers are set up and the orthogonal analog inputs are multiplied real time. The resultant two outputs are accessed via the PH/OP1 (Pin 7) and PH/OP4 (Pin 6), alternatively they can be directly applied to the output Clark transform. The Clark output is the vector sum of the analog input vector (Cosθ (PH/OP1), Cos (θ + 120°) (PH/OP2), Cos (θ + 240°) (PH/OP3) and the digital input vector ϕ.

For other configurations, please refer to "Forward and Reverse Transformation."

CONNECTING THE CONVERTER

Power Supply Connection

The power supply voltages connected to V_{DD} and V_{SS} pins should be +5 V dc and −5 V dc and must not be reversed. Pin 4 (V_{DD}) and Pin 41 (V_{DD}) should both be connected to +5 V; similarly, Pin 5 (V_{SS}) and Pin 19 (V_{SS}) should both be connected to −5 V dc.

It is recommended that decoupling capacitors, 100 nF (ceramic) and 10 μF (tantalum) or other high quality capacitors, are connected in parallel between the power line V_{DD}, V_{SS} and AGND adjacent to the converter. Separate decoupling capacitors should be used for each converter. The connections are shown in Figure 4.

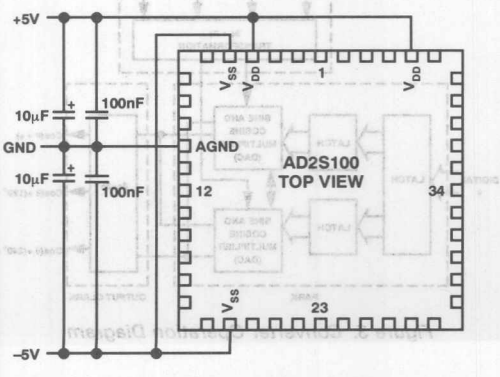

Figure 4. AD2S100 Power Supply Connection

ANALOG SIGNAL INPUT AND OUTPUT CONNECTIONS

Input Analog Signals

All analog signal inputs to AD2S100 are voltages. There are two different voltage levels of three-phase (0°, 120°, 240°) signal inputs. One is the nominal level, which is ±2.8 V dc or 2 V rms and the corresponding input pins are PH/IP1 (Pin 17), PH/IP2 (Pin 15), PH/IP3 (Pin 13) and PH/IP4 (Pin 11).

The high level inputs can accommodate voltages from nominal up to a maximum of $\pm V_{DD}/V_{SS}$. The corresponding input pins are PH/IPH1 (Pin 16), PH/IPH2 (Pin 14) and PH/IPH3 (Pin 12). The homopolar output can only be used in the three-phase connection mode.

The converter can accept both two-phase format and three-phase format input signals. For the two-phase format input, the two inputs must be orthogonal to each other. For the three-phase format input, there is the choice of using all three inputs or using two of the three inputs. In the latter case, the third input signal will be generated internally by using the information of other two inputs. The high level input mode, however, can only be selected with three-phase/three-input format. All these different conversion modes, including nominal/high input level and two/three-phase input format can be selected using two select pins (Pin 23, Pin 24). The functions are summarized in Table I.

Table I. Conversion Mode Selection

Mode	Description	CONV1 (Pin 23)	CONV2 (Pin 24)
MODE1	2-Phase Orthogonal with 2 Inputs Nominal Input Level	NC	DGND
MODE2	3-Phase (0°, 120°, 240°) with 3 Inputs Nominal/High Input Level*	DGND	V_{DD}
MODE3	3-Phase (0°, 120°, 240°) with 2 Inputs Nominal Input Level	V_{DD}	V_{DD}

*The high level input mode can only be selected with MODE2.

MODE1: 2-Phase/2 Inputs with Nominal Input Level
In this mode, PH/IP1 and PH/IP4 are the inputs and the Pins 12 through 16 must be left unconnected.

MODE2: 3-Phase/3 Inputs with Nominal/High Input Level
In this mode, either nominal or high level inputs can be used. For nominal level input operation, PH/IP1, PH/IP2 and PH/IP3 are the inputs, and there should be no connections to PH/IPH1, PH/IPH2 and PH/IPH3; similarly, for high level input operation, the PH/IPH1, PH/IPH2 and PH/IPH3 are the inputs, and there should be no connections to PH/IP1, PH/IP2 and PH/IP3. In both cases, the PH/IP4 should be left unconnected. For high level signal input operation, select MODE2 only.

MODE3: 3-Phase/2 Inputs with Nominal Input Level
In this mode, PH/IP2 and PH/IP3 are the inputs and the third signal will be generated internally by using the information of other two inputs. It is recommended that PH/IP1, PH/IPH1, PH/IPH2, PH/IP4 and PH/IPH3 should be left unconnected.

Output Analog Signals
There are three forms of analog output from the AD2S100.

Sin/Cos orthogonal output signals are derived from the Clark/three-to-two-phase conversion before the Park angle rotation. These signals are available on Pin 25 (Cos θ) and Pin 26 (Sin θ), and occur before Park angle rotation.

Three-Phase Output Signals
(Cos (θ + ϕ), Cos (ϕ + θ + 120°), Cos (ϕ + θ + 240°)), where ϕ represents digital input angle. These signals are available on Pin 7 (PH/OP1), Pin 9 (PH/OP2) and Pin 8 (PH/OP3), respectively.

Two-Phase (Sin (θ + ϕ), Cos (θ + ϕ)) Signals
These represent the output of the coordinate transformation. These signals are available on Pin 6 (PH/OP4, Sin (θ + ϕ)) and Pin 7 (PH/OP1, Cos (θ + ϕ)).

HOMOPOLAR OUTPUT

Homopolar Reference
In a three-phase ac system, the sum of the three inputs to the converter can be used to indicate whether or not the phases are balanced.

If V_{SUM} = PH/IP1 + PH/IP2 + PH/IP3 (or PH/IPH1 + PH/IPH2 +PH/IPH3) this can be rewritten as V_{SUM} = [Cosθ,+ Cos (θ + 120°) + Cos (θ + 240°)] = 0. Any imbalances in the line will cause the sum $V_{SUM} \neq 0$. The AD2S100 homopolar output (HPOP) goes high when $V_{SUM} > 3 \times V_{ts}$. The voltage level at which the HPOP indicates an imbalance is determined by the HPREF threshold, V_{ts}. This is set internally at ±0.5 V dc (±0.1 V dc). The HPOP goes high when

$$V_{ts} < \frac{|Cos\theta + Cos(\theta + 120°) + Cos(\theta + 240°)|}{3} \times V$$

where V is the nominal input voltage.

With no external components V_{SUM} must exceed ±1.5 V dc in order for HPOP to indicate an imbalance. The sensitivity of the threshold can be reduced by connecting an external resistor between HPOP and ground as shown in Figure 5, where,

$$V_{ts} = \frac{0.5\ R_{EXT}}{R_{EXT} + 20000}$$

R_{EXT} = Ω
V_{ts} = V dc.

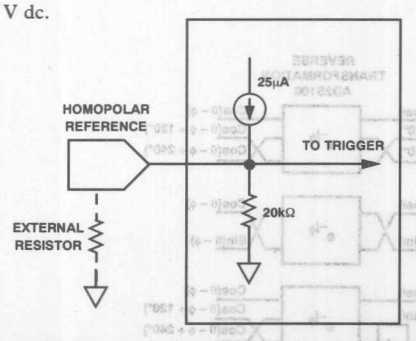

Figure 5. The Equivalent Homopolar Reference Input Circuitry

Example: From the equivalent circuit, it can be seen that the inclusion of a 20 kΩ resistor will reduce V_{ts} to ±0.25 V dc. This corresponds to an imbalance of ±0.75 V dc in the inputs.

Homopolar Filtering
The equation V_{SUM} = Cosθ + Cos (θ + 120°) + Cos (θ + 240°) = 0 denotes an imbalance when $V_{SUM} \neq 0$. There are conditions, however, when an actual imbalance will occur and the conditions as define by V_{SUM} will be valid. For example, if the first phase was open circuit when θ = 90° or 270°, the first phase is valid at 0 V dc. V_{SUM} is valid, therefore, when Cosθ is close to 0. In order to detect an imbalance θ has to move away from 90° or 270°, i.e., when on a balanced line Cos θ ≠ 0.

Line imbalance is detected as a function of HPREF, either set by the user or internally set at ±0.5 V dc. This corresponds to a dead zone when ϕ = 90° or 270° ± 30°, i.e., V_{SUM} = 0, and, therefore, no indicated imbalance. If an external 20 kΩ resistor is added, this halves V_{ts} and reduces the zone to ±15°. Note this example only applies if the first phase is detached.

In order to prevent this false triggering an external capacitor needs to be placed from HPFILT to ground, as shown in Figure 5. This averages out the perceived imbalance over a complete cycle and will prevent the HPOP from alternatively indicating balance and imbalance over θ = 0° to 360°.

For

$$\frac{d\theta}{dt} = 1000\ rpm \quad C_{EXT} = 200\ nF$$

$$\frac{d\theta}{dt} = 100\ rpm \quad C_{EXT} = 2.2\ \mu F$$

Note: The slower the input rotational speed, the larger the time constant required over which to average the HPOP output. Use of the homopolar output at slow rotational speeds becomes impractical with respect to the increased value for C_{EXT}.

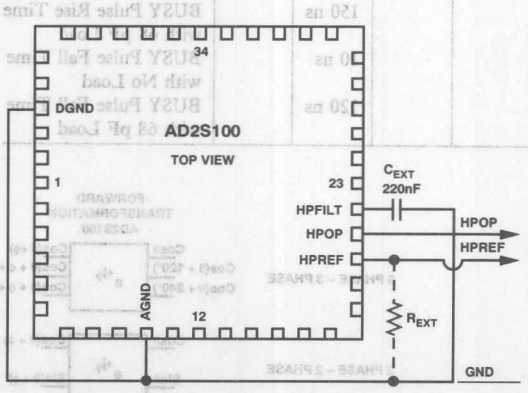

Figure 6. AD2S100 Homopolar Output Connections

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Busy Output

The state of converter is indicated by the state of the BUSY output (Pin 44). The BUSY output will go HI at the negative edge of the STROBE input. This is used to synchronize digital input data and load the digital angular rotation information into the device counter. The BUSY output will remain HI for 2 μs, and go LO until the next strobe negative edge occurs.

Strobe Input

The width of the positive STROBE pulse should be at least 100 ns, in order to successfully start the conversion. The maximum frequency of STROBE input is 366 kHz, i.e., there should be at least 2.73 μs from the negative edge of one STROBE pulse to the next rising edge. This is illustrated by the following timing diagram and table.

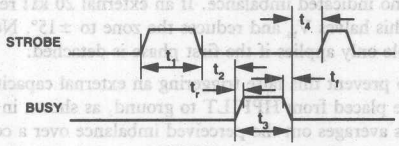

Figure 7. AD2S100 Timing Diagram

Note: Digital data should be stable 25 ns before and after positive strobe edge.

Table II. AD2S100 Timing Table

Parameter	Min	Typ	Max	Condition
t_1	100 ns			STROBE Pulse Width
t_2		30 ns		STROBE ↓ to BUSY ↑
t_3	1.7 μs		2.5 μs	BUSY Pulse Width
t_4		100 ns		BUSY ↓ to STROBE ↑
t_r		20 ns		BUSY Pulse Rise Time with No Load
		150 ns		BUSY Pulse Rise Time with 68 pF Load
t_f		10 ns		BUSY Pulse Fall Time with No Load
		120 ns		BUSY Pulse Fall Time with 68 pF Load

Figure 8 shows a typical circuit configuration for the AD2S100 in a three phase, nominal level input mode (MODE2).

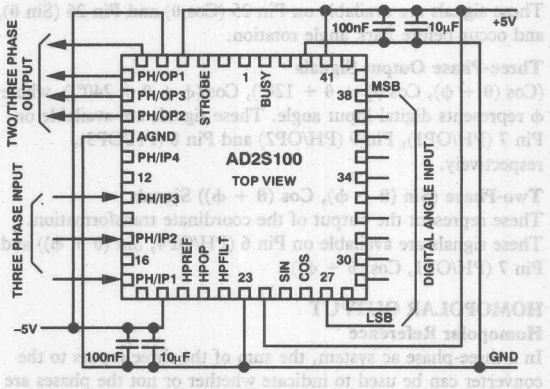

Figure 8. Typical Circuit Configuration

APPLICATIONS

Forward and Reverse Transformation

The AD2S100 can perform both forward and reverse transformations. The section "Theory of Operation" explains how the chip operates with the core operator $e^{+j\phi}$, which performs a forward transformation. The reverse transformation, $e^{-j\phi}$, is not mentioned in the above sections of the data sheet simply to avoid the confusion in the functionality and pinout. However, the reverse transformation is very useful in many different applications, and the AD2S100 can be easily configured in a reverse transformation configuration. Figure 9 shows four different phase input/output connections for AD2S100 reverse transformation operation.

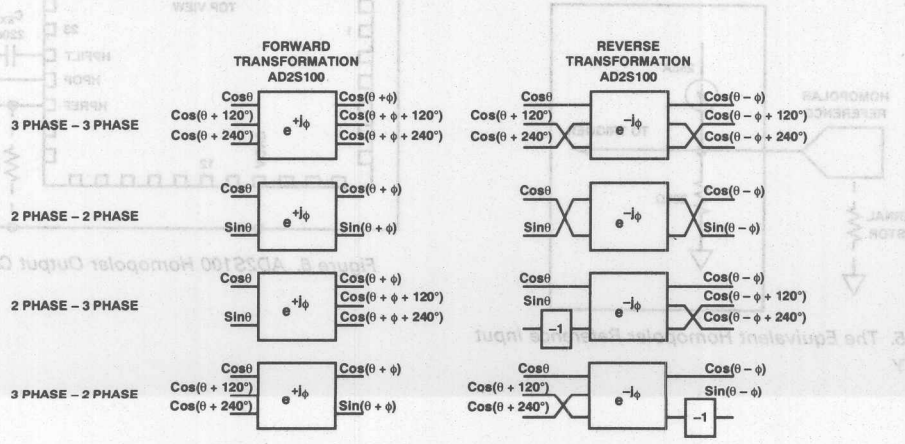

Figure 9. Reverse Transformation Connections

√In Figure 9, "−1" operator performs a 180° phase shift operation. It can be illustrated by a 2-phase-to-3-phase reverse transformation. An example is shown in Figure 10.

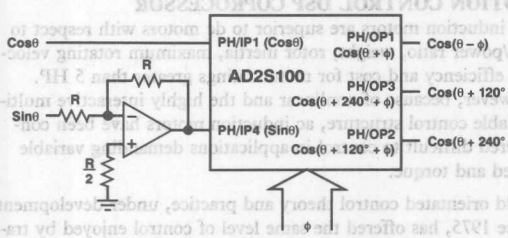

Figure 10. Two-Phase to Three-Phase Reverse Transformation

Field Oriented Control of AC Induction Machine in a Rotor Flux Frame

The architecture shown in Figure 11 identifies a simplified scheme where the AD2S100 permits the DSP computing core to execute the motor control in what is normally termed the rotor reference frame. This reference frame actually operates in synchronism with the rotor of a motor. This has significant benefits regarding motor control efficiency and economics. The calculating power required in the rotor reference frame is significantly reduced because the currents and flux are rotating at the slip frequency. This permits calculations to be carried out in time frames of, 100 µs, or under by a fixed-point DSP. Benchmark timing in this type of architecture can attain floating-point speed processing with a fixed-point processor. Perhaps the largest advantage is in the ease with which the rotor flux position can be obtained. A large amount of computation time is, therefore, removed by the AD2S100 vector processors due to the split architecture shown in Figure 11. Motor control systems employing one DSP to carry out the cartesian to polar transformations required for vector control are, therefore, tasked with additional duties due to the fact that they normally operate in the flux reference frame.

The robustness of the control system can also be increased by carrying out the control in the rotor reference frame. This is achieved through the ability to increase and improve both the algorithm quality in nonlinear calculations attributed to magnetizing inductance and rotor time constant for example. An increase in sampling time can also be concluded with this architecture by avoiding the additional computing associated with number truncation and rounding errors which reduce the signal to noise rejection ratio.

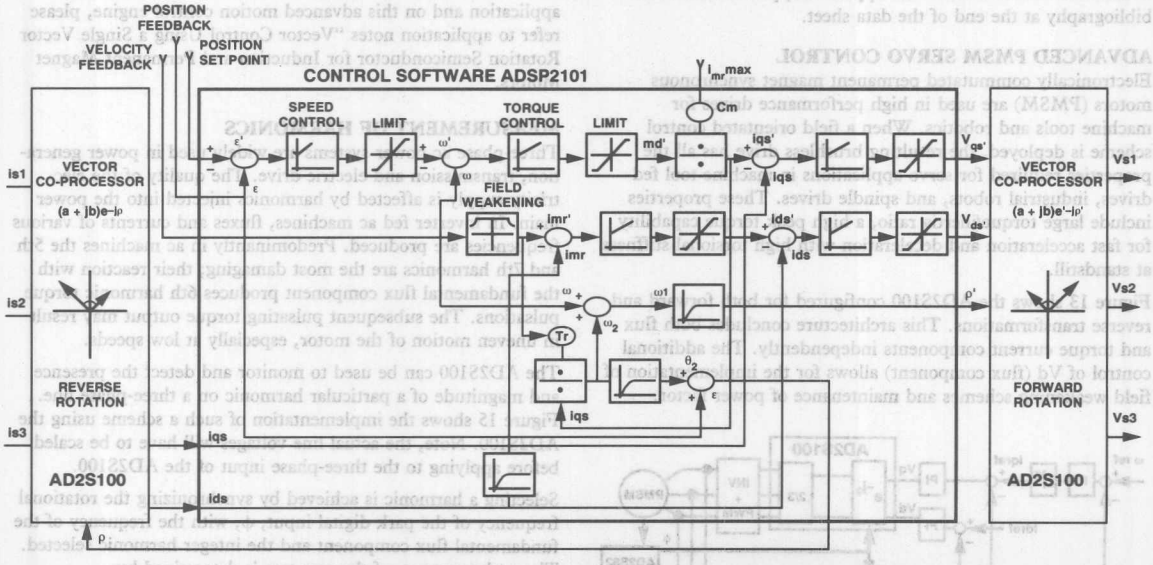

Figure 11. Rotor Reference Frame Architecture

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SIMPLE SLIP CONTROL

In an adjustable-frequency drive, the control strategy must ensure that motor operation is restricted to low slip frequencies, resulting in stable operation with a high power factor and a high torque per stator ampere. Figure 12 shows the block diagram of simple slip control using the AD2S100. Here, the slip frequency command ω_2 and the current amplitude command are sent to the microprocessor to generate two orthogonal signals, $|I|$ Sin θ and $|I|$ Cos θ here ($\theta = \omega_2$.) With the actual shaft position angle, ϕ, (resolver-to-digital converter) and the orthogonal signals from

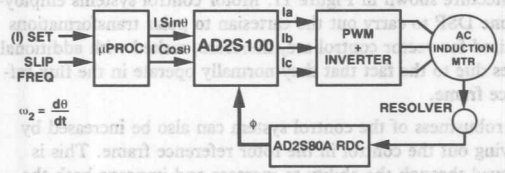

Figure 12. Slip Control of AC Induction Motor with AD2S100

the µP, the AD2S100 generates the inverter frequency and amplitude command into a three-phase format. The three-phase sine wave reference currents are reproduced in the stator phases. For general applications, both the steady-state and dynamic performance of this simple control scheme is satisfactory. For detailed information about this application, please refer to the bibliography at the end of the data sheet.

ADVANCED PMSM SERVO CONTROL

Electronically commutated permanent magnet synchronous motors (PMSM) are used in high performance drives for machine tools and robotics. When a field orientated control scheme is deployed, the resulting brushless drive has all the properties required for servo applications in machine tool fed drives, industrial robots, and spindle drives. These properties include large torque/inertia ratio, a high peak torque capability for fast acceleration and deceleration with high torsional stiffness at standstill.

Figure 13 shows the AD2S100 configured for both forward and reverse transformations. This architecture concludes both flux and torque current components independently. The additional control of Vd (flux component) allows for the implementation of field weakening schemes and maintenance of power factor.

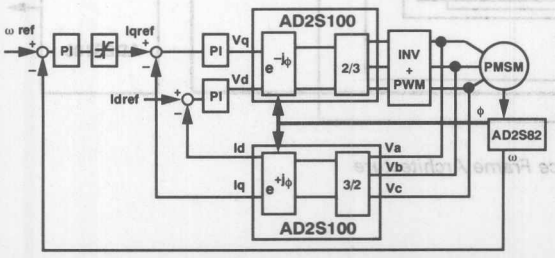

Figure 13. PMSM Servo Control Using AD2S100

For more detailed information, please refer to the application note "Vector Control Using a Single Vector Rotation Semiconductor for Induction and Permanent Magnet Motors."

MOTION CONTROL DSP COPROCESSOR

AC induction motors are superior to dc motors with respect to size/power ratio, weight, rotor inertia, maximum rotating velocity, efficiency and cost for motor ratings greater than 5 HP. However, because of nonlinear and the highly interactive multivariable control structure, ac induction motors have been considered difficult to control in applications demanding variable speed and torque.

Field orientated control theory and practice, under development since 1975, has offered the same level of control enjoyed by traditional dc machines. Practical implementation of these algorithms involves the use of DSP and microprocessor based architectures. The AD2S100 removes the needs for software implementation of the rotor-to-stator and stator-to-rotor transformations in the DSP or µP. The reduction in throughput times from typically 100 µs (µP) and 40 µs (DSP) to 2 µs increases system bandwidths while also allowing additional features to be added to the CPU. The combination of the fixed point ADSP-2101 and the AD2S100, the "advanced motion control engine" shown in Figure 14, enables bandwidths previously attainable only through the use of floating point devices.

For more detailed information on the AD2S100 vector control application and on this advanced motion control engine, please refer to application notes "Vector Control Using a Single Vector Rotation Semiconductor for Induction and Permanent Magnet Motors."

MEASUREMENT OF HARMONICS

Three-phase ac power systems are widely used in power generation, transmission and electric drive. The quality of the electricity supply is affected by harmonics injected into the power main. In inverter fed ac machines, fluxes and currents of various frequencies are produced. Predominantly in ac machines the 5th and 7th harmonics are the most damaging; their reaction with the fundamental flux component produces 6th harmonic torque pulsations. The subsequent pulsating torque output may result in uneven motion of the motor, especially at low speeds.

The AD2S100 can be used to monitor and detect the presence and magnitude of a particular harmonic on a three-phase line. Figure 15 shows the implementation of such a scheme using the AD2S100. Note, the actual line voltages will have to be scaled before applying to the three-phase input of the AD2S100.

Selecting a harmonic is achieved by synchronizing the rotational frequency of the park digital input, ϕ, with the frequency of the fundamental flux component and the integer harmonic selected. The update rate, r, of the counters is determined by:

$$r = 4096 \times \frac{n \times \omega}{2\pi}$$

Here, r = input clock pulse rate (pulses/second);
n = the order of harmonics to be measured;
ω = fundamental angular frequency of the ac signal.

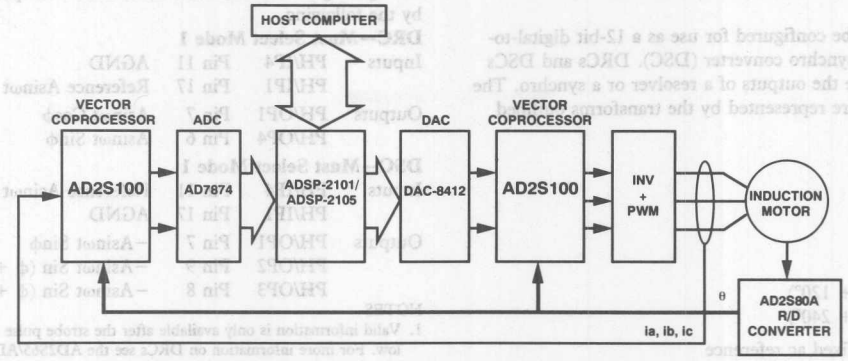

Figure 14. Advanced Motion Control Engine

The magnitude of the n-th harmonic as well as the fundamental component in the power line is represented by the output of the low-pass filter, a_k. In concert with magnitude of the harmonic the AD2S100 homopolar output will indicate whether the three phases are balanced or not. For more details about this application, refer to the related application note listed in the bibliography.

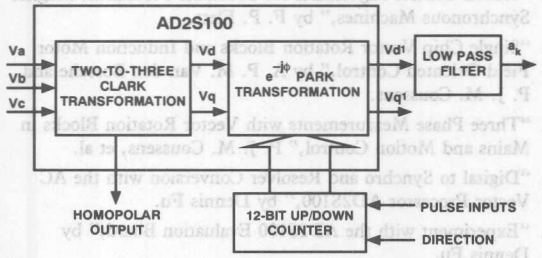

Figure 15. Harmonics Measurement Using AD2S100

MULTIPLE POLE MOTORS

For multi-pole motor applications where a single speed resolver is used, the AD2S100 input has to be configured to match the electrical cycle of the resolver with the phasing of the motor windings. The input to the AD2S100 is the output of a resolver-to-digital converter, e.g., AD2S80A series. The parallel output of the converter needs to be multiplied by 2^{n-1}, where n = the number of pole parts of the motor. In practice this is implemented by shifting the parallel output of the converter left relative to the number of pole pairs.

Figure 16 shows the generic configuration of the AD2S80A with the AD2S100 for a motor with n pole pairs. The MSB of the AD2S100 is connected to MSB-(n-1) bit of the AD2S80A digital output, MSB-1 bit to MSB-(n-2) bit, . . . , LSB bit to LSB bit of AD2S80A, etc.

Figure 17 shows the AD2S80A configured for use with a four pole motor, where n = 2. Using the formula described the MSB is shifted left once.

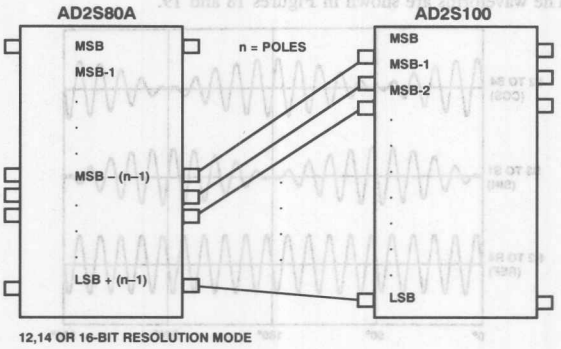

Figure 16. A General Consideration in Connecting R/D Converter and AD2S100 for Multiple Pole Motors

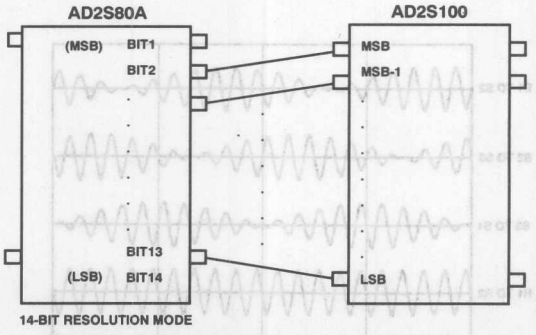

Figure 17. Connecting of R/D Converter AD2S80A and AD2S100 for Four-Pole Motor Application

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DIGITAL-TO-RESOLVER AND SYNCHRO CONVERSION

The AD2S100 can be configured for use as a 12-bit digital-to-resolver (DRC) or synchro converter (DSC). DRCs and DSCs are used to simulate the outputs of a resolver or a synchro. The simulated outputs are represented by the transforms outlined below.

Resolver Outputs

Asinωt.cosϕ
Asinωt.sinϕ

Synchro Outputs

Asinωt.sinϕ
Asinωt.sin (ϕ + 120°)
Asinωt.sin (ϕ + 240°)

where: *Asinωt* = fixed ac reference

ϕ = digital input angle, i.e., shaft position

The waveforms are shown in Figures 18 and 19.

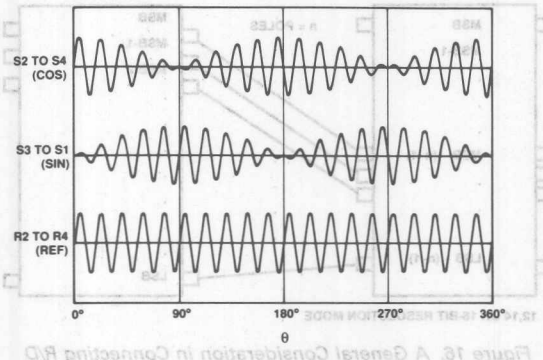


Figure 18. Electrical Representation and Typical Resolver Signals

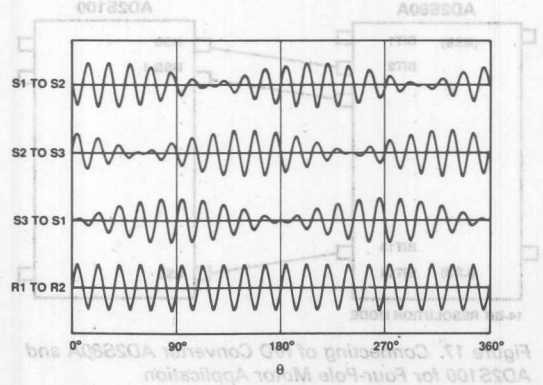


Figure 19. Electrical Representation and Typical Synchro Signals

Configuring the AD2S100 for DRC and DSC operation is done by the following.

DRC—Must Select Mode 1

Inputs	PH/IP4	Pin 11	AGND
	PH/IP1	Pin 17	Reference Asinωt
Outputs	PH/OP1	Pin 7	Asinωt Cosϕ
	PH/OP4	Pin 6	Asinωt Sinϕ

DSC—Must Select Mode 1

Inputs	PH/IP4	Pin 11	Reference Asinωt
	PH/IP1	Pin 17	AGND
Outputs	PH/OP1	Pin 7	−Asinωt Sinϕ
	PH/OP2	Pin 9	−Asinωt Sin (ϕ + 120°)
	PH/OP3	Pin 8	−Asinωt Sin (ϕ + 240°)

NOTES

1. Valid information is only available after the strobe pulse and BUSY go low. For more information on DRCs see the AD2S65/AD2S66 data sheet.
2. To correct for inverse phasing of the DSC outputs the reference should be inverted, or the MSB can be inverted.

APPLICATION NOTES LIST

1. "Vector Control Using a Single Vector Rotation Semiconductor for Induction and Permanent Magnet Motors," by F. P. Flett, Analog Devices.
2. "Gamana – DSP Vector Coprocessor for Brushless Motor Control," by Analog Devices and Infosys Manufacturing System.
3. "Silicon Control Algorithms for Brushless Permanent Magnet Synchronous Machines," by F. P. Flett.
4. "Single Chip Vector Rotation Blocks and Induction Motor Field Oriented Control," by A. P. M. Van den Bossche and P. J. M. Coussens.
5. "Three Phase Measurements with Vector Rotation Blocks in Mains and Motion Control," P. J. M. Coussens, et al.
6. "Digital to Synchro and Resolver Conversion with the AC Vector Processor AD2S100," by Dennis Fu.
7. "Experiment with the AD2S100 Evaluation Board," by Dennis Fu.

ANALOG DEVICES

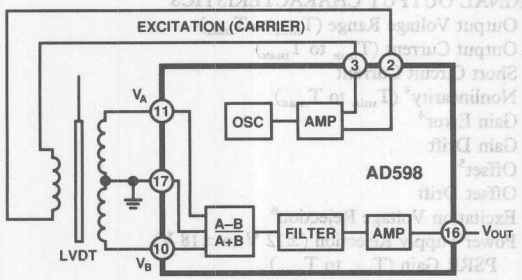
LVDT Signal Conditioner

AD598

FEATURES

- Single Chip Solution, Contains Internal Oscillator and Voltage Reference
- No Adjustments Required
- Insensitive to Transducer Null Voltage
- Insensitive to Primary to Secondary Phase Shifts
- DC Output Proportional to Position
- 20 Hz to 20 kHz Frequency Range
- Single or Dual Supply Operation
- Unipolar or Bipolar Output
- Will Operate a Remote LVDT at Up to 300 Feet
- Position Output Can Drive Up to 1000 Feet of Cable
- Will Also Interface to an RVDT
- Outstanding Performance
  - Linearity: 0.05% of FS max
  - Output Voltage: ±11 V min
  - Gain Drift: 50 ppm/°C of FS max
  - Offset Drift: 50 ppm/°C of FS max

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD598 is a complete, monolithic Linear Variable Differential Transformer (LVDT) signal conditioning subsystem. It is used in conjunction with LVDTs to convert transducer mechanical position to a unipolar or bipolar dc voltage with a high degree of accuracy and repeatability. All circuit functions are included on the chip. With the addition of a few external passive components to set frequency and gain, the AD598 converts the raw LVDT secondary output to a scaled dc signal. The device can also be used with RVDT transducers.

The AD598 contains a low distortion sine wave oscillator to drive the LVDT primary. The LVDT secondary output consists of two sine waves that drive the AD598 directly. The AD598 operates upon the two signals, dividing their difference by their sum, producing a scaled unipolar or bipolar dc output.

The AD598 uses a unique ratiometric architecture (patent pending) to eliminate several of the disadvantages associated with traditional approaches to LVDT interfacing. The benefits of this new circuit are: no adjustments are necessary, transformer null voltage and primary to secondary phase shift does not affect system accuracy, temperature stability is improved, and transducer interchangeinterchangeabilityability is improved.

The AD598 is available in two performance grades:

Grade	Temperature Range	Package
AD598JR	0 to +70°C	20-Pin Small Outline (SOIC)
AD598AD	−40°C to +85°C	20-Pin Ceramic DIP

It is also available processed to MIL-STD-883B, for the military range of −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD598 offers a monolithic solution to LVDT and RVDT signal conditioning problems; few extra passive components are required to complete the conversion from mechanical position to dc voltage and no adjustments are required.
2. The AD598 can be used with many different types of LVDTs because the circuit accommodates a wide range of input and output voltages and frequencies; the AD598 can drive an LVDT primary with up to 24 V rms and accept secondary input levels as low as 100 mV rms.
3. The 20 Hz to 20 kHz LVDT excitation frequency is determined by a single external capacitor. The AD598 input signal need not be synchronous with the LVDT primary drive. This means that an external primary excitation, such as the 400 Hz power mains in aircraft, can be used.
4. The AD598 uses a ratiometric decoding scheme such that primary to secondary phase shifts and transducer null voltage have absolutely no effect on overall circuit performance.
5. Multiple LVDTs can be driven by a single AD598, either in series or parallel as long as power dissipation limits are not exceeded. The excitation output is thermally protected.
6. The AD598 may be used in telemetry applications or in hostile environments where the interface electronics may be remote from the LVDT. The AD598 can drive an LVDT at the end of 300 feet of cable, since the circuit is not affected by phase shifts or absolute signal magnitudes. The position output can drive as much as 1000 feet of cable.
7. The AD598 may be used as a loop integrator in the design of simple electromechanical servo loops.

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD598—SPECIFICATIONS (typical @ +25°C and ±15 V dc, C1 = 0.015 μF, R2 = 80 kΩ, R_L = 2 kΩ, unless otherwise noted. See Figure 7.)

	V_A+V_B						
OVERALL ERROR[2]							
T_{min} to T_{max}		0.6	2.35		0.6	1.65	% of FS
SIGNAL OUTPUT CHARACTERISTICS							
Output Voltage Range (T_{min} to T_{max})	±11			±11			V
Output Current (T_{min} to T_{max})	8			6			mA
Short Circuit Current		20			20		mA
Nonlinearity[3] (T_{min} to T_{max})		75	±500		75	±500	ppm of FS
Gain Error[4]		0.4	±1		0.4	±1	% of FS
Gain Drift		20	±100		20	±50	ppm/°C of FS
Offset[5]		0.3	±1		0.3	±1	% of FS
Offset Drift		7	±200		7	±50	ppm/°C of FS
Excitation Voltage Rejection[6]		100			100		ppm/dB
Power Supply Rejection (±12 V to ±18 V)							
PSRR Gain (T_{min} to T_{max})	300	100		400	100		ppm/V
PSRR Offset (T_{min} to T_{max})	100	15		200	15		ppm/V
Common Mode Rejection (±3 V)							
CMRR Gain (T_{min} to T_{max})	100	25		200	25		ppm/V
CMRR Offset (T_{min} to T_{max})	100	6		200	6		ppm/V
Output Ripple[7]		4			4		mV rms
EXCITATION OUTPUT CHARACTERISTICS (@ 2.5 kHz)							
Excitation Voltage Range	2.1		24	2.1		24	V rms
Excitation Voltage							
(R1 = Open)[8]	1.2		2.1	1.2		2.1	V rms
(R1 = 12.7 kΩ)[8]	2.6		4.1	2.6		4.1	V rms
(R1 = 487 Ω)[8]	14		20	14		20	V rms
Excitation Voltage TC[9]		600			600		ppm/°C
Output Current	30			30			mA rms
T_{min} to T_{max}	12			12			mA rms
Short Circuit Current		60			60		mA
DC Offset Voltage (Differential, R1 = 12.7 kΩ)							
T_{min} to T_{max}		30	±100		30	±100	mV
Frequency	20		20k	20		20k	Hz
Frequency TC, (R1 = 12.7 kΩ)		200			200		ppm/°C
Total Harmonic Distortion		−50			−50		dB
SIGNAL INPUT CHARACTERISTICS							
Signal Voltage	0.1		3.5	0.1		3.5	V rms
Input Impedance		200			200		kΩ
Input Bias Current (AIN and BIN)		1	5		1	5	μA
Signal Reference Bias Current		2	10		2	10	μA
Excitation Frequency	0		20	0		20	kHz
POWER SUPPLY REQUIREMENTS							
Operating Range	13		36	13		36	V
Dual Supply Operation (±10 V Output)	±13			±13			V
Single Supply Operation							
0 to +10 V Output	17.5			17.5			V
0 to −10 V Output	17.5			17.5			V
Current (No Load at Signal and Excitation Outputs)		12	15		12	15	mA
T_{min} to T_{max}			16			18	mA
TEMPERATURE RANGE							
JR (SOIC)	0		70				°C
AD (DIP)				−40		+85	°C
PACKAGE OPTION[10]							
SOIC (R-20)	AD598JR						
Side Brazed DIP (D-20)				AD598AD			

NOTES

[1]V_A and V_B represent the Mean Average Deviation (MAD) of the detected sine waves. Note that for this Transfer Function to linearly represent positive displacement, the sum of V_A and V_B of the LVDT must remain constant with stroke length. See "Theory of Operation." Also see Figures 7 and 12 for R2.

[2]From T_{min} to T_{max} the overall error due to the AD598 alone is determined by combining gain error, gain drift and offset drift. For example, the worst case overall error for the AD598AD from T_{min} to T_{max} is calculated as follows: overall error = gain error at +25°C (±1% full scale) + gain drift from −40°C to +25°C (50 ppm/°C of FS × +65°C) + offset drift from −40°C to +25°C (50 ppm/°C of FS× 65°C) = ±1.65% of full scale. Note that 1000 ppm of full scale equals 0.1% of full scale. Full scale is defined as the voltage difference between the maximum positive and maximum negative output.

[3]Nonlinearity of the AD598 only, in units of ppm of full scale. Nonlinearity is defined as the maximum measured deviation of the AD598 output voltage from a straight line. The straight line is determined by connecting the maximum produced full-scale negative voltage with the maximum produced full-scale positive voltage.

[4]See Transfer Function.

[5]This offset refers to the $(V_A-V_B)/(V_A+V_B)$ input spanning a full-scale range of ±1. [For $(V_A-V_B)/(V_A+V_B)$ to equal +1, V_B must equal zero volts; and correspondingly for $(V_A-V_B)/(V_A+V_B)$ to equal −1, V_A must equal zero volts. Note that offset errors do not allow accurate use of zero magnitude inputs; practical inputs are limited to 100 mV rms.] The ±1 span is a convenient reference point to define offset referred to input. For example, with this input span a value of R2 = 20 kΩ would give V_{OUT} span a value of ±10 volts. Caution, most LVDTs will typically exercise less of the $(V_A-V_B)/(V_A+V_B)$ input span and thus require a larger value of R2 to produce the ±10 V output span. In this case the offset is correspondingly magnified when referred to the output voltage. For example, a Schaevitz E100 LVDT requires 80.2 kΩ for R2 to produce a ±10.69 V output and $(V_A-V_B)/(V_A+V_B)$ equals 0.27. This ratio may be determined from the graph shown in Figure 18, $(V_A-V_B)/(V_A+V_B)$ = (1.71 V rms−0.99 V rms)/(1.71 V rms+0.99 V rms). The maximum offset value referred to the ±10.69 V output may be determined by multiplying the maximum value shown in the data sheet (±1% of FS by 1/0.27 which equals ±3.7% maximum. Similarly, to determine the maximum values of offset drift, offset CMRR and offset PSRR when referred to the ±10.69 V output, these data sheet values should also be multiplied by (1/0.27). For this example, for the AD598AD the maximum values of offset drift, PSRR offset and CMRR offset would be: 185 ppm/°C of FS; 741 ppm/V and 741 ppm/V respectively when referred to the ±10.69 V output.

[6]For example, if the excitation to the primary changes by 1 dB, the gain of the system will change by typically 100 ppm.

[7]Output ripple is a function of the AD598 bandwidth determined by C2, C3 and C4. See Figures 16 and 17.

[8]R1 is shown in Figures 7 and 12.

[9]Excitation voltage drift is not an important specification because of the ratiometric operation of the AD598.

[10]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tested are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

THERMAL CHARACTERISTICS

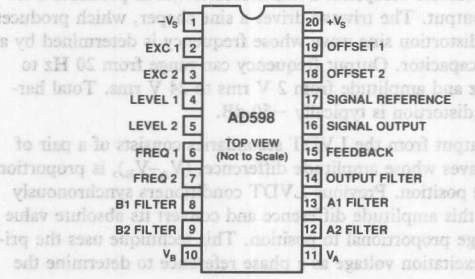
	θ_{JC}	θ_{JA}
SOIC Package	22°C/W	80°C/W
Side Brazed Package	25°C/W	85°C/W

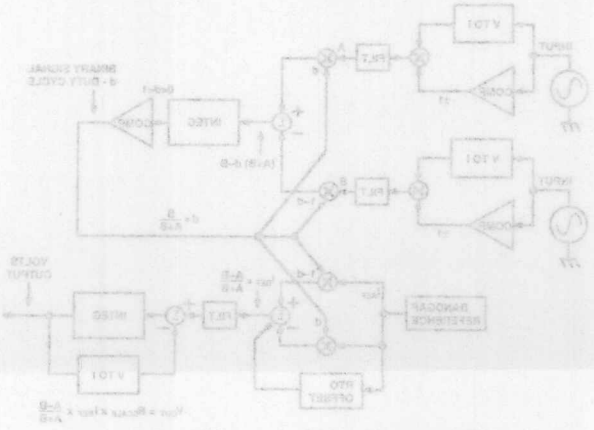
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ . . . . . 36 V
Storage Temperature Range
R Package . . . . . −65°C to +150°C
D Package . . . . . −65°C to +150°C
Operating Temperature Range
AD598JR . . . . . 0 to +70°C
AD598AD . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 60 Seconds) . . . . +300°C
Power Dissipation Up to +65°C . . . . . 1.2 W
Derides Above +65°C . . . . . 12 mW/°C

CONNECTION DIAGRAM

Plastic SOIC (R) Package
and
Side Brazed Ceramic DIP (D) Package





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THEORY OF OPERATION

A block diagram of the AD598 along with an LVDT (Linear Variable Differential Transformer) connected to its input is shown in Figure 5. The LVDT is an electromechanical transducer whose input is the mechanical displacement of a core and whose output is a pair of ac voltages proportional to core position. The transducer consists of a primary winding energized by an external sine wave reference source, two secondary windings connected in series, and the moveable core to couple flux between the primary and secondary windings.

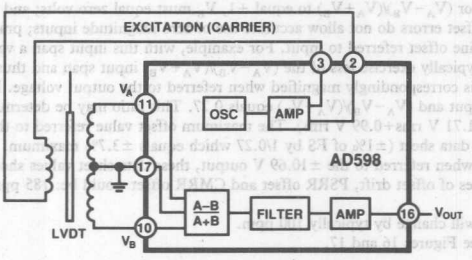


Figure 5. AD598 Functional Block Diagram

The AD598 energizes the LVDT primary, senses the LVDT secondary output voltages and produces a dc output voltage proportional to core position. The AD598 consists of a sine wave oscillator and power amplifier to drive the primary, a decoder which determines the ratio of the difference between the LVDT secondary voltages divided by their sum, a filter and an output amplifier.

The oscillator comprises a multivibrator which produces a triwave output. The triwave drives a sine shaper, which produces a low distortion sine wave whose frequency is determined by a single capacitor. Output frequency can range from 20 Hz to 20 kHz and amplitude from 2 V rms to 24 V rms. Total harmonic distortion is typically −50 dB.

The output from the LVDT secondaries consists of a pair of sine waves whose amplitude difference, (V_A-V_B), is proportional to core position. Previous LVDT conditioners synchronously detect this amplitude difference and convert its absolute value to a voltage proportional to position. This technique uses the primary excitation voltage as a phase reference to determine the polarity of the output voltage. There are a number of problems associated with this technique such as (1) producing a constant amplitude, constant frequency excitation signal, (2) compensating for LVDT primary to secondary phase shifts, and (3) compensating for these shifts as a function of temperature and frequency.

The AD598 eliminates all of these problems. The AD598 does not require a constant amplitude because it works on the ratio of the difference and sum of the LVDT output signals. A constant frequency signal is not necessary because the inputs are rectified and only the sine wave carrier magnitude is processed. There is no sensitivity to phase shift between the primary excitation and the LVDT outputs because synchronous detection is not employed. The ratiometric principle upon which the AD598 operates requires that the sum of the LVDT secondary voltages remains constant with LVDT stroke length. Although LVDT manufacturers generally do not specify the relationship between V_A+V_B and stroke length, it is recognized that some LVDTs do not meet this requirement. In these cases a nonlinearity will result. However, the majority of available LVDTs do in fact meet these requirements.

The AD598 utilizes a special decoder circuit. Referring to the block diagram and Figure 6 below, an implicit analog computing loop is employed. After rectification, the A and B signals are multiplied by complementary duty cycle signals, d and (1–d) respectively. The difference of these processed signals is integrated and sampled by a comparator. It is the output of this comparator that defines the original duty cycle, d, which is fed back to the multipliers.

As shown in Figure 2, the input to the integrator is [(A+B)d]-B. Since the integrator input is forced to 0, the duty cycle $d = B/(A+B)$.

The output comparator which produces $d = B/(A+B)$ also controls an output amplifier driven by a reference current. Duty cycle signals d and (1−d) perform separate modulations on the reference current as shown in Figure 6, which are summed. The summed current, which is the output current, is $I_{REF} \times (1-2d)$. Since $d = B/(A+B)$, by substitution the output current equals $I_{REF} \times (A-B)/(A+B)$. This output current is then filtered and converted to a voltage since it is forced to flow through the scaling resistor R2 such that:

$$V_{OUT} = I_{REF} \times (A-B)/(A+B) \times R2$$

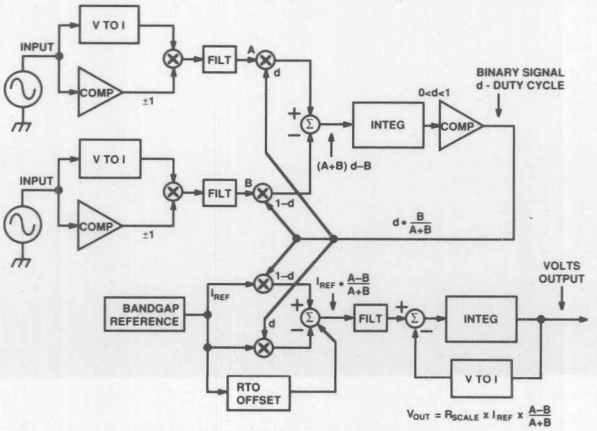


Figure 6. Block Diagram of Decoder

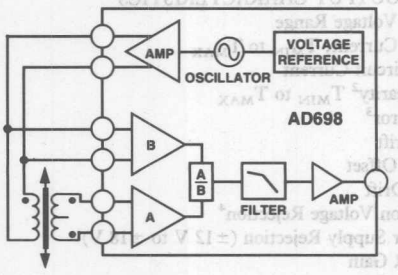
Universal LVDT Signal Conditioner

AD698

FEATURES

- Single Chip Solution, Contains Internal Oscillator and Voltage Reference
- No Adjustments Required
- Interfaces to Half-Bridge LVDT, 4-Wire LVDT
- DC Output Proportional to Position
- 20 Hz to 20 kHz Frequency Range
- Unipolar or Bipolar Output
- Will Also Implement AC Bridge
- Outstanding Performance
  - Linearity: 0.05%
  - Output Voltage: ±11 V
  - Gain Drift: 20 ppm/°C (typ)
  - Offset Drift: 5 ppm/°C (typ)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD698 is a complete, monolithic Linear Variable Differential Transformer (LVDT) signal conditioning subsystem. It is used in conjunction with LVDTs to convert transducer mechanical position to a unipolar or bipolar dc voltage with a high degree of accuracy and repeatability. All circuit functions are included on the chip. With the addition of a few external passive components to set frequency and gain, the AD698 converts the raw LVDT output to a scaled dc signal. The device will operate with half-bridge LVDTs, LVDTs connected in the series opposed configuration, (4-wire), RVDTs.

The AD698 contains a low distortion sine wave oscillator to drive the LVDT primary. Two synchronous demodulation channels of the AD698 are used to detect primary and secondary amplitude. The part divides the output of the secondary by the amplitude of the primary and multiplies by a scale factor. This eliminates scale factor errors due to drift in the amplitude of the primary drive, improving temperature performance and stability.

The AD698 uses a unique ratiometric architecture to eliminate several of the disadvantages associated with traditional approaches to LVDT interfacing. The benefits of this new circuit are: no adjustments are necessary; temperature stability is improved; and transducer interchangeability is improved.

The AD698 is available in two performance grades:

Grade	Temperature Range	Package
AD698AP	−40°C to +85°C	28-Pin PLCC
AD698SQ	−55°C to +125°C	24-Pin Cerdip

PRODUCT HIGHLIGHTS

1. The AD698 offers a single chip solution to LVDT signal conditioning problems. All active circuits are on the monolithic chip with only passive components required to complete the conversion from mechanical position to dc voltage.
2. The AD698 can be used with many different types of position sensors. The circuit is optimized for use with any LVDT, including half-bridge and series opposed, (4 wire) configurations. The AD698 accommodates a wide range of input and output voltages and frequencies.
3. The 20 Hz to 20 kHz excitation frequency is determined by a single external capacitor. The AD698 provides up to 24 volts rms to differentially drive the LVDT primary, and the AD698 meets its specifications with secondary input levels as low as 100 millivolts rms.
4. Change in oscillator amplitude with temperature will not affect overall circuit performance. The AD698 computes the ratio of the secondary voltage to the primary voltage to determine position and direction. No adjustments are required.
5. Multiple LVDTs can be driven by a single AD698 either in series or parallel as long as power dissipation limits are not exceeded. The excitation output is thermally protected.
6. The AD698 may be used as a loop integrator in the design of simple electromechanical servo loops.
7. The sum of the secondaries' voltages do not need to be constant.

TRANSFER FUNCTION[1]	$V_{OUT} = \frac{A}{B} \times 500\ \mu A \times R2$						V
OVERALL ERROR T_{MIN} to T_{MAX}		0.4	1.65		0.4	1.65	% of FS
SIGNAL OUTPUT CHARACTERISTICS							
Output Voltage Range	±11			±11			V
Output Current, T_{MIN} to T_{MAX}		11			11		mA
Short Circuit Current		20			20		mA
Nonlinearity[2] T_{MIN} to T_{MAX}		75	±500		75	±500	ppm of FS
Gain Error[3]		0.1	±1.0		0.1	±1.0	% of FS
Gain Drift		20	±100		20	±100	ppm/°C of FS
Output Offset		0.02	±1		0.02	±1	% of FS
Offset Drift		5	±25		5	±25	ppm/°C of FS
Excitation Voltage Rejection[4]		100			100		ppm/dB
Power Supply Rejection (±12 V to ±18 V)							
PSRR Gain		50	300		50	300	ppm/V
PSRR Offset		15	100		15	100	ppm/V
Common-Mode Rejection (±3 V)							
CMRR Gain		25	100		25	100	ppm/V
CMRR Offset		2	100		2	100	ppm/V
Output Ripple[5]		4			4		mV rms
EXCITATION OUTPUT CHARACTERISTICS (@ 2.5 kHz)							
Excitation Voltage Range	2.1		24	2.1		24	V rms
Excitation Voltage (Resistors Are 1% Absolute Values)							
(R1 = Open)[6]	1.2		2.15	1.2		2.15	V rms
(R1 = 12.7 kΩ)	2.6		4.35	2.6		4.35	V rms
(R1 = 487 Ω)	14		21.2	14		21.2	V rms
Excitation Voltage TC[7]		100			100		ppm/°C
Output Current	30	50		30	50		mA rms
T_{MIN} to T_{MAX}		40			40		mA rms
Short Circuit Current		60			60		mA
DC Offset Voltage (Differential, R1 = 12.7 kΩ)							
T_{MIN} to T_{MAX}		30	±100		30	±100	mV
Frequency	20		20 k	20		20 k	Hz
Frequency TC		200			200		ppm/°C
Total Harmonic Distortion		−50			−50		dB
SIGNAL INPUT CHARACTERISTICS							
A/B Ratio Usable Full-Scale Range	0.1		0.9	0.1		0.9	
Signal Voltage B Channel	0.1		3.5	0.1		3.5	V rms
Signal Voltage A Channel	0.0		3.5	0.0		3.5	V rms
Input Impedance		200			200		kΩ
Input Bias Current (BIN, AIN)		1	5		1	5	μA
Signal Reference Bias Current		2	10		2	10	μA
Excitation Frequency	0		20k	0		20k	Hz
POWER SUPPLY REQUIREMENTS							
Operating Range	13		36	13		36	V
Dual Supply Operation (±10 V Output)	±13			±13			V
Single Supply Operation							
0 V to +10 V Output	17.5			17.5			V
0 V to −10 V Output	17.5			17.5			V
Current (No Load at Signal and Excitation Outputs)		12	15		12	15	mA
T_{MIN} to T_{MAX}			18			18	mA
OPERATING TEMPERATURE RANGE	−55		+125	−40		+85	°C

tor, i.e., multiply $V_{OUT} \times +1$ for $A_{COMP+} > A_{COMP-}$, and $V_{OUT} \times -1$ for $A_{COMP-} > A_{COMP+}$.

[2]Nonlinearity of the AD698 only in units of ppm of full scale. Nonlinearity is defined as the maximum measured deviation of the AD698 output voltage from a straight line. The straight line is determined by connecting the maximum produced full-scale negative voltage with the maximum produced full-scale positive voltage.

[3]See Transfer Function.

[4]For example, if the excitation to the primary changes by 1 dB, the gain of the system will change by typically 100 ppm.

[5]Output ripple is a function of the AD698 bandwidth determined by C1 and C2. A 1000 pF capacitor should be in parallel with R2 to reduce the output ripple. See Figures 7 and 13.

[6]R1 is shown in Figures 7 and 13.

[7]Excitation voltage drift is not an important specification because of the ratiometric operation of the AD698.

[8]From T_{MIN} to T_{MAX} the overall error due to the AD698 alone is determined by combining gain error, gain drift and offset drift. For example, the typical overall error for the AD698AP from T_{MIN} to T_{MAX} is calculated as follows: Overall Error = Gain Error at 25°C (±0.2% Full Scale) + Gain Drift from −40°C to 25°C (20 ppm/°C × 65°C) + Offset Drift from −40°C to 25°C (5 ppm/°C × 65°C) = ±0.36% of full scale. Note that 1000 ppm of full scale equals 0.1% of full scale.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tested are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage ($+V_S$ to $-V_S$) . . . . . 36 V

Storage Temperature Range

P Package . . . . . −65°C to +150°C

Q Package . . . . . −65°C to +150°C

Operating Temperature Range

AD698SQ . . . . . −55°C to +125°C

AD698AP . . . . . −40°C to +85°C

Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

Power Dissipation Derates above +65°C

P Package . . . . . 12 mW/°C

Q Package . . . . . 12 mW/°C

THERMAL CHARACTERISTICS

	θ_{JC}	θ_{JA}
P Package	30°C/W	60°C/W
Q Package	26°C/W	62°C/W

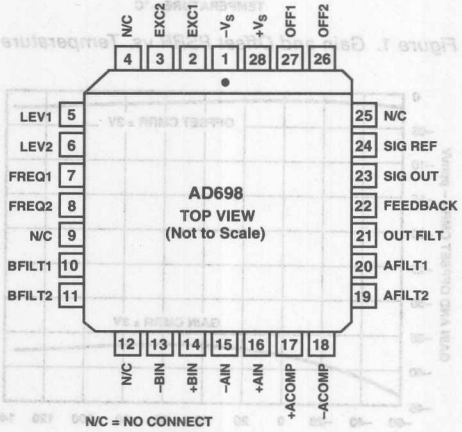
ORDERING GUIDE

Model	Package Description	Package Option*
AD698AP	28-Pin PLCC	P-28A
AD698SQ	24-Pin Double Cerdip	Q-24A

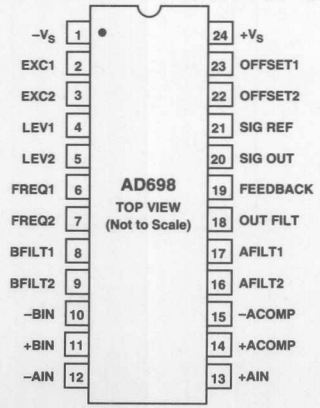
*For outline information see Package Information section.

CONNECTION DIAGRAMS

28-Pin PLCC



24-Pin Cerdip



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CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD698 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Characteristics (at +25°C and V_S = ±15 V unless otherwise noted)

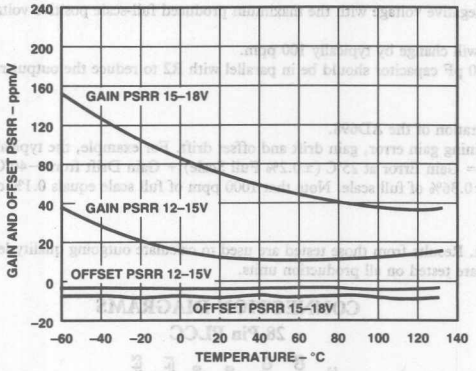

Figure 1. Gain and Offset PSRR vs. Temperature

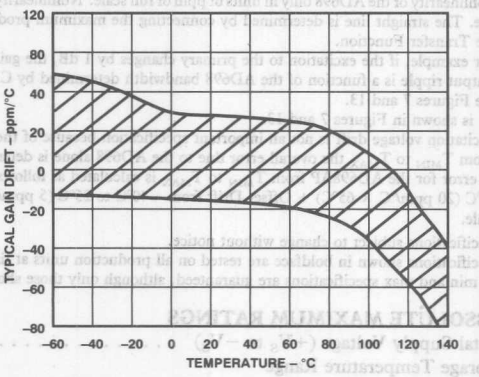

Figure 3. Typical Gain Drift vs. Temperature

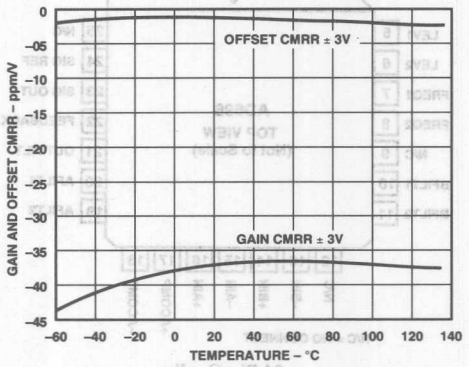

Figure 2. Gain and Offset CMRR vs. Temperature

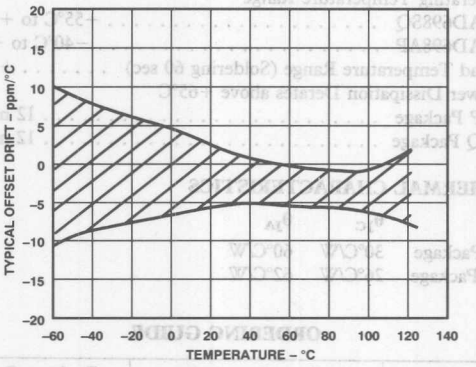

Figure 4. Typical Offset Drift vs. Temperature

THEORY OF OPERATION

A block diagram of the AD698 along with an LVDT (linear variable differential transformer) connected to its input is shown in Figure 5 below. The LVDT is an electromechanical transducer—its input is the mechanical displacement of a core, and its output is an ac voltage proportional to core position. Two popular types of LVDTs are the half-bridge type and the series opposed or four-wire LVDT. In both types the moveable core couples flux between the windings. The series-opposed connected LVDT transducer consists of a primary winding energized by an external sine wave reference source and two secondary windings connected in the series opposed configuration. The output voltage across the series secondary increases as the core is moved from the center. The direction of movement is detected by measuring the phase of the output. Half-bridge LVDTs have a single coil with a center tap and work like an autotransformer. The excitation voltage is applied across the coil; the voltage at the center tap is proportional to position. The device behaves very similar to a resistive voltage divider.

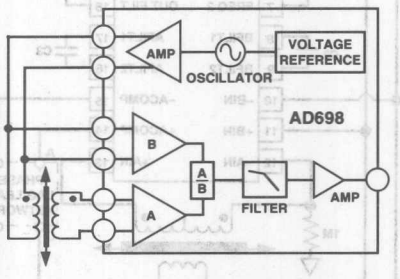

Figure 5. Functional Block Diagram

The AD698 energizes the LVDT coil, senses the LVDT output voltages and produces a dc output voltage proportional to core position. The AD698 has a sine wave oscillator and power amplifier to drive the LVDT. Two synchronous demodulation stages are available for decoding the primary and secondary voltages. A decoder determines the ratio of the output signal voltage to the input drive voltage, (A/B). A filter stage and output amplifier are used to scale the resulting output.

The oscillator comprises a multivibrator which produces a triwave output. The triwave drives a sine shaper which produces a low distortion sine wave. Frequency and amplitude are determined by a single resistor and capacitor. Output frequency can range from 20 Hz to 20 kHz and amplitude from 2 V to 24 V rms. Total harmonic distortion is typically −50 dB.

The AD698 decodes LVDTs by synchronously demodulating the amplitude modulated input (secondaries), A, and a fixed input reference (primary or sum of secondaries or fixed input), B. A common problem with earlier solutions was that any drift in the amplitude of the drive oscillator corresponds directly to a gain error in the output. The AD698, eliminates these errors by calculating the ratio of the LVDT output to its input excitation in order to cancel out any drift effects. This device differs from the AD598 LVDT signal conditioner in that it implements a different circuit transfer function and does not require the sum of the LVDT secondaries (A + B) to be constant with stroke length.

The AD698 block diagram is shown below. The inputs consist of two independent synchronous demodulation channels. The B channel is designed to monitor the drive excitation to the LVDT. The full wave rectified output is filtered by C2 and sent to the computational circuit. Channel A is identical except that the comparator is pinned out separately. Since the A channel may reach 0 V output at LVDT null, the A channel demodulator is usually triggered by the primary voltage, (B Channel). In addition, a phase compensation network may be required to add a phase lead or lag to the A Channel to compensate for the LVDT primary to secondary phase shift. For half-bridge circuits the phase shift is noncritical, and the A channel voltage is large enough to trigger the demodulator.

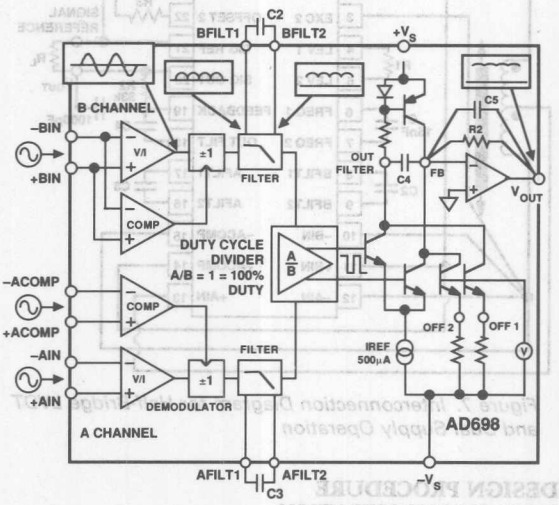

Figure 6. AD698 Block Diagram

Once both channels are demodulated and filtered a division circuit, implemented with a duty cycle multiplier, is used to calculate the ratio A/B. The output of the divider is a duty cycle. When A/B is equal to 1, the duty cycle will be equal to 100%. (This signal can be used as is if a pulse width modulated output is required.) The duty cycle drives a circuit that modulates and filters a reference current proportional to the duty cycle. The output amplifier scales the 500 μA reference current converting it to a voltage. The output transfer function is thus,

$$V_{OUT} = I_{REF} \times A/B \times R2, \text{ where } I_{REF} = 500\ \mu A$$

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CONNECTING THE AD698

The AD698 can easily be connected for dual or single supply operation as shown in Figures 7 and 13. The following general design procedures demonstrate how external component values are selected and can be used for any LVDT that meets AD698 input/output criteria. The connections for the A and B channels and the A channel comparators will depend on which transducer is used. In general follow the guidelines below.

Parameters set with external passive components include: excitation frequency and amplitude, AD698 input signal frequency, and the scale factor (V/inch). Additionally, there are optional features; offset null adjustment, filtering, and signal integration, which can be implemented by adding external components.

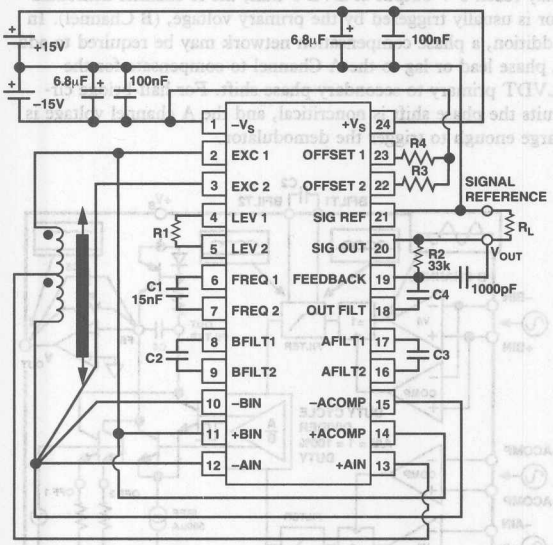

Figure 7. Interconnection Diagram for Half-Bridge LVDT and Dual Supply Operation

DESIGN PROCEDURE

DUAL SUPPLY OPERATION

Figure 7 shows the connection method for half-bridge LVDTs. Figure 8 demonstrates the connections for 3- and 4-wire LVDTs connected in the series opposed configuration. Both examples use dual ±15 volt power supplies.

A. Determine the Oscillator Frequency

Frequency is often determined by the required BW of the system. However, in some system the frequency is set to match the LVDT zero phase frequency as recommended by the manufacturer; in this case skip to Step 4.

1. Determine the mechanical bandwidth required for LVDT position measurement subsystem, $f_{SUBSYSTEM}$. For this example, assume $f_{SUBSYSTEM}$ = 250 Hz.
2. Select minimum LVDT excitation frequency approximately 10 × $f_{SUBSYSTEM}$. Therefore, let excitation frequency = 2.5 kHz.
3. Select a suitable LVDT that will operate with an excitation frequency of 2.5 kHz. The Schaevitz E100, for instance, will operate over a range of 50 Hz to 10 kHz and is an eligible candidate for this example.
4. Select excitation frequency determining component C1.

$$C1 = 35\ \mu F\ Hz/f_{EXCITATION}$$

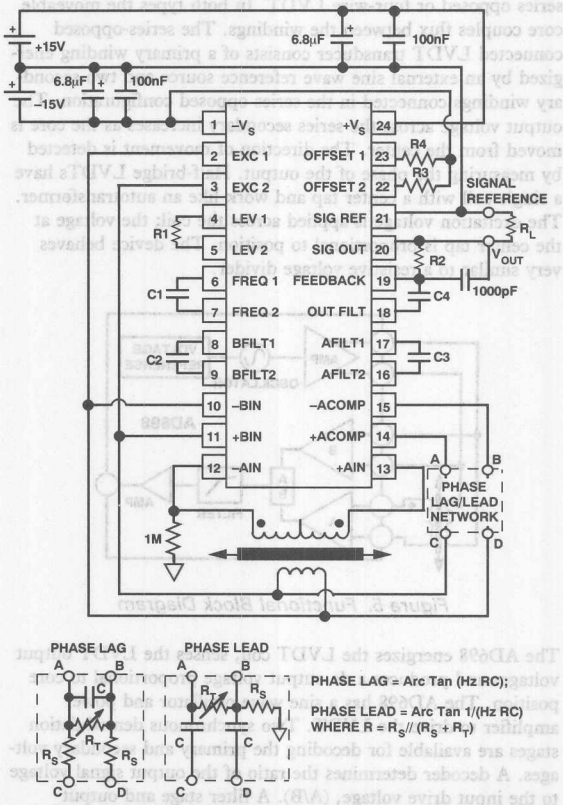

Figure 8. AD698 Interconnection Diagram for Series Opposed LVDT and Dual Supply Operation

B. Determine the Oscillator Amplitude

Amplitude is set such that the primary signal is in the 1.0 V to 3.5 V rms range and the secondary signal is in the 0.25 V to 3.5 V rms range when the LVDT is at its mechanical full-scale position. This optimizes linearity and minimizes noise susceptibility. Since the part is ratiometric, the exact value of the excitation is relatively unimportant.

5. Determine optimum LVDT excitation voltage, V_{EXC}. For a 4-wire LVDT determine the voltage transformation ratio, VTR, of the LVDT at its mechanical full scale. VTR = LVDT sensitivity × Maximum Stroke Length from null.

   LVDT sensitivity is listed in the LVDT manufacturer's catalog and has units of volts output per volts input per inch displacement. The E100 has a sensitivity of 2.4 mV/V/mil. In the event that LVDT sensitivity is not given by the manufacturer, it can be computed. See section on determining LVDT sensitivity.

Multiply the primary excitation voltage by the VTR to get the expected secondary voltage at mechanical full scale. For example, for an LVDT with a sensitivity of 2.4 mV/V/mil and a full scale of ±0.1 inch, the VTR = 0.0024 V/V/Mil × 100 mil = 0.24. Assuming the maximum excitation of 3.5 V rms, the maximum secondary voltage will be 3.5 V rms × 0.24 = 0.84 V rms, which is in the acceptable range.

Conversely the VTR may be measured explicitly. With the LVDT energized at its typical drive level V_{PRI}, as indicated by the manufacturer. Set the core displacement to its mechanical full-scale position and measure the output V_{SEC} of the secondary. Compute the LVDT voltage transformation ratio, VTR. VTR = V_{SEC}/V_{PRI}. For the E100, V_{SEC} = 0.72 V for V_{PRI} = 3 V. VTR = 0.24.

For situations where LVDT sensitivity is low, or the mechanical FS is a small fraction of the total stroke length an input excitation of more than 3.5 V rms may be needed. In this case a voltage divider network may be placed across the LVDT primary to provide smaller voltage for the +BIN and −BIN input. If, for example, a network was added to divide the B Channel input by 1/2 then the VTR should also be reduced by 1/2 for the purpose of component selection.

Check the power supply voltages by verifying that the peak values of V_A and V_B are at least 2.5 volts less than the voltages at $+V_S$ and $-V_S$.

6. Referring to Figure 9, for V_S = ±15 V, select the value of the amplitude determining component R1 as shown by the curve in Figure 9.

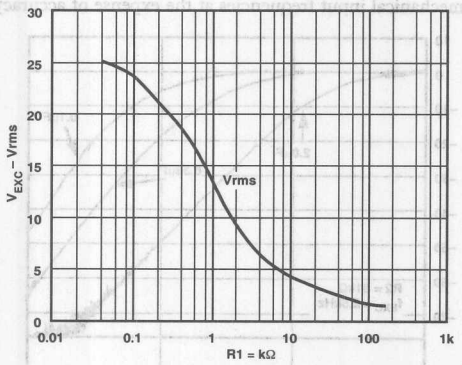

Figure 9. Excitation Voltage V_{EXC} vs. R1

C. Choose the Filter Capacitors: C2, C3, C4

7. C2, C3 and C4 are a function of the desired bandwidth of the AD698 position measurement subsystem. They should be nominally equal values.

$$C2 = C3 = C4 = 10^{-4}\ Farad\ Hz/f_{SUBSYSTEM}\ (Hz)$$

If the desired system bandwidth is 250 Hz, then

$$C2 = C3 = C4 = 10^{-4}\ Farad\ Hz/250\ Hz = 0.4\ \mu F$$

See Figures 14, 15 and 16 for more information about AD698 bandwidth and phase characterization.

D. Set the Full-Scale Output Voltage

8. Compute R2, which sets the AD698 gain or full-scale output range, several pieces of information are needed:

a. LVDT sensitivity, S

b. Full-scale core displacement from null, d

S × d = VTR and also equals the ratio A/B at mechanical full scale. The VTR should be converted to units of V/V.

For a full-scale displacement of d inches, voltage out of the AD698 is computed as

$$V_{OUT} = S \times d \times 500\ \mu A \times R2.$$

V_{OUT} is measured with respect to the signal reference, Pin 17 shown in Figure 7.

Solving for R2,

$$R2 = \frac{V_{OUT}}{S \times d \times 500\ \mu A} \quad (1)$$

For V_{OUT} = ±10 V full-scale range, (20 V span) and d = ±0.1 inch full-scale displacement, (0.2 inch span)

$$R2 = \frac{20\ V}{2.4 \times 0.2 \times 500\ \mu A} = 83.3\ k\Omega$$

V_{OUT} as a function of displacement for the above example is shown in Figure 10.

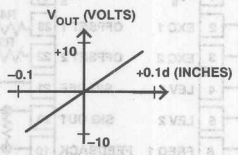

Figure 10. V_{OUT} (±10 V Full Scale) vs. Core Displacement (±0.1 Inch)

E. Optional Offset of Output Voltage Swing

9. Selections of R3 and R4 permit a positive or negative output voltage offset adjustment.

$$V_{OS} = 1.2\ V \times R2 \times \left(\frac{1}{R3 + 2\ k\Omega} - \frac{1}{R4 + 2\ k\Omega}\right) \quad (2)$$

For no offset adjustment R3 and R4 should be open circuit.

To design a circuit producing a 0 V to +10 V output for a displacement of ±0.1 inch, set V_{OUT} to +10 V, d = 0.2 inch and solve Equation (1) for R2.

$$R2 = 37.6\ k\Omega$$

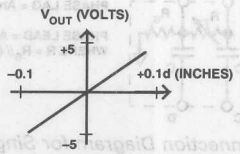

Figure 11. V_{OUT} (±5 V Full Scale) vs. Core Displacement (±0.1 Inch)

This will produce a response shown in Figure 11.

In Equation (2) set V_{OS} = 5 V and solve for R3 and R4. Since a positive offset is desired, let R4 be open circuit. Rearranging Equation (2) and solving for R3

$$R3 = \frac{1.2 \times R2}{V_{OS}} - 2\ k\Omega = 4.02\ k\Omega$$

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Figure 12 shows the desired response.

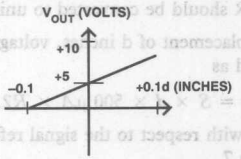

Figure 12. V_{OUT} (0 V–10 V Full Scale) vs. Displacement (±0.1 Inch)

DESIGN PROCEDURE
SINGLE SUPPLY OPERATION

Figure 13 shows the single supply connection method.

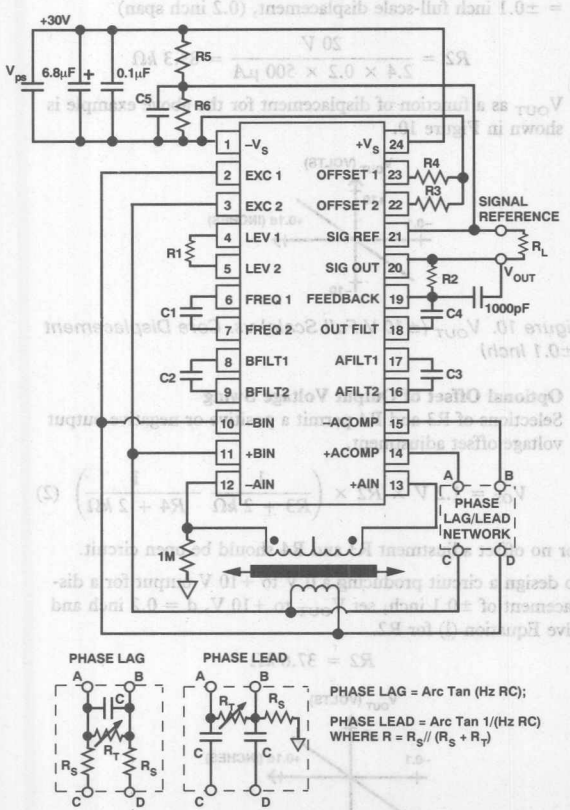

Figure 13. Interconnection Diagram for Single Supply Operation

For single supply operation, repeat Steps 1 through 10 of the design procedure for dual supply operation. R5, R6 and C5 are additional component values to be determined. V_{OUT} is measured with respect to SIGNAL REFERENCE.

10. Compute a maximum value of R5 and R6 based upon the relationship

$$R5 \pm R6 \leq V_{PS}/100\ \mu A$$

$$2 + 10\ k\Omega \left(\frac{1.2\ V}{R4 + 2\ k\Omega} + 250\ \mu A + \frac{V_{OUT}}{4 \times R2} \right) Volts$$

Therefore

$$R5 \geq \frac{2 + 10\ k\Omega \left(\frac{1.2\ V}{R4 + 2\ k\Omega} + 250\ \mu A + \frac{V_{OUT}}{4 \times R2} \right)}{100\ \mu A} Ohms$$

Based upon the constraints of R5 + R6 (Step 11) and R5 (Step 12), select an interim value of R6.

12. Load current through R_L returns to the junction of R5 and R6, and flows back to V_{PS}. Under maximum load conditions, make sure the voltage drop across R5 is met as defined in Step 11.

    As a final check on the power supply voltages, verify that the peak values of V_A and V_B are at least 2.5 volts less than the voltages at $+V_S$ and $-V_S$.

13. C5 is a bypass capacitor in the range of 0.1 μF to 1μF.

Gain Phase Characteristics

To use an LVDT in a closed loop mechanical servo application, it is necessary to know the dynamic characteristics of the transducer and interface elements. The transducer itself is very quick to respond once the core is moved. The dynamics arise primarily from the interface electronics. Figures 14, 15 and 16 show the frequency response of the AD698 LVDT Signal Conditioner. Note that Figures 15 and 16 are basically the same; the difference is frequency range covered. Figure 15 shows a wider range of mechanical input frequencies at the expense of accuracy.

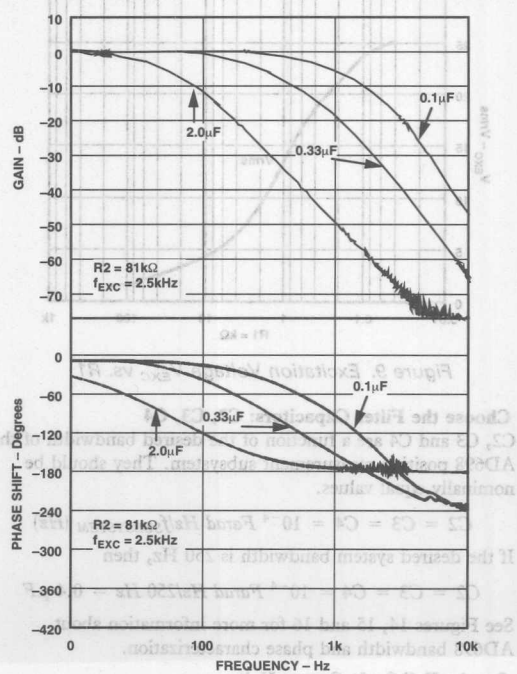

Figure 14. Gain and Phase Characteristics vs. Frequency (0 kHz–10 kHz)

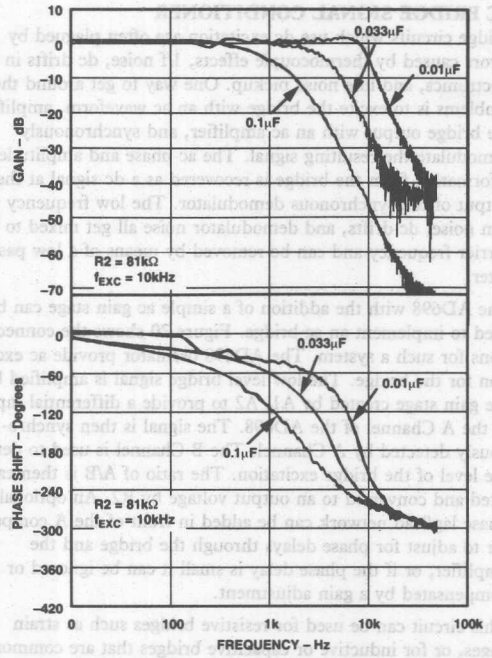

Figure 15. Gain and Phase Characteristics vs. Frequency (0 kHz–50 kHz)

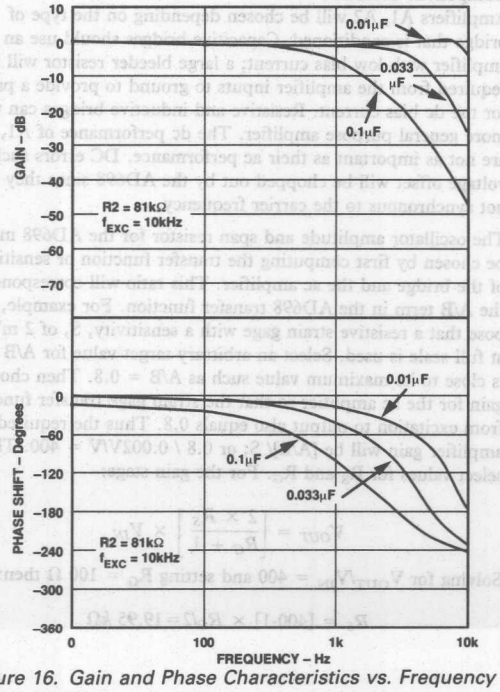

Figure 16. Gain and Phase Characteristics vs. Frequency (0 kHz–10 kHz)

Figure 16 shows a more limited frequency range with enhanced accuracy. The figures are transfer functions with the input to be considered as a sinusoidally varying mechanical position and the output as the voltage from the AD698; the units of the transfer function are volts per inch. The value of C2, C3, and C4, from Figure 7, are all equal and designated as a parameter in the figures. The response is approximately that of two real poles. However, there is appreciable excess phase at higher frequencies. An additional pole of filtering can be introduced with a shunt capacitor across R2, Figure 7; this will also increase phase lag.

When selecting values of C2, C3 and C4 to set the bandwidth of the system, a trade-off is involved. There is ripple on the "dc" position output voltage, and the magnitude is determined by the filter capacitors. Generally, smaller capacitors will give higher system bandwidth and larger ripple. Figures 17 and 18 show the magnitude of ripple as a function of C2, C3 and C4, again all equal in value. Note also a shunt capacitor across R2, Figure 7 is shown as a parameter. The value of R2 used was 81 kΩ with a Schaevitz E100 LVDT.

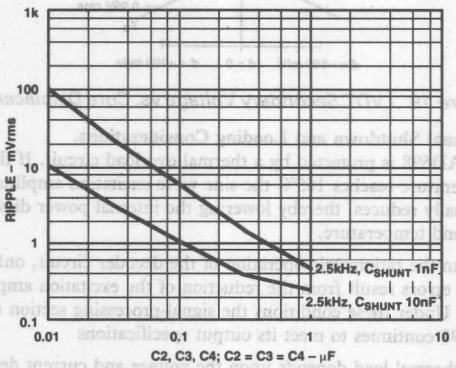

Figure 17. Output Voltage Ripple vs. Filter Capacitance

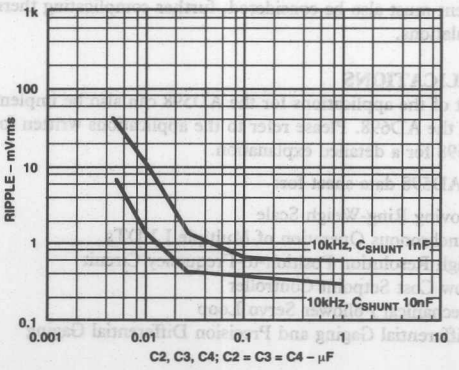

Figure 18. Output Voltage Ripple vs. Filter Capacitance

Determining LVDT Sensitivity
LVDT sensitivity can be determined by measuring the LVDT secondary voltages as a function of primary drive and core position, and performing a simple computation.

Energize the LVDT at its recommended primary drive level, V_{PRI} (3 V rms for the E100). Set the core displacement to its mechanical full-scale position and measure secondary voltages V_A and V_B.

$$Sensitivity = \frac{V_{SECONDARY}}{V_{PRI} \times d}$$

From Figure 19,

$$Sensitivity = \frac{0.84}{3.5\ V \times 100\ mils} = 2.4\ mV/V\ mil$$

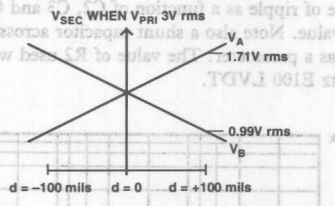

Figure 19. LVDT Secondary Voltage vs. Core Displacement

Thermal Shutdown and Loading Considerations.
The AD698 is protected by a thermal overload circuit. If the die temperature reaches 165°C the sine wave excitation amplitude gradually reduces, thereby lowering the internal power dissipation and temperature.

Due to the ratiometric operation of the decoder circuit, only small errors result from the reduction of the excitation amplitude. Under these conditions the signal-processing section of the AD698 continues to meet its output specifications

The thermal load depends upon the voltage and current delivered to the load as well as the power supply potentials. An LVDT Primary will present an inductive load to the sine wave excitation. The phase angle between the excitation voltage and current must also be considered, further complicating thermal calculations.

APPLICATIONS

Most of the applications for the AD598 can also be implemented with the AD698. Please refer to the applications written for the AD598 for a detailed explanation.

See AD598 data sheet for:

- Proving Ring-Weigh Scale
- Synchronous Operation of Multiple LVDTs
- High Resolution Position-to-Frequency Circuit
- Low Cost Setpoint Controller
- Mechanical Follower Servo Loop
- Differential Gaging and Precision Differential Gaging

AC BRIDGE SIGNAL CONDITIONER

Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, 1/f noise, dc drifts in the electronics, and line noise pickup. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low pass filter.

The AD698 with the addition of a simple ac gain stage can be used to implement an ac bridge. Figure 20 shows the connections for such a system. The AD698 oscillator provide ac excitation for the bridge. The low level bridge signal is amplified by the gain stage created by A1, A2 to provide a differential input to the A Channel of the AD698. The signal is then synchronously detected by A Channel. The B Channel is used to detect the level of the bridge excitation. The ratio of A/B is then calculated and converted to an output voltage by R2. An optional phase lag/lead network can be added in front of the A comparator to adjust for phase delays through the bridge and the amplifier, or if the phase delay is small it can be ignored or compensated by a gain adjustment.

This circuit can be used for resistive bridges such as strain gages, or for inductive or capacitive bridges that are commonly used for pressure or flow sensors. The low level signal outputs of these sensors are susceptible to noise and interference and are good candidates for ac signal processing techniques.

Component Selection
Amplifiers A1, A2 will be chosen depending on the type of bridge that is conditioned. Capacitive bridges should use an amplifier with low bias current; a large bleeder resistor will be required from the amplifier inputs to ground to provide a path for the dc bias current. Resistive and inductive bridges can use a more general purpose amplifier. The dc performance of A1, A2 are not as important as their ac performance. DC errors such as voltage offset will be chopped out by the AD698 since they are not synchronous to the carrier frequency.

The oscillator amplitude and span resistor for the AD698 may be chosen by first computing the transfer function or sensitivity of the bridge and the ac amplifier. This ratio will correspond to the A/B term in the AD698 transfer function. For example, suppose that a resistive strain gage with a sensitivity, S, of 2 mV/V at full scale is used. Select an arbitrary target value for A/B that is close to its maximum value such as A/B = 0.8. Then choose a gain for the ac amplifier so that the strain gage transfer function from excitation to output also equals 0.8. Thus the required amplifier gain will be [A/B]/ S; or 0.8 / 0.002V/V = 400. Then select values for R_S and R_G. For the gain stage:

$$V_{OUT} = \left[\frac{2 \times R_S}{R_G + 1}\right] \times V_{IN}$$

Solving for V_{OUT}/V_{IN} = 400 and setting R_G = 100 Ω then:

$$R_S = [400\text{-}1] \times R_G/2 = 19.95\ k\Omega$$

Choose an oscillator amplitude that is in the range of 1 V to 3.5 V rms. For an input excitation level of 3 V rms the output signal from the amplifier gain stage will be 3.5 V rms × 0.8 V or 2.4V rms, which is in the acceptable range.

Since A/B is known, the value of R2, the output FS resistor may be chosen by the formula:

$$V_{OUT} = A/B \times 500\ \mu A \times R2$$

For a 10 V output at FS, with an A/B of 0.8; solve for R2.

$$R2 = 10\ V/[0.8 \times 500\ \mu A] = 25.0\ k\Omega$$

This will result in a V_{OUT} of 10 V for a full-scale signal from the bridge. The other components, C1, C2, C3, C4 may be selected by following the guidelines on general device operation mentioned earlier.

If a gain trim is required, then a trim resistor can be used to adjust either R2 or R_G. Bridge offsets should be adjusted by a trim network on the OFFSET 1 and OFFSET 2 pins of the AD698.

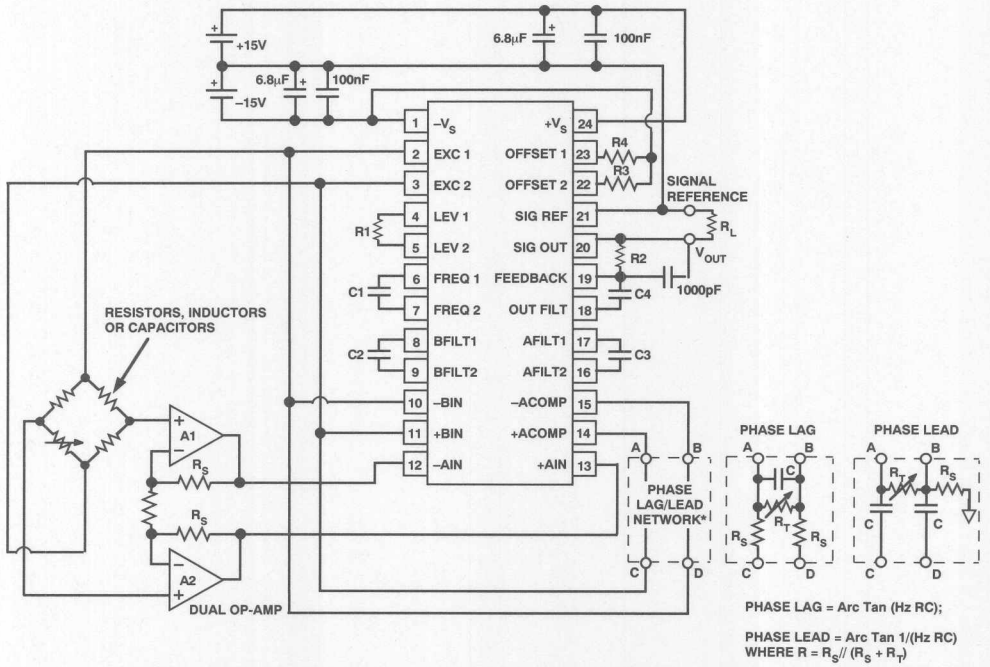

Figure 20. AD698 Interconnection Diagram for AC Bridge Applications

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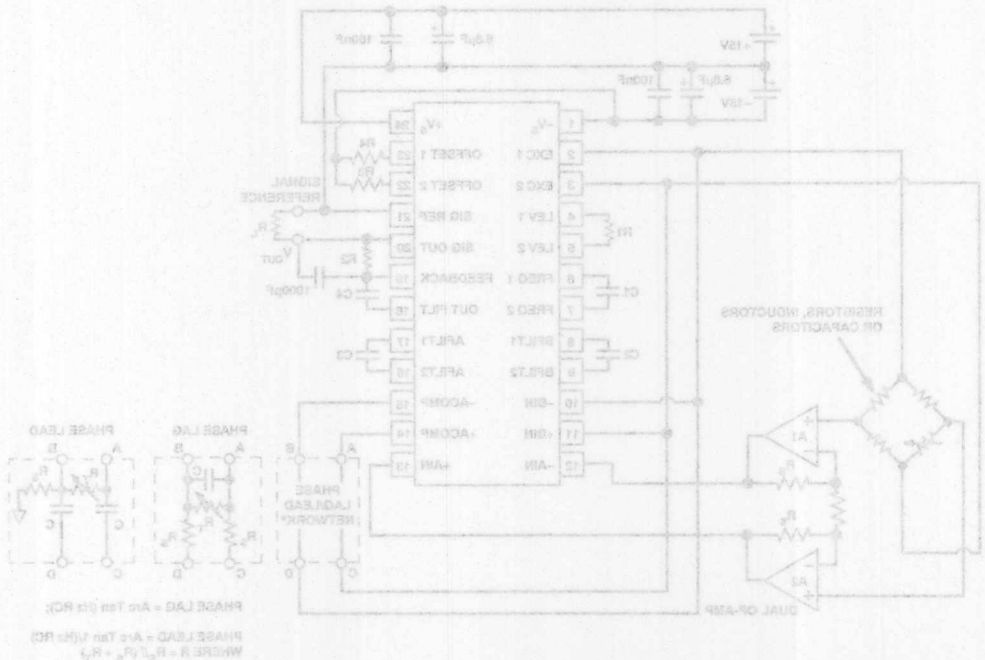

Multipliers and Dividers
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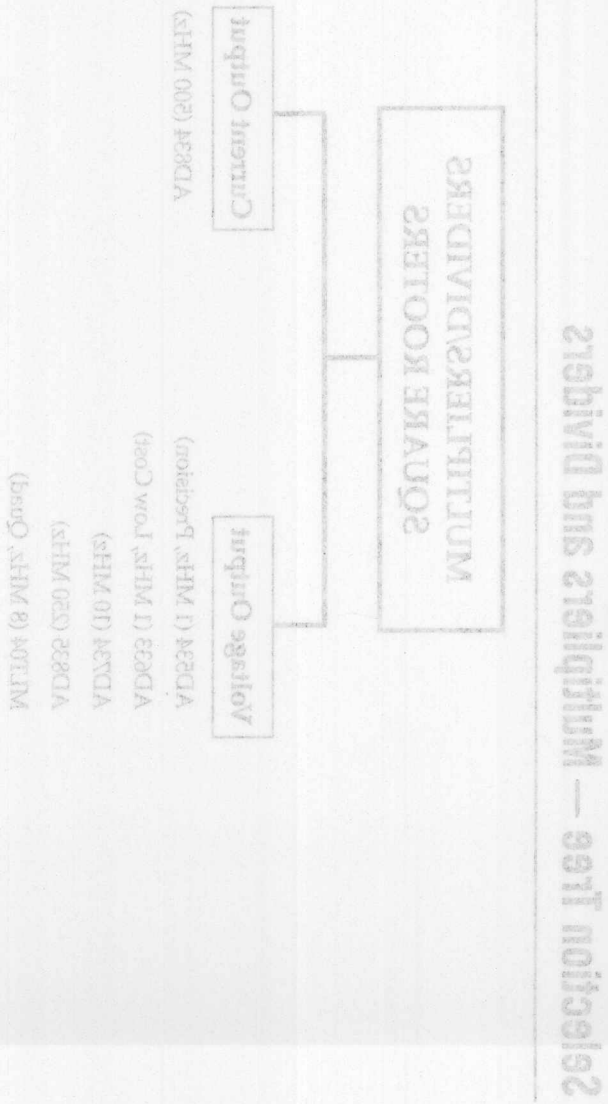

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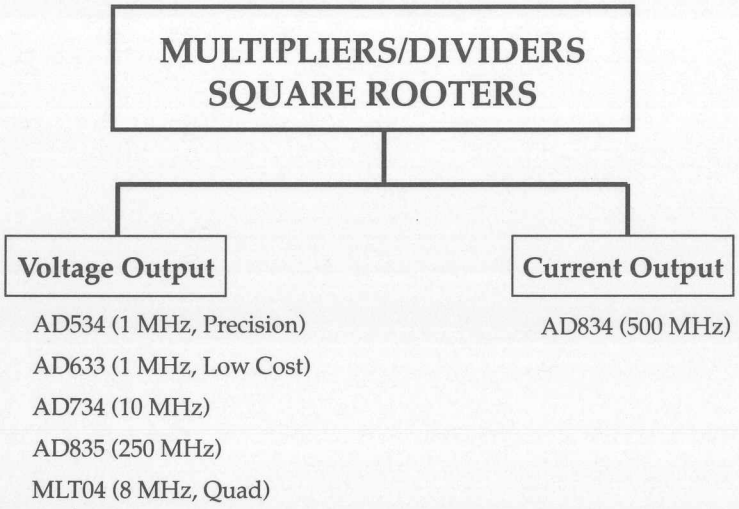
Selection Tree — Multipliers and Dividers



Selection Guides—Multipliers and Dividers

Multipliers/Dividers

Model	BW MHz typ[1]	Accuracy % FS max	Supply Voltage	Output Voltage Swing	Package Options[2]	Temp Ranges[3]	Comments	Page[4]
AD834	**>500**	**±2**	**+4 V to ±9 V**		**N, Q, R**	**C, I, M/S**	**Very High Speed, 4-Quadrant Mult/Div**	**17–14**
AD835	**150**		**±4.5 V to ±5.5 V**	**±2**	**N, Q, R**	**I, M**	**High Speed Voltage Output, 4-Quadrant Multiplier**	**17–17**
AD539	60	±1.5–2.5	±4.5 V to ±15 V		D, E, N	C, M/D	High Speed, 2-Channel, 2-Quadrant Mult/Div	SL 2–27
AD734	**10**	**±0.25–0.4**	**±8 V to ±16.5 V**	**±12 V min**	**N, Q**	**I, M/**	**Very High Accuracy Replacement for AD534**	**17–11**
AD633	**1**	**±2**	**±8 V to ±18 V**	**±11 V min**	**N, R**	**C**	**Low Cost, 4-Quadramt Multiplier**	**17–9**
AD532	1	±1–2	±10 V to ±22 V	±10 V min	D, E, H	C, M/J	Accurate 4-Quadrant Mult/Div	SL 2–9
AD632	1	±0.5–1	±8 V to ±22 V	±11 V min	D, H	I, M/S	High Accuracy Replacement for AD532	SL 2–43
AD534	**1**	**±0.25–1**	**±8 V to ±22 V**	**±11 V min**	**D, E, H**	**C, M/JS**	**High Accuracy, 4-Quadrant Mult/Div**	**17–5**
AD538	0.4	±0.5–1	±4.5 V to ±18 V	±11 V	D	I, M/	Simultaneous Mult/Div/Exponentiator	SL 2–23
MLT04	**8**	**±1**	**±4.75 to ±5.25**	**±3.0**	**N, R**	**I**	**Quad, High Speed Multiplier for CRT Correction**	**17–23**

Modulator/Demodulator

Model	Unity Gain BW MHz[1]	Gain	Slew Rate V/μs	Output Voltage Swing	Package Options[2]	Temp Ranges[3]	Comments	Page[4]
AD630	2	±1, ±2	45	±10 V min	D, E, N	C, I, M/D	Balanced Modulator/Demodulator with 10 V FS Output	SL 2–35

[1]Unity gain small signal bandwidth.
[2]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[3]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, J for JAN, D for SMD, and S for space level.
[4]SL = *Special Linear Reference Manual*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Selection Guides—Multipliers and Dividers

Multipliers/Dividers

Model	BW MHz (typ)[1]	Accuracy % FS max	Supply Voltage	Output Voltage Swing	Package Options[2]	Temp Ranges[3]	Comments	Page
AD834	>500	±2	+4 V to ±9 V		N, Q, R	C, I, M/[5]	Very High Speed, 4-Quadrant Mult/Div	17-
AD835	150		±4.5 V to ±5.5 V	±2	N, Q, R	I, M	High Speed Voltage Output, 4-Quadrant Multiplier	17-
AD539	60	±1.5–2.5	±4.5 V to ±15 V		D, E, N	C, M/[D]	High Speed, 2-Channel, 2-Quadrant Mult/Div	SL
AD734	10	±0.25–0.4	±8 V to ±16.5 V	±12 V min	N, Q	I, M/	Very High Accuracy Replacement for AD534	17-
AD633	1	±2	±8 V to ±18 V	±11 V min	N, R	C	Low Cost, 4-Quadrant Multiplier	17-
AD532	1	±1–2	±10 V to ±22 V	±10 V min	D, E, H	C, M/[1]	Accurate 4-Quadrant Mult/Div	SL
AD632	1	±0.5–1	±8 V to ±22 V	±11 V min	D, H	I, M/[5]	High Accuracy Replacement for AD532	SL
AD534	1	±0.25–1	±8 V to ±22 V	±11 V min	D, E, H	C, M/[5]	High Accuracy, 4-Quadrant Mult/Div	17-
AD538	0.4	±0.5–1	±4.5 V to ±18 V	±11 V	D	I, M/	Simultaneous Mult/Div/Exponentiator	SL
MLT704	8	±1	±4.75 to ±5.25	±3.0	N, R	I	Quad, High Speed Multiplier for CRT Correction	17-

Modulator/Demodulator

Model	Unity Gain BW MHz[1]	Gain	Slew Rate V/µs	Output Voltage Swing	Package Options[2]	Temp Ranges[3]	Comments	Page
AD630	2	±1, ±2	45	±10 V min	D, E, N	C, I, M/[D]	Balanced Modulator/Demodulator with 10 V PS Output	SL

[1]Unity gain small signal bandwidth.

[2]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Chip Carrier; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Quad Flatpack ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Monbermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.

[3]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, –40°C to +85°C (Some older products –25°C to +85°C); M = Military, –55°C to +125°C. If a device has military grade offerings temperature designator will be followed by / to indicate 883B. [1] for JAN, [D] for SMD, and [S] for space level.

[4]SL = Special Linear Reference Manual. All other entries refer to this volume.

Boldface Type: Data sheet information in this volume.

Internally Trimmed Precision IC Multiplier

AD534

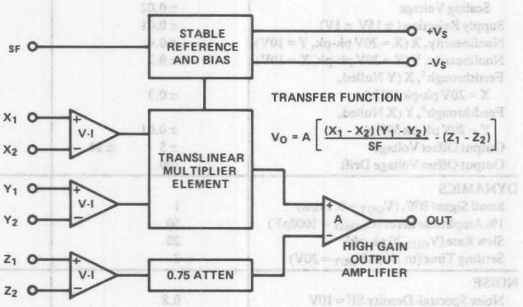
FEATURES

- Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
- All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10V]+Z_2$ Transfer Function
- Scale-Factor Adjustable to Provide up to X100 Gain
- Low Noise Design: 90μV rms, 10Hz–10kHz
- Low Cost, Monolithic Construction
- Excellent Long Term Stability

APPLICATIONS

- High Quality Analog Signal Processing
- Differential Ratio and Percentage Computations
- Algebraic and Trigonometric Function Synthesis
- Wideband, High-Crest rms-to-dc Conversion
- Accurate Voltage Controlled Oscillators and Filters
- Available in Chip Form

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier divider having accuracy specifications previously found only in expensive hybrid or modular products. A maximum multiplication error of ±0.25% is guaranteed for the AD534L without any external trimming. Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions of use. It is the first multiplier to offer fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00V; by means of an external resistor, this can be reduced to values as low as 3V.

The wide spectrum of applications and the availability of several grades commend this multiplier as the first choice for all new designs. The AD534J (±1% max error), AD534K (±0.5% max) and AD534L (±0.25% max) are specified for operation over the 0 to +70°C temperature range. The AD534S (±1% max) and AD534T (±0.5% max) are specified over the extended temperature range, −55°C to +125°C. All grades are available in hermetically sealed TO-100 metal cans and TO-116 ceramic DIP packages. AD534J, K, S and T chips are also available.

PROVIDES GAIN WITH LOW NOISE

The AD534 is the first general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD534 can be very effectively employed as a variable gain differential input amplifier with high common mode rejection. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. The utility of this feature is enhanced by the inherent low noise of the AD534: 90μV, rms (depending on the gain), a factor of 10 lower than previous monolithic multipliers. Drift and feedthrough are also substantially reduced over earlier designs.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility found in no other currently available multiplier. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD534—SPECIFICATIONS (T_A = +25°C, $\pm V_S$ = 15V, R≥2kΩ)

Model	AD534J			AD534K			AD534L			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] (−10V≤X, Y≤+10V)			**±1.0**			**±0.5**			**±0.25**	%
T_A = min to max		±1.5			±1.0			±0.5		%
Total Error vs Temperature		±0.022			±0.015			±0.008		%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1			±0.1		%
Temperature-Coefficient of Scaling Voltage		±0.02			±0.01			±0.005		%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	**±0.3**		±0.10	**±0.12**	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.2			±0.1	**±0.1**		±0.005	**±0.1**	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	**±0.3**		±0.05	**±0.12**	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	**±0.1**		±0.003	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±2	**±10**	mV
Output Offset Voltage Drift		200			100			100		μV/°C
DYNAMICS										
Small Signal BW, (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20			20		V/μs
Settling Time (to 1%; ΔV_{OUT} = 20V)		2			2			2		μs
NOISE										
Noise Spectral-Density SF = 10V		0.8			0.8			0.8		μV/√Hz
SF = 3V[4]		0.4			0.4			0.4		μV/√Hz
Wideband Noise f = 10Hz to 5MHz		1			1			1		mV/rms
f = 10Hz to 10kHz		90			90			90		μV/rms
OUTPUT										
Output Voltage Swing	**±11**			**±11**			**±11**			V
Output Impedance (f≤1kHz)		0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]										
Signal Voltage Range (Diff. or CM		±10			±10			±10		V
Operating Diff.)		±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			50		μV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±2	**±10**	mV
Offset Voltage Drift Z		200			100			100		μV/°C
CMRR	60	80		70	90		70	90		dB
Bias Current		0.8	2.0		0.8	2.0		0.8	2.0	μA
Offset Current		0.1			0.1			0.05	0.2	μA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10V, −10V≤Z≤+10V)		±0.75			±0.35			±0.2		%
(X = 1V, −1V≤Z≤+1V)		±2.0			±1.0			±0.8		%
(0.1V≤X≤10V, −10V≤Z≤10V)		±2.5			±1.0			±0.8		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1+X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$		
Total Error (−10V≤X≤10V)		±0.6			±0.3			±0.2		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function ($Z_1 \le Z_2$)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] (1V≤Z≤10V)		±1.0			±0.5			±0.25		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	±8		**±18**	±8		**±18**	±8		**±18**	V
Supply Current										
Quiescent		4	**6**		4	6		4	**6**	mA

NOTES

[1]Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3V.
[5]See functional block diagram for definition of sections.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD534S Min	AD534S Typ	AD534S Max	AD534T Min	AD534T Typ	AD534T Max	Units
MULTIPLIER PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] (−10V≤X, Y≤+10V)			±1.0			±0.5	%
T_A = min to max			±2.0			±1.0	%
Total Error vs Temperature			±0.02			±0.01	%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1		%
Temperature-Coefficient of Scaling Voltage		±0.02				±0.005	%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	±0.3	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.2			±0.1	±0.1	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	±0.3	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	±0.1	%
Output Offset Voltage		±5	±30		±2	±15	mV
Output Offset Voltage Drift			500			300	µV/°C
DYNAMICS							
Small Signal BW, (V_{OUT} = 0.1 rms)		1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2		µs
NOISE							
Noise Spectral-Density SF = 10V		0.8			0.8		$\mu V/\sqrt{Hz}$
SF = 3V[4]		0.4			0.4		$\mu V/\sqrt{Hz}$
Wideband Noise f = 10Hz to 5MHz		1.0			1.0		mV/rms
f = 10Hz to 10kHz		90			90		µV/rms
OUTPUT							
Output Voltage Swing	±11			±11			V
Output Impedance (f≤1kHz)		0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]							
Signal Voltage Range (Diff. or CM		±10			±10		V
Operating Diff.)		±12			±12		V
Offset Voltage X, Y		±5	±20		±2	±10	mV
Offset Voltage Drift X, Y		100			150		µV/°C
Offset Voltage Z		±5	±30		±2	±15	mV
Offset Voltage Drift Z			500			300	µV/°C
CMRR	60	80		70	90		dB
Bias Current		0.8	2.0		0.8	2.0	µA
Offset Current		0.1			0.1		µA
Differential Resistance		10			10		MΩ
DIVIDER PERFORMANCE							
Transfer Function ($X_1>X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10V, −10V≤Z≤+10V)		±0.75			±0.35		%
(X = 1V, −1V≤Z≤+1V)		±2.0			±1.0		%
(0.1V≤X≤10V, −10V≤Z≤10V)		±2.5			±1.0		%
SQUARE PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$		
Total Error (−10V≤X≤10V)		±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE							
Transfer Function (Z_1≤Z_2)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] (1V≤Z≤10V)		±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS							
Supply Voltage							
Rated Performance		±15			±15		V
Operating	±8		±22	±8		±22	V
Supply Current							
Quiescent		4	6		4	6	mA

NOTES
[1]Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3V.
[5]See functional block diagram for definition of sections.
Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

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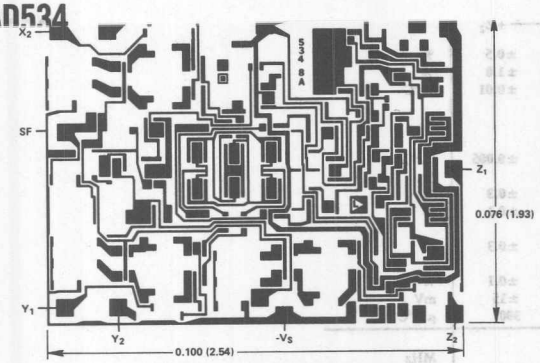


THE AD534 IS AVAILABLE IN LASER-TRIMMED CHIP FORM

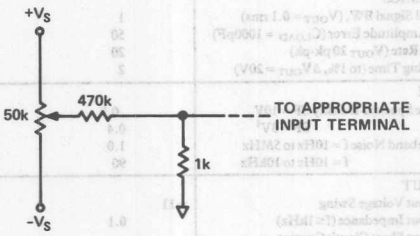
Internal Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinte	*
Input Voltages, $X_1\ X_2\ Y_1\ Y_2\ Z_1\ Z_2$	$\pm V_S$	*
Rated Operating Temperature Range	0 to +70°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature, 60s Soldering	+300°C	*
ESD Rating	1000V	

*Same as AD534J specs.

Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W for H-10A
θ_{JA} = 150°C/W for H-10A
θ_{JC} = 25°C/W for D-14 or E-20A
θ_{JA} = 95°C/W for D-14 or E-20A

OPTIONAL TRIMMING CONFIGURATION



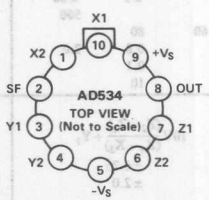
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD534JD	0°C to +70°C	Side Brazed DIP	D-14
AD534KD	0°C to +70°C	Side Brazed DIP	D-14
AD534LD	0°C to +70°C	Side Brazed DIP	D-14
AD534JH	0°C to +70°C	Header	H-10A
AD534KH	0°C to +70°C	Header	H-10A
AD534LH	0°C to +70°C	Header	H-10A
AD534J Chip	0°C to +70°C	Chip	
AD534K Chip	0°C to +70°C	Chip	
AD534SD	−55°C to +125°C	Side Brazed DIP	D-14
AD534SD/883B	−55°C to +125°C	Side Brazed DIP	D-14
AD534TD	−55°C to +125°C	Side Brazed DIP	D-14
AD534TD/883B	−55°C to +125°C	Side Brazed DIP	D-14
JM38510/13902BCA	−55°C to +125°C	Side Brazed DIP	D-14
JM38510/13901BCA	−55°C to +125°C	Side Brazed DIP	D-14
AD534SE	−55°C to +125°C	LCC	E-20A
AD534SE/883B	−55°C to +125°C	LCC	E-20A
AD534TE	−55°C to +125°C	LCC	E-20A
AD534TE/883B	−55°C to +125°C	LCC	E-20A
AD534SH	−55°C to +125°C	Header	H-10A
AD534SH/883B	−55°C to +125°C	Header	H-10A
AD534TH	−55°C to +125°C	Header	H-10A
AD534TH/883B	−55°C to +125°C	Header	H-10A
JM38510/13902BIA	−55°C to +125°C	Header	H-10A
JM38510/13901BIA	−55°C to +125°C	Header	H-10A
AD534S Chip	−55°C to +125°C	Chip	
AD534T Chip	−55°C to +125°C	Chip	

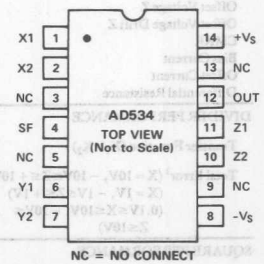
*For outline information see Package Information section.

PIN CONFIGURATIONS

TO-100 (H-10A) Package

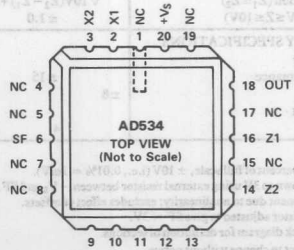


TO-116 (D-14) Package



NC = NO CONNECT

LCC (E-20A) Package



NC = NO CONNECT

ANALOG DEVICES

Low Cost Analog Multiplier

AD633

FEATURES
Four-Quadrant Multiplication
Low Cost 8-Pin Package
Complete—No External Components Required
Laser-Trimmed Accuracy and Stability
Total Error Within 2% of FS
Differential High Impedance X and Y Inputs
High Impedance Unity-Gain Summing Input
Laser-Trimmed 10 V Scaling Reference

APPLICATIONS
Multiplication, Division, Squaring
Modulation/Demodulation, Phase Detection
Voltage-Controlled Amplifiers/Attenuators/Filters

PRODUCT DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The AD633 is the first product to offer these features in modestly priced 8-pin plastic DIP and SOIC packages.

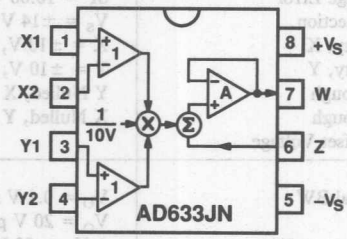
The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y-input is typically less than 0.1% and noise referred to the output is typically less than 100 μV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/μs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns.

The AD633's versatility is not compromised by its simplicity. The Z-input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications.

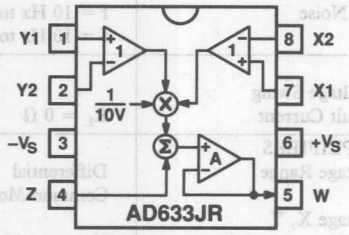
The AD633 is available in an 8-pin plastic mini-DIP package (N) and 8-pin SOIC (R) and is specified to operate over the 0°C to +70°C commercial temperature range.

CONNECTION DIAGRAMS

8-Pin Plastic DIP (N) Package



8-Pin Plastic SOIC (R) Package



$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z$$

PRODUCT HIGHLIGHTS

1. The AD633 is a complete four-quadrant multiplier offered in low cost 8-pin plastic packages. The result is a product that is cost effective and easy to apply.
2. No external components or expensive user calibration are required to apply the AD633.
3. Monolithic construction and laser calibration make the device stable and reliable.
4. High (10 MΩ) input resistances make signal source loading negligible.
5. Power supply voltages can range from ±8 V to ±18 V. The internal scaling voltage is generated by a stable Zener diode; multiplier accuracy is essentially supply insensitive.

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD633—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, $R_L \geq 2$ kΩ)

Model		AD633J			
TRANSFER FUNCTION		$W = \frac{(X_1-X_2)(Y_1-Y_2)}{10\,V} + Z$			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
MULTIPLIER PERFORMANCE					
Total Error	−10 V ≤ X, Y ≤ +10 V		±1	**±2**	% Full Scale
T_{min} to T_{max}			±3		% Full Scale
Scale Voltage Error	SF = 10.00 V Nominal		±0.25%		% Full Scale
Supply Rejection	V_S = ±14 V to ±16 V		±0.01		% Full Scale
Nonlinearity, X	X = ±10 V, Y = +10 V		±0.4	**±1**	% Full Scale
Nonlinearity, Y	Y = ±10 V, X = +10 V		±0.1	**±0.4**	% Full Scale
X Feedthrough	Y Nulled, X = ±10 V		±0.3	**±1**	% Full Scale
Y Feedthrough	X Nulled, Y = ±10 V		±0.1	**±0.4**	% Full Scale
Output Offset Voltage			±5	**±50**	mV
DYNAMICS					
Small Signal BW	V_O = 0.1 V rms,		1		MHz
Slew Rate	V_O = 20 V p–p		20		V/μs
Settling Time to 1%	Δ V_O = 20 V		2		μs
OUTPUT NOISE					
Spectral Density			0.8		μV/√Hz
Wideband Noise	f = 10 Hz to 5 MHz		1		mV rms
	f = 10 Hz to 10 kHz		90		μV rms
OUTPUT					
Output Voltage Swing		**±11**			V
Short Circuit Current	R_L = 0 Ω		30	**40**	mA
INPUT AMPLIFIERS					
Signal Voltage Range	Differential	**±10**			V
	Common Mode	**±10**			V
Offset Voltage X, Y			±5	**±30**	mV
CMRR X, Y	V_{CM} = ±10 V, f = 50 Hz	**60**	80		dB
Bias Current X, Y, Z			0.8	**2.0**	μA
Differential Resistance			10		MΩ
POWER SUPPLY					
Supply Voltage					
Rated Performance			±15		V
Operating Range		**±8**		**±18**	V
Supply Current	Quiescent		4	**6**	mA

NOTES

Specifications shown in **boldface** are tested on all production units at electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 500 mW
Input Voltages[3] . . . . . ±18 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C
ESD Rating . . . . . 1000 V

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

[2]8-Pin Plastic Package: θ_{JA} = 165°C/W; 8-Pin Small Outline Package: θ_{JA} = 155°C/W.

[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING GUIDE

Model	Description	Package Option*
AD633JN	8-Pin Plastic DIP	N-8
AD633JR	8-Pin Plastic SOIC	R-8
AD633JR-REEL	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.

ANALOG DEVICES

10 MHz, 4-Quadrant Multiplier/Divider

AD734

FEATURES

High Accuracy
- 0.1% Typical Error

High Speed
- 10 MHz Full-Power Bandwidth
- 450 V/μs Slew Rate
- 200 ns Settling to 0.1% at Full Power

Low Distortion
- −80 dBc from Any Input
- Third-Order IMD Typically −75 dBc at 10 MHz

Low Noise
- 94 dB SNR, 10 Hz to 20 kHz
- 70 dB SNR, 10 Hz to 10 MHz

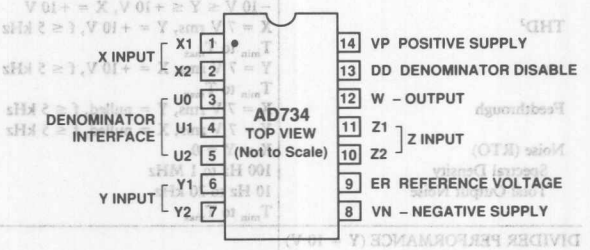
Direct Division Mode
- 2 MHz BW at Gain of 100

APPLICATIONS

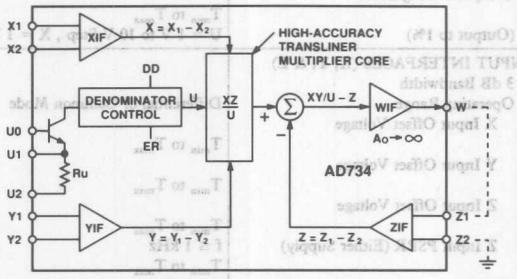
High Performance Replacement for AD534
Multiply, Divide, Square, Square Root
Modulator, Demodulator
Wideband Gain Control, RMS-DC Conversion
Voltage-Controlled Amplifiers, Oscillators, and Filters
Demodulator with 40 MHz Input Bandwidth

CONNECTION DIAGRAM

14-Pin DIP
(Q Package) & (N Package)



FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD734 is an accurate high speed, four-quadrant analog multiplier that is pin-compatible with the industry-standard AD534 and provides the transfer function W = XY/U. The AD734 provides a low-impedance voltage output with a full-power (20 V pk–pk) bandwidth of 10 MHz. Total static error (scaling, offsets, and nonlinearities combined) is 0.1% of Full Scale. Distortion is typically less than −80 dBc and guaranteed. The low-capacitance X, Y and Z inputs are fully differential. In most applications, no external components are required to define the function.

The internal scaling (denominator) voltage U is 10 V, derived from a buried-Zener voltage reference. A new feature provides the option of substituting an external denominator voltage, allowing the use of the AD734 as a two-quadrant divider with a 1000:1 denominator range and a signal bandwidth that remains 10 MHz to a gain of 20 dB, 2 MHz at a gain of 40 dB and 200 kHz at a gain of 60 dB, for a gain-bandwidth product of 200 MHz.

The advanced performance of the AD734 is achieved by a combination of new circuit techniques, the use of a high speed complementary bipolar process and a novel approach to laser-trimming based on ac signals rather than the customary dc methods. The wide bandwidth (>40 MHz) of the AD734's input stages and the 200 MHz gain-bandwidth product of the multiplier core allow the AD734 to be used as a low distortion demodulator with input frequencies as high as 40 MHz as long as the desired output frequency is less than 10 MHz.

The AD734AQ and AD734BQ are specified for the industrial temperature range of −40°C to +85°C and come in a 14-pin ceramic DIP. The AD734SQ/883B, available processed to MIL-STD-883B for the military range of −55°C to +125°C, is available in a 14-pin ceramic DIP.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

The AD734 embodies more than two decades of experience in the design and manufacture of analog multipliers, to provide:

1. A new output amplifier design with more than twenty times the slew-rate of the AD534 (450 V/μs versus 20 V/μs) for a full power (20 V pk–pk) bandwidth of 10 MHz.
2. Very low distortion, even at full power, through the use of circuit and trimming techniques that virtually eliminate all of the spurious nonlinearities found in earlier designs.
3. Direct control of the denominator, resulting in higher multiplier accuracy and a gain-bandwidth product at small denominator values that is typically 200 times greater than that of the AD534 in divider modes.
4. Very clean transient response, achieved through the use of a novel input stage design and wide-band output amplifier, which also ensure that distortion remains low even at high frequencies.
5. Superior noise performance by careful choice of device geometries and operating conditions, which provide a guaranteed 88 dB of dynamic range in a 20 kHz bandwidth.

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AD734—SPECIFICATIONS (T_A = +25°C, $+V_S$ = VP = +15 V, $-V_S$ = VN = −15 V, $R_L \geq 2$ kΩ)

TRANSFER FUNCTION

$$W = A_O\left\{\frac{(X_1 - X_2)(Y_1 - Y_2)}{(U_1 - U_2)} - (Z_1 - Z_2)\right\}$$

Parameter	Conditions	A Min	A Typ	A Max	B Min	B Typ	B Max	S Min	S Typ	S Max	Units
MULTIPLIER PERFORMANCE											
Transfer Function			W = XY/10			W = XY/10			W = XY/10		
Total Static Error[1]	−10 V ≤ X,Y ≤ 10 V		0.1	0.4		0.1	0.25		0.1	0.4	%
Over T_{min} to T_{max}				1			0.6			1.25	%
vs. Temperature	T_{min} to T_{max}		0.004			0.003			0.004		%/°C
vs. Either Supply	$\pm V_S$ = 14 V to 16 V		0.01	0.05		0.01	0.05		0.01	0.05	%/V
Peak Nonlinearity	−10 V ≤ X ≤ +10 V, Y = +10 V		0.05			0.05			0.05		%
	−10 V ≤ Y ≤ +10 V, X = +10 V		0.025			0.025			0.025		%
THD[2]	X = 7 V rms, Y = +10 V, f ≤ 5 kHz			−58			−66			−58	dBc
	T_{min} to T_{max}			−55			−63			−55	dBc
	Y = 7 V rms, X = +10 V, f ≤ 5 kHz			−60			−80			−60	dBc
	T_{min} to T_{max}			−57			−74			−57	dBc
Feedthrough	X = 7 V rms, Y = nulled, f ≤ 5 kHz		−85	−60		−85	−70		−85	−60	dBc
	Y = 7 V rms, X = nulled, f ≤ 5 kHz		−85	−66		−85	−76		−85	−66	dBc
Noise (RTO)	X = Y = 0										
Spectral Density	100 Hz to 1 MHz		1.0			1.0			1.0		$\mu V/\sqrt{Hz}$
Total Output Noise	10 Hz to 20 kHz		−94	−88		−94	−88		−94	−88	dBc
	T_{min} to T_{max}			−85			−85			−85	dBc
DIVIDER PERFORMANCE (Y = 10 V)											
Transfer Function			W = XY/U			W = XY/U			W = XY/U		
Gain Error	Y = 10 V, U = 100 mV to 10 V		1			1			1		%
X Input Clipping Level	Y ≤ 10 V		1.25 × U			1.25 × U			1.25 × U		V
U Input Scaling Error[3]				0.3			0.15			0.3	%
	T_{min} to T_{max}			0.8			0.65			1	%
(Output to 1%)	U = 1 V to 10 V Step , X = 1 V		100			100			100		ns
INPUT INTERFACES (X, Y, & Z)											
3 dB Bandwidth			40			40			40		MHz
Operating Range	Differential or Common Mode		±12.5			±12.5			±12.5		V
X Input Offset Voltage				15			5			15	mV
	T_{min} to T_{max}			25			15			25	mV
Y Input Offset Voltage				10			5			10	mV
	T_{min} to T_{max}			12			6			12	mV
Z Input Offset Voltage				20			10			20	mV
	T_{min} to T_{max}			50			50			90	mV
Z Input PSRR (Either Supply)	f ≤ 1 kHz	54	70		66	70		54	70		dB
	T_{min} to T_{max}	50			56			50			dB
CMRR	f = 5 kHz	70	85		70	85		70	85		dB
Input Bias Current (X, Y, Z Inputs)			50	300		50	150		50	300	nA
	T_{min} to T_{max}			400			300			500	nA
Input Resistance	Differential		50			50			50		kΩ
Input Capacitance	Differential		2			2			2		pF
DENOMINATOR INTERFACES (U0, U1, & U2)											
Operating Range			VN to VP-3			VN to VP-3			VN to VP-3		V
Denominator Range			1000:1			1000:1			1000:1		
Interface Resistor	U1 to U2		28			28			28		kΩ
OUTPUT AMPLIFIER (W)											
Output Voltage Swing	T_{min} to T_{max}		±12			±12			±12		V
Open-Loop Voltage Gain	X = Y = 0, Input to Z		72			72			72		dB
Dynamic Response	From X or Y Input, CL ≤ 20 pF										
3 dB Bandwidth	W ≤ 7 V rms	8	10		8	10		8	10		MHz
Slew Rate			450			450			450		V/μs
Settling Time	+20 V or −20 V Output Step										
To 1%			125			125			125		ns
To 0.1%			200			200			200		ns
Short-Circuit Current	T_{min} to T_{min}	20	50	80	20	50	80	20	50	80	mA
POWER SUPPLIES, $\pm V_S$											
Operating Supply Range		±8		±16.5	±8		±16.5	±8		±16.5	V
Quiescent Current	T_{min} to T_{max}	6	9	12	6	9	12	6	9	12	mA

NOTES

[1]Figures given are percent of full scale (e.g., 0.01% = 1 mV).

[2]dBc refers to deciBels relative to the full scale input (carrier) level of 7 V rms.

[3]See Figure 10 for test circuit.

All min and max specifications are guaranteed. Specifications in **Boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
for T_J max = 175°C . . . . . 500 mW
X, Y and Z Input Voltages . . . . . VN to VP
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
Q . . . . . −65°C to +150°C
Operating Temperature Range
AD734A, B (Industrial) . . . . . −40°C to +85°C
AD734S (Military) . . . . . −55°C to +125°C
Lead Temperature Range (soldering 60 sec) . . . . . +300°C
Transistor Count 81
ESD Rating . . . . . 500 V

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.
[2]14-Pin Ceramic DIP: θ_{JA} = 110°C/W

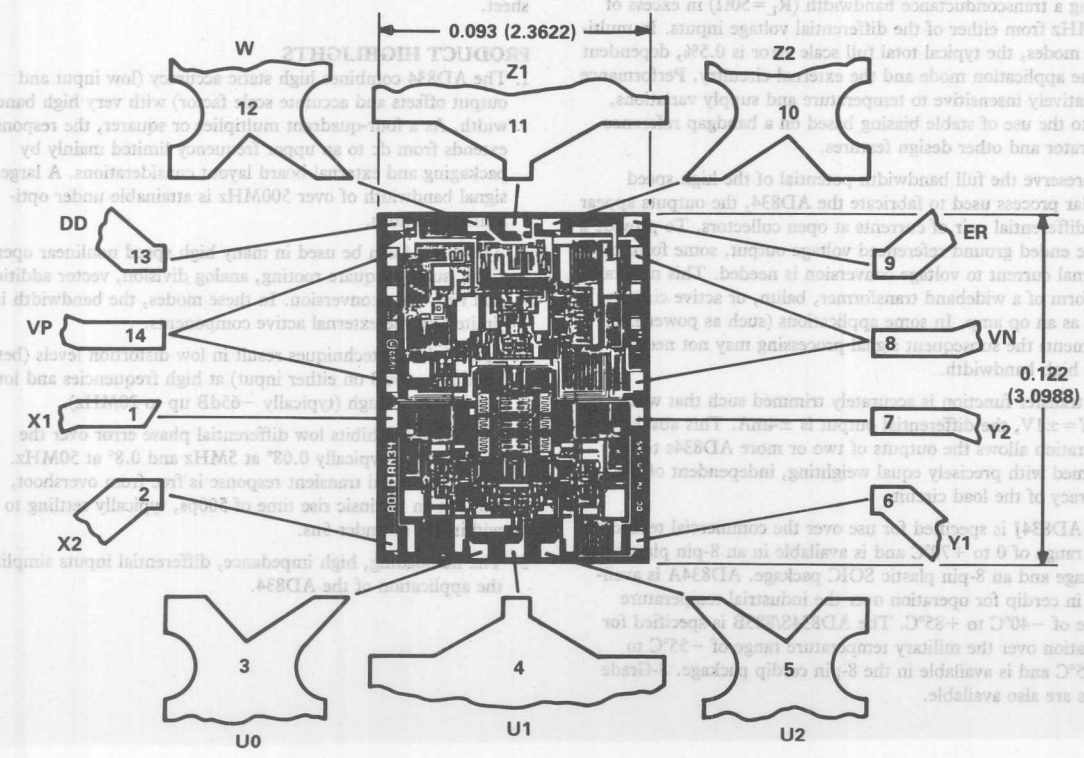
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD734AN	−40°C to +85°C	Plastic DIP	N-14
AD734BN	−40°C to +85°C	Plastic DIP	N-14
AD734AQ	−40°C to +85°C	Cerdip	Q-14
AD734BQ	−40°C to +85°C	Cerdip	Q-14
AD734SQ	−55°C to +125°C	Cerdip	Q-14
AD734SQ/883B	−55°C to +125°C	Cerdip	Q-14
AD734S Chip	−55°C to +125°C	Chip	

*For outline information see Package Information section.

CHIP DIMENSIONS & BONDING DIAGRAM

Dimensions shown in inches and (mm).
(Contact factory for latest dimensions.)



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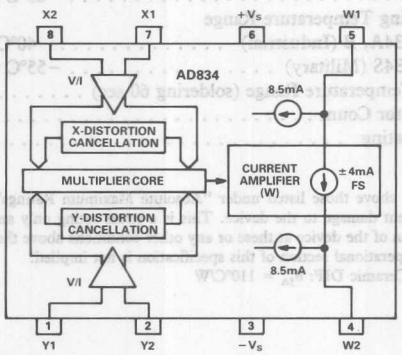
FEATURES

DC to >500MHz Operation
Differential ±1V Full Scale Inputs
Differential ±4mA Full Scale Output Current
Low Distortion (≤0.05% for 0dBm Input)
Supply Voltages from ±4V to ±9V
Low Power (280mW typical at V_S=±5V)

APPLICATIONS

High Speed Real Time Computation
Wideband Modulation and Gain Control
Signal Correlation and RF Power Measurement
Voltage Controlled Filters and Oscillators
Linear Keyers for High Resolution Television
Wideband True RMS

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD834 is a monolithic laser-trimmed four-quadrant analog multiplier intended for use in high frequency applications, having a transconductance bandwidth (R_L=50Ω) in excess of 500MHz from either of the differential voltage inputs. In multiplier modes, the typical total full scale error is 0.5%, dependent on the application mode and the external circuitry. Performance is relatively insensitive to temperature and supply variations, due to the use of stable biasing based on a bandgap reference generator and other design features.

To preserve the full bandwidth potential of the high speed bipolar process used to fabricate the AD834, the outputs appear as a differential pair of currents at open collectors. To provide a single ended ground referenced voltage output, some form of external current to voltage conversion is needed. This may take the form of a wideband transformer, balun, or active circuitry such as an op amp. In some applications (such as power measurement) the subsequent signal processing may not need to have high bandwidth.

The transfer function is accurately trimmed such that when X=Y=±1V, the differential output is ±4mA. This absolute calibration allows the outputs of two or more AD834s to be summed with precisely equal weighting, independent of the accuracy of the load circuit.

The AD834J is specified for use over the commercial temperature range of 0 to +70°C and is available in an 8-pin plastic DIP package and an 8-pin plastic SOIC package. AD834A is available in cerdip for operation over the industrial temperature range of −40°C to +85°C. The AD834S/883B is specified for operation over the military temperature range of −55°C to +125°C and is available in the 8-pin cerdip package. S-Grade chips are also available.

Two application notes featuring the AD834 (AN-212 and AN-216) can now be obtained by calling 1-800-ANALOG-D. For additional applications circuits, consult the AD811 data sheet.

PRODUCT HIGHLIGHTS

1. The AD834 combines high static accuracy (low input and output offsets and accurate scale factor) with very high bandwidth. As a four-quadrant multiplier or squarer, the response extends from dc to an upper frequency limited mainly by packaging and external board layout considerations. A large signal bandwidth of over 500MHz is attainable under optimum conditions.
2. The AD834 can be used in many high speed nonlinear operations, such as square rooting, analog division, vector addition and rms-to-dc conversion. In these modes, the bandwidth is limited by the external active components.
3. Special design techniques result in low distortion levels (better than −60dB on either input) at high frequencies and low signal feedthrough (typically −65dB up to 20MHz).
4. The AD834 exhibits low differential phase error over the input range—typically 0.08° at 5MHz and 0.8° at 50MHz. The large signal transient response is free from overshoot, and has an intrinsic rise time of 500ps, typically settling to within 1% in under 5ns.
5. The nonloading, high impedance, differential inputs simplify the application of the AD834.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (T_A = +25°C and $\pm V_S$ = ±5V, unless otherwise noted; dBm assumes 50Ω load.)

Model	Conditions	AD834J Min	AD834J Typ	AD834J Max	AD834A, S Min	AD834A, S Typ	AD834A, S Max	Units
MULTIPLIER PERFORMANCE								
Transfer Function			$W = \frac{XY}{(1V)^2} \times 4mA$			$W = \frac{XY}{(1V)^2} \times 4mA$		
Total Error[1] (Figure 6)	−1V≤X,Y<+1V		±0.5	**±2**		±0.5	**±2**	% FS
vs. Temperature	T_{min} to T_{max}					±1.5	**±3**	% FS
vs. Supplies[2]	±4V to ±6V		0.1	**0.3**		0.1	**0.3**	% FS/V
Linearity[3]			±0.5	**±1**		±0.5	**±1**	% FS
Bandwidth[4]	See Figure 5	500			500			MHz
Feedthrough, X	X=±1V, Y=Nulled		0.2	**0.3**		0.2	**0.3**	% FS
Feedthrough, Y	X=Nulled, Y=±1V		0.1	**0.2**		0.1	**0.2**	% FS
AC Feedthrough, X[5]	X=0dBm, Y=Nulled							
	f=10MHz		−65			−65		dB
	f=100MHz		−50			−50		dB
AC Feedthrough, Y[5]	X=Nulled, Y=0dBm							
	f=10MHz		−70			−70		dB
	f=100MHz		−50			−50		dB
INPUTS (X1, X2, Y1, Y2)								
Full Scale Range	Differential		±1			±1		V
Clipping Level	Differential	**±1.1**	±1.3		**±1.1**	±1.3		V
Input Resistance	Differential		25			25		kΩ
Offset Voltage			0.5	**3**		0.5	**3**	mV
vs. Temperature	T_{min} to T_{max}		10			10		µV/°C
				4			**4**	mV
vs. Supplies[2]	±4V to ±6V		100	**300**		100	**300**	µV/V
Bias Current			45			45		µA
Common Mode Rejection	f≤100kHz; 1V p–p		70			70		dB
Nonlinearity, X	Y=1V; X=±1V		0.2	**0.5**		0.2	**0.5**	% FS
Nonlinearity, Y	X=1V; Y=±1V		0.1	**0.3**		0.1	**0.3**	% FS
Distortion, X	X=0dBm, Y=1V							
	f=10MHz		−60			−60		dB
	f=100MHz		−44			−44		dB
Distortion, Y	X=1V, Y=0dBM							
	f=10MHz		−65			−65		dB
	f=100MHz		−50			−50		dB
OUTPUTS (W1, W2)								
Zero Signal Current	Each Output		8.5			8.5		mA
Differential Offset	X=0, Y=0		±20	**±60**		±20	**±60**	µA
vs. Temperature	T_{min} to T_{max}		40			40		nA/°C
							±60	µA
Scaling Current	Differential	3.96	4	4.04	3.96	4	4.04	mA
Output Compliance		4.75		9	4.75		9	V
Noise Spectral Density	f=10Hz to 1MHz Outputs into 50Ω Load		16			16		nV/√Hz
POWER SUPPLIES								
Operating Range		±4		±9	±4		±9	V
Quiescent Current[6]	T_{min} to T_{max}							
$+V_S$			11	**14**		11	**14**	mA
$-V_S$			28	**35**		28	**35**	mA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0 to +70°C)			AD834J, JR-REEL					
Military (−55°C to +125°C)						AD834S		
Industrial (−40°C to +85°C)						AD834A		
PACKAGE OPTIONS								
8-Pin SOIC (R)			AD834JR					
8-Pin Cerdip (Q)						AD834AQ		
8-Pin Plastic DIP (N)			AD834JN			AD834SQ/883B		

NOTES

[1]Error is defined as the maximum deviation from the ideal output, and expressed as a percentage of the full scale output.

[2]Both supplies taken simultaneously; sinusoidal input at f≤10kHz.

[3]Linearity is defined as residual error after compensating for input offset voltage, output offset current and scaling current errors.

[4]Bandwidth is guaranteed when configured in squarer mode. See Figure 5.

[5]Sine input; relative to full scale output; zero input port nulled; represents feedthrough of the fundamental.

[6]Negative supply current is equal to the sum of positive supply current, the signal currents into each output, W1 and W2, and the input bias currents.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S$ to $-V_S$) 18V
Internal Power Dissipation 500mW
Input Voltages (X1, X2, Y1, Y2) . . . . . $+V_S$
Operating Temperature Range
AD834J . . . . . 0 to +70°C
AD834A . . . . . −40°C to +85°C
AD834S/883B . . . . . −55°C to +125°C
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (R, N) . . . . . −65°C to +125°C
Lead Temperature, Soldering 60sec . . . . . +300°C
ESD Rating . . . . . 500 V

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

	θ_{JC}	θ_{JA}
8-Pin Cerdip Package (Q)	30°C/W	110°C/W
8-Pin Plastic SOIC (R)	45°C/W	165°C/W
8-Pin Plastic Mini-DIP (N)	50°C/W	99°C/W

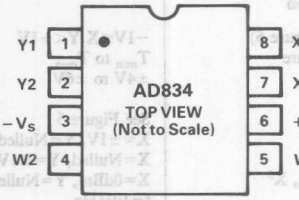
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD834JN	0 to +70°C	N-8
AD834JR	0 to +70°C	R-8
AD834JR-REEL	0 to +70°C	R-8
AD834AQ	−40°C to +85°C	Q-8
AD834SQ/883B	−55°C to +125°C	Q-8
AD834S Chips		Chips

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC) Package. For outline information see Package Information section.

CONNECTION DIAGRAM

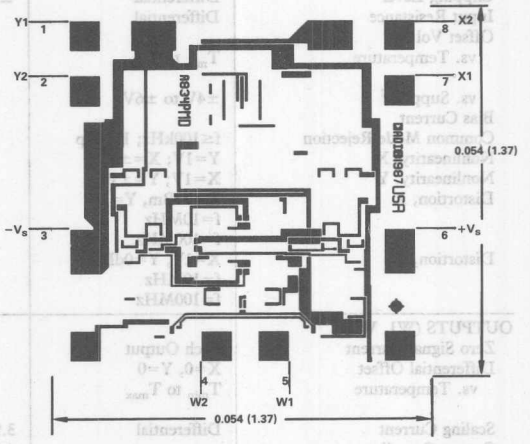
Small Outline (R) Package
Plastic DIP (N) Package
Cerdip (Q) Package



METALIZATION PHOTOGRAPH

CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



250 MHz, Voltage Output 4-Quadrant Multiplier

AD835

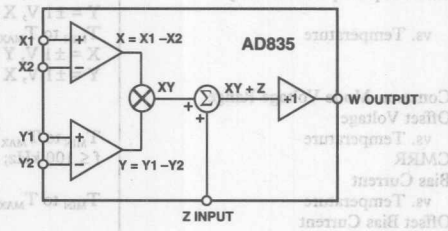
FEATURES

Simple: Basic Function is W = XY + Z
Complete: Minimal External Components Required
Very Fast: Settles to 0.1% of FS in 20 ns
DC-Coupled Voltage Output Simplifies Use
High Differential Input Impedance X, Y and Z Inputs
Low Multiplier Noise: 50 nV/$\sqrt{\text{Hz}}$

APPLICATIONS

Very Fast Multiplication, Division, Squaring
Wideband Modulation and Demodulation
Phase Detection and Measurement
Sinusoidal Frequency Doubling
Video Gain Control and Keying
Voltage Controlled Amplifiers and Filters

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD835 is a complete four-quadrant voltage output analog multiplier fabricated on an advanced dielectrically isolated complementary bipolar process. It generates the linear product of its X and Y voltage inputs, with a –3 dB output bandwidth of 250 MHz (a small signal rise time of 1 ns). Full-scale (–1 V to +1 V) rise/fall times are 2.5 ns (with the standard R_L of 150 Ω) and the settling time to 0.1% under the same conditions is typically 20 ns.

Its differential multiplication inputs (X, Y) and its summing input (Z) are at high impedance. The low impedance output voltage (W) can provide up to ±2.5 V and drive loads as low as 25 Ω. Normal operation is from ±5 V supplies.

Though providing state-of-the-art speed, the AD835 is simple to use and versatile. For example, as well as permitting the addition of a signal at the output, the Z input provides the means to operate the AD835 with voltage gains up to about ×10. In this capacity, the very low product noise of this multiplier (50 nV$\sqrt{\text{Hz}}$) makes it much more useful than earlier products.

The AD835 is available in an 8-pin plastic mini-DIP package (N) and an 8-pin SOIC (R) and is specified to operate over the –40°C to +85°C industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD835 is the first monolithic 250 MHz four quadrant voltage output multiplier.
2. Minimal external components are required to apply the AD835 to a variety of signal processing applications.
3. High input impedances (100 kΩ‖2 pF) make signal source loading negligible.
4. High output current capability allows low impedance loads to be driven.
5. State of the art noise levels achieved through careful device optimization and the use of a special low noise bandgap voltage reference.
6. Designed to be easy to use and cost effective in applications which formerly required the use of hybrid or board level solutions.

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

TRANSFER FUNCTION		$W = \frac{(X1-X2)(Y1-Y2)}{U} + Z$			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS (X, Y)					
Differential Voltage Range	V_{CM} = 0		±1		V
Differential Clipping Level		±1.2	±1.4		V
Low Frequency Nonlinearity	X = ±1 V, Y = 1 V		0.3	**0.5**	% FS
	Y = ±1 V, X = 1 V		0.1	**0.3**	% FS
vs. Temperature	T_{MIN} to T_{MAX}[1]				
	X = ±1 V, Y = 1 V			0.7	% FS
	Y = ±1 V, X = 1 V			0.5	% FS
Common-Mode Voltage Range		–2.5		+3	V
Offset Voltage			±3	**±20**	mV
vs. Temperature	T_{MIN} to T_{MAX}[1]			±25	mV
CMRR	f ≤ 100 kHz; ±1 V p-p	**70**			dB
Bias Current			10	**20**	µA
vs. Temperature	T_{MIN} to T_{MAX}[1]			27	µA
Offset Bias Current			2		µA
Differential Resistance			100		kΩ
Single-Sided Capacitance			2		pF
Feedthrough, X	X = ±1 V, Y = 0 V			**–46**	dB
Feedthrough, Y	Y = ±1 V, X = 0 V			**–60**	dB
DYNAMIC CHARACTERISTICS					
–3 dB Small-Signal Bandwidth		150	250		MHz
–0.1 dB Gain Flatness Frequency			15		MHz
Slew Rate	W = –2.5 V to +2.5 V		1000		V/µs
Differential Gain Error, X	f = 3.58 MHz		0.3		%
Differential Phase Error, X	f = 3.58 MHz		0.2		Degrees
Differential Gain Error, Y	f = 3.58 MHz		0.1		%
Differential Phase Error, Y	f = 3.58 MHz		0.1		Degrees
Harmonic Distortion	X or Y = 10 dBm, 2nd and 3rd Harmonic				
	Fund = 10 MHz		–70		dB
	Fund = 50 MHz		–40		dB
Settling Time, X or Y	To 0.1%, W = 2 V p-p		20		ns
SUMMING INPUT (Z)					
Gain	From Z to W, f ≤ 10 MHz	0.990	0.995		
–3 dB Small-Signal Bandwidth			250		MHz
Differential Input Resistance			60		kΩ
Single Sided Capacitance			2		pF
Maximum Gain	X, Y to W, Z Shorted to W, f = 1 kHz		50		dB
Bias Current			50		µA
OUTPUT CHARACTERISTICS					
Voltage Swing		±2.2	±2.5		V
vs. Temperature	T_{MIN} to T_{MAX}[1]	±2.0			V
Voltage Noise Spectral Density	X = Y = 0, f < 10 MHz		50		nV/√Hz
Offset Voltage			±25	**±75**	mV
vs. Temperature[2]	T_{MIN} to T_{MAX}[1]			±10	mV
Short Circuit Current			75		mA
Scale Factor Error			±5	**±8**	% FS
vs. Temperature	T_{MIN} to T_{MAX}[1]			±9	% FS
Linearity (Relative Error)[3]			±0.5	**±1.0**	% FS
vs. Temperature	T_{MIN} to T_{MAX}[1]			±1.25	% FS
POWER SUPPLIES					
Supply Voltage					
For Specified Performance		±4.5	±5	±5.5	V
Quiescent Supply Current			16	**25**	mA
vs. Temperature	T_{MIN} to T_{MAX}[1]			26	mA
PSRR at Output vs. Vp	+4.5 V to +5.5 V			**0.5**	%/V
PSRR at Output vs. Vn	–4.5 V to –5.5 V			**0.5**	%/V

NOTES
[1]T_{MIN} = –40°C, T_{MAX} = +85°C.
[2]Normalized to zero at +25°C.
[3]Linearity is defined as residual error after compensating for input offset, output voltage offset and scale factor errors.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

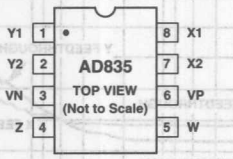
Supply Voltage . . . . . ±6 V
Internal Power Dissipation[2] . . . . . 300 mW
Operating Temperature Range . . . . . –40°C to +85C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Soldering 60 sec . . . . . +300°C
ESD Rating . . . . . 1500 V

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

[2]Thermal Characteristics:
8-Pin Plastic DIP (N): θ_{JC} = 35°C/W; θ_{JA} = 90°C/W
8-Pin Plastic SOIC (R): θ_{JC} = 45°C/W; θ_{JA} = 115°C/W.

PIN CONNECTIONS
8-Pin Plastic DIP (N)
8-Pin Plastic SOIC (R)



ORDERING GUIDE

Model	Temperature Range	Package Options*
AD835AN	–40°C to +85°C	N-8
AD835AR	–40°C to +85°C	R-8

*N = Plastic DIP; R = Small Outline IC Plastic Package (SOIC). For outline information see Package information section

Typical Performance Characteristics

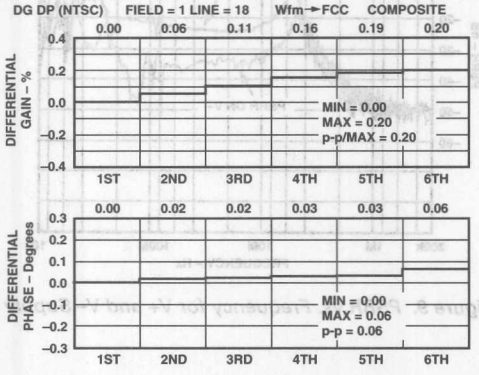


Figure 1. Typical Composite Output Differential Gain & Phase, NTSC for X Channel; f = 3.58 MHz, R_L = 150 Ω

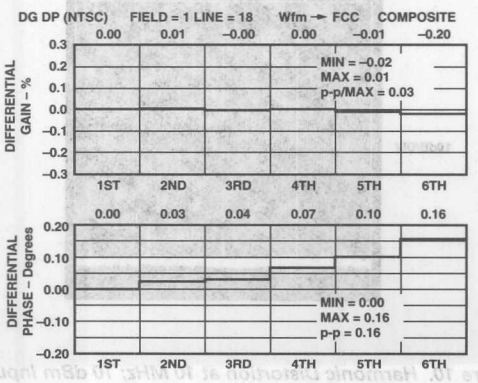


Figure 2. Typical Composite Output Differential Gain & Phase, NTSC for Y Channel; f = 3.58 MHz, R_L = 150 Ω

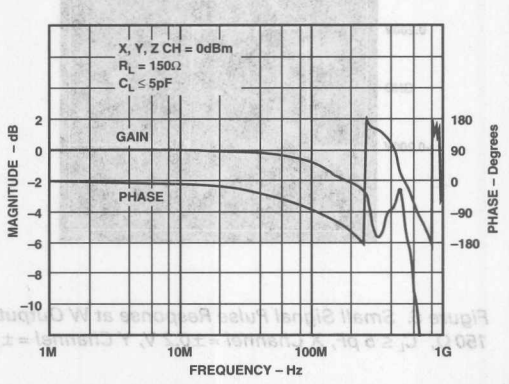


Figure 3. Gain & Phase vs. Frequency of X, Y, Z Inputs

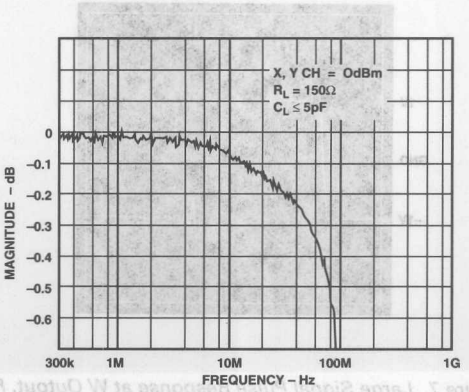


Figure 4. Gain Flatness to 0.1 dB

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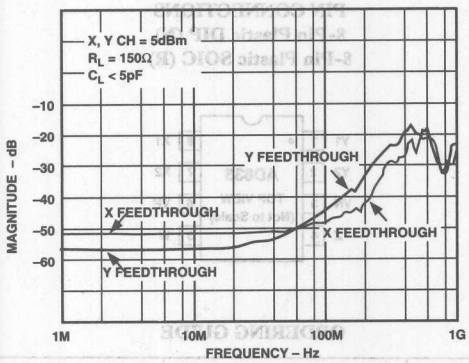

Figure 5. X and Y Feedthrough vs. Frequency

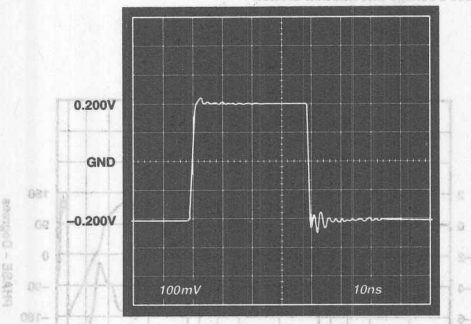

Figure 6. Small Signal Pulse Response at W Output, R_L = 150 Ω, $C_L \leq$ 5 pF, X Channel = ±0.2 V, Y Channel = ±1.0 V

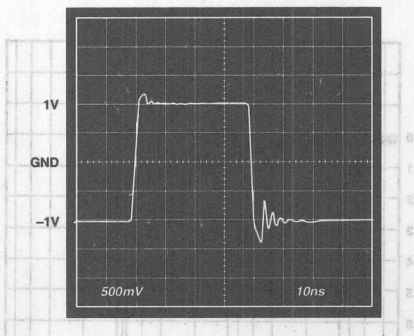

Figure 7. Large Signal Pulse Response at W Output, R_L = 150 Ω, $C_L \leq$ 5 pF, X Channel = ±1.0 V, Y Channel = ±1.0 V

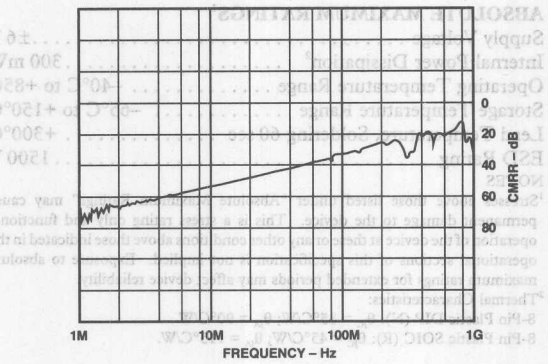

Figure 8. CMRR vs. Frequency for X or Y Channel, R_L = 150 Ω, $C_L \leq$ 5 pF

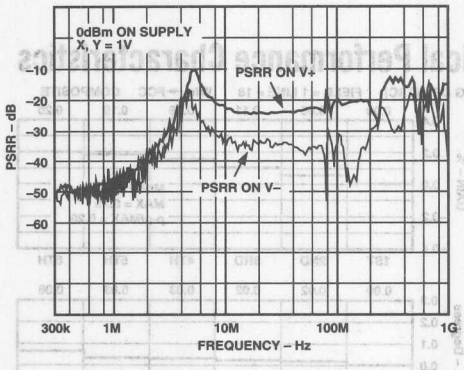

Figure 9. PSRR vs. Frequency for V+ and V– Supply

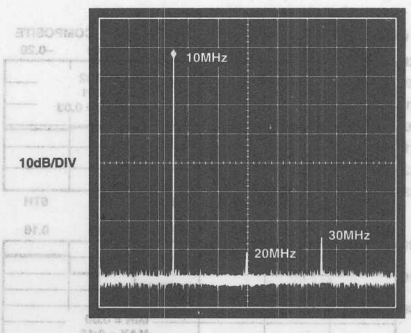

Figure 10. Harmonic Distortion at 10 MHz; 10 dBm Input to X or Y Channels, R_L = 150 Ω, $C_L = \leq$ 5 pF

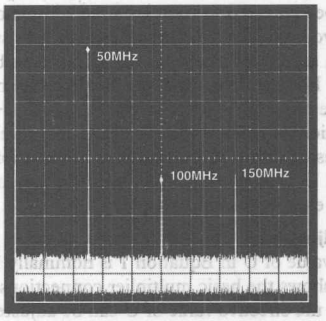

Figure 11. Harmonic Distortion at 50 MHz, 10 dBm Input to X or Y Channel, R_L = 150 Ω, C_L ≤ 5 pF

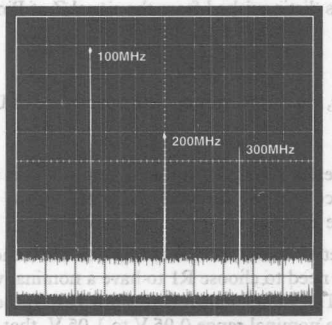

Figure 12. Harmonic Distortion at 100 MHz, 10 dBm Input to X or Y Channel, R_L = 150 Ω, C_L ≤ 5 pF

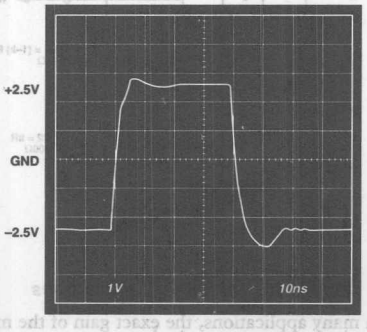

Figure 13. Maximum Output Voltage Swing, R_L = 50 Ω, C_L ≤ 5 pF

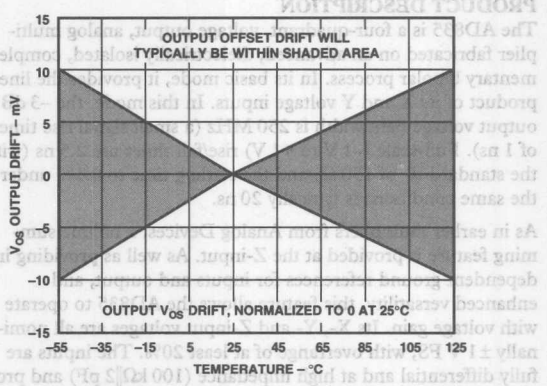

Figure 14. V_{OS} Output Drift vs. Temperature

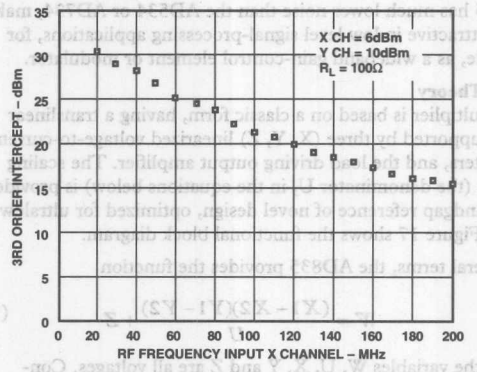

Figure 15. Fixed LO on Y Channel vs. RF Frequency Input to X Channel

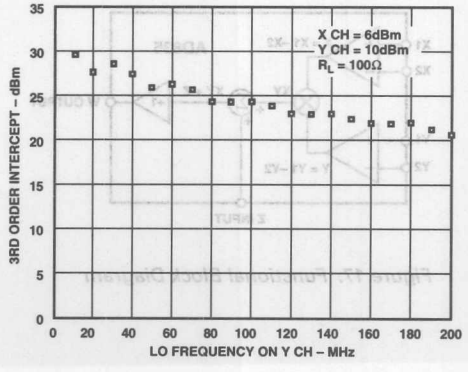

Figure 16. Fixed IF vs. LO Frequency on Y Channel

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The AD835 is a four-quadrant, voltage output, analog multiplier fabricated on an advanced, dielectrically isolated, complementary bipolar process. In its basic mode, it provides the linear product of its X and Y voltage inputs. In this mode, the –3 dB output voltage bandwidth is 250 MHz (a small signal rise time of 1 ns). Full-scale (–1 V to +1 V) rise/fall times are 2.5 ns (with the standard R_L of 150 Ω) and the settling time to 0.1% under the same conditions is typically 20 ns.

As in earlier multipliers from Analog Devices, a unique summing feature is provided at the Z-input. As well as providing independent ground references for inputs and output, and enhanced versatility, this feature allows the AD835 to operate with voltage gain. Its X-, Y- and Z-input voltages are all nominally ±1 V FS, with overrange of at least 20%. The inputs are fully differential and at high impedance (100 kΩ‖2 pF) and provide a 70 dB CMRR (f ≤ 1 MHz).

The low impedance output is capable of driving loads as small as 25 Ω. The peak output can be as large as ±2.2 V minimum for R_L = 150 Ω, or ±2.0 V minimum into R_L = 50 Ω. The AD835 has much lower noise than the AD534 or AD734, making it attractive in low level signal-processing applications, for example, as a wideband gain-control element or modulator.

Basic Theory

The multiplier is based on a classic form, having a translinear core, supported by three (X, Y, Z) linearized voltage-to-current converters, and the load driving output amplifier. The scaling voltage (the denominator U, in the equations below) is provided by a bandgap reference of novel design, optimized for ultralow noise. Figure 17 shows the functional block diagram.

In general terms, the AD835 provides the function

$$W = \frac{(X1 - X2)(Y1 - Y2)}{U} + Z \quad (1)$$

where the variables W, U, X, Y and Z are all voltages. Connected as a simple multiplier, with X = X1 – X2, Y = Y1 – Y2 and Z = 0, and with a scale factor adjustment (see below) which sets U = 1 V, the output can be expressed as

$$W = XY \quad (2)$$

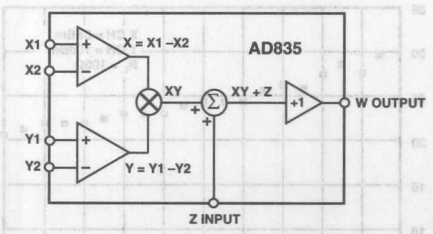


Figure 17. Functional Block Diagram

sumed to be expressed in *volts*, are used throughout this data sheet, to avoid the needless use of less-intuitive subscripted variables (such as V_{X1}). We can view all variables as being *normalized to 1 V*. For example, the input X can either be stated as being in the range –1 V to +1 V, or simply –1 to +1. The latter representation will be found to facilitate the development of new functions using the AD835. The explicit inclusion of the denominator, U, is also less helpful, as in the case of the AD835, if it is not an electrical input variable.

Scaling Adjustment

The basic value of U in Equation 1 is nominally 1.05 V. Figure 18, which shows the basic multiplier connections, also shows how the effective value of U can be adjusted to have any lower voltage (usually 1 V) through the use of a resistive-divider between W (Pin 5) and Z (Pin 4). Using the general resistor values shown, we can rewrite Equation 1 as

$$W = \frac{XY}{U} + kW + (1 - k)Z' \quad (3)$$

(where Z' is distinguished from the signal Z at Pin 4). It follows that

$$W = \frac{XY}{(1 - k)U} + Z' \quad (4)$$

In this way, we can modify the effective value of U to

$$U' = (1 - k)U \quad (5)$$

without altering the scaling of the Z' input. (This is to be expected, since the only "ground reference" for the output is through the Z' input.)

Thus, to set U' to 1 V, remembering that the basic value of U is 1.05 V, we need to choose R1 to have a nominal value of 20 times R2. The values shown here allow U to be adjusted through the nominal range 0.95 V to 1.05 V, that is, R2 provides a 5% gain adjustment.

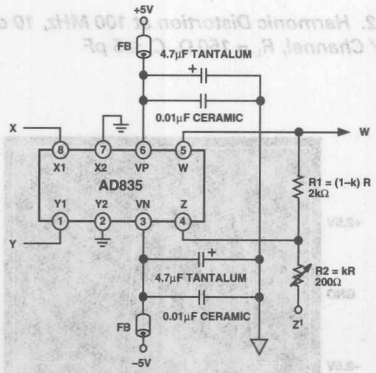


Figure 18. Multiplier Connections

Note that in many applications, the exact gain of the multiplier may not be very important; in which case, this network may be omitted entirely, or R2 fixed at 100 Ω.

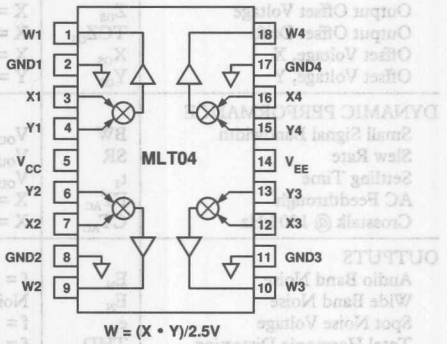
Four-Channel, Four-Quadrant Analog Multiplier

MLT04

FEATURES
- Four Independent Channels
- Voltage IN, Voltage OUT
- No External Parts Required
- 8 MHz Bandwidth
- Four-Quadrant Multiplication
- Voltage Output; W = (X × Y)/2.5 V
  - 0.2% Typical Linearity Error on X or Y Inputs
- Excellent Temperature Stability: 0.005%
- ±2.5 V Analog Input Range
- Operates from ±5 V Supplies
- Low Power Dissipation: 150 mW typ
- Spice Model Available

APPLICATIONS
- Geometry Correction in High-Resolution CRT Displays
- Waveform Modulation & Generation
- Voltage Controlled Amplifiers
- Automatic Gain Control
- Modulation and Demodulation

FUNCTIONAL BLOCK DIAGRAM
18-Lead Epoxy DIP (P Suffix)
18-Lead Wide Body SOIC (S Suffix)



GENERAL DESCRIPTION

The MLT04 is a complete, four-channel, voltage output analog multiplier packaged in an 18-pin DIP or SOIC-18. These complete multipliers are ideal for general purpose applications such as voltage controlled amplifiers, variable active filters, "zipper" noise free audio level adjustment, and automatic gain control. Other applications include cost-effective multiple-channel power calculations (I × V), polynomial correction generation, and low frequency modulation. The MLT04 multiplier is ideally suited for generating complex, high-order waveforms especially suitable for geometry correction in high-resolution CRT display systems.

Fabricated in a complementary bipolar process, the MLT04 includes four 4-quadrant multiplying cells which have been laser-trimmed for accuracy. A precision internal bandgap reference normalizes signal computation to a 0.4 scale factor. Drift over temperature is under 0.005%/°C. Spot noise voltage of 0.3 μV/√Hz results in a THD + Noise performance of 0.02% (LPF = 22 kHz) for the lower distortion Y channel. The four 8 MHz channels consume a total of 150 mW of quiescent power.

The MLT04 is available in 18-pin plastic DIP, and SOIC-18 surface mount packages. All parts are offered in the extended industrial temperature range (–40°C to +85°C).

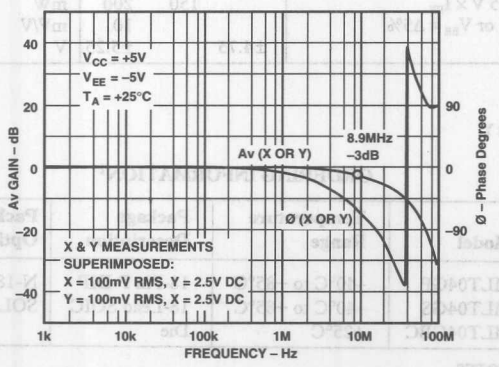


Figure 1. Gain & Phase vs. Frequency Response

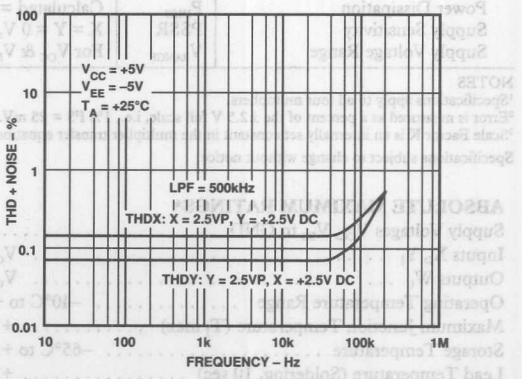


Figure 2. THD + Noise vs. Frequency

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MLT04—SPECIFICATIONS (V_{CC} = +5 V, V_{EE} = –5 V, V_{IN} = ±2.5 V_P, R_L = 2 kΩ, T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
MULTIPLIER PERFORMANCE[1]						
Total Error[2] X	E_X	–2.5 V < X < +2.5 V, Y = +2.5 V	–5	±2	5	% FS
Total Error[2] Y	E_Y	–2.5 V < Y < +2.5 V, X = +2.5 V	–5	±2	5	% FS
Linearity Error[2] X	LE_X	–2.5 V < X < +2.5 V, Y = +2.5 V	–1	±0.2	+1	% FS
Linearity Error[2] Y	LE_Y	–2.5 V < Y < +2.5 V, X = +2.5 V	–1	±0.2	+1	% FS
Total Error Drift	TCE_X	X = –2.5 V, Y = 2.5 V, T_A = –40°C to +85°C		0.005		%/°C
Total Error Drift	TCE_Y	Y = –2.5 V, X = 2.5 V, T_A = –40°C to +85°C		0.005		%/°C
Scale Factor[3]	K	X = ±2.5 V, Y = ±2.5 V, T_A = –40°C to +85°C	0.38	0.40	0.42	1/V
Output Offset Voltage	Z_{OS}	X = 0 V, Y = 0 V, T_A = –40°C to +85°C	–50	±10	50	mV
Output Offset Drift	TCZ_{OS}	X = 0 V, Y = 0 V, T_A = –40°C to +85°C		50		µV/°C
Offset Voltage, X	X_{OS}	X = 0 V, Y = ±2.5 V, T_A = –40°C to +85°C	–50	±10.5	50	mV
Offset Voltage, Y	Y_{OS}	Y = 0 V, X = ±2.5 V, T_A = –40°C to +85°C	–50	±10.5	50	mV
DYNAMIC PERFORMANCE						
Small Signal Bandwidth	BW	V_{OUT} = 0.1 V rms		8		MHz
Slew Rate	SR	V_{OUT} = ±2.5 V	30	53		V/µs
Settling Time	t_S	V_{OUT} = Δ2.5 V to 1% Error Band		1		µs
AC Feedthrough	FT_{AC}	X = 0 V, Y = 1 V rms @ f = 100 kHz		–65		dB
Crosstalk @ 100 kHz	CT_{AC}	X = Y = 1 V rms Applied to Adjacent Channel		–90		dB
OUTPUTS						
Audio Band Noise	E_N	f = 10 Hz to 50 kHz		76		µV rms
Wide Band Noise	E_N	Noise BW = 1.9 MHz		380		µV rms
Spot Noise Voltage	e_N	f = 1 kHz		0.3		µV/√Hz
Total Harmonic Distortion	THD_X	f = 1 kHz, LPF = 22 kHz, Y = 2.5 V		0.1		%
	THD_Y	f = 1 kHz, LPF = 22 kHz, X = 2.5 V		0.02		%
Open Loop Output Resistance	R_{OUT}			40		Ω
Voltage Swing	V_{PK}	V_{CC} = +5 V, V_{EE} = –5 V	±3.0	±3.3		V_P
Short Circuit Current	I_{SC}			30		mA
INPUTS						
Analog Input Range	IVR	GND = 0 V	–2.5		+2.5	V
Bias Current	I_B	X = Y = 0 V		2.3	10	µA
Resistance	R_{IN}			1		MΩ
Capacitance	C_{IN}			3		pF
SQUARE PERFORMANCE						
Total Square Error	E_{SQ}	X = Y = 1		5		% FS
POWER SUPPLIES						
Positive Current	I_{CC}	V_{CC} = 5.25 V, V_{EE} = –5.25 V		15	20	mA
Negative Current	I_{EE}	V_{CC} = 5.25 V, V_{EE} = –5.25 V		15	20	mA
Power Dissipation	P_{DISS}	Calculated = 5 V × I_{CC} + 5 V × I_{EE}		150	200	mW
Supply Sensitivity	PSSR	X = Y = 0 V, V_{CC} = Δ5% or V_{EE} = Δ5%			10	mV/V
Supply Voltage Range	V_{RANGE}	For V_{CC} & V_{EE}	±4.75		±5.25	V

NOTES
[1]Specifications apply to all four multipliers.
[2]Error is measured as a percent of the ±2.5 V full scale, i.e., 1% FS = 25 mV.
[3]Scale Factor K is an internally set constant in the multiplier transfer equation W = K × X × Y.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltages V_{CC}, V_{EE} to GND ..... ±7 V
Inputs X_I, Y_I ..... V_{CC}, V_{EE}
Outputs W_I ..... V_{CC}, V_{EE}
Operating Temperature Range ..... –40°C to +85°C
Maximum Junction Temperature (T_J max) ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... $(T_J max – T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
PDIP-18 (N-18) ..... 74°C/W
SOIC-18 (SOL-18) ..... 89°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification are not implied.

ORDERING INFORMATION[1]

Model	Temperature Range	Package Description	Package Option[2]
MLT04GP	–40°C to +85°C	18-Pin P-DIP	N-18
MLT04GS	–40°C to +85°C	18-Lead SOIC	SOL-18
MLT04GBC	+25°C	Die	

NOTES
[1]For die specifications contact your local Analog sales office. The MLT04 contains 211 transistors.
[2]For outline information see Package Information section.

FUNCTIONAL DESCRIPTION

The MLT04 is a low cost quad, 4-quadrant analog multiplier with single-ended voltage inputs and voltage outputs. The functional block diagram for each of the multipliers is illustrated in Figure 3. Due to packaging constraints, access to internal nodes for externally adjusting scale factor, output offset voltage, or additional summing signals is not provided.

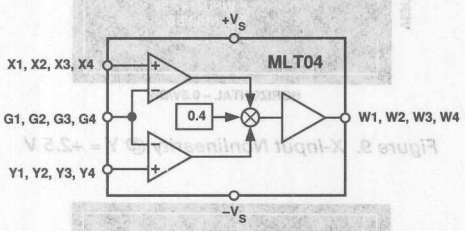

Figure 3. Functional Block Diagram of Each MLT04 Multiplier

Each of the MLT04's analog multipliers is based on a Gilbert cell multiplier configuration, a 1.23 V bandgap reference, and a unity-connected output amplifier. Multiplier scale factor is determined through a differential pair/trimmable resistor network external to the core. An equivalent circuit for each of the multipliers is shown in Figure 4.

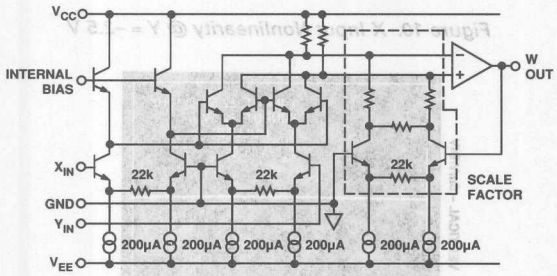

Figure 4. Equivalent Circuit for the MLT04

Details of each multiplier's output-stage amplifier are shown in Figure 5. The output stages idles at 200 µA, and the resistors in series with the emitters of the output stage are 25 Ω. The output stage can drive load capacitances up to 500 pF without oscillation. For loads greater than 500 pF, the outputs of the MLT04 should be isolated from the load capacitance with a 100 Ω resistor.

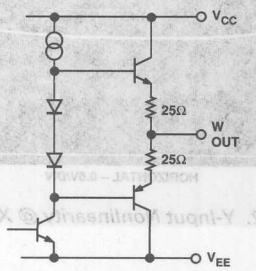

Figure 5. Equivalent Circuit for MLT04 Output Stages

ANALOG MULTIPLIER ERROR SOURCES

Multiplier errors consist primarily of input and output offsets, scale factor errors, and nonlinearity in the multiplying core. An expression for the output of a *real* analog multiplier is given by:

$$V_O = (K + \Delta K)\{(V_X + X_{OS})(V_Y + Y_{OS}) + Z_{OS} + f(X, Y)\}$$

where:
- K = Multiplier Scale Factor
- ΔK = Scale Factor Error
- V_X = X-Input Signal
- X_{OS} = X-Input Offset Voltage
- V_Y = Y-Input Signal
- Y_{OS} = Y-Input Offset Voltage
- Z_{OS} = Multiplier Output Offset Voltage
- $f(X, Y)$ = Nonlinearity

Executing the algebra to simplify the above expression yields expressions for all the errors in an analog multiplier:

Term	Description	Dependence on Input
KV_XV_Y	True Product	Goes to Zero As Either or Both Inputs Go to Zero
ΔKV_YV_Y	Scale-Factor Error	Goes to Zero at V_X, $V_Y = 0$
V_XY_{OS}	Linear "X" Feedthrough Due to Y-Input Offset	Proportional to V_X
V_YX_{OS}	Linear "Y" Feedthrough Due to X-Input Offset	Proportional to V_Y
$X_{OS}Y_{OS}$	Output Offset Due to X-, Y-Input Offsets	Independent of V_X, V_Y
Z_{OS}	Output Offset	Independent of V_X, V_Y
$f(X, Y)$	Nonlinearity	Depends on Both V_X, V_Y. Contains Terms Dependent on V_X, V_Y, Their Powers and Cross Products

As shown in the table, the primary static errors in an analog multiplier are input offset voltages, output offset voltage, scale factor, and nonlinearity. Of the four sources of error, only two are externally trimmable in the MLT04: the X- and Y-input offset voltages. Output offset voltage in the MLT04 is factory-trimmed to ±50 mV, and the scale factor is internally adjusted to ±2.5% of full scale. Input offset voltage errors can be eliminated by using the optional trim circuit of Figure 6. This scheme then reduces the net error to output offset, scale-factor (gain) error, and an irreducible nonlinearity component in the multiplying core.

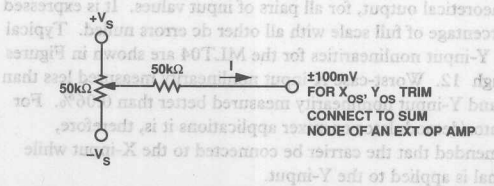

Figure 6. Optional Offset Voltage Trim Configuration

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will "feedthrough" the multiplier and appear at the output. This is caused by the product of the nonzero input and the offset voltage of the "zero" input. Introducing an offset equal to and opposite of the "zero" input offset voltage will null the linear component of the feedthrough. Residual feedthrough at the output of the multiplier is then irreducible core nonlinearity.

Typical X- and Y-input feedthrough curves for the MLT04 are shown in Figures 7 and 8, respectively. These curves illustrate MLT04 feedthrough after "zero" input offset voltage trim. Residual X-input feedthrough measures 0.08% of full scale, whereas residual Y-input feedthrough is almost immeasurable.

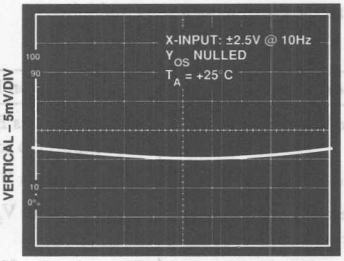

Figure 7. X-Input Feedthrough with Y_{OS} Nulled

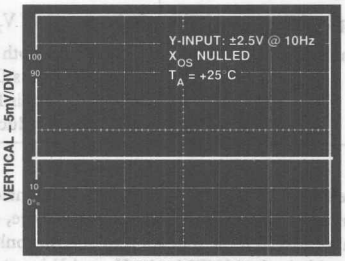

Figure 8. Y-Input Feedthrough with X_{OS} Nulled

Nonlinearity

Multiplier core nonlinearity is the irreducible component of error. It is the difference between actual performance and "best-straight-line" theoretical output, for all pairs of input values. It is expressed as a percentage of full scale with all other dc errors nulled. Typical X- and Y-input nonlinearities for the MLT04 are shown in Figures 9 through 12. Worst-case X-input nonlinearity measured less than 0.2%, and Y-input nonlinearity measured better than 0.06%. For modulator/demodulator or mixer applications it is, therefore, recommended that the carrier be connected to the X-input while the signal is applied to the Y-input.

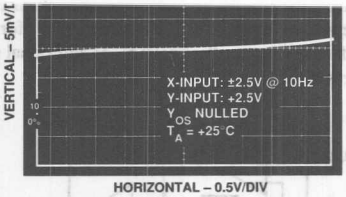

Figure 9. X-Input Nonlinearity @ Y = +2.5 V

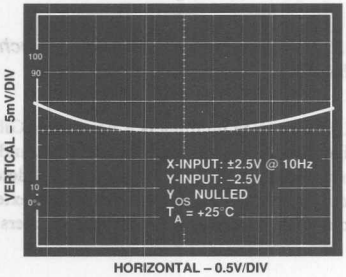

Figure 10. X-Input Nonlinearity @ Y = –2.5 V

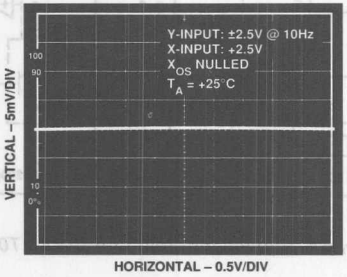

Figure 11. Y-Input Nonlinearity @ X = +2.5 V

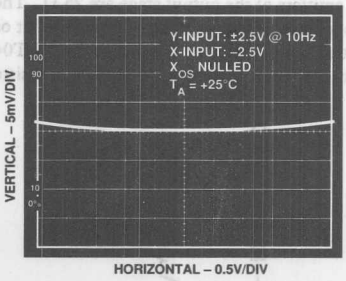

Figure 12. Y-Input Nonlinearity @ X = –2.5 V

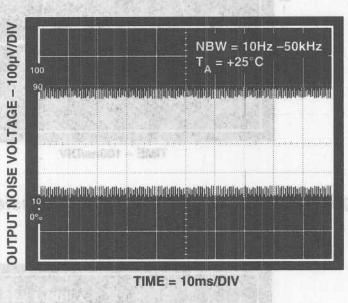

Figure 13. Broadband Noise

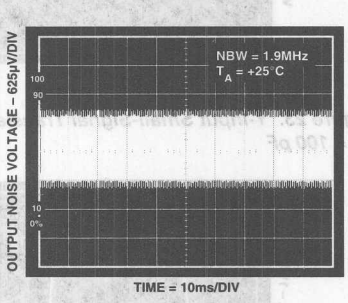

Figure 14. Broadband Noise

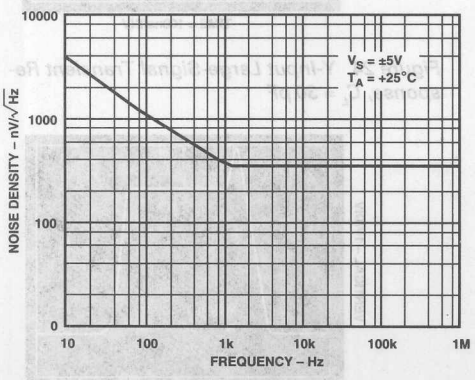

Figure 15. Noise Density vs. Frequency

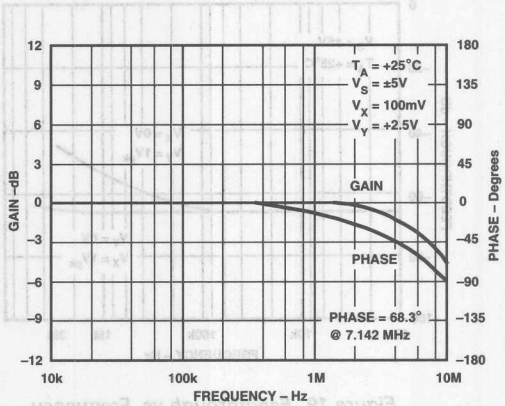

Figure 16. X-Input Gain and Phase vs. Frequency

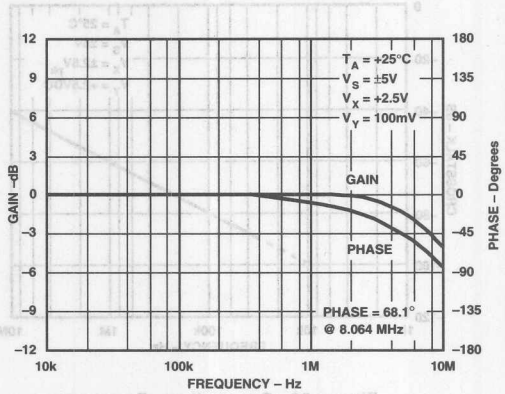

Figure 17. Y-Input Gain and Phase vs. Frequency

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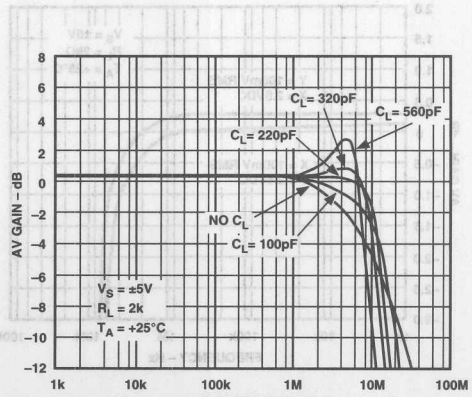

Figure 18. Amplitude Response vs. Capacitive Load

MLT04 – Typical Performance Characteristics

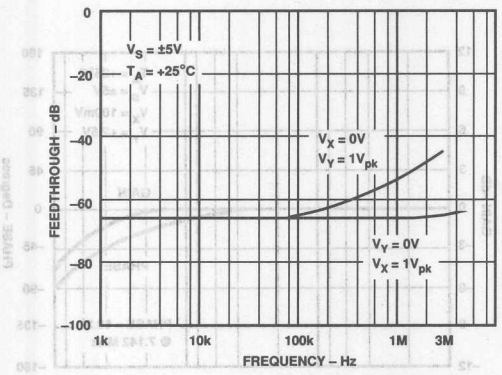

Figure 19. Feedthrough vs. Frequency

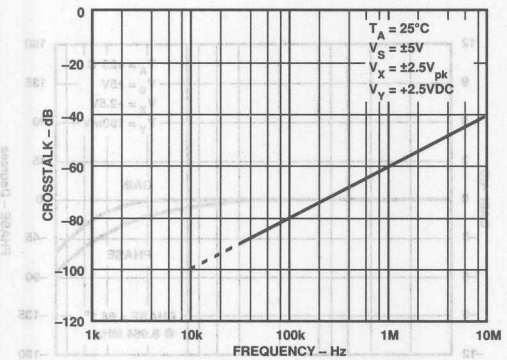

Figure 20. Crosstalk vs. Frequency

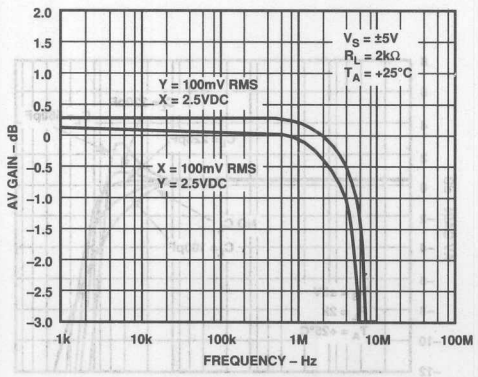

Figure 21. Gain Flatness vs. Frequency

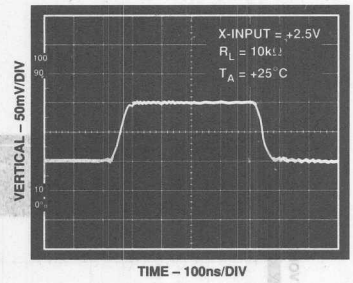

Figure 22. Y-Input Small-Signal Transient Response, C_L = 30 pF

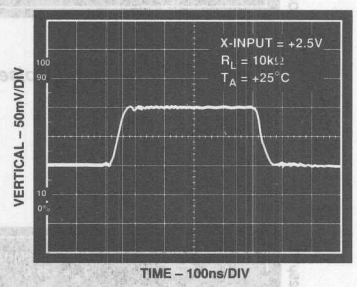

Figure 23. Y-Input Small-Signal Transient Response, C_L = 100 pF

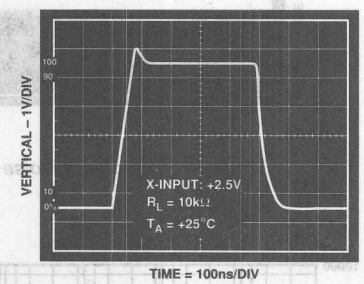

Figure 24. Y-Input Large-Signal Transient Response, C_L = 30 pF

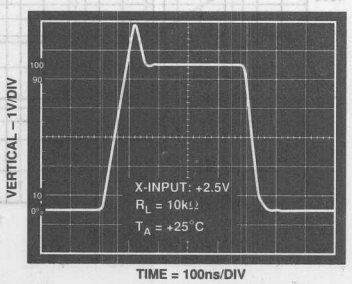

Figure 25. Y-Input Large-Signal Transient Response, C_L = 100 pF

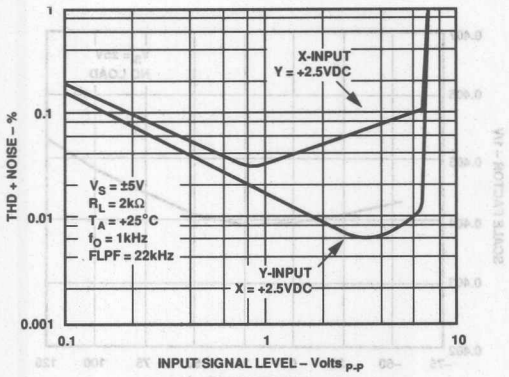

Figure 26. THD + Noise vs. Input Signal Level

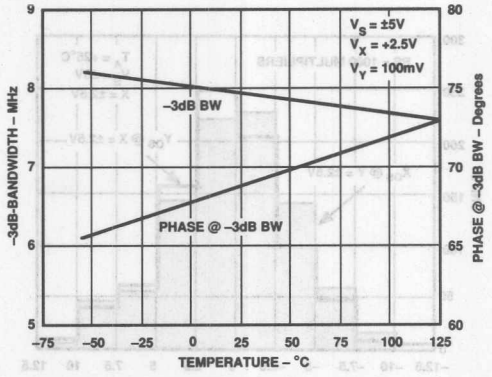

Figure 29. Y-Input Gain Bandwidth vs. Temperature

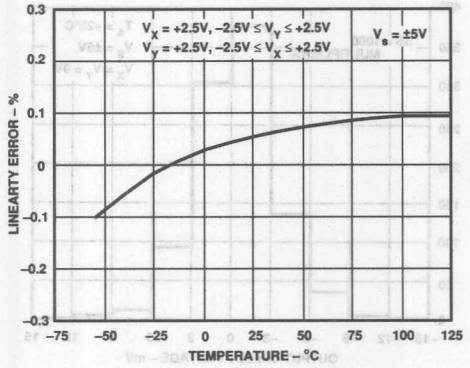

Figure 27. Linearity Error vs. Temperature

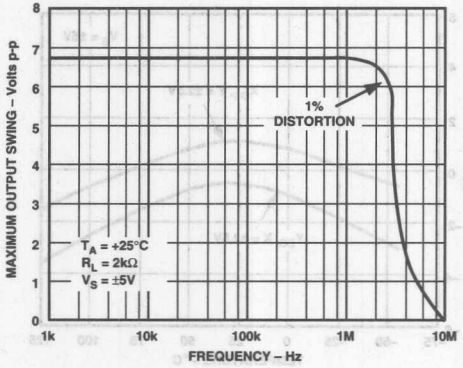

Figure 30. Maximum Output Swing vs. Frequency

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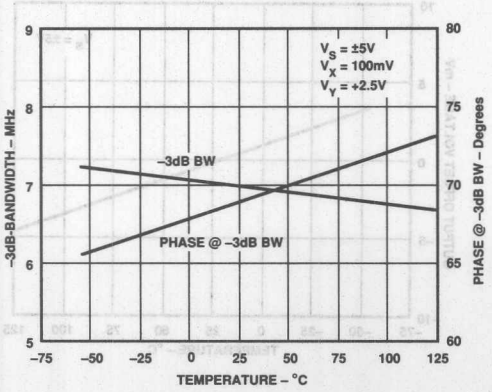

Figure 28. X-Input Gain Bandwidth vs. Temperature

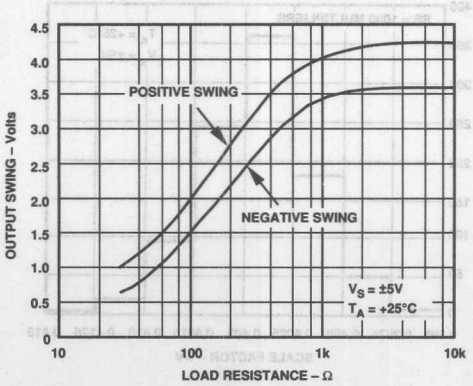

Figure 31. Maximum Output Swing vs. Resistive Load

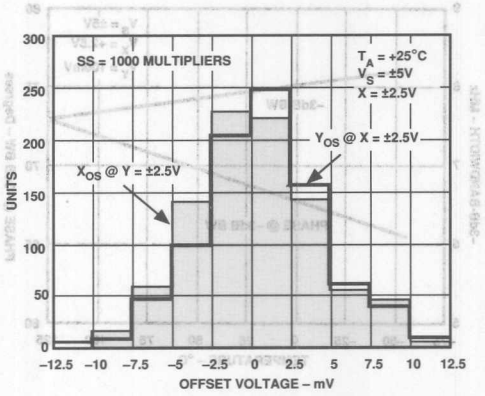

Figure 32. Offset Voltage Distribution

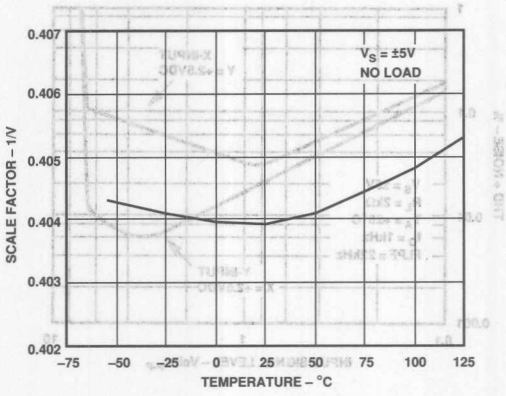

Figure 35. Scale Factor vs. Temperature

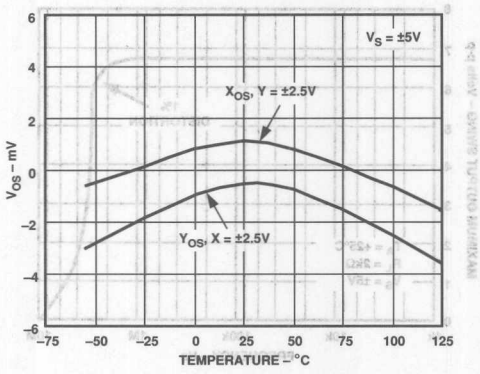

Figure 33. Offset Voltage vs. Temperature

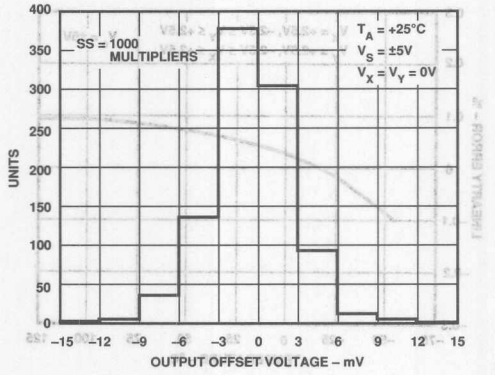

Figure 36. Output Offset Voltage (Z_{OS}) Distribution

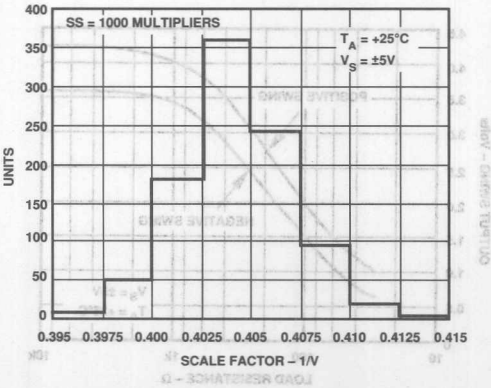

Figure 34. Scale Factor Distribution

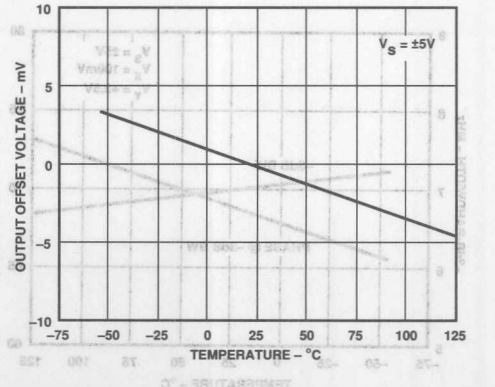

Figure 37. Output Offset Voltage (Z_{OS}) vs. Temperature

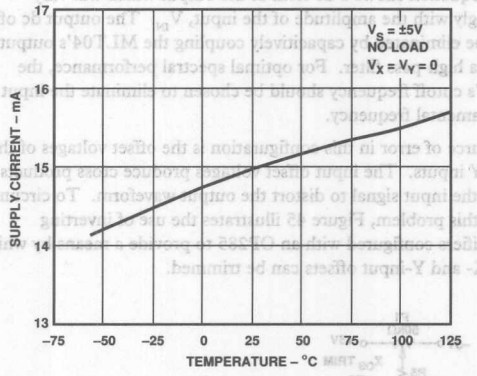

Figure 38. Supply Current vs. Temperature

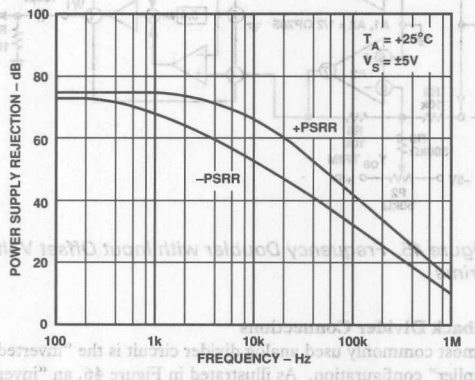

Figure 39. Power Supply Rejection vs. Frequency

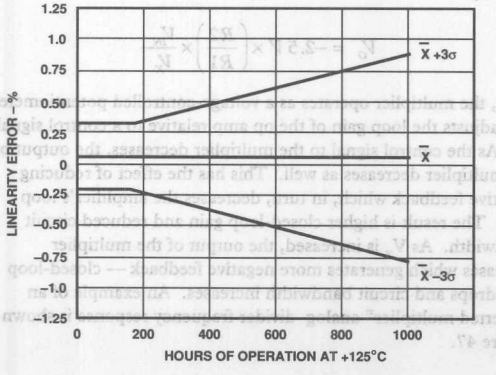

Figure 40. Linearity Error (LE) Distribution Accelerated by Burn-in

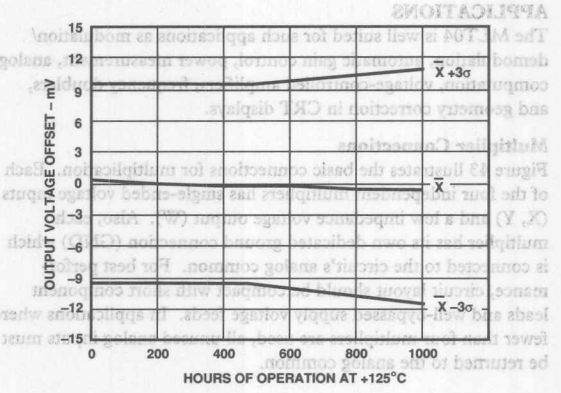

Figure 41. Output Voltage Offset (Z_{OS}) Distribution Accelerated by Burn-in

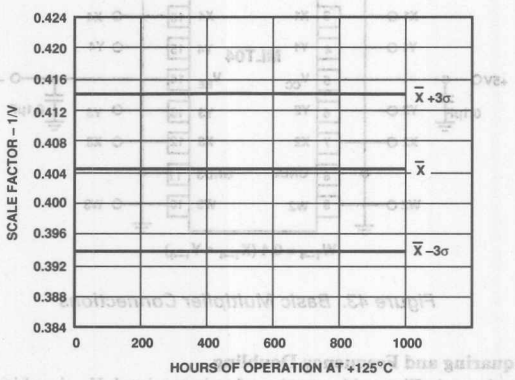

Figure 42. Scale Factor (K) Distribution Accelerated by Burn-in

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demodulation, automatic gain control, power measurement, analog computation, voltage-controlled amplifiers, frequency doublers, and geometry correction in CRT displays.

Multiplier Connections

Figure 43 illustrates the basic connections for multiplication. Each of the four independent multipliers has single-ended voltage inputs (X, Y) and a low impedance voltage output (W). Also, each multiplier has its own dedicated ground connection (GND) which is connected to the circuit's analog common. For best performance, circuit layout should be compact with short component leads and well-bypassed supply voltage feeds. In applications where fewer than four multipliers are used, all unused analog inputs must be returned to the analog common.

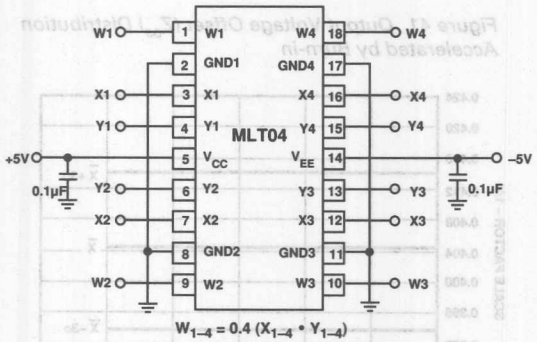

Figure 43. Basic Multiplier Connections

Squaring and Frequency Doubling

As shown in Figure 44, squaring of an input signal, V_{IN}, is achieved by connecting the X-and Y-inputs in parallel to produce an output of $V_{IN}^2/2.5$ V. The input may have either polarity, but the output will be positive.

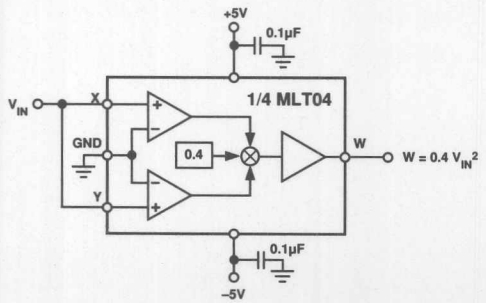

Figure 44. Connections for Squaring

When the input is a sine wave given by V_{IN} sin ωt, the squaring circuit behaves as a frequency doubler because of the trigonometric identity:

$$\frac{(V_{IN}\ \sin\omega t)^2}{2.5V} = \frac{V_{IN}^2}{2.5V}\left(\frac{1}{2}\right)(1-\cos 2\omega t)$$

can be eliminated by capacitively coupling the MLT04's output with a high-pass filter. For optimal spectral performance, the filter's cutoff frequency should be chosen to eliminate the input fundamental frequency.

A source of error in this configuration is the offset voltages of the X and Y inputs. The input offset voltages produce cross products with the input signal to distort the output waveform. To circumvent this problem, Figure 45 illustrates the use of inverting amplifiers configured with an OP285 to provide a means by which the X- and Y-input offsets can be trimmed.

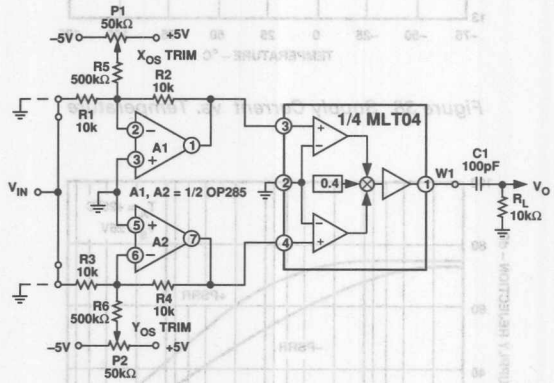

Figure 45. Frequency Doubler with Input Offset Voltage Trims

Feedback Divider Connections

The most commonly used analog divider circuit is the "inverted multiplier" configuration. As illustrated in Figure 46, an "inverted multiplier" analog divider can be configured with a multiplier operating in the feedback loop of an operational amplifier. The general form of the transfer function for this circuit configuration is given by:

$$V_O = -2.5\,V \times \left(\frac{R2}{R1}\right) \times \frac{V_{IN}}{V_X}$$

Here, the multiplier operates as a voltage-controlled potentiometer that adjusts the loop gain of the op amp relative to a control signal, V_X. As the control signal to the multiplier decreases, the output of the multiplier decreases as well. This has the effect of reducing negative feedback which, in turn, decreases the amplifier's loop gain. The result is higher closed-loop gain and reduced circuit bandwidth. As V_X is increased, the output of the multiplier increases which generates more negative feedback — closed-loop gain drops and circuit bandwidth increases. An example of an "inverted multiplier" analog divider frequency response is shown in Figure 47.

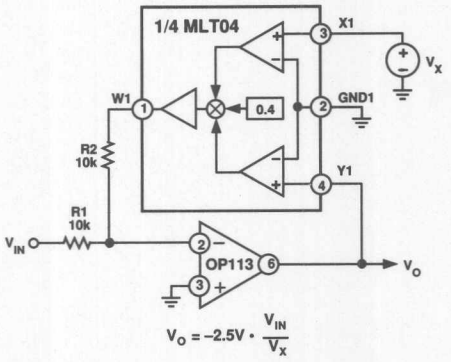

Figure 46. "Inverted-Multiplier" Configuration for Analog Division

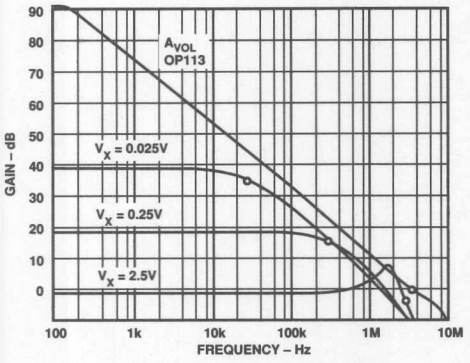

Figure 47. Signal-Dependent Feedback Makes Variables Out of Amplifier Bandwidth and Stability

Although this technique works well with almost any operational amplifier, there is one caveat: for best circuit stability, the unity-gain crossover frequency of the operational amplifier should be equal to or less than the MLT04's 8 MHz bandwidth.

Connection for Square Rooting

Another application of the "inverted multiplier" configuration is the square-root function. As shown in Figure 48, both inputs of the MLT04 are wired together and are used as the output of the circuit. Because the circuit configuration exhibits the following generalized transfer function:

$$V_O = \sqrt{-2.5 \times \left(\frac{R2}{R1}\right) \times V_{IN}}$$

the input signal voltage is limited to the range $-2.5\ V \le V_{IN} < 0$. To prevent circuit latchup due to positive feedback or input signal polarity reversal, a 1N4148-type junction diode is used in series with the output of the multiplier.

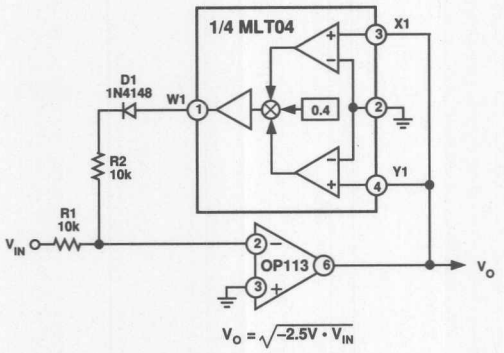

Figure 48. Connections for Square Rooting

Voltage-Controlled Low-Pass Filter

The circuit in Figure 49 illustrates how to construct a voltage-controlled low-pass filter with an analog multiplier. The advantage with this approach over conventional active-filter configurations is that the overall characteristic cut-off frequency, ω_O, will be directly proportional to a multiplying input voltage. This permits the construction of filters in which the capacitors are adjustable (directly or inversely) by a control voltage. Hence, the frequency scale of a filter can be manipulated by means of a single voltage without affecting any other parameters. The general form of the circuit's transfer function is given by:

$$\frac{V_O}{V_{IN}} = -\left(\frac{R2}{R1}\right)\left\{\frac{1}{s\left(\frac{R2+R1}{R1}\right)\left(\frac{2.5RC}{V_X}\right)+1}\right\}$$

In this circuit, the ratio of R2 to R1 sets the passband gain, and the break frequency of the filter, ω_{LP}, is given by:

$$\omega_{LP} = \left(\frac{R1}{R1+R2}\right)\left(\frac{V_X}{2.5RC}\right)$$

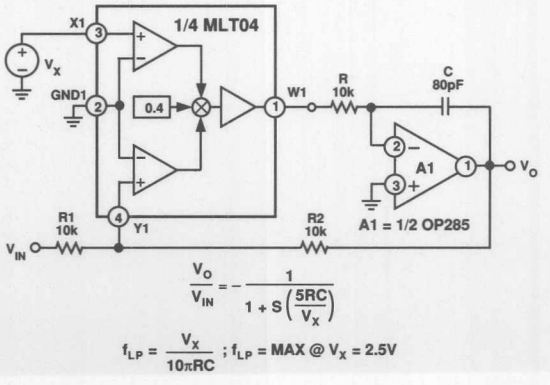

Figure 49. A Voltage-Controlled Low-Pass Filter

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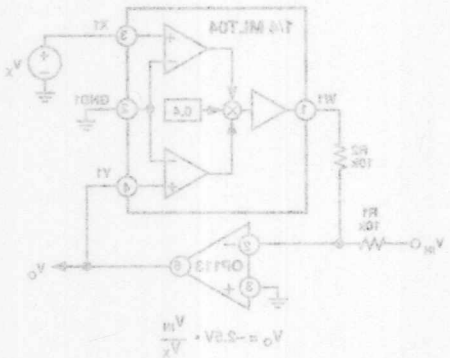


Figure 46. "Inverted-Multiplier" Configuration for Analog Division

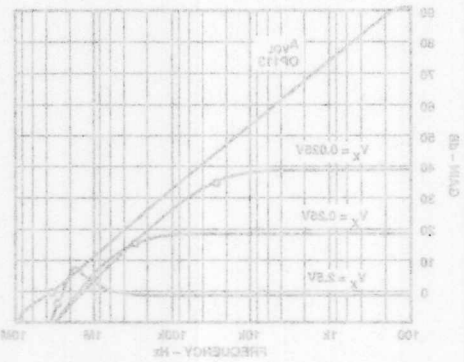


Figure 47. Signal-Dependent Feedback Makes Variables Out of Amplifier Bandwidth and Stability

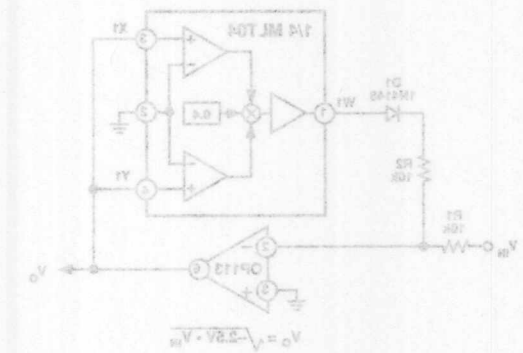
Although this technique works well with almost any operational amplifier, there is one caveat: for best circuit stability, the unity-gain crossover frequency of the operational amplifier should be equal to or less than the ML1704's 8 MHz bandwidth.

Connection for Square Rooting

Another application of the "inverted multiplier" configuration is the square-root function. As shown in Figure 48, both inputs of the ML1704 are wired together and are used as the output of the circuit. Because the circuit configuration exhibits the following generalized transfer function:

$$V_O = \sqrt{-2.5 \times \left(\frac{R2}{R1}\right) \times V_{IN}}$$

the input signal voltage is limited to the range $-2.5\ V \geq V_{IN} < 0$. To prevent circuit latching due to positive feedback or input signal polarity reversal, a 1N4148-type junction diode is used in series with the output of the multiplier.



$$V_O = \sqrt{-2.5V \cdot V_{IN}}$$

Figure 48. Connections for Square Rooting

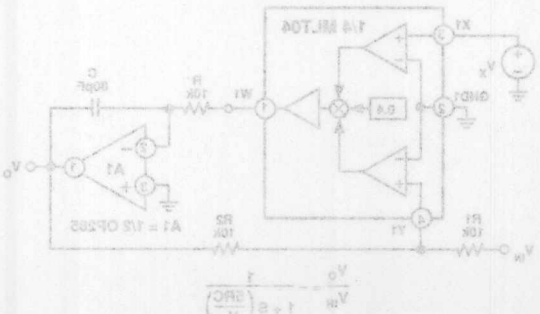
Voltage-Controlled Low-Pass Filter

The circuit in Figure 49 illustrates how to construct a voltage-controlled low-pass filter with an analog multiplier. The advantage with this approach over conventional active-filter configurations is that the overall characteristic cut-off frequency, ω_{Ch}, will be directly proportional to a multiplying input voltage. This permits the construction of filters in which the capacitors are adjustable (directly or inversely) by a control voltage. Hence, the frequency scale of a filter can be manipulated by means of a single voltage without affecting any other parameters. The general form of the circuit's transfer function is given by:

$$\frac{V_O}{V_{IN}} = \left\{\frac{1}{\left(\frac{R2 + R1}{R1}\right)\left(\frac{2.5RC}{V_X}\right)^2 + 1}\right\}\left(\frac{R2}{R1}\right)$$

In this circuit, the ratio of R2 to R1 sets the passband gain, and the break frequency of the filter, ω_{Ch}, is given by:

$$\omega_{Ch} = \left(\frac{R1}{R1 + R2}\right)\left(\frac{V_X}{2.5RC}\right)$$



$$\frac{V_O}{V_{IN}} = \frac{-1}{1 + s\left(\frac{2.5RC}{V_X}\right)^2}$$

$$f_{Ch} = \frac{V_X}{10\pi RC}\ ;\ f_{Ch} = \text{MAX @ } V_X = 2.5V$$

Figure 49. A Voltage-Controlled Low-Pass Filter

RMS-to-DC Converters
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AD736 – Low Cost, Low Power, True RMS-to-DC Converter	18–14
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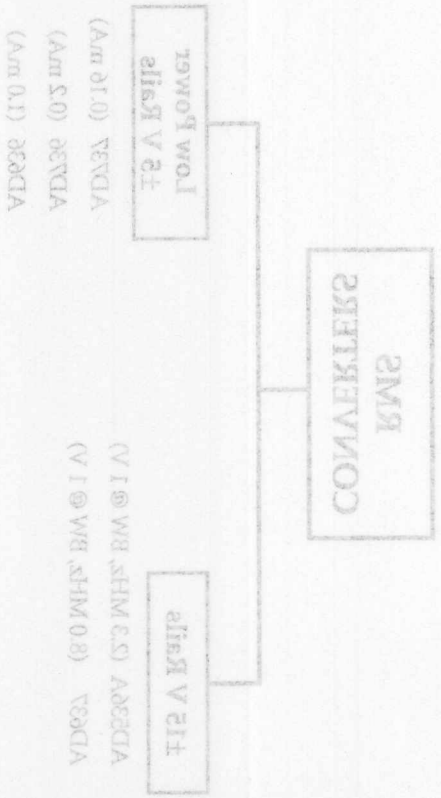
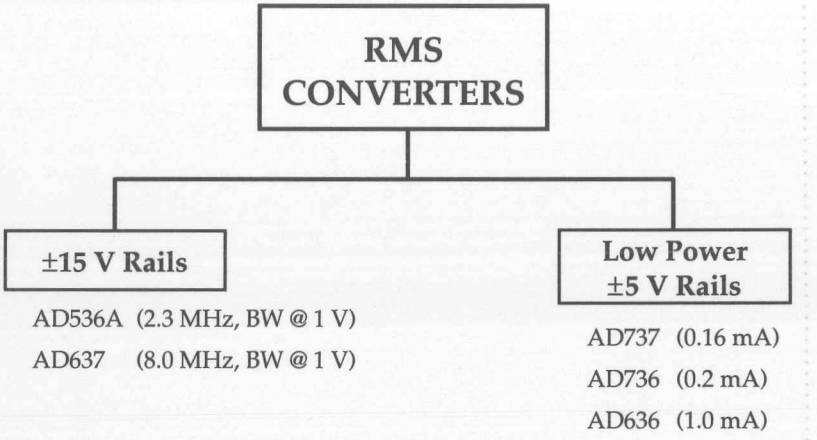


Selection Tree — RMS-to-DC Converters



Selection Guide—RMS-to-DC Converters

Model	Conversion Accuracy mV ±%Read max	Full-Scale Range V RMS	dB Output Error dB max	Package Options[1]	Temp Ranges[2]	Comments	Page
AD737	(0.2±0.3)–(0.4±0.5)	0.2		N, Q, R	C, I	Low Cost, Low Power, Power Down	18–17
AD736	(0.3±0.3)–(0.5±0.5)	0.2		N, Q, R	C, I	General Purpose, Low Cost, Low Power	18–14
AD636	(0.2±0.3)–(0.5±0.6)	0.2	0.2–0.5	D, H	C	Low Power	18–8
AD637	(0.5±0.2)–(1±0.5)	7	0.3 (typ)	D, Q, R	C, $M/_D$	High Accuracy, Wide Bandwidth	18–11
AD536A	(2±0.2)–(5±0.5)	7	0.3–0.6	D, E, H, Q	C, M/	General Purpose	18–5

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
Boldface Type: Data sheet information in this volume.

Selection Guide — RMS-to-DC Converters

Model	Conversion Accuracy ±%Reading ±mV max	Bandwidth (-3dB) Full-Scale Range V RMS	Output Noise mV rms	Response Time to 99% Final Value	Comments	Page
AD536A	(0.2±0.3)+(0.4±0.5)	0.2	N, H, D, E, R, G	1 sec, Low Cost, Low Power		18-12
AD637	(0.02±0.3)+(0.2±0.5)	7	0.3 (typ)	0.2-0.5	Wide Bandwidth, Accuracy, Low Power	18-8
AD638	(0.2±0.3)+(0.2±0.5)	0.2	0.3 (typ)	0.2-0.5	Low Power	18-8
AD736	(0.2±0.3)+(0.3±0.5)	0.2	N, H, D, E, R, G	1 sec, Low Cost, Low Power		18-14
AD737	(0.2±0.3)+(1±0.5)	7	0.3 (typ)	0.2-0.5	Wide Bandwidth, Accuracy, Low Power	18-8
AD8436	(5±0.5)+(5±0.5)	7	0.3-0.6	0.3-0.6	General Purpose	18-5

Package Options: D = Hermetic DIP, Ceramic w/Metal Lid; E = CerDIP, Ceramic w/Glass Lid; H = Hermetic Metal Can; N = Plastic DIP; R = SOIC; G = Ceramic Leadless Chip Carrier.
N = Plastic Mini-DIP; Q = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC; Surface Mount Plastic Package; Z = Ceramic Leaded Chip Carrier.
Chip Topside: ST = Thin Oxide Passivation; T = TiO2-Si3N4-Thin Oxide Passivation; W = Nichrome Thin Film; Y = Silicon Nitride Passivation.
Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, -40°C to +85°C; M = Military, -55°C to +125°C. If a device has multiple grade options, the most commonly available grade will be displayed first. For complete specifications, see the Data Conversion/Acquisition Databook, 1st Edition, 1992, or the 1993 Data Conversion/Acquisition Databook, 2nd Edition, 1993, and the Military Databook, 1st Edition, 1992.

Integrated Circuit, True RMS-to-DC Converter

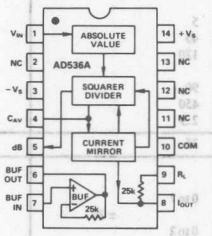
AD536A

FEATURES

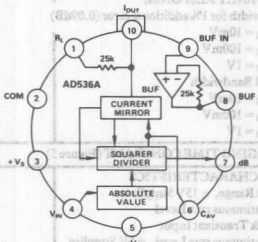
- True RMS-to-DC Conversion
- Laser-Trimmed to High Accuracy
  - 0.2% max Error (AD536AK)
  - 0.5% max Error (AD536AJ)
- Wide Response Capability:
  - Computes RMS of AC and DC Signals
  - 450kHz Bandwidth: $V_{rms} > 100mV$
  - 2MHz Bandwidth: $V_{rms} > 1V$
  - Signal Crest Factor of 7 for 1% Error
- dB Output with 60dB Range
- Low Power: 1.2mA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- −55°C to +125°C Operation (AD536AS)

PIN CONFIGURATIONS AND FUNCTIONAL BLOCK DIAGRAMS

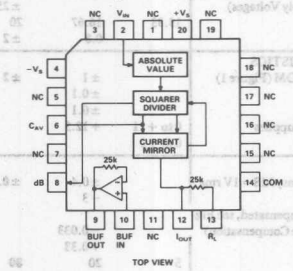
TO-116 (D-14) and Q-14 Packages



TO-100 (H-10A) Package



LCC (E-20A) Package



PRODUCT DESCRIPTION

The AD536A is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300kHz with 3dB error for signal levels above 100mV.

An important feature of the AD536A not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60 dB. Using an externally supplied reference current, the 0dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536A is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal error), and full-scale accuracy at 7V rms. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J, K) for commercial temperature range (0 to +70°C) applications, and one grade (S) rated for the −55°C to +125°C extended range. The AD536AK offers a maximum total error of ±2mV ±0.2% of reading, and the AD536AJ and AD536AS have maximum errors of ±5mV ±0.5% of reading. All three versions are available in either a hermetically sealed 14-pin DIP or 10-pin TO-100 metal can. The AD536AS is also available in a 20-pin hermetically sealed ceramic leadless chip carrier.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536A allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.
4. The AD536A will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The one milliampere quiescent supply current makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. The AD536A directly replaces the AD536 and provides improved bandwidth and temperature drift specifications.

TRANSFER FUNCTION	$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Figure 1)			±5 ±0.5			±2 ±0.2			±5 ±0.5	mV ± % of Reading
vs. Temperature, T_{min} to +70°C			±0.1 ±0.01			±0.05 ±0.005			±0.1 ±0.005	mV ± % of Reading/°C
+70°C to +125°C									±0.3 ±0.005	mV ± % of Reading/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading/V
dc Reversal Error		±0.2			±0.1			±0.2		± % of Reading
Total Error, External Trim[1] (Figure 2)		±3 ±0.3			±2 ±0.1			±3 ±0.3		mV ± % of Reading
ERROR VS. CREST FACTOR[2]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		−0.1			−0.1			−0.1		% of Reading
Crest Factor = 7		−1.0			−1.0			−1.0		% of Reading
FREQUENCY RESPONSE[3]										
Bandwidth for 1% additional error (0.09dB)										
V_{IN} = 10mV		5			5			5		kHz
V_{IN} = 100mV		45			45			45		kHz
V_{IN} = 1V		120			120			120		kHz
± 3dB Bandwidth										
V_{IN} = 10mV		90			90			90		kHz
V_{IN} = 100mV		450			450			450		kHz
V_{IN} = 1V		2.3			2.3			2.3		MHz
AVERAGING TIME CONSTANT (Figure 5)		25			25			25		ms/μF CAV
INPUT CHARACTERISTICS										
Signal Range, ± 15V Supplies										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±20			±20			±20	V peak
Continuous rms Level, ± 5V Supplies		0 to 2			0 to 2			0 to 2		V rms
Peak Transient Input, ± 5V Supplies			±7			±7			±7	V peak
Maximum Continuous Nondestructive Input Level (All Supply Voltages)			±25			±25			±25	V peak
Input Resistance	13.33	16.67	20	13.33	16.67	20	13.33	16.67	20	kΩ
Input Offset Voltage		0.8	±2		0.5	±1		0.8	±2	mV
OUTPUT CHARACTERISTICS										
Offset Voltage, V_{IN} = COM (Figure 1)		±1	±2		±0.5	±1		±2		mV
vs. Temperature		±0.1			±0.1			±0.2		mV/°C
vs. Supply Voltage		±0.1			±0.1			±0.2		mV/V
Voltage Swing, ± 15V Supplies	0 to +11	+12.5		0 to +11	+12.5		0 to +11	+12.5		V
± 5V Supply	0 to +2			0 to +2			0 to +2			V
dB OUTPUT (Figure 13)										
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±0.4	±0.6		±0.2	±0.3		±0.5	±0.6	dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor TC (Uncompensated, see Figure 1 for Temperature Compensation)		−0.033			−0.033			−0.033		dB/°C
		+0.33			+0.33			+0.33		% of Reading/°C
I_{REF} for 0dB = 1V rms	5	20	80	5	20	80	5	20	80	μA
I_{REF} Range	1		100	1		100	1		100	μA
I_{OUT} TERMINAL										
I_{OUT} Scale Factor		40			40			40		μA/V rms
I_{OUT} Scale Factor Tolerance		±10	±20		±10	±20		±10	±20	%
Output Resistance	20	25	30	20	25	30	20	25	30	kΩ
Voltage Compliance		$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5)			$-V_S$ to ($+V_S$ −2.5V)		V
BUFFER AMPLIFIER										
Input and Output Voltage Range	$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)			V
Input Offset Voltage, R_S = 25k		±0.5	±4		±0.5	±4		±0.5	±4	mV
Input Bias Current		20	60		20	60		20	60	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5mA, −130μA)			(+5mA, −130μA)			(+5mA, −130μA)			
Short Circuit Current		20			20			20		mA
Output Resistance			0.5			0.5			0.5	Ω
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[4]		5			5			5		V/μs
POWER SUPPLY										
Voltage Rated Performance		±15			±15			±15		V
Dual Supply	±3.0		±18	±3.0		±18	±3.0		±18	V
Single Supply	+5		+36	+5		+36	+5		+36	V
Quiescent Current										
Total V_S, 5V to 36V, T_{min} to T_{max}		1.2	2		1.2	2		1.2	2	mA
TEMPERATURE RANGE										
Rated Performance	0		+70	0		+70	−55		+125	°C
NUMBER OF TRANSISTORS		65			65			65		

NOTES

[1]Accuracy is specified for 0 to 7V rms, dc or 1kHz sinewave input with the AD536A connected as in the figure referenced.

[2]Error vs. crest factor is specified as an additional error for 1V rms rectangular pulse input, pulse width = 200μs.

[3]Input voltages are expressed in volts rms, and error is percent of reading.

[4]With 2k external pulldown resistor.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage
- Dual Supply . . . . . ±18V
- Single Supply . . . . . +36V

Internal Power Dissipation[2] 500mW
Maximum Input Voltage . . . . . ±25V Peak
Buffer Maximum Input Voltage . . . . . $\pm V_S$
Maximum Input Voltage . . . . . ±25V Peak
Storage Temperature Range . . . . . −55°C to +150°C
Operating Temperature Range
- AD536AJ/K . . . . . 0°C to +70°C
- AD536AS . . . . . −55°C to +125°C

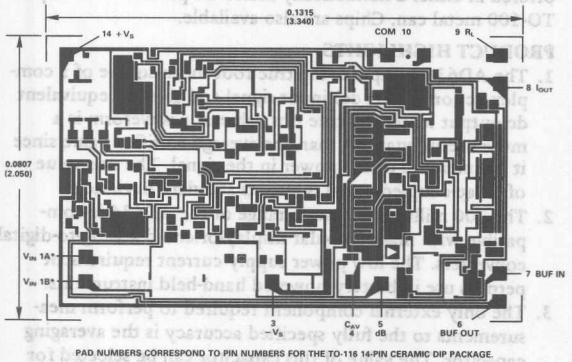
Lead Temperature Range
- (Soldering 60 sec) . . . . . 300°C

ESD Rating . . . . . 1000 V

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]10-Pin Header: θ_{JA} = 150°C/W
20-Pin LCC: θ_{JA} = 95°C/W
14-Pin Size Brazed Ceramic DIP: θ_{JA} = 95°C/W

CHIP DIMENSIONS AND PAD LAYOUT

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-116 14-PIN CERAMIC DIP PACKAGE.

NOTE
*BOTH PADS SHOWN MUST BE CONNECTED TO V_{IN}.
THE AD536A IS AVAILABLE IN LASER TRIMMED CHIP FORM.
SUBSTRATE CONNECTED TO $-V_S$.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD536AJD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD536AKD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD536AJH	0°C to +70°C	Header	H-10A
AD536AKH	0°C to +70°C	Header	H-10A
AD536AJQ	0°C to +70°C	Cerdip	Q-14
AD536AKQ	0°C to +70°C	Cerdip	Q-14
AD536ASD	−55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD536ASD/883B	−55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD536ASE	−55°C to +125°C	LCC	E-20A
AD536ASE/883B	−55°C to +125°C	LCC	E-20A
AD536ASH	−55°C to +125°C	Header	H-10A
AD536ASH/883B	−55°C to +125°C	Header	H-10A

NOTES
[1]"S" grade chips are available tested at +25°C and +125°C. "J" grade chips are also available.
[2]For outline information see Package Information section.

STANDARD CONNECTION

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%; at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with the input, as shown in Figure 3, the capacitor must be nonpolar. If the AD536A is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible.

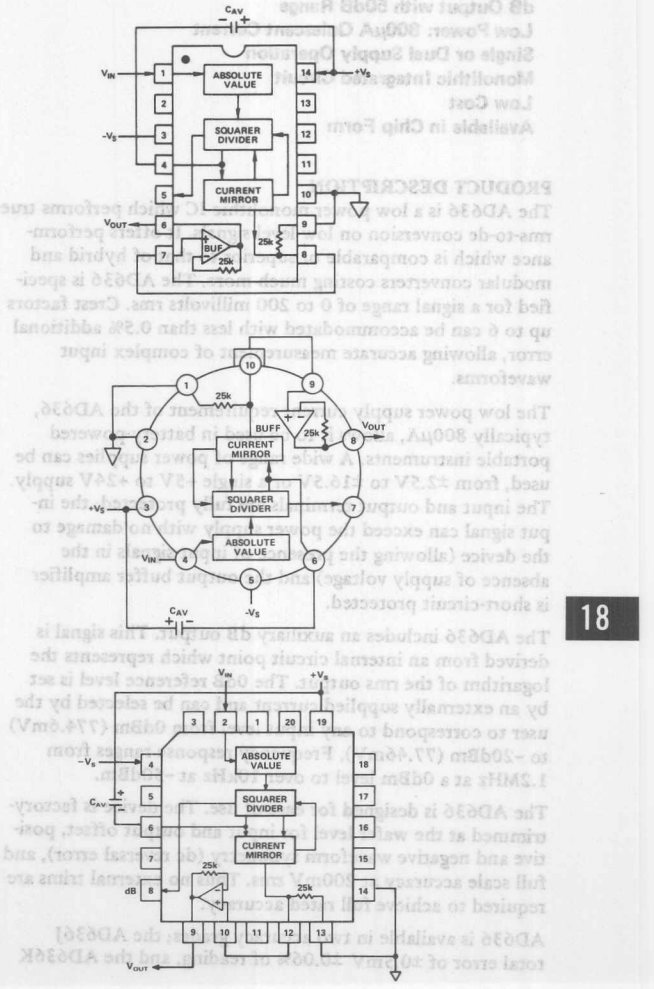


Figure 1. Standard RMS Connection

Low Level, True RMS-to-DC Converter

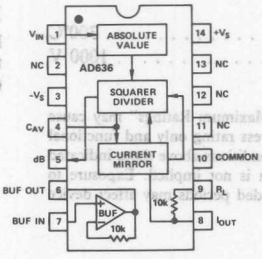
AD636

FEATURES

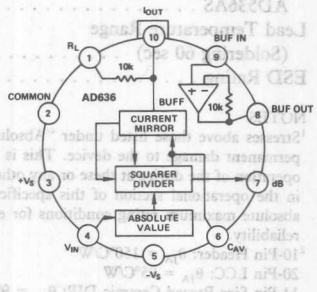
- True rms-to-dc Conversion
- 200mV Full Scale
- Laser-Trimmed to High Accuracy
  - 0.5% max Error (AD636K)
  - 1.0% max Error (AD636J)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 1MHz -3dB Bandwidth: V_{rms}>100mV
  - Signal Crest Factor of 6 for 0.5% Error
- dB Output with 50dB Range
- Low Power: 800μA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- Low Cost
- Available in Chip Form

PIN CONNECTIONS & FUNCTIONAL BLOCK DIAGRAM

"D" Package (TO-116)



"H" Package (TO-100)



PRODUCT DESCRIPTION

The AD636 is a low power monolithic IC which performs true rms-to-dc conversion on low level signals. It offers performance which is comparable or superior to that of hybrid and modular converters costing much more. The AD636 is specified for a signal range of 0 to 200 millivolts rms. Crest factors up to 6 can be accommodated with less than 0.5% additional error, allowing accurate measurement of complex input waveforms.

The low power supply current requirement of the AD636, typically 800μA, allows it to be used in battery-powered portable instruments. A wide range of power supplies can be used, from ±2.5V to ±16.5V or a single +5V to +24V supply. The input and output terminals are fully protected; the input signal can exceed the power supply with no damage to the device (allowing the presence of input signals in the absence of supply voltage) and the output buffer amplifier is short-circuit protected.

The AD636 includes an auxiliary dB output. This signal is derived from an internal circuit point which represents the logarithm of the rms output. The 0dB reference level is set by an externally supplied current and can be selected by the user to correspond to any input level from 0dBm (774.6mV) to -20dBm (77.46mV). Frequency response ranges from 1.2MHz at a 0dBm level to over 10kHz at -50dBm.

The AD636 is designed for ease of use. The device is factory-trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal error), and full scale accuracy at 200mV rms. Thus no external trims are required to achieve full rated accuracy.

AD636 is available in two accuracy grades; the AD636J total error of ±0.5mV ±0.06% of reading, and the AD636K is accurate within ±0.2mV to ±0.03% of reading. Both versions are specified for the 0 to +70°C temperature range, and are offered in either a hermetically sealed 14-pin DIP or a 10-pin TO-100 metal can. Chips are also available.

PRODUCT HIGHLIGHTS

1. The AD636 computes the true root-mean-square of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it is a measure of the power in the signal. The rms value of an ac-coupled signal is also its standard deviation.
2. The 200 millivolt full scale range of the AD636 is compatible with many popular display-oriented analog-to-digital converters. The low power supply current requirement permits use in battery-powered hand-held instruments.
3. The only external component required to perform measurements to the fully specified accuracy is the averaging capacitor. The value of this capacitor can be selected for the desired trade-off of low frequency accuracy, ripple, and settling time.
4. The on-chip buffer amplifier can be used to buffer either the input or the output. Used as an input buffer, it provides accurate performance from standard 10MΩ input attenuators. As an output buffer, it can supply up to 5 milliamps of output current.
5. The AD636 will operate over a wide range of power supply voltages, including single +5V to +24V or split ±2.5V to ±16.5V sources. A standard 9V battery will provide several hundred hours of continuous operation.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C, and $+V_S = +3V$, $-V_S = -5V$ unless otherwise noted)

Model	AD636J Min	AD636J Typ	AD636J Max	AD636K Min	AD636K Typ	AD636K Max	Units
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY							
Total Error, Internal Trim[1,2]			±0.5 ±1.0			±0.2 ±0.5	mV ± % of Reading
vs. Temperature, 0 to +70°C			±0.1 ±0.01			±0.1 ±0.005	mV ± % of Reading/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading/V
dc Reversal Error at 200mV		±0.2			±0.1		% of Reading
Total Error, External Trim[1]		±0.3 ±0.3			±0.1 ±0.2		mV ± % of Reading
ERROR VS. CREST FACTOR[3]							
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy		
Crest Factor = 3		−0.2			−0.2		% of Reading
Crest Factor = 6		−0.5			−0.5		% of Reading
AVERAGING TIME CONSTANT		25			25		ms/μF CAV
INPUT CHARACTERISTICS							
Signal Range, All Supplies							
Continuous rms Level		0 to 200			0 to 200		mV rms
Peak Transient Inputs							
+3V, −5V Supply			±2.8			±2.8	V pk
±2.5V Supply			±2.0			±2.0	V pk
±5V Supply			±5.0			±5.0	V pk
Maximum Continuous Non-Destructive							
Input Level (All Supply Voltages)			±12			±12	V pk
Input Resistance	5.33	6.67	8	5.33	6.67	8	kΩ
Input Offset Voltage			±0.5			±0.2	mV
FREQUENCY RESPONSE[2,4]							
Bandwidth for 1% additional error (0.09dB)							
V_{IN} = 10mV		14			14		kHz
V_{IN} = 100mV		90			90		kHz
V_{IN} = 200mV		130			130		kHz
±3dB Bandwidth							
V_{IN} = 10mV		100			100		kHz
V_{IN} = 100mV		900			900		kHz
V_{IN} = 200mV		1.5			1.5		MHz
OUTPUT CHARACTERISTICS[2]							
Offset Voltage, V_{IN} = COM			±0.5			±0.2	mV
vs. Temperature		±10			±10		μV/°C
vs. Supply		±0.1			±0.1		mV/V
Voltage Swing							
+3V, −5V Supply	0.3	0 to +1.0		0.3	0 to +1.0		V
±5V to ±16.5V Supply	0.3	0 to +1.0		0.3	0 to +1.0		V
Output Impedance	8	10	12	8	10	12	kΩ
dB OUTPUT							
Error, V_{IN} = 7mV to 300mV rms		±0.3	±0.5		±0.1	±0.2	dB
Scale Factor		−3.0			−3.0		mV/dB
Scale Factor Temperature Coefficient		+0.33			+0.33		% of Reading/°C
		−0.033			−0.033		dB/°C
I_{REF} for 0dB = 0.1V rms	2	4	8	2	4	8	μA
I_{REF} Range	1		50	1		50	μA
I_{OUT} TERMINAL							
I_{OUT} Scale Factor		100			100		μA/V rms
I_{OUT} Scale Factor Tolerance	−20	±10	+20	−20	±10	+20	%
Output Resistance	8	10	12	8	10	12	kΩ
Voltage Compliance		$-V_S$ to ($+V_S$ −2V)			$-V_S$ to ($+V_S$ −2V)		V
BUFFER AMPLIFIER							
Input and Output Voltage Range		$-V_S$ to ($+V_S$ −2V)			$-V_S$ to ($+V_S$ −2V)		V
Input Offset Voltage, R_S = 10k		±0.8	±2		±0.5	±1	mV
Input Bias Current		100	300		100	300	nA
Input Resistance		10^8			10^8		Ω
Output Current	(+5mA, −130μA)			(+5mA, −130μA)			
Short Circuit Current		20			20		mA
Small Signal Bandwidth		1			1		MHz
Slew Rate[5]		5			5		V/μs
POWER SUPPLY							
Voltage, Rated Performance		+3, −5			+3, −5		V
Dual Supply	+2, −2.5		±16.5	+2, −2.5		±16.5	V
Single Supply	+5		+24	+5		+24	V
Quiescent Current[6]		0.80	1.00		0.80	1.00	mA

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TEMPERATURE RANGE					
Rated Performance	0	+70	0	+70	°C
Storage	−55	+150	−55	+150	°C
TRANSISTOR COUNT	62		62		

NOTES
[1]Accuracy specified for 0 to 200mV rms, dc or 1kHz sinewave input. Accuracy is degraded at higher rms signal levels.
[2]Measured at pin 8 of DIP (I_{OUT}), with pin 9 tied to common.
[3]Error vs. crest factor is specified as additional error for a 200mV rms rectangular pulse train, pulse width = 200µs.
[4]Input voltages are expressed in volts rms.
[5]With 10kΩ pull down resistor from pin 6 (BUF OUT) to $-V_S$.
[6]With BUF input tied to Common.
Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test are used to calculate outgoing quality levels.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage
- Dual Supply . . . . . ±16.5 V
- Single Supply . . . . . +24 V

Internal Power Dissipation[2] . . . . . 500 mW
Maximum Input Voltage . . . . . ±12 V Peak
Storage Temperature Range . . . . . −55°C to +150°C
Operating Temperature Range
- AD636J/K . . . . . 0°C to +70°C

Lead Temperature Range (Soldering 60 sec) . . . . . +300°C
ESD Rating . . . . . 1000 V

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation ofthe device at these or anyother conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]10-Pin Header: θ_{JA} = 150°C/W.
14-Pin Sidebrazed Ceramic DIP: θ_{JA} = 95°C/W.

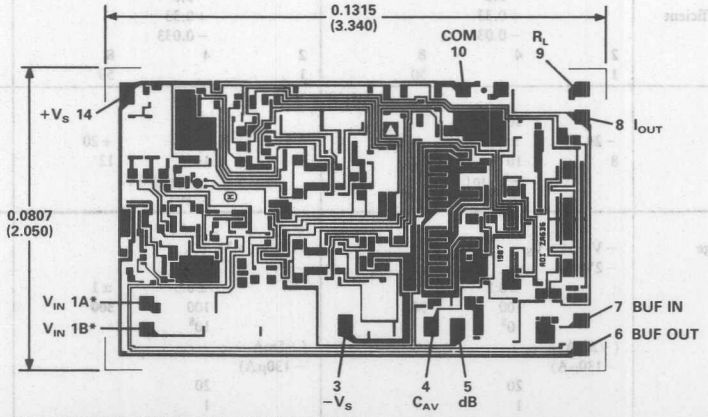
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD636JD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD636KD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD636JH	0°C to +70°C	Header	H-10A
AD636KH	0°C to +70°C	Header	H-10A
AD636J Chip	0°C to +70°C	Chip	
AD636K Chip	0°C to +70°C	Chip	

*For outline information see Package Information section.

METALIZATION PHOTOGRAPHY

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-116 14-PIN CERAMIC DIP PACKAGE.

NOTE
*BOTH PADS SHOWN MUST BE CONNECTED TO V_{IN}.

High Precision, Wideband RMS-to-DC Converter

AD637

FEATURES

High Accuracy
- **0.02% Max Nonlinearity, 0 to 2V RMS Input**
- **0.10% Additional Error to Crest Factor of 3**

Wide Bandwidth
- **8MHz at 1V RMS Input**
- **600kHz at 100mV RMS**

Computes:
- **True RMS**
- **Square**
- **Mean Square**
- **Absolute Value**

dB Output (60dB Range)

Chip Select-Power Down Feature Allows:
- **Analog "3-State" Operation**
- **Quiescent Current Reduction from 2.2mA to 350μA**

Side Brazed DIP, Low-Cost Cerdip and SOIC

PRODUCT DESCRIPTION

The AD637 is a complete high accuracy monolithic rms to dc converter that computes the true rms value of any complex waveform. It offers performance that is unprecedented in integrated circuit rms to dc converters and comparable to discrete and modular techniques in accuracy, bandwidth and dynamic range. A crest factor compensation scheme in the AD637 permits measurements of signals with crest factors of up to 10 with less than 1% additional error. The circuit's wide bandwidth permits the measurement of signals up to 600kHz with inputs of 200mV rms and up to 8MHz when the input levels are above 1V rms.

As with previous monolithic rms converters from Analog Devices, the AD637 has an auxiliary dB output available to the user. The logarithm of the rms output signal is brought out to a separate pin allowing direct dB measurement with a useful range of 60dB. An externally programmed reference current allows the user to select the 0dB reference voltage to correspond to any level between 0.1V and 2.0V rms.

A chip select connection on the AD637 permits the user to decrease the supply current from 2.2mA to 350μA during periods when the rms function is not in use. This feature facilitates the addition of precision rms measurement to remote or hand-held applications where minimum power consumption is critical. In addition when the AD637 is powered down the output goes to a high impedance state. This allows several AD637s to be tied together to form a wide-band true rms multiplexer.

The input circuitry of the AD637 is protected from overload voltages that are in excess of the supply levels. The inputs will not be damaged by input signals if the supply voltages are lost.

The AD637 is available in two accuracy grades (J, K) for commercial (0 to +70°C) temperature range applications; two accuracy grades (A, B) for industrial (−40°C to +85°C) applications; and one (S) rated over the −55°C to +125°C temperature range. All versions are available in hermetically-sealed, 14-pin side-brazed ceramic DIPs as well as low-cost cerdip packages. A 16-pin SOIC package is also available.

PRODUCT HIGHLIGHTS

1. The AD637 computes the true root-mean-square, mean square, or absolute value of any complex ac (or ac plus dc) input waveform and gives an equivalent dc output voltage. The true rms value of a waveform is more useful than an average rectified signal since it relates directly to the power of the signal. The rms value of a statistical signal is also related to the standard deviation of the signal.
2. The AD637 is laser wafer trimmed to achieve rated performance without external trimming. The only external component required is a capacitor which sets the averaging time period. The value of this capacitor also determines low frequency accuracy, ripple level and settling time.
3. The chip select feature of the AD637 permits the user to power down the device down during periods of nonuse, thereby, decreasing battery drain in remote or hand-held applications.
4. The on-chip buffer amplifier can be used as either an input buffer or in an active filter configuration. The filter can be used to reduce the amount of ac ripple, thereby, increasing the accuracy of the measurement.

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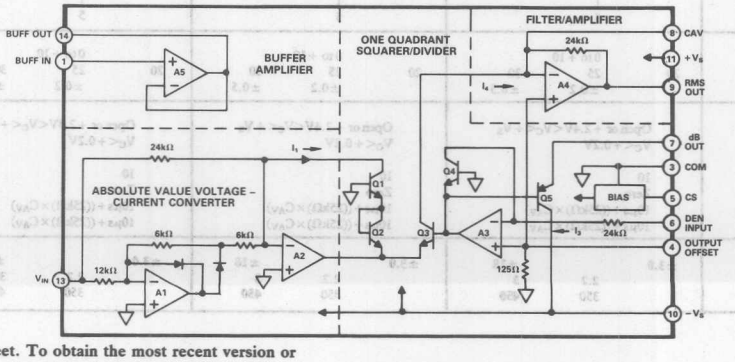
SIMPLIFIED SCHEMATIC



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

Total Error, Internal Trim (Fig. 2)			±1 ±0.5			±0.5 ±0.2			±1 ±0.5	mV ± % of Reading
T_{min} to T_{max}			±3.0 ±0.6			±2.0 ±0.3			±6 ±0.7	mV ± % of Reading
vs. Supply, + V_{IN} = + 300mV		30	150		30	150		30	150	μV/V
vs. Supply, − V_{IN} = − 300mV		100	300		100	300		100	300	μV/V
dc Reversal Error at 2V			0.25			0.1			0.25	% of Reading
Nonlinearity 2V Full Scale[2]			0.04			0.02			0.04	% of FSR
Nonlinearity 7V Full Scale			0.05			0.05			0.05	% of FSR
Total Error, External Trim		±0.5 ±0.1			±0.25 ±0.05			±0.5 ±0.1		mV ± % of Reading
ERROR VS. CREST FACTOR[3]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		±0.1			±0.1			±0.1		% of Reading
Crest Factor = 10		±1.0			±1.0			±1.0		% of Reading
AVERAGING TIME CONSTANT		25			25			25		ms/μF C_{AV}
INPUT CHARACTERISTICS										
Signal Range, ± 15V Supply										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input		±15				±15			±15	V p-p
Signal Range, ± 5V Supply										
Continuous rms Level		0 to 4			0 to 4			0 to 4		V rms
Peak Transient Input		±6				±6			±6	V p-p
Maximum Continuous Non-Destructive Input Level (All Supply Voltages)		±15				±15			±15	V p-p
Input Resistance	6.4	8	9.6	6.4	8	9.6	6.4	8	9.6	kΩ
Input Offset Voltage			±0.5			±0.2			±0.5	mV
FREQUENCY RESPONSE[4]										
Bandwidth for 1% additional error (0.09dB)										
V_{IN} = 20mV		11			11			11		kHz
V_{IN} = 200mV		66			66			66		kHz
V_{IN} = 2V		200			200			200		kHz
± 3dB Bandwidth										
V_{IN} = 20mV		150			150			150		kHz
V_{IN} = 200mV		1			1			1		MHz
V_{IN} = 2V		8			8			8		MHz
OUTPUT CHARACTERISTICS										
Offset Voltage			±1			±0.5			±1	mV
vs. Temperature		±0.05	±0.089		±0.04	±0.056		±0.04	±0.07	mV/°C
Voltage Swing, ± 15V Supply, 2kΩ Load	0 to +12.0	+13.5		0 to +12.0	+13.5		0 to +12.0	+13.5		V
Voltage Swing, ± 3V Supply, 2kΩ Load	0 to +2	+2.2		0 to +2	+2.2		0 to +2	+2.2		V
Output Current	6			6			6			mA
Short Circuit Current		20			20			20		mA
Resistance, Chip Select "High"		0.5			0.5			0.5		Ω
Resistance, Chip Select "Low"		100			100			100		kΩ
dB OUTPUT										
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±0.5			±0.3			±0.5		dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor Temperature Coefficient		+0.33			+0.33			+0.33		% of Reading/°C
		−0.033			−0.033			−0.033		dB/°C
I_{REF} for 0dB = 1V rms	5	20	80	5	20	80	5	20	80	μA
I_{REF} Range	1		100	1		100	1		100	μA
BUFFER AMPLIFIER										
Input and Output Voltage Range	−V_S to (+V_S −2.5V)			−V_S to (+V_S −2.5V)			−V_S to (+V_S −2.5V)			V
Input Offset Voltage		±0.8	±2		±0.5	±1		±0.8	±2	mV
Input Current		±2	±10		±2	±5		±2	±10	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5mA, −130μA)			(+5mA, −130μA)			(+5mA, −130μA)			
Short Circuit Current		20			20			20		mA
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[5]		5			5			5		V/μs
DENOMINATOR INPUT										
Input Range		0 to +10			0 to +10			0 to +10		V
Input Resistance	20	25	30	20	25	30	20	25	30	kΩ
Offset Voltage		±0.2	±0.5		±0.2	±0.5		±0.2	±0.5	mV
CHIP SELECT PROVISION (CS)										
rms "ON" Level	Open or + 2.4V<V_C< + V_S			Open or + 2.4V<V_C< + V_S			Open or + 2.4V<V_C< + V_S			
rms "OFF" Level	V_C< + 0.2V			V_C< + 0.2V			V_C< + 0.2V			
I_{OUT} of Chip Select										
CS "LOW"	10			10			10			μA
CS "HIGH"	Zero			Zero			Zero			
On Time Constant	10μs + ((25kΩ) × C_{AV})			10μs + ((25kΩ) × C_{AV})			10μs + ((25kΩ) × C_{AV})			
Off Time Constant	10μs + ((25kΩ) × C_{AV})			10μs + ((25kΩ) × C_{AV})			10μs + ((25kΩ) × C_{AV})			
POWER SUPPLY										
Operating Voltage Range	±3.0		±18	±3.0		±18	±3.0		±18	V
Quiescent Current		2.2	3		2.2	3		2.2	3	mA
Standby Current		350	450		350	450		350	450	μA

Model	AD637J/A Min	AD637J/A Typ	AD637J/A Max	AD637K/B Min	AD637K/B Typ	AD637K/B Max	AD637S Min	AD637S Typ	AD637S Max	Units
TRANSISTOR COUNT		107			107			107		

NOTES
[1]Accuracy specified 0-7V rms dc with AD637 connected as shown in Figure 2.
[2]Nonlinearity is defined as the maximum deviation from the straight line connecting the readings at 10mV and 2V.
[3]Error vs. crest factor is specified as additional error for 1V rms.
[4]Input voltages are expressed in volts rms. % are in % of reading.
[5]With external 2kΩ pull down resistor tied to $-V_S$.
Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

ESD Rating . . . . . 500 V
Supply Voltage . . . . . ±18 V dc
Internal Quiescent Power Dissipation . . . . . 108 mW
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C
Rated Operating Temperature Range
AD637J, K . . . . . 0°C to +70°C
AD637A, B . . . . . −40°C to +85°C
AD637S, 5962-8963701CA . . . . . −55°C to +125°C

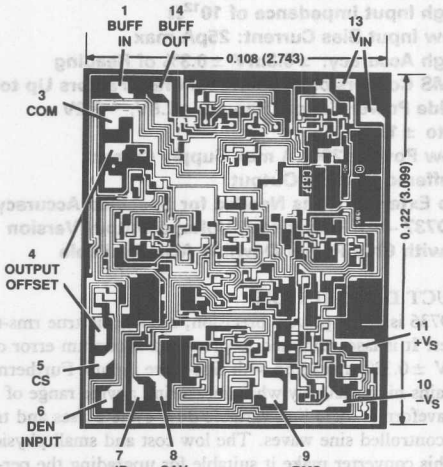
ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option[3]
AD637AR	−40°C to +85°C	SOIC	R-16
AD637BR	−40°C to +85°C	SOIC	R-16
AD637AQ	−40°C to +85°C	Cerdip	Q-14
AD637BQ	−40°C to +85°C	Cerdip	Q-14
AD637JR-Reel	0°C to +70°C	SOIC	R-16
AD637JD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD637KD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD637JQ	0°C to +70°C	Cerdip	Q-14
AD637KQ	0°C to +70°C	Cerdip	Q-14
AD637JR	0°C to +70°C	SOIC	R-16
AD637SD	−55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD637SD/883B	−55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD637SQ/883B	−55°C to +125°C	Cerdip	Q-14

NOTES
[1]"J" and "S" grade chips are also available.
[2]A Standard Military Drawing, 5962-89637, is also available.
[3]For outline information see Package Information section.

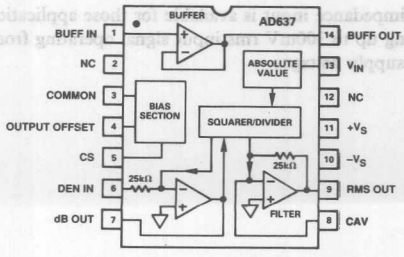
CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).



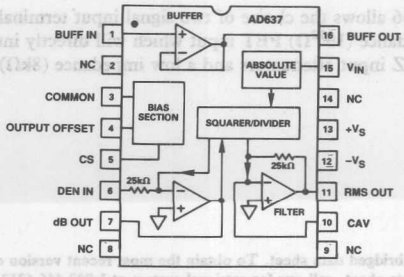
PIN CONFIGURATIONS

Ceramic DIP (D) and Cerdip (Q) Packages



NC = NO CONNECT

SOIC (R) Package



NC = NO CONNECT

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Low Cost, Low Power, True RMS-to-DC Converter

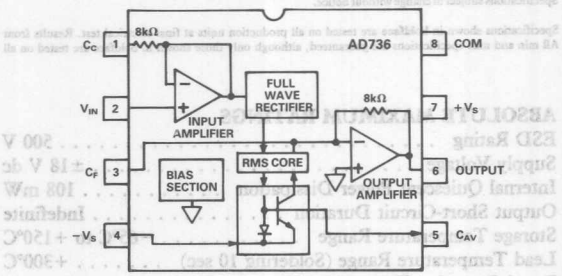
AD736

FEATURES

COMPUTES
- True RMS Value
- Average Rectified Value
- Absolute Value

PROVIDES
- 200mV Full-Scale Input Range (Larger Inputs with Input Attenuator)
- High Input Impedance of $10^{12}\Omega$
- Low Input Bias Current: 25pA max
- High Accuracy: ±0.3mV ±0.3% of Reading
- RMS Conversion with Signal Crest Factors Up to 5
- Wide Power Supply Range: +2.8V, −3.2V to ±16.5V
- Low Power: 200μA max Supply Current
- Buffered Voltage Output
- No External Trims Needed for Specified Accuracy
- AD737 – An Unbuffered Voltage Output Version with Chip Power Down Is Also Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD736 is a low power, precision, monolithic true rms-to-dc converter. It is laser trimmed to provide a maximum error of ±0.3mV ±0.3% of reading with sine-wave inputs. Furthermore, it maintains high accuracy while measuring a wide range of input waveforms, including variable duty cycle pulses and triac (phase) controlled sine waves. The low cost and small physical size of this converter make it suitable for upgrading the performance of non-rms "precision rectifiers" in many applications. Compared to these circuits, the AD736 offers higher accuracy at equal or lower cost.

The AD736 can compute the rms value of both ac and dc input voltages. It can also be operated ac coupled by adding one external capacitor. In this mode, the AD736 can resolve input signal levels of 100μV rms or less, despite variations in temperature or supply voltage. High acccuracy is also maintained for input waveforms with crest factors of 1 to 3. In addition, crest factors as high as 5 can be measured (while introducing only 2.5% additional error) at the 200mV full-scale input level.

The AD736 has its own output buffer amplifier, thereby providing a great deal of design flexibility. Requiring only 200μA of power supply current, the AD736 is optimized for use in portable multimeters and other battery powered applications.

The AD736 allows the choice of two signal input terminals: a high impedance ($10^{12}\Omega$) FET input which will directly interface with high Z input attenuators and a low impedance (8kΩ) input which allows the measurement of 300mV input levels, while operating from the minimum power supply voltage of +2.8V, −3.2V. The two inputs may be used either singly or differentially.

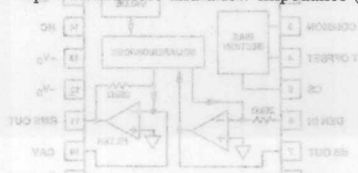
The AD736 achieves a 1% of reading error bandwidth exceeding 10kHz for input amplitudes from 20mV rms to 200mV rms while consuming only 1mW.

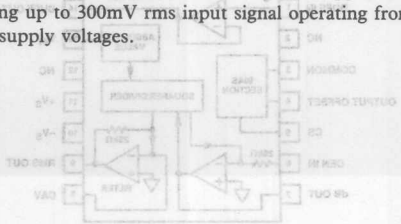
The AD736 is available in four performance grades. The AD736J and AD736K grades are rated over the commercial temperature range of 0 to +70°C. The AD736A and AD736B grades are rated over the industrial temperature range of −40°C to +85°C.

The AD736 is available in three low-cost 8-pin packages: plastic mini-DIP, plastic SO and hermetic cerdip.

PRODUCT HIGHLIGHTS

1. The AD736 is capable of computing the average rectified value, absolute value or true rms value of various input signals.
2. Only one external component, an averaging capacitor, is required for the AD736 to perform true rms measurement.
3. The low power consumption of 1mW makes the AD736 suitable for many battery powered applications.
4. A high input impedance of $10^{12}\Omega$ eliminates the need for an external buffer when interfacing with input attenuators.
5. A low impedance input is available for those applications requiring up to 300mV rms input signal operating from low power supply voltages.





This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C ±5V supplies, ac coupled with 1kHz sine-wave input applied unless otherwise noted.)

Model	Conditions	AD736J/A Min	AD736J/A Typ	AD736J/A Max	AD736K/B Min	AD736K/B Typ	AD736K/B Max	Units
TRANSFER FUNCTION			V_{OUT} $\sqrt{\text{Avg.}(V_{IN}^2)}$			V_{OUT} $\sqrt{\text{Avg.}(V_{IN}^2)}$		
CONVERSION ACCURACY	1kHz Sine Wave							
Total Error, Internal Trim[1]	ac Coupled Using C_C:							
All Grades	0-200mV rms		0.3/0.3	**0.5/0.5**		0.2/0.2	**0.3/0.3**	± mV/± % of Reading
	200mV-1V rms		1.2	**±2.0**		1.2	**±2.0**	% of Reading
T_{min}-T_{max}								
A&B Grades	@ 200mV rms			**0.7/0.7**			**0.5/0.5**	± mV/± % of Reading
J&K Grades	@ 200mV rms		0.007			0.007		± % of Reading/°C
vs. Supply Voltage								
@ 200mV rms Input	V_S ±5V to ±16.5V	**0**	+0.06	**+0.1**	**0**	+0.06	**+0.1**	%/V
@ 200mV rms Input	V_S ±5V to ±3V	**0**	0.18	**−0.3**	**0**	−0.18	**−0.3**	%/V
dc Reversal Error, dc Coupled	@ 600mV dc		1.3	2.5		1.3	2.5	% of Reading
Nonlinearity[2], 0-200mV	@ 100mV rms	**0**	+0.25	**+0.35**	**0**	+0.25	**+0.35**	% of Reading
Total Error, External Trim	0-200mV rms		0.1/0.5			0.1/0.3		± mV/± % of Reading
ERROR vs. CREST FACTOR[3]								
Crest Factor 1 to 3	C_{AV}, C_F = 100µF		0.7			0.7		% Additional Error
Crest Factor = 5	C_{AV}, C_F = 100µF		2.5			2.5		% Additional Error
INPUT CHARACTERISTICS								
High Impedance Input (Pin 2)								
Signal Range								
Continuous rms Level	V_S +2.8V, 3.2V			**200**			**200**	mV rms
Continuous rms Level	V_S ±5V to ±16.5V			**1**			**1**	V rms
Peak Transient Input	V_S +2.8V, 3.2V	**±0.9**			**±0.9**			V
Peak Transient Input	V_S ±5V		±2.7			±2.7		V
Peak Transient Input	V_S ±16.5V	**±4.0**			**±4.0**			V
Input Resistance			10^{12}			10^{12}		Ω
Input Bias Current	±5V		1	25		1	25	pA
Low Impedance Input (Pin 1)								
Signal Range								
Continuous rms Level	V_S = +2.8V, −3.2V			300			300	mV rms
Continuous rms Level	V_S = ±5V to ±16.5V			1			1	V rms
Peak Transient Input	V_S = +2.8V, −3.2V		±1.7			±1.7		V
Peak Transient Input	V_S = ±5V		±3.8			±3.8		V
Peak Transient Input	V_S = ±16.5V		±11			±11		V
Input Resistance		6.4	8	9.6	6.4	8	9.6	kΩ
Maximum Continuous Non-Destructive Input	All Supply Voltages			±12			±12	V p-p
Input Offset Voltage[4]	ac Coupled							
J&K Grades				**±3**			**±3**	mV
A&B Grades				**±3**			**±3**	mV
vs. Temperature			8	30		8	30	µV/°C
vs. Supply	V_S = ±5V to ±16.5V		50	**150**		50	**150**	µV/V
vs. Supply	V_S = ±5V to ±3V		80			80		µV/V
OUTPUT CHARACTERISTICS								
Output Offset Voltage								
J&K Grades			±0.1	**±0.5**		±0.1	**±0.3**	mV
A&B Grades				**±0.5**			**±0.3**	mV
vs. Temperature			1	20		1	20	µV/°C
vs. Supply	V_S = ±5V to ±16.5V		50	**130**		50	**130**	µV/V
	V_S = ±5V to ±3V		50			50		µV/V
Output Voltage Swing								
2kΩ Load	V_S = +2.8V, −3.2V	0 to +1.6	+1.7		0 to +1.6	+1.7		V
2kΩ Load	V_S = ±5V	0 to +3.6	+3.8		0 to +3.6	+3.8		V
2kΩ Load	V_S = ±16.5V	**0 to +4**	+5		**0 to +4**	+5		V
No Load	V_S = ±16.5V	**0 to +4**	+12		**0 to +4**	+12		V
Output Current		2			2			mA
Short-Circuit Current			3			3		mA
Output Resistance	@ dc		0.2			0.2		Ω
FREQUENCY RESPONSE								
High Impedance Input (Pin 2)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1mV rms			1			1		kHz
V_{IN} = 10mV rms			6			6		kHz
V_{IN} = 100mV rms			37			37		kHz
V_{IN} = 200mV rms			33			33		kHz
±3dB Bandwidth	Sine-Wave Input							
V_{IN} = 1mV rms			5			5		kHz
V_{IN} = 10mV rms			55			55		kHz
V_{IN} = 100mV rms			170			170		kHz
V_{IN} = 200mV rms			190			190		kHz

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Low Impedance Input (Pin 1)							
For 1% Additional Error	Sine-Wave Input						
V_{IN} = 1mV rms			1			1	kHz
V_{IN} = 10mV rms			6			6	kHz
V_{IN} = 100mV rms			90			90	kHz
V_{IN} = 200mV rms			90			90	kHz
±3dB Bandwidth	Sine-Wave Input						
V_{IN} = 1mV rms			5			5	kHz
V_{IN} = 10mV rms			55			55	kHz
V_{IN} = 100mV rms			350			350	kHz
V_{IN} = 200mV rms			460			460	kHz
POWER SUPPLY							
Operating Voltage Range		+2.8, −3.2	±5	±16.5	+2.8, −3.2	±5	±16.5	Volts
Quiescent Current	Zero Signal		160	**200**		160	**200**	µA
200mV rms, No Load	Sine-Wave Input		230	270		230	270	µA
TEMPERATURE RANGE							
Operating, Rated Performance							
Commercial (0 to +70°C)			AD736J			AD736K	
Industrial (−40°C to +85°C)			AD736A			AD736B	

NOTES
[1]Accuracy is specified with the AD736 connected as shown in Figure 16 with capacitor C_C.
[2]Nonlinearity is defined as the maximum deviation (in percent error) from a straight line connecting the readings at 0 and 200mV rms. Output offset voltage is adjusted to zero.
[3]Error vs. Crest Factor is specified as additional error for a 200mV rms signal. C.F. = V_{PEAK}/V rms.
[4]DC offset does not limit ac resolution.

Specifications are subject to change without notice.
Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±16.5V
Internal Power Dissipation[2] 200mW
Input Voltage . . . . . ±V_S
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . +V_S and −V_S
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD736J/K . . . . . 0 to +70°C
AD736A/B . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C
ESD Rating . . . . . 500 V

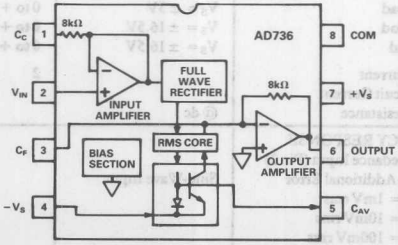
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 165°C/W
8-Pin Cerdip Package: θ_{JA} = 110°C/W
8-Pin Small Outline Package: θ_{JA} = 155°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD736JN	0°C to +70°C	Plastic Mini-DIP	N-8
AD736KN	0°C to +70°C	Plastic Mini-DIP	N-8
AD736JR	0°C to +70°C	Plastic SOIC	R-8
AD736KR	0°C to +70°C	Plastic SOIC	R-8
AD736AQ	−40°C to +85°C	Cerdip	Q-8
AD736BQ	−40°C to +85°C	Cerdip	Q-8
AD736JR-Reel	0°C to +70°C	Plastic SOIC	R-8
AD736KR-Reel	0°C to +70°C	Plastic SOIC	R-8

*For outline information see Package Information section.

PIN CONFIGURATIONS
8-Pin Mini-DIP (N-8), 8-Pin SOIC (R-8)
8-Pin Cerdip (Q-8)

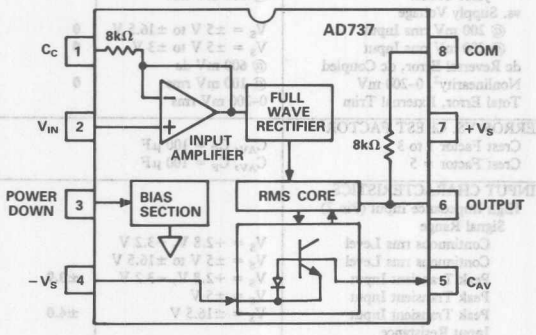


FEATURES

COMPUTES
- True RMS Value
- Average Rectified Value
- Absolute Value

PROVIDES
- 200mV Full-Scale Input Range (Larger Inputs with Input Attenuator)
- Direct Interfacing with 3 1/2 Digit CMOS A/D Converters
- Power Down Feature Which Reduces Supply Current
- High Input Impedance: $10^{12}\ \Omega$
- Low Input Bias Current: 25 pA max
- High Accuracy: ±0.2 mV ±0.3% of Reading
- RMS Conversion with Signal Crest Factors Up to 5
- Wide Power Supply Range: +2.8 V, −3.2 V to ±16.5 V
- Low Power: 160 μA max Supply Current
- No External Trims Needed for Specified Accuracy
- AD736 – A General Purpose, Buffered Voltage Output Version Also Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD737 is a low power, precision, monolithic true rms-to-dc converter. It is laser trimmed to provide a maximum error of ±0.2 mV ±0.3% of reading with sine wave inputs. Furthermore, it maintains high accuracy while measuring a wide range of input waveforms, including variable duty cycle pulses and triac (phase) controlled sine waves. The low cost and small physical size of this converter make it suitable for upgrading the performance of non-rms "precision rectifiers" in many applications. Compared to these circuits, the AD737 offers higher accuracy at equal or lower cost.

The AD737 can compute the rms value of both ac and dc input voltages. It can also be operated ac coupled by adding one external capacitor. In this mode, the AD737 can resolve input signal levels of 100 μV rms or less, despite variations in temperature or supply voltage. High accuracy is also maintained for input waveforms with crest factors of 1 to 3. In addition, crest factors as high as 5 can be measured (while introducing only 2.5% additional error) at the 200 mV full-scale input level.

The AD737 has no output buffer amplifier, thereby significantly reducing dc offset errors occurring at the output. This allows the device to be highly compatible with high input impedance A/D converters.

Requiring only 160 μA of power supply current, the AD737 is optimized for use in portable multimeters and other battery powered applications. This converter also provides a "power down" feature which reduces the power supply standby current to less than 30 μA.

The AD737 allows the choice of two signal input terminals: a high impedance ($10^{12}\ \Omega$) FET input which will directly interface with high Z input attenuators and a low impedance (8 kΩ) input which allows the measurement of 300 mV input levels while operating from the minimum power supply voltage of +2.8 V, −3.2 V. The two inputs may be used either singly or differentially.

The AD737 achieves a 1% of reading error bandwidth exceeding 10 kHz for input amplitudes from 20 mV rms to 200 mV rms while consuming only 0.72 mW.

The AD737 is available in four performance grades. The AD737J and AD737K grades are rated over the commercial temperature range of 0 to +70°C. The AD737A and AD737B grades are rated over the industrial temperature range of −40°C to +85°C.

The AD737 is available in three low cost, 8-pin packages: plastic mini-DIP, plastic SO and hermetic cerdip.

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PRODUCT HIGHLIGHTS

1. The AD737 is capable of computing the average rectified value, absolute value or true rms value of various input signals.
2. Only one external component, an averaging capacitor, is required for the AD737 to perform true rms measurement.
3. The low power consumption of 0.72 mW makes the AD737 suitable for many battery powered applications.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD737—SPECIFICATIONS (@ +25°C, ±5 V supplies, ac coupled with 1 kHz sine wave input applied unless otherwise noted.)

Model	Conditions	AD737J/A Min	AD737J/A Typ	AD737J/A Max	AD737K/B Min	AD737K/B Typ	AD737K/B Max	Units
TRANSFER FUNCTION			$V_{OUT} = -\sqrt{Avg.(V_{IN}^2)}$			$V_{OUT} = -\sqrt{Avg.(V_{IN}^2)}$		
CONVERSION ACCURACY	1 kHz Sine Wave							
Total Error, Internal Trim[1]	AC Coupled Using C_C							
All Grades	0–200 mV rms		0.2/0.3	0.4/0.5		0.2/0.2	0.2/0.3	±mV/±% of Reading
	200 mV–1 V rms		−1.2	±2.0		−1.2	±2.0	% of Reading
T_{min}–T_{max}								
A&B Grades	@ 200 mV rms			0.5/0.7			0.3/0.5	±mV/±% of Reading
J&K Grades	@ 200 mV rms		0.007			0.007		±% of Reading/°C
vs. Supply Voltage								
@ 200 mV rms Input	V_S = ±5 V to ±16.5 V	0	+0.06	+0.1	0	+0.06	+0.1	%/V
@ 200 mV rms Input	V_S = ±5 V to ±3 V	0	−0.18	−0.3	0	−0.18	−0.3	%/V
dc Reversal Error, dc Coupled	@ 600 mV dc		1.3	2.5		1.3	2.5	% of Reading
Nonlinearity[2], 0–200 mV	@ 100 mV rms	0	+0.25	+0.35	0	+0.25	+0.35	% of Reading
Total Error, External Trim	0–200 mV rms		0.1/0.2			0.1/0.2		±mV/±% of Reading
ERROR VS. CREST FACTOR[3]								
Crest Factor 1 to 3	C_{AV}, C_F = 100 µF		0.7			0.7		% Additional Error
Crest Factor = 5	C_{AV}, C_F = 100 µF		2.5			2.5		% Additional Error
INPUT CHARACTERISTICS								
High Impedance Input (Pin 2)								
Signal Range								
Continuous rms Level	V_S = +2.8 V, −3.2 V			200			200	mV rms
Continuous rms Level	V_S = ±5 V to ±16.5 V			1			1	V rms
Peak Transient Input	V_S = +2.8 V, −3.2 V	±0.9			±0.9			V
Peak Transient Input	V_S = ±5 V		±2.7			±2.7		V
Peak Transient Input	V_S = ±16.5 V	±4.0			±4.0			V
Input Resistance			10^{12}			10^{12}		Ω
Input Bias Current	V_S = ±5 V		1	25		1	25	pA
Low Impedance Input (Pin 1)								
Signal Range								
Continuous rms Level	V_S = +2.8 V, −3.2 V			300			300	mV rms
Continuous rms Level	V_S = ±5 V to ±16.5 V			1			1	V rms
Peak Transient Input	V_S = +2.8 V, −3.2 V		±1.7			±1.7		V
Peak Transient Input	V_S = ±5 V		±3.8			±3.8		V
Peak Transient Input	V_S = ±16.5 V		±11			±11		V
Input Resistance		6.4	8	9.6	6.4	8	9.6	kΩ
Maximum Continuous Nondestructive Input	All Supply Voltages			±12			±12	V p-p
Input Offset Voltage[4]	ac Coupled							
J&K Grades				±3			±3	mV
A&B Grades				±3			±3	mV
vs. Temperature			8	30		8	30	µV/°C
vs. Supply	V_S = ±5 V to ±16.5 V		50	150		50	150	µV/V
vs. Supply	V_S = ±5 V to ±3 V		80			80		µV/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
No Load	V_S = +2.8 V, −3.2 V	0 to −1.6	−1.7		0 to −1.6	−1.7		V
No Load	V_S = ±5 V	0 to −3.3	−3.4		0 to −3.3	−3.4		V
No Load	V_S = ±16.5 V	0 to −4	−5		0 to −4	−5		V
Output Resistance	@ dc	6.4	8	9.6	6.4	8	9.6	kΩ
FREQUENCY RESPONSE								
High Impedance Input (Pin 2)								
For 1% Additional Error	Sine Wave Input							
V_{IN} = 1 mV rms			1			1		kHz
V_{IN} = 10 mV rms			6			6		kHz
V_{IN} = 100 mV rms			37			37		kHz
V_{IN} = 200 mV rms			33			33		kHz
±3 dB Bandwidth	Sine Wave Input							
V_{IN} = 1 mV rms			5			5		kHz
V_{IN} = 10 mV rms			55			55		kHz
V_{IN} = 100 mV rms			170			170		kHz
V_{IN} = 200 mV rms			190			190		kHz
FREQUENCY RESPONSE								
Low Impedance Input (Pin 1)								
For 1% Additional Error	Sine Wave Input							
V_{IN} = 1 mV rms			1			1		kHz
V_{IN} = 10 mV rms			6			6		kHz
V_{IN} = 100 mV rms			90			90		kHz
V_{IN} = 200 mV rms			90			90		kHz
±3 dB Bandwidth	Sine Wave Input							
V_{IN} = 1 mV rms			5			5		kHz
V_{IN} = 10 mV rms			55			55		kHz
V_{IN} = 100 mV rms			350			350		kHz
V_{IN} = 200 mV rms			460			460		kHz

Model	Conditions	AD737J/A Min	AD737J/A Typ	AD737J/A Max	AD737K/B Min	AD737K/B Typ	AD737K/B Max	Units
POWER SUPPLY								
Operating Voltage Range		+2.8,−3.2	±5	±16.5	+2.8,−3.2	±5	±16.5	V
Quiescent Current	Zero Signal		120	**160**		120	**160**	μA
V_{IN} = 200 mV rms, No Load	Sine Wave Input		170	210		170	210	μA
Power Down Mode Current	Pin 3 tied to $+V_S$		25	**40**		25	**40**	μA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0 to +70°C)			AD737J			AD737K		
Industrial (−40°C to +85°C)			AD737A			AD737B		

NOTES
[1]Accuracy is specified with the AD737 connected as shown in Figure 16 with capacitor C_C.
[2]Nonlinearity is defined as the maximum deviation (in percent error) from a straight line connecting the readings at 0 and 200 mV rms.
[3]Error vs. Crest Factor is specified as additional error for a 200 mV rms signal. C.F. = V_{PEAK}/V rms.
[4]DC offset does not limit ac resolution.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±16.5 V
Internal Power Dissipation[2] . . . . . 200 mW
Input Voltage . . . . . $\pm V_S$
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD737J/K . . . . . 0 to +70°C
AD737A/B . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C
ESD Rating . . . . . 500 V

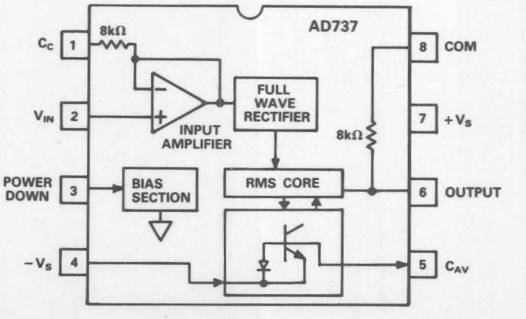
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 165°C/W
8-Pin Ceramic Package: θ_{JA} = 110°C/W
8-Pin SOIC: θ_{JA} = 155°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD737JN	0°C to +70°C	Plastic Mini-DIP	N-8
AD737KN	0°C to +70°C	Plastic Mini-DIP	N-8
AD737JR	0°C to +70°C	SOIC	R-8
AD737KR	0°C to +70°C	SOIC	R-8
AD737AQ	−40°C to +85°C	Cerdip	Q-8
AD737BQ	−40°C to +85°C	Cerdip	Q-8
AD737JR-Reel	−40°C to +85°C	SOIC	R-8
AD737KR-Reel	−40°C to +85°C	SOIC	R-8

*For outline information see Package Information section.

PIN CONFIGURATIONS
8-Pin Mini-DIP (N-8), 8-Pin SOIC (R-8)
8-Pin Cerdip (Q-8)



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Operating Voltage Range		+2.8, −3.2	±5	±16.5	+2.8, −3.2 ±5 ±16.5 V
Quiescent Current	Zero Signal		120	160	120 160 μA
V_{IN} = 200 mV rms, No Load	Sine Wave Input		170	210	170 210 μA
Power Down Mode Current	Pin 3 tied to $+V_S$		25	40	25 40 μA
TEMPERATURE RANGE					
Operating, Rated Performance					
Commercial (0 to +70°C)		AD737J			AD737K
Industrial (−40°C to +85°C)		AD737A			AD737B

NOTES

[1]Accuracy is specified with the AD737 connected as shown in Figure 16 with capacitor C_F.

[2]Nonlinearity is defined as the maximum deviation (in percent error) from a straight line connecting the readings at 0 and 200 mV rms.

[3]Error vs. Crest Factor is specified as additional error for a 200 mV rms signal. C.F. = V_{PEAK}/V rms.

[4]DC offset does not limit ac resolution.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±16.5 V
Internal Power Dissipation[2] . . . . . 200 mW
Input Voltage . . . . . ±V_S
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . +V_S and −V_S
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD737JN . . . . . 0 to +70°C
AD737AQ . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C
ESD Rating . . . . . 500 V

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

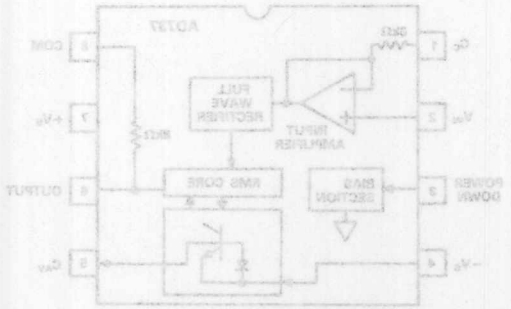
[2]8-Pin Plastic Package: θ_{JA} = 165°C/W
8-Pin Ceramic Package: θ_{JA} = 110°C/W
8-Pin SOIC: θ_{JA} = 155°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD737JN	0°C to +70°C	Plastic Mini-DIP	N-8
AD737KN	0°C to +70°C	Plastic Mini-DIP	N-8
AD737JR	0°C to +70°C	SOIC	R-8
AD737KR	0°C to +70°C	SOIC	R-8
AD737AQ	−40°C to +85°C	Cerdip	Q-8
AD737BQ	−40°C to +85°C	Cerdip	Q-8
AD737JR-Reel	−40°C to +85°C	SOIC	R-8
AD737KR-Reel	−40°C to +85°C	SOIC	R-8

*For outline information see Package Information section.

PIN CONFIGURATIONS
8-Pin Mini-DIP (N-8), 8-Pin SOIC (R-8)
8-Pin Cerdip (Q-8)



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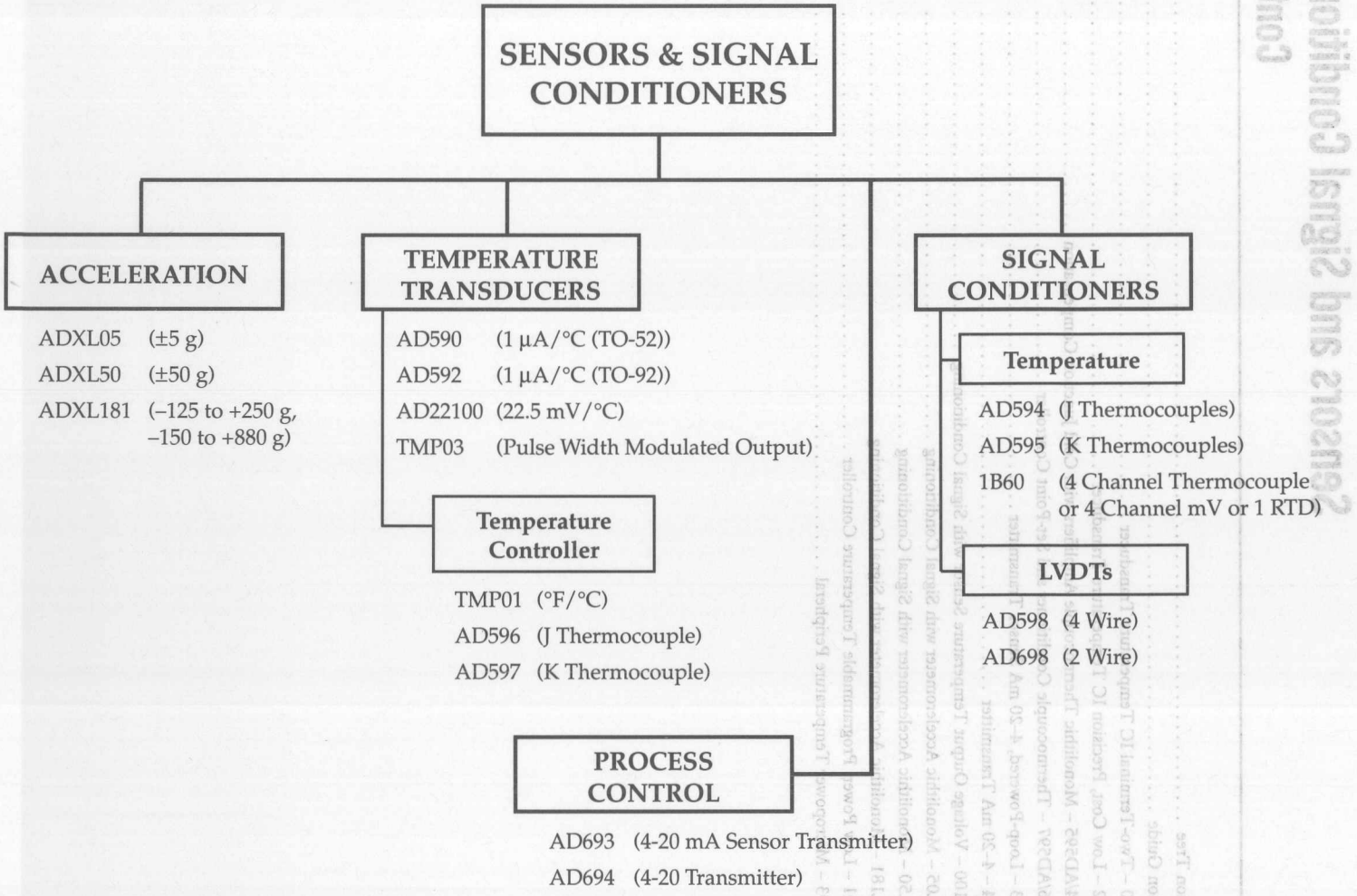
Selection Tree — Sensors and Signal Conditioners



Selection Guides—Sensors and Signal Conditioners

Temperature Sensors

Model	I_{OUT} µA/K	V_{OUT} mV/K	Cal Error °C max	Nonlin °C max	Package Options[1]	Temp Ranges[2]	Page[3]	Comments
AC2626	1	—	0.5–5	0.3–1.5 Steel Sheath	3/16″ Stainless	C, M	SL 10–5	General Purpose Temperature Probe 4″ and 6″ Length
AD590	**1**	**—**	**0.5–5**	**0.3–1.5**	**F, H**	**M+/$_{DS}$**	**19–5**	**Wide Temperature Range, Accurate**
AD592	**1**	**—**	**0.5–2.5**	**0.15–0.35**	**N**	**I+**	**19–9**	**Low Cost, Accurate**
TMP01	**—**	**5**	**1.5–3**	**0.5–2.0**	**H, N, R**	**I, M+**	**19–57**	**Complete Programmable Temperature Controller**
TMP03	**—**	**—**	**1.2–2.4**	**1.0**	**H, R, T**	**M+**	**19–72**	**3 Pins, Direct Serial Digital Output**
AD22100	**—**	**22.5**	**2.0**	**1–2**	**R, T**	**M+**	**19–31**	**3 Pins, Output Proportional to V+**

Sensor Interfaces

Model	Sensor Type	Output	Accuracy	Package Options[1]	Temp Ranges[2]	Page[3]	Comments
AD594	**Thermocouple Type J**	**10 mV/°C**	**1–3°C**	**D, Q**	**C**	**19–12**	**Cold Junction Compensation, Alternate Thermocouple Types**
AD595	**Thermocouple Type K**	**10 mV/°C**	**1–3°C**	**D, Q**	**C**	**19–12**	**Cold Junction Compensation, Alternate Thermocouple Types**
AD596	**Thermocouple Type J**	**10 mV/°C**	**4°C**	**H**	**C**	**19–15**	**Lower Cost, Set Point Control**
AD597	**Thermocouple Type K**	**10 mV/°C**	**4°C**	**H**	**C**	**19–15**	**Lower Cost, Set Point Control**
AD693	**RTD or Low Level mV**	**4–20 mA/0–20 mA**	**2°C/0.5%**	**D, E, Q**	**I**	**19–18**	**Loop Powered Sensor Transmitter**
AD694	**High Level 4–20 mA Transmitter**	**4–20 mA/0–20 mA**	**0.15–0.3%**	**N, Q, R**	**C, I**	**19–24**	**5 V Supply, Wide Compliance**
AD598	**LVDT Position Sensor**	**V_{OUT} Prop. to Position**	**0.05%**	**D, R**	**C, I**	**16–63**	**Complete Interface with Oscillator/Driver**
AD698	**LVDT Position Sensor**	**V_{OUT} Prop. to Position**	**0.05%**	**P, Q**	**I, M**	**16–67**	**Universal LVDT Interface**

Accelerometers

Model	Range	Linearity Error	Freq Response	Power Supply	Package Options[1]	Temp Ranges[2]	Page[3]	Comments
ADXL05	**±5 g**	**0.5%**	**DC to 4 kHz**	**+5 V**	**H**	**M**	**19–37**	**Complete Acceleration Sensor/Amplifier**
ADXL50	**±50 g**	**0.2%**	**DC to 10 kHz**	**+5 V**	**H**	**M**	**19–39**	**500 µg Sensitivity**
ADXL181	**−125 to +250 g**	**0.2%**	**DC to 3 kHz**	**+5 V**	**H**	**M**	**19–55**	**2000 g Shock Survivable**
	−150 to +880 g	**0.2%**	**DC to 3 kHz**	**+12 V**				

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]*SL = Special Linear Reference Manual*. All other entries refer to this volume.
Boldface Type: Data sheet information in this volume.

Selection Guides—Sensors and Signal Conditioners

Temperature Sensors

Model	I_{OUT} µA/K	V_{OUT} mV/K	Cal Error °C max	Nonlin °C max	Package Options[1]	Temp Ranges[2]	Page[2]	Comments
AD2625	1	—	0.5–5	0.3–1.5	Steel Sheath	C, M	SL 10–5	General Purpose Temperature Probe 4" and 6"
AD590	1	—	0.5–5	0.3–1.5	F, H	M+/Ice	19–5	Wide Temperature Range, Accurate
AD592	1	—	0.5–2.5	0.15–0.35	N	I+	19–9	Low Cost, Accurate
TMP01	—	5	1.5–3	0.5–2.0	H, N, R	I, M+	19–17	Complete Programmable Temperature Control
TMP03	—	—	1.3–2.4	1.0	H, R, T	M+	19–22	3 Pins, Direct Serial Digital Output
AD22100	—	22.5	2.0	1–2	R, T	M+	19–21	3 Pins, Output Proportional to V+

Sensor Interfaces

Model	Sensor Type	Output	Accuracy	Package Options[1]	Temp Ranges[2]	Page[2]	Comments
AD594	Thermocouple Type J	10 mV/°C	1–3°C	D, Q	C	19–12	Cold Junction Compensation, Alternate Thermocouple
AD595	Thermocouple Type K	10 mV/°C	1–3°C	D, Q	C	19–12	Cold Junction Compensation, Alternate Thermocouple
AD596	Thermocouple Type J	10 mV/°C	4°C	H	C	19–15	Lower Cost, Set Point Control
AD597	Thermocouple Type K	10 mV/°C	4°C	H	C	19–15	Lower Cost, Set Point Control
AD693	RTD or Low Level mV	4–20 mA/0–20 mA	2°C/0.5%	D, E, Q	I	19–18	Loop Powered Sensor Transmitter
AD694	High Level 4–20 mA Transmitter	4–20 mA/0–20 mA	0.15–0.3%	N, Q, R	C, I	19–24	5 V Supply, Wide Compliance
AD698	LVDT Position Sensor	V_{OUT} Prop. to Position	0.05%	D, R	C, I	19–63	Complete Interface with Oscillator/Driver
AD598	LVDT Position Sensor	V_{OUT} Prop. to Position	0.05%	P, Q	I, M	19–67	Universal LVDT Interface

Accelerometers

Model	Range	Linearity Error	Freq Response	Power Supply	Package Options[1]	Temp Ranges[2]	Page[1]	Comments
ADXL05	±5 g	0.5%	DC to 4 kHz	+5 V	H	M	19–37	Complete Acceleration Sensor
ADXL50	±50 g	0.2%	DC to 10 kHz	+5 V	H	M	19–39	500 µg Sensitivity
ADXL181	–125 to +250 g	0.2%	DC to 3 kHz	+5 V	H	M	19–55	2000 g Shock Survivable
	–150 to +350 g	0.2%	DC to 3 kHz	+12 V				

[1]Package Options: D = Hermetic DIP; Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.

[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, –40°C to +85°C (Some older products –25°C to +85°C); M = Military, –55°C to +125°C. If a device has military grade offerings, temperature designators will be followed by / to indicate 883B, ^{1} for JAN, ^{D} for SMD, and ^{2} for space level.

[3]SL = Special Linear Reference Manual. All other entries refer to this volume.

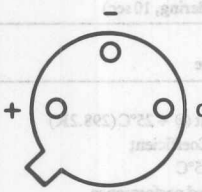
Boldface Type: Data sheet information in this volume.

Two-Terminal IC Temperature Transducer

AD590*

FEATURES
- Linear Current Output: 1μA/K
- Wide Range: -55°C to +150°C
- Probe Compatible Ceramic Sensor Package
- Two-Terminal Device: Voltage In/Current Out
- Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)
- Excellent Linearity: ±0.3°C Over Full Range (AD590M)
- Wide Power Supply Range: +4V to +30V
- Sensor Isolation from Case
- Low Cost

PIN DESIGNATIONS



BOTTOM VIEW

PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V the device acts as a high impedance, constant current regulator passing 1μA/K. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2K (+25°C).

The AD590 should be used in any temperature sensing application below +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

***Covered by Patent No. 4,123,698.**

PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply (+4V to +30V). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable.
3. Superior interference rejection results from the output being a current rather than a voltage. In addition, power requirements are low (1.5mW's @ 5V @ +25°C). These features make the AD590 easy to apply as a remote sensor.
4. The high output impedance (>10MΩ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from 5V to 10V results in only a 1μA maximum current change, or 1°C equivalent error.
5. The AD590 is electrically durable: it will withstand a forward voltage up to 44V and a reverse voltage of 20V. Hence, supply irregularities or pin reversal will not damage the device.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD590—SPECIFICATIONS (@ +25°C and V_S = +5V unless otherwise noted)

Model	AD590J			AD590K			
	Min	Typ	Max	Min	Typ	Max	Units
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E+ to E−)			+44			+44	Volts
Reverse Voltage (E+ to E−)			−20			−20	Volts
Breakdown Voltage (Case to E+ or E−)			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		μA
Nominal Temperature Coefficient		1			1		μA/K
Calibration Error @ +25°C			**±5.0**			**±2.5**	°C
Absolute Error (over rated performance temperature range)							
Without External Calibration Adjustment			**±10**			**±5.5**	°C
With +25°C Calibration Error Set to Zero			**±3.0**			**±2.0**	°C
Nonlinearity			**±1.5**			**±0.8**	°C
Repeatability[2]			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA/$\sqrt{\text{Hz}}$
Power Supply Rejection							
$+4V \le V_S \le +5V$		0.5			0.5		μA/V
$+5V \le V_S \le +15V$		0.2			0.2		μA/V
$+15V \le V_S \le +30V$		0.1			0.1		μA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		μs
Reverse Bias Leakage Current[4] (Reverse Voltage = 10V)		10			10		pA
PACKAGE OPTIONS[5]							
TO-52 (H-03A)		AD590JH			AD590KH		
Flat Pack (F-2A)		AD590JF			AD590KF		

NOTES

[1]The AD590 has been used at −100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

[2]Maximum deviation between +25°C readings after temperature cycling between −55°C and +150°C; guaranteed not tested.

[3]Conditions: constant +5V, constant +125°C; guaranteed, not tested.

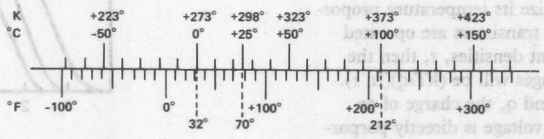
[4]Leakage current doubles every 10°C.

[5]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Model	AD590L Min	AD590L Typ	AD590L Max	AD590M Min	AD590M Typ	AD590M Max	Units
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E+ to E−)			+44			+44	Volts
Reverse Voltage (E+ to E−)			−20			−20	Volts
Breakdown Voltage (Case to E+ or E−)			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		μA
Nominal Temperature Coefficient		1			1		μA/K
Calibration Error @ +25°C			±1.0			±0.5	°C
Absolute Error (over rated performance temperature range)							
Without External Calibration Adjustment			±3.0			±1.7	°C
With +25°C Calibration Error Set to Zero			±1.6			±1.0	°C
Nonlinearity			±0.4			±0.3	°C
Repeatability[2]			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA$\sqrt{\text{Hz}}$
Power Supply Rejection							
$+4V \le V_S \le +5V$		0.5			0.5		μA/V
$+5V \le V_S \le +15V$		0.2			0.2		μA/V
$+15V \le V_S \le +30V$		0.1			0.1		μA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		μs
Reverse Bias Leakage Current[4] (Reverse Voltage = 10V)		10			10		pA
PACKAGE OPTION[5]							
TO-52 (H-03A)		AD590LH			AD590MH		
Flat Pack (F-2A)		AD590LF			AD590MF		



TEMPERATURE SCALE CONVERSION EQUATIONS

$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

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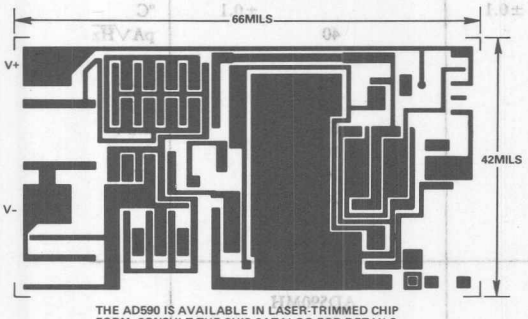
The 590H has 60μ inches of gold plating on its Kovar leads and Kovar header. A resistance welder is used to seal the nickel cap to the header. The AD590 chip is eutectically mounted to the header and ultrasonically bonded to with 1 MIL aluminum wire. Kovar composition: 53% iron nominal; 29% ±1% nickel; 17% ±1% cobalt; 0.65% manganese max; 0.20% silicon max; 0.10% aluminum max; 0.10% magnesium max; 0.10% zirconium max; 0.10% titanium max; 0.06% carbon max.

The 590F is a ceramic package with gold plating on its Kovar leads, Kovar lid, and chip cavity. Solder of 80/20 Au/Sn composition is used for the 1.5 mil thick solder ring under the lid. The chip cavity has a nickel underlay between the metalization and the gold plating. The AD590 chip is eutectically mounted in the chip cavity at 410°C and ultrasonically bonded to with 1 mil aluminum wire. Note that the chip is in direct contact with the ceramic base, not the metal lid. When using the AD590 in die form, the chip substrate must be kept electrically isolated, (floating), for correct circuit operation.

METALIZATION DIAGRAM



THE AD590 IS AVAILABLE IN LASER-TRIMMED CHIP FORM; CONSULT THE CHIP CATALOG FOR DETAILS.

CIRCUIT DESCRIPTION[1]

The AD590 uses a fundamental property of the silicon transistors from which it is made to realize its temperature proportional characteristic: if two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in their base-emitter voltages will be (kT/q)(In r). Since both k, Boltzman's constant and q, the charge of an electron, are constant, the resulting voltage is directly porportional to absolute temperature (PTAT).

In the AD590, this PTAT voltage is converted to a PTAT current by low temperature coefficient thin film resistors. The total current of the device is then forced to be a multiple of this PTAT current. Referring to Figure 1, the schematic diagram of the AD590, Q8 and Q11 are the transistors that produce the PTAT voltage. R5 and R6 convert the voltage to current. Q10, whose collector current tracks the collector currents in Q9 and Q11, supplies all the bias and substrate leakage current for the rest of the circuit, forcing the total current to be PTAT. R5 and R6 are laser trimmed on the wafer to calibrate the device at +25°C.

Figure 2 shows the typical V–I characteristic of the circuit at +25°C and the temperature extremes.

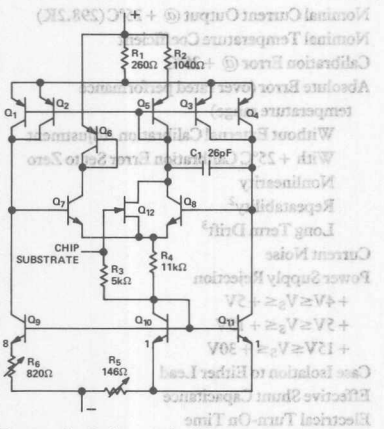


Figure 1. Schematic Diagram

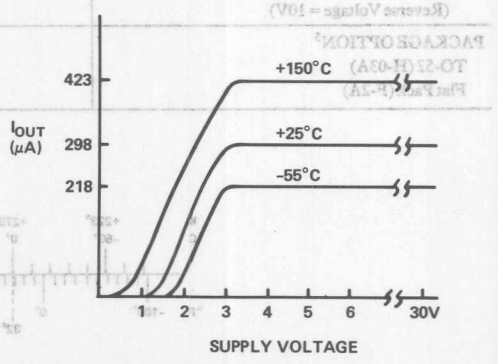


Figure 2. V–I Plot

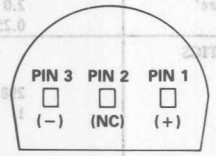
[1] For a more detailed circuit description see M.P. Timko, "A Two-Terminal IC Temperature Transducer," IEEE J. Solid State Circuits, Vol. SC-11, p. 784-788, Dec. 1976.

Low Cost, Precision IC Temperature Transducer

AD592*

FEATURES
High Precalibrated Accuracy: 0.5°C max @ 25°C
Excellent Linearity: 0.15°C max (0 to +70°C)
Wide Operating Temperature Range: −25°C to +105°C
Single Supply Operation: +4V to +30V
Excellent Repeatability and Stability
High Level Output: 1μA/K
Two Terminal Monolithic IC: Temperature In/ Current Out
Minimal Self-Heating Errors

CONNECTION DIAGRAM



***PIN 2 CAN BE EITHER ATTACHED OR UNCONNECTED**

BOTTOM VIEW

PRODUCT DESCRIPTION

The AD592 is a two terminal monolithic integrated circuit temperature transducer that provides an output current proportional to absolute temperature. For a wide range of supply voltages the transducer acts as a high impedance temperature dependent current source of 1μA/K. Improved design and laser wafer trimming of the IC's thin film resistors allows the AD592 to achieve absolute accuracy levels and nonlinearity errors previously unattainable at a comparable price.

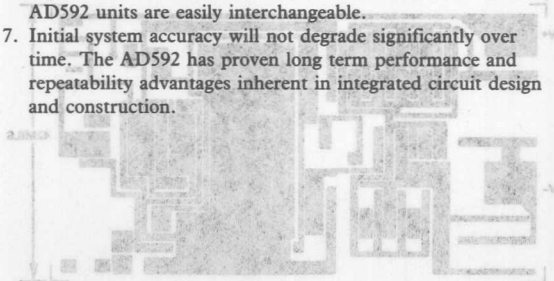
The AD592 can be employed in applications between −25°C and +105°C where conventional temperature sensors (i.e., thermistor, RTD, thermocouple, diode) are currently being used. The inherent low cost of a monolithic integrated circuit in a plastic package, combined with a low total parts count in any given application, make the AD592 the most cost effective temperature transducer currently available. Expensive linearization circuitry, precision voltage references, bridge components, resistance measuring circuitry and cold junction compensation are not required with the AD592.

Typical application areas include; appliance temperature sensing, automotive temperature measurement and control, HVAC (heating/ventilating/air conditioning) system monitoring, industrial temperature control, thermocouple cold junction compensation, board-level electronics temperature diagnostics, temperature readout options in instrumentation, and temperature correction circuitry for precision electronics. Particularly useful in remote sensing applications, the AD592 is immune to voltage drops and voltage noise over long lines due to its high impedance current output. AD592s can easily be multiplexed; the signal current can be switched by a CMOS multiplexer or the supply voltage can be enabled with a tri-state logic gate.

The AD592 is available in three performance grades; the AD592AN, AD592BN and AD592CN. All devices are packaged in a plastic TO-92 case rated from −45°C to +125°C. Performance is specified from −25°C to +105°C. AD592 chips are also available, contact the factory for details.

PRODUCT HIGHLIGHTS

1. With a single supply (4V to 30V) the AD592 offers 0.5°C temperature measurement accuracy.
2. A wide operating temperature range (−25°C to +105°C) and highly linear output make the AD592 an ideal substitute for older, more limited sensor technologies (i.e., thermistors, RTDs, diodes, thermocouples).
3. The AD592 is electrically rugged; supply irregularities and variations or reverse voltages up to 20V will not damage the device.
4. Because the AD592 is a temperature dependent current source, it is immune to voltage noise pickup and IR drops in the signal leads when used remotely.
5. The high output impedance of the AD592 provides greater than 0.5°C/V rejection of supply voltage drift and ripple.
6. Laser wafer trimming and temperature testing insures that AD592 units are easily interchangeable.
7. Initial system accuracy will not degrade significantly over time. The AD592 has proven long term performance and repeatability advantages inherent in integrated circuit design and construction.



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***Protected by Patent No. 4,123,698.**

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD592—SPECIFICATIONS (typical @ +25°C, V_S = +5V unless otherwise noted)

Model	AD592AN Min	AD592AN Typ	AD592AN Max	AD592BN Min	AD592BN Typ	AD592BN Max	AD592CN Min	AD592CN Typ	AD592CN Max	Units
ACCURACY										
Calibration Error @25°C[1]		1.5	2.5		0.7	1.0		0.3	0.5	°C
T_A = 0 to +70°C										
Error over Temperature		1.8	3.0		0.8	1.5		0.4	0.8	°C
Nonlinearity[2]		0.15	0.35		0.1	0.25		0.05	0.15	°C
T_A = −25 to +105°C										
Error over Temperature[3]		2.0	3.5		0.9	2.0		0.5	1.0	°C
Nonlinearity[2]		0.25	0.5		0.2	0.4		0.1	0.35	°C
OUTPUT CHARACTERISTICS										
Nominal Current Output @25°C (298.2K)		298.2			298.2			298.2		µA
Temperature Coefficient		1			1			1		µA/°C
Repeatability[4]			0.1			0.1			0.1	°C
Long Term Stability[5]			0.1			0.1			0.1	°C/month
ABSOLUTE MAXIMUM RATINGS										
Operating Temperature	−25		+105	−25		+105	−25		+105	°C
Package Temperature[6]	−45		+125	−45		+125	−45		+125	°C
Forward Voltage (+ to −)			44			44			44	V
Reverse Voltage (− to +)			20			20			20	V
Lead Temperature (Soldering 10 sec)			300			300			300	°C
POWER SUPPLY										
Operating Voltage Range	4		30	4		30	4		30	V
Power Supply Rejection										
+4V<V_S<+5V			0.5			0.5			0.5	°C/V
+5V<V_S<+15V			0.2			0.2			0.2	°C/V
+15V<V_S<+30V			0.1			0.1			0.1	°C/V

NOTES

[1]An external calibration trim can be used to zero the error @25°C.

[2]Defined as the maximum deviation from a mathematically best fit line.

[3]Parameter tested on all production units at +105°C only. C grade at −25°C also.

[4]Maximum deviation between +25°C readings after a temperature cycle between −45°C and +125°C. Errors of this type are noncummulative.

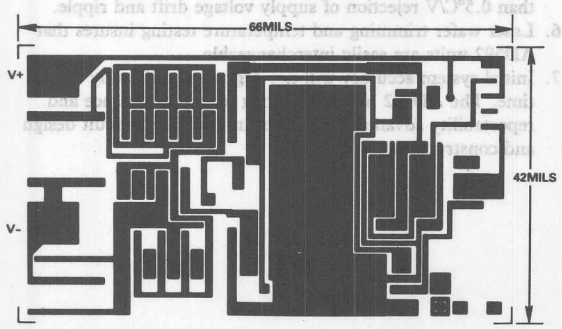
[5]Operation @125°C, error over time is noncummulative.

[6]Although performance is not specified beyond the operating temperature range, temperature excursions within the package temperature range will not damage the device.

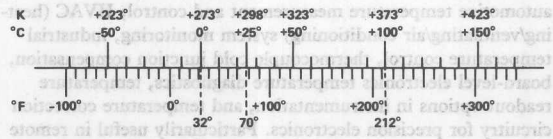
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION DIAGRAM



THE AD592 IS AVAILABLE IN LASER-TRIMMED CHIP FORM.



TEMPERATURE SCALE CONVERSION EQUATIONS

$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

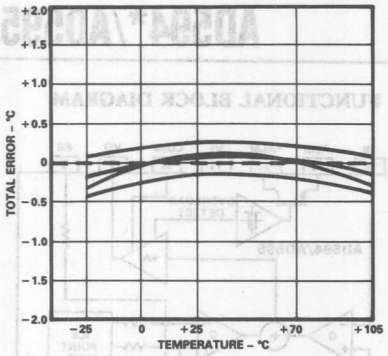
ORDERING GUIDE

Model	Max Cal Error @ 25°C	Max Error −25°C to +105°C	Max Nonlinearity −25°C to +105°C	Package Option*
AD592CN	0.5°C	1.0°C	0.35°C	TO-92
AD592BN	1.0°C	2.0°C	0.4°C	TO-92
AD592AN	2.5°C	3.5°C	0.5°C	TO-92

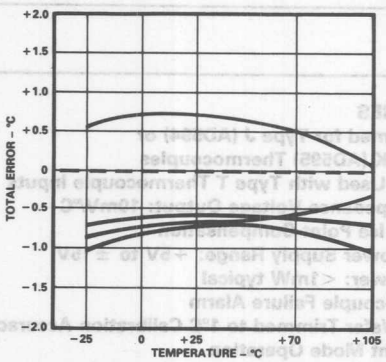
*For outline information see Package Information section.

Typical Performance Curves

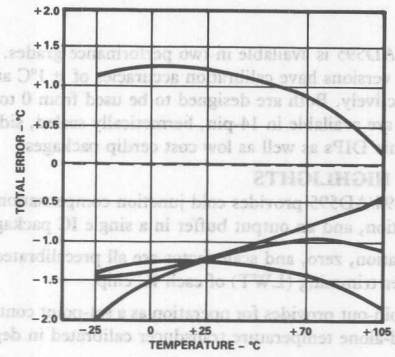
Typical @ V_S = +5V



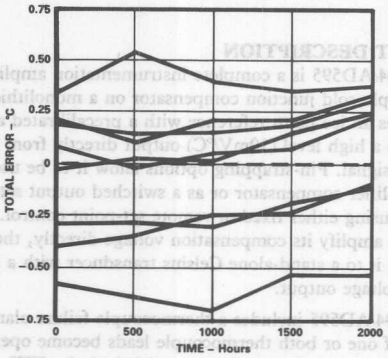
AD592CN Accuracy Over Temperature



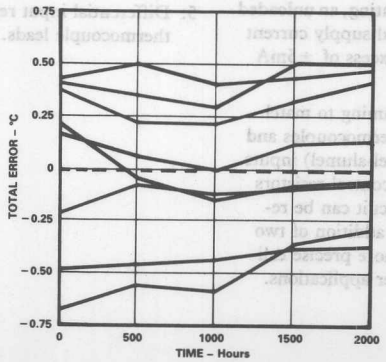
AD592BN Accuracy Over Temperature



AD592AN Accuracy Over Temperature



Long-Term Stability @ 85°C and 85% Relative Humidity



Long-Term Stability @ 125°C

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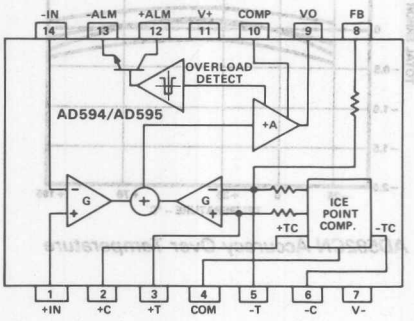
Monolithic Thermocouple Amplifiers with Cold Junction Compensation

AD594*/AD595*

FEATURES

- Pretrimmed for Type J (AD594) or Type K (AD595) Thermocouples
- Can Be Used with Type T Thermocouple Inputs
- Low Impedance Voltage Output: 10mV/°C
- Built-in Ice Point Compensation
- Wide Power Supply Range: +5V to ±15V
- Low Power: <1mW typical
- Thermocouple Failure Alarm
- Laser Wafer Trimmed to 1°C Calibration Accuracy
- Set-Point Mode Operation
- Self-Contained Celsius Thermometer Operation
- High Impedance Differential Input
- Side-Brazed DIP or Low Cost Cerdip

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to produce a high level (10mV/°C) output directly from a thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby converting it to a stand-alone Celsius transducer with a low-impedance voltage output.

The AD594/AD595 includes a thermocouple failure alarm that indicates if one or both thermocouple leads become open. The alarm output has a flexible format which includes TTL drive capability.

The AD594/AD595 can be powered from a single ended supply (including +5V) and by including a negative supply, temperatures below 0°C can be measured. To minimize self-heating, an unloaded AD594/AD595 will typically operate with a total supply current of 160μA, but is also capable of delivering in excess of ±5mA to a load.

The AD594 is precalibrated by laser wafer trimming to match the characteristic of type J (iron-constantan) thermocouples and the AD595 is laser trimmed for type K (chromel-alumel) inputs. The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit can be recalibrated for other thermocouple types by the addition of two or three resistors. These terminals also allow more precise calibration for both thermocouple and thermometer applications.

***Protected by U.S. Patent No. 4,029,974.**

The AD594/AD595 is available in two performance grades. The C and the A versions have calibration accuracies of ±1°C and ±3°C, respectively. Both are designed to be used from 0 to +50°C, and are available in 14-pin, hermetically sealed, side-brazed ceramic DIPs as well as low cost cerdip packages.

PRODUCT HIGHLIGHTS

1. The AD594/AD595 provides cold junction compensation, amplification, and an output buffer in a single IC package.
2. Compensation, zero, and scale factor are all precalibrated by laser wafer trimming (LWT) of each IC chip.
3. Flexible pin-out provides for operation as a set-point controller or a stand-alone temperature transducer calibrated in degrees Celsius.
4. Operation at remote application sites is facilitated by low quiescent current and a wide supply voltage range of +5V to dual supplies spanning 30V.
5. Differential input rejects common-mode noise voltage on the thermocouple leads.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C and V_S = 5 V, Type J (AD594), Type K (AD595) Thermocouple, unless otherwise noted)

Model	AD594A Min	AD594A Typ	AD594A Max	AD594C Min	AD594C Typ	AD594C Max	AD595A Min	AD595A Typ	AD595A Max	AD595C Min	AD595C Typ	AD595C Max	Units
ABSOLUTE MAXIMUM RATINGS													
$+V_S$ to $-V_S$			36			36			36			36	Volts
Common-Mode Input Voltage	$-V_S$ −0.15		$+V_S$	$-V_S$ −0.15		$+V_S$	$-V_S$ −0.15		$+V_S$	$-V_S$ −0.15		$+V_S$	Volts
Differential Input Voltage	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Alarm Voltages													
+ALM	$-V_S$		$-V_S$ +36	$-V_S$		$-V_S$ +36	$-V_S$		$-V_S$ +36	$-V_S$		$-V_S$ +36	Volts
−ALM	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Operating Temperature Range	−55		+125	−55		+125	−55		+125	−55		+125	°C
Output Short Circuit to Common	Indefinite			Indefinite			Indefinite			Indefinite			
TEMPERATURE MEASUREMENT													
(Specified Temperature Range 0 to +50°C)													
Calibration Error at +25°C[1]			±3			±1			±3			±1	°C
Stability vs. Temperature[2]			±0.05			±0.025			±0.05			±0.025	°C/°C
Gain Error			±1.5			±0.75			±1.5			±0.75	%
Nominal Transfer Function			10			10			10			10	mV/°C
AMPLIFIER CHARACTERISTICS													
Closed Loop Gain[3]		193.4			193.4			247.3			247.3		
Input Offset Voltage	(Temperature in °C)×51.70 µV/°C			(Temperature in °C)×51.70 µV/°C			(Temperature in °C)×40.44 µV/°C			(Temperature in °C)×40.44 µV/°C			µV
Input Bias Current		0.1			0.1			0.1			0.1		µA
Differential Input Range	−10		+50				−10		+50	−10		+50	mV
Common-Mode Range	$-V_S$ −0.15		$+V_S$ −4	$-V_S$ −0.15		$+V_S$ −4	$-V_S$ −0.15		$+V_S$ −4	$-V_S$ −0.15		$+V_S$ −4	Volts
Common-Mode Sensitivity – RTO			10			10			10			10	mV/V
Power Supply Sensitivity – RTO			10			10			10			10	mV/V
Output Voltage Range													
Dual Supplies	$-V_S$ +2.5		$+V_S$ −2	$-V_S$ +2.5		$+V_S$ −2	$-V_S$ +2.5		$+V_S$ −2	$-V_S$ +2.5		$+V_S$ −2	Volts
Single Supply	0		$+V_S$ −2	0		$+V_S$ −2	0		$+V_S$ +2	0		$+V_S$ −2	Volts
Usable Output Current[4]		±5			±5			±5			±5		mA
3 dB Bandwidth		15			15			15			15		kHz
ALARM CHARACTERISTICS													
$V_{CE(SAT)}$ at 2 mA		0.3			0.3			0.3			0.3		Volts
Leakage Current			±1			±1			±1			±1	µA max
Operating Voltage at – ALM			$+V_S$ −4			$+V_S$ −4			$+V_S$ −4			$+V_S$ −4	Volts
Short Circuit Current		20			20			20			20		mA
POWER REQUIREMENTS													
Specified Performance		$+V_S$ = 5, $-V_S$ = 0			$+V_S$ = 5, $-V_S$ = 0			$+V_S$ = 5, $-V_S$ = 0			$+V_S$ = 5, $-V_S$ = 0		Volts
Operating[5]		$+V_S$ to $-V_S$ ≤30			$+V_S$ to $-V_S$ ≤30			$+V_S$ to $-V_S$ ≤30			$+V_S$ to $-V_S$ ≤30		Volts
Quiescent Current (No Load)													
$+V_S$		160	300		160	300		160	300		160	300	µA
$-V_S$		100			100			100			100		µA
PACKAGE OPTION[6]													
TO-116 (D-14)		AD594AD			AD594CD			AD595AD			AD595CD		
Cerdip (Q-14)		AD594AQ			AD594CQ			AD595AQ			AD595CQ		

NOTES

[1]Calibrated for minimum error at +25°C using a thermocouple sensitivity of 51.7 µV/°C. Since a J type thermocouple deviates from this straight line approximation, the AD594 will normally read 3.1 mV when the measuring junction is at 0°C. The AD595 will similarly read 2.7 mV at 0°C.

[2]Defined as the slope of the line connecting the AD594/AD595 errors measured at 0°C and 50°C ambient temperature.

[3]Pin 8 shorted to Pin 9.

[4]Current Sink Capability in single supply configuration is limited to current drawn to ground through a 50 kΩ resistor at output voltages below 2.5 V.

[5]$-V_S$ must not exceed −16.5 V.

[6]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

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Thermocouple Temperature °C	Type J Voltage mV	AD594 Output mV	Type K Voltage mV	AD595 Output mV	Thermocouple Temperature °C	Type J Voltage mV	AD594 Output mV	Type K Voltage mV	AD595 Output mV
−200	−7.890	−1523	−5.891	−1454	500	27.388	5300	20.640	5107
−180	−7.402	−1428	−5.550	−1370	520	28.511	5517	21.493	5318
−160	−6.821	−1316	−5.141	−1269	540	29.642	5736	22.346	5529
−140	−6.159	−1188	−4.669	−1152	560	30.782	5956	23.198	5740
−120	−5.426	−1046	−4.138	−1021	580	31.933	6179	24.050	5950
−100	−4.632	−893	−3.553	−876	600	33.096	6404	24.902	6161
−80	−3.785	−729	−2.920	−719	620	34.273	6632	25.751	6371
−60	−2.892	−556	−2.243	−552	640	35.464	6862	26.599	6581
−40	−1.960	−376	−1.527	−375	660	36.671	7095	27.445	6790
−20	−.995	−189	−.777	−189	680	37.893	7332	28.288	6998
−10	−.501	−94	−.392	−94	700	39.130	7571	28.128	7206
0	0	3.1	0	2.7	720	40.382	7813	29.965	7413
10	.507	101	.397	101	740	41.647	8058	30.799	7619
20	1.019	200	.798	200	750	42.283	8181	31.214	7722
25	1.277	250	1.000	250	760	–	–	31.629	7825
30	1.536	300	1.203	300	780	–	–	32.455	8029
40	2.058	401	1.611	401	800	–	–	33.277	8232
50	2.585	503	2.022	503	820	–	–	34.095	8434
60	3.115	606	2.436	605	840	–	–	34.909	8636
80	4.186	813	3.266	810	860	–	–	35.718	8836
100	5.268	1022	4.095	1015	880	–	–	36.524	9035
120	6.359	1233	4.919	1219	900	–	–	37.325	9233
140	7.457	1445	5.733	1420	920	–	–	38.122	9430
160	8.560	1659	6.539	1620	940	–	–	38.915	9626
180	9.667	1873	7.338	1817	960	–	–	39.703	9821
200	10.777	2087	8.137	2015	980	–	–	40.488	10015
220	11.887	2302	8.938	2213	1000	–	–	41.269	10209
240	12.998	2517	9.745	2413	1020	–	–	42.045	10400
260	14.108	2732	10.560	2614	1040	–	–	42.817	10591
280	15.217	2946	11.381	2817	1060	–	–	43.585	10781
300	16.325	3160	12.207	3022	1080	–	–	44.349	10970
320	17.432	3374	13.039	3327	1100	–	–	45.108	11158
340	18.537	3588	13.874	3434	1120	–	–	45.863	11345
360	19.640	3801	14.712	3641	1140	–	–	46.612	11530
380	20.743	4015	15.552	3849	1160	–	–	47.356	11714
400	21.846	4228	16.395	4057	1180	–	–	48.095	11897
420	22.949	4441	17.241	4266	1200	–	–	48.828	12078
440	24.054	4655	18.088	4476	1220	–	–	49.555	12258
460	25.161	4869	18.938	4686	1240	–	–	50.276	12436
480	26.272	5084	19.788	4896	1250	–	–	50.633	12524

Table I. Output Voltage vs. Thermocouple Temperature (Ambient +25°C, V_S = −5V, +15V)

INTERPRETING AD594/AD595 OUTPUT VOLTAGES

To achieve a temperature proportional output of 10mV/°C and accurately compensate for the reference junction over the rated operating range of the circuit, the AD594/AD595 is gain trimmed to match the transfer characteristic of J and K type thermocouples at 25°C. For a type J output in this temperature range the TC is 51.70μV/°C, while for a type K it is 40.44μV/°C. The resulting gain for the AD594 is 193.4 (10mV/°C divided by 51.7μV/°C) and for the AD595 is 247.3 (10mV/°C divided by 40.44μV/°C). In addition, an absolute accuracy trim induces an input offset to the output amplifier characteristic of 16μV for the AD594 and 11μV for the AD595. This offset arises because the AD594/AD595 is trimmed for a 250mV output while applying a 25°C thermocouple input.

Because a thermocouple output voltage is nonlinear with respect to temperature, and the AD594/AD595 linearly amplifies the compensated signal, the following transfer functions should be used to determine the actual output voltages:

AD594 output = (Type J Voltage + 16μV) × 193.4

AD595 output = (Type K Voltage + 11μV) × 247.3

or conversely:

Type J voltage = (AD594 output / 193.4) − 16μV

Type K voltage = (AD595 output / 247.3) − 11μV

Table I above lists the ideal AD594/AD595 output voltages as a function of Celsius temperature for type J and K ANSI standard thermocouples, with the package and reference junction at 25°C. As is normally the case, these outputs are subject to calibration, gain and temperature sensitivity errors. Output values for intermediate temperatures can be interpolated, or calculated using the output equations and ANSI thermocouple voltage tables referred to zero degrees Celsius. Due to a slight variation in alloy content between ANSI type J and DIN Fe–CuNi thermocouples Table I should not be used in conjunction with European standard thermocouples. Instead the transfer function given previously and a DIN thermocouple table should be used. ANSI type K and DIN NiCr–Ni thermocouples are composed of identical alloys and exhibit similar behavior. The upper temperature limits in Table I are those recommended for type J and type K thermocouples by the majority of vendors.

Thermocouple Conditioner and Set-Point Controller

AD596*/AD597*

FEATURES
- Low Cost
- Operates with Type J (AD596) or Type K (AD597) Thermocouples
- Built-in Ice Point Compensation
- Temperature Proportional Operation – 10mV/°C
- Temperature Set-Point Operation – ON/OFF
- Programmable Switching Hysteresis
- High Impedance Differential Input

PRODUCT DESCRIPTION

The AD596/AD597 is a monolithic temperature set-point controller which has been optimized for use at elevated temperatures such as those found in oven control applications. The device cold junction compensates and amplifies a type J or K thermocouple input to derive an internal signal proportional to temperature. The internal signal is then compared with an externally applied set-point voltage to yield a low impedance switched output voltage. Dead-Band or switching hysteresis can be programmed using a single external resistor. Alternately, the AD596/AD597 can be configured to provide a voltage output (10mV/°C) directly from a type J or K thermocouple signal. It can also be used as a stand-alone voltage output temperature sensor.

The AD596/AD597 can be powered with a single supply from +5V to +30V, or dual supplies up to a total span of 36V. Typical quiescent supply current is 160μA which minimizes self-heating errors.

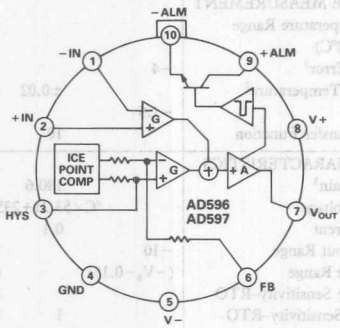
The AD596/AD597 H package option includes a thermocouple failure alarm that indicates an open thermocouple lead when operated in the temperature proportional measurement mode. The alarm output has a flexible format which can be used to drive relays, LEDs or TTL logic.

The device is packaged in a reliability qualified, cost effective 10-pin metal can, 8-pin plastic minidip or SOIC and is trimmed to operate over an ambient temperature range from +25°C to +100°C. Operation over an extended ambient temperature range is possible with slightly reduced accuracy. The AD596 will amplify thermocouple signals covering the entire −200°C to +760°C temperature range recommended for type J thermocouples while the AD597 can accommodate −200°C to +1250°C type K inputs.

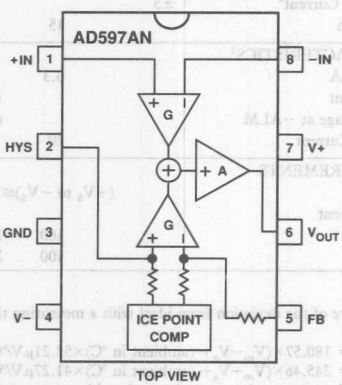
The AD596/AD597 has a calibration accuracy of ±4°C at an ambient temperature of 60°C and an ambient temperature stability specification of 0.05°C/°C from +25°C to +100°C. If higher accuracy, or a lower ambient operating temperature is required, either the AD594 (J thermocouple) or AD595 (K thermocouple) should be considered.

FUNCTIONAL BLOCK DIAGRAMS

TO-100
(H) Package



8-Pin Plastic Mini-DIP (N) Package
or SOIC (R) Package



PRODUCT HIGHLIGHTS

1. The AD596/AD597 provides cold junction compensation and a high gain amplifier which can be used as a set-point comparator.
2. The input stage of the AD596/AD597 is a high quality instrumentation amplifier that allows the thermocouple to float over most of the supply voltage range.
3. Linearization not required for thermocouple temperatures close to 175°C (+100°C to +540°C for AD596).
4. Cold junction compensation is optimized for ambient temperatures ranging from +25°C to +100°C.
5. In the stand-alone mode, the AD596/AD597 produces an output voltage that indicates its own temperature.

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*Protected by U.S. Patent No. 4,029,974.

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AD596/AD597 — SPECIFICATIONS (@ +60°C and V_S = 10V, Type J (AD596), Type K (AD597)

Common-Mode Input Voltage	($-V_S$ −0.15)		$+V_S$	($-V_S$ −0.15)		$+V_S$	($-V_S$ −0.15)		$+V_S$	Volts
Differential Input Voltage	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Alarm Voltages										
+ALM	$-V_S$		($-V_S$ +36)	$-V_S$		($-V_S$ +36)	$-V_S$		($-V_S$ +36)	Volts
−ALM	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Operating Temperature Range	−55		+125	−55		+125	−40		+125	°C
Output Short Circuit to Common	Indefinite			Indefinite			Indefinite			
TEMPERATURE MEASUREMENT										
(Specified Temperature Range +25°C to +100°C)										
Calibration Error[1]	**−4**		**+4**	**−4**		**+4**	**−4**		**+4**	°C
Stability vs. Temperature[2]		±0.02	±0.05		±0.02	±0.05		±0.02	±0.05	°C/°C
Gain Error	**−1.5**		**+1.5**	**−1.5**		**+1.5**	**−1.5**		**+1.5**	%
Nominal Transfer Function		10			10			10		mV/°C
AMPLIFIER CHARACTERISTICS										
Closed Loop Gain[3]		180.6			245.5			245.5		V/V
Input Offset Voltage		°C×53.21+235			°C×41.27−37			°C×41.27−37		µV
Input Bias Current		0.1			0.1			0.1		µA
Differential Input Range	−10		+50	−10		+50	−10		+50	mV
Common Mode Range	($-V_S$−0.15)		($+V_S$−4)	($+V_S$−0.15)		($+V_S$−4)	($-V_S$−0.15)		($+V_S$−4)	Volts
Common Mode Sensitivity–RTO			**10**			**10**			**10**	mV/V
Power Supply Sensitivity–RTO		1	**10**		1	**10**		1	**10**	mV/V
Output Voltage Range										
Dual Supplies	**($-V_S$+2.5)**		**($+V_S$−2)**	**($-V_S$+2.5)**		**($+V_S$−2)**	**($-V_S$+2.5)**		**($+V_S$−2)**	Volts
Single Supply	**0**		**($+V_S$−2)**	**0**		**($+V_S$−2)**	**0**		**($+V_S$−2)**	Volts
Usable Output Current[4]	±5			±5			±5			mA
3dB Bandwidth		15			15			15		kHz
ALARM CHARACTERISTICS[5]							Alarm Function Not Pinned Out			
$V_{CE(SAT)}$ at 2mA		0.3			0.3					Volts
Leakage Current			**±1**			**±1**				µA
Operating Voltage at −ALM			**($+V_S$−4)**			**($+V_S$−4)**				Volts
Short Circuit Current		20			20					mA
POWER REQUIREMENTS										
Operating	($+V_S$ to $-V_S$)≤30			($+V_S$ to $-V_S$)≤30			($+V_S$ to $-V_S$)≤30			Volts
Quiescent Current										
$+V_S$		160	**300**		160	**300**		160	**300**	µA
$-V_S$		100	**200**		100	**200**		100	**200**	µA

NOTES

[1]This is a measure of the deviation from ideal with a measuring thermocouple junction of 175°C and a chip temperature of 60°C. The ideal transfer function is given by:

AD596: V_{OUT} = 180.57×(V_m−V_a+ (ambient in °C)×53.21µV/°C +235µV)

AD597: V_{OUT} = 245.46×(V_m−V_a+ (ambient in °C)×41.27µV/°C −37µV)

where V_m and V_a represent the measuring and ambient temperatures and are taken from the appropriate J or K thermocouple table. The ideal transfer function minimizes the error over the ambient temperature range of 25°C to 100°C with a thermocouple temperature of approximately 175°C.

[2]Defined as the slope of the line connecting the AD596/AD597 CJC errors measured at 25°C and 100°C ambient temperature.

[3]Pin 6 shorted to pin 7.

[4]Current Sink Capability in single supply configuration is limited to current drawn to ground through a 50kΩ resistor at output voltages below 2.5V.

[5]Alarm function available on H package option only.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Model	Package Description	Package Option[1]
AD596AH	TO-100	H-10A
AD597AH	TO-100	H-10A
AD597AN[2]	Plastic DIP	N-8
AD597AR[2]	SOIC	R-8

NOTES

[1]For outline information see Package Information section.

[2]Consult factory for availability.

Thermocouple Temperature °C	Type J Voltage mV	AD596 Output mV	Type K Voltage mV	AD597 Output mV
−200	−7.890	−1370	−5.891	−1446
−180	−7.402	−1282	−5.550	−1362
−160	−6.821	−1177	−5.141	−1262
−140	−6.159	−1058	−4.669	−1146
−120	−5.426	−925	−4.138	−1016
−100	−4.632	−782	−3.553	−872
−80	−3.785	−629	−2.920	−717
−60	−2.892	−468	−2.243	−551
−40	−1.960	−299	−1.527	−375
−20	−.995	−125	−.777	−191
−10	−.501	−36	−.392	−96
0	0	54	0	0
10	.507	146	.397	97
20	1.019	238	.798	196
25	1.277	285	1.000	245
30	1.536	332	1.203	295
40	2.058	426	1.611	395
50	2.585	521	2.022	496
60	3.115	617	2.436	598
80	4.186	810	3.266	802
100	5.268	1006	4.095	1005
120	6.359	1203	4.919	1207
140	7.457	1401	5.733	1407
160	8.560	1600	6.539	1605
180	9.667	1800	7.338	1801
200	10.777	2000	8.137	1997
220	11.887	2201	8.938	2194
240	12.998	2401	9.745	2392
260	14.108	2602	10.560	2592
280	15.217	2802	11.381	2794
300	16.325	3002	12.207	2996
320	17.432	3202	13.039	3201
340	18.537	3402	13.874	3406
360	19.640	3601	14.712	3611
380	20.743	3800	15.552	3817
400	21.846	3999	16.395	4024
420	22.949	4198	17.241	4232
440	24.054	4398	18.088	4440
460	25.161	4598	18.938	4649
480	26.272	4798	19.788	4857
500	27.388	5000	20.640	5066
520	28.511	5203	21.493	5276
540	29.642	5407	22.346	5485
560	30.782	5613	23.198	5694
580	31.933	5821	24.050	5903
600	33.096	6031	24.902	6112
620	34.273	6243	25.751	6321
640	35.464	6458	26.599	6529
660	36.671	6676	27.445	6737
680	37.893	6897	28.288	6944
700	39.130	7120	29.128	7150
720	40.382	7346	29.965	7355
740	41.647	7575	30.799	7560
750	42.283	7689	31.214	7662
760	–	–	31.629	7764
780	–	–	32.455	7966
800	–	–	33.277	8168
820	–	–	34.095	8369
840	–	–	34.909	8569
860	–	–	35.718	8767
880	–	–	36.524	8965
900	–	–	37.325	9162
920	–	–	38.122	9357
940	–	–	38.915	9552
960	–	–	39.703	9745
980	–	–	40.488	9938
1000	–	–	41.269	10130
1020	–	–	42.045	10320
1040	–	–	42.817	10510
1060	–	–	43.585	10698
1080	–	–	44.439	10908
1100	–	–	45.108	11072
1120	–	–	45.863	11258
1140	–	–	46.612	11441
1160	–	–	47.356	11624
1180	–	–	48.095	11805
1200	–	–	48.828	11985
1220	–	–	49.555	12164
1240	–	–	50.276	12341
1250	–	–	50.633	12428

Table I. Output Voltage vs. Thermocouple Temperature (Ambient +60°C, V_S = −5V, +15V)

TEMPERATURE PROPORTIONAL OUTPUT MODE

The AD596/AD597 can be used to generate a temperature proportional output of 10mV/°C when operated with J and K type thermocouples as shown in Figure 1. Thermocouples produce low level output voltages which are a function of both the temperature being measured and the reference or cold junction temperature. The AD596/AD597 compensates for the cold junction temperature and amplifies the thermocouple signal to produce a high level 10mV/°C voltage output which is a function only of the temperature being measured. The temperature stability of the part indicates the sensitivity of the output voltage to changes in ambient or device temperatures. This is typically 0.02°C/°C over the +25°C to +100°C recommended ambient temperature range. The parts will operate over the extended ambient temperature ranges from −55°C to +125°C, but thermocouple nonlinearity at the reference junction will degrade the temperature stability over this extended range. Table I is a list of ideal AD596/AD597 output voltages as a function of Celsius temperature for type J and K ANSI standard thermocouples with package and reference junction at 60°C. As is normally the case, these outputs

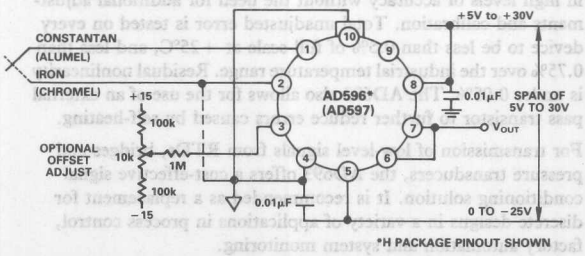

Figure 1. Temperature Proportional Output Connection

are subject to calibration and temperature sensitivity errors. These tables are derived using the ideal transfer functions:

AD596 output = (Type J voltage +301.5µV) × 180.57
AD597 output = (Type K voltage) × 245.46

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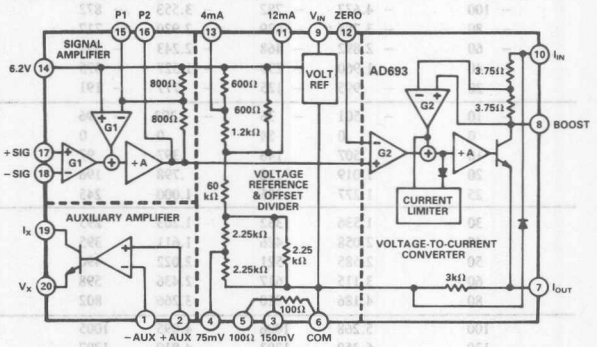
Loop-Powered 4–20mA Sensor Transmitter

AD693

FEATURES

Instrumentation Amplifier Front End
Loop-Powered Operation
Precalibrated 30mV or 60mV Input Spans
Independently Adjustable Output Span and Zero
Precalibrated Output Spans: 4–20mA Unipolar
0–20mA Unipolar
12 ± 8mA Bipolar
Precalibrated 100Ω RTD Interface
6.2V Reference with Up to 3.5mA of Current Available
Uncommitted Auxiliary Amp for Extra Flexibility
Optional External Pass Transistor to Reduce Self-Heating Errors

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD693 is a monolithic signal conditioning circuit which accepts low-level inputs from a variety of transducers to control a standard 4–20mA, two-wire current loop. An on-chip voltage reference and auxiliary amplifier are provided for transducer excitation; up to 3.5mA of excitation current is available when the device is operated in the loop-powered mode. Alternatively, the device may be locally powered for three-wire applications when 0–20mA operation is desired.

Precalibrated 30mV and 60mV input spans may be set by simple pin strapping. Other spans from 1mV to 100mV may be realized with the addition of external resistors. The auxiliary amplifier may be used in combination with on-chip voltages to provide six precalibrated ranges for 100Ω RTDs. Output span and zero are also determined by pin strapping to obtain the standard ranges: 4–20mA, 12 ± 8mA and 0–20mA.

Active laser trimming of the AD693's thin-film resistors result in high levels of accuracy without the need for additional adjustments and calibration. Total unadjusted error is tested on every device to be less than 0.5% of full scale at +25°C, and less than 0.75% over the industrial temperature range. Residual nonlinearity is under 0.05%. The AD693 also allows for the use of an external pass transistor to further reduce errors caused by self-heating.

For transmission of low-level signals from RTDs, bridges and pressure transducers, the AD693 offers a cost-effective signal conditioning solution. It is recommended as a replacement for discrete designs in a variety of applications in process control, factory automation and system monitoring.

The AD693 is packaged in a 20-pin ceramic side-brazed DIP, 20-pin Cerdip, and 20-pin LCCC and is specified over the −40°C to +85°C industrial temperature range.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. The AD693 is a complete monolithic low-level voltage-to-current loop signal conditioner.
2. Precalibrated output zero and span options include 4–20mA, 0–20mA, and 12 ± 8mA in two- and three-wire configurations.
3. Simple resistor programming adds a continuum of ranges to the basic 30mV and 60mV input spans.
4. The common-mode range of the signal amplifier input extends from ground to near the device's operating voltage.
5. Provision for transducer excitation includes a 6.2V reference output and an auxiliary amplifier which may be configured for voltage or current output and signal amplification.
6. The circuit configuration permits simple linearization of bridge, RTD, and other transducer signals.
7. A monitored output is provided to drive an external pass transistor. This feature off-loads power dissipation to extend the temperature range of operation, enhance reliability, and minimize self-heating errors.
8. Laser-wafer trimming results in low unadjusted errors and affords precalibrated input and output spans.
9. Zero and span are independently adjustable and noninteractive to accommodate transducers or user defined ranges.
10. Six precalibrated temperature ranges are available with a 100Ω RTD via pin strapping.

SPECIFICATIONS (@ +25°C and V_S = +24V. Input Span = 30mV or 60mV, Output Span = 4–20mA, R_L = 250Ω, V_{CM} = 3.1V, with external pass transistor unless otherwise noted)

Model	Conditions	AD693AD/AQ/AE Min	Typ	Max	Units
LOOP-POWERED OPERATION					
TOTAL UNADJUSTED ERROR[1, 2]			±0.25	**±0.5**	% Full Scale
T_{min} to T_{max}			±0.4	**±0.75**	% Full Scale
100Ω RTD CALIBRATION ERROR[3]	(See Fig. 17)		±0.5	±2.0	°C
LOOP POWERED OPERATION[2]					
Zero Current Error[4]	Zero = 4mA		±25	**±80**	µA
	Zero = 12mA		±40	**±120**	µA
	Zero = 0mA[5]	+7	+35	**+100**	µA
vs. Temp.	Zero = 4mA		±0.5	±1.5	µA/°C
Power Supply Rejection (RTI)	12V ≤ V_{OP} ≤ 36V[6]		±3.0	**±5.6**	µV/V
	0V ≤ V_{CM} ≤ 6.2V				
Common-Mode Input Range	(See Fig. 3)	0		$+V_{OP}-4V$[6]	V
Common-Mode Rejection (RTI)	0V ≤ V_{CM} ≤ 6.2V		±10	**±30**	µV/V
Input Bias Current[7]			+5	**+20**	nA
T_{min} to T_{max}			+7	**+25**	nA
Input Offset Current[7]	V_{SIG} = 0		±0.5	**±3.0**	nA
Transconductance					
Nominal	30mV Input Span		0.5333		A/V
	60mV Input Span		0.2666		A/V
Unadjusted Error			±0.05	**±0.2**	%
vs. Common-Mode	0V ≤ V_{CM} ≤ 6.2V				
	30mV Input Span		±0.03	±0.04	%/V
	60mV Input Span		±0.05	±0.06	%/V
Error vs. Temp.			±20	±50	ppm/°C
Nonlinearity[8]	30mV Input Span		±0.01	**±0.05**	% of Span
	60mV Input Span		±0.02	**±0.07**	% of Span
OPERATIONAL VOLTAGE RANGE					
Operational Voltage, V_{OP}[6]		**+12**		**+36**	V
Quiescent Current	Into Pin 9		+500	**+700**	µA
OUTPUT CURRENT LIMIT		**+21**	+25	+32	mA
COMPONENTS OF ERROR					
SIGNAL AMPLIFIER[9]					
Input Voltage Offset			±40	**±200**	µV
vs. Temp			±1.0	±2.5	µV/°C
Power Supply Rejection	12V ≤ V_{OP} ≤ 36V[6]		±3.0	**±5.6**	µV/V
	0V ≤ V_{CM} ≤ 6.2V				
V/I CONVERTER[9, 10]					
Zero Current Error	Output Span = 4–20mA		±30	±80	µA
Power Supply Rejection	12V ≤ V_{OP} ≤ 36V[6]		±1.0	±3.0	µA/V
Transconductance					
Nominal			0.2666		A/V
Unadjusted Error			±0.05	±0.2	%
6.200V REFERENCE[9, 12]					
Output Voltage Tolerance			±3	**±12**	mV
vs. Temp.			±20	±50	ppm/°C
Line Regulation	12V ≤ V_{OP} ≤ 36V[6]		±200	**±300**	µV/V
Load Regulation[11]	0mA ≤ I_{REF} ≤ 3mA		±0.3	**±0.75**	mV/mA
Output Current[13]	Loop Powered, (Fig. 10)	**+3.0**	+3.5		mA
	3-Wire Mode, (Fig. 15)		+5.0		mA

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AUXILIARY AMPLIFIER					
Common-Mode Range		0		$+V_{OP}-4V^{6}$	V
Input Offset Voltage			±50	±200	μV
Input Bias Current			+5	+20	nA
Input Offset Current			+0.5	±3.0	nA
Common-Mode Rejection			90		dB
Power Supply Rejection			105		dB
Output Current Range	Pin I_X OUT	+0.01		+5	mA
Output Current Error	Pin V_X − Pin I_X		±0.005		%
TEMPERATURE RANGE					
Case Operating[14]	T_{min} to T_{max}	−40		+85	°C
Storage		−65		+150	°C

NOTES

[1]Total error can be significantly reduced (typically less than 0.1%) by trimming the zero current. The remaining unadjusted error sources are transconductance and nonlinearity.

[2]The AD693 is tested as a loop powered device with the signal amp, V/I converter, voltage reference, and application voltages operating together. Specifications are valid for preset spans and spans between 30mV and 60mV.

[3]Error from ideal output assuming a perfect 100Ω RTD at 0 and +100°C.

[4]Refer to the Error Analysis to calculate zero current error for input spans less than 30mV.

[5]By forcing the differential signal amplifier input sufficiently negative the 7μA zero current can always be achieved.

[6]The operational voltage (V_{OP}) is the voltage directly across the AD693 (Pin 10 to 6 in two-wire mode, Pin 9 to 6 in local power mode). For example, $V_{OP} = V_S - (I_{LOOP} \times R_L)$ in two-wire mode (refer to Figure 10).

[7]Bias currents are not symmetrical with input signal level and flow out of the input pins. The input bias current of the inverting input increases with input signal voltage, see Figure 2.

[8]Nonlinearity is defined as the deviation of the output from a straight line connecting the endpoints as the input is swept over a 30mV and 60mV input span.

[9]Specifications for the individual functional blocks are components of error that contribute to, and that are included in, the Loop Powered Operation specifications.

[10]Includes error contributions of V/I converter and Application Voltages.

[11]Changes in the reference output voltage due to load will affect the Zero Current. A 1% change in the voltage reference output will result in an error of 1% in the value of the Zero Current.

[12]If not used for external excitation, the reference should be loaded by approximately 1mA (6.2kΩ to common).

[13]In the loop powered mode up to 5mA can be drawn from the reference, however, the lower limit of the output span will be increased accordingly. 3.5mA is the maximum current the reference can source while still maintaining a 4mA zero.

[14]The AD693 is tested with a pass transistor so $T_A \cong T_C$.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

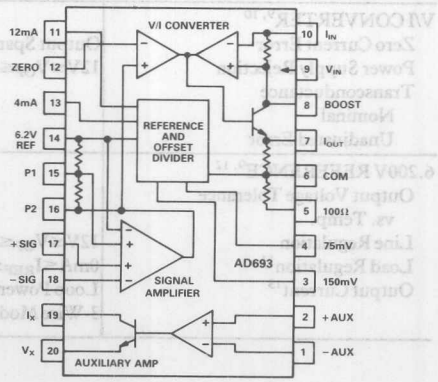
Supply Voltage . . . . . +36V
Reverse Loop Current 200mA
Signal Amp Input Range . . . . . −0.3V to V_{OP}
Reference Short Circuit to Common . . . . . Indefinite
Auxiliary Amp Input Voltage Range . . . . . −0.3V to V_{OP}
Auxiliary Amp Current Output 10mA
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature, 10sec Soldering . . . . . +300°C
Max Junction Temperature . . . . . +150°C

ORDERING GUIDE

Model	Package Description	Package Option*
AD693AD	Ceramic Side-Brazed DIP	D-20
AD693AQ	Cerdip	Q-20
AD693AE	Leadless Ceramic Chip Carrier (LCCC)	E-20A

*For outline information see Package Information section.

AD693 PIN CONFIGURATION (AD, AW, AE Packages)



Functional Diagram

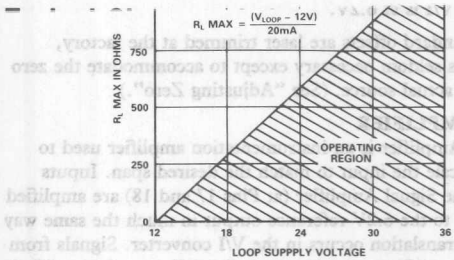


Figure 1. Maximum Load Resistance vs. Power Supply

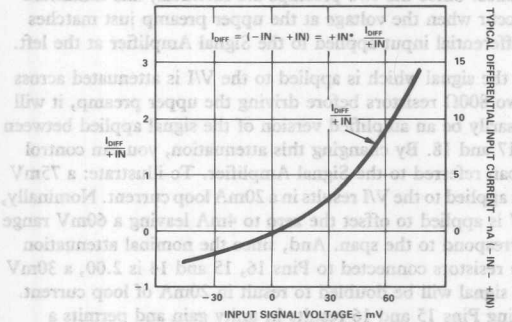


Figure 2. Differential Input Current vs. Input Signal Voltage Normalized to +IN

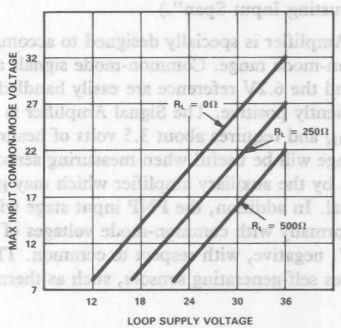


Figure 3. Maximum Common-Mode Voltage vs. Supply

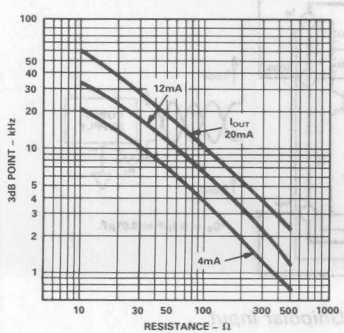


Figure 4. Bandwidth vs. Series Load Resistance

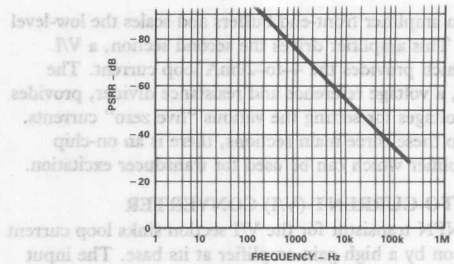


Figure 5. Signal Amplifier PSRR vs. Frequency

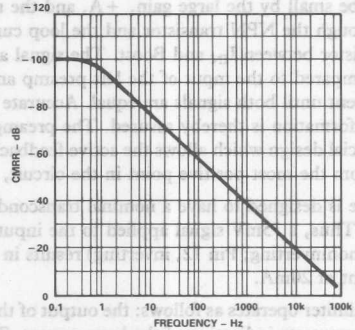


Figure 6. CMRR (RTI) vs. Frequency

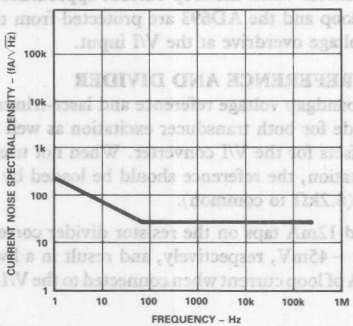


Figure 7. Input Current Noise vs. Frequency

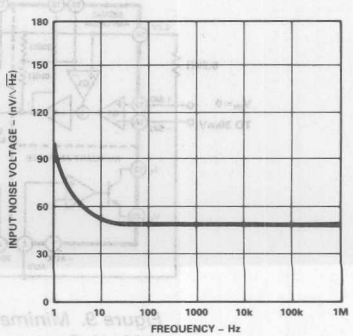


Figure 8. Input Voltage Noise vs. Frequency

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FUNCTIONAL DESCRIPTION

The operation of the AD693 can be understood by dividing the circuit into three functional parts (see Figure 9). First, an instrumentation amplifier front-end buffers and scales the low-level input signal. This amplifier drives the second section, a V/I converter, which provides the 4–to–20mA loop current. The third section, a voltage reference and resistance divider, provides application voltages for setting the various "live zero" currents. In addition to these three main sections, there is an on-chip auxiliary amplifier which can be used for transducer excitation.

VOLTAGE-TO-CURRENT (V/I) CONVERTER

The output NPN transistor for the V/I section sinks loop current when driven on by a high gain amplifier at its base. The input for this amplifier is derived from the difference in the outputs of the matched preamplifiers having gains, G2. This difference is caused to be small by the large gain, +A, and the negative feedback through the NPN transistor and the loop current sampling resistor between I_{IN} and Boost. The signal across this resistor is compared to the input of the left preamp and servos the loop current until both signals are equal. Accurate voltage-to-current transformation is thereby assured. The preamplifiers employ a special design which allows the active feedback amplifier to operate from the most positive point in the circuit, I_{IN}.

The V/I stage is designed to have a nominal transconductance of 0.2666 A/V. Thus, a 75mV signal applied to the inputs of the V/I (Pin 16, noninverting; Pin 12, inverting) results in a full-scale output current of 20mA.

The current limiter operates as follows: the output of the feedback preamp is an accurate indication of the loop current. This output is compared to an internal setpoint which backs off the drive to the NPN transistor when the loop current approaches 25mA. As a result, the loop and the AD693 are protected from the consequences of voltage overdrive at the V/I input.

VOLTAGE REFERENCE AND DIVIDER

A stabilized bandgap voltage reference and laser-trimmed resistor divider provide for both transducer excitation as well as precalibrated offsets for the V/I converter. When not used for external excitation, the reference should be loaded by approximately 1mA (6.2kΩ to common).

The 4mA and 12mA taps on the resistor divider correspond to −15mV and −45mV, respectively, and result in a live zero of 4mA or 12mA of loop current when connected to the V/I converter's inverting input (Pin 12). Arranging the zero offset in this way makes the zero signal output current independent of input span. When the input to the signal amp is zero, the noninverting input of the V/I is at 6.2V.

Since the standard offsets are laser trimmed at the factory, adjustment is seldom necessary except to accommodate the zero offset of the actual source. (See "Adjusting Zero".)

SIGNAL AMPLIFIER

The Signal Amplifier is an instrumentation amplifier used to buffer and scale the input to match the desired span. Inputs applied to the Signal Amplifier (at Pins 17 and 18) are amplified and referred to the 6.2V reference output in much the same way as the level translation occurs in the V/I converter. Signals from the two preamplifiers are subtracted, the difference is amplified, and the result is fed back to the upper preamp to minimize the difference. Since the two preamps are identical, this minimum will occur when the voltage at the upper preamp just matches the differential input applied to the Signal Amplifier at the left.

Since the signal which is applied to the V/I is attenuated across the two 800Ω resistors before driving the upper preamp, it will necessarily be an amplified version of the signal applied between Pins 17 and 18. By changing this attenuation, you can control the span referred to the Signal Amplifier. To illustrate: a 75mV signal applied to the V/I results in a 20mA loop current. Nominally, 15mV is applied to offset the zero to 4mA leaving a 60mV range to correspond to the span. And, since the nominal attenuation of the resistors connected to Pins 16, 15 and 14 is 2.00, a 30mV input signal will be doubled to result in 20mA of loop current. Shorting Pins 15 and 16 results in unity gain and permits a 60mV input span. Other choices of span may be implemented with user supplied resistors to modify the attenuation. (See section "Adjusting Input Span".)

The Signal Amplifier is specially designed to accommodate a large common-mode range. Common-mode signals anywhere up to and beyond the 6.2V reference are easily handled as long as V_{IN} is sufficiently positive. The Signal Amplifier is biased with respect to V_{IN} and requires about 3.5 volts of headroom. The extended range will be useful when measuring sensors driven, for example, by the auxiliary amplifier which may go above the 6.2V potential. In addition, the PNP input stage will continue to operate normally with common-mode voltages of several hundred mV, negative, with respect to common. This feature accommodates self-generating sensors, such as thermocouples,

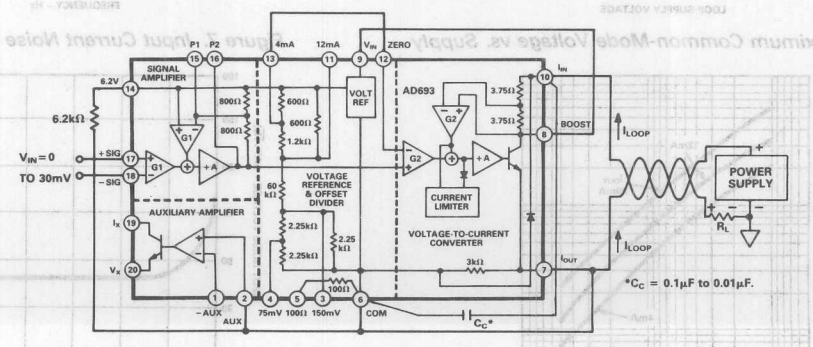


Figure 9. Minimal Connection for 0-30mV Unipolar Input, 4-20mA Output

which may produce small negative normal-mode signals as well as common-mode noise on "grounded" signal sources.

AUXILIARY AMPLIFIER

The Auxiliary Amplifier is included in the AD693 as a signal conditioning aid. It can be used as an op amp in noninverting applications and has special provisions to provide a controlled current output. Designed with a differential input stage and an unbiased Class A output stage, the amplifier can be resistively loaded to common with the self-contained 100Ω resistor or with a user supplied resistor.

As a functional element, the Auxiliary Amplifier can be used in dynamic bridges and arrangements such as the RTD signal conditioner shown in Figure 17. It can be used to buffer, amplify and combine other signals with the main Signal Amplifier. The Auxiliary Amplifier can also provide other voltages for excitation if the 6.2V of the reference is unsuitable. Configured as a simple follower, it can be driven from a user supplied voltage divider or the precalibrated outputs of the AD693 divider (Pins 3 and 4) to provide a stiff voltage output at less than the 6.2 level, or by incorporating a voltage divider as feedback around the amplifier, one can gain-up the reference to levels higher than 6.2V. If large positive outputs are desired, I_X, the Auxiliary Amplifier output current supply, should be strapped to either V_{IN} or Boost. Like the Signal Amplifier, the Auxiliary requires about 3.5V of headroom with respect to V_{IN} at its input and about 2V of difference between I_X and the voltage to which V_X is required to swing.

The output stage of the Auxiliary Amplifier is actually a high gain Darlington transistor where I_X is the collector and V_X is the emitter. Thus, the Auxiliary Amplifier can be used as a V/I converter when configured as a follower and resistively loaded. I_X functions as a high-impedance current source whose current is equal to the voltage at V_X divided by the load resistance. For example, using the onboard 100Ω resistor and the 75mV or 150mV application voltages, either a 750μA or 1.5mA current source can be set up for transducer excitation.

The I_X terminal has voltage compliance within 2V of V_X. If the Auxiliary Amplifier is not to be used, then Pin 2, the noninverting input, should be grounded.

REVERSE VOLTAGE PROTECTION FEATURE

In the event of a reverse voltage being applied to the AD693 through a current-limited loop (limited to 200mA), an internal shunt diode protects the device from damage. This protection mode avoids the compliance voltage penalty which results from a series diode that must be added if reversal protection is required in high-current loops.

APPLICATION EXAMPLES

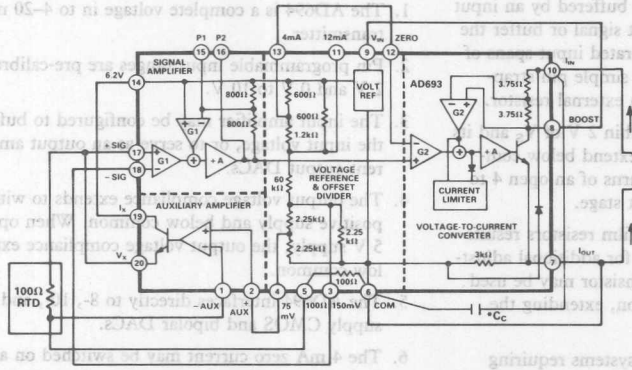


Figure 10. 0 to 104°C Direct Three-Wire 100Ω RTD Interface, 4-20 mA Output

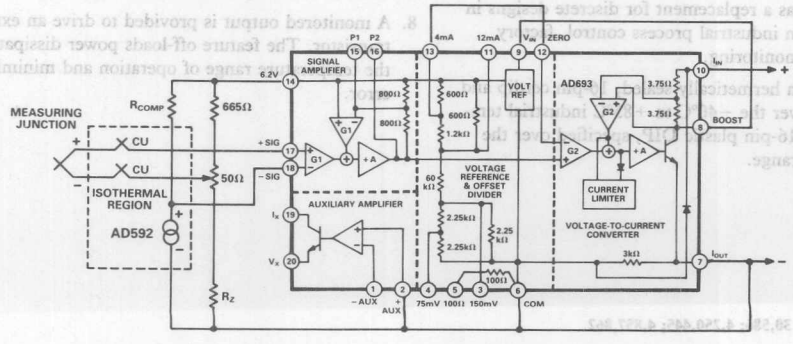


Figure 11. Thermocouple Inputs with Cold Junction Compensation.

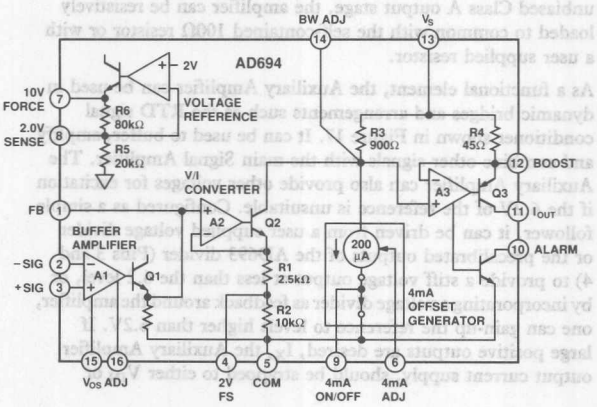
4–20 mA Transmitter

AD694*

FEATURES

4–20 mA, 0–20 mA Output Ranges
Precalibrated Input Ranges:
0 V to 2 V, 0 V to 10 V
Precision Voltage Reference
Programmable to 2.000 V or 10.000 V
Single or Dual Supply Operation
Wide Power Supply Range: +4.5 V to +36 V
Wide Output Compliance
Input Buffer Amplifier
Open-Loop Alarm
Optional External Pass Transistor to Reduce Self-Heating Errors
0.002% typ Nonlinearity

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD694 is a monolithic current transmitter that accepts high level signal inputs to drive a standard 4–20 mA current loop for the control of valves, actuators, and other devices commonly used in process control. The input signal is buffered by an input amplifier that can be used to scale the input signal or buffer the output from a current mode DAC. Precalibrated input spans of 0 V to 2 V and 0 V to 10 V are selected by simple pin strapping; other spans may be programmed with external resistor.

The output stage compliance extends to within 2 V of V_S and its special design allows the output voltage to extend below common in dual supply operation. An alarm warns of an open 4 to 20 mA loop or noncompliance of the output stage.

Active laser trimming of the AD694's thin film resistors results in high levels of accuracy without the need for additional adjustments and calibration. An external pass transistor may be used with the AD694 to off-load power dissipation, extending the temperature range of operation.

The AD694 is the ideal building block for systems requiring noise immune 4–20 mA signal transmission to operate valves, actuators, and other control devices, as well as for the transmission of process parameters such as pressure, temperature, or flow. It is recommended as a replacement for discrete designs in a variety of applications in industrial process control, factory automation, and system monitoring.

The AD694 is available in hermetically sealed, 16-pin cerdip and plastic SOIC, specified over the −40°C to +85°C industrial temperature range, and in a 16-pin plastic DIP, specified over the 0 to +70°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD694 is a complete voltage in to 4–20 mA out current transmitter.
2. Pin programmable input ranges are pre-calibrated at 0 V to 2 V and 0 V to 10 V.
3. The input amplifier may be configured to buffer and scale the input voltage, or to serve as an output amplifier for current output DACs.
4. The output voltage compliance extends to within 2 V of the positive supply and below common. When operated with a 5 V supply, the output voltage compliance extends 30 V below common.
5. The AD694 interfaces directly to 8-, 10-, and 12-bit single supply CMOS and bipolar DACs.
6. The 4 mA zero current may be switched on and off with a TTL control pin, allowing 0–20 mA operation.
7. An open collector alarm warns of loop failure due to open wires or noncompliance of the output stage.
8. A monitored output is provided to drive an external pass transistor. The feature off-loads power dissipation to extend the temperature range of operation and minimize self-heating error.

*Protected by U.S. Patents: 30,586; 4,250,445; 4,857,862.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C, R_L = 250 Ω and V_S = +24 V, unless otherwise noted)

Model	AD694JN/AQ/AR			AD694BQ/BR			Units
	Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS							
Input Voltage Range	−0.2	V_S−2.0V	V_S−2.5 V	−0.2	V_S−2.0 V	V_S−2.5 V	V
Input Bias Current							
Either Input, T_{min} to T_{max}		1.5	5		1.5	5	nA
Offset Current, T_{min} to T_{max}		±0.1	±1		±0.1	±1	nA
Offset Current Drift		±1.0	±5.0		±1.0	±5.0	pA/°C
Input Impedance	5			5			MΩ
OUTPUT CHARACTERISTICS							
Operating Current Range	0		23	0		23	mA
Specified Performance	4		20	4		20	mA
Output Voltage Compliance	V_S−36 V		V_S−2 V	V_S−36 V		V_S−2 V	V
Output Impedance, 4–20 mA	40.0	50.0		40.0	50.0		MΩ
Current Limit @ 2× FS Overdrive	24		44	24		44	mA
Slew Rate		1.3			1.3		mA/μs
SPAN AND ZERO ACCURACY[1]							
4 mA Offset Error @ 0 V Input[2]							
Error from 4.000 mA, 4 mA On		±10	±20		±5	±10	μA
Error from 0.000 mA, 4 mA Off	0	+10	+20	0	+5	+10	μA
T_{min} to T_{max}		±10	±40		±5	±20	μA
vs. Supply (2 V Span/10 V Span)		0.3/0.05	0.8/0.4		0.3/0.05	0.8/0.4	μA/V
Trim Range, 4 mA Zero	2.0		4.8	2.0		4.8	mA
Span							
Nominal Transfer Function							
Input FS = 2 V		8.0			8.0		mA/V
Input FS = 10 V		1.6			1.6		mA/V
Transfer Function Error from Nom,							
Input FS = 2 V, 10 V		±0.1	±0.3		±0.05	±0.15	% of Span
T_{min} to T_{max}		±0.002	±0.005		±0.001	±0.0025	% of Span/°C
vs. Supply		±0.001	±0.005		±0.001	±0.005	% of Span/V
Nonlinearity[3]		±0.005	±0.015		±0.001	±0.005	% of Span
4 mA On: Max Pin 9 Voltage			0.8			0.8	V
4 mA Off: Min Pin 9 Voltage	3.0	2.5		3.0	2.5		V
VOLTAGE REFERENCE							
Output Voltage: 10 V Reference	9.960	10.000	10.040	9.980	10.000	10.020	V
Output Voltage: 2 V Reference	1.992	2.000	2.008	1.996	2.000	2.004	V
T_{min} to T_{max}[4]		30	50		20	30	ppm/°C
vs. Load, V_{REF} = 2 V, 10 V		0.15	0.50		0.15	0.50	mV/mA
vs. Supply, V_{REF} = 2 V, 10 V		±0.001	±0.005		±0.001	±0.005	%/V
Output Current							
Source	5			5			mA
Sink		0.2			0.2		mA
ALARM CHARACTERISTICS							
$V_{CE(SAT)}$ @ 2.5 mA		0.35			0.35		V
Leakage Current			±1			±1	μA
Alarm Pin Current (Pin 10)		20			20		mA
POWER REQUIREMENTS							
Specified Performance		24			24		V
Operating Range							
2 V FS, V_{REF} = 2 V	4.5		36	4.5		36	V
2 V, 10 V FS, V_{REF} = 2 V, 10 V	12.5		36	12.5		36	V
Quiescent Current, 4 mA Off		1.5	2.0		1.5	2.0	mA
TEMPERATURE RANGE							
Specified Performance[5] AD694AQ/BQ/AR/BR	−40		+85	−40		+85	°C
AD694JN	0		+70	0		+70	°C
Operating AD694AQ/BQ/AR/BR	−55		+125	−55		+125	°C
AD694JN	−40		+85	−40		+85	°C

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BUFFER AMPLIFIER[6]							
Input Offset Voltage							
Initial Offset		±150	±500		±50	±500	μV
T_{min} to T_{max}		±2	±3		±2	±3	μV/°C
vs. Supply	80	90		80	90		dB
vs. Common Mode	80	90		80	90		dB
Trim Range	±2.5	±4.0		±2.5	±4.0		mV
Frequency Response							
Unity Gain, Small Signal		300			300		kHz
Input Voltage Noise (0.1 to 10 Hz)		2			2		μV p–p
Open-Loop Gain							
V_O = +10 V, $R_L \geq 10$ kΩ		50			50		V/mV
Output Voltage @ Pin 1, FB[1]							
Minimum Output Voltage		1.0	10		1.0	10	mV
Maximum Output Voltage	V_S–2.5 V	V_S–2 V		V_S–2.5 V	V_S–2 V		V

NOTES

[1]The single supply op amps of the AD694, lacking pull down current, may not reach 0.000 V at their outputs. For this reason, span, offset, and nonlinearity are specified with the input amplifiers operating in their linear range. The input voltage used for the tests is 5 mV to 2 V and 5 mV to 10 V for the two pre-calibrated input ranges. Span and zero accuracy are tested with the buffer amplifier configured as a follower.

[2]Offset at 4 mA out and 0 mA out are extrapolated to 0.000 V input from measurements made at 5 mV and at full scale. See Note 1.

[3]Nonlinearity is specified as the maximum deviation of the output, as a % of span, from a straight line drawn through the endpoints of the transfer function.

[4]Voltage reference drift guaranteed by the Box Method. The voltage reference output over temperature will fall inside of a box whose length is determined by the temperature range and whose height is determined by the maximum temperature coefficient multiplied by the temperature span in degrees C.

[5]Devices tested at these temperatures with a pass transistor. Allowable temperature range of operation is dependent upon internal power dissipation. Absolute maximum junction and case temperature should not be exceeded. See section: "Power Dissipation Considerations."

[6]Buffer amplifier specs for reference. Buffer amplifier offset and drift already included in Span and Zero accuracy specs above.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +36 V
V_S to I_{OUT} . . . . . +36 V
Input Voltage, (Either Input Pin 2 or 3) . . . . −0.3 V to +36 V
Reference Short Circuit to Common . . . . . Indefinite
Alarm Voltage, Pin 10 . . . . . +36 V
4 mA Adj, Pin 6 . . . . . +1 V
4 mA On/Off, Pin 9 . . . . . 0 V to 36 V
Storage Temperature Range
AD694Q . . . . . −65°C to +150°C
AD694N, R . . . . . −65°C to +125°C
Lead Temperature, 10 sec Soldering . . . . . +300°C
Maximum Junction Temperature . . . . . +150°C
Maximum Case Temperature
Plastic Package (N, R) . . . . . +125°C
Cerdip Package (Q) . . . . . +125°C

Transistor Count: . . . . . 75 Active Devices
Substrate Connection: . . . . . to Com, Pin 5

Thermal Characteristics:

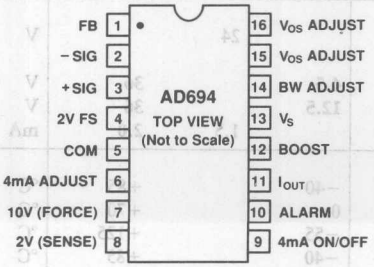
Plastic (N) Package: θ_{JC} = 50°C/Watt
θ_{CA} (Still Air) = 85°C/Watt
Cerdip (Q) Package: θ_{JC} = 30°C/Watt
θ_{CA} (Still Air) = 70°C/Watt
Plastic (R) Package: θ_{JC} = 27°C/Watt
θ_{CA} (Still Air) = 73°C/Watt

ESD Susceptibility

All pins are rated for a minimum of 4000 V protection, except for Pins 2, 3 and 9 which are rated to survive a minimum of 1500 V. ESD testing conforms to Human Body Model. Always practice ESD prevention.

No pin, other than I_{OUT} (11) and ±Sig (2), (3) as noted, may be permitted to become more negative than Com (5). No pin may be permitted to become more positive than V_S (13).

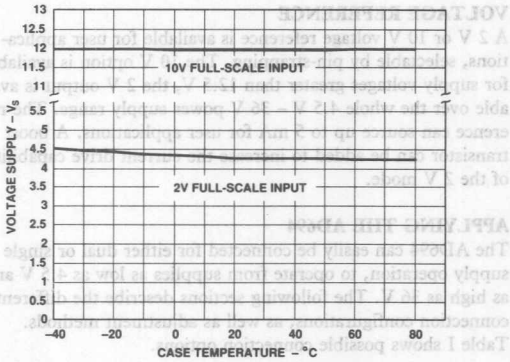
PIN CONFIGURATION (N, R, Q Package)



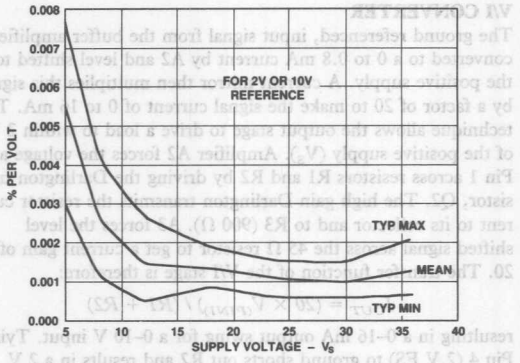
ORDERING GUIDE

Model	Temperature Range	Package Options*
AD694JN	0°C to +70°C	N-16
AD694AQ	−40°C to +85°C	Q-16
AD694AR	−40°C to +85°C	R-16
AD694BQ	−40°C to +85°C	Q-16
AD694BR	−40°C to +85°C	R-16

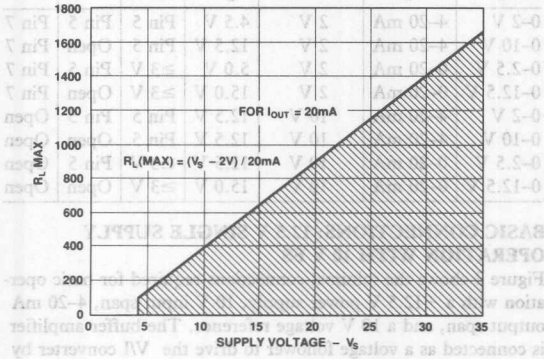
*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.



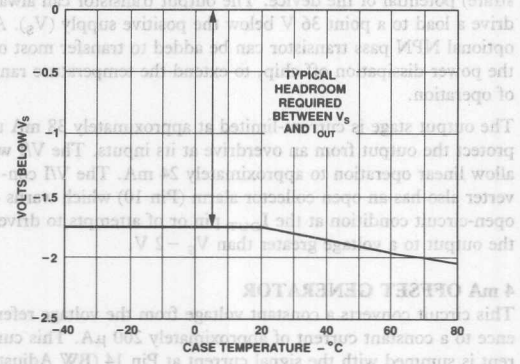
Typical Minimum Supply Voltage vs. Temperature for 2 V & 10 V Full Scale



Voltage Reference Power Supply Rejection



Maximum R_L vs. Supply Voltage



I_{OUT}: Voltage Compliance vs. Temperature

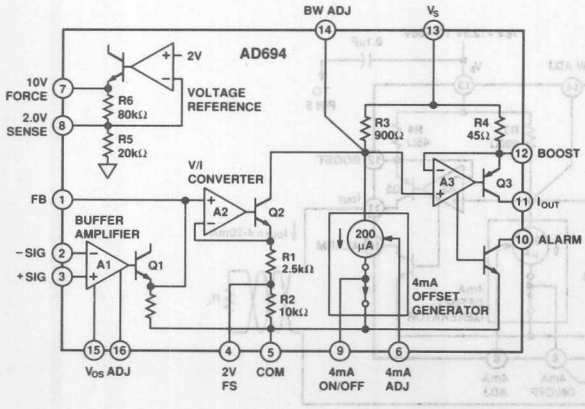


Figure 1. Functional Block Diagram

FUNCTIONAL DESCRIPTION

The operation of the AD694 can best be understood by dividing the circuit into three functional parts (see Figure 1). First, a single supply input amplifier buffers the high level, single-ended input signal. The buffer amplifier drives the second section, a voltage to current (V/I) converter, that makes a 0 to 16 mA signal dependent current.

The third section, a voltage reference and offset generator, is responsible for providing the 4 mA offset current signal.

BUFFER AMPLIFIER

The buffer amplifier is a single supply amplifier that may be used as a unity gain buffer, an output amplifier for a current output D/A converter, or as a gain block to amplify low level signals. The amplifier's PNP input stage has a common-mode range that extends from a few hundred mV below ground to within 2.5 V of V_S. The Class A output of the amplifier appears at Pin 1 (FB). The output range extends from about 1 mV above common to within 2.5 V of V_S when the amplifier is operated as a follower. The amplifier can source a maximum load of 5 kΩ, but can sink only as much as its internal 10 kΩ pull-down resistor allows.

V/I CONVERTER

The ground referenced, input signal from the buffer amplifier is converted to a 0 to 0.8 mA current by A2 and level shifted to the positive supply. A current mirror then multiplies this signal by a factor of 20 to make the signal current of 0 to 16 mA. This technique allows the output stage to drive a load to within 2 V of the positive supply (V_S). Amplifier A2 forces the voltage at Pin 1 across resistors R1 and R2 by driving the Darlington transistor, Q2. The high gain Darlington transmits the resistor current to its collector and to R3 (900 Ω). A3 forces the level shifted signal across the 45 Ω resistor to get a current gain of 20. The transfer function of the V/I stage is therefore:

$$I_{OUT} = (20 \times V_{(PIN1)}) / (R1 + R2)$$

resulting in a 0–16 mA output swing for a 0–10 V input. Tying Pin 4 (2 V FS) to ground shorts out R2 and results in a 2 V full-scale input for a 16 mA output span.

The output stage of the V/I converter is of a unique design that allows the I_{OUT} pin to drive a load below the common (substrate) potential of the device. The output transistor can always drive a load to a point 36 V below the positive supply (V_S). An optional NPN pass transistor can be added to transfer most of the power dissipation off-chip, to extend the temperature range of operation.

The output stage is current-limited at approximately 38 mA to protect the output from an overdrive at its inputs. The V/I will allow linear operation to approximately 24 mA. The V/I converter also has an open collector alarm (Pin 10) which warns of open-circuit condition at the I_{OUT} pin or of attempts to drive the output to a voltage greater than V_S −2 V.

4 mA OFFSET GENERATOR

This circuit converts a constant voltage from the voltage reference to a constant current of approximately 200 μA. This current is summed with the signal current at Pin 14 (BW Adjust), to result in a constant 4 mA offset current at I_{OUT}. The 4 mA Adj (Pin 6) allows the offset current to be adjusted to any current in the range of 2 mA to 4.8 mA. Pin 9 (4 mA On/Off) can shut off the offset current completely if it is lifted to 3.0 V or more, allowing 0 to 20 mA operation of the AD694. In normal 4–20 mA operation, Pin 9 is connected to ground.

VOLTAGE REFERENCE

A 2 V or 10 V voltage reference is available for user applications, selectable by pin-strapping. The 10 V option is available for supply voltages greater than 12.5 V, the 2 V output is available over the whole 4.5 V – 36 V power supply range. The reference can source up to 5 mA for user applications. A boost transistor can be added to increase the current drive capability of the 2 V mode.

APPLYING THE AD694

The AD694 can easily be connected for either dual or single supply operation, to operate from supplies as low as 4.5 V and as high as 36 V. The following sections describe the different connection configurations, as well as adjustment methods. Table I shows possible connection options.

Table I. Precalibrated Ranges for the AD694

Input Range	Output Range	Voltage Reference	Min V_S	Pin 9	Pin 4	Pin 8
0–2 V	4–20 mA	2 V	4.5 V	Pin 5	Pin 5	Pin 7
0–10 V	4–20 mA	2 V	12.5 V	Pin 5	Open	Pin 7
0–2.5 V	0–20 mA	2 V	5.0 V	≥3 V	Pin 5	Pin 7
0–12.5 V	0–20 mA	2 V	15.0 V	≥3 V	Open	Pin 7
0–2 V	4–20 mA	10 V	12.5 V	Pin 5	Pin 5	Open
0–10 V	4–20 mA	10 V	12.5 V	Pin 5	Open	Open
0–2.5 V	0–20 mA	10 V	12.5 V	≥3 V	Pin 5	Open
0–12.5 V	0–20 mA	10 V	15.0 V	≥3 V	Open	Open

BASIC CONNECTIONS: 12.5 V SINGLE SUPPLY OPERATION WITH 10 V FS

Figure 2 shows the minimal connections required for basic operation with a +12.5 V power supply, 10 V input span, 4–20 mA output span, and a 10 V voltage reference. The buffer amplifier is connected as a voltage follower to drive the V/I converter by connecting FB (Pin 1) to −Sig (Pin 2). 4 mA On/Off (Pin 9) is tied to ground (Pin 5) to enable the 4 mA offset current. The AD694 can drive a maximum load $R_L = [V_S - 2\ V] / 20\ mA$, thus the maximum load with a 12.5 V supply is 525 Ω.

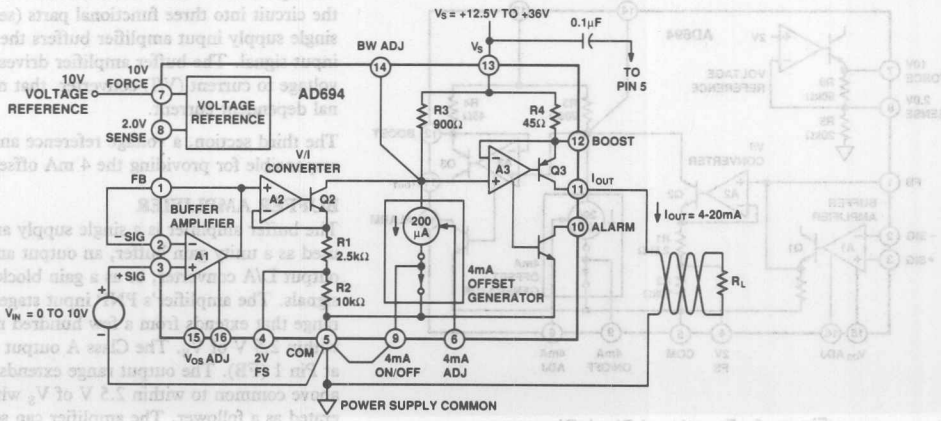


Figure 2. Minimal Connections for 0–10 V Single-Ended Input, 4–20 mA Output, 10 V Reference Output

SELECTING A 2 V FULL-SCALE INPUT

The 2 V full-scale option is selected by shorting Pin 4 (2 V FS) to Pin 5 (Common). The connection should be as short as possible; any parasitic resistance will affect the precalibrated span accuracy.

SELECTING THE 2 V VOLTAGE REFERENCE

The voltage reference is set to a 2 V output by shorting Pin 7 to Pin 8 (10 V Force to 2 V Sense). If desired, the 2 V reference can be set up for remote force and sense connection. Keep in mind that the 2 V Sense line carries a constant current of 100 μA that could cause an offset error over long wire runs. The 2 V reference option can be used with all supply voltages greater than 4.5 V.

An NPN boost transistor can be added in the 2 V mode to increase the current drive capability of the 2 V reference. The 10 V force pin is connected to the base of the NPN, and the NPN emitter is connected to the 2 V sense pin. The minimum V_S of the part increases by approximately 0.7 V.

4.5 V SINGLE SUPPLY OPERATION

For operation with a +4.5 V power supply, the input span and the voltage reference output must be reduced to give the amplifiers their required 2.5 V of head room for operation. This is done by adjusting the AD694 for 2 V full-scale input, and a voltage reference output of 2 V as described above.

GENERAL DESIGN GUIDELINES

A 0.1 μF decoupling capacitor is recommended in all applications from V_S (Pin 13) to Com (Pin 5). Additional components may be required if the output load is nonresistive, see section on driving nonresistive loads. The buffer amplifier PNP inputs should not be brought more than −0.3 V of common, or they will begin to source large amounts of current. Input protection resistors must be added to the inputs if there is a danger of this occurring. The output of the buffer amplifier, Pin 1 (FB), is not short circuit protected. Shorting this pin to ground or V_S with a signal present on the amplifier may damage it. Input signals should not drive Pin 1 (FB) directly; always use the buffer amplifier to buffer input signals.

DRIVING NONRESISTIVE LOADS

The AD694 is designed to be stable when driving resistive loads. Adding a 0.01 μF capacitor from I_{OUT} (Pin 11) to Com (Pin 5), as shown in Figure 3, insures the stability of the AD694 when driving inductive or poorly defined loads. This capacitor is recommended when there is any uncertainty as to the characteristics of the load.

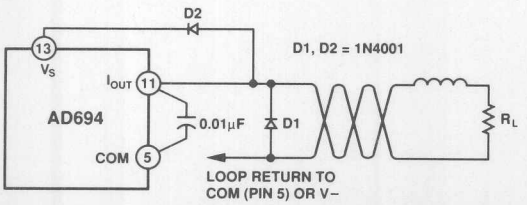


Figure 3. Capacitor Utilized When Driving Nonresistive Loads; Protection Diodes Used When Driving Inductive Loads

Additional protection is recommended when driving inductive loads. Figure 3 shows two protective diodes, D1 and D2, added to protect against voltage spikes that may extend above V_S or below common that could damage the AD694. These diodes should be used in addition to the 0.01 μF capacitor. When the optional NPN transistor is used, the capacitor and diodes should connect to the NPN emitter instead of Pin 11.

0–20 mA OPERATION

A 0–20 mA output range is available with the AD694 by removing the 4 mA offset current with the 4 mA On/Off pin. In normal 4–20 mA operation 4 mA On/Off (Pin 9) is tied to ground, enabling the 4 mA offset current. Tying Pin 9 to a potential of 3 V or greater turns off the 4 mA offset current; connecting Pin 9 to the 10 V reference, the positive supply, or a TTL control pin, is a convenient way to do this. In 0–20 mA mode the input span is increased by 20%, thus the precalibrated input spans of 2 V and 10 V become 2.5 V and 12.5 V. Minimum supply voltages for the two spans increase to 5 V and 15 V.

The 4 mA On/Off pin may also be used as a "jiggle pin" to unstick valves or actuators, or as a way to shut off a 4–20 mA loop entirely. Note that the pin only removes the 4 mA offset and not the signal current.

DUAL SUPPLY OPERATION

Figure 4 shows the AD694 operated in dual supply mode. (Note that the pass transistor is shown for illustration and is not required for dual supply operation.) The device is powered completely by the positive supply which may be as low as 4.5 V. The unique design of the output stage allows the I_{OUT} pin to extend below common to a negative supply. The output stage can source a current to a point 36 V below the positive supply. For example, when operated with a +12.5 V supply, the AD694 can source a current to a point as low as 23.5 V below common. This feature can simplify the interface to dual supply D/A converters by eliminating grounding and level-shifting problems while increasing the load that the transmitter is able to drive. Note that the I_{OUT} pin is the only pin that should be allowed to extend lower than −0.3 V of common.

OPERATION WITH A PASS TRANSISTOR

The AD694 can operate as a stand-alone 4–20 mA converter with no additional active components. However, provisions have been made to connect I_{OUT} to the base of an external NPN pass transistor as shown in Figure 4. This permits a majority of the power dissipation to be moved off-chip to enhance performance and extend the temperature range of operation. Note that the positive output voltage compliance is reduced by approximately 0.7 V, the V_{BE} of the pass device. A 50 Ω resistor should be added in series with the pass transistor collector, when the AD694 is operated with dual supplies, as shown in Figure 4. This will not reduce the voltage compliance of the output stage.

The external pass transistor selected should have a BV_{CEO} greater than the intended supply voltage with a sufficient power rating for continuous operation with 25 mA current at the supply voltage. Ft should be in the 10 MHz to 100 MHz range and β should be greater than 10 at a 20 mA emitter current. Heat sinking the external pass transistor is suggested.

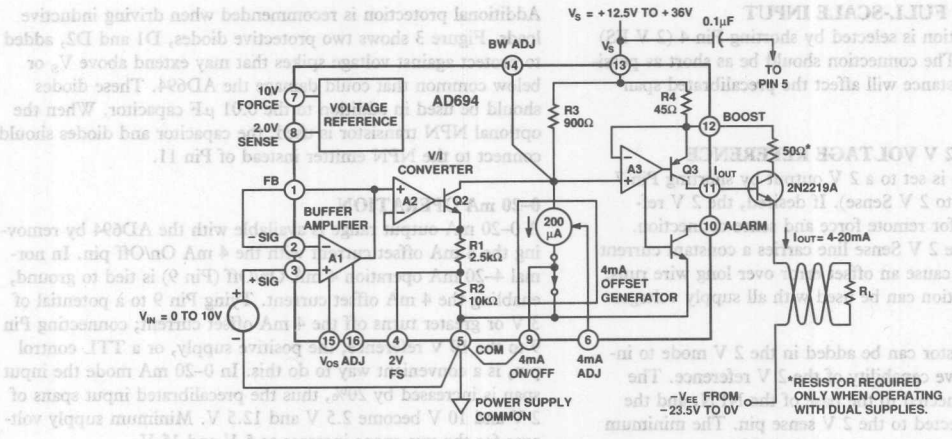


Figure 4. Using Optional Pass Transistor to Minimize Self-Heating Errors; Dual Supply Operation Shown

APPLICATION EXAMPLE

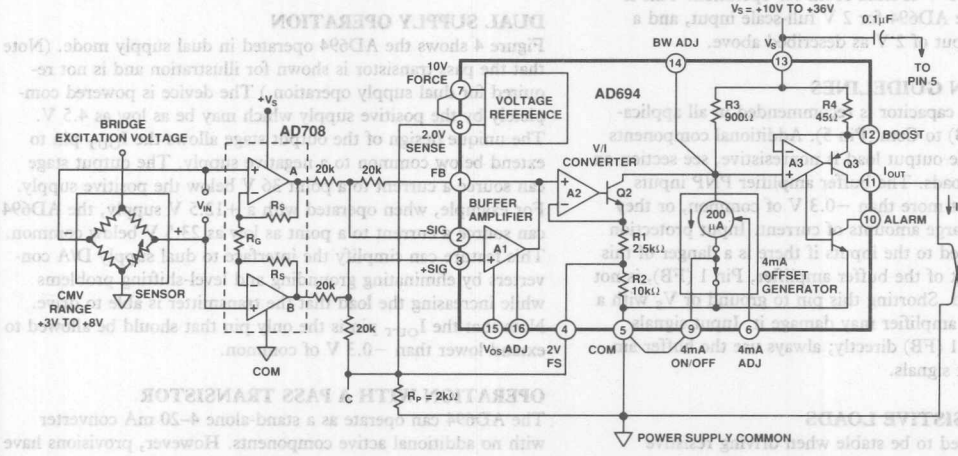


Figure 5. Low Cost Sensor Transmitter

Voltage Output Temperature Sensor with Signal Conditioning

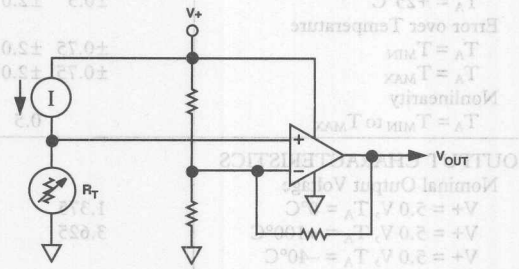
AD22100*

FEATURES
200°C Temperature Span
Accuracy Better than ±2% of Full Scale
Linearity Better than ±1% of Full Scale
Temperature Coefficient of 22.5 mV/°C
Output Proportional to Temperature × V+
Single Supply Operation
Reverse Voltage Protection
Minimal Self Heating
High Level, Low Impedance Output

APPLICATIONS
HVAC Systems
System Temperature Compensation
Board Level Temperature Sensing
Electronic Thermostats

MARKETS
Industrial Process Control
Instrumentation
Automotive

SIMPLIFIED BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD22100 is a monolithic temperature sensor with on-chip signal conditioning. It can be operated over the temperature range –50°C to +150°C, making it ideal for use in numerous HVAC, instrumentation and automotive applications.

The signal conditioning eliminates the need for any trimming, buffering or linearization circuitry, greatly simplifying the system design and reducing the overall system cost.

The output voltage is proportional to the temperature times the supply voltage (ratiometric). The output swings from 0.25 V at –50°C to +4.75 V at +150°C using a single +5.0 V supply.

Due to its ratiometric nature, the AD22100 offers a cost effective solution when interfacing to an analog-to-digital converter. This is accomplished by using the ADC's +5 V power supply as a reference to both the ADC and the AD22100 (See Figure 1), eliminating the need for and cost of a precision reference.

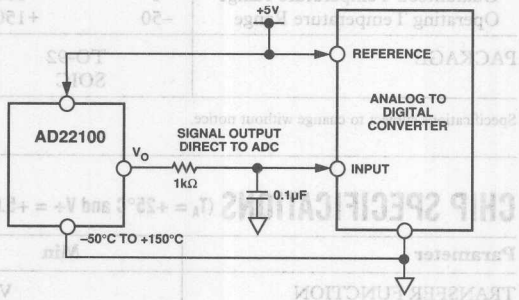


Figure 1. Application Circuit

*Protected by U.S. Patent Nos. 5030849 and 5243319.

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AD22100 SPECIFICATIONS

TEMPERATURE COEFFICIENT	(V+/5 V) × 22.5									mV/°C
TOTAL ERROR										
Initial Error										
T_A = +25°C		±0.5	±2.0		±1.0	±2.0		±1.0	±2.0	°C
Error over Temperature										
$T_A = T_{MIN}$		±0.75	±2.0		±2.0	±3.7		±3.0	±4.0	°C
$T_A = T_{MAX}$		±0.75	±2.0		±2.0	±3.0		±3.0	±4.0	°C
Nonlinearity										
$T_A = T_{MIN}$ to T_{MAX}			0.5			0.5			1.0	% FS[1]
OUTPUT CHARACTERISTICS										
Nominal Output Voltage										
V+ = 5.0 V, T_A = 0°C		1.375								V
V+ = 5.0 V, T_A = +100°C		3.625								V
V+ = 5.0 V, T_A = –40°C					0.475					V
V+ = 5.0 V, T_A = +85°C					3.288					V
V+ = 5.0 V, T_A = –50°C								0.250		V
V+ = 5.0 V, T_A = +150°C								4.750		V
POWER SUPPLY										
Operating Voltage	+4.0	+5.0	+6.0	+4.0	+5.0	+6.0	+4.0	+5.0	+6.0	V
Quiescent Current		500	650		500	650		500	650	µA
TEMPERATURE RANGE										
Guaranteed Temperature Range	0		+100	–40		+85	–50		+150	°C
Operating Temperature Range	–50		+150	–50		+150	–50		+150	°C
PACKAGE		TO-92			TO-92			TO-92		
		SOIC			SOIC			SOIC		

Specifications subject to change without notice.

CHIP SPECIFICATIONS (T_A = +25°C and V+ = +5.0 V unless otherwise noted)

Parameter	Min	Typ	Max	Units
TRANSFER FUNCTION		$V_{OUT} = (V+/5\ V) \times [1.375 + 22.5\ mV/°C \times T_A]$		V
TEMPERATURE COEFFICIENT		(V+/5 V) × 22.5		mV/°C
OUTPUT CHARACTERISTICS				
Error				
T_A = +25°C		±0.5	±2.0	°C
Nominal Output Voltage				
T_A = +25°C		1.938		V
POWER SUPPLY				
Operating Voltage	+4.0	+5.0	+6.0	V
Quiescent Current		500	650	µA
TEMPERATURE RANGE				
Guaranteed Temperature Range		25°C		°C
Operating Temperature Range	–50		+150	°C

NOTES

[1]FS (Full Scale) is defined as that of the operating temperature range, –50°C to +150°C. The listed max specification limit applies to the guaranteed temperature range. For example, the AD22100K has a nonlinearity of (0.5%) × (200°C) = 1°C over the guaranteed temperature range of 0°C to +100°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	+10 V
Reversed Continuous Supply Voltage	–10 V
Operating Temperature	–50°C to +150°C
Storage Temperature	–65°C to +160°C
Output Short Circuit to V+ or Ground	Indefinite
Lead Temperature (Soldering, 10 sec)	+300°C

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model/Grade	Guaranteed Temperature Range	Package Description[1]	Package Option[2]
AD22100 KT	0°C to 100°C	TO-92	TO-92
AD22100 KR	0°C to 100°C	SOIC	SO-8
AD22100 AT	–40°C to +85°C	TO-92	TO-92
AD22100 AR	–40°C to +85°C	SOIC	SO-8
AD22100 ST	–50°C to +150°C	TO-92	TO-92
AD22100 SR	–50°C to +150°C	SOIC	SO-8
AD22100KChips	+25°C	N/A	N/A

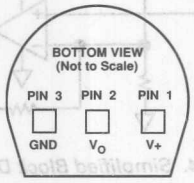
NOTES
[1]Minimum purchase quantities of 100 pieces for all chip orders.
[2]For outline information see Package Information section.

PIN DESCRIPTION

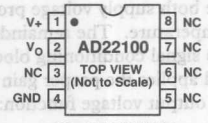
Mnemonic	Function
V+	Power Supply Input
V_O	Device Output
GND	Ground Pin must be connected to 0 V.
NC	No Connect

PIN CONFIGURATIONS

TO-92



SOIC



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD22100 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Performance Curves

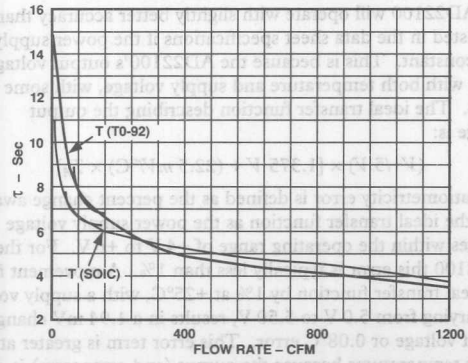


Figure 2. Thermal Response vs. Flow Rate

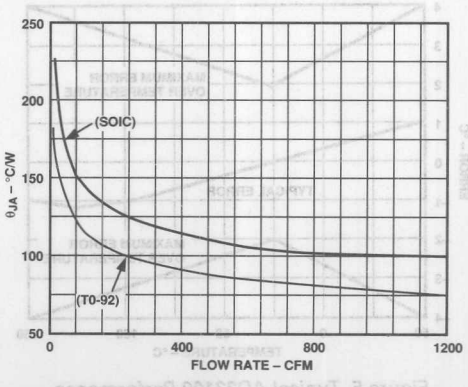


Figure 3. Thermal Resistance vs. Flow Rate

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THEORY OF OPERATION

The AD22100 is a ratiometric temperature sensor IC whose output voltage is proportional to power supply voltage. The heart of the sensor is a proprietary temperature-dependent resistor, similar to an RTD, which is built into the IC. Figure 4 shows a simplified block diagram of the AD22100.

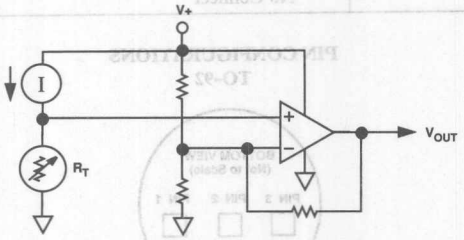


Figure 4. Simplified Block Diagram

The temperature-dependent resistor, labeled R_T, exhibits a change in resistance that is nearly linearly proportional to temperature. This resistor is excited with a current source that is proportional to power supply voltage. The resulting voltage across R_T is therefore both supply voltage proportional and linearly varying with temperature. The remainder of the AD22100 consists of an op amp signal conditioning block that takes the voltage across R_T and applies the proper gain and offset to achieve the following output voltage function:

$$V_{OUT} = (V+/5\ V) \times [1.375\ V + (22.5\ mV/°C) \times T_A]$$

ABSOLUTE ACCURACY AND NONLINEARITY SPECIFICATIONS

Figure 5 graphically depicts the guaranteed limits of accuracy for the AD22100 and shows the performance of a typical part. As the output is very linear, the major sources of error are offset, i.e., error at room temperature, and span error, i.e., deviation from the theoretical 22.5 mV/°C. Demanding applications can achieve improved performance by calibrating these offset and gain errors so that only the residual nonlinearity remains as a significant source of error.

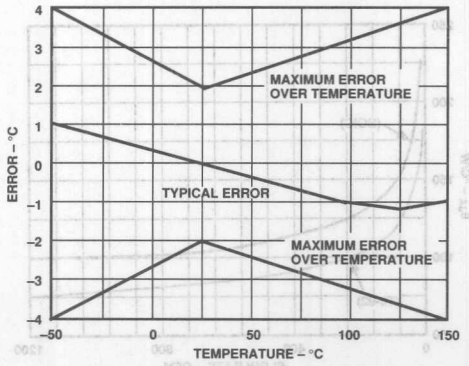


Figure 5. Typical AD22100 Performance

OUTPUT STAGE CONSIDERATIONS

As previously stated, the AD22100 is a voltage output device. A basic understanding of the nature of its output stage is useful for proper application. Note that at the nominal supply voltage of 5.0 V, the output voltage extends from 0.25 V at –50°C to +4.75 V at +150°C. Furthermore, the AD22100 output pin is capable of withstanding an indefinite short circuit to either ground or the power supply. These characteristics are provided by the output stage structure shown in Figure 6.

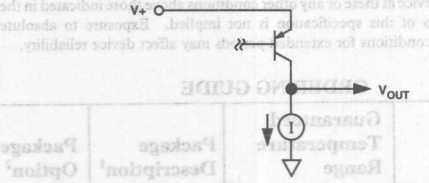


Figure 6. Output Stage Structure

The active portion of the output stage is a PNP transistor with its emitter connected to the V+ supply and collector connected to the output node. This PNP transistor sources the required amount of output current. A limited pull-down capability is provided by a fixed current sink of about –80 µA. (Here, "fixed" means the current sink is fairly insensitive to either supply voltage or output loading conditions. The current sink capability is a function of temperature, increasing its pull-down capability at lower temperatures.)

Due to its limited current sinking ability, the AD22100 is incapable of driving loads to the V+ power supply and is instead intended to drive grounded loads. A typical value for short circuit current limit is 7 mA, so devices can reliably source 1 mA or 2 mA. However, for best output voltage accuracy and minimal internal self-heating, output current should be kept below 1 mA. Loads connected to the V+ power supply should be avoided as the current sinking capability of the AD22100 is fairly limited. These considerations are typically not a problem when driving a microcontroller analog to digital converter input pin (see MICROPROCESSOR A/D INTERFACE ISSUES).

RATIOMETRICITY CONSIDERATIONS

The AD22100 will operate with slightly better accuracy than that listed in the data sheet specifications if the power supply is held constant. This is because the AD22100's output voltage varies with both temperature and supply voltage, with some errors. The ideal transfer function describing the output voltage is:

$$(V+/5\ V) \times [1.375\ V + (22.5\ mV/°C) \times T_A]$$

The ratiometricity error is defined as the percent change away from the ideal transfer function as the power supply voltage changes within the operating range of +4 V to +6 V. For the AD22100 this error is typically less than 1%. A movement from the ideal transfer function by 1% at +25°C, with a supply voltage varying from 5.0 V to 5.50 V, results in a 1.94 mV change in output voltage or 0.08°C error. This error term is greater at higher temperatures because the output (and error term) is directly proportional to temperature. At 150°C, the error in output voltage is 4.75 mV or 0.19°C.

For example, with V_S = 5.0 V, and T_A = +25°C, the nominal output of the AD22100 will be 1.9375 V. At V_S = 5.50 V, the nominal output will be 2.1313 V, an increase of 193.75 mV. A proportionality error of 1% is applied to the 193.75 mV, yielding an error term of 1.9375 mV. This error term translates to a variation in output voltage of 2.1293 V to 2.3332 V. A 1.94 mV error at the output is equivalent to about 0.08°C error in accuracy.

If we substitute 150°C for 25°C in the above example, then the error term translates to a variation in output voltage of 5.2203 V to 5.2298 V. A 4.75 mV error at the output is equivalent to about 0.19°C error in accuracy.

MOUNTING CONSIDERATIONS

If the AD22100 is thermally attached and properly protected, it can be used in any measuring situation where the maximum range of temperatures encountered is between –50°C and +150°C. Because plastic IC packaging technology is employed, excessive mechanical stress must be avoided when fastening the device with a clamp or screw-on heat tab. Thermally conductive epoxy or glue is recommended for typical mounting conditions. In wet or corrosive environments, an electrically isolated metal or ceramic well should be used to shield the AD22100. Because the part has a voltage output (as opposed to current), it offers modest immunity to leakage errors, such as those caused by condensation at low temperatures.

THERMAL ENVIRONMENT EFFECTS

The thermal environment in which the AD22100 is used determines two performance traits: the effect of self-heating on accuracy and the response time of the sensor to rapid changes in temperature. In the first case, a rise in the IC junction temperature above the ambient temperature is a function of two variables; the power consumption of the AD22100 and the thermal resistance between the chip and the ambient environment θ_{JA}. Self-heating error in °C can be derived by multiplying the power dissipation by θ_{JA}. Because errors of this type can vary widely for surroundings with different heat sinking capacities, it is necessary to specify θ_{JA} under several conditions. Table I shows how the magnitude of self-heating error varies relative to the environment. A typical part will dissipate about 2.2 mW at room temperature with a 5 V supply and negligible output loading. In still air, without a "heat sink," the table below indicates a θ_{JA} of 190°C/W, yielding a temperature rise of 0.4°C. Thermal rise will be considerably less in either moving air or with direct physical connection to a solid (or liquid) body.

Table I. Thermal Resistance (TO-92)

Medium	θ_{JA} (°C/Watt)	τ (sec) *
Aluminum Block	60	2
Moving Air**		
Without Heat Sink	75	3.5
Still Air		
Without Heat Sink	190	15

*The time constant τ is defined as the time to reach 63.2% of the final temperature change.
**1200 CFM.

Response of the AD22100 output to abrupt changes in ambient temperature can be modeled by a single time constant τ exponential function. Figure 7 shows typical response time plots for a few media of interest.

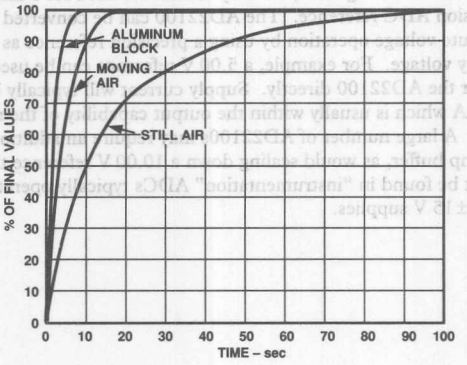


Figure 7. Response Time

The time constant τ is dependent on θ_{JA} and the thermal capacities of the chip and the package. Table I lists the effective τ (time to reach 63.2% of the final value) for a few different media. Copper printed circuit board connections were neglected in the analysis; however, they will sink or conduct heat directly through the AD22100's solder plated copper leads. When faster response is required, a thermally conductive grease or glue between the AD22100 and the surface temperature being measured should be used.

MICROPROCESSOR A/D INTERFACE ISSUES

The AD22100 is especially well suited to providing a low cost temperature measurement capability for microprocessor/microcontroller based systems. Many inexpensive 8-bit microprocessors now offer an onboard 8-bit ADC capability at a modest cost premium. Total "cost of ownership" then becomes a function of the voltage reference and analog signal conditioning necessary to mate the analog sensor with the microprocessor ADC. The AD22100 can provide an ideal low cost system by eliminating the need for a precision voltage reference and any additional active components. The ratiometric nature of the AD22100 allows the microprocessor to use the same power supply as its ADC reference. Variations of hundreds of millivolts in the supply voltage have little effect as both the AD22100 and the ADC use the supply as their reference. The nominal AD22100 signal range of 0.25 V to 4.75 V (–50°C to +150°C) makes good use of the input range of a 0 V to 5 V ADC. A single resistor and capacitor are recommended to provide immunity to the high speed charge dump glitches seen at many microprocessor ADC inputs (see Figure 1).

An 8-bit ADC with a reference of 5 V will have a least significant bit (LSB) size of 5 V/256 = 19.5 mV. This corresponds to a nominal resolution of about 0.87°C.

operation without a precision voltage reference, it can still be used in such systems. Overall system requirements involving other sensors or signal inputs may dictate the need for a fixed precision ADC reference. The AD22100 can be converted to absolute voltage operation by using a precision reference as the supply voltage. For example, a 5.00 V reference can be used to power the AD22100 directly. Supply current will typically be 500 μA which is usually within the output capability of the reference. A large number of AD22100s may require an additional op amp buffer, as would scaling down a 10.00 V reference that might be found in "instrumentation" ADCs typically operating from ±15 V supplies.

Monolithic Accelerometer with Signal Conditioning

ADXL05*

FEATURES

Complete Acceleration Measurement System on a Single Monolithic IC
Full-Scale Measurement Range: ±5 g
Self-Test on Digital Command
Single Supply Operation: +5 V
Sensitivity Precalibrated to 200 mV/g
Internal Buffer Amplifier for User Adjustable Span and Zero-g Levels
Frequency Response: DC to 4 kHz
Post Filtering with External Passive Components
High Shock Survival: >1000 g Unpowered
Other Accelerometer Products, Measuring Different g Levels, Are Available

GENERAL DESCRIPTION

The ADXL05 is a low noise member of the ADXL50 family of products. It is a complete acceleration measurement system on a single monolithic IC. Three external capacitors and a +5 volt regulated power supply are all that is required to measure accelerations up to ±5 g. Device sensitivity is factory trimmed to a scale factor of 200 mV/g resulting in a full-scale output swing of ±1 volt for a ±5 g applied acceleration. Its zero-g output level is +1.8 volts.

A TTL compatible self-test function can electrostatically deflect the sensor beam at any time to verify device functionality.

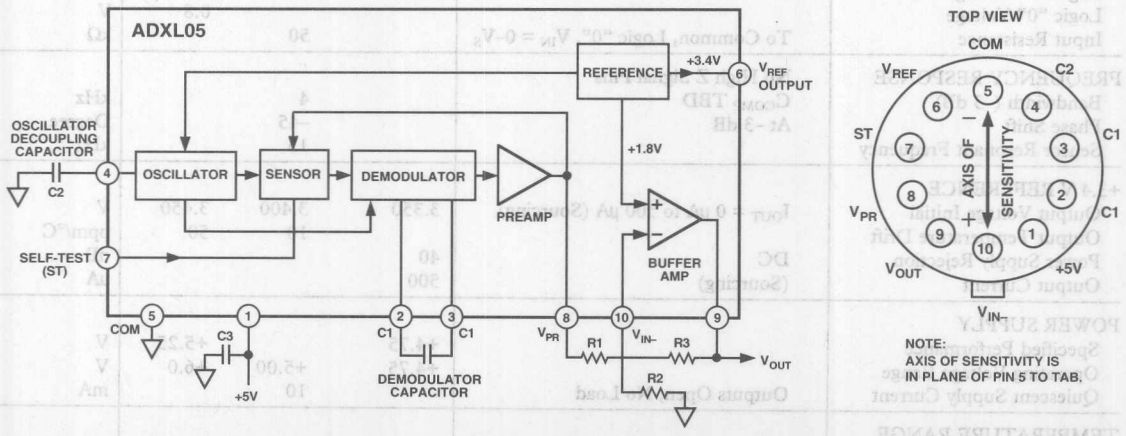
For convenience, the ADXL05 has an internal buffer amplifier with a full 0.25 V to 4.75 V output range. This may be used to set the zero-g level and change the output sensitivity by using external resistors. External capacitors may be added to the resistor network to provide 1 or 2 poles of filtering. No external active components are required to interface directly to most analog-to-digital converters (ADCs) or microcontrollers.

The ADXL05 uses a capacitive measurement method. The analog output voltage is directly proportional to acceleration and is fully scaled, referenced and temperature compensated, resulting in high accuracy and linearity over a wide temperature range. Internal circuitry implements a forced-balance control loop that improves accuracy by compensating for mechanical sensor variations.

The ADXL05 is powered from a standard +5 V supply and is robust, allowing its use in harsh industrial and automotive environments. It will survive shocks of 1000 g unpowered. The ADXL05 is available in a hermetic 10-pin TO-100 metal can. Contact factory for grades of performance and temperature ranges.

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM AND PINOUT



*Patent pending.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ADXL05–SPECIFICATIONS (T_A = +25°C, V_S = +5 V, @ Acceleration = 0 g, unless otherwise noted)

Parameter	Conditions	ADXL05 Min	Typ	Max	Units
SENSITIVITY					
@ V_{PR} Output	@ +25°C		0.2		V/g
Sensitivity Drift	T_{MIN}–T_{MAX}		±1		% of 25° Rdg.
ZERO g BIAS LEVEL AT V_{PR}					
Initial	+25°C	1.45	1.8	2.15	V
Drift	T_{MIN}–T_{MAX}		±100		mV
VOLTAGE NOISE DENSITY			500		µg/√Hz
			100		µV/√Hz
SENSOR INPUT					
FS Measurement Range			±5		g
Nonlinearity			0.5		% of FS
Alignment Error			±1		Degree
Transverse Sensitivity			±2		%
Shock Survival	Unpowered		1000		g
	Powered		500		g
BUFFER AMPLIFIER					
Output Voltage Swing	@ I_{OUT} = +300 µA (Sinking)			0.25	V
	@ I_{OUT} = –300 µA (Sourcing)	V_S–0.25			V
Input Offset Voltage	Deviation from 1.8 V Nominal		±10		mV
Input Bias Current			5	20	nA
Open-Loop Gain	DC	1	10		V/mV
Unity Gain Bandwidth			200		kHz
Capacitance Load Drive		1000			pF
Power Supply Rejection	DC	40	60		dB
SELF-TEST INPUT					
Output Change at V_{OUT}	ST Pin from Logic "0" to "1"	+0.9	+1.0	+1.1	V
Logic "1" Voltage		2.0			V
Logic "0" Voltage				0.8	V
Input Resistance	To Common, Logic "0", V_{IN} = 0–V_S		50		kΩ
FREQUENCY RESPONSE	No High Z Signal Pins				
Bandwidth (–3 dB)	C_{COMP} TBD		4		kHz
Phase Shift	At –3 dB		–45		Degree
Sensor Resonant Frequency			13		kHz
+3.4 V REFERENCE					
Output Voltage Initial	I_{OUT} = 0 µA to 500 µA (Sourcing)	3.350	3.400	3.450	V
Output Temperature Drift			10	50	ppm/°C
Power Supply Rejection	DC	40			dB
Output Current	(Sourcing)	500			µA
POWER SUPPLY					
Specified Performance		+4.75		+5.25	V
Operating Voltage Range		+4.75	+5.00	+6.0	V
Quiescent Supply Current	Outputs Open, No Load		10		mA
TEMPERATURE RANGE					
Specified Performance		–55		+125	°C

Both specifications and temperature range are subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Monolithic Accelerometer With Signal Conditioning

ADXL50*

FEATURES

Complete Acceleration Measurement System on a Single Monolithic IC
Full-Scale Measurement Range: ±50 g
Self-Test on Digital Command
+5 V Single Supply Operation
Sensitivity Precalibrated to 19 mV/g
Internal Buffer Amplifier for User Adjustable Sensitivity and Zero-g Level
Frequency Response: DC to 10 kHz
Post Filtering with External Passive Components
High Shock Survival: >2000 g Unpowered
Other Versions Available: ADXL05 (±5 g)
ADXL181 (+880 g, −150 g)

GENERAL DESCRIPTION

The ADXL50 is a complete acceleration measurement system on a single monolithic IC. Three external capacitors and a +5 volt power supply are all that is required to measure accelerations up to ±50 g. Device sensitivity is factory trimmed to 19 mV/g, resulting in a full-scale output swing of ±0.95 volts for a ±50 g applied acceleration. Its zero g output level is +1.8 volts.

A TTL compatible self-test function can electrostatically deflect the sensor beam at any time to verify device functionality.

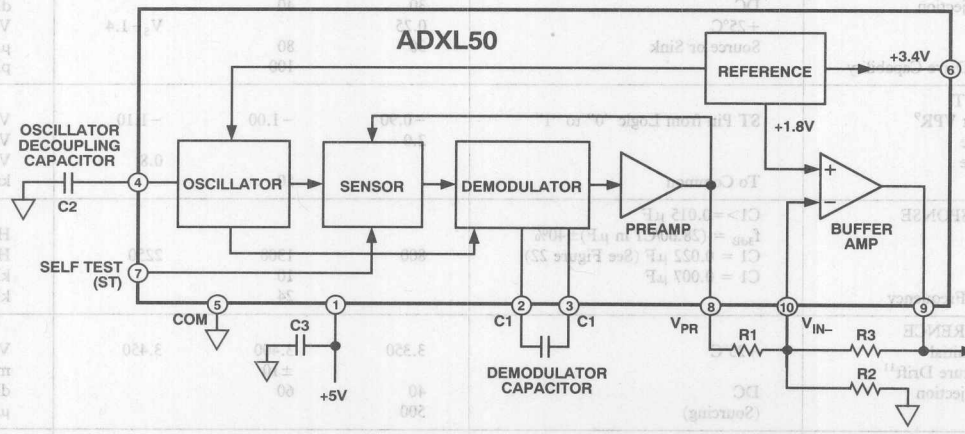
For convenience, the ADXL50 has an internal buffer amplifier with a full 0.25 V to 4.75 V output range. This may be used to set the zero-g level and change the output sensitivity by using external resistors. External capacitors may be added to the resistor network to provide 1 or 2 poles of filtering. No external active components are required to interface directly to most analog-to-digital converters (ADCs) or microcontrollers.

The ADXL50 uses a capacitive measurement method. The analog output voltage is directly proportional to acceleration, and is fully scaled, referenced and temperature compensated, resulting in high accuracy and linearity over a wide temperature range. Internal circuitry implements a forced-balance control loop that improves accuracy by compensating for any mechanical sensor variations.

The ADXL50 is powered from a standard +5 V supply and is robust for use in harsh industrial and automotive environments and will survive shocks of more than 2000 g unpowered.

The ADXL50 is available in a hermetic 10-pin TO-100 metal can, specified over the 0°C to +70°C commercial, and −40°C to +85°C industrial temperature ranges. Contact factory for availability of devices specified for operation over the −40°C to +105°C automotive and −55°C to +125°C military temperature ranges and for availability of 883B devices.

ADXL50 FUNCTIONAL BLOCK DIAGRAM



*Patents pending.

	Min	Typ	Max	Min	Typ	Max	Units
SENSITIVITY[1]							
+25°C	16.1	19.0	21.9	16.7	19.0	21.3	mV/g
Temperature Drift[2]		±0.75/1.0			±0.75/1.0/1.5	±1.75/2.0/2.5	% of RDG
ZERO g BIAS LEVEL[3]							
+25°C	1.55/1.60	1.80	2.05/2.00	1.60	1.80	2.00	V
Temperature Drift[2]		±15/35			±10/20/50	±35/50/80	mV
VOLTAGE NOISE DENSITY[4]		125	225		125	225	$\mu V/\sqrt{Hz}$
		6.6			6.6		$mg/\sqrt{Hz}$
SENSOR INPUT							
Measurement Range[5]	−50		+50	−50		+50	g
Nonlinearity[6]		0.2			0.2		% of FS
Alignment Error[7]		±1			±1		Degrees
Transverse Sensitivity[8]		±2			±2		%

NOTES

[1]As measured at the preamplifier output, V_{PR} with 15 g p-p @ 100 Hz applied.

[2]Specification refers to the maximum change in parameter from its initial value at +25°C to its worst case value at T_{MIN} or T_{MAX}.

[3]As measured at V_{PR}.

[4]BW = 10 Hz to 1 kHz. A capacitor, C2, greater than or equal to 0.022 μF, must be connected from the oscillator decoupling capacitor pin to ground.

[5]The axis of sensitivity of the device is a straight line drawn through the package along its most sensitive axis. For the 10-pin header (TO-100) package, this line passes through Pin 5 and the tab. See device connection and orientation figures.

[6]Best Fit Straight Line. Full scale = 50 g.

[7]Alignment error is specified as the angle between the true and indicated axis of sensitivity. The ADXL50 output will be the true acceleration times the cosine of the alignment error angle.

[8]Transverse sensitivity is measured with an applied acceleration which is 90° (i.e., transverse) from the indicated axis of sensitivity. Transverse sensitivity error is specified as the percent of transverse acceleration which appears at the V_{PR} output. This is the algebraic sum of the alignment and the inherent sensor sensitivity errors.

Specifications subject to change without notice.

*Contact factory for availability.

ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_S = +5$ V ± 5%, @ Acceleration = 0 g, and C1 = C2 = 0.022 μF unless otherwise noted)

Parameter	Conditions	ADXL50J/A/K/B/T Min	Typ	Max	Units
PREAMPLIFIER OUTPUT					
Power Supply Rejection	DC	30	40		dB
Voltage Swing	+25°C	0.25		$V_S-1.4$	V
Current Output	Source or Sink	30	80		μA
Capacitive Load Drive Capability			100		pF
SELF TEST INPUT					
Output Change at VPR[9]	ST Pin from Logic "0" to "1"	−0.90	−1.00	−1.10	V
Logic "1" Voltage		2.0			V
Logic "0" Voltage				0.8	V
Input Impedance	To Common		50		kΩ
FREQUENCY RESPONSE	C1>=0.015 μF				
3 dB Equation	f_{3dB} = (28.60/C1 in μF)±40%				Hz
Bandwidth[10]	C1 = 0.022 μF (See Figure 22)	800	1300	2250	Hz
	C1 = 0.007 μF		10		kHz
Sensor Resonant Frequency			24		kHz
+3.4 VOLT REFERENCE					
Output Voltage Initial	+25°C	3.350	3.400	3.450	V
Output Temperature Drift[11]			±10		mV
Power Supply Rejection	DC	40	60		dB
Output Current	(Sourcing)	500			μA
BUFFER AMPLIFIER					
Input Offset Voltage[12]	Deviation from Nominal 1.800 V		±10	±25	mV
Input Bias Current			5	20	nA
Open Loop Gain	DC		80		dB
Unity Gain Bandwidth			200		kHz
Output Voltage Swing	I_{OUT} = ±100 μA	0.25		$V_S-0.25$	V
Capacitive Load Drive Capability		1000			pF
Power Supply Rejection	DC	40	60		dB
POWER SUPPLY					
Specified Performance		+4.75		+5.25	V
Operating Voltage Range		+4.75	+5.00	+6.0	V
Quiescent Supply Current			10	13	mA

Parameter	Conditions	ADXL50J/A/K/B/T Min	Typ	Max	Units
TEMPERATURE RANGE					
Specified Performance J, K		0		+70	°C
Specified Performance A, B		−40		+85	°C
Specified Performance T*		−55		+125	°C
Automotive Grade*		−40		+105	°C

NOTES
[9]Applying logic "high" to the self-test input has an effect on the acceleration sensing element equivalent to applying an acceleration of minus 52.6 g to the ADXL50.
[10]This is the deviation from the ideal 3 dB bandwidth using an exact C1 value.
[11]Specification refers to the maximum change in parameter from its initial value at +25°C to its worst case value at T_{MIN} or T_{MAX}.
[12]Input offset voltage is defined as an output voltage (referred to input at buffer $-V_{IN}$ terminal) when the buffer amplifier is connected as a follower. The voltage at this pin has a temperature drift proportional to that of the +3.4 V reference.
*Contact factory for availability.
Specifications subject to change without notice.
All min and max specifications are guaranteed. Typical specifications are not tested or guaranteed.

ABSOLUTE MAXIMUM RATINGS**

Acceleration (Any Axis, Unpowered for 0.5 ms) . . . . . 2000 g
Acceleration (Any Axis, Powered for 0.5 ms) . . . . . 500 g
$+V_S$ . . . . . −0.3 V to +7.0 V
Output Short Circuit Duration
(V_{PR}, V_{OUT}, V_{REF} Terminals to Common) . . . . . Indefinite
Operating Temperature . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C

**Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Characteristics

Package	θ_{JA}	θ_{JC}	Device Weight
10-Pin TO-100	130°C/W	30°C/W	5 Grams

ORDERING GUIDE

Model	Temperature Range	Typ 0 g Bias Drift	Max 0 g Bias Drift	Package Option[1]
ADXL50JH	0°C to +70°C	±15 mV		H-10A
ADXL50KH[2]	0°C to +70°C	±10 mV	±35 mV	H-10A
ADXL50AH	−40°C to +85°C	±35 mV		H-10A
ADXL50BH[2]	−40°C to +85°C	±20 mV	±50 mV	H-10A
ADXL50TH[2]	−55°C to +125°C	±50 mV	±80 mV	H-10A

NOTES
[1]For outline information see Package Information section.
[2]Contact factory for availability.

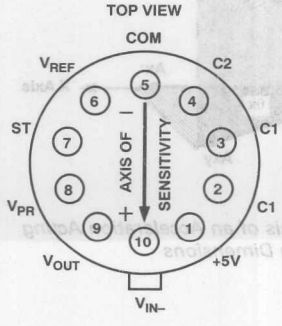
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADXL50 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ADXL50 PIN DESCRIPTION

+5 V	The power supply input pin.
C2	Connection for an external bypass capacitor (nominally 0.022 μF) used to prevent oscillator switching noise from interfering with other ADXL50 circuitry. Please see the section on component selection.
C1	Connections for the demodulator capacitor, nominally 0.022 μF. See the section on component selection for application information.
COM	The power supply common (or "ground") connection.
V_{REF}	Output of the internal 3.4 V voltage reference.
ST	The digital self-test input. It is both CMOS and TTL compatible.
V_{PR}	The ADXL50 preamplifier output providing an output voltage of 19 mV per g of acceleration.
V_{OUT}	Output of the uncommitted buffer amplifier.
V_{IN-}	The inverting input of the uncommitted buffer amplifier.

ADXL50 10-HEADER (TO-100) CONNECTION DIAGRAM



NOTES:
AXIS OF SENSITIVITY IS ALONG A LINE BETWEEN PIN 5 AND THE TAB.
THE CASE OF THE METAL CAN PACKAGE IS CONNECTED TO PIN 5 (COMMON).
ARROW INDICATES DIRECTION OF POSITIVE ACCELERATION ALONG AXIS OF SENSITIVITY.

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Figure 1. Output Polarity at V_{PR}

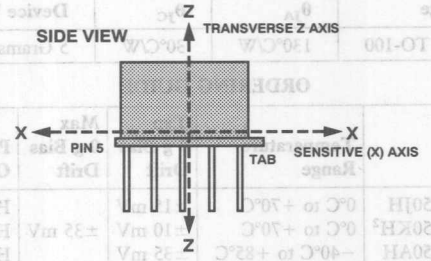

Figure 2a. Sensitive X and Transverse Z Axis

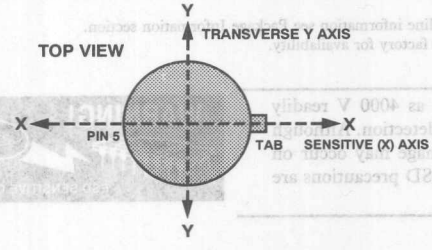

Figure 2b. Sensitive X and Transverse Y Axis

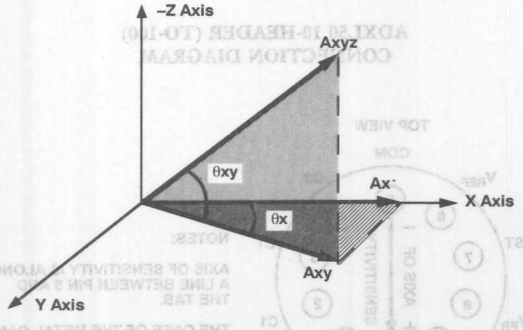

Figure 2c. A Vector Analysis of an Acceleration Acting Upon the ADXL50 in Three Dimensions

Polarity of the Acceleration Output

The polarity of the ADXL50 output is shown in the Figure 1. When oriented to the earth's gravity (and held in place), the ADXL50 will experience an acceleration of +1 g. This corresponds to a change of approximately +19 mV at the V_{PR} output pin. Note that the polarity will be reversed to a negative going signal at the buffer amplifier output V_{OUT}, due to its inverting configuration.

Mounting Considerations

There are three main causes of measurement error when using accelerometers. The first two are alignment and transverse sensitivity errors. The third source of error is due to resonances or vibrations of the sensor in its mounting fixture.

Errors Due to Misalignment

The ADXL50 is a sensor designed to measure accelerations that result from an applied force. Because these forces act on the sensor in a vector manner, the alignment of the sensor to the force to be measured may be critical.

The ADXL50 responds to the component of acceleration on its sensitive X axis. Figures 2a and 2b show the relationship between the sensitive "X" axis and the transverse "Z" and "Y" axes as they relate to the TO-100 package.

Figure 2c describes a three dimensional acceleration vector (A_{XYZ}) which might act on the sensor, where A_X is the component of interest. To determine A_X, first, the component of acceleration in the XY plane (A_{XY}) is found using the cosine law:

$$A_{XY} = A_{XYZ}\,(cos\theta_{XY})\ then$$
$$A_X = A_{XY}\,(cos\theta_X)$$

Therefore: Typical $V_{PR} = 19\ mV/g\ (A_{XYZ})\ (cos\theta_{XY})\ cos\theta_X$.

Note that an ideal sensor will react to forces along or at angles to its sensitive axis but will reject signals from its various transverse axes, i.e., those exactly 90° from the sensitive "X" axis. But even an ideal sensor will produce output signals if the transverse signals are not exactly 90° to the sensitive axis. An acceleration that is acting on the sensor from a direction different from the sensitive axis will show up at the ADXL50 output at a reduced amplitude.

Table I. Ideal Output Signals for Off Axis Applied Accelerations Disregarding Device Alignment and Transverse Sensitivity Errors

θ_X	% of Signal Appearing at Output	Output in g's for a 50 g Applied Acceleration
0	100%	50 (On Axis)
1°	99.98%	49.99
2°	99.94%	49.97
3°	99.86%	49.93
5°	99.62%	49.81
10°	98.48%	49.24
30°	86.60%	43.30
45°	70.71%	35.36
60°	50.00%	25.00
80°	17.36%	8.68
85°	8.72%	4.36
87°	5.25%	2.63
88°	3.49%	1.75
89°	1.7%	0.85
90°	0%	0.00 (Transverse Axis)

Table I shows the percentage signals resulting from various θ_X angles. Note that small errors in alignment have a negligible effect on the output signal. A 1° error will only cause a 0.02% error in the signal. Note, however, that a signal coming 1° off of the transverse axis (i.e., 89° off the sensitive axis) will still contribute 1.7% of its signal to the output. Thus large transverse signals could cause output signals as large as the signals of interest.

Table I may also be used to approximate the effect of the ADXL50's internal errors due to misalignment of the die to the package. For example: a 1 degree sensor alignment error will allow 1.7% of a transverse signal to appear at the output. In a nonideal sensor, transverse sensitivity may also occur due to inherent sensor properties. That is, if the sensor physically moves due to a force applied exactly 90° to its sensitive axis, then this might be detected as an output signal, whereas an ideal sensor would reject such signals. In every day use, alignment errors may cause a small output peak with accelerations applied close to the sensitive axis but the largest errors are normally due to large accelerations applied close to the transverse axis.

Errors Due to Mounting Fixture Resonances

A common source of error in acceleration sensing is resonance of the mounting fixture. For example, the circuit board that the ADXL50 mounts to may have resonant frequencies in the same range as the signals of interest. This could cause the signals measured to be larger than they really are. A common solution to this problem is to dampen these resonances by mounting the ADXL50 near a mounting post or by adding extra screws to hold the board more securely in place.

When testing the accelerometer in your end application, it is recommended that you test the application at a variety of frequencies in order to ensure that no major resonance problems exist.

GLOSSARY OF TERMS

Acceleration: Change in velocity per unit time.

Acceleration Vector: Vector describing the net acceleration acting upon the ADXL50 (A_{XYZ}).

g: A unit of acceleration equal to the average force of gravity occurring at the earth's surface. A g is approximately equal to 32.17 feet/s^2, or 9.807 meters/s^2.

Nonlinearity: The maximum deviation of the ADXL50 output voltage from a best fit straight line fitted to a plot of acceleration vs. output voltage, calculated as a % of the full-scale output voltage (@ 50 g).

Resonant Frequency: The natural frequency of vibration of the ADXL50 sensor's central plate (or "beam"). At its resonant frequency of 24 kHz, the ADXL50's moving center plate has a peak in its frequency response with a Q of 3 or 4.

Sensitivity: The output voltage change per g unit of acceleration applied, specified at the V_{PR} pin in mV/g.

Sensitive Axis (X) The most sensitive axis of the accelerometer sensor. Defined by a line drawn between the package tab and Pin 5 in the plane of the pin circle. See Figures 2a and 2b.

Sensor Alignment Error: Misalignment between the ADXL50's on-chip sensor and the package axis, defined by Pin 5 and the package tab.

Total Alignment Error: Net misalignment of the ADXL50's on-chip sensor and the measurement axis of the application. This error includes errors due to sensor die alignment to the package, and any misalignment due to installation of the sensor package in a circuit board or module.

Transverse Acceleration: Any acceleration applied 90° to the axis of sensitivity.

Transverse Sensitivity Error: The percent of a transverse acceleration that appears at the V_{PR} output. For example, if the transverse sensitivity is 1%, then a +10 g transverse acceleration will cause a 0.1 g signal to appear at V_{PR} (1% of 10 g). Transverse sensitivity can result from a sensitivity of the sensor to transverse forces or from misalignment of the internal sensor to its package.

Transverse Y Axis: The axis perpendicular (90°) to the package axis of sensitivity in the plane of the package pin circle. See Figure 2.

Transverse Z Axis: The axis perpendicular (90°) to both the package axis of sensitivity and the plane of the package pin circle. See Figure 2.

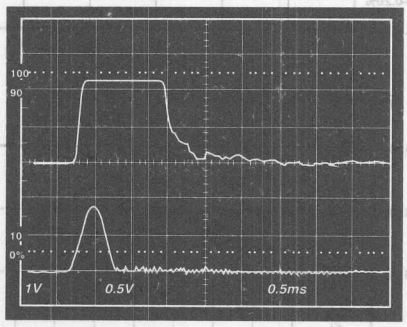

Figure 3. 500 g Shock Overload Recovery. Top Trace: ADXL50 Output. Bottom Trace: Reference Accelerometer Output

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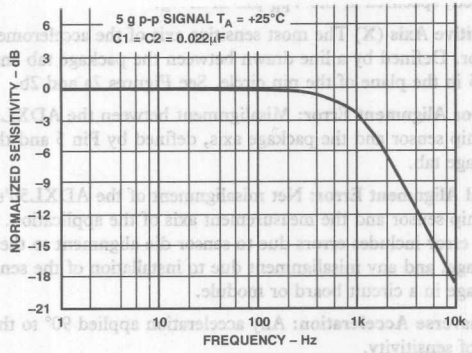

Figure 4. Normalized Sensitivity vs. Frequency

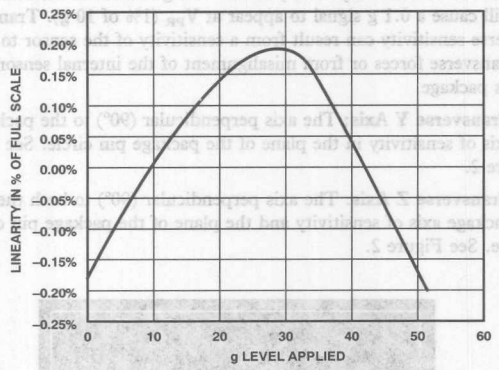

Figure 5. Linearity in Percent of Full Scale

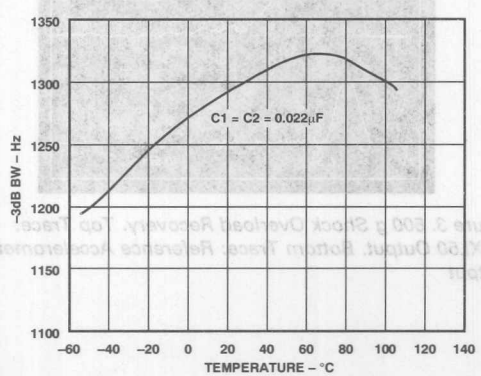

Figure 6. −3 dB Bandwidth vs. Temperature at V_{PR}

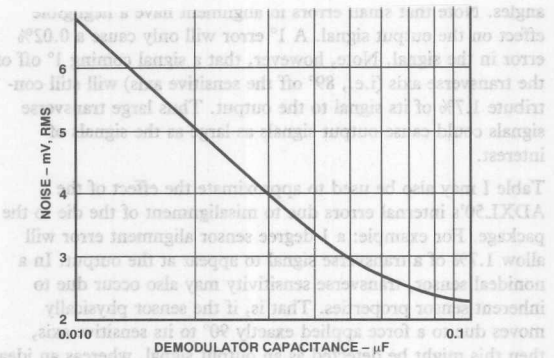

Figure 7. RMS Noise vs. Value of Demodulator Capacitor, C1

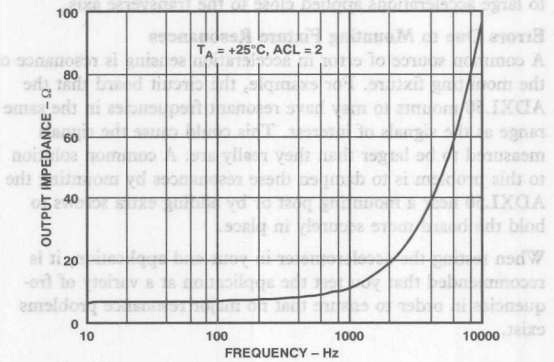

Figure 8. Buffer Amplifier Output Impedance vs. Frequency

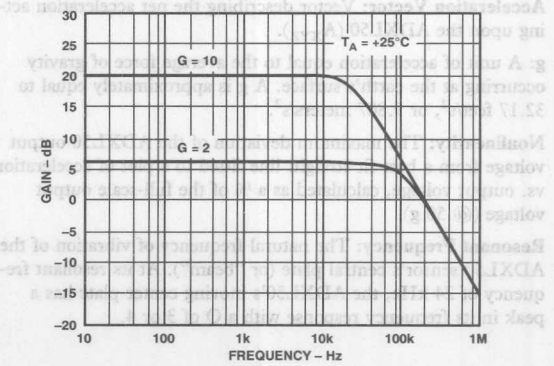

Figure 9. Buffer Amplifier Closed-Loop Gain vs. Frequency

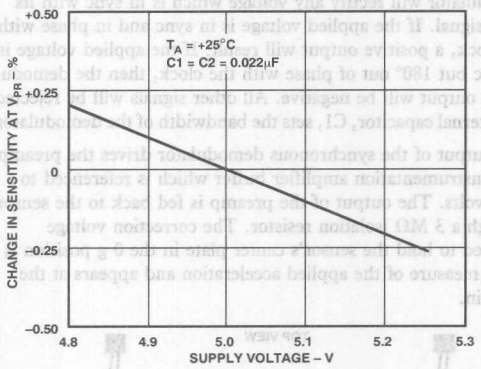

Figure 10. Change in Sensitivity vs. Supply Voltage

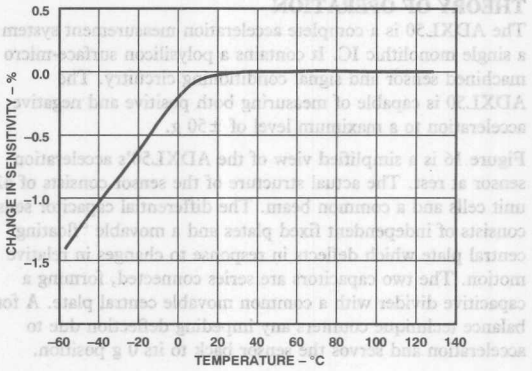

Figure 13. Percent Change In Sensitivity at V_{PR} vs. Temperature

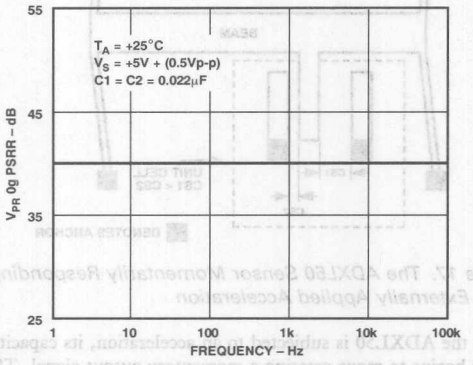

Figure 11. V_{PR} 0 g PSRR vs. Frequency

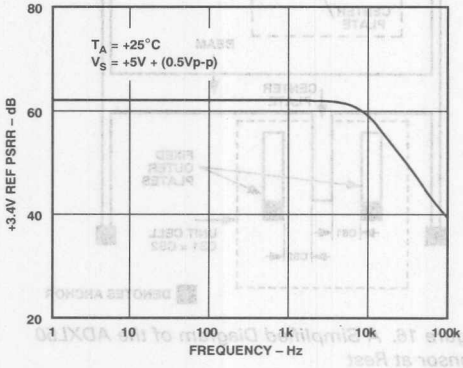

Figure 14. +3.4 V REF PSRR vs. Frequency

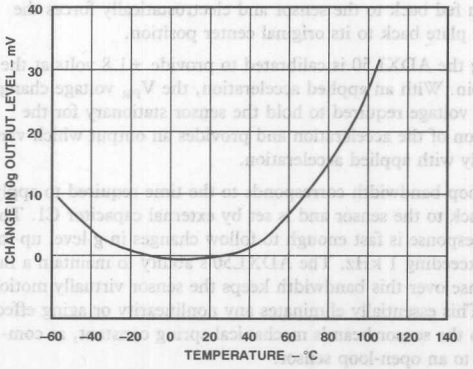

Figure 12. 0 g Bias Level vs. Temperature

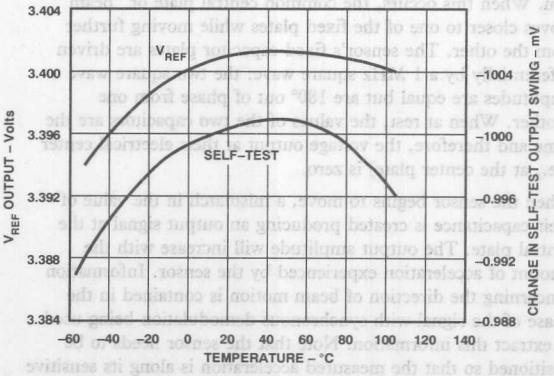

Figure 15. V_{REF} Output and Change in Self-Test Output Swing vs. Temperature

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THEORY OF OPERATION

The ADXL50 is a complete acceleration measurement system on a single monolithic IC. It contains a polysilicon surface-micro machined sensor and signal conditioning circuitry. The ADXL50 is capable of measuring both positive and negative acceleration to a maximum level of ±50 g.

Figure 16 is a simplified view of the ADXL50's acceleration sensor at rest. The actual structure of the sensor consists of 42 unit cells and a common beam. The differential capacitor sensor consists of independent fixed plates and a movable "floating" central plate which deflects in response to changes in relative motion. The two capacitors are series connected, forming a capacitive divider with a common movable central plate. A force balance technique counters any impeding deflection due to acceleration and servos the sensor back to its 0 g position.

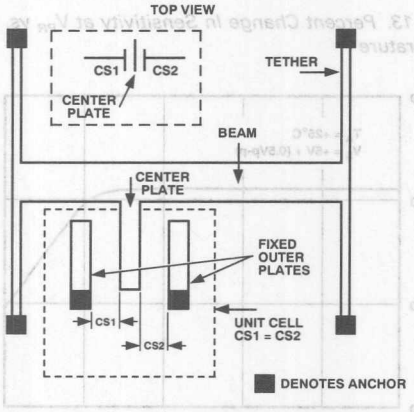

Figure 16. A Simplified Diagram of the ADXL50 Sensor at Rest

Figure 17 shows the sensor responding to an applied acceleration. When this occurs, the common central plate or "beam" moves closer to one of the fixed plates while moving further from the other. The sensor's fixed capacitor plates are driven deferentially by a 1 MHz square wave: the two square wave amplitudes are equal but are 180° out of phase from one another. When at rest, the values of the two capacitors are the same and therefore, the voltage output at their electrical center (i.e., at the center plate) is zero.

When the sensor begins to move, a mismatch in the value of their capacitance is created producing an output signal at the central plate. The output amplitude will increase with the amount of acceleration experienced by the sensor. Information concerning the direction of beam motion is contained in the phase of the signal with synchronous demodulation being used to extract this information. Note that the sensor needs to be positioned so that the measured acceleration is along its sensitive axis.

Figure 18 shows a block diagram of the ADXL50. The voltage output from the central plate of the sensor is buffered and then applied to a synchronous demodulator. The demodulator is also supplied with a (nominal) 1 MHz clock signal from the same oscillator which drives the fixed plates of the sensor. The demodulator will rectify any voltage which is in sync with its clock signal. If the applied voltage is in sync and in phase with the clock, a positive output will result. If the applied voltage is in sync but 180° out of phase with the clock, then the demodulator's output will be negative. All other signals will be rejected. An external capacitor, C1, sets the bandwidth of the demodulator.

The output of the synchronous demodulator drives the preamp —an instrumentation amplifier buffer which is referenced to +1.8 volts. The output of the preamp is fed back to the sensor through a 3 MΩ isolation resistor. The correction voltage required to hold the sensor's center plate in the 0 g position is a direct measure of the applied acceleration and appears at the V_{PR} pin.

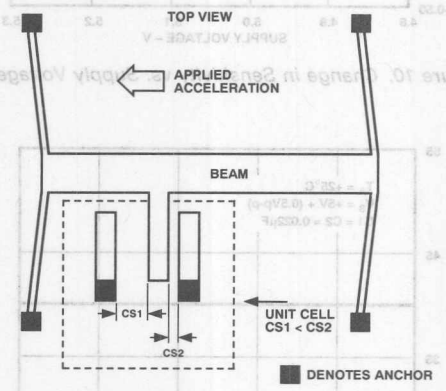

Figure 17. The ADXL50 Sensor Momentarily Responding to an Externally Applied Acceleration

When the ADXL50 is subjected to an acceleration, its capacitive sensor begins to move creating a momentary output signal. This is signal conditioned and amplified by the demodulator and preamp circuits. The dc voltage appearing at the preamp output is then fed back to the sensor and electrostatically forces the center plate back to its original center position.

At 0 g the ADXL50 is calibrated to provide +1.8 volts at the V_{PR} pin. With an applied acceleration, the V_{PR} voltage changes to the voltage required to hold the sensor stationary for the duration of the acceleration and provides an output which varies directly with applied acceleration.

The loop bandwidth corresponds to the time required to apply feedback to the sensor and is set by external capacitor C1. The loop response is fast enough to follow changes in g level up to and exceeding 1 kHz. The ADXL50's ability to maintain a flat response over this bandwidth keeps the sensor virtually motionless. This essentially eliminates any nonlinearity or aging effects due to the sensor beam's mechanical spring constant, as compared to an open-loop sensor.

An uncommitted buffer amplifier provides the capability to adjust the scale factor and 0 g offset level over a wide range. An internal reference supplies the necessary regulated voltages for powering the chip and +3.4 volts for external use.

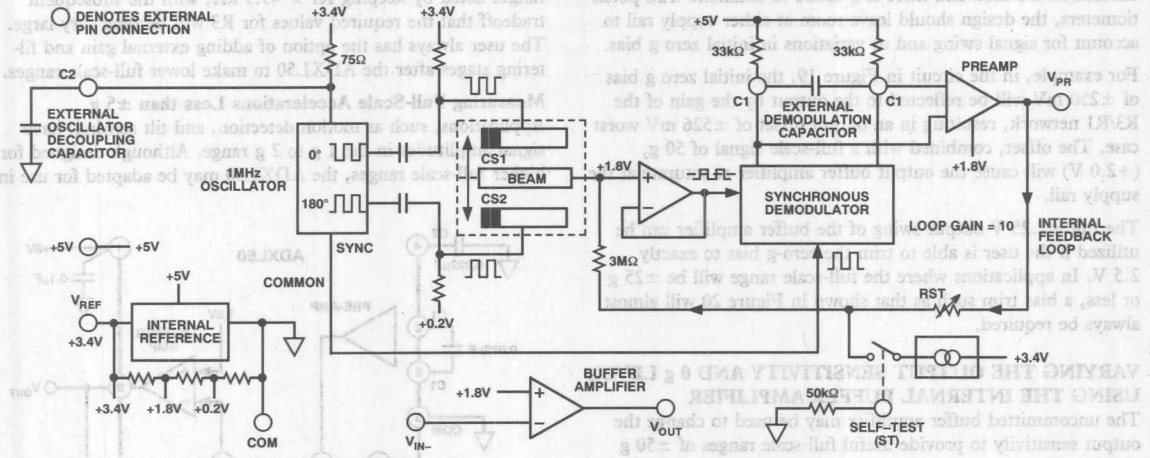

Figure 18. ADXL50 Functional Block Diagram

The sensor's tight mechanical spacing allows it to be electrostatically deflected to full scale while operating on a 5 volt supply. A self-test is initiated by applying a TTL "high" level voltage (>+2.0 V) to the ADXL50's self-test pin which causes the chip to apply a deflection voltage to the beam which moves it an amount equal to −50 g (the negative full-scale output of the device). Note that the ±10% tolerance of the self-test circuit is not proportional to the sensitivity error, see Self-Test section.

The output of the ADXL50's preamplifier is 1.8 V at 0 g acceleration with an output range of ±0.95 V for a ±50 g input, i.e., 19 mV/g. An uncommitted buffer amplifier has been included on-chip to enhance the user's ability to offset the 0 g signal level and to amplify and filter the signal. Access is provided to both the inverting input and the output of this amplifier via pins V_{OUT} and V_{IN-}, while the noninverting input is connected internally to a +1.8 V reference. The +1.8 V is derived from a resistor divider connected to the 3.4 V reference.

BASIC CONNECTIONS FOR THE ADXL50

Figure 19 shows the basic connections needed for the ADXL50 to measure accelerations in the ±50 g range with an output scale factor 40 mV/g corresponding to a 2.5 V 0 g level, a ±2.0 V full-scale swing around 0 g and a 3 dB bandwidth of approximately 1 kHz.

In general, the designer will need to take into account the initial zero g bias when designing circuits. For the ADXL50J this offset is 1.8 V ± 250 mV. When microprocessors and software

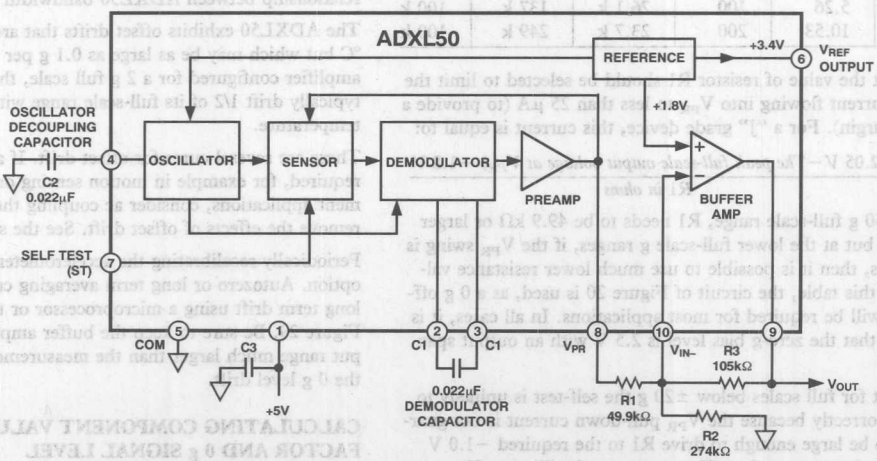

Figure 19. ADXL50 Application Providing an Output Sensitivity of 40 mV/g, a +2.5 V 0 g Level and a Bandwidth of 1 kHz

calibration are used and there is a desire to eliminate trim potentiometers, the design should leave room at either supply rail to account for signal swing and or variations in initial zero g bias.

For example, in the circuit in Figure 19, the initial zero g bias of ±250 mV will be reflected to the output by the gain of the R3/R1 network, resulting in an output offset of ±526 mV worst case. The offset, combined with a full-scale signal of 50 g, (+2.0 V) will cause the output buffer amplifier to saturate at the supply rail.

The full ±2.25 V output swing of the buffer amplifier can be utilized if the user is able to trim the zero-g bias to exactly 2.5 V. In applications where the full-scale range will be ±25 g or less, a bias trim such as that shown in Figure 20 will almost always be required.

VARYING THE OUTPUT SENSITIVITY AND 0 g LEVEL USING THE INTERNAL BUFFER AMPLIFIER

The uncommitted buffer amplifier may be used to change the output sensitivity to provide useful full-scale ranges of ±50 g and below. Table II provides recommended resistor values for several standard ranges down to ±10 g. As the full-scale range is decreased, buffer amplifier gain is increased, and the noise contribution as a percentage of full scale will also increase. For all ranges, the signal-to-noise ratio can be improved by reducing the circuit bandwidth, either by increasing the demodulator capacitor, C1, or by adding a post filter using the buffer amplifier.

Table II. Recommended Resistor Values for Setting the Circuit of Figure 20 to Several Common Full-Scale Ranges

FS (g)	Buffer Gain	SF in mV/g	R1	R3	R2
±50.0	2.11	40	49.9 k	105 k	100 k
±40.0	2.63	50	39.2 k	103 k	100 k
±30.8	3.42	65	40.2 k	137 k	100 k
±26.7	3.95	75	28.7 k	113 k	100 k
±20.0	5.26	100	26.1 k	137 k	100 k
±10.0	10.53	200	23.7 k	249 k	100 k

Note that the value of resistor R1 should be selected to limit the output current flowing into V_{PR} to less than 25 µA (to provide a safety margin). For a "J" grade device, this current is equal to:

$$I_{PR} = \frac{(2.05\ V - \textit{The peak full-scale output voltage at } V_{PR}) - 1.8\ V}{R1\ \textit{in ohms}}$$

For a ±50 g full-scale range, R1 needs to be 49.9 kΩ or larger in value; but at the lower full-scale g ranges, if the V_{PR} swing is much less, then it is possible to use much lower resistance values. For this table, the circuit of Figure 20 is used, as a 0 g offset trim will be required for most applications. In all cases, it is assumed that the zero-g bias level is 2.5 V with an output span of ±2 V.

Note that for full scales below ±20 g the self-test is unlikely to operate correctly because the V_{PR} pull-down current is not guaranteed to be large enough to drive R1 to the required −1.0 V swing. In these cases, the self-test command will cause V_{OUT} to saturate at the rail, and it will be necessary to monitor the self-test at V_{PR}. Self-test can remain operational at V_{PR} for all g ranges listed by keeping R1 > 49.9 kΩ, with the subsequent tradeoff that the required values for R3 will become very large. The user always has the option of adding external gain and filtering stages after the ADXL50 to make lower full-scale ranges.

Measuring Full-Scale Accelerations Less than ±5 g

Applications, such as motion detection, and tilt sensing, have signal amplitudes in the 1 g to 2 g range. Although designed for higher full-scale ranges, the ADXL50 may be adapted for use in low g applications; the two main design considerations are noise and 0 g offset drift (BH, KH grades recommended).

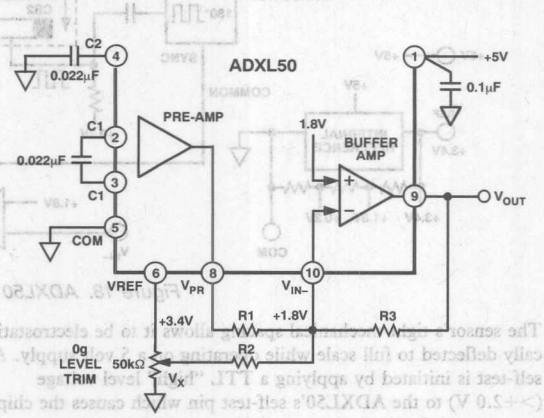

Figure 20. ADXL50 Circuit Using the Buffer Amplifier to Set the Output Scaling and 0 g Offset Level

At its full 1 kHz bandwidth, the ADXL50 will typically exhibit 1 g p-p of noise. With ±50 g accelerations this is generally not a problem, but at a ±2 g full-scale level the signal-to-noise ratio will be very poor. However, reducing the bandwidth to 100 Hz or less considerably improves the S/N ratio. Figure 25 shows the relationship between ADXL50 bandwidth and noise.

The ADXL50 exhibits offset drifts that are typically 0.02 g per °C but which may be as large as 0.1 g per °C. With the buffer amplifier configured for a 2 g full scale, the ADXL50 will typically drift 1/2 of its full-scale range with a 50°C increase in temperature.

There are several cures for offset drift. If a dc response is not required, for example in motion sensing or vibration measurement applications, consider ac coupling the acceleration signal to remove the effects of offset drift. See the section on ac coupling.

Periodically recalibrating the accelerometer's 0 g level is another option. Autozero or long term averaging can be used to remove long term drift using a microprocessor or the autozero circuit of Figure 29. Be sure to keep the buffer amplifier's full-scale output range much larger than the measurement range to allow for the 0 g level drift.

CALCULATING COMPONENT VALUES FOR SCALE FACTOR AND 0 g SIGNAL LEVEL

The ADXL50 buffer's scale factor is set by −R3/R1 (since the amplifier is in the inverter mode).

As an example, if the desired span is ±2.0 V for a ±50 g input, then R3/R1 should be chosen such that

$$R3/R1 = V_{OUT}\ Span/V_{PR}\ Span = 2.00/0.95 = 2.105 \quad (1)$$

where V_{PR} span is the output from the preamplifier and V_{OUT} span is the buffer amplifier's output, giving

$$R3 = 2.105 \times R1 \quad (2)$$

In noncritical applications, a resistor, R2, may simply be connected between V_{IN-} and common to provide an approximate 0 g offset level (see Figure 19). In this simplified configuration R2 is found using:

$$R2 = (1.8\ V \times R3)/(V_{OUT} @\ 0\ g - 1.8\ V)$$

When used with a trim potentiometer, as in Figure 20, resistor R2 sets the 0 g offset range and also sets the resolution of the offset trim. A value of 100 kΩ is typical. Increasing R2 above this value makes trimming the offset easier, but may not provide enough trim range to set V_{OUT} equal to +2.5 V for all devices.

To provide an output span of ±2.00 V, with a 0 g output of +2.5 V, R1 could be set to the standard value of 49.9 kΩ and from Equation 2, R3 = 105 kΩ.

For Figure 20, the circuit transfer function is:

$$V_{OUT} = \left(\frac{R3}{R1}(1.8\ V - V_{PR})\right) + \left(\frac{R3}{R2}(1.8\ V - V_X)\right) + 1.8\ V$$

The summing amplifier configuration allows noninteractive trimming of offset and span. Since V_{PR} is not always exactly 1.8 V at 0 g, it will contribute to output offset. Therefore, span must be trimmed first, followed by 0 g offset adjustment.

LOAD DRIVE CAPABILITIES OF THE V_{PR} AND BUFFER OUTPUTS

The V_{PR} and the buffer amplifier outputs are both capable of driving a load to voltage levels approaching that of the supply rail. However, both outputs are limited in how much current they can supply, affecting component selection.

V_{PR} Output

The V_{PR} pin has the ability to source current up to 500 μA but only has a sinking capability of 30 μA which limits its ability to drive loads. It is recommended that the buffer amplifier be used in most applications, to avoid loading down V_{PR}. In standard ±50 g applications, the resistor R1 from V_{PR} to V_{IN-} is recommended to have a value greater than 50 kΩ to reduce loading effects.

Capacitive loading of the V_{PR} pin should be minimized. A load capacitance between the V_{PR} pin and common will introduce an offset of approximately 1 mV for every 10 pF of load. The V_{PR} pin may be used to directly drive an A/D input or other source as long as these sensitivities are taken into account. It is always preferable to drive A/D converters or other sources using the buffer amplifier (or an external op amp) instead of the V_{PR} pin.

Buffer Amplifier Output

The buffer output can drive a load to within 0.25 V of either power supply rail and is capable of driving 1000 pF capacitive loads. Note that a capacitance connected across the buffer feedback resistor for low-pass filtering does not appear as a capacitive load to the buffer. The buffer amplifier is limited to sourcing or sinking a maximum of 100 μA. Component values for the resistor network should be selected to ensure that the buffer amplifier can drive the filter under worst case transient conditions.

SELF-TEST FUNCTION

The digital self-test input is compatible with both CMOS and TTL signals. A Logic "1" applied to the self-test (ST) input will cause an electrostatic force to be applied to the sensor which will cause it to deflect to the approximate negative full-scale output of the device. Accordingly, a correctly functioning accelerometer will respond by initiating an approximate −1 volt output change at V_{PR}. If the ADXL50 is experiencing an acceleration when the self-test is initiated, the V_{PR} output will equal the algebraic sum of the two inputs. The output will stay at the self-test level as long as the ST input remains high and will return to the 0 g level when the ST voltage is removed.

A self-test output that varies more than ±10% from the nominal −1.0 V change indicates a defective beam or a circuit problem such as an open or shorted pin or component.

Operating the ADXL50's buffer amplifier at Gains > 2, to provide full-scale outputs of less than ±50 g, may cause the self-test output to overdrive the buffer into saturation. The self-test may still be used in the case, but the change in the output must then be monitored at the V_{PR} pin instead of the buffer output.

Note that the value of the self-test delta is not an exact indication of the sensitivity (mV/g) of the ADXL50 and, therefore, may not be used to calibrate the device for sensitivity error.

In critical applications, it may be desirable to monitor shifts in the zero-g bias voltage from its initial value. A shift in the 0 g bias level may indicate that the 0 g level has shifted which may warrant an alarm.

POWER SUPPLY DECOUPLING

The ADXL50 power supply should be decoupled with a 0.1 μF ceramic capacitor from +5 V pin of the ADXL50 to common using very short component leads. For other decoupling considerations, see EMI/RFI section.

OSCILLATOR DECOUPLING CAPACITOR, C2

An oscillator decoupling capacitor, C2, is used to remove 1 MHz switching transients in the sensor excitation signal, and is required for proper operation of the ADXL50. A ceramic capacitor with a minimum value of 0.022 μF is recommended from the oscillator decoupling capacitor pin to common. Small amounts of capacitor leakage due to a dc resistance greater than 1 MΩ will not affect operation (i.e., a high quality capacitor is not needed here). As with the power supply bypass capacitor, very short component leads are recommended. Although 0.022 μF is a good typical value, it may be increased for reasons of convenience, but doing this will not improve the noise performance of the ADXL50.

DEMODULATOR CAPACITOR, C1

The demodulator capacitor is connected across Pins 2 and 3 to filter the demodulated signal from the sensor beam and to set the bandwidth of the force balance control loop. This capacitor may be used to approximately set the bandwidth of the accelerometer. A capacitor is always required for proper operation.

The frequency response of the ADXL50 exhibits a single pole roll-off response whose nominal 3 dB frequency is set by the following equation:

$$f_{3\,dB} = (28.60/C1\ in\ \mu F)\ \pm 40\%$$

A nominal value of 0.022 μF is recommended for C1. In general, the design bandwidth should be set 40% higher than the minimum desired system bandwidth due to the ±40% tolerance.

A minimum value of 0.015 μF is required, (over temperature and system life), to prevent device instability or oscillation. The demodulation capacitor should be a low leakage, low drift ceramic type with an NPO (best) or X7R (good) dielectric.

In general, it's best to use the recommended 0.022 μF capacitor across the demodulator pins and perform any additional low-pass filtering using the buffer amplifier. Using a large denominator capacitor for low-pass filtering has the disadvantage that the capacitive sensor will be slow to respond to rapid changes in acceleration and, therefore, the full shock survivability of the device could be compromised. The use of the buffer for low-pass filtering generally results in smaller capacitance values and better overall performance. It is also a convenient and more precise way to set the system bandwidth. Post filtering allows bandwidth to be controlled accurately by component selection and avoids the ±40% demodulation tolerance. Note that signal noise is proportional to the square root of the bandwidth of the ADXL50 and may be a consideration in component selection—see section on noise.

Care should be taken to reduce or eliminate any leakage paths from the demodulator capacitor pins to common or to the +5 V pin. Even a small imbalance in the leakage paths from these pins will result in offset shifts in the zero-g bias level. As an example, an unbalanced parasitic resistance of 30 MΩ from either demodulator pin to ground will result in an offset shift at V_{PR} of approximately 50 mV. Conformal coating of PC boards with a high impedance material is recommended to avoid leakage problems due to aging or moisture.

REDUCING THE AVERAGE POWER CONSUMPTION OF THE ADXL50

The ADXL50 is a versatile accelerometer that can be used in a wide variety of applications. In some battery powered applications, such as shipping recorders, power consumption is a critical parameter. The ADXL50 typically draws 10 mA current from a 5 V power supply which may exceed the power budgeted for the accelerometer.

For such applications, the ADXL50 can be successfully power cycled, where the power is turned on only during the period when data is sampled. Figure 21 illustrates the power-on settling of the ADXL50 during cycling where the output amplifier has a gain of one with no filtering. The settling time-constant is approximately 0.12 ms, waiting 1 ms before sampling ensures maximally accurate readings.

For example, to reduce the average power to 5 mW from its typical 50 mW, the power should be on 10% of the time. With the power on for 1 ms and off for 9 ms, a maximum sample rate of 100 Hz is achievable. Further reduction in average power can be realized with lower sample rates.

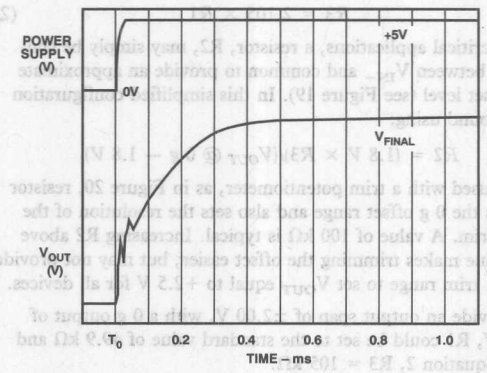

Figure 21. Power-On Settling Time when Power Cycling

SYSTEM BANDWIDTH CONTROL AND POST FILTERING

Unlike piezoresistive sensors, the resonant frequency of the ADXL50's capacitive sensor element is typically greater than 20 kHz and does not limit the useful bandwidth of the device. Usually, the resonant frequency of the beam appears as a peak in the bandwidth response at approximately 24 kHz with a Q of 3 to 4, as shown in Figure 22.

When using the recommended 0.022 μF demodulator capacitor, be advised that the nominal 1300 Hz pole it establishes within the device can vary ±40%. Therefore, if additional low-pass filtering is used—at frequencies much above 600 Hz—the two poles may interact and result in a net circuit bandwidth that is lower than expected.

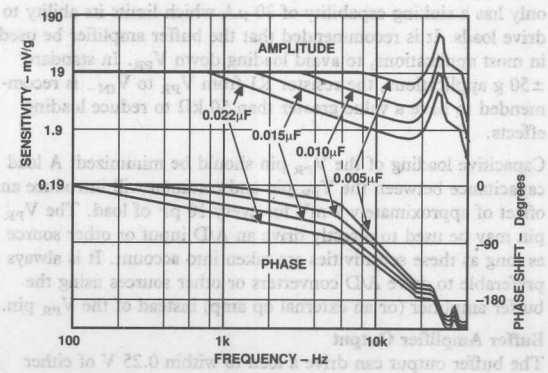

Figure 22. Frequency Response of the ADXL50 for Various Demodulator Capacitors

RECOMMENDED COMPONENT VALUES FOR VARIOUS FULL SCALE RANGES AND A 300Hz BANDWIDTH

FULL SCALE	mV per g	3dB BW (Hz)	R1a kΩ	R1b kΩ	R3 kΩ	R2 kΩ	C4 µF
±10 g	200	300	5	21.5	249	100	0.0022
±20 g	100	300	5	23.7	137	100	0.0039
±40 g	50	300	10	34	105	100	0.0056
±50 g	40	300	10	45.3	105	100	0.0056

$$3dB\ BW = \frac{1}{2\pi\ R3\ C4}$$

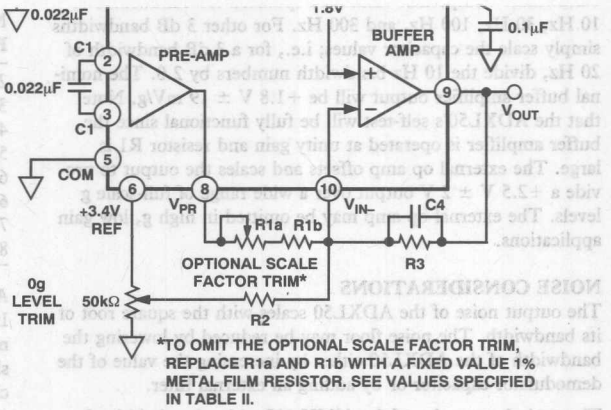

Figure 23. Using the Buffer Amplifier to Provide One Pole Post Filtering Plus Scale Factor and 0 g Level Trimming

ONE POLE POST FILTERING

Figure 23 shows the ADXL50 buffer amplifier connected to provide one pole post filtering, 0 g offset trimming, and output scaling. The table included with the figure lists practical component values for various full-scale g levels and approximate circuit bandwidths. For bandwidths other than those listed, use the formula:

$$Capacitor\ C4\ in\ Farads = 1/(2\ \pi \times R3\ in\ Ohms \times 3\ dB\ BW\ in\ Hertz)$$

or simply scale the value of capacitor C4 accordingly; i.e., for a ±20 g application with a 50 Hz bandwidth, the value of C4 will need to be twice as large as its 100 Hz value or 0.012 µF × 2 = 0.024 µF. The closest standard value of 0.022 µF should then be used.

TWO POLE POST FILTERING

Figure 24 shows a circuit which uses the ADXL50's buffer amplifier to provide two pole post filtering. An AD820 external op amp allows noninteractive adjustment of 0 g offset and scale factor. Component values for the two pole filter were selected to operate the buffer at unity gain with a Q of one.

2 POLE FILTER COMPONENT VALUES

3dB BW(Hz)	C3µF	C4µF
300	0.027	0.0033
100	0.082	0.01
30	0.27	0.033
10	0.82	0.1

OFFSET & SCALING AMPLIFIER COMPONENT VALUES

FULL SCALE	mV per g	GAIN	R4a kΩ	R4b kΩ	R5 kΩ
±10 g	200	10.53	5	21.5	249
±20 g	100	5.26	5	23.7	137
±40 g	50	2.63	10	34	105
±50 g	40	2.11	10	45.3	105

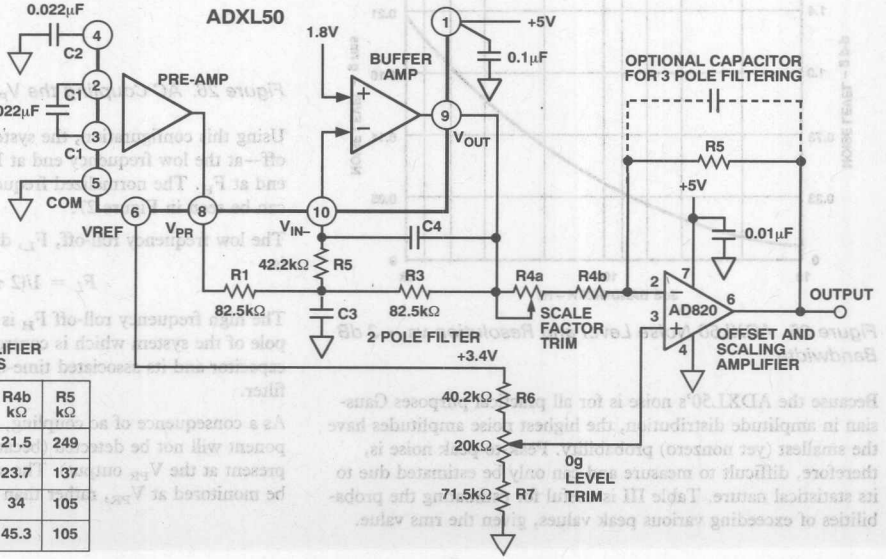

Figure 24. Circuit Providing Two Pole Post Filtering and 0 g Offset and Scale Factor Trimming

Capacitors C3 and C4 are chosen to provide the desired 3 dB bandwidth. Component values are specified for bandwidths of 10 Hz, 30 Hz, 100 Hz, and 300 Hz. For other 3 dB bandwidths simply scale the capacitor values; i.e., for a 3 dB bandwidth of 20 Hz, divide the 10 Hz bandwidth numbers by 2.0. The nominal buffer amplifier output will be +1.8 V ± 19 mV/g. Note that the ADXL50's self-test will be fully functional since the buffer amplifier is operated at unity gain and resistor R1 is large. The external op amp offsets and scales the output to provide a +2.5 V ± 2 V output over a wide range of full-scale g levels. The external op amp may be omitted in high g, low gain applications.

NOISE CONSIDERATIONS

The output noise of the ADXL50 scales with the square root of its bandwidth. The noise floor may be reduced by lowering the bandwidth of the ADXL50 either by increasing the value of the demodulator capacitor or by adding an external filter.

The typical rms noise of the ADXL50J with a bandwidth of 100 Hz and a noise density of 125 $\mu V/\sqrt{Hz}$ is estimated as follows:

$$Noise\ (rms) = (125\ \mu V/\sqrt{Hz}) \sqrt{100} = 1.25\ mV\ rms$$

Peak-to-peak noise may be estimated with the following equation:

$$Noise\ p\text{-}p = (6.6)\ Noise\ rms$$

Peak-to-peak noise is thus estimated at 8.25 mV or approximately 0.4 g p-p. The ADXL50 noise is characteristic of white noise. Typical rms and p-p noise for various 3 dB bandwidths is estimated in Figure 25.

Figure 25. ADXL50 Noise Level and Resolution vs. –3 dB Bandwidth

Because the ADXL50's noise is for all practical purposes Gaussian in amplitude distribution, the highest noise amplitudes have the smallest (yet nonzero) probability. Peak-to-peak noise is, therefore, difficult to measure and can only be estimated due to its statistical nature. Table III is useful for estimating the probabilities of exceeding various peak values, given the rms value.

Table III.

Nominal Peak-to-Peak Value	% of Time that Noise will Exceed Nominal Peak-to-Peak Value
2.0 × rms	32%
3.0 × rms	13%
4.0 × rms	4.6%
5.0 × rms	1.2%
6.0 × rms	0.27%
6.6 × rms	**0.1%**
7.0 × rms	0.046%
8.0 × rms	0.006%

AC COUPLING V_{PR} TO BUFFER INPUT

If a dc response is not required, as in applications such as motion detection or vibration measurement, then ac coupling should be considered. In low g applications, the output voltage change due to acceleration is small compared to the 0 g offset voltage drift. Because ac coupling removes the dc component of the output, the preamp output signal may be amplified considerably without increasing the 0 g level drift. The most effective way to ac couple the ADXL50 is between the preamp output at V_{PR} and the buffer input, V_{IN-}, as shown in Figure 26.

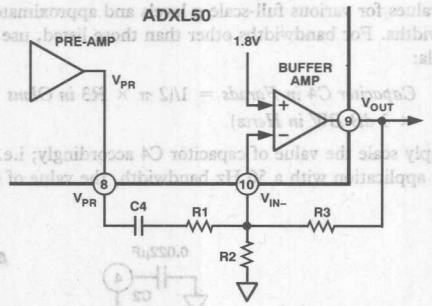

Figure 26. AC Coupling the V_{PR} Output to the Buffer Input

Using this configuration, the system's ac response is now rolled off—at the low frequency end at F_L, and at the high frequency end at F_H. The normalized frequency response of the system can be seen in Figure 27.

The low frequency roll-off, F_L, due to the ac coupling network is:

$$F_L = 1/(2\ \pi\ R1\ C4)$$

The high frequency roll-off F_H is determined by the dominant pole of the system which is controlled by either the demodulator capacitor and its associated time-constant or by a dominant post filter.

As a consequence of ac coupling, any constant acceleration component will not be detected (because this too is a dc voltage present at the V_{PR} output). The self-test feature, if used, must be monitored at V_{PR}, rather than at the buffer output.

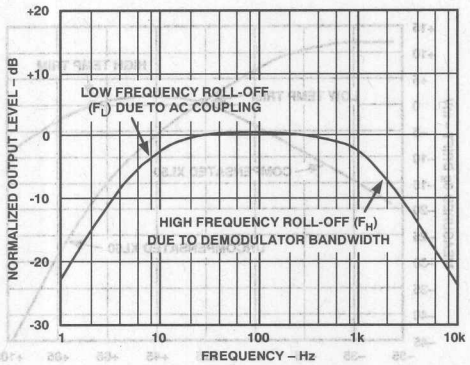

Figure 27. Normalized Output Level vs. Frequency for a Typical Application Using AC Coupling Between V_{PR} and Buffer Amplifier

MINIMIZING EMI/RFI

The architecture of the ADXL50 and its use of synchronous demodulation make the device immune to most electro-magnetic (EMI) and radio frequency (RFI) interference. The use of synchronous demodulation allows the circuit to reject all signals except those at the frequency of the oscillator driving the sensor element. However, the ADXL50 does have a sensitivity to RFI that is within ±5 kHz of the internal oscillator's nominal frequency of 1 MHz. The internal oscillator frequency will exhibit part to part variation in the range of 0.6 MHz to 1.4 MHz.

In general the effect is difficult to notice as the interference must match the internal oscillator within ±5 kHz and must be large in amplitude. For example: a 1 MHz interference signal of 20 mV p-p applied to the +5 V power supply pin will produce a 200 mV p-p signal at the V_{PR} pin if the internal oscillator and interference signals are matched exactly. If the same 20 mV interference is applied but 5 kHz above or below the internal oscillator's frequency, the signal level at V_{PR} will only be 20 mV p-p in amplitude.

Power supply decoupling, short component leads (especially for capacitors C1 and C2), physically small (surface mount, etc.) components and attention to good grounding practices all help to prevent RFI and EMI problems. Please consult the factory for applications assistance in instances where this may be of concern.

SELF-CALIBRATING THE ADXL50

If a calibrated shaker is not available, both the 0 g level and scale factor of the ADXL50 may be easily set to fair accuracy by using a self-calibration technique based on the 1 g (average) acceleration of the earth's gravity. Figure 28 shows how gravity and package orientation affect the ADXL50's output (TO-100 package shown). Note that the output polarity is that which appears at V_{PR}; the output at V_{OUT} will have the opposite sign. With its axis of sensitivity in the vertical plane, the ADXL50 should register a 1 g acceleration, either positive or negative, depending on orientation. With the axis of sensitivity in the horizontal plane, no acceleration (0 g) should be indicated.

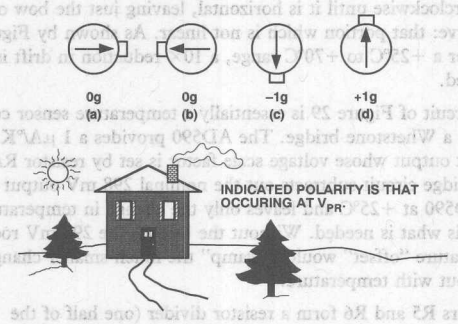

Figure 28. Using the Earth's Gravity to Self-Calibrate the ADXL50

To self-calibrate the ADXL50, place the accelerometer on its side with its axis of sensitivity oriented as shown in "a." The 0 g offset potentiometer, Rt, is then roughly adjusted for midscale: +2.5 V at the buffer output. If the optional scale factor trimming is to be used, it should be adjusted next.

Next, the package axis should be oriented as in "c" (pointing down) and the output reading noted. The package axis should then be rotated 180° to position "d" and the scale factor potentiometer, R1a, adjusted so that the output voltage indicates a change of 2 g's in acceleration. For example, if the circuit scale factor at the buffer output is 100 mV per g, then the scale factor trim should be adjusted so that an output change of 200 mV is indicated.

Adjusting the circuit's scale factor will have some effect on its 0 g level so this should be readjusted, as before, but this time checked in both positions "a" and "b." If there is a difference in the 0 g reading, a compromise setting should be selected so that the reading in each direction is equidistant from +2.5 V. Scale factor and 0 g offset adjustments should be repeated until both are correct. Temporarily placing a capacitor across the buffer amplifier's feedback resistor will reduce output noise and so aid in trimming the device. Note that, for high full-scale g ranges, ±2 g may be a very small fraction of the full-scale range and device nonlinearity will, therefore, affect the circuit's high g level accuracy.

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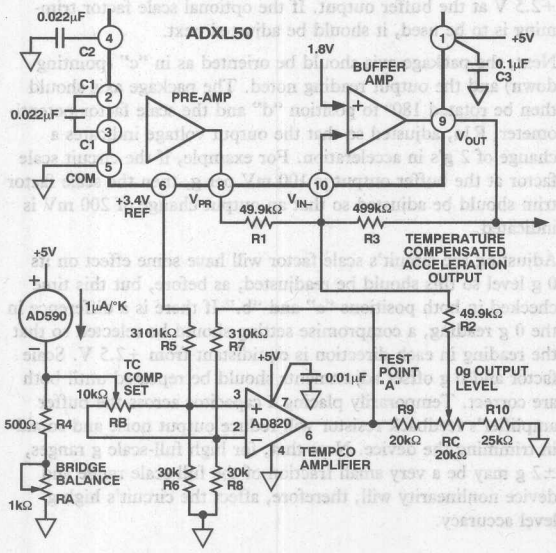
Compensating for the 0 g Drift of the ADXL50 Accelerometer

The circuit of Figure 29 provides a linear temperature compensation for the ADXL50. Figure 30 shows the 0 g drift over temperature for a typical ADXL50 with and without this circuit. As shown by Figure 30, the linear portion of the drift curve has been subtracted out. In effect, the curve has been rotated counterclockwise until it is horizontal, leaving just the bow of the curve: that portion which is not linear. As shown by Figure 30, over a +25°C to +70°C range, a 10× reduction in drift is achieved.

The circuit of Figure 29 is essentially a temperature sensor coupled to a Whetstone bridge. The AD590 provides a 1 μA/°K current output whose voltage scale factor is set by resistor RA. The bridge circuit subtracts out the nominal 298 mV output of the AD590 at +25°C and leaves only the change in temperature, which is what is needed. Without the bridge, the 298 mV room temperature "offset" would "swamp" the much smaller change in output with temperature.

Resistors R5 and R6 form a resistor divider (one half of the bridge) which divides down the +3.4 V reference output of the ADXL50 to 0.3 V which appears at the noninverting input of the AD820 op amp. Resistors R7 and R8 form the other half of the bridge, and because they have the same ratio as R5 and R6, the op amp will have a +3.4 V output at room temperature.



CALIBRATION PROCEEDURE:
AT T_{MIN} OR LOWER TEMP CAL POINT...

1. SET RB ALL THE WAY TO ONE SIDE.
2. ADJUST RA FOR +3.4V AT TEST POINT "A."
3. SET RC FOR +2.5V V_{OUT} (AT PIN 9 OF ADXL50).
4. TEMPORARILY CONNECT A 1.5kΩ RESISTOR BETWEEN THE CENTER OF RB AND GROUND.
5. ADJUST RB FOR +2.5V AT V_{OUT}.
6. REMOVE THE 1.5kΩ RESISTOR. V_{OUT} SHOULD NOT CHANGE.
7. GO TO T_{MAX} OR HIGH TEMP CAL POINT.
8. READJUST RB FOR +2.5V.
9. CALIBRATION COMPLETE.

Figure 29. ADXL50 0 g Drift Compensation Circuit

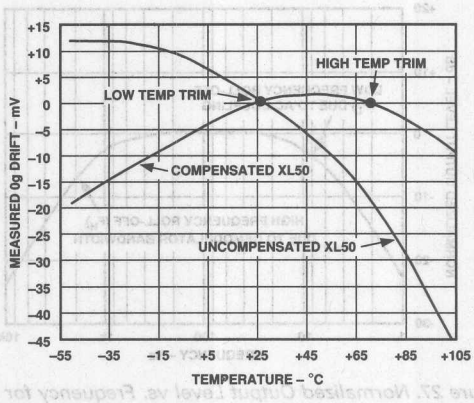


Figure 30. ADXL50 0 g Drift With and Without the Compensation Circuit of Figure 29

ADXL50 Applications Literature Available

Contact the Analog Devices Literature Center.

1. *Using the ADXL50 Accelerometer in Low g Applications* (AN-374)
   Application note covering resolution issues, bandwidth limiting, ac coupling issues, oversampling and other noise reduction techniques, gain selection issues, offset drift considerations, plus low g circuits and tables.
2. *Using the ADXL50EM Accelerometer Evaluation Module* (AN-376)
   Application note covering mounting and resonance issues, effects of potting the module cavity, typical frequency response curves.
3. *Reducing the Average Power Consumption of the ADXL50* (AN-378)
   How to power cycle the ADXL50 to dramatically reduce the standby current of the device for longer battery life.
4. *Mounting Considerations for the ADXL50* (AN-379)
   An overview of accelerometer mounting and resonance issues.
5. *Increasing the Frequency Response of the ADXL50* (AN-377)
   How to extend the high frequency response of the ADXL50 by decreasing the value of compensation capacitor.
6. *Compensating for the ADXL50 0 g Drift* (AN-380)
   Practical hardware and software corrections to compensate for the 0 g bias level drift over temperature.

Monolithic Accelerometer with Signal Conditioning

ADXL181*

FEATURES

Complete Acceleration Measurement System on a Single Monolithic IC
Full-Scale Measurement Range:
+5 V Supply: –125 g, +250 g
+12 V Supply: –150 g, +880 g
Self-Test on Digital Command
Single Supply Operation
Sensitivity Precalibrated to 8 mV/g
Internal Buffer Amplifier for User Adjustable Sensitivity and Zero-g Level
Frequency Response: DC to 3 kHz
Post Filtering with External Passive Components
High Shock Survival: >2000 g Unpowered
Other Products Available Providing Different Sensitivities and Full-Scale Ranges

GENERAL DESCRIPTION

The ADXL181 is a complete acceleration measurement system on a single monolithic IC, using a surface micromachined capacitive measurement method. The analog output voltage is directly proportional to acceleration and is fully scaled, referenced, and temperature compensated, resulting in high accuracy and linearity over a wide temperature range. Internal circuitry implements a force-balance control loop that compensates for any mechanical sensor variations.

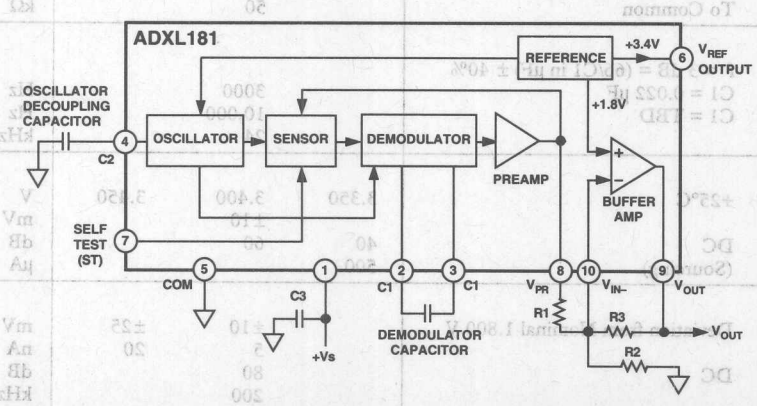
A TTL compatible self-test feature can electrostatically deflect the sensor beam at any time to verify device functionality.

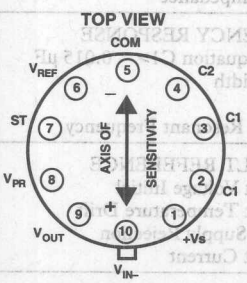
An internal buffer amplifier has a 0.25 V to V_S – 0.25 V output range. This may be used to gain and offset adjust the output signal so that it has a symmetrical output range. The amplifier can also be used to gain adjust and filter the sensor output. No external active components are necessary to connect the output signal directly to an analog-to-digital converter or microcontroller.

The ADXL181 is packaged in a hermetic 10-pin TO-100 metal can. Contact factory for availability of devices with specific temperature ranges and performance.

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM AND PINOUT





10-PIN TO-100 HEADER PACKAGE

NOTE:
AXIS OF SENSITIVITY IS IN PLANE OF PIN 5 TO TAB.

*Patent pending.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SENSITIVITY				
+25°C		8		mV/g
Temperature Drift		±0.75		% of Reading
ZERO g BIAS LEVEL				
+25°C		8		V
T_{MIN}–T_{MAX}				V
Temperature Drift		±75		mV
VOLTAGE NOISE DENSITY		65		$\mu V/\sqrt{Hz}$
SENSOR INPUT				
FS Measurement Range[1]	–125		+250	g
Nonlinearity		0.2		% of FS
Alignment Error		±1		Degrees
Transverse Sensitivity		±2		%

NOTES
[1]Accelerations up to –150 g, +880 g using a +12 V Supply.
Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_S = +5$ V ± 5% @ Acceleration = 0 g, and C1 = C2 = 0.022 µF unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
PREAMPLIFIER OUTPUT					
Power Supply Rejection	DC	30	40		dB
Voltage Swing	+25°C	0.25		V_S – 0.25	V
Current Output	Source or Sink	30	80		µA
Capacitive Load Drive			100		pF
SELF-TEST INPUT					
Output Change at V_{PR}					
ST Pin from Logic "0" to "1"		–0.80	–0.90	–1.00	V
Logic "1" Voltage		2.0			V
Logic "0" Voltage				0.8	V
Input Impedance	To Common		50		kΩ
FREQUENCY RESPONSE					
3 dB Equation C1> = 0.015 µF	f = 3 dB = (66/C1 in µF) ± 40%				
Bandwidth	C1 = 0.022 µF		3000		Hz
	C1 = TBD		10,000		Hz
Sensor Resonant Frequency			24		kHz
+3.4 VOLT REFERENCE					
Output Voltage Initial	+25°C	3.350	3.400	3.450	V
Output Temperature Drift			±10		mV
Power Supply Rejection	DC	40	60		dB
Output Current	(Sourcing)	500			µA
BUFFER AMPLIFIER					
Input Offset Voltage	Deviation from Nominal 1.800 V		±10	±25	mV
Input Bias Current			5	20	nA
Open Loop Gain	DC		80		dB
Unity Gain Bandwidth			200		kHz
Output Voltage Swing	I_{OUT} = 100 µA	0.25		V_S – 0.25	V
Capacitive Load Drive		1000			pF
POWER SUPPLY					
Specified Performance	5 V Supply	+4.75		+5.25	V
	12 V Supply	+11.6		+12.6	V
Quiescent Supply Current	5 V Supply		11	14	mA
TEMPERATURE RANGE		–55		+125	°C

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Low Power, Programmable Temperature Controller

TMP01*

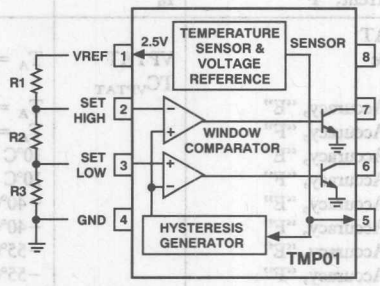
FEATURES

−55°C to +125°C (−67°F to +257°F) Operation
±0.5°C Accuracy Over Temperature (typ)
Temperature-Proportional Voltage Output
User Programmable Temperature Trip Points
User Programmable Hysteresis
20 mA Open Collector Trip Point Outputs
TTL/CMOS Compatible
Single-Supply Operation (4.5 V to 13.2 V)
Low Cost 8-Pin DIP and SO Packages

APPLICATIONS

Over/Under Temperature Sensor and Alarm
Board Level Temperature Sensing
Temperature Controllers
Electronic Thermostats
Thermal Protection
HVAC Systems
Industrial Process Control
Remote Sensors

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The TMP01 is a temperature sensor which generates a voltage output proportional to absolute temperature and a control signal from one of two outputs when the device is either above or below a specific temperature range. Both the high/low temperature trip points and hysteresis (overshoot) band are determined by user-selected external resistors. For high volume production, these resistors are available on-board.

The TMP01 consists of a bandgap voltage reference combined with a pair of matched comparators. The reference provides both a constant 2.5 V output and a voltage proportional to absolute temperature (VPTAT) which has a precise temperature coefficient of 5 mV/K and is 1.49 V (nominal) at +25°C. The comparators compare VPTAT with the externally set temperature trip points and generate an open-collector output signal when one of their respective thresholds has been exceeded.

*Protected by U.S. Patent No. 5,195,827.

Hysteresis is also programmed by the external resistor chain and is determined by the total current drawn out of the 2.5 V reference. This current is mirrored and used to generate a hysteresis offset voltage of the appropriate polarity after a comparator has been tripped. The comparators are connected in parallel, which guarantees that there is no hysteresis overlap and eliminates erratic transitions between adjacent trip zones.

The TMP01 utilizes proprietary thin film resistors in conjunction with production laser trimming to maintain a temperature accuracy of ±2°C (typ) over the rated temperature range, with excellent linearity. The open-collector outputs are capable of sinking 20 mA, enabling the TMP01 to drive control relays directly. Operating from a +5 V supply, quiescent current is only 500 μA (max).

The TMP01 is available in the low cost 8-pin epoxy mini-DIP and SO (small outline) packages, and in die form.

TMP01P/S—SPECIFICATIONS

Plastic DIP and Surface Mount Packages (V+ = +5 V, GND = 0 V, −40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUTS SET HIGH, SET LOW						
Offset Voltage	V_{OS}			0.25		mV
Offset Voltage Drift	TCV_{OS}			3		µV/°C
Input Bias Current, "E"	I_B			25	50	nA
Input Bias Current, "F"	I_B			25	100	nA
OUTPUT VPTAT[1]						
Output Voltage	VPTAT	T_A = +25°C, No Load		1.49		V
Scale Factor	TC_{VPTAT}			5		mV/K
Temperature Accuracy, "E"		T_A = +25°C, No Load	−1.5	±0.5	1.5	°C
Temperature Accuracy, "F"		T_A = +25°C, No Load	−3	±1.0	3	°C
Temperature Accuracy, "E"		10°C < T_A < 40°C, No Load		±0.75		°C
Temperature Accuracy, "F"		10°C < T_A < 40°C, No Load		±1.5		°C
Temperature Accuracy, "E"		−40°C < T_A < 85°C, No Load	−3.0	±1	3.0	°C
Temperature Accuracy, "F"		−40°C < T_A < 85°C, No Load	−5.0	±2	5.0	°C
Temperature Accuracy, "E"		−55°C < T_A < 125°C, No Load		±1.5		°C
Temperature Accuracy, "F"		−55°C < T_A < 125°C, No Load		±2.5		°C
Repeatability Error	ΔVPTAT	Note 4		0.25		Degree
Long Term Drift Error		Notes 2 and 6		0.25	0.5	Degree
Power Supply Rejection Ratio	PSRR	T_A = +25°C, 4.5 V ≤ V+ ≤ 13.2 V		±0.02	±0.1	%/V
OUTPUT VREF						
Output Voltage, "E"	VREF	T_A = +25°C, No Load	2.495	2.500	2.505	V
Output Voltage, "F"	VREF	T_A = +25°C, No Load	2.490	2.500	2.510	V
Output Voltage, "E"	VREF	−40°C < T_A < 85°C, No Load	2.490	2.500	2.510	V
Output Voltage, "F"	VREF	−40°C < T_A < 85°C, No Load	2.485	2.500	2.515	V
Output Voltage, "E"	VREF	−55°C < T_A < 125°C, No Load		2.5 ± 0.01		V
Output Voltage, "F"	VREF	−55°C < T_A < 125°C, No Load		2.5 ± 0.015		V
Drift	TC_{VREF}			−10		ppm/°C
Line Regulation		4.5 V ≤ V+ ≤ 13.2 V		±0.01	±0.05	%/V
Load Regulation		10 µA ≤ I_{VREF} ≤ 500 µA		±0.1	±0.25	%/mA
Output Current, Zero Hysteresis	I_{VREF}			7		µA
Hysteresis Current Scale Factor	SF_{HYS}	(Note 1)		5.0		µA/°C
Turn-On Settling Time		To Rated Accuracy		25		µs
OPEN-COLLECTOR OUTPUTS OVER, UNDER						
Output Low Voltage	V_{OL}	I_{SINK} = 1.6 mA		0.25	0.4	V
Output Low Voltage	V_{OL}	I_{SINK} = 20 mA		0.6		V
Output Leakage Current	I_{OH}	V+ = 12 V		1	100	µA
Fall Time	t_{HL}	See Test Load		40		ns
POWER SUPPLY						
Supply Range	V+		4.5		13.2	V
Supply Current	I_{SY}	Unloaded, +V = 5 V		400	500	µA
Supply Current	I_{SY}	Unloaded, +V = 13.2 V		450	800	µA
Power Dissipation	P_{DISS}	+V = 5 V		2.0	2.5	mW

NOTES

[1]K = °C + 273.15.

[2]Guaranteed but not tested.

[3]Does not consider errors caused by heating due to dissipation of output load currents.

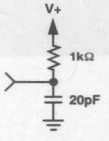
[4]Maximum deviation between +25°C readings after temperature cycling between −55°C and +125°C.

[5]Typical values indicate performance measured at T_A = +25°C.

[6]Observed in a group sample over an accelerated life test of 500 hours at 150°C.

Specifications subject to change without notice.

Test Load



TMP01J—SPECIFICATIONS

TO-99 Metal Can Package (V+ = +5 V, GND = 0 V, −40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUTS SET HIGH, SET LOW						
Offset Voltage	V_{OS}			0.25		mV
Offset Voltage Drift	TCV_{OS}			3		µV/°C
Input Bias Current, "F"	I_B			25	100	nA
OUTPUT VPTAT[1]						
Output Voltage	VPTAT	T_A = +25°C, No Load		1.49		V
Scale Factor	TC_{VPTAT}			5		mV/K
Temperature Accuracy, "F"		T_A = +25°C, No Load	−3	±1.0	3	°C
Temperature Accuracy, "F"		10°C < T_A < 40°C, No Load		±1.5		°C
Temperature Accuracy, "F"		−40°C < T_A < 85°C, No Load	−5.0	±2	5.0	°C
Temperature Accuracy, "F"		−55°C < T_A < 125°C, No Load		±2.5		°C
Repeatability Error	ΔVPTAT	Note 4		0.25		Degree
Long Term Drift Error		Notes 2 and 6		0.25	0.5	Degree
Power Supply Rejection Ratio	PSRR	T_A = +25°C, 4.5 V ≤ V+ ≤ 13.2 V		±0.02	±0.1	%/V
OUTPUT VREF						
Output Voltage, "F"	VREF	T_A = +25°C, No Load	2.490	2.500	2.510	V
Output Voltage, "F"	VREF	−40°C < T_A < 85°C, No Load	2.480	2.500	2.520	V
Output Voltage, "F"	VREF	−55°C < T_A < 125°C, No Load		2.5 ± 0.015		V
Drift	TC_{VREF}			−10		ppm/°C
Line Regulation		4.5 V ≤ V+ ≤ 13.2 V		±0.01	±0.05	%/V
Load Regulation		10 µA ≤ I_{VREF} ≤ 500 µA		±0.1	±0.25	%/mA
Output Current, Zero Hysteresis	I_{VREF}			7		µA
Hysteresis Current Scale Factor	SF_{HYS}	(Note 1)		5.0		µA/°C
Turn-On Settling Time		To Rated Accuracy		25		µs
OPEN-COLLECTOR OUTPUTS OVER, UNDER						
Output Low Voltage	V_{OL}	I_{SINK} = 1.6 mA		0.25	0.4	V
Output Low Voltage	V_{OL}	I_{SINK} = 20 mA		0.6		V
Output Leakage Current	I_{OH}	V+ = 12 V		1	100	µA
Fall Time	t_{HL}	See Test Load, Note 2		40		ns
POWER SUPPLY						
Supply Range	V+		4.5		13.2	V
Supply Current	I_{SY}	Unloaded, +V = 5 V		400	500	µA
Supply Current	I_{SY}	Unloaded, +V = 13.2 V		450	800	µA
Power Dissipation	P_{DISS}	+V = 5 V		2.0	2.5	mW

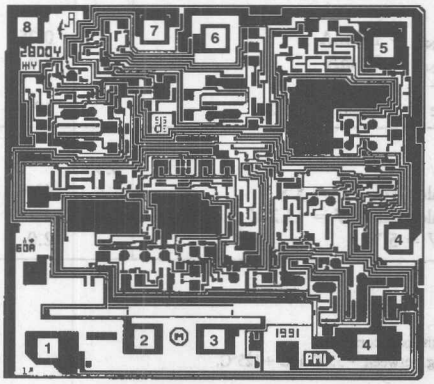
NOTES
[1]K = °C + 273.15.
[2]Guaranteed but not tested.
[3]Does not consider errors caused by heating due to dissipation of output load currents.
[4]Maximum deviation between +25°C readings after temperature cycling between −55°C and +125°C.
[5]Typical values indicate performance measured at T_A = +25°C.
[6]Observed in a group sample over an accelerated life test of 500 hours at 150°C.
Specifications subject to change without notice.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUTS SET HIGH, SET LOW						
Input Bias Current	I_B				100	nA
OUTPUT VPTAT						
Temperature Accuracy		T_A = +25°C, No Load			1.5	°C
OUTPUT VREF						
Nominal Value	VREF	T_A = +25°C, No Load	2.490		2.510	V
Line Regulation		4.5 V ≤ V+ ≤ 13.2 V			±0.05	%/V
Load Regulation		10 µA ≤ I_{VREF} ≤ 500 µA			±0.25	%/mA
OPEN-COLLECTOR OUTPUTS OVER, UNDER						
Output Low Voltage	V_{OL}	I_{SINK} = 1.6 mA			0.4	mV
Output Low Voltage	V_{OL}	I_{SINK} = 20 mA			1.0	V
Output Leakage Current	I_{OH}				100	µA
POWER SUPPLY						
Supply Range	V+		4.5		13.2	V
Supply Current	I_{SY}	Unloaded			600	µA

NOTES
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

DICE CHARACTERISTICS

Die Size 0.078 × 0.071 inch, 5,538 sq. mils
(1.98 × 1.80 mm, 3.57 sq. mm)
Transistor Count: 105



1. VREF
2. SETHIGH
3. SETLOW
4. GND (TWO PLACES)
(CONNECTED TO SUBSTRATE)
5. VPTAT
6. UNDER
7. OVER
8. V+

For additional DICE ordering information, refer to databook.

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage . . . . . −0.3 V to +15 V
Maximum Input Voltage
(SETHIGH, SETLOW) . . . . . −0.3 V to [(V+) +0.3 V]
Maximum Output Current (VREF, VPTAT) . . . . . 2 mA
Maximum Output Current (Open Collector Outputs) . . 50 mA
Maximum Output Voltage (Open Collector Outputs) . . . . 15 V
Operating Temperature Range . . . . . −55°C to +150°C
Dice Junction Temperature . . . . . +150°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}	θ_{JC}	Units
8-Pin Plastic DIP (P)	103[1]	43	°C/W
8-Lead SOIC (S)	158[2]	43	°C/W
8-Lead TO-99 Can (J)	150[1]	18	°C/W

NOTES
[1]θ_{JA} is specified for device in socket (worst case conditions).
[2]θ_{JA} is specified for device mounted on PCB.

CAUTION

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected, however, permanent damage may occur on unprotected units from high energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures.
3. Remove power before inserting or removing units from their sockets.

ORDERING GUIDE

Model/Grade	Temperature Range[1]	Package Description	Package Option[2]
TMP01EP	XIND	Plastic DIP	N-8
TMP01FP	XIND	Plastic DIP	N-8
TMP01ES	XIND	SOIC	SO-8
TMP01FS	XIND	SOIC	SO-8
TMP01FJ[3]	XIND	TO-99 Can	H-08A
TMP01GBC	25°C	Die	

NOTES
[1]XIND = −40°C to +85°C.
[2]For outline information see Package Information section.
[3]Consult factory for availability of MIL/883 version in TO-99 can.

GENERAL DESCRIPTION

The TMP01 is a very linear voltage-output temperature sensor, with a window comparator that can be programmed by the user to activate one of two open-collector outputs when a predetermined temperature setpoint voltage has been exceeded. A low drift voltage reference is available for setpoint programming.

The temperature sensor is basically a very accurately temperature-compensated, bandgap-type voltage reference with a buffered output voltage proportional to absolute temperature (VPTAT), accurately trimmed to a scale factor of 5 mV/K. See the applications information following.

The low drift 2.5 V reference output VREF is easily divided externally with fixed resistors or potentiometers to accurately establish the programmed heat/cool setpoints, independent of temperature. Alternatively, the setpoint voltages can be supplied by other ground-referenced voltage sources such as user-programmed DACs or controllers. The high and low setpoint voltages are compared to the temperature sensor voltage, thus creating a two-temperature thermostat function. In addition, the total output current of the reference (I_{VREF}) determines the magnitude of the temperature hysteresis band. The open-collector outputs of the comparators can be used to control a wide variety of devices.

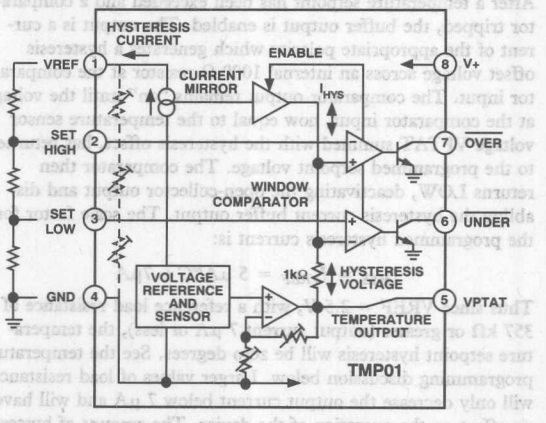


Figure 1. Detailed Block Diagram

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Temperature Hysteresis

The temperature hysteresis is the number of degrees beyond the original setpoint temperature that must be sensed by the TMP01 before the setpoint comparator will be reset and the output disabled. Figure 2 shows the hysteresis profile. The hysteresis is programmed by the user by setting a specific load on the reference voltage output VREF. This output current I_{VREF} is also called the hysteresis current, which is mirrored internally and fed to a buffer with an analog switch.

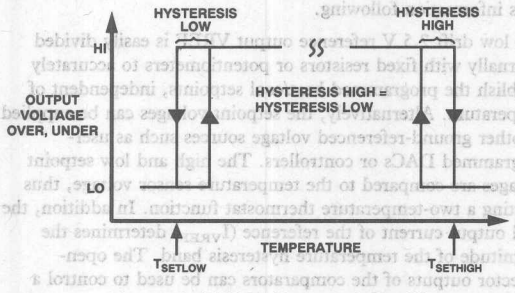

Figure 2. TMP01 Hysteresis Profile

After a temperature setpoint has been exceeded and a comparator tripped, the buffer output is enabled. The output is a current of the appropriate polarity which generates a hysteresis offset voltage across an internal 1000 Ω resistor at the comparator input. The comparator output remains "on" until the voltage at the comparator input, now equal to the temperature sensor voltage VPTAT summed with the hysteresis offset, has returned to the programmed setpoint voltage. The comparator then returns LOW, deactivating the open-collector output and disabling the hysteresis current buffer output. The scale factor for the programmed hysteresis current is:

$$I_{HYS} = I_{VREF} = 5\ \mu A/°C + 7\mu A$$

Thus since VREF = 2.5 V, with a reference load resistance of 357 kΩ or greater (output current 7 μA or less), the temperature setpoint hysteresis will be zero degrees. See the temperature programming discussion below. Larger values of load resistance will only decrease the output current below 7 μA and will have no effect on the operation of the device. The amount of hysteresis is determined by selecting a value of load resistance for VREF, as shown below.

Programming the TMP01

In the basic fixed-setpoint application utilizing a simple resistor ladder voltage divider, the desired temperature setpoints are programmed in the following sequence:

1. Select the desired hysteresis temperature.
2. Calculate the hysteresis current I_{VREF}.
3 Select the desired setpoint temperatures.
4. Calculate the individual resistor divider ladder values needed to develop the desired comparator setpoint voltages at SETHIGH and SETLOW.

The hysteresis current is readily calculated, as shown above. For example, for 2 degrees of hysteresis, I_{VREF} = 17 μA. Next, the setpoint voltages $V_{SETHIGH}$ and V_{SETLOW} are determined using the VPTAT scale factor of 5 mV/K = 5 mV/(°C + 273.15), which is 1.49 V for +25°C. We then calculate the divider resistors, based on those setpoints. The equations used to calculate the resistors are:

$$V_{SETHIGH} = (T_{SETHIGH} + 273.15)(5\ mV/°C)$$

$$V_{SETLOW} = (T_{SETLOW} + 273.15)(5\ mV/°C)$$

$$R1\ (k\Omega) = (V_{VREF} - V_{SETHIGH})/I_{VREF} = (2.5\ V - V_{SETHIGH})/I_{VREF}$$

$$R2\ (k\Omega) = (V_{SETHIGH} - V_{SETLOW})/I_{VREF}$$

$$R3\ (k\Omega) = V_{SETLOW}/I_{VREF}$$

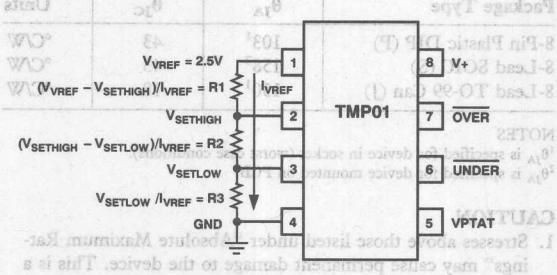

Figure 3. TMP01 Setpoint Programming

The total R1 + R2 + R3 is equal to the load resistance needed to draw the desired hysteresis current from the reference, or I_{VREF}.

The formulas shown above are also helpful in understanding the calculation of temperature setpoint voltages in circuits other than the standard two-temperature thermostat. If a setpoint function is not needed, the appropriate comparator should be disabled. SETHIGH can be disabled by tying it to V+, SETLOW by tying it to GND. Either output can be left unconnected.

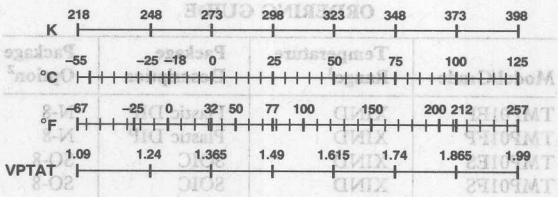

Figure 4. Temperature–VPTAT Scale

Understanding Error Sources

The accuracy of the VPTAT sensor output is well characterized and specified, however preserving this accuracy in a heating or cooling control system requires some attention to minimizing the various potential error sources. The internal sources of setpoint programming error include the initial tolerances and temperature drifts of the reference voltage VREF, the setpoint comparator input offset voltage and bias current, and the hysteresis current scale factor. When evaluating setpoint programming errors, remember that any VREF error contribution at the comparator inputs is reduced by the resistor divider ratios. The comparator input bias current (inputs SETHIGH, SETLOW) drops to less than 1 nA (typ) when the comparator is tripped. This can account for some setpoint voltage error, equal to the change in bias current times the effective setpoint divider ladder resistance to ground.

The thermal mass of the TMP01 package and the degree of thermal coupling to the surrounding circuitry are the largest factors in determining the rate of thermal settling, which ultimately determines the rate at which the desired temperature measurement accuracy may be reached. Thus, one must allow sufficient time for the device to reach the final temperature. The typical thermal time constant for the plastic package is approximately 140 seconds in still air! Therefore, to reach the final temperature accuracy within 1%, for a temperature change of 60 degrees, a settling time of 5 time constants, or 12 minutes, is necessary.

The setpoint comparator input offset voltage and zero hysteresis current affect setpoint error. While the 7 μA zero hysteresis current allows the user to program the TMP01 with moderate resistor divider values, it does vary somewhat from device to device, causing slight variations in the actual hysteresis obtained in practice. Comparator input offset directly impacts the programmed setpoint voltage and thus the resulting hysteresis band, and must be included in error calculations.

External error sources to consider are the accuracy of the external programming resistors, grounding error voltages, comparator input noise, comparator input bias current, and the overall problem of thermal gradients. The accuracy of the external programming resistors directly impacts the resulting setpoint accuracy. Thus in fixed-temperature applications the user should select resistor tolerances appropriate to the desired programming accuracy. Resistor temperature drift must be taken into account also. This effect can be minimized by selecting good quality components, and by keeping all components in close thermal proximity. Applications requiring high measurement accuracy require great attention to detail regarding thermal gradients. Careful circuit board layout, component placement, and protection from stray air currents are necessary to minimize common thermal error sources.

Also, the user should take care to keep the bottom of the setpoint programming divider ladder as close to GND (Pin 4) as possible to minimize errors due to IR voltage drops and coupling of external noise sources. In any case, a 0.1 μF capacitor for power supply bypassing is always recommended at the chip.

Safety Considerations In Heating And Cooling System Design

Designers should anticipate potential system fault conditions which may result in significant safety hazards which are outside the control of and cannot be corrected by the TMP01-based circuit. Governmental and industrial regulations regarding safety requirements and standards for such designs should be observed where applicable.

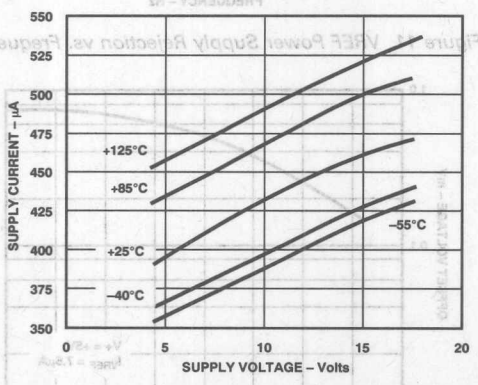

Figure 5. Supply Current vs. Supply Voltage

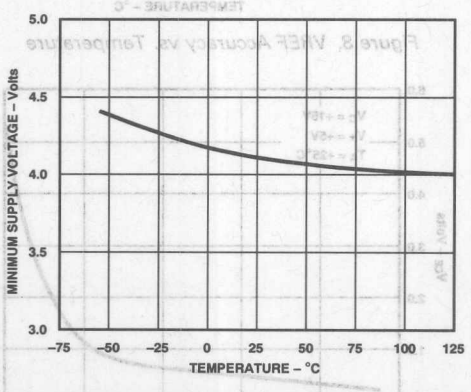

Figure 6. Minimum Supply Voltage vs. Temperature

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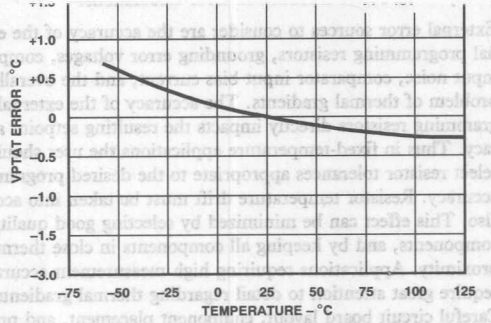


Figure 7. VPTAT Accuracy vs. Temperature

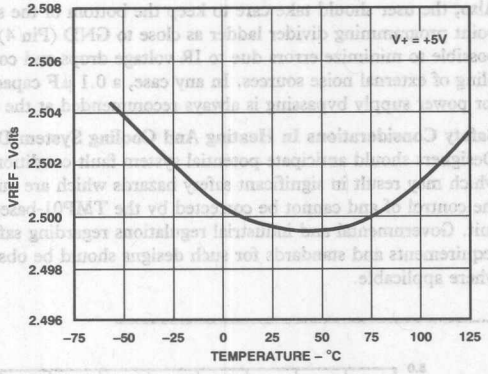


Figure 8. VREF Accuracy vs. Temperature

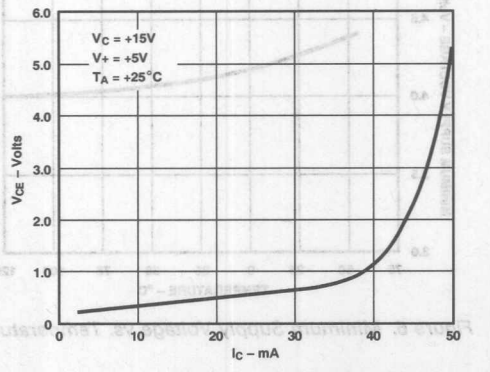


Figure 9. Open-Collector Output ($\overline{OVER}$, $\overline{UNDER}$) Saturation Voltage vs. Output Current

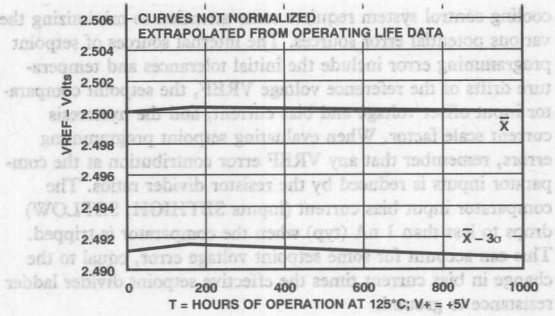


Figure 10. VREF Long Term Drift Accelerated by Burn-In

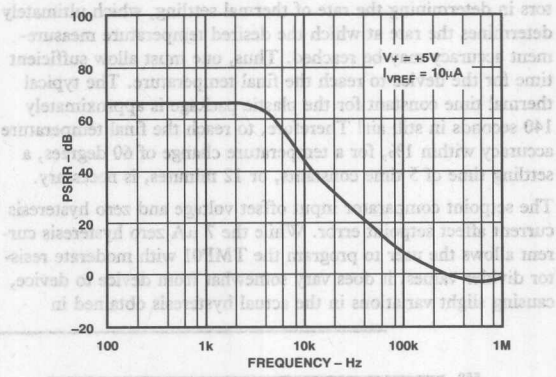


Figure 11. VREF Power Supply Rejection vs. Frequency

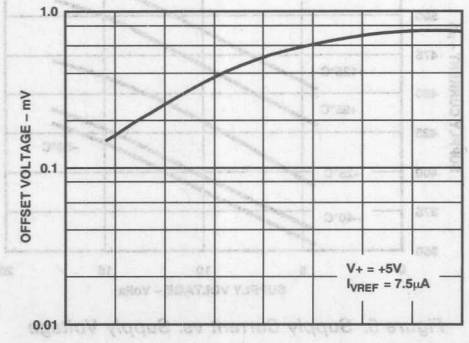


Figure 12. Set High, Set Low Input Offset Voltage vs. Temperature

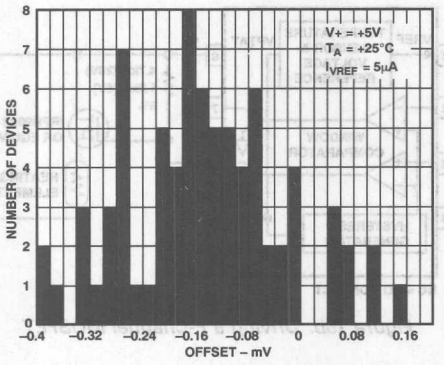


Figure 13. Comparator Input Offset Distribution

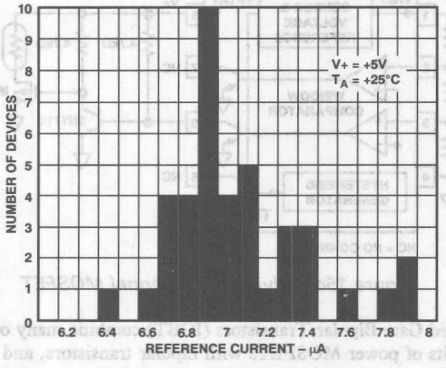


Figure 14. Zero Hysteresis Current Distribution

APPLICATIONS INFORMATION

Self-Heating Effects

In some applications the user should consider the effects of self-heating due to the power dissipated by the open-collector outputs, which are capable of sinking 20 mA continuously. Under full load, the TMP01 open-collector output device is dissipating

$$P_{DISS} = 0.6\ V \times .020A = 12\ mW$$

which in a surface-mount SO package accounts for a temperature increase due to self-heating of

$$\Delta T = P_{DISS} \times \theta_{JA} = .012\ W \times 158°C/W = 1.9°C.$$

This will of course directly affect the accuracy of the TMP01 and will for example cause the device to switch the heating output "OFF" 2 degrees early. Alternatively, bonding the same package to a moderate heatsink limits the self-heating effect to approximately

$$\Delta T = P_{DISS} \times \theta_{JC} = .012\ W \times 43°C/W = 0.52°C$$

which is a much more tolerable error in most systems. The VREF and VPTAT outputs are also capable of delivering sufficient current to contribute heating effects and should not be ignored.

Buffering the Voltage Reference

As mentioned above, the reference output VREF is used to generate the temperature setpoint programming voltages for the TMP01 and also is used to determine the hysteresis temperature band by the reference load current I_{VREF}. The on-board output buffer amplifier is typically capable of 500 μA output drive into as much as 50 pF load (max). Exceeding this load will affect the accuracy of the reference voltage, could cause thermal sensing errors due to dissipation, and may induce oscillations. Selection of a low drift buffer functioning as a voltage follower with high input impedance will ensure optimal reference accuracy, and will not affect the programmed hysteresis current. Amplifiers which offer the low drift, low power consumption, and low cost appropriate to this application include the OP295, and members of the OP90, OP97, OP177 families, and others as shown in the following applications circuits.

With excellent drift and noise characteristics, V_{REF} offers a good voltage reference for data acquisition and transducer excitation applications as well. Output drift is typically better than −10 ppm/°C, with 315 nV/$\sqrt{Hz}$ (typ) noise spectral density at 1 kHz.

Preserving Accuracy Over Wide Temperature Range Operation

The TMP01 is unique in offering both a wide-range temperature sensor and the associated detection circuitry needed to implement a complete thermostatic control function in one monolithic device. While the voltage reference, setpoint comparators, and output buffer amplifiers have been carefully compensated to maintain accuracy over the specified temperature range, the user has an additional task in maintaining the accuracy over wide operating temperature ranges in his application. Since the TMP01 is both sensor and control circuit, in many applications it is possible that the external components used to program and interface the device may be subjected to the same temperature extremes. Thus it may be necessary to locate components in close thermal proximity to minimize large temperature differentials, and to account for thermal drift errors where appropriate, such as resistor matching tempcos, amplifier error drift, and the like. Circuit design with the TMP01 requires a sightly different perspective regarding the thermal behavior of electronic components.

Thermal Response Time

The time required for a temperature sensor to settle to a specified accuracy is a function of the thermal mass of, and the thermal conductivity between the sensor and the object being sensed. Thermal mass is often considered equivalent to capacitance. Thermal conductivity is commonly specified using the symbol Q, and can be thought of as thermal resistance. It is commonly specified in units of degrees per watt of power transferred across the thermal joint. Thus, the time required for the TMP01 to settle to the desired accuracy is dependent on the package selected, the thermal contact established in that particular application, and the equivalent power of the heat source. In most applications, the settling time is probably best determined empirically.

Switching Loads With The Open-Collector Outputs

In many temperature sensing and control applications some type of switching is required. Whether it be to turn on a heater when the temperature goes below a minimum value or to turn off a motor that is overheating, the open-collector outputs Over and Under can be used. For the majority of applications, the switches used need to handle large currents on the order of 1 Amp and above. Because the TMP01 is accurately measuring temperature, the open-collector outputs should handle less than 20 mA of current to minimize self-heating. Clearly, the Overtemp and Undertemp outputs should not drive the equipment directly. Instead, an external switching device is required to handle the large currents. Some examples of these are relays, power MOSFETs, thyristors, IGBTs, and Darlingtons.

Figure 15 shows a variety of circuits where the TMP01 controls a switch. The main consideration in these circuits, such as the relay in Figure 15a, is the current required to activate the switch.

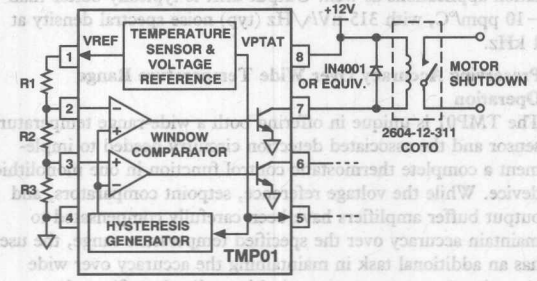


Figure 15a. Reed Relay Drive

It is important to check the particular relay you choose to ensure that the current needed to activate the coil does not exceed the TMP01's recommended output current of 20 mA. This is easily determined by dividing the relay coil voltage by the specified coil resistance. Keep in mind that the inductance of the relay will create large voltage spikes that can damage the TMP01 output unless protected by a commutation diode across the coil, as shown. The relay shown has a contact rating of 10 watts maximum. If a relay capable of handling more power is desired, the larger contacts will probably require a commensurately larger coil, with lower coil resistance and thus higher trigger current. As the contact power handling capability increases, so does the current needed for the coil. In some cases an external driving transistor should be used to remove the current load on the TMP01 as explained in the next section.

Power FETs are popular for handling a variety of high current DC loads. Figure 15b shows the TMP01 driving a p-channel MOSFET transistor for a simple heater circuit. When the output transistor turns on, the gate of the MOSFET is pulled down to approximately 0.6 V, turning it on. For most MOSFETs a gate-to-source voltage or Vgs on the order of −2 V to −5 V is sufficient to turn the device on. Figure 15c shows a similar circuit for turning on an n-channel MOSFET, except that now the gate to source voltage is positive. Because of this reason an external transistor must be used as an inverter so that the MOSFET will turn on when the "Under Temp" output pulls down.

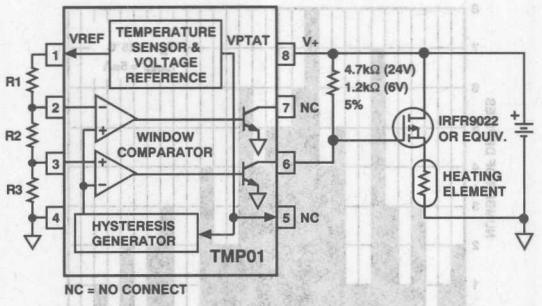


Figure 15b. Driving a P-Channel MOSFET

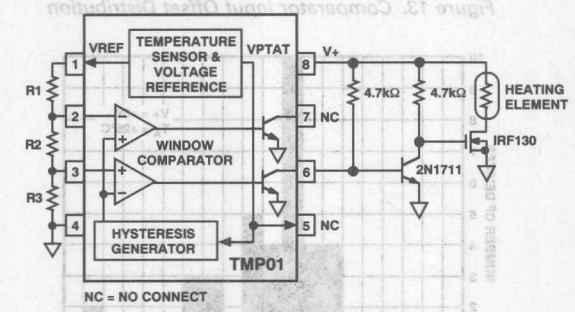


Figure 15c. Driving a N-Channel MOSFET

Isolated Gate Bipolar Transistors (IGBT) combine many of the benefits of power MOSFETs with bipolar transistors, and are used for a variety of high power applications. Because IGBTs have a gate similar to MOSFETs, turning on and off the devices is relatively simple as shown in Figure 15d. The turn on voltage for the IGBT shown (IRGBC40S) is between 3.0 and 5.5 volts. This part has a continuous collector current rating of 50 A and a maximum collector to emitter voltage of 600 V, enabling it to work in very demanding applications.

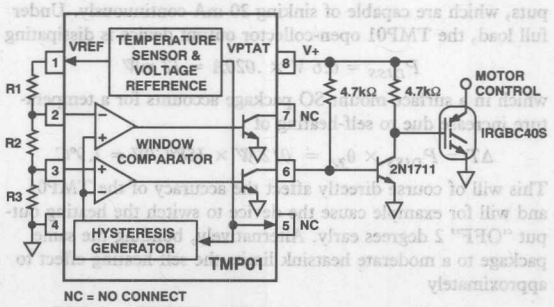


Figure 15d. Driving an IGBT

The last class of high power devices discussed here are Thyristors, which includes SCRs and Triacs. Triacs are a useful alternative to relays for switching ac line voltages. The 2N6073A shown in Figure 15e is rated to handle 4A (rms). The opto-isolated MOC3021 Triac shown features excellent electrical isolation from the noisy ac line and complete control over the high power Triac with only a few additional components.

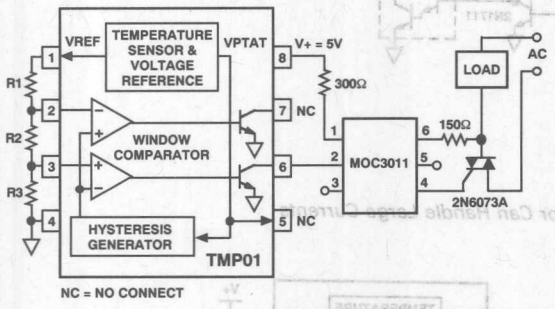


Figure 15e. Controlling the 2N6073A Triac

High Current Switching

As mentioned above, internal dissipation due to large loads on the TMP01 outputs will cause some temperature error due to self-heating. External transistors remove the load from the TMP01, so that virtually no power is dissipated in the internal transistors and no self-heating occurs. Figure 16 shows a few examples using external transistors. The simplest case, using a single transistor on the output to invert the output signal is shown in Figure 16a. When the open-collector of the TMP01 turns "ON" and pulls the output down, the external transistor Q1's base will be pulled low, turning off the transistor. Another transistor can be added to reinvert the signal as shown in Figure 16b. Now, when the output of the TMP01 is pulled down, the first transistor, Q1, turns off and its collector goes high, which turns Q2 on, pulling its collector low. Thus, the output taken from the collector of Q2 is identical to the output of the TMP01. By picking a transistor that can accommodate large amounts of current, many high power devices can be switched.

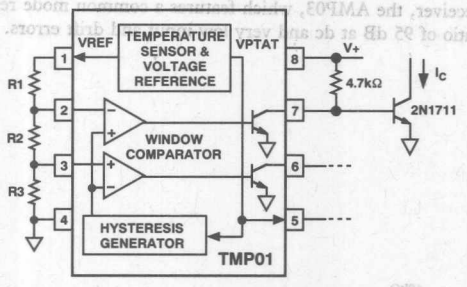


Figure 16a. An External Resistor Minimizes Self-Heating

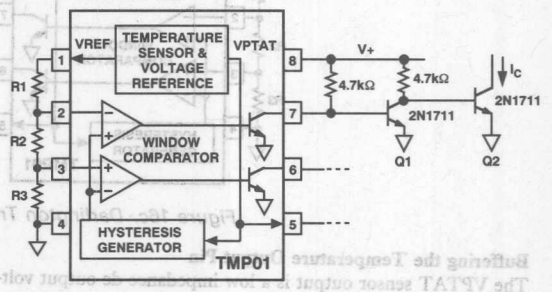


Figure 16b. Second Transistor Maintains Polarity of TMP01 Output

An example of a higher power transistor is a standard Darlington configuration as shown in Figure 16c. The part chosen, TIP-110, can handle 2A continuous which is more than enough to control many high power relays. In fact the Darlington itself can be used as the switch, similar to MOSFETs and IGBTs.

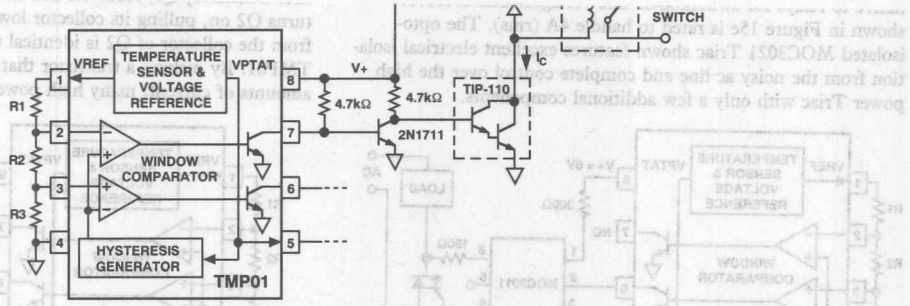


Figure 16c. Darlington Transistor Can Handle Large Currents

Buffering the Temperature Output Pin

The VPTAT sensor output is a low impedance dc output voltage with a 5 mV/K temperature coefficient, and is useful in a number of measurement and control applications. In many applications, this voltage needs to be transmitted to a central location for processing. The buffered VPTAT voltage output is capable of 500 μA drive into 50 pF (max). As mentioned in the discussion above regarding buffering circuits for the VREF output, it is useful to consider external amplifiers for interfacing VPTAT to external circuitry to ensure accuracy, and to minimize loading which could create dissipation-induced temperature sensing errors. An excellent general-purpose buffer circuit using the OP177 is shown in Figure 17 which is capable of driving over 10 mA, and will remain stable under capacitive loads of up to 0.1 μF. Other interfacing ideas are shown below.

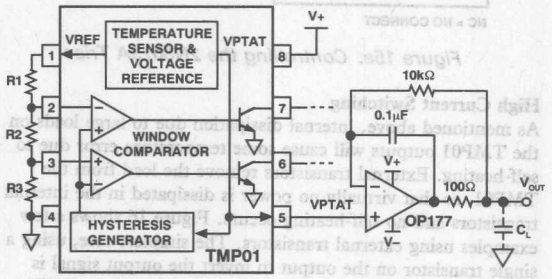


Figure 17. Buffer VPTAT to Handle Difficult Loads

Differential Transmitter

In noisy industrial environments, it is difficult to send an accurate analog signal over a significant distance. However, by sending the signal differentially on a wire pair, these errors can be significantly reduced. Since the noise will be picked up equally on both wires, a receiver with high common-mode input rejection can be used to cancel out the noise very effectively at the receiving end. Figure 18 shows two amplifiers being used to send the signal differentially, and an excellent differential receiver, the AMP03, which features a common mode rejection ratio of 95 dB at dc and very low input and drift errors.

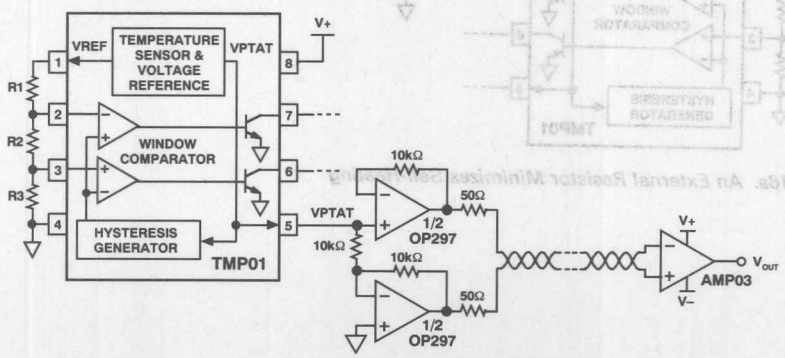


Figure 18. Send the Signal Differentially for Noise Immunity

4 mA–20 mA Current Loop

Another, very common method of transmitting a signal over long distances is to use a 4 mA–20 mA Loop, as shown in Figure 19. An advantage of using a 4 mA–20 mA loop is that the accuracy of a current loop is not compromised by voltage drops across the line. One requirement of 4 mA–20 mA circuits is that the remote end must receive all of its power from the loop, meaning that the circuit must consume less than 4 mA. Operating from +5 V, the quiescent current of the TMP01 is 500 μA max, and the OP90's is 20 μA max, totaling less than 4 mA. Although not shown, the open collector outputs and temperature setting pins can be connected to do any local control of switching.

The current is proportional to the voltage on the VPTAT output, and is calibrated to 4 mA at a temperature of −40°C, to 20 mA for +85°C. The main equation governing the operation of this circuit gives the current as a function of VPTAT:

$$I_{OUT} = \frac{1}{R_6}\left(\frac{VPTAT \times R_5}{R_2} - \frac{VREF \times R_3}{R_3 + R_1}\left(1 + \frac{R_5}{R_2}\right)\right)$$

The resulting temperature coefficient of the output current is 128 μA/°C.

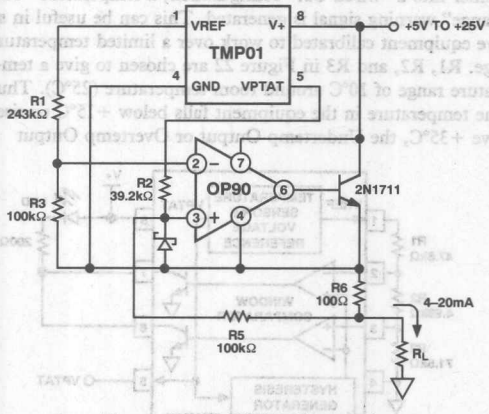


Figure 19. 4–20 mA Current Loop

To determine the resistor values in this circuit, first note that VREF remains constant over temperature. Thus the ratio of R5 over R2 must give a variation of I_{OUT} from 4 mA to 20 mA as VPTAT varies from 1.165 V at −40°C to 1.79 V at +85°C. The absolute value of the resistors is not important, only the ratio. For convenience, 100 kΩ is chosen for R5. Once R2 is calculated, the value of R3 and R1 is determined by substituting 4 mA for I_{OUT} and 1.165 V for VPTAT and solving. The final values are shown in the circuit. The OP90 is chosen for this circuit because of its ability to operate on a single supply and its high accuracy. For initial accuracy, a 10 kΩ trim potentiometer can be included in series with R3, and the value of R3 lowered to 95 kΩ. The potentiometer should be adjusted to produce an output current of 12.3 mA at 25°C.

Temperature-to-Frequency Converter

Another common method of transmitting analog information is to convert a voltage to the frequency domain. This is easily done with any of the low cost monolithic Voltage-to-Frequency Converters (VFCs) available, which feature a robust, open-collector digital output. A digital signal is very immune to noise and voltage drops because the only important information is the frequency. As long as the conversions between temperature and frequency are done accurately, the temperature data can be successfully transmitted.

A simple circuit to do this combines the TMP01 with an AD654 VFC, as shown in Figure 20. The AD654 outputs a square wave that is proportional to the dc input voltage according to the following equation:

$$F_{OUT} = \frac{V_{IN}}{10\,(R_1 + R_2)\,C_T}$$

By simply connecting the VPTAT output to the input of the AD654, the 5 mV/°C temperature coefficient gives a sensitivity of 25 Hz/°C, centered around 7.5 kHz at 25°C. The trimming resistor R2 is needed to calibrate the absolute accuracy of the AD654. For more information on that part, please consult the AD654 data sheet. Finally, the AD650 can be used to accurately convert the frequency back to a dc voltage on the receiving end.

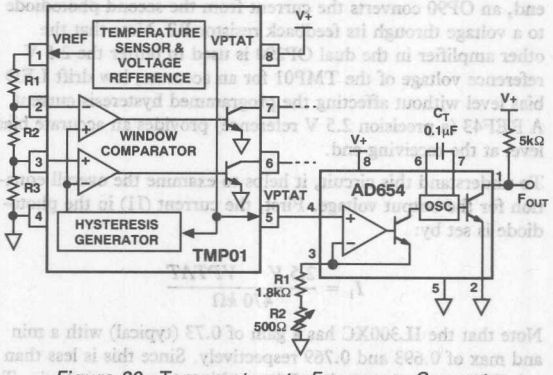


Figure 20. Temperature-to-Frequency Converter

Isolation Amplifier

In many industrial applications the sensor is located in an environment that needs to be electrically isolated from the central processing area. Figure 21 shows a simple circuit that uses an 8-pin optoisolator (IL300XC) that can operate across a 5,000 V barrier. IC1 (an OP290 single-supply amplifier) is used to drive the LED connected between Pins 1 to 2. The feedback actually

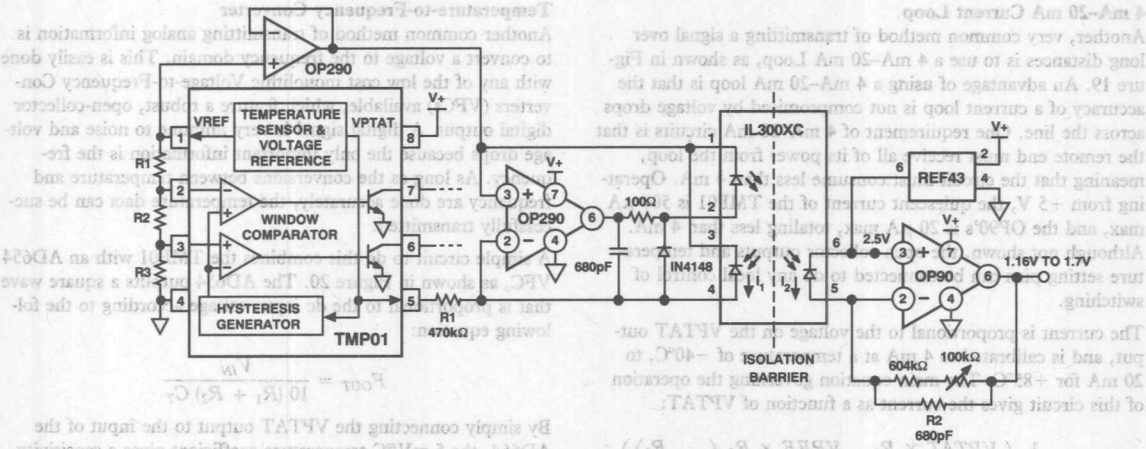


Figure 21. Isolation Amplifier

comes from the photodiode connected from Pins 3 to 4. The OP290 drives the LED such that there is enough current generated in the photodiode to exactly equal the current derived from the VPTAT voltage across the 470 kΩ resistor. On the receiving end, an OP90 converts the current from the second photodiode to a voltage through its feedback resistor R2. Note that the other amplifier in the dual OP290 is used to buffer the 2.5 V reference voltage of the TMP01 for an accurate, low drift LED bias level without affecting the programmed hysteresis current. A REF43 (a precision 2.5 V reference) provides an accurate bias level at the receiving end.

To understand this circuit, it helps to examine the overall equation for the output voltage. First, the current (I1) in the photodiode is set by:

$$I_1 = \frac{2.5\ V - VPTAT}{470\ k\Omega}$$

Note that the IL300XC has a gain of 0.73 (typical) with a min and max of 0.693 and 0.769 respectively. Since this is less than 1.0, R2 must be larger than R1 to achieve overall unity gain. To show this the full equation is:

$$V_{OUT} = 2.5\ V - I_2R_2 = 2.5\ V - 0.7\left(\frac{2.5\ V - VPTAT}{470\ k\Omega}\right)644\ k\Omega = VPTAT$$

A trim is included for R2 to correct for the initial gain accuracy of the IL300XC. To perform this trim, simply adjust for an output voltage equal to VPTAT at any particular temperature. For example, at room temperature, VPTAT = 1.49 V, so adjust R2 until V_{OUT} = 1.49 V as well. Both the REF43 and the OP90 operate from a single supply, and contribute no significant error due to drift.

In order to avoid the accuracy trim, and to reduce board space, complete isolation amplifiers are available, such as the high accuracy AD202.

Out-of-Range Warning

By connecting the two open collector outputs of the TMP01 together into a "wired-OR" configuration, a temperature "out-of-range" warning signal is generated. This can be useful in sensitive equipment calibrated to work over a limited temperature range. R1, R2, and R3 in Figure 22 are chosen to give a temperature range of 10°C around room temperature (25°C). Thus, if the temperature in the equipment falls below +15°C or rises above +35°C, the Undertemp Output or Overtemp Output

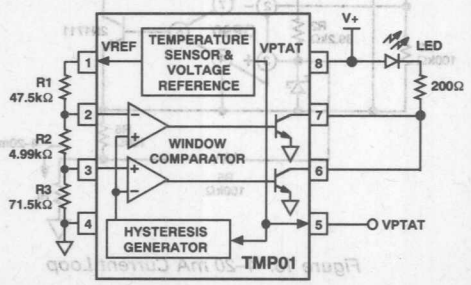


Figure 22. Out-of-Range Warning

respectively will go low and turn the LED on. The LED may be replaced with a simple pull-up resistor to give a logic output for controlling the instrument, or any of the switching devices discussed above can be used.

Translating 5 mV/K to 10 mV/°C

A useful circuit is shown in Figure 23 that translates the VPTAT output voltage, which is calibrated in Kelvins, into an output that can be read directly in degrees Celsius on a voltmeter display. To accomplish this, an external amplifier is configured as a differential amplifier. The resistors are scaled so the VREF voltage will exactly cancel the VPTAT voltage at 0.0°C.

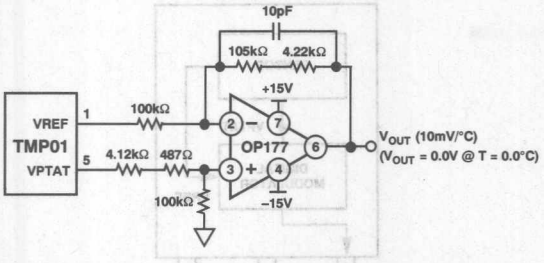


Figure 23. Translating 5 mV/K to 10 mV/°C

However, the gain from VPTAT to the output is two, so that 5 mV/K becomes 10 mV/°C. Thus, for a temperature of +80°C, the output voltage is 800 mV. Circuit errors will be due primarily to the inaccuracies of the resistor values. Using 1% resistors the observed error was less than 10 mV, or 1°C. The 10 pF feedback capacitor helps to ensure against oscillations. For better accuracy, a adjustment potentiometer can be added in series with either 100 kΩ resistor.

Translating VPTAT to the Fahrenheit Scale

A very similar circuit to the one shown in Figure 23 can be used to translate VPTAT into an output that can be read directly in degrees Fahrenheit, with a scaling of 10 mV/°F. Only unity gain or less is available from the first stage differentiating circuit, so the second amplifier provides a gain of two to complete the conversion to the Fahrenheit scale. Using the circuit in Figure 24, a temperature of 0.0°F gives an output of 0.00 V. At room temperature (70°F) the output voltage is 700 mV. A −40°C to +85°C operating range translates into −40°F to +185°F. The errors are essentially the same as for the circuit in Figure 23.

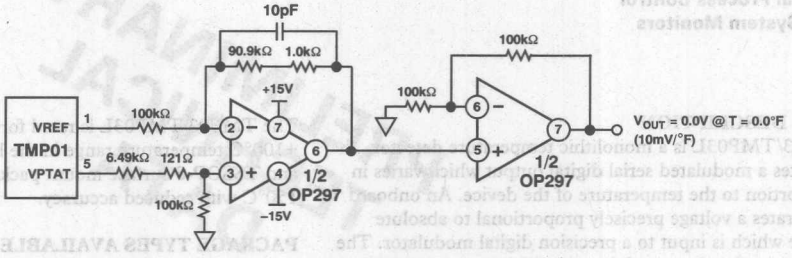
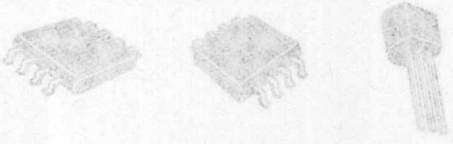


Figure 24. Translating 5 mV/K to 10 mV/°F



Micropower Temperature Peripheral

TMP03/TMP03L*

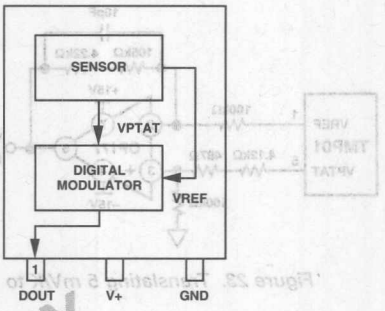
FEATURES

Modulated Serial Digital Output
Proportional to Temperature
±1.2°C Accuracy Over Temperature (typ)
Specified –40°C to +100°C, Operation to 150°C
Power Consumption 3.5 mW at 5 V
No External Components
Flexible Open Collector Output (TMP03)
CMOS/TTL Compatible Output on TMP03L
Low Voltage Operation (4.5 V to 7 V)
Low Cost 3-Pin Packages

APPLICATIONS

Isolated Sensors
Environmental Control Systems
Thermal Protection
Industrial Process Control
Power System Monitors

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

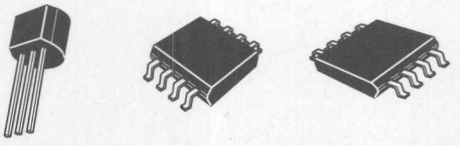
The TMP03/TMP03L is a monolithic temperature detector that generates a modulated serial digital output which varies in direct proportion to the temperature of the device. An onboard sensor generates a voltage precisely proportional to absolute temperature which is input to a precision digital modulator. The ratiometric encoding format of the serial digital output is independent of the clock drift errors common to most serial modulation techniques such as voltage-to-frequency converters. Overall accuracy is ±1.2 degrees (typical) over the rated operating temperature range, with excellent transducer linearity. The digital output of the TMP03L is CMOS/TTL compatible and is easily interfaced to the serial inputs of most popular microprocessors. The open collector output of the TMP03 is capable of sinking 20 mA and is suitable for industrial systems including isolated circuits utilizing opto-couplers or isolation transformers.

The TMP03 and the TMP03L are specified for operation at supply voltages from 4.5 V to 7 V. Operating from +5 V, supply current (unloaded) is less than 700 µA (max).

The TMP03/TMP03L is rated for operation over the –40°C to +100°C temperature range in the low cost TO-92, and SO-8 and TSSOP-8 surface mount packages. Operation extends to 150°C with reduced accuracy.

PACKAGE TYPES AVAILABLE

TO-92 **SO-8** **TSSOP-8**



***Patent pending.**

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

TMP03E/TMP03F–SPECIFICATIONS (V+ = +5 V, −40°C ≤ T_A ≤ +100°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ACCURACY						
Scale Factor Deviation "E"		0°C < T_A < 40°C[1]		0.6	1.2	°C
Scale Factor Deviation "F"		0°C < T_A < 40°C[1]		0.8	2.4	°C
Scale Factor Deviation "E"		Over Rated Temperature[1]		1.2	2.2	°C
Scale Factor Deviation "F"		Over Rated Temperature[1]		1.8	2.8	°C
Nominal Duty Cycle		T_A = 0°C		42.2		%
Power Supply Rejection Ratio	PSRR	Over Rated Supply		0.05		%/V
OUTPUTS						
Output Low Voltage	V_{OL}	I_{SINK} = 1.6 mA			0.2	V
Output Low Voltage	V_{OL}	I_{SINK} = 15 mA			1	V
Digital Output Capacitance	C_{OUT}	(Note 3)		15		pF
Fall Time	t_{HL}	See Test Load			250	ns
Device Turn-On Time				20		ms
POWER SUPPLY						
Supply Range	V+		4.5		7	V
Supply Current	I_{SY}	Unloaded			700	µA

NOTES
[1]Maximum deviation from output duty cycle transfer function over specified temperature range.
[2]Does not consider errors caused by heating due to dissipation of output load currents.
[3]Guaranteed but not tested.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

TMP03LE/TMP03LF–SPECIFICATIONS (V+ = +5 V, −40°C ≤ T_A ≤ +100°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ACCURACY						
Scale Factor Deviation "E"		0°C < T_A < 40°C		0.6	1.2	°C
Scale Factor Deviation "F"		0°C < T_A < 40°C		0.8	2.4	°C
Scale Factor Deviation "E"		Over Rated Temperature[1]		1.2	2.2	°C
Scale Factor Deviation "F"		Over Rated Temperature[1]		1.8	2.8	°C
Nominal Duty Cycle		T_A = 0°C		42.2		%
Power Supply Rejection Ratio	PSRR	Over Rated Supply		0.05		%/V
OUTPUTS						
Output High Voltage	V_{OH}	I_{OH} = 800 µA	V+ −0.4			V
Output Low Voltage	V_{OL}	I_{OL} = 800 µA			400	mV
Digital Output Capacitance	C_{OUT}	(Note 3)		15		pF
Fall Time	t_{HL}	See Test Load			250	ns
Rise Time	t_{LH}	See Test Load			250	ns
Device Turn-On Time				20		ms
POWER SUPPLY						
Supply Range	V+		4.5		7	V
Supply Current	I_{SY}	Unloaded			700	µA

NOTES
[1]Maximum deviation from output duty cycle transfer function over specified temperature range.
[2]Does not consider errors caused by heating due to dissipation of output load currents.
[3]Guaranteed but not tested.
Specifications subject to change without notice.

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measurement system with digital output, on a single chip. The onboard temperature sensor follows in the footsteps of the TMP01 low power, programmable temperature controller, offering excellent accuracy and linearity over the entire rated temperature range without correction or calibration by the user.

The sensor output is digitized by an advanced first order sigma-delta modulator, also known as the "charge balance" type analog-to-digital converter. See Figure 1. This type of converter utilizes time domain oversampling and a high accuracy comparator to deliver 12 bits of effective accuracy in an extremely compact circuit

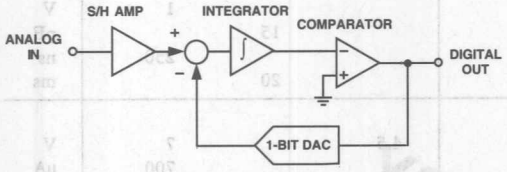

Figure 1. First-Order Sigma-Delta Modulator

Basically, the sigma-delta modulator consists of an input sample-and-hold, a summing amplifier, an integrator, a comparator, and a 1-bit DAC. Similar to the voltage-to-frequency converter, this architecture creates in effect a negative feedback loop whose intent is to minimize the integrator output by changing the duty cycle of the comparator output in response to input voltage changes. The comparator samples the output of the integrator at a much higher rate than the input sampling frequency, called oversampling. This spreads the quantization noise over a much wider band than that of the input signal, improving overall noise performance and increasing accuracy.

The modulated output of the comparator is encoded using a patented technique which results in a serial digital signal with a ratiometric duty cycle format which is easily decoded by any microprocessor into either degrees Centigrade or degrees Fahrenheit values, and readily transmitted or modulated over a single wire. Most importantly, this encoding method neatly avoids major error sources common to other modulation techniques, as it is clock independent.

Output Encoding

Accurate sampling of an analog signal requires precise spacing of the sampling interval in order to maintain an accurate representation of the signal in the time domain. This dictates a master clock between the digitizer and the signal processor. In the case of compact, cost-effective data acquisition systems, the addition of a buffered high speed clock line can represent a significant burden on the overall system design. Alternatively, the addition of an onboard clock circuit with the appropriate accuracy and drift performance to an integrated circuit can add significant cost. The modulation and encoding techniques utilized in the TMP03/TMP03L avoid this problem and allow the overall circuit to fit into a compact, three-pin package. To achieve this, a simple, compact onboard clock and an oversampling digitizer which is insensitive to sampling rate variations are used. TMP03L's clock is irrelevant, and the effects of clock variations at the counter are effectively cancelled upon decoding.

The output of the TMP03/TMP03L is a square wave with a nominal frequency of 45 Hz. The output format is readily decoded by the user as follows:

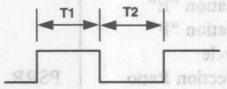

Figure 2. TMP03/TMP03L Output Format

$$Temperature\,(°C) = 260 - \left(\frac{450 \times T1}{T2}\right)$$

$$Temperature\,(°F) = 500 - \left(\frac{810 \times T1}{T2}\right)$$

where the time period T1 (low period) and T2 (high period) are counter values easily read by a microprocessor input port, and the above calculations performed in software. Since both periods are obtained consecutively, using the same clock, performing the division indicated in the above formulas results in a ratiometric value that is independent of the exact frequencies of, or drift in, either the originating clock of the TMP03 or the user's counting clock.

A period counting clock of approximately 1 MHz (or higher) will provide sufficient resolution to maintain the specified measurement accuracy of the TMP03/TMP03L. While a system running a 1 MHz clock will require counter registers of at least 12 bits, faster clocks will require commensurately larger registers to avoid overflow truncation errors. See the Applications section below which discusses a variety of hardware interfacing and software ideas.

Self-Heating Effects

Observing the thermal conductivity of the various TMP03/TMP03L packages, in some applications the user should consider the effects of self-heating due to the power dissipated by the digital output, which is capable of sinking 800 µA continuous. Under full load, the output may dissipate

$$P_{DISS} = (0.6\,V)(0.8\,mA) = 0.48\,mW$$

which in a free-standing surface-mount TSSOP package accounts for a temperature increase due to self-heating of

$$\Delta T = P_{DISS} \times \theta_{JA} = 0.48\,mW \times XXX\,°C/W = YY\,°C.$$

This will, of course, directly affect the accuracy of the TMP03/TMP03L relative to the true ambient temperature. Alternatively, when the same package has been bonded to measure a large plate or other thermal mass (effectively a large heatsink), the self-heating error might be limited to approximately

$$\Delta T = P_{DISS} \times \theta_{JC} = 0.48\,mW \times 10°C/W = 0.0048°C$$

which is a negligible error.

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Signal Compression Components
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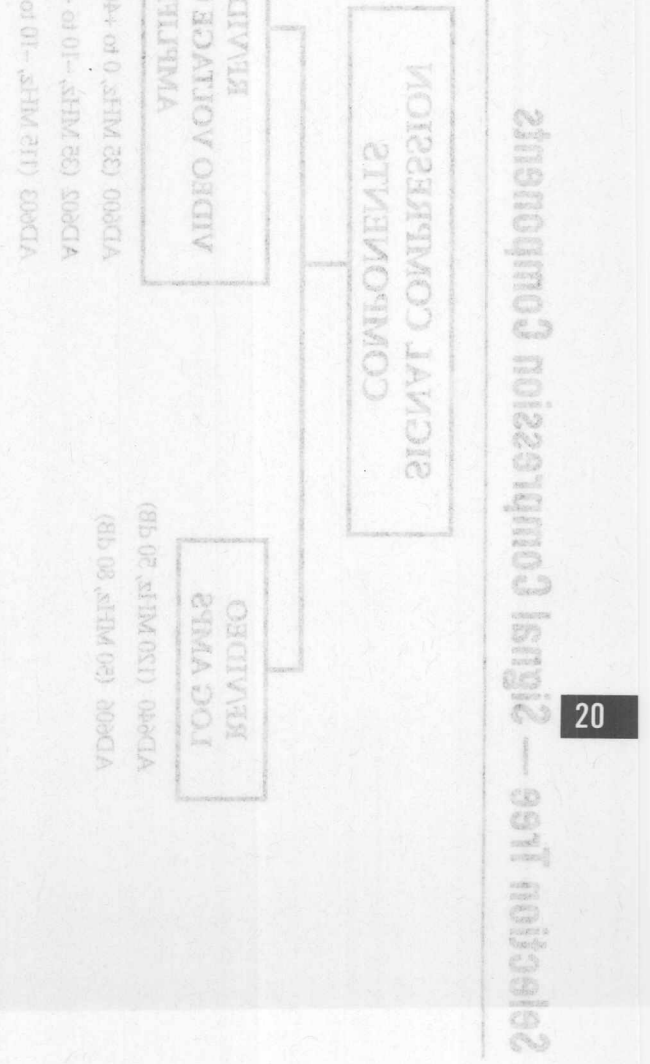
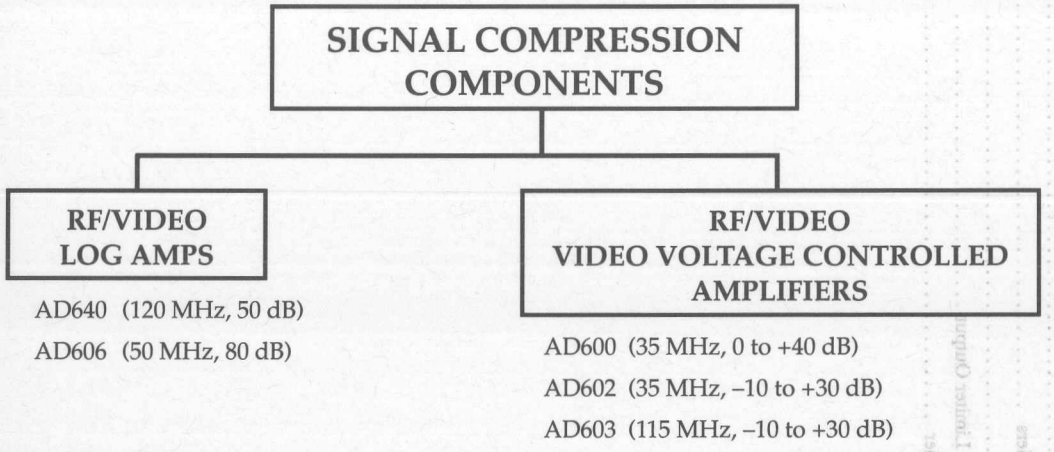
AD606 – 50 MHz, 80 dB Demodulating Logarithmic Amplifier with Limiter Output	20–29
AD640 – DC Coupled Demodulating 120 MHz Logarithmic Amplifier	20–40



Selection Tree — Signal Compression Components



Selection Guide—Signal Compression Components

Model	Input Range	Log Conformity RTI	BW kHz	Package Options[1]	Temp Ranges[2]	Comments	Page
AD640	**0.75 mV–200 mV**	**±0.6 dB**	**120 MHz**	**D, E, N, P**	**C, I, M/$_{DS}$**	**120 MHz, 45 dB, DC Demodulating Logarithmic Amplifier**	**20–40**
AD600	**±2 V**	**±0.5 dB**	**30 MHz**	**N, R**	**C, I, M/**	**Dual 0 dB to +40 dB Variable Gain Amplifier**	**20–5**
AD602	**±2 V**	**±0.5 dB**	**30 MHz**	**N, R**	**C, I, M/**	**Dual −10 dB to +30 dB Variable Gain Amplifier**	**20–5**
AD603	**±2 V**	**±0.4 dB**	**100 MHz**	**N, R**	**I, M**	**Single Channel Variable Gain Amplifier**	**20–17**
AD606	**−80 to +10 dBm (50 Ω)**	**±1 dB**	**50 MHz**	**N, R**	**C**	**50 MHz, 80 dB Demodulating Logarithmic Amplifier with Limiter Output**	**20–29**

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_{J}$ for JAN, $_{D}$ for SMD, and $_{S}$ for space level.
Boldface Type: Data sheet information in this volume.

FEATURES

Two Channels with Independent Gain Control
"Linear in dB" Gain Response
Two Gain Ranges:
AD600: 0 dB to +40 dB
AD602: −10 dB to +30 dB
Accurate Absolute Gain: ±0.3 dB
Low Input Noise: 1.4 nV/√Hz
Low Distortion: −60 dBc THD at ±1 V Output
High Bandwidth: DC to 35 MHz (−3 dB)
Stable Group Delay: ±2 ns
Low Power: 125 mW (max) per Amplifier
Signal Gating Function for Each Amplifier
Drives High Speed A/D Converters
MIL-STD-883 Compliant and DESC Versions Available

APPLICATIONS

Ultrasound and Sonar Time-Gain Control
High Performance Audio and RF AGC Systems
Signal Measurement

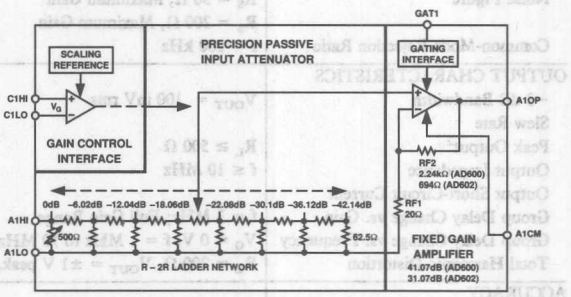
PRODUCT DESCRIPTION

The AD600 and AD602 dual channel, low noise variable gain amplifiers are optimized for use in ultrasound imaging systems, but are applicable to any application requiring very precise gain, low noise and distortion, and wide bandwidth. Each independent channel provides a gain of 0 to +40 dB in the AD600 and −10 dB to +30 dB in the AD602. The lower gain of the AD602 results in an improved signal-to-noise ratio at the output. However, both products have the same 1.4 nV/√Hz input noise spectral density. The decibel gain is directly proportional to the control voltage, is accurately calibrated, and is supply- and temperature-stable.

To achieve the difficult performance objectives, a proprietary circuit form—the X-AMP™—has been developed. Each channel of the X-AMP comprises a variable attenuator of 0 dB to −42.14 dB followed by a high speed fixed gain amplifier. In this way, the amplifier never has to cope with large inputs, and can benefit from the use of negative feedback to precisely define the gain and dynamics. The attenuator is realized as a seven-stage R-2R ladder network having an input resistance of 100 Ω, laser-trimmed to ±2%. The attenuation between tap points is 6.02 dB; the gain-control circuit provides continuous interpolation between these taps. The resulting control function is linear in dB.

X-AMP is a trademark of Analog Devices, Inc.
*Patented.

FUNCTIONAL BLOCK DIAGRAM



The gain-control interfaces are fully differential, providing an input resistance of ~15 MΩ and a scale factor of 32 dB/V (that is, 31.25 mV/dB) defined by an internal voltage reference. The response time of this interface is less than 1 μs. Each channel also has an independent gating facility that optionally blocks signal transmission and sets the dc output level to within a few millivolts of the output ground. The gating control input is TTL and CMOS compatible.

The maximum gain of the AD600 is 41.07 dB, and that of the AD602 is 31.07 dB; the −3 dB bandwidth of both models is nominally 35 MHz, essentially independent of the gain. The signal-to-noise ratio (SNR) for a 1 V rms output and a 1 MHz noise bandwidth is typically 76 dB for the AD600 and 86 dB for the AD602. The amplitude response is flat within ±0.5 dB from 100 kHz to 10 MHz; over this frequency range the group delay varies by less than ±2 ns at all gain settings.

Each amplifier channel can drive 100 Ω load impedances with low distortion. For example, the peak specified output is ±2.5 V minimum into a 500 Ω load, or ±1 V into a 100 Ω load. For a 200 Ω load in shunt with 5 pF, the total harmonic distortion for a ±1 V sinusoidal output at 10 MHz is typically −60 dBc.

The AD600J and AD602J are specified for operation from 0°C to +70°C, and are available in both 16-pin plastic DIP (N) and 16-pin SOIC (R). The AD600A and AD602A are specified for operation from −40°C to +85°C and are available in both 16-pin Cerdip (Q) and 16-pin SOIC (R).

The AD600S and AD602S are specified for operation from −55°C to +125°C and are available in a 16-pin Cerdip (Q) package and are MIL-STD-883 compliant. The AD600S and AD602S are also available under DESC SMD 5962-94572.

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD600/AD602—SPECIFICATIONS

(Each amplifier section, at T_A = +25°C, V_S = ±5 V, −625 mV ≤ V_G ≤ +625 mV, R_L = 500 Ω, and C_L = 5 pF, unless otherwise noted. Specifications for AD600 and AD602 are identical unless otherwise noted.)

Parameter	Conditions	AD600J/AD602J Min	AD600J/AD602J Typ	AD600J/AD602J Max	AD600A/AD602A Min	AD600A/AD602A Typ	AD600A/AD602A Max	Units
INPUT CHARACTERISTICS								
Input Resistance	Pins 2 to 3; Pins 6 to 7	**98**	**100**	**102**	**95**	**100**	**105**	Ω
Input Capacitance			2			2		pF
Input Noise Spectral Density[1]			1.4			1.4		nV/√Hz
Noise Figure	R_S = 50 Ω, Maximum Gain		5.3			5.3		dB
	R_S = 200 Ω, Maximum Gain		2			2		dB
Common-Mode Rejection Ratio	f = 100 kHz		30			30		dB
OUTPUT CHARACTERISTICS								
−3 dB Bandwidth	V_{OUT} = 100 mV rms		35			35		MHz
Slew Rate			275			275		V/μs
Peak Output[2]	$R_L \geq$ 500 Ω	±2.5	±3		±2.5	±3		V
Output Impedance	f ≤ 10 MHz		2			2		Ω
Output Short-Circuit Current			50			50		mA
Group Delay Change vs. Gain	f = 3 MHz; Full Gain Range		±2			±2		ns
Group Delay Change vs. Frequency	V_G = 0 V; f = 1 MHz to 10 MHz		±2			±2		ns
Total Harmonic Distortion	R_L = 200 Ω, V_{OUT} = ±1 V peak, Rpd = 1 kΩ		−60			−60		dBc
ACCURACY								
AD600								
Gain Error	0 dB to 3 dB Gain	**0**	**+0.5**	**+1**	**−0.5**	**+0.5**	**+0.5**	dB
	3 dB to 37 dB Gain	**−0.5**	**±0.2**	**+0.5**	**−0.1**	**±0.2**	**+1.0**	dB
	37 dB to 40 dB Gain	**−1**	**−0.5**	**0**	**−1.5**	**−0.5**	**+0.5**	dB
Maximum Output Offset Voltage[3]	V_G = −625 mV to +625 mV		10	**50**		10	**65**	mV
Output Offset Variation	V_G = −625 mV to +625 mV		10	**50**		10	**65**	mV
AD602								
Gain Error	−10 dB to −7 dB Gain	**0**	**0.5**	**+1**	**−0.5**	**0.5**	**+1.5**	dB
	−7 dB to 27 dB Gain	**−0.5**	**±0.2**	**+0.5**	**−1.0**	**±0.2**	**+1.0**	dB
	27 dB to 30 dB Gain	**−1**	**−0.5**	**0**	**−1.5**	**−0.5**	**+0.5**	dB
Maximum Output Offset Voltage[3]	V_G = −625 mV to +625 mV		5	**30**		10	**45**	mV
Output Offset Variation	V_G = −625 mV to +625 mV		5	**30**		10	**45**	mV
GAIN CONTROL INTERFACE								
Gain Scaling Factor	3 dB to 37 dB (AD600); −7 dB to 27 dB (AD602)	**31.7**	**32**	**32.3**	**30.5**	**32**	**33.5**	dB/V
Common-Mode Range		−0.75		2.5	−0.75		2.5	V
Input Bias Current			0.35	1		0.35	1	μA
Input Offset Current			10	50		10	50	nA
Differential Input Resistance	Pins 1 to 16; Pins 8 to 9		15			15		MΩ
Response Rate	Full 40 dB Gain Change		40			40		dB/μs
SIGNAL GATING INTERFACE								
Logic Input "LO" (Output ON)				0.8			0.8	V
Logic Input "HI" (Output OFF)		2.4			2.4			V
Response Time	ON to OFF, OFF to ON		0.3			0.3		μs
Input Resistance	Pins 4 to 3; Pins 5 to 6		30			30		kΩ
Output Gated OFF								
Output Offset Voltage			±10	**±100**		±10	**±400**	mV
Output Noise Spectral Density			65			65		nV/√Hz
Signal Feedthrough @ 1 MHz								
AD600			−80			−80		dB
AD602			−70			−70		dB
POWER SUPPLY								
Specified Operating Range		±4.75		±5.25	±4.75		±5.25	V
Quiescent Current			11	**12.5**		11	**14**	mA

NOTES

[1]Typical open or short-circuited input; noise is lower when system is set to maximum gain and input is short-circuited. This figure includes the effects of both voltage and current noise sources.

[2]Using resistive loads of 500 Ω or greater, or with the addition of a 1 kΩ pull-down resistor when driving lower loads.

[3]The dc gain of the main amplifier in the AD600 is X113; thus an input offset of only 100 μV becomes an 11.3 mV output offset. In the AD602, the amplifier's gain is X35.7; thus, an input offset of 100 μV becomes a 3.57 mV output offset.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage $\pm V_S$ . . . . . ±7.5 V
Input Voltages
Pins 1, 8, 9, 16 . . . . . $\pm V_S$
Pins 2, 3, 6, 7 . . . . . ±2 V Continuous
. . . . . $\pm V_S$ for 10 ms
Pins 4, 5 . . . . . $\pm V_S$
Internal Power Dissipation[2] . . . . . 600 mW
Operating Temperature Range (J) . . . . . 0°C to +70°C
Operating Temperature Range (A) . . . . . −40°C to +85°C
Operating Temperature Range (S) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature, Soldering 60 sec . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics: 16-Pin Plastic Package; θ_{JA} = 85°C/Watt
16-Pin SOIC Package; θ_{JA} = 100°C/Watt
16-Pin Cerdip Package; θ_{JA} = 120°C/Watt

ORDERING GUIDE

Model	Gain Range	Temperature Range	Package Option[1]
AD600AQ	0 dB to +40 dB	−40°C to +85°C	Q-16
AD600AR	0 dB to +40 dB	−40°C to +85°C	R-16
AD602AQ	−10 dB to +30 dB	−40°C to +85°C	Q-16
AD602AR	−10 dB to +30 dB	−40°C to +85°C	R-16
AD600JN	0 dB to +40 dB	0°C to +70°C	N-16
AD600JR	0 dB to +40 dB	0°C to +70°C	R-16
AD602JN	−10 dB to +30 dB	0°C to +70°C	N-16
AD602JR	−10 dB to +30 dB	0°C to +70°C	R-16
AD600SQ/883B[2]	0 dB to +40 dB	−55°C to +150°C	Q-16
AD602SQ/883B[3]	−10 dB to +30 dB	−55°C to +150°C	Q-16

NOTES
[1]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[2]Refer to AD600/AD602 Military data sheet. Also available as 5962-9457201MPA.
[3]Refer to AD600/AD602 Military data sheet. Also available as 5962-9457202MPA.

CAUTION

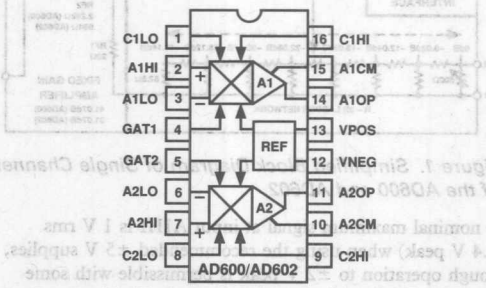
ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN DESCRIPTIONS

Pin	Function	Description
Pin 1	C1LO	CH1 Gain-Control Input "LO" (Positive Voltage Reduces CH1 Gain).
Pin 2	A1HI	CH1 Signal Input "HI" (Positive Voltage Increases CH1 Output).
Pin 3	A1LO	CH1 Signal Input "LO" (Usually Taken to CH1 Input Ground).
Pin 4	GAT1	CH1 Gating Input (A Logic "HI" Shuts Off CH1 Signal Path).
Pin 5	GAT2	CH2 Gating Input (A Logic "HI" Shuts Off CH2 Signal Path).
Pin 6	A2LO	CH2 Signal Input "LO" (Usually Taken to CH2 Input Ground).
Pin 7	A2HI	CH2 Signal Input "HI" (Positive Voltage Increases CH2 Output).
Pin 8	C2LO	CH2 Gain-Control Input "LO" (Positive Voltage Reduces CH2 Gain).
Pin 9	C2HI	CH2 Gain-Control Input "HI" (Positive Voltage Increases CH2 Gain).
Pin 10	A2CM	CH2 Common (Usually Taken to CH2 Output Ground).
Pin 11	A2OP	CH2 Output.
Pin 12	VNEG	Negative Supply for Both Amplifiers.
Pin 13	VPOS	Positive Supply for Both Amplifiers.
Pin 14	A1OP	CH1 Output.
Pin 15	A1CM	CH1 Common (Usually Taken to CH1 Output Ground).
Pin 16	C1HI	CH1 Gain-Control Input "HI" (Positive Voltage Increases CH1 Gain).

CONNECTION DIAGRAM

16-Pin Plastic DIP (N) Package
16-Pin Plastic SOIC (R) Package
16-Pin Cerdip (Q) Package



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independent control interfaces, each having a scaling factor of 32 dB per volt. The gain of each amplifier in the AD600 is laser trimmed to 41.07 dB (X113), thus providing a control range of −1.07 dB to 41.07 dB (0 dB to 40 dB with overlap), while the AD602 amplifiers have a gain of 31.07 dB (X35.8) and provide an overall gain of −11.07 dB to 31.07 dB (−10 dB to 30 dB with overlap).

The advantage of this topology is that the amplifier can use negative feedback to increase the accuracy of its gain; also, since the amplifier never has to handle large signals at its input, the distortion can be very low. A further feature of this approach is that the small-signal gain and phase response, and thus the pulse response, are essentially independent of gain.

The following discussion describes the AD600. Figure 1 is a simplified schematic of one channel. The input attenuator is a seven-section R-2R ladder network, using untrimmed resistors of nominally R = 62.5 Ω, which results in a characteristic resistance of 125 Ω ±20%. A shunt resistor is included at the input and laser trimmed to establish a more exact input resistance of 100 Ω ±2%, which ensures accurate operation (gain and HP corner frequency) when used in conjunction with external resistors or capacitors.

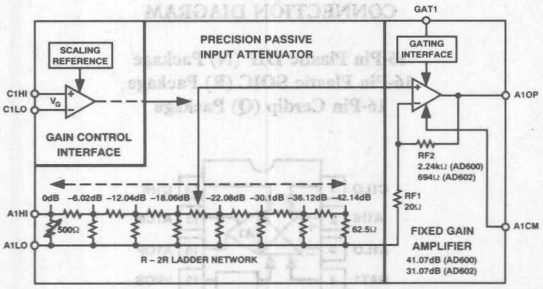

Figure 1. Simplified Block Diagram of Single Channel of the AD600 and AD602

The nominal maximum signal at input A1HI is 1 V rms (±1.4 V peak) when using the recommended ±5 V supplies, although operation to ±2 V peak is permissible with some increase in HF distortion and feedthrough. Each attenuator is provided with a separate signal "LO" connection, for use in rejecting common-mode, the voltage between input and output grounds. Circuitry is included to provide rejection of up to ±100 mV.

The signal applied at the input of the ladder network is attenuated by 6.02 dB by each section; thus, the attenuation to each of the taps is progressively 0, 6.02, 12.04, 18.06, 24.08, 30.1, 36.12 and 42.14 dB. A unique circuit technique is employed to interpolate between these tap points, indicated by the "slider" in Figure 1, providing continuous attenuation from 0 dB to 42.14 dB.

determined, and a linear decibel relationship is automatically guaranteed between the gain and the control parameter which determines the position of the slider. In practice, the gain deviates from the ideal law, by about ±0.2 dB peak (see, for example, Figure 6).

Note that the signal inputs are not fully differential: A1LO and A1CM (for CH1) and A2LO and A2CM (for CH2) provide separate access to the input and output grounds. This recognizes the practical fact that even when using a ground plane, small differences will arise in the voltages at these nodes. It is important that A1LO and A2LO be connected directly to the input ground(s); significant impedance in these connections will reduce the gain accuracy. A1CM and A2CM should be connected to the load ground(s).

Noise Performance

An important reason for using this approach is the superior noise performance that can be achieved. The nominal resistance seen at the inner tap points of the attenuator is 41.7 Ω (one third of 125 Ω), which exhibits a Johnson noise spectral density (NSD) of 0.84 nV/$\sqrt{\text{Hz}}$ (that is, $\sqrt{4kTR}$) at 27°C, which is a large fraction of the total input noise. The first stage of the amplifier contributes a further 1.12 nV/$\sqrt{\text{Hz}}$, for a total input noise of 1.4 nV/$\sqrt{\text{Hz}}$.

The noise at the 0 dB tap depends on whether the input is short-circuited or open-circuited: when shorted, the minimum NSD of 1.12 nV/$\sqrt{\text{Hz}}$ is achieved; when open, the resistance of 100 Ω at the first tap generates 1.29 nV/$\sqrt{\text{Hz}}$, so the noise increases to a total of 1.71 nV/$\sqrt{\text{Hz}}$. (This last calculation would be important if the AD600 were preceded, for example, by a 900 Ω resistor to allow operation from inputs up to ±10 V rms. However, in most cases the low impedance of the source will limit the maximum noise resistance.)

It will be apparent from the foregoing that it is essential to use a low resistance in the design of the ladder network to achieve low noise. In some applications this may be inconvenient, requiring the use of an external buffer or preamplifier. However, very few amplifiers combine the needed low noise with low distortion at maximum input levels, and the power consumption needed to achieve this performance is fundamentally required to be quite high (due to the need to maintain very low resistance values while also coping with large inputs). On the other hand, there is little value in providing a buffer with high input impedance, since the usual reason for this—the minimization of loading of a high resistance source—is not compatible with low noise.

Apart from the small variations just discussed, the signal-to-noise (S/N) ratio at the output is essentially independent of the attenuator setting, since the maximum undistorted output is 1 V rms and the NSD at the output of the AD600 is fixed at 113 times 1.4 nV$\sqrt{\text{Hz}}$, or 158 nV/$\sqrt{\text{Hz}}$. Thus, in a 1 MHz bandwidth, the output S/N ratio would be 76 dB. The input NSD of the AD600 and AD602 are the same, but because of the 10 dB lower gain in the AD602's fixed amplifier, its output S/N ratio is 10 dB better, or 86 dB in a 1 MHz bandwidth.

The Gain-Control Interface

The attenuation is controlled through a differential, high impedance (15 MΩ) input, with a scaling factor which is laser trimmed to 32 dB per volt, that is, 31.25 mV/dB. Each of the two amplifiers has its own control interface. An internal bandgap reference ensures stability of the scaling with respect to supply and temperature variations, and is the only circuitry common to both channels.

When the differential input voltage V_G = 0 V, the attenuator "slider" is centered, providing an attenuation of 21.07 dB, thus resulting in an overall gain of 20 dB (= −21.07 dB + 41.07 dB). When the control input is −625 mV, the gain is lowered by 20 dB (= 0.625 × 32), to 0 dB; when set to +625 mV, the gain is increased by 20 dB, to 40 dB. When this interface is overdriven in either direction, the gain approaches either −1.07 dB (= −42.14 dB + 41.07 dB) or 41.07 dB (= 0 + 41.07 dB), respectively.

The gain of the AD600 can thus be calculated using the following simple expression:

$$Gain\ (dB) = 32\ V_G + 20 \quad (1)$$

where V_G is in volts. For the AD602, the expression is:

$$Gain\ (dB) = 32\ V_G + 10 \quad (2)$$

Operation is specified for V_G in the range from −625 mV dc to +625 mV dc. The high impedance gain-control input ensures minimal loading when driving many amplifiers in multiple-channel applications. The differential input configuration provides flexibility in choosing the appropriate signal levels and polarities for various control schemes.

For example, the gain-control input can be fed differentially to the inputs, or single-ended by simply grounding the unused input. In another example, if the gain is to be controlled by a DAC providing a positive only ground referenced output, the "Gain Control LO" pin (either C1LO or C2LO) should be biased to a fixed offset of +625 mV, to set the gain to 0 dB when "Gain Control HI" (C1HI or C2HI) is at zero, and to 40 dB when at +1.25 V.

It is a simple matter to include a voltage divider to achieve other scaling factors. When using an 8-bit DAC having a FS output of +2.55 V (10 mV/bit) a divider ratio of 1.6 (generating 6.25 mV/bit) would result in a gain setting resolution of 0.2 dB/bit. Later, we will discuss how the two sections of an AD600 or AD602 may be cascaded, when various options exist for gain control.

Signal-Gating Inputs

Each amplifier section of the AD600 and AD602 is equipped with a signal gating function, controlled by a TTL or CMOS logic input (GAT1 or GAT2). The ground references for these inputs are the signal input grounds A1LO and A2LO, respectively. Operation of the channel is unaffected when this input is LO or left open-circuited. Signal transmission is blocked when this input is HI. The dc output level of the channel is set to within a few millivolts of the output ground (A1CM or A2CM), and simultaneously the noise level drops significantly. The reduction in noise and spurious signal feedthrough is useful in ultrasound beam-forming applications, where many amplifier outputs are summed.

Common-Mode Rejection

A special circuit technique is used to provide rejection of voltages appearing between input grounds (A1LO and A2LO) and output grounds (A1CM and A2CM). This is necessary because of the "op amp" form of the amplifier, as shown in Figure 1. The feedback voltage is developed across the resistor RF1 (which, to achieve low noise, has a value of only 20 Ω). The voltage developed across this resistor is referenced to the input common, so the output voltage is also referred to that node.

To provide rejection of this common voltage, an auxiliary amplifier (not shown) is included, which senses the voltage difference between input and output commons and cancels this error component. Thus, for zero differential signal input between A1HI and A1LO, the output A1OP simply follows the voltage at A1CM. Note that the range of voltage differences which can exist between A1LO and A1CM (or A2LO and A2CM) is limited to about ±100 mV. Figure 50 (one of the typical performance curves at the end of this data sheet) shows typical common-mode rejection ratio versus frequency.

ACHIEVING 80 dB GAIN RANGE

The two amplifier sections of the X-AMP can be connected in series to achieve higher gain. In this mode, the output of A1 (A1OP and A1CM) drives the input of A2 via a high-pass network (usually just a capacitor) that rejects the dc offset. The nominal gain range is now −2 dB to +82 dB for the AD600 or −22 dB to +62 dB for the AD602.

There are several options in connecting the gain-control inputs. The choice depends on the desired signal-to-noise ratio (SNR) and gain error (output ripple). The following examples feature the AD600; the arguments generally apply to the AD602, with appropriate changes to the gain values.

Sequential Mode (Maximum S/N Ratio)

In the sequential mode of operation, the SNR is maintained at its highest level for as much of the gain control range possible, as shown in Figure 2. Note here that the gain range is 0 dB to 80 dB. Figure 3 shows the general connections to accomplish this. Both gain-control inputs, C1HI and C2HI, are driven in parallel by a positive only, ground referenced source with a range of 0 V to +2.5 V.

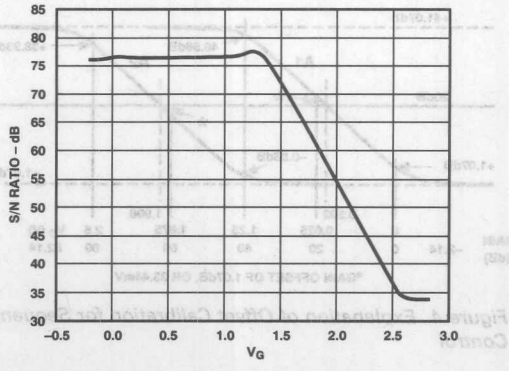

Figure 2. S/N Ratio vs. Control Voltage Sequential Control (1 MHz Bandwidth)

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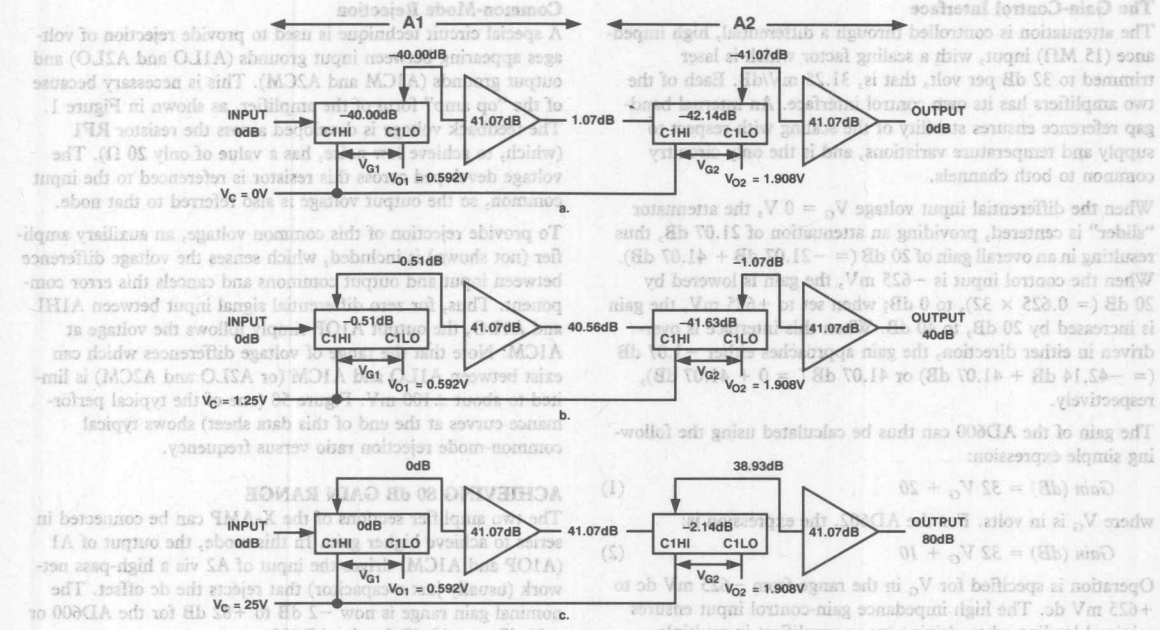

Figure 3. AD600 Gain Control Input Calculations for Sequential Control Operation

The gains are offset (Figure 4) such that A2's gain is increased only after A1's gain has reached its maximum value. Note that for a differential input of −700 mV or less, the gain of a single amplifier (A1 or A2) will be at its minimum value of −1.07 dB; for a differential input of +700 mV or more, the gain will be at its maximum value of 41.07 dB. Control inputs beyond these limits will not affect the gain and can be tolerated without damage or foldover in the response. See the Specifications Section of this data sheet for more details on the allowable voltage range. The gain is now

$$Gain\ (dB) = 32\ V_C \quad (3)$$

where V_C is the applied control voltage.

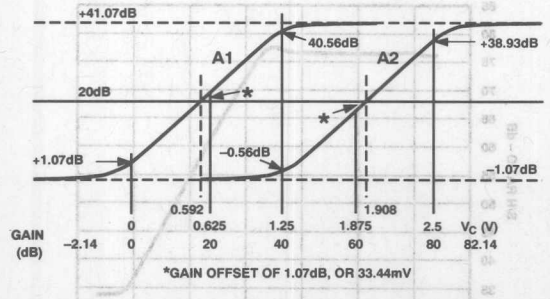

Figure 4. Explanation of Offset Calibration for Sequential Control

When V_C is set to zero, V_{G1} = −0.592 V and the gain of A1 is +1.07 dB (recall that the gain of each amplifier section is 0 dB for V_G = −625 mV); meanwhile, V_{G2} = −1.908 V so the gain of A2 is −1.07 dB. The overall gain is thus 0 dB (see Figure 3a). When V_C = +1.25 V, V_{G1} = 1.25 V − 0.592 V = +0.658 V, which sets the gain of A1 to 40.56 dB, while V_{G2} = 1.25 V − 1.908 V = −0.658 V, which sets A2's gain at −0.56 dB. The overall gain is now 40 dB (see Figure 3b). When V_C = +2.5 V, the gain of A1 is 41.07 dB and that of A2 is 38.93 dB, resulting in an overall gain of 80 dB (see Figure 3c). This mode of operation is further clarified by Figure 5, which is a plot of the separate gains of A1 and A2 and the overall gain versus the control voltage. Figure 6 is a plot of the gain error of the cascaded amplifiers versus the control voltage.

Parallel Mode (Simplest Gain-Control Interface)

In this mode, the gain-control voltage is applied to both inputs in parallel — C1HI and C2HI are connected to the control voltage, and C1LO and C2LO are optionally connected to an offset voltage of +0.625 V. The gain scaling is then doubled to 64 dB/V, requiring only 1.25 V for an 80 dB change of gain. The amplitude of the gain ripple in this case is also doubled, as shown in Figure 7, and the instantaneous signal-to-noise ratio at the output of A2 decreases linearly as the gain is increased (Figure 8).

Low Ripple Mode (Minimum Gain Error)

As can be seen in Figures 6 and 7, the output ripple is periodic. By offsetting the gains of A1 and A2 by half the period of the ripple, or 3 dB, the residual gain errors of the two amplifiers can be made to cancel. Figure 9 shows the much lower gain ripple when configured in this manner. Figure 10 plots the S/N ratio as a function of gain; it is very similar to that in the "Parallel Mode."

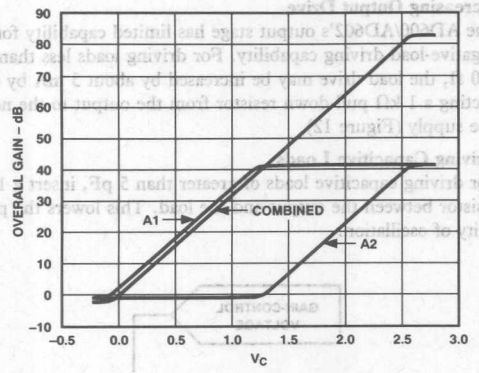

Figure 5. Plot of Separate and Overall Gains in Sequential Control

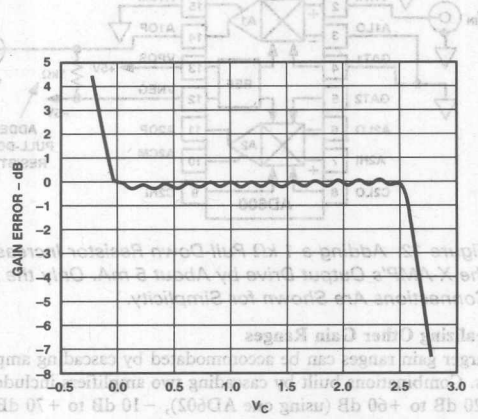

Figure 6. Gain Error for Cascaded Stages—Sequential Control

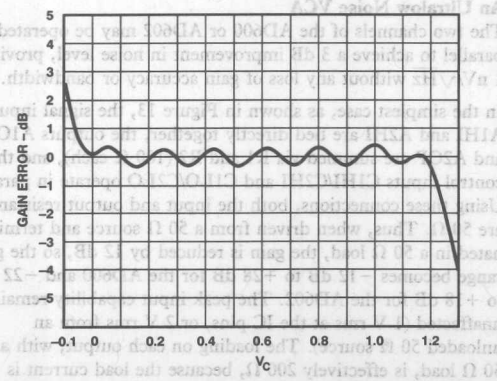

Figure 7. Gain Error for Cascaded Stages—Parallel Control

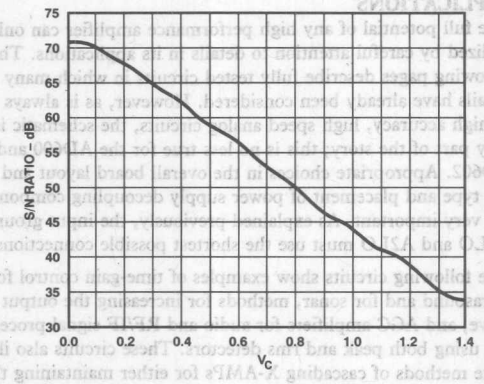

Figure 8. SNR for Cascaded Stages—Parallel Control

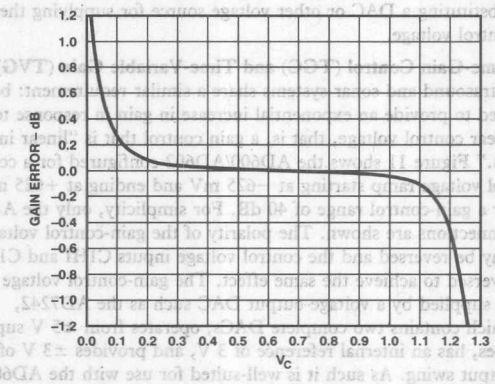

Figure 9. Gain Error for Cascaded Stages—Low Ripple Mode

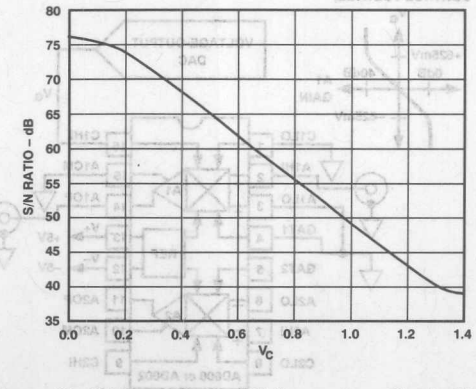

Figure 10. ISNR vs. Control Voltage—Low Ripple Mode

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APPLICATIONS

The full potential of any high performance amplifier can only be realized by careful attention to details in its applications. The following pages describe fully tested circuits in which many such details have already been considered. However, as is always true of high accuracy, high speed analog circuits, the schematic is only part of the story; this is no less true for the AD600 and AD602. Appropriate choices in the overall board layout and the type and placement of power supply decoupling components are very important. As explained previously, the input grounds A1LO and A2LO must use the shortest possible connections.

The following circuits show examples of time-gain control for ultrasound and for sonar, methods for increasing the output drive, and AGC amplifiers for audio and RF/IF signal processing using both peak and rms detectors. These circuits also illustrate methods of cascading X-AMPs for either maintaining the optimal S/N ratio or maximizing the accuracy of the gain-control voltage for use in signal measurement. These AGC circuits may be modified for use as voltage-controlled amplifiers for use in sonar and ultrasound applications by removing the detector and substituting a DAC or other voltage source for supplying the control voltage.

Time-Gain Control (TGC) and Time-Variable Gain (TVG)

Ultrasound and sonar systems share a similar requirement: both need to provide an exponential increase in gain in response to a linear control voltage, that is, a gain control that is "linear in dB." Figure 11 shows the AD600/AD602 configured for a control voltage ramp starting at −625 mV and ending at +625 mV for a gain-control range of 40 dB. For simplicity, only the A1 connections are shown. The polarity of the gain-control voltage may be reversed and the control voltage inputs C1HI and C1LO reversed to achieve the same effect. The gain-control voltage can be supplied by a voltage-output DAC such as the AD7242, which contains two complete DACs, operates from ±5 V supplies, has an internal reference of 3 V, and provides ±3 V of output swing. As such it is well-suited for use with the AD600/AD602, needing only a few resistors to scale the output voltage of the DACs to the levels needed by the AD600/AD602.

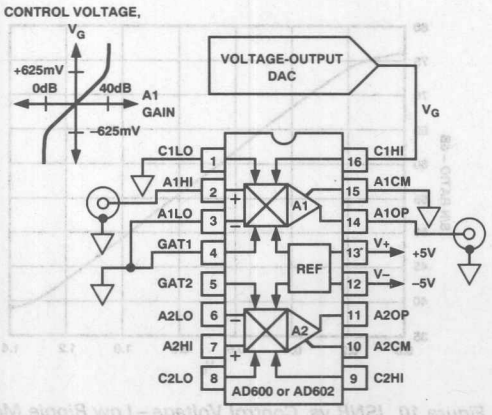

Figure 11. The Simplest Application of the X-AMP is as a TGC or TVG Amplifier in Ultrasound or Sonar. Only the A1 Connections Are Shown for Simplicity.

Increasing Output Drive

The AD600/AD602's output stage has limited capability for negative-load driving capability. For driving loads less than 500 Ω, the load drive may be increased by about 5 mA by connecting a 1 kΩ pull-down resistor from the output to the negative supply (Figure 12).

Driving Capacitive Loads

For driving capacitive loads of greater than 5 pF, insert a 10 Ω resistor between the output and the load. This lowers the possibility of oscillation.

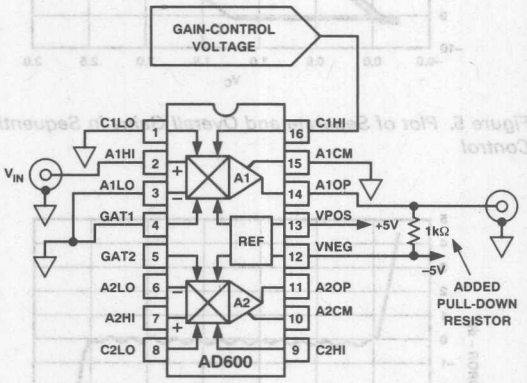

Figure 12. Adding a 1 kΩ Pull-Down Resistor Increases the X-AMP's Output Drive by About 5 mA. Only the A1 Connections Are Shown for Simplicity.

Realizing Other Gain Ranges

Larger gain ranges can be accommodated by cascading amplifiers. Combinations built by cascading two amplifiers include −20 dB to +60 dB (using one AD602), −10 dB to +70 dB (1/2 of an AD602 followed by 1/2 of an AD600), and 0 dB to 80 dB (one AD600). In multiple-channel applications, extra protection against oscillations can be provided by using amplifier sections from different packages.

An Ultralow Noise VCA

The two channels of the AD600 or AD602 may be operated in parallel to achieve a 3 dB improvement in noise level, providing 1 nV/$\sqrt{\text{Hz}}$ without any loss of gain accuracy or bandwidth.

In the simplest case, as shown in Figure 13, the signal inputs A1HI and A2HI are tied directly together, the outputs A1OP and A2OP are summed via R1 and R2 (100 Ω each), and the control inputs C1HI/C2HI and C1LO/C2LO operate in parallel. Using these connections, both the input and output resistances are 50 Ω. Thus, when driven from a 50 Ω source and terminated in a 50 Ω load, the gain is reduced by 12 dB, so the gain range becomes −12 dB to +28 dB for the AD600 and −22 dB to +18 dB for the AD602. The peak input capability remains unaffected (1 V rms at the IC pins, or 2 V rms from an unloaded 50 Ω source). The loading on each output, with a 50 Ω load, is effectively 200 Ω, because the load current is shared between the two channels, so the overall amplifier still meets its specified maximum output and distortion levels for a 200 Ω load. This amplifier can deliver a maximum sine wave power of +10 dBm to the load.

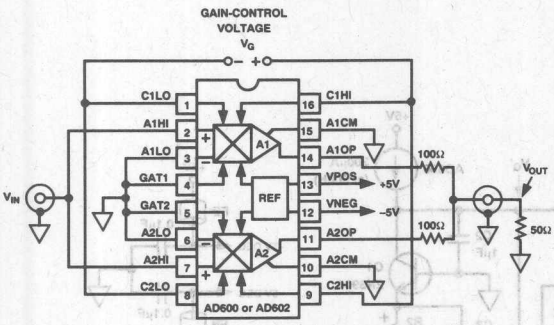

Figure 13. An Ultralow Noise VCA Using the AD600 or AD602

A Low Noise, 6 dB Preamplifier

In some ultrasound applications, the user may wish to use a high input impedance preamplifier to avoid the signal attenuation that would result from loading the transducer by the 100 Ω input resistance of the X-AMP. High gain cannot be tolerated, because the peak transducer signal is typically ±0.5 V, while the peak input capability of the AD600 or AD602 is only slightly more than ±1 V. A gain of two is a suitable choice. It can be shown that if the preamplifier's overall referred-to-input (RTI) noise is to be the same as that due to the X-AMP alone (1.4 nV/$\sqrt{\text{Hz}}$), then the input noise of a X2 preamplifier must be $\sqrt{(3/4)}$ times as large, that is, 1.2 nV/$\sqrt{\text{Hz}}$.

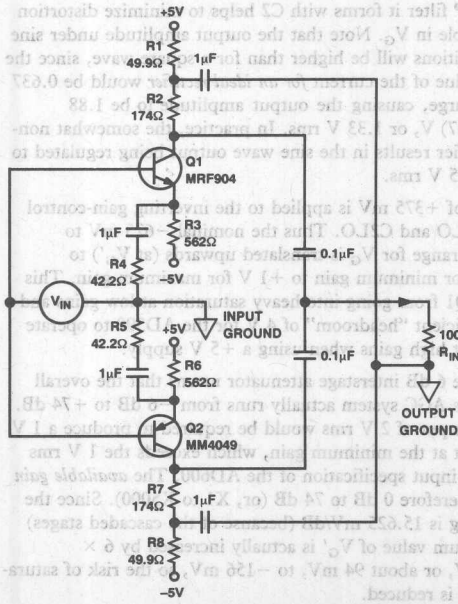

Figure 14. A Low Noise Preamplifier for the AD600 and AD602

An inexpensive circuit, using complementary transistor types chosen for their low $r_{bb'}$, is shown in Figure 14. The gain is determined by the ratio of the net collector load resistance to the net emitter resistance, that is, it is an open-loop amplifier. The gain will be X2 (6 dB) only into a 100 Ω load, assumed to be provided by the input resistance of the X-AMP; R2 and R7 are in shunt with this load, and their value is important in defining the gain. For small-signal inputs, both transistors contribute an equal transconductance, which is rendered less sensitive to signal level by the emitter resistors R4 and R5, which also play a dominant role in setting the gain.

This is a Class AB amplifier. As V_{IN} increases in a positive direction, Q1 conducts more heavily and its r_e becomes lower while that of Q2 increases. Conversely, more negative values of V_{IN} result in the r_e of Q2 decreasing, while that of Q1 increases. The design is chosen such that the net emitter resistance is essentially independent of the instantaneous value of V_{IN}, resulting in moderately low distortion. Low values of resistance and moderately high bias currents are important in achieving the low noise, wide bandwidth, and low distortion of this preamplifier. Heavy decoupling prevents noise on the power supply lines from being conveyed to the input of the X-AMP.

Table I. Measured Preamplifier Performance

Measurement		Value	Units
Gain (f = 30 MHz)		6	dB
Bandwidth (−3 dB)		250	MHz
Input Signal for 1 dB Compression		1	V p-p
Distortion			
V_{IN} = 200 mV p-p	HD2	0.27	%
	HD3	0.14	%
V_{IN} = 500 mV p-p	HD2	0.44	%
	HD3	0.58	%
System Input Noise Spectral Density (NSD) (Preamp plus X-AMP)		1.03	nV/$\sqrt{\text{Hz}}$
Input Resistance		1.4	kΩ
Input Capacitance		15	pF
Input Bias Current		±150	μA
Power Supply Voltage		±5	V
Quiescent Current		15	mA

A Low Noise AGC Amplifier with 80 dB Gain Range

Figure 15 provides an example of the ease with which the AD600 can be connected as an AGC amplifier. A1 and A2 are cascaded, with 6 dB of attenuation introduced by the 100 Ω resistor R1, while a time constant of 5 ns is formed by C1 and the 50 Ω of net resistance at the input of A2. This has the dual effect of (a) lowering the overall gain range from {0 dB to 80 dB} to {6 dB to 74 dB} and (b) introducing a single-pole low-pass filter with a −3 dB frequency of about 32 MHz. This ensures stability at the maximum gain for a slight reduction in the overall bandwidth. The capacitor C4 blocks the small dc offset voltage at the output of A1 (which might otherwise saturate A2 at its maximum gain) and introduces a high pass corner at about 8 kHz, useful in eliminating low frequency noise and spurious signals which may be present at the input.

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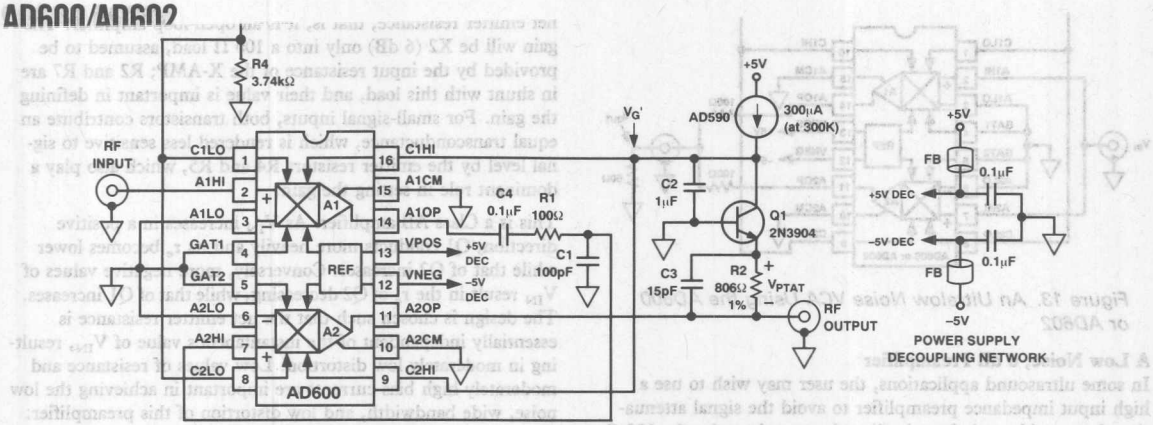

Figure 15. This Accurate HF AGC Amplifier Uses Just Three Active Components.

A simple half-wave detector is used, based on Q1 and R2. The average current into capacitor C2 is just the difference between the current provided by the AD590 (300 μA at 300 K, 27°C) and the collector current of Q1. In turn, the control voltage V_G is the time integral of this *error* current. When V_G (and thus the gain) is stable, the rectified current in Q1 must, on average, exactly balance the current in the AD590. If the output of A2 is too small to do this, V_G will ramp up, causing the gain to increase, until Q1 conducts sufficiently. The operation of this control system will now be described in detail.

First, consider the particular case where R2 *is zero* and the output voltage V_{OUT} is a square wave at, say, 100 kHz, that is, well above the corner frequency of the control loop. During the time V_{OUT} is negative, Q1 conducts; when V_{OUT} is positive, it is cut off. Since the *average* collector current is forced to be 300 μA, and the square wave has a 50% duty-cycle, the current when conducting must be 600 μA. With R2 omitted, the peak value of V_{OUT} would be just the V_{BE} of Q1 at 600 μA (typically about 700 mV) or 2 V_{BE} peak-to-peak. This voltage, hence the amplitude at which the output stabilizes, has a strong negative temperature coefficient (TC), typically −1.7 mV/°C. While this may not be troublesome in some applications, the correct value of R2 will render the output stable with temperature.

To understand this, first note that the current in the AD590 is closely proportional to absolute temperature (PTAT). (In fact, this IC is intended for use as a thermometer.) For the moment, continue to assume that the signal is a square wave. When Q1 is conducting, V_{OUT} is the now the *sum* of V_{BE} and a voltage which is PTAT and which can be chosen to have an equal but opposite TC to that of the base-to-emitter voltage. This is actually nothing more than the "bandgap voltage reference" principle in thinly veiled disguise! When we choose R2 such that the sum of the voltage across it and the V_{BE} of Q1 is close to the bandgap voltage of about 1.2 V, V_{OUT} will be stable over a wide range of temperatures, provided, of course, that Q1 and the AD590 share the same thermal environment.

Since the average emitter current is 600 μA during each half-cycle of the square wave, a resistor of 833 Ω would add a PTAT voltage of 500 mV at 300 K, increasing by 1.66 mV/°C. In practice, the optimum value of R2 will depend on the transistor used, and, to a lesser extent, on the waveform for which the temperature stability is to be optimized; for the devices shown and sine wave signals, the recommended value is 806 Ω. This resistor also serves to lower the peak current in Q1 and the 200 Hz LP filter it forms with C2 helps to minimize distortion due to ripple in V_G. Note that the output amplitude under sine wave conditions will be higher than for a square wave, since the average value of the current *for an ideal rectifier* would be 0.637 times as large, causing the output amplitude to be 1.88 (=1.2/0.637) V, or 1.33 V rms. In practice, the somewhat non-ideal rectifier results in the sine wave output being regulated to about 1.275 V rms.

An offset of +375 mV is applied to the inverting gain-control inputs C1LO and C2LO. Thus the nominal −625 mV to +625 mV range for V_G is translated upwards (at V_G') to −0.25 V for minimum gain to +1 V for maximum gain. This prevents Q1 from going into heavy saturation at low gains and leaves sufficient "headroom" of 4 V for the AD590 to operate correctly at high gains when using a +5 V supply.

In fact, the 6 dB interstage attenuator means that the overall gain of this AGC system actually runs from −6 dB to +74 dB. Thus, an input of 2 V rms would be required to produce a 1 V rms output at the minimum gain, which exceeds the 1 V rms maximum input specification of the AD600. The *available gain* range is therefore 0 dB to 74 dB (or, X1 to X5000). Since the gain scaling is 15.625 mV/dB (because of the cascaded stages) the minimum value of V_G' is actually increased by 6 × 15.625 mV, or about 94 mV, to −156 mV, so the risk of saturation in Q1 is reduced.

The emitter circuit of Q1 is somewhat inductive (due its finite f_t and base resistance). Consequently, the effective value of R2 increases with frequency. This would result in an increase in the stabilized output amplitude at high frequencies, but for the

addition of C3, determined experimentally to be 15 pF for the 2N3904 for maximum response flatness. Alternatively, a faster transistor can be used here to reduce HF peaking. Figure 16 shows the ac response at the stabilized output level of about 1.3 V rms. Figure 17 demonstrates the output stabilization for sine wave inputs of 1 mV to 1 V rms at frequencies of 100 kHz, 1 MHz and 10 MHz.

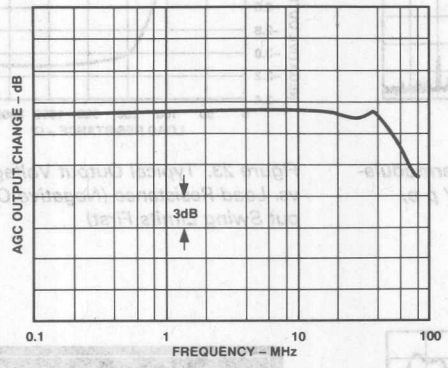

Figure 16. AC Response at the Stabilized Output Level of 1.3 V RMS

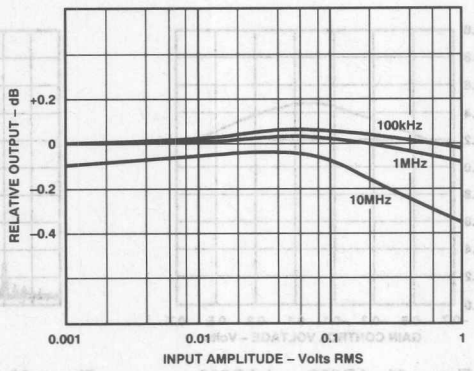

Figure 17. Output Stabilization vs. RMS Input for Sine Wave Inputs at 100 kHz, 1 MHz, and 10 MHz

While the "bandgap" principle used here sets the output amplitude to 1.2 V (for the square wave case), the stabilization point can be set to any higher amplitude, up to the maximum output of $\pm$ (V_S – 2) V which the AD600 can support. It is only necessary to split R2 into two components of appropriate ratio whose parallel sum remains close to the zero-TC value of 806 Ω. This is illustrated in Figure 18, which shows how the output can be raised, without altering the temperature stability.

Typical Performance Characteristics

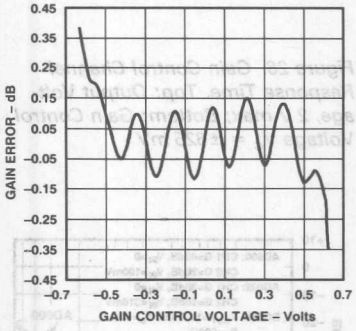

Figure 18. Gain Error vs. Gain Control Voltage

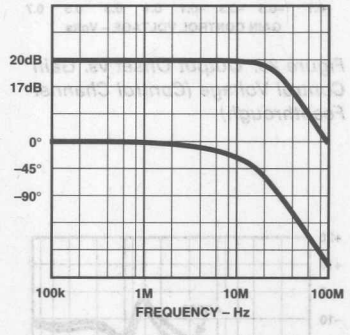

Figure 19. AD600 Frequency and Phase Response vs. Gain

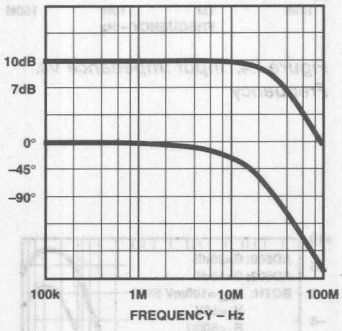

Figure 20. AD602 Frequency and Phase Response vs. Gain

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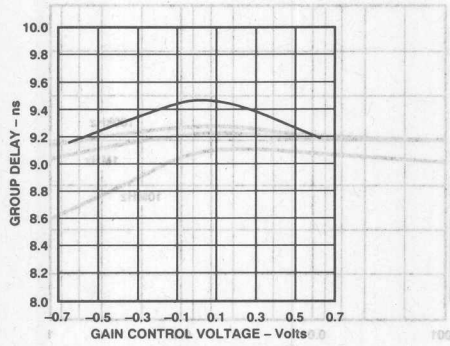


Figure 21. AD600 and AD602 Typical Group Delay vs. V_C

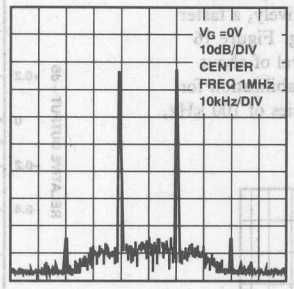


Figure 22. Third Order Intermodulation Distortion, V_{OUT} = 2 V p-p, R_L = 500 Ω

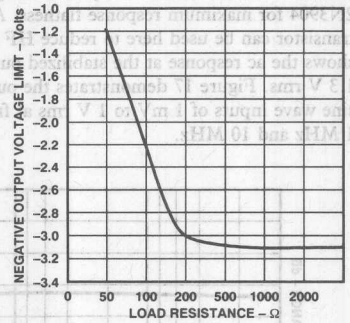


Figure 23. Typical Output Voltage vs. Load Resistance (Negative Output Swing Limits First)

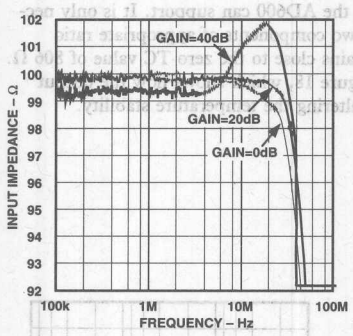


Figure 24. Input Impedance vs. Frequency

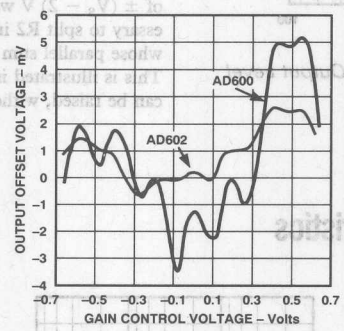


Figure 25. Output Offset vs. Gain Control Voltage (Control Channel Feedthrough)

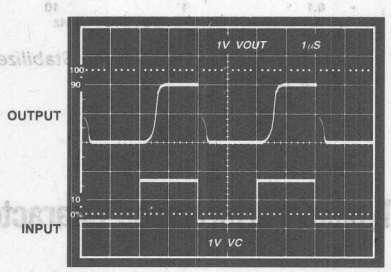


Figure 26. Gain Control Channel Response Time. Top: Output Voltage, 2 V max; Bottom: Gain Control Voltage V_C = ±625 mV

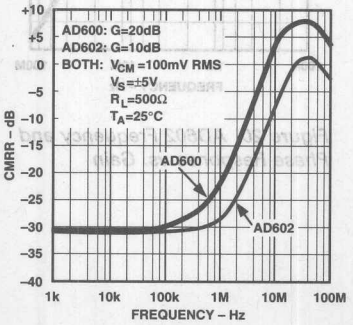


Figure 27. CMRR vs. Frequency

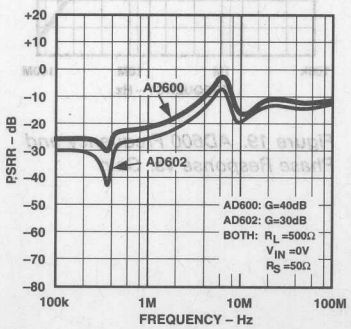


Figure 28. PSRR vs. Frequency

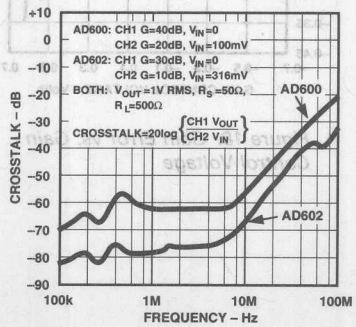


Figure 29. Crosstalk Between A1 and A2 vs. Frequency

Low Noise, 90 MHz Variable-Gain Amplifier

AD603*

FEATURES
"Linear in dB" Gain Control
Pin Programmable Gain Ranges
−11 dB to +31 dB with 90 MHz Bandwidth
+9 dB to +51 dB with 9 MHz Bandwidth
Any Intermediate Range, e.g., −1 dB to +41 dB with 45 MHz Bandwidth
Bandwidth Independent of Variable Gain
1.3 nV/$\sqrt{Hz}$ Input Noise Spectral Density
±0.5 dB Typical Gain Accuracy
MIL-STD-883 Compliant and DESC Versions Available

APPLICATIONS
RF/IF AGC Amplifier
Video Gain Control
A/D Range Extension
Signal Measurement

PRODUCT DESCRIPTION

The AD603 is a low noise, voltage-controlled amplifier for use in RF and IF AGC systems. It provides accurate, pin selectable gains of −11 dB to +31 dB with a bandwidth of 90 MHz or +9 dB to +51 dB with a bandwidth of 9 MHz. Any intermediate gain range may be arranged using one external resistor. The input referred noise spectral density is only 1.3 nV/$\sqrt{Hz}$ and power consumption is 125 mW at the recommended ±5 V supplies.

The decibel gain is "linear in dB," accurately calibrated, and stable over temperature and supply. The gain is controlled at a high impedance (50 MΩ), low bias (200 nA) differential input; the scaling is 25 mV/dB, requiring a gain-control voltage of only 1 V to span the central 40 dB of the gain range. An over- and under-range of 1 dB is provided whatever the selected range. The gain-control response time is less than 1 μs for a 40 dB change.

The differential gain-control interface allows the use of either differential or single-ended positive or negative control voltages. Several of these amplifiers may be cascaded and their gain-control gains offset to optimize the system S/N ratio.

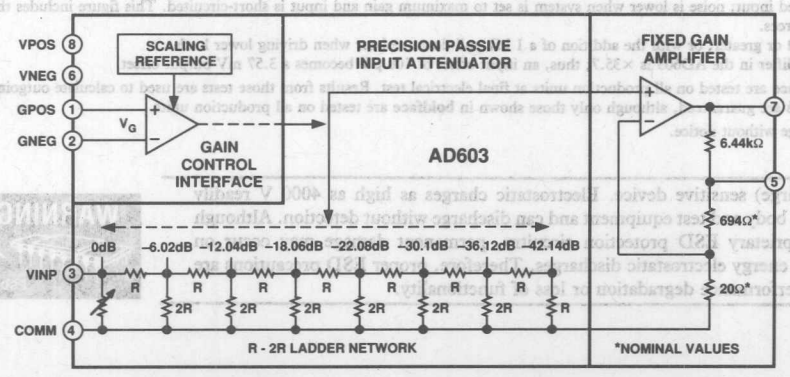
The AD603 can drive a load impedance as low as 100 Ω with low distortion. For a 500 Ω load in shunt with 5 pF, the total harmonic distortion for a ±1 V sinusoidal output at 10 MHz is typically −60 dBc. The peak specified output is ±2.5 V minimum into a 500 Ω load, or ±1 V into a 100 Ω load.

The AD603 uses a proprietary circuit topology—the X-AMP™. The X-AMP comprises a variable attenuator of 0 dB to −42.14 dB followed by a fixed-gain amplifier. Because of the attenuator, the amplifier never has to cope with large inputs and can use negative feedback to define its (fixed) gain and dynamic performance. The attenuator has an input resistance of 100 Ω, laser trimmed to ±3%, and comprises a seven-stage R-2R ladder network, resulting in an attenuation between tap points of 6.021 dB. A proprietary interpolation technique provides a continuous gain-control function which is linear in dB.

The AD603A is specified for operation from −40°C to +85°C and is available in both 8-pin SOIC (R) and 8-pin ceramic DIP (Q). The AD603S is specified for operation from −55°C to +125°C and is available in an 8-pin ceramic DIP (Q). The AD603 is also available under DESC SMD 5962-94572.

*Patented.
X-AMP is a trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



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AD603 SPECIFICATIONS (At T_A = +25°C, V_S = ±5 V, −500 mV ≤ V_G ≤ +500 mV, −10 dB to +30 dB

Input Resistance	Pins 3 to 4	**97**	100	**103**	Ω
Input Capacitance			2		pF
Input Noise Spectral Density[1]	Input Short Circuited		1.3		$nV/\sqrt{Hz}$
Peak Input Voltage			±1.4	±2	V
OUTPUT CHARACTERISTICS					
−3 dB Bandwidth	V_{OUT} = 100 mV rms		90		MHz
Slew Rate	$R_L \geq 500\ \Omega$		275		V/μs
Peak Output[2]	$R_L \geq 500\ \Omega$	±2.5	±3.0		V
Output Impedance	f ≤ 10 MHz		2		Ω
Output Short-Circuit Current			50		mA
Group Delay Change vs. Gain	f = 3 MHz; Full Gain Range		±2		ns
Group Delay Change vs. Frequency	V_G = 0 V; f = 1 to 10 MHz		±2		ns
Differential Gain			0.2		%
Differential Phase			0.2		Degree
Total Harmonic Distortion	f = 10 MHz, V_{OUT} = 1 V rms		−60		dBc
ACCURACY					
Gain Accuracy	−500 mV ≤ V_G ≤ +500 mV		±0.5	**±1**	dB
T_{MIN} to T_{MAX}				±1.5	
Output Offset Voltage[3]	V_G = 0 V			**20**	mV
T_{MIN} to T_{MAX}				30	
Output Offset Variation vs. V_G	−500 mV ≤ V_G ≤ +500 mV			**20**	mV
T_{MIN} to T_{MAX}				30	mV
GAIN CONTROL INTERFACE					
Gain Scaling Factor		**39.4**	40	**40.6**	dB/V
T_{MIN} to T_{MAX}		38		42	dB/V
Common-Mode Range		−1.2		+2.0	V
Input Bias Current			200		nA
Input Offset Current			10		nA
Differential Input Resistance	Pins 1 to 2		50		MΩ
Response Rate	Full 40 dB Gain Change		40		dB/μs
POWER SUPPLY					
Specified Operating Range		±4.75		±5.25	V
Quiescent Current			12.5	**17**	mA
T_{MIN} to T_{MAX}				20	mA

NOTES

[1]Typical open or short-circuited input; noise is lower when system is set to maximum gain and input is short-circuited. This figure includes the effects of both voltage and current noise sources.

[2]Using resistive loads of 500 Ω or greater, or with the addition of a 1 kΩ pull-down resistor when driving lower loads.

[3]The dc gain of the main amplifier in the AD603 is ×35.7; thus, an input offset of 100 μV becomes a 3.57 mV output offset.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD603 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage $\pm V_S$ . . . . . ± 7.5 V
Input Voltage VINP (Pin 3) . . . . . ± 2 V Continuous
. . . . . $\pm V_S$ for 10 ms
GNEG, GPOS (Pins 1, 2) . . . . . $\pm V_S$
Internal Power Dissipation[1] . . . . . 400 mW
Operating Temperature Range
AD603A . . . . . −40°C to +85°C
AD603S . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature, Soldering 60 sec . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

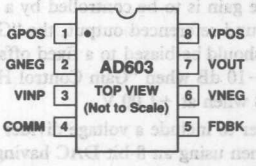
[1]Thermal Characteristics:
8-Pin SOIC Package: θ_{JA} = 155°C/Watt, θ_{JC} = 33°C/Watt
8-Pin Ceramic Package: θ_{JA} = 140°C/Watt, θ_{JC} = 15°C/Watt.

PIN DESCRIPTION

Pin	Mnemonic	Description
Pin 1	GPOS	Gain-Control Input "HI" (Positive Voltage Increases Gain)
Pin 2	GNEG	Gain-Control Input "LO" (Negative Voltage Increases Gain)
Pin 3	VINP	Amplifier Input
Pin 4	COMM	Amplifier Ground
Pin 5	FDBK	Connection to Feedback Network
Pin 6	VNEG	Negative Supply Input
Pin 7	VOUT	Amplifier Output
Pin 8	VPOS	Positive Supply Input

CONNECTION DIAGRAM

8-Pin Plastic SOIC (R) Package
8-Pin Ceramic DIP (Q) Package



ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option[1]
AD603AR	−40°C to +85°C	8-Pin SOIC	R-8
AD603AQ	−40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD603SQ/883B[2]	−55°C to +125°C	8-Pin Ceramic DIP	Q-8

NOTES
[1]R = SOIC; Q = Cerdip. For outline information see Package Information section.
[2]Refer to AD603 Military data sheet. Also available as 5962-9457203MPA.

THEORY OF OPERATION

The AD603 comprises a fixed-gain amplifier, preceded by a broadband passive attenuator of 0 to 42.14 dB, having a gain-control scaling factor of 40 dB per volt. The fixed gain is laser-trimmed in two ranges, to either 31.07 dB (×35.8) or 50 dB (×358), or may be set to any range in between using one external resistor between Pins 5 and 7. Somewhat higher gain can be obtained by connecting the resistor from Pin 5 to common, but the increase in output offset voltage limits the maximum gain to about 60 dB. For any given range, the bandwidth is independent of the voltage-controlled gain. This system provides an under- an over-range of 1.07 dB in all cases; for example, the overall gain is −11.07 dB to 31.07 dB in the maximum-bandwidth mode (Pin 5 and Pin 7 strapped).

This *X-AMP* structure has many advantages over former methods of gain-control based on nonlinear elements. Most importantly, the fixed-gain amplifier can use negative feedback to increase its accuracy. Since large inputs are first attenuated, the amplifier input is always small. For example, to deliver a ±1 V output in the −1 dB/+41 dB mode (that is, using a fixed amplifier gain of 41.07 dB) its input is only 8.84 mV; thus the distortion can be very low. Equally important, the small-signal gain and phase response, and thus the pulse response, are essentially independent of gain.

Figure 1 is a simplified schematic. The input attenuator is a seven-section R-2R ladder network, using untrimmed resistors of nominally R= 62.5 Ω, which results in a characteristic resistance of 125 Ω ± 20%. A shunt resistor is included at the input and laser trimmed to establish a more exact input resistance of 100 Ω ± 3%, which ensures accurate operation (gain and HP corner frequency) when used in conjunction with external resistors or capacitors.

The nominal maximum signal at input VINP is 1 V rms (±1.4 V peak) when using the recommended ±5 V supplies, although operation to ±2 V peak is permissible with some increase in HF distortion and feedthrough. *Pin 4 (SIGNAL COMMON) must be connected directly to the input ground; significant impedance in this connection will reduce the gain accuracy.*

The signal applied at the input of the ladder network is attenuated by 6.02 dB by each section; thus, the attenuation to each of the taps is progressively 0 dB, 6.02 dB, 12.04 dB, 18.06 dB, 24.08 dB, 30.1 dB, 36.12 dB and 42.14 dB. A unique circuit technique is employed to interpolate between these tap-points, indicated by the "slider" in Figure 1, thus providing continuous attenuation from 0 dB to 42.14 dB. It will help, in understanding the AD603, to think in terms of a mechanical means for moving this slider from left to right; in fact, its "position" is controlled by the voltage between Pins 1 and 2. The details of the gain-control interface are discussed later.

The gain is at all times very exactly determined, and a linear-in-dB relationship is automatically guaranteed by the exponential nature of the attenuation in the ladder network (the X-AMP principle). In practice, the gain deviates slightly from the ideal law, by about ±0.2 dB peak (see, for example, Figure 16).

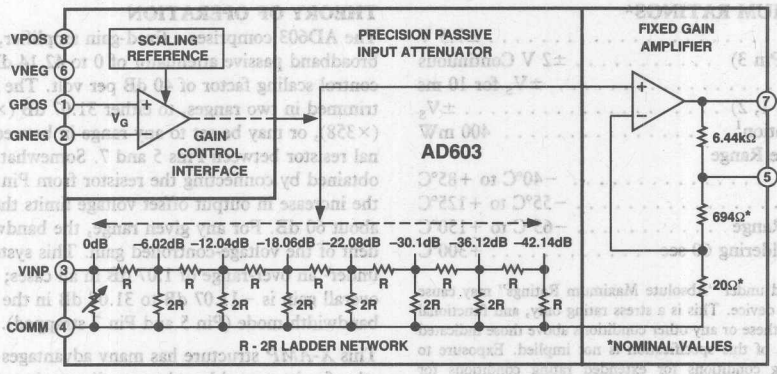


Figure 1. Simplified Block Diagram of the AD603

Noise Performance

An important advantage of the X-AMP is its superior noise performance. The nominal resistance seen at inner tap points is 41.7 Ω (one third of 125 Ω), which exhibits a Johnson noise-spectral density (NSD) of 0.83 nV/$\sqrt{\text{Hz}}$ (that is, $\sqrt{4kTR}$) at 27°C, which is a large fraction of the total input noise. The first stage of the amplifier contributes a further 1 nV/$\sqrt{\text{Hz}}$, for a total input noise of 1.3 nV/$\sqrt{\text{Hz}}$. It will be apparent that it is essential to use a low resistance in the ladder network to achieve the very low specified noise level. The signal's source impedance forms a voltage divider with the AD603's 100 Ω input resistance. In some applications, the resulting attenuation may be unacceptable, requiring the use of an external buffer or preamplifier to match a high impedance source to the low impedance AD603.

The noise at maximum gain (that is, at the 0 dB tap) depends on whether the input is short-circuited or open-circuited: when shorted, the minimum NSD of slightly over 1 nV/$\sqrt{\text{Hz}}$ is achieved; when open, the resistance of 100 Ω looking into the first tap generates 1.29 nV/$\sqrt{\text{Hz}}$, so the noise increases to a total of 1.63 nV/$\sqrt{\text{Hz}}$. (This last calculation would be important if the AD603 were preceded by, for example, a 900 Ω resistor to allow operation from inputs up to 10 V rms.) As the selected tap moves away from the input, the dependence of the noise on source impedance quickly diminishes.

Apart from the small variations just discussed, the signal-to-noise (S/N) ratio at the output is essentially independent of the attenuator setting. For example, on the −11 dB/+31 dB range the fixed gain of X35.8 raises the output NSD to 46.5 nV/$\sqrt{\text{Hz}}$. Thus, for the maximum undistorted output of 1 V rms and a 1 MHz bandwidth, the output S/N ratio would be 86.6 dB, that is, 20 log (1 V/46.5 μV).

The Gain-Control Interface

The attenuation is controlled through a differential, high-impedance (50 MΩ) input, with a scaling factor which is laser-trimmed to 40 dB per volt, that is, 25 mV/dB. An internal bandgap reference ensures stability of the scaling with respect to supply and temperature variations.

When the differential input voltage V_G = 0 V, the attenuator "slider" is centered, providing an attenuation of 21.07 dB. For the maximum bandwidth range, this results in an overall gain of 10 dB (= −21.07 dB + 31.07 dB). When the control input is −500 mV, the gain is lowered by 20 dB (= 0.500 V × 40 dB/V), to −10 dB; when set to +500 mV, the gain is increased by 20 dB, to 30 dB. When this interface is overdriven in either direction, the gain approaches either −11.07 dB (= −42.14 dB + 31.07 dB) or 31.07 dB (= 0 + 31.07 dB), respectively. The only constraint on the gain-control voltage is that it be kept within the common-mode range (−1.2 V to +2.0 V assuming +5 V supplies) of the gain control interface.

The basic gain of the AD603 can thus be calculated using the following simple expression:

$$Gain\ (dB) = 40\ V_G + 10 \qquad \text{Eq. (1)}$$

where V_G is in volts. When Pins 5 and 7 are strapped (see next section) the gain becomes

$$Gain\ (dB) = 40\ V_G + 20\ for\ 0\ to\ +40\ dB$$

and

$$Gain\ (dB) = 40\ V_G + 30\ for\ +10\ to\ +50\ dB \qquad \text{Eq. (2)}$$

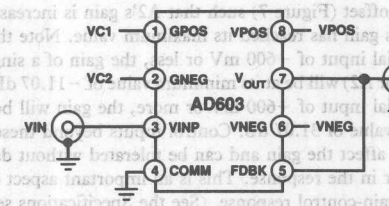
The high impedance gain-control input ensures minimal loading when driving many amplifiers in multiple channel or cascaded applications. The differential capability provides flexibility in choosing the appropriate signal levels and polarities for various control schemes.

For example, if the gain is to be controlled by a DAC providing a positive only ground-referenced output, the "Gain Control LO" (GNEG) pin should be biased to a fixed offset of +500 mV, to set the gain to −10 dB when "Gain Control HI" (GPOS) is at zero, and to 30 dB when at +1.00 V.

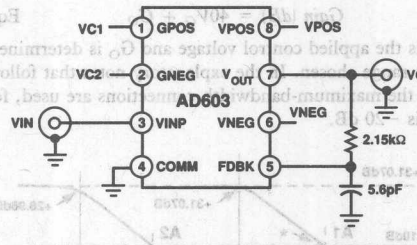
It is a simple matter to include a voltage divider to achieve other scaling factors. When using an 8-bit DAC having a FS output of +2.55 V (10 mV/bit), a divider ratio of 2 (generating 5 mV/bit) would result in a gain-setting resolution of 0.2 dB/bit. The use of such offsets is valuable when two AD603s are cascaded, when various options exist for optimizing the S/N profile, as will be shown later.

Programming the Fixed-Gain Amplifier Using Pin Strapping

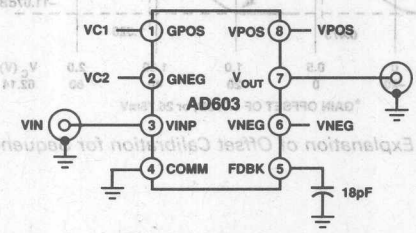
Access to the feedback network is provided at Pin 5 (FDBK). The user may program the gain of the AD603's output amplifier using this pin, as shown in Figure 2. There are three modes: in the default mode, FDBK is unconnected, providing the range +9 dB/+51 dB; when V_{OUT} and FDBK are shorted, the gain is lowered to −11 dB/+31 dB; when an external resistor is placed between V_{OUT} and FDBK any intermediate gain can be achieved, for example, −1 dB/+41 dB. Figure 3 shows the nominal maximum gain versus external resistor for this mode.



a. −10 dB to +30 dB; 90 MHz Bandwidth



b. 0 dB to 40 dB; 45 MHz Bandwidth



c. +10 dB to 50 dB; 9 MHz Bandwidth

Figure 2. Pin Strapping to Set Gain

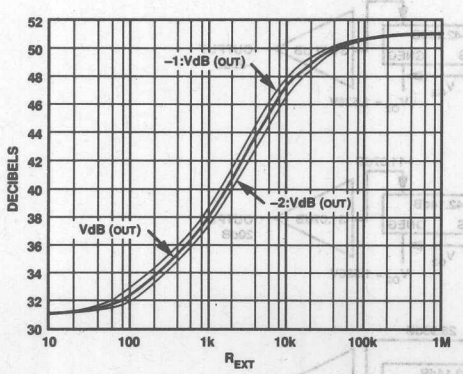


Figure 3. Gain vs. R_{EXT}, Showing Worst-Case Limits Assuming Internal Resistors Have a Maximum Tolerance of 20%

Optionally, when a resistor is placed from FDBK to COMM, higher gains can be achieved. This fourth mode is of limited value because of the low bandwidth and the elevated output offsets; it is thus not included in Figure 2.

The gain of this amplifier in the first two modes is set by the ratio of on-chip laser-trimmed resistors. While the ratio of these resistors is very accurate, the absolute value of these resistors can vary by as much as ±20%. Thus, when an external resistor is connected in parallel with the nominal 6.44 kΩ ± 20% internal resistor, the overall gain accuracy is somewhat poorer. The worst-case error occurs at about 2 kΩ (see Figure 4).

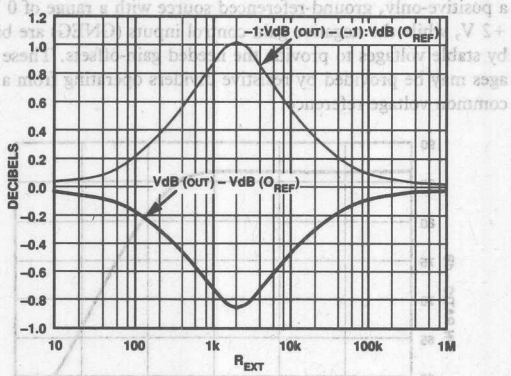


Figure 4. Worst-Case Gain Error, Assuming Internal Resistors Have a Maximum Tolerance of −20% (Top Curve) or +20% (Bottom Curve)

While the gain-bandwidth product of the fixed-gain amplifier is about 4 GHz, the actual bandwidth is not exactly related to the maximum gain. This is because there is a slight enhancing of the ac response magnitude on the maximum bandwidth range, due to higher order poles in the open-loop gain function; this mild peaking is not present on the higher gain ranges. Figure 2 shows how optional capacitors may be added to extend the frequency response in high gain modes.

CASCADING TWO AD603s

Two or more AD603s can be connected in series to achieve higher gain. Invariably, ac coupling must be used to prevent the dc offset voltage at the output of each amplifier from overloading the following amplifier at maximum gain. The required high pass coupling network will usually be just a capacitor, chosen to set the desired corner frequency in conjunction with the well-defined 100 Ω input resistance of the following amplifier.

For two AD603s, the total gain-control range becomes 84 dB (two times 42.14 dB); the overall −3 dB bandwidth of cascaded stages will be somewhat reduced. Depending on the pin-strapping, the gain and bandwidth for two cascaded amplifiers can range from −22 dB to +62 dB (with a bandwidth of about 70 MHz) to +22 dB to +102 dB (with a bandwidth of about 6 MHz).

There are several ways of connecting the gain-control inputs in cascaded operation. The choice depends on whether it is important to achieve the highest possible Instantaneous Signal-to-Noise Ratio (ISNR), or, alternatively, to minimize the ripple in the gain error. The following examples feature the AD603 programmed for maximum bandwidth; the explanations apply to other gain/bandwidth combinations with appropriate changes to the arrangements for setting the maximum gain.

In the sequential mode of operation, the ISNR is maintained at its highest level for as much of the gain control range possible. Figure 5, shows the SNR over a gain range of −22 dB to +62 dB, assuming an output of 1 V rms and a 1 MHz bandwidth; Figure 6 shows the general connections to accomplish this. Here, both the positive gain-control inputs (GPOS) are driven in parallel by a positive-only, ground-referenced source with a range of 0 V to +2 V, while the negative gain-control inputs (GNEG) are biased by stable voltages to provide the needed gain-offsets. These voltages may be provided by resistive dividers operating from a common voltage reference.

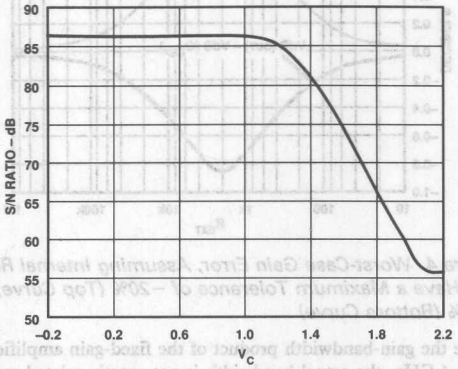


Figure 5. SNR vs. Control Voltage—Sequential Control (1 MHz) Bandwidth)

only after A1's gain has reached its maximum value. Note that for a differential input of −600 mV or less, the gain of a single amplifier (A1 or A2) will be at its minimum value of −11.07 dB; for a differential input of +600 mV or more, the gain will be at its maximum value of 31.07 dB. Control inputs beyond these limits will not affect the gain and can be tolerated without damage or foldover in the response. This is an important aspect of the AD603's gain-control response. (See the Specifications section of this data sheet for more details on the allowable voltage range). The gain is now

$$Gain\ (dB) = 40V_G + G_O \qquad \text{Eq. (3)}$$

where V_G is the applied control voltage and G_O is determined by the gain range chosen. In the explanatory notes that follow, we assume the maximum-bandwidth connections are used, for which G_O is −20 dB.

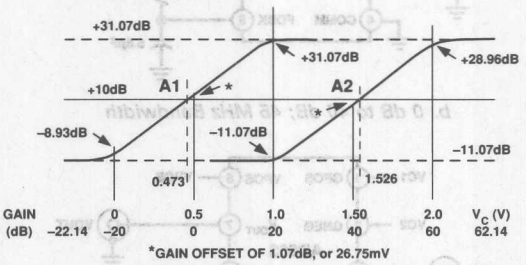


Figure 7. Explanation of Offset Calibration for Sequential Control

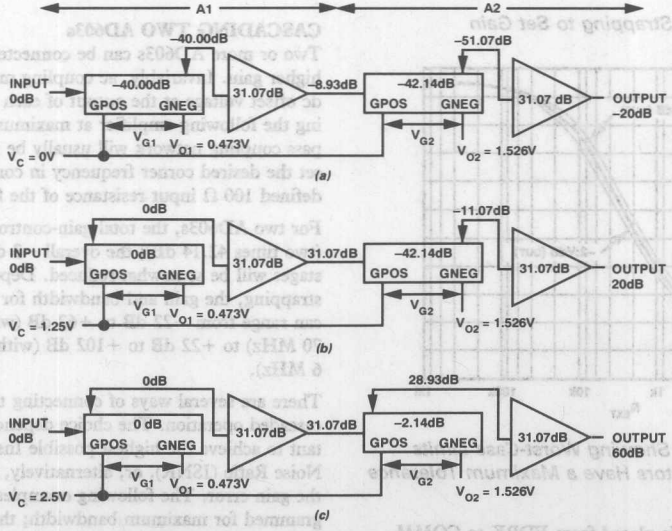


Figure 6. AD603 Gain Control Input Calculations for Sequential Control Operation

With reference to Figure 6, note that V_{G1} refers to the differential gain-control input to A1 and V_{G2} refers to the differential gain-control input to A2. When V_G is zero, $V_{G1} = -473$ mV and thus the gain of A1 is −8.93 dB (recall that the gain of each individual amplifier in the maximum-bandwidth mode is −10 dB for $V_G = -500$ mV and 10 dB for $V_G = 0$ V); meanwhile, VG2 = −1.908 V so the gain of A2 is "pinned" at −11.07 dB. The overall gain is thus −20 dB. This situation is shown in Figure 6a.

When $V_G = +1.00$ V, $V_{G1} = 1.00$ V − 0.473 V = +0.526 V, which sets the gain of A1 to at nearly its maximum value of 31.07 dB, while $V_{G2} = 1.00$ V − 1.526 V = −0.526 V, which sets A2's gain at nearly its minimum value −11.07 dB. Close analysis shows that the degree to which neither AD603 is completely pushed to its maximum or minimum gain exactly cancels in the overall gain, which is now +20 dB. This is depicted in Figure 6b.

When $V_G = +2.0$ V, the gain of A1 is pinned at 31.07 dB and that of A2 is near its maximum value of 28.93 dB, resulting in an overall gain of 60 dB (see Figure 6c). This mode of operation is further clarified by Figure 8, which is a plot of the separate gains of A1 and A2 and the overall gain versus the control voltage. Figure 9 is a plot of the gain error of the cascaded amplifiers versus the control voltage. Figure 10 is a plot of the gain error of the cascaded stages versus the control voltages.

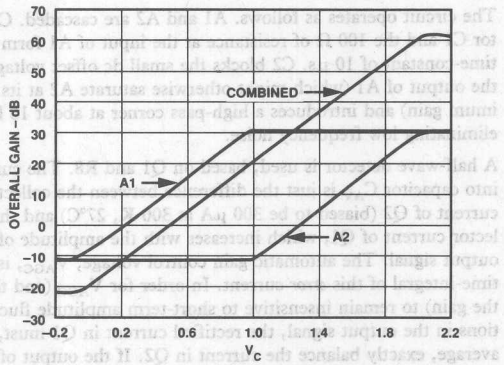


Figure 8. Plot of Separate and Overall Gains in Sequential Control

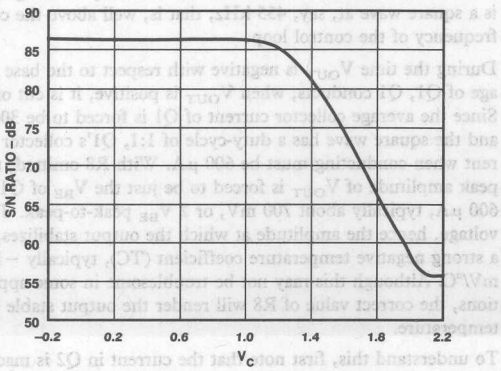


Figure 9. SNR for Cascaded Stages—Sequential Control

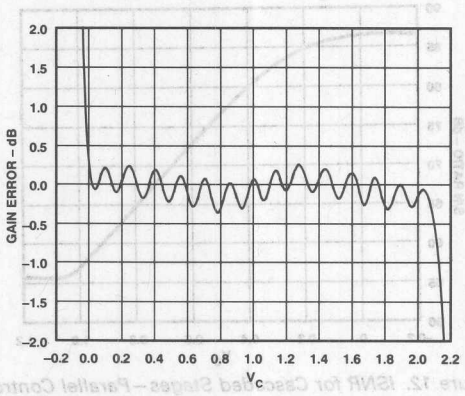


Figure 10. Gain Error for Cascaded Stages—Sequential Control

Parallel Mode (Simplest Gain-Control Interface)
In this mode, the gain-control of voltage is applied to both inputs in parallel—the GPOS pins of both A1 and A2 are connected to the control voltage and the GNEW inputs are grounded. The gain scaling is then doubled to 80dB/V, requiring only a 1.00 V change for an 80 dB change of gain:

$$Gain\ (dB) = 80\ V_G + G_O \qquad \text{Eq. (4)}$$

where, as before G_O depends on the range selected; for example, in the maximum-bandwidth mode, G_O is +20 dB. Alternatively, the GNEG pins may be connected to an offset voltage of +0.500 V, in which case, G_O is −20 dB.

The amplitude of the gain ripple in this case is also doubled, as shown in Figure 11, while the instantaneous signal-to-noise ratio at the output of A2 now decreases linearly as the gain increased (Figure 12).

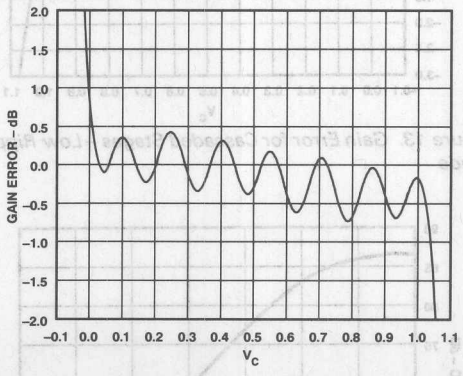


Figure 11. Gain Error for Cascaded Stages—Parallel Control

Low Gain Ripple Mode (Minimum Gain Error)
As can be seen from Figures 9 and 10, the error in the gain is periodic, that is, it shows a small ripple. (Note that there is also a variation in the *output offset voltage*, which is due to the gain

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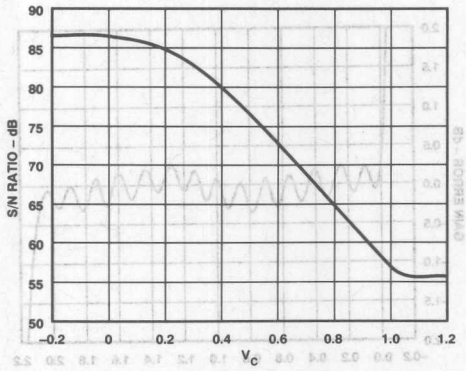


Figure 12. ISNR for Cascaded Stages—Parallel Control

interpolation, but this is not exact in amplitude.) By offsetting the gains of A1 and A2 by half the period of the ripple, that is, by 3 dB, the residual gain errors of the two amplifiers can be made to cancel. Figure 13 shows that much lower gain ripple when configured in this manner. Figure 14 plots the ISNR as a function of gain; it is very similar to that in the "Parallel Mode."

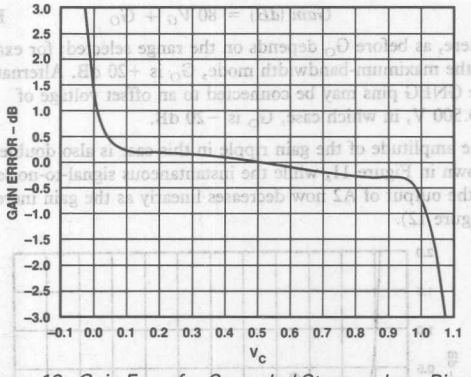


Figure 13. Gain Error for Cascaded Stages—Low Ripple Mode

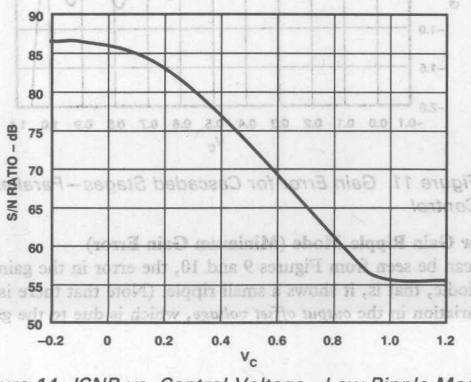


Figure 14. ISNR vs. Control Voltage—Low Ripple Mode

THEORY OF THE AD603

A Low Noise AGC Amplifier

Figure 15 shows the ease with which the AD603 can be connected as an AGC amplifier. The circuit illustrates many of the points previously discussed: It uses few parts, has linear-in-dB gain, operates from a single supply, uses two cascaded amplifiers in sequential gain mode for maximum S/N ratio, and an external resistor programs each amplifier's gain. It also uses a simple temperature-compensated detector.

The circuit operates from a single 10 V supply. Resistors R1, R2 and R3, R4 bias the common pins of A1 and A2 at 5 V. This pin is a low impedance point and must have a low impedance path to ground, here provided by the 100 μF tantalum capacitors and the 0.1 μF ceramic capacitors.

The cascaded amplifiers operate in sequential gain. Here, the offset voltage between the pins 2 (GNEG) of A1 and A2 is 1.05 V (42.14 dB × 25 mV/dB), provided by a voltage divider consisting of resistors R5, R6, and R7. Using standard values, the offset is not exact but it is not critical for this application.

The gain of both A1 and A2 is programmed by resistors R13 and R14, respectively, to be about 42 dB; thus the maximum gain of the circuit is twice that, or 84 dB. The gain-control range can be shifted up by as much as 20 dB by appropriate choices of R13 and R14.

The circuit operates as follows. A1 and A2 are cascaded. Capacitor C1 and the 100 Ω of resistance at the input of A1 form a time-constant of 10 μs. C2 blocks the small dc offset voltage at the output of A1 (which might otherwise saturate A2 at its maximum gain) and introduces a high-pass corner at about 16 kHz, eliminating low frequency noise.

A half-wave detector is used, based on Q1 and R8. The current into capacitor C_{AV} is just the difference between the collector current of Q2 (biased to be 300 μA at 300 K, 27°C) and the collector current of Q1, which increases with the amplitude of the output signal. The automatic gain control voltage, V_{AGC}, is the time-integral of this *error* current. In order for V_{AGC} (and thus the gain) to remain insensitive to short-term amplitude fluctuations in the output signal, the rectified current in Q1 must, on average, exactly balance the current in Q2. If the output of A2 is too small to do this, V_{AGC} will increase, causing the gain to increase, until Q1 conducts sufficiently.

Consider the case where R8 is zero and the output voltage V_{OUT} is a square wave at, say, 455 kHz, that is, well above the corner frequency of the control loop.

During the time V_{OUT} is negative with respect to the base voltage of Q1, Q1 conducts; when V_{OUT} is positive, it is cut off. Since the average collector current of Q1 is forced to be 300 μA, and the square wave has a duty-cycle of 1:1, Q1's collector current when conducting must be 600 μA. With R8 omitted, the peak amplitude of V_{OUT} is forced to be just the V_{BE} of Q1 at 600 μA, typically about 700 mV, or 2 V_{BE} peak-to-peak. This voltage, hence the amplitude at which the output stabilizes, has a strong negative temperature coefficient (TC), typically −1.7 mV/°C. Although this may not be troublesome in some applications, the correct value of R8 will render the output stable with temperature.

To understand this, first note that the current in Q2 is made to be proportional to absolute temperature (PTAT). For the moment, continue to assume that the signal is a square wave.

When Q1 is conducting, V_{OUT} is now the sum of V_{BE} and a voltage which is PTAT and which can be chosen to have an equal but opposite TC to that of the V_{BE}. This is actually nothing more than an application of the "bandgap voltage reference" principle. When R8 is chosen such that the sum of the voltage across it and the V_{BE} of Q1 is close to the bandgap voltage of about 1.2 V, V_{OUT} will be stable over a wide range of temperatures, provided, of course, that Q1 and Q2 share the same thermal environment.

Since the average emitter current is 600 μA during each half-cycle of the square wave a resistor of 833 Ω would add a PTAT voltage of 500 mV at 300 K, increasing by 1.66 mV/°C. In practice, the optimum value will depend on the type of transistor used, and, to a lesser extent, on the waveform for which the temperature stability is to be optimized; for the inexpensive 2N3904/2N306 pair and sine wave signals, the recommended value is 806 Ω.

This resistor also serves to lower the peak current in Q1 when more typical signals (usually, sinusoidal) are involved, and the 1.8 kHz LP filter it forms with C_{AV} helps to minimize distortion due to ripple in VAGC. Note that the output amplitude under sinewave conditions will be higher than for a square wave, since the average value of the current *for an ideal rectifier* would be 0.637 times as large, causing the output amplitude to be 1.88 (=1.2/0.637) V, or 1.33 V rms. In practice, the somewhat nonideal rectifier results in the sine wave output being regulated to about 1.4 V rms, or 3.6 V p-p.

The bandwidth of the circuit exceeds 40 MHz. At 10.7 MHz, the AGC threshold is 100 μV (−67 dBm) and its maximum gain is 83 dB (20 log 1.4V/100 μV). The circuit holds its output at 1.4 V rms for inputs as low as −67 dBm to +15 dBm (82 dB), where the input signal exceeds the AD603's maximum input rating. For a −30 dBm input at 10.7 MHz, the second harmonic is 34 dB down from the fundamental and the third harmonic is 35 dB down.

CAUTION

Careful component selection, circuit layout, power-supply decoupling, and shielding are needed to minimize the AD603's susceptibility to interference from radio and TV stations, etc. In bench evaluation, we recommend placing all of the components in a shielded box and using feedthrough decoupling networks for the supply voltage. Circuit layout and construction are also critical, since stray capacitances and lead inductances can form resonant circuits and are a potential source of circuit peaking, oscillation, or both.

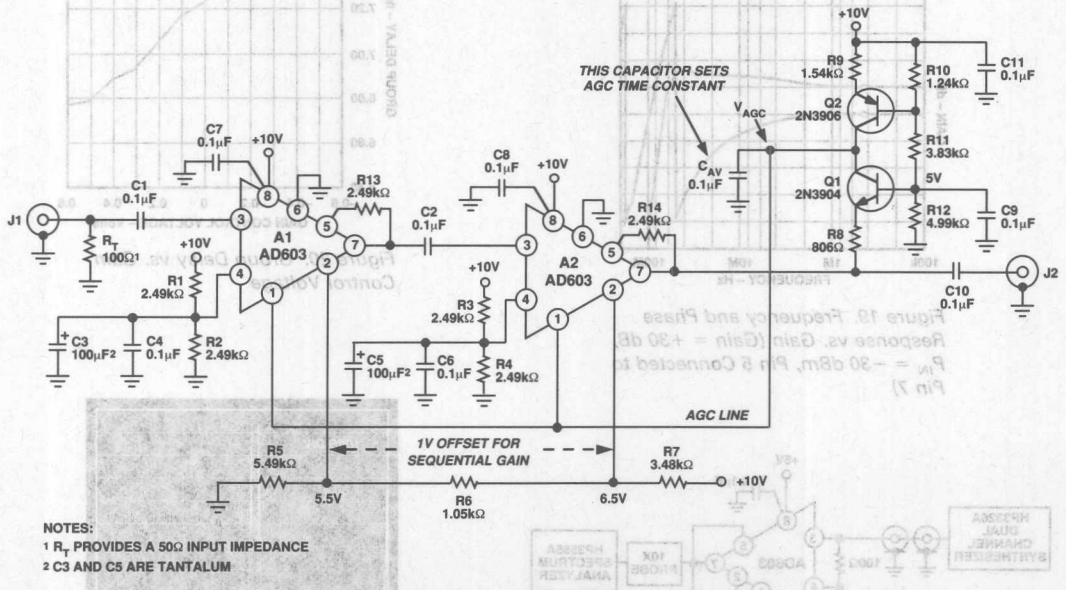


Figure 15. A Low Noise AGC Amplifier

AD603—Typical Characteristics

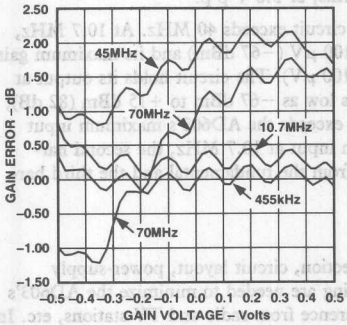


Figure 16. Gain Error vs. Gain Control Voltage at 455 kHz, 10.7 MHz, 45 MHz, 70 MHz

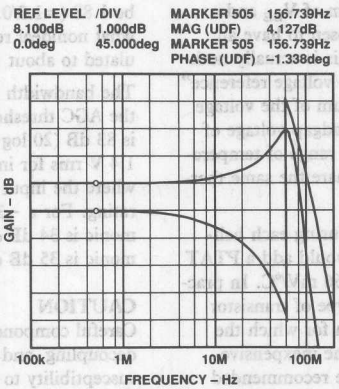


Figure 17. Frequency and Phase Response vs. Gain (Gain = −10 dB, P_{IN} = −30 dBm, Pin 5 Connected to Pin 7)

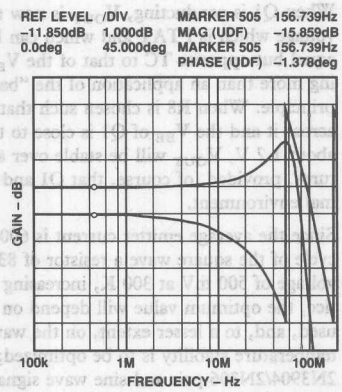


Figure 18. Frequency and Phase Response vs. Gain (Gain = +10 dB, P_{IN} = −30 dBm, Pin 5 Connected to Pin 7)

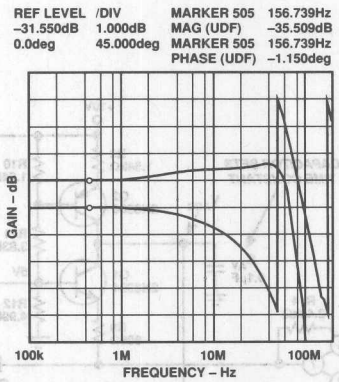


Figure 19. Frequency and Phase Response vs. Gain (Gain = +30 dB, P_{IN} = −30 dBm, Pin 5 Connected to Pin 7)

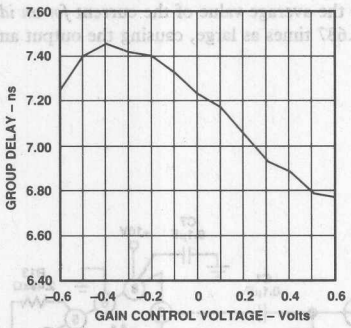


Figure 20. Group Delay vs. Gain Control Voltage

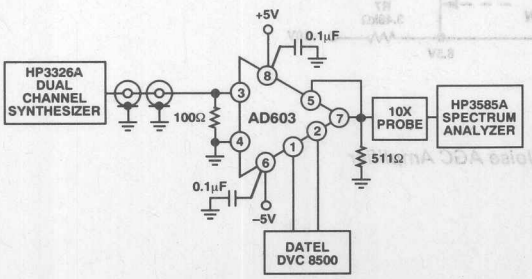


Figure 21. Third Order Intermodulation Distortion Test Setup

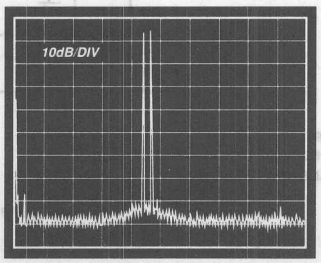


Figure 22. Third Order Intermodulation Distortion at 455 kHz (10× Probe Used to HP3585A Spectrum Analyzer, Gain = 0 dB, P_{IN} = 0 dBm, Pin 5 Connected to Pin 7)

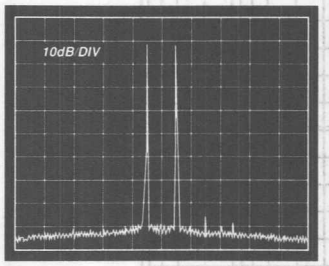


Figure 23. Third Order Intermodulation Distortion at 10.7 MHz (10× Probe Used to HP3585A Spectrum Analyzer, Gain = 0 dB, P_{IN} = 0 dBm, Pin 5 Connected to Pin 7)

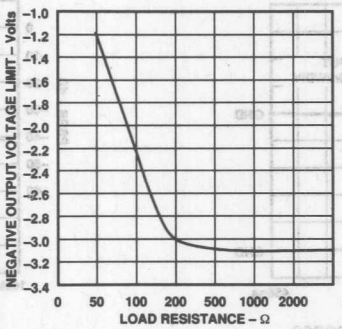


Figure 24. Typical Output Voltage Swing vs. Load Resistance (Negative Output Swing Limits First)

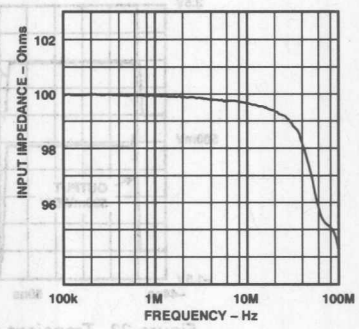


Figure 25. Input Impedance vs. Frequency (Gain = −10 dB)

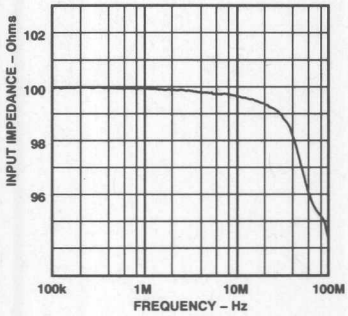


Figure 26. Input Impedance vs. Frequency (Gain = +10 dB)

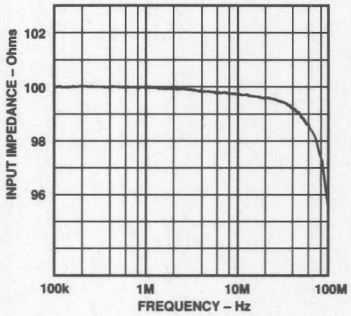


Figure 27. Input Impedance vs. Frequency (Gain = +30 dB)

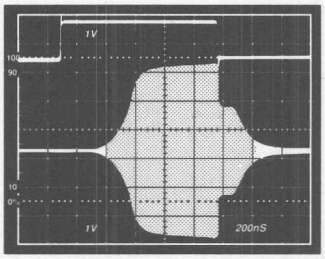


Figure 28. Gain-Control Channel Response Time

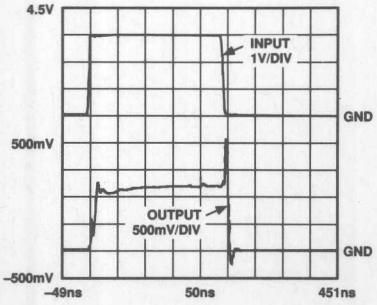


Figure 29. Input Stage Overload Recovery Time, Pin 5 Connected to Pin 7 (Input Is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

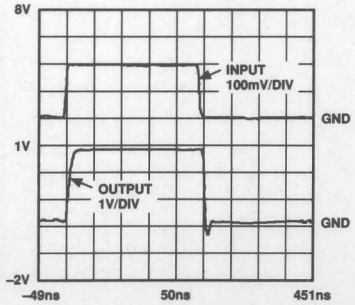


Figure 30. Output Stage Overload Recovery Time, Pin 5 Connected to Pin 7 (Input is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

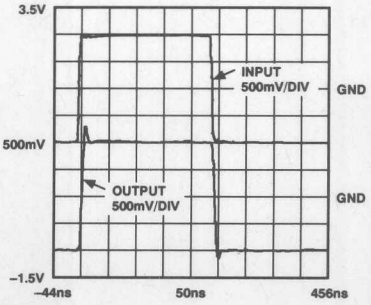


Figure 31. Transient Response, G = 0 dB, Pin 5 Connected to Pin 7 (Input is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

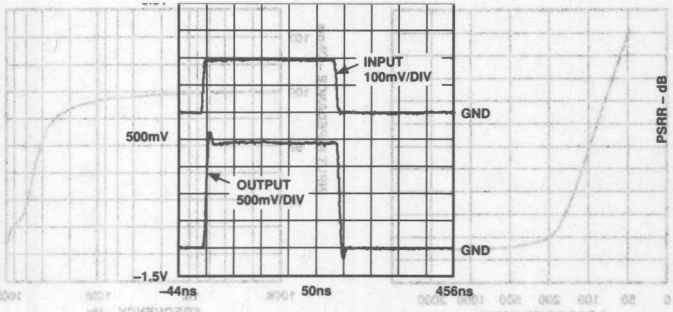


Figure 32. Transient Response, G = +20 dB, Pin 5 Connected to Pin 7 (Input is 500 ns Period, 50% Duty-Cycle Square Ware, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

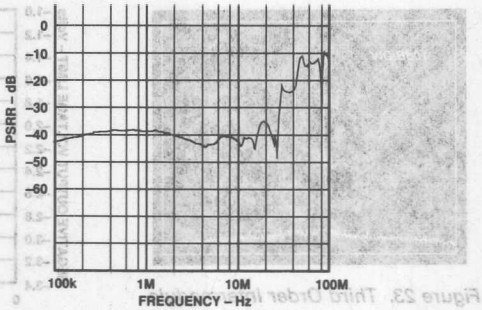


Figure 33. PSRR vs. Frequency (Worst-Case is Negative Supply PSRR, Shown Here)

50 MHz, 80 dB Demodulating Logarithmic Amplifier with Limiter Output

AD606

FEATURES

Logarithmic Amplifier Performance
- −75 dBm to +5 dBm Dynamic Range
- ≤1.5nV/√Hz Input Noise
- Usable to >50 MHz
- 37.5 mV/dB Voltage Output
- On-Chip Low-Pass Output Filter

Limiter Performance
- ±1 dB Output Flatness over 80 dB Range
- ±3° Phase Stability at 10.7 MHz over 80 dB Range
- Adjustable Output Amplitude

Low Power
- +5 V Single Supply Operation
- 65 mW Typical Power Consumption
- CMOS Compatible Power-Down to 325 μW typ
- <5 μs Enable/Disable Time

APPLICATIONS

- Ultrasound and Sonar Processing
- Phase-Stable Limiting Amplifier to 100 MHz
- Received Signal Strength Indicator (RSSI)
- Wide Range Signal and Power Measurement

PRODUCT DESCRIPTION

The AD606 is a complete, monolithic logarithmic amplifier using a 9-stage "successive-detection" technique. It provides both logarithmic and limited outputs. The logarithmic output is from a three-pole post-demodulation low-pass filter and provides a loadable output voltage of +0.1 V dc to +4 V dc. The logarithmic scaling is such that the output is +0.5 V for a sinusoidal input of −75 dBm and +3.5 V at an input of +5 dBm; over this range the logarithmic linearity is typically within ±0.4 dB. All scaling parameters are proportional to the supply voltage.

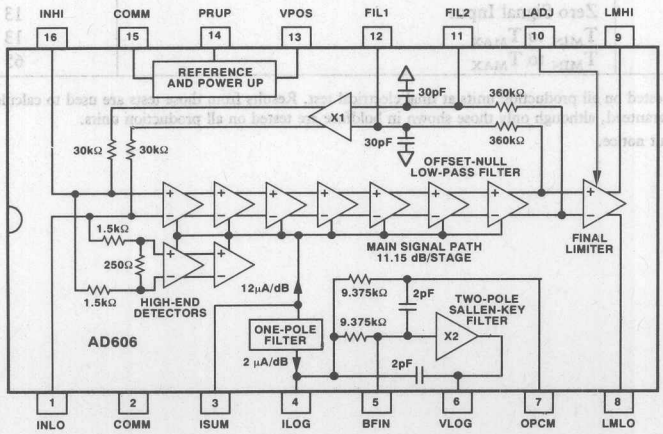
The AD606 can operate above and below these limits, with reduced linearity, to provide as much as 90 dB of conversion range. A second low-pass filter automatically nulls the input offset of the first stage down to the submicrovolt level. Adding external capacitors to both filters allows operation at input frequencies as low as a few hertz.

The AD606's limiter output provides a hard-limited signal output as a differential current of ±1.2 mA from open-collector outputs. In a typical application, both of these outputs are loaded by 200 Ω resistors to provide a voltage gain of more than 90 dB from the input. Transition times are 1.5 ns, and the phase is stable to within ±3° at 10.7 MHz for signals from −75 dBm to +5 dBm.

The logarithmic amplifier operates from a single +5 V supply and typically consumes 65 mW. It is enabled by a CMOS logic-level voltage input, with a response time of <5 μs. When disabled, the standby power is reduced to <1 mW within 5 μs.

The AD606J is specified for the commercial temperature range of 0°C to +70°C and is available in 16-pin plastic DIPs or SOICs. Consult the factory for other packages and temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



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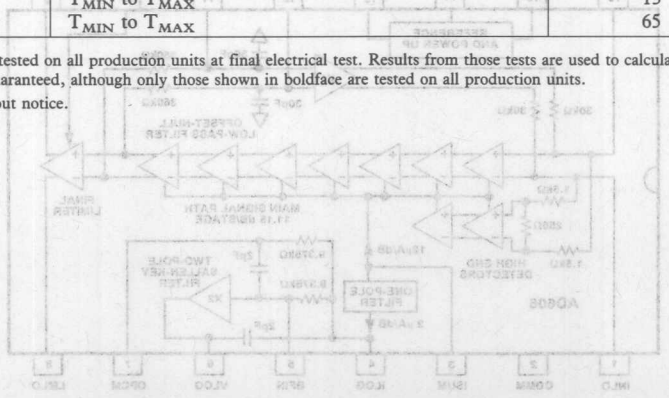
AD606—SPECIFICATIONS (T_A = +25°C and supply = +5 V unless otherwise noted; dBm assumes 50 Ω)

Model		AD606J			
Parameter	Conditions	Min	Typ	Max	Units
SIGNAL INPUT					
Log Amp f_{MAX}	AC Coupled; Sinusoidal Input		50		MHz
Limiter f_{MAX}	AC Coupled; Sinusoidal Input		100		MHz
Dynamic Range			80		dB
Input Resistance	Differential Input	500	2,500		Ω
Input Capacitance	Differential Input		2		pF
SIGNAL OUTPUT					
Limiter Flatness	−75 dBm to +5 dBm Input Signal at 10.7 MHz With Pin 9 to V_{POS} via a 200 Ω Resistor and Pin 8 to V_{POS} via a 200 Ω Resistor	−1.5		+1.5	dB
Output Current	At Pins 8 or 9, Proportional to V_{POS}, LADJ Grounded		1.2		mA
	LADJ Open Circuited		0.48		mA
Phase Variation with Input Level	−75 dBm to +5 dBm Input Signal at 10.7 MHz		±3		°
LOG (RSSI) OUTPUT					
Nominal Slope	At 10.7 MHz; (0.0075 × V_{POS})/dB		37.5		mV/dB
	At 45 MHz		35		mV/dB
Slope Accuracy	Untrimmed at 10.7 MHz	−15	±5	+15	%
Intercept	Sinusoidal Input; Independent of V_{POS}		−88.33		dBm
Logarithmic Conformance	−75 dBm to +5 dBm Input Signal at 10.7 MHz	−1.5	0.4	+1.5	dB
Nominal Output	Input Level = −75 dBm		0.5		V
	Input Level = −35 dBm		2		V
	Input Level = +5 dBm		3.5		V
Accuracy over Temperature	After Calibration at −35 dBm at 10.7 MHz T_{MIN} to T_{MAX}	−3		3	dB
Video Response Time	From Onset of Input Signal Until Output Reaches 95% of Final Value		400		ns
POWER-DOWN INTERFACE					
Power-Up Response Time	Time Delay Following HI Transition Until Device Meets Full Specifications AC Coupled with 100 pF Coupling Capacitors		3.5		µs
Input Bias Current	Logical HI Input (See Figure 12)		1		nA
	Logical LO Input		4		µA
POWER SUPPLY					
Operating Range		4.5		5.5	V
Powered-Up Current	Zero Signal Input		13		mA
	T_{MIN} to T_{MAX}		13	20	mA
Powered-Down Current	T_{MIN} to T_{MAX}		65	200	µA

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage V_{POS} . . . . . +9 V
Internal Power Dissipation[1] . . . . . 600 mW
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature, Soldering 60 sec . . . . . +300°C

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

[1]Thermal Characteristics:
16-Pin Plastic DIP Package: θ_{JA} = 85°C/W
16-Pin SOIC Package: θ_{JA} = 100°C/W

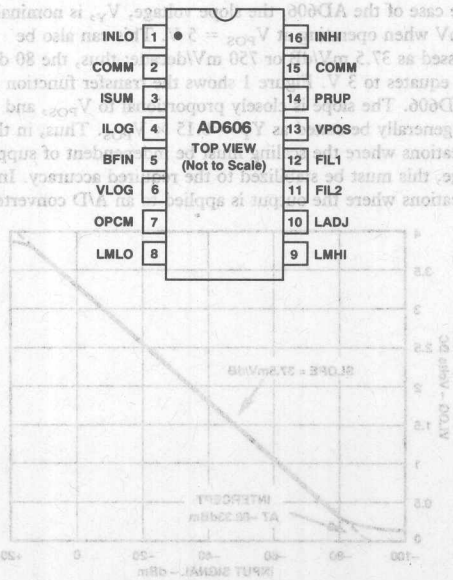
ORDERING GUIDE

Model	Temperature Range	Package*
AD606JN	0°C to +70°C	16-Pin Plastic DIP (N-16)
AD606JR	0°C to +70°C	16-Pin Narrow-Body SOIC (R-16A)

*For outline information see Package Information section.

CONNECTION DIAGRAM

Plastic DIP (N) and Small Outline (R) Packages



PIN FUNCTIONS

Pin	Mnemonic	Function
1	INLO	DIFFERENTIAL RF INPUT −75 dBm to +5 dBm, Inverting, AC Coupled.
2	COMM	POWER SUPPLY COMMON Connect to Ground.
3	ISUM	LOG DETECTOR SUMMING NODE
4	ILOG	LOG CURRENT OUTPUT Normally No Connection; 2 μA/dB Output Current.
5	BFIN	BUFFER INPUT Optionally Used to Realize Low Frequency Post-Demodulation Filters.
6	VLOG	BUFFERED LOG OUTPUT 37.5 mV/dB (100 mV to 4.5 V).
7	OPCM	OUTPUT COMMON Connect to Ground.
8	LMLO	DIFFERENTIAL LIMITER OUTPUT 1.2 mA Full-Scale Output Current. Open Collector Output Must Be "Pulled" Up to VPOS with R ≤ 400 Ω.
9	LMHI	DIFFERENTIAL LIMITER OUTPUT 1.2 mA Full-Scale Output Current. Open Collector Output Must Be "Pulled" Up to VPOS with R ≤ 400 Ω.
10	LADJ	LIMITER LEVEL ADJUSTMENT Optionally Used to Adjust Limiter Output Current.
11	FIL1	OFFSET LOOP LOW-PASS FILTER Normally No Connection; a Capacitor Between FIL1 and FIL2 May Be Added to Lower the Filter Cutoff Frequency.
12	FIL2	OFFSET LOOP LOW-PASS FILTER Normally No Connection; See Above.
13	VPOS	POSITIVE SUPPLY Connect to +5 V at 13 mA.
14	PRUP	POWER UP CMOS (5 V) Logical High = Device On (≈ 65 mW). CMOS (0 V) Logical Low = Device Off (≈ 325 μW).
15	COMM	POWER SUPPLY COMMON Connect to Ground.
16	INHI	DIFFERENTIAL RF INPUT −75 dBm to +5 dBm, Noninverting, AC Coupled.

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dBm, meaning decibels with respect to 1 mW. Unfortunately, this is not precise for several reasons.

1. Log amps respond not to power but to voltage. In this respect, it would be less ambiguous to use "dBV" (decibels referred to 1 V) as the input metric. Also, power is dependent on the rms (root-mean-square) value of the signal, while log amps are not inherently rms responding.
2. The response of a demodulating log amp depends on the waveform. Convention assumes that the input is sinusoidal. However, the AD606 is capable of accurately handling any input waveform, including ac voltages, pulses and square waves, Gaussian noise, and so on. See the AD640 data sheet, which covers the effect of waveform on logarithmic intercept, for more information.
3. The impedance in which the specified power is measured is not always stated. In the log amp context it is invariably assumed to be 50 Ω. Thus, 0 dBm means "1 mW rms in 50 Ω," and corresponds to an rms voltage of $\sqrt{(1\text{ mW} \times 50\ \Omega)}$, or 224 mV.

Popular convention requires the use of dBm to simplify the comparison of log amp specifications. Unless otherwise stated, sinusoidal inputs expressed as dBm in 50 Ω are used to specify the performance of the AD606 throughout this data sheet. We will also show the corresponding rms voltages where it helps to clarify the specification. Noise levels will likewise be given in dBm; the response to Gaussian noise is 0.5 dB higher than for a sinusoidal input of the same rms value.

Note that dynamic range, being a simple ratio, is always specified simply as "dB", and the slope of the logarithmic transfer function is correctly specified as "mV/dB," NOT as "mV/dBm."

LOGARITHMIC SLOPE AND INTERCEPT

A generalized logarithmic amplifier having an input voltage V_{IN} and output voltage V_{LOG} must satisfy a transfer function of the form

$$V_{LOG} = V_Y \log_{10}(V_{IN}/V_X)$$

where, in the case of the AD606, the voltage V_{IN} is the difference between the voltages on pins INHI and INLO, and the voltage V_{LOG} is that measured at the output pin VLOG. V_Y and V_X are fixed voltages that determine the slope and intercept of the logarithmic amplifier, respectively. These parameters are inherent in the design of a particular logarithmic amplifier, although may be adjustable, as in the AD606. When $V_{IN} = V_X$, the logarithmic argument is one, hence the logarithm is zero. V_X is, therefore, called the logarithmic *intercept* voltage because the output voltage V_{LOG} crosses zero for this input. The slope voltage V_Y is can also be interpreted as the "volts per decade" when using base-10 logarithms as shown here.

Note carefully that V_{LOG} and VLOG in the above paragraph (and elsewhere in this data sheet) are different. The first is a voltage; the second is a pin designation.

This equation suggests that the input V_{IN} is a dc quantity, and, if V_X is positive, that V_{IN} must likewise be positive, since the logarithm of a negative number has no simple meaning. In fact, in the AD606, *the response is independent of the sign of* V_{IN} because of the particular way in which the circuit is built. This is part of the demodulating nature of the amplifier, which

The single supply nature of the AD606 results in common-mode level of the inputs INHI and INLO being at about +2.5 V (using the recommended +5 V supply). In normal ac operation, this bias level is developed internally and the input signal is coupled in through dc-blocking capacitors. Any residual dc offset voltage in the first stage limits the logarithmic accuracy for small inputs. In ac operation, this offset is automatically and continuously nulled via a feedback path from the last stage, provided that the pins INHI and INLO are not shorted together, as would be the case if transformer coupling were used for the signal.

While any logarithmic amplifier must eventually conform to the basic equation shown above, which, with appropriate elaboration, can also fully account for the effect of the signal waveform on the effective intercept,[1] it is more convenient in RF applications to use a simpler expression. This simplification results from first, assuming that the input is always sinusoidal, and second, using a decibel representation for the input level. The standard representation of RF levels is (incorrectly, in a log amp context) in terms of power, specifically, decibels above 1 milliwatt (dBm) with a presumed impedance level of 50 Ω. That being the case, we can rewrite the transfer function as

$$V_{LOG} = V_Y (P_{IN} - P_X)$$

where it must be understood that P_{IN} means the sinusoidal input power level in a 50 Ω system, expressed in dBm, and P_X is the intercept, also expressed in dBm. In this case, P_{IN} and P_X are simple, dimensionless numbers. (P_X is sometimes called the "logarithmic offset," for reasons which are obvious from the above equation.) V_Y is still defined as the logarithmic slope, usually specified as so many millivolts per decibel, or mV/dB.

In the case of the AD606, the slope voltage, V_Y, is nominally 750 mV when operating at V_{POS} = 5 V. This can also be expressed as 37.5 mV/dB or 750 mV/decade; thus, the 80 dB range equates to 3 V. Figure 1 shows the transfer function of the AD606. The slope is closely proportional to V_{POS}, and can more generally be stated as $Y_Y = 0.15 \times V_{POS}$. Thus, in those applications where the scaling must be independent of supply voltage, this must be stabilized to the required accuracy. In applications where the output is applied to an A/D converter,

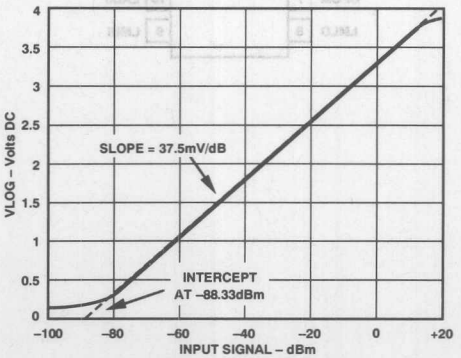

Figure 1. Nominal Transfer Function

[1]See, for example, the AD640 data sheet, which is published in Section 3 of the *Special Linear Reference Manual* or Section 9.3 of the *1992 Amplifier Applications Guide*.

V_{POS}, if possible. The slope is essentially independent of temperature.

The intercept P_X is essentially independent of either the supply voltage or temperature. However, the AD606 is not factory-calibrated, and both the slope and intercept may need to be externally adjusted. Following calibration, the conformance to an ideal logarithmic law will be found to be very close, particularly at moderate frequencies (see Figure 14), and still acceptable at the upper end of the frequency range (Figure 15).

CIRCUIT DESCRIPTION

Figure 2 is a block diagram of the AD606, which is a complete logarithmic amplifier system in monolithic form. It uses a total of nine limiting amplifiers in a "successive detection" scheme to closely approximate a logarithmic response over a total dynamic range of 90 dB (Figure 2). The signal input is differential, at nodes INHI and INLO, and will usually be sinusoidal and ac coupled. The source may be either differential or single-sided; the input impedance is about 2.5 kΩ in parallel with 2 pF. Seven of the amplifier/detector stages handle inputs from −80 dBm (32 μV rms) up to about −14 dBm (45 mV rms). The noise floor is about −83 dBm (18 μV rms). Another two stages receive the input attenuated by 22.3 dB, and respond to inputs up to +10 dBm (707 mV rms). The gain of each of these stages is 11.15 dB and is accurately stabilized over temperature by a precise biasing system.

The detectors provide full-wave rectification of the alternating signal present at each limiter output. Their outputs are in the form of currents, proportional to the supply voltage. Each cell incorporates a low-pass filter pole, as the first step in recovering the average value of the demodulated signal, which contains appreciable energy at even harmonics of the input frequency. A further real pole can be introduced by adding a capacitor between the summing node ISUM and VPOS. The summed detector output currents are applied to a 6:1 reduction current mirror. Its output at ILOG is scaled 2 μA/dB, and is converted to voltage by an internal load resistor of 9.375 kΩ between ILOG and OPCM (output common, which is usually grounded).

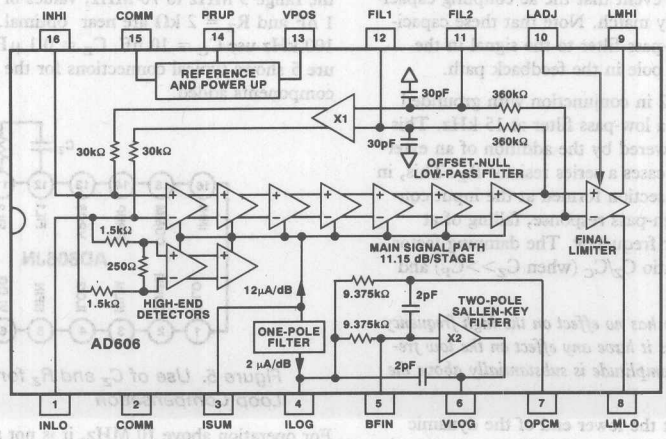

Figure 2. AD606 Simplified Block Diagram

decade).

In applications where V_{LOG} is taken to an A/D converter which allows the use of an external reference, this reference input should also be connected to the same +5 V supply. The power-supply voltage may be in the range +4.5 V to +5.5 V, providing a range of slopes from nominally 33.75 mV/dB (675 mV/decade) to 41.25 mV/dB (825 mV/decade).

A buffer amplifier, having a gain of two, provides a final output scaling at V_{LOG} of 37.5 mV/dB (750 mV/decade). This low-impedance output can run from close to ground to over +4 V (using the recommended +5 V supply) and is tolerant of resistive and capacitive loads. Further filtering is provided by a conjugate pole pair, formed by internal capacitors which are an integral part of the output buffer. The corner frequency of the overall filter is 2 MHz, and the 10%–90% rise time is 150 ns. Later, we will show how the slope and intercept can be altered using simple external adjustments. The direct buffer input BFIN is used in these cases.

The last limiter output is available as complementary currents from open collectors at pins LMHI and LMLO. These currents are each 1.2 mA typical with LADJ grounded and may be converted to voltages using external load resistors connected to VPOS; typically, a 200 Ω resistor is used on just one output. The voltage gain is then over 90 dB, resulting in a hard-limited output for all input levels down to the noise floor. The phasing is such that the voltage at LMHI goes high when the input (INHI to INLO) is positive. The overall delay time from the signal inputs to the limiter outputs is 8 ns. Of particular importance is the phase stability of these outputs versus input level. At 50 MHz, the phase typically remains within ±4° from −70 dBm to +5 dBm. The rise time of this output (essentially a square wave) is about 1.2 ns, resulting in clean operation to more than 70 MHz.

Offset-Control Loop

The offset-control loop nulls the input offset voltage, and sets up the bias voltages at the input pins INHI and INLO. A full understanding of this offset-control loop is useful, particularly

when using larger input coupling capacitors and an external filter capacitor to lower the minimum acceptable operating frequency. The loop's primary purpose is to extend the lower end of the dynamic range in the case where the offset voltage of the first stage should be high enough to cause later stages to prematurely enter limiting, because of the high dc gain (about 8000) of the main amplifier system. For example, an offset voltage of only 20 μV would become 160 mV at the output of the last stage in the main amplifier (before the final limiter section), driving the last stage well into limiting. In the absence of noise, this limiting would simply result in the logarithmic output ceasing to become any lower below a certain signal level at the input. The offset would also degrade the logarithmic conformance in this region. In practice, the finite noise of the first stage also plays a role in this regard, even if the dc offset were zero.

Figure 3 shows a representation of this loop, reduced to essentials. The figure closely corresponds to the internal circuitry, and correctly shows the input resistance. Thus, the forward gain of the main amplifier section is 7 × 11.15 dB, but the loop gain is lowered because of the attenuation in the network formed by

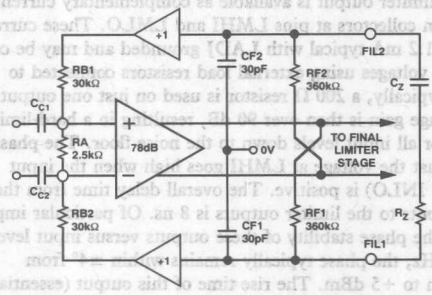

Figure 3. Offset Control Loop

RB1 and RB2 and the input resistance RA. The connection polarity is such as to result in negative feedback, which reduces the input offset voltage by the dc loop gain, here about 50 dB, that is, by a factor of about 316. We use a *differential* representation, because later we will examine the consequences to the power-up response time in the event that the ac coupling capacitors C_{C1} and C_{C2} do not exactly match. Note that these capacitors, as well as forming a high-pass filter to the signal in the forward path, also introduce a pole in the feedback path.

Internal resistors RF1 and RF2 in conjunction with grounded capacitors CF1 and CF2 form a low-pass filter at 15 kHz. This frequency can optionally be lowered by the addition of an external capacitor C_Z, and in some cases a series resistor R_Z. This, in conjunction with the low-pass section formed at the input coupling, results in a two-pole high-pass response, falling of at 40 dB/decade below the corner frequency. The damping factor of this filter depends on the ratio C_Z/C_C (when $C_Z >> C_F$) and also on the value of R_Z.

The inclusion of this control loop has no effect on the high frequency response of the AD606. Nor does it have any effect on the low frequency response when the input amplitude is substantially above the input offset voltage.

The loop's effect is felt only at the lower end of the dynamic range, that is, from about −80 dBm to −70 dBm, and when the signal frequency is near the lower edge of the passband. Thus, the small signal results which are obtained using the suggested model are not indicative of the ac response at moderate to high signal levels. Figure 4 shows the response of this model for the default case (using C_C = 100 pF and C_Z = 0) and with C_Z = 150 pF. In general, a *maximally flat ac* response occurs when C_Z is roughly twice C_C (making due allowance for the internal 30 pF capacitors). Thus, for audio applications, one can use C_C = 2.7 μF and C_Z = 4.7 μF to achieve a high-pass corner (−3 dB) at 25 Hz.

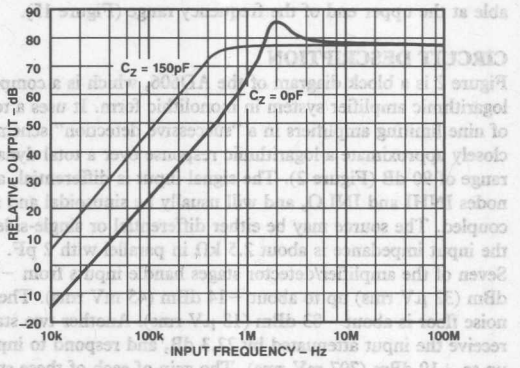

Figure 4. Frequency Response of Offset Control Loop for C_Z = 0 pF and C_Z = 150 pF (C_C = 100 pF)

However, the maximally flat ac response is not optimal in two special cases. First, where the RF input level is rapidly pulsed, the fast edges will cause the loop filter to ring. Second, ringing can also occur when using the power-up feature, and the ac coupling capacitors do not exactly match in value. We will examine the latter case in a moment. Ringing in a linear amplifier is annoying, but in a log amp, with its much enhanced sensitivity to near zero signals, it can be very disruptive.

To optimize the low level accuracy, that is, achieve a highly-damped pulse response in this filter, it is recommended to include a resistor R_Z in series with an increased value of C_Z. Some experimentation may be necessary, but for operation in the range 3 MHz to 70 MHz, values of C_C = 100 pF, C_Z = 1 nF and R_Z = 2 kΩ are near optimal. For operation down to 100 kHz use C_C = 10 nF, C_Z = 0.1 μF and R_Z = 13 kΩ. Figure 5 shows typical connections for the AD606 with these filter components added.

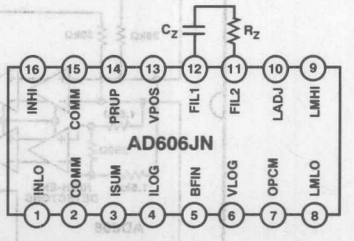

Figure 5. Use of C_Z and R_Z for Offset Control Loop Compensation

For operation above 10 MHz, it is not necessary to add the external capacitors CF1, CF2, and C_Z, although an improvement in low frequency noise can be achieved by so doing (see

APPLICATIONS). Note that the offset control loop does not materially affect the low-frequency cutoff at high input levels, when the offset voltage is swamped by the signal.

Power-Up Interface

The AD606 features a power-saving mode, controlled by the logic level at Pin 14 (PRUP). When powered down, the quiescent current is typically 65 μA, or about 325 μW. A CMOS logical HIGH applied to PRUP activates both internal references, and the system becomes fully functional within about 3.5 μs. When this input is a CMOS logical LOW, the system shuts down to the quiescent level within about 5 μs.

The power-up time is somewhat dependent on the signal level and can be degraded by mismatch of the input coupling capacitors. The explanation is as follows. When the AD606 makes the transition from powered-down to fully active, the dc bias voltage at the input nodes INHI and INLO (about +2.5 V) inevitably changes slightly, as base current in the input transistors flows in the bias resistors. In fact, first-order correction for this is included in the specially designed offset buffer amplifier, but even a few millivolts of change at these inputs represents a significant equivalent "dBm" level.

Now, if the coupling capacitors do not match exactly, some fractional part of this residual voltage step becomes coupled into the amplifier. For example, if there is a 10 % capacitor mismatch, and INHI and INLO jump 20 mV at power-up, there is a 2 mV pulse input to the system, which may cause the offset control loop to ring. Note that 2 mV is roughly 40 times greater than the amplitude of a sinusoidal input at –75 dBm. As long as the ringing persists, the AD606 will be "blind" to the actual input, and V_{LOG} will show major disturbances.

The solution to this problem is first, to ensure that the loop filter does not ring, and second, to use well-matched capacitors at the signal input. Use the component values suggested above to minimize ringing.

APPLICATIONS

Note that the AD606 has more than 70 MHz of input bandwidth and 90 dB of gain! Careful shielding is needed to realize its full dynamic range, since nearly all application sites will be pervaded by many kinds of interference, radio and TV stations, etc., all of which the AD606 faithfully hears. In bench evaluation, we recommend placing all of the components in a shielded box and using feedthrough decoupling networks for the supply voltage. In many applications, the AD606's low power drain allows the use of a 6 V battery inside the box.

Basic RSSI Application

Figure 6 shows the basic RSSI (Receiver Signal Strength Indicator) application circuit, including the calibration adjustments, either or both of which may be omitted in noncritical applications. This circuit may be used "as is" in such measurement applications as the log/IF strip in a spectrum or network analyzer or, with the addition of an FM or QPSK demodulator fed by the limiter outputs, as an IF strip in such communications applications as a GSM digital mobile radio or FM receiver.

The slope adjustment works in this way: the buffer amplifier (which forms part of a Sallen-Key two-pole filter, see Figure 2) has a dc gain of plus two, and the resistance from BFIN (buffer in) to OPCM (output common) is nominally 9.375 kΩ. This resistance is driven from the logarithmic detector sections with a current scaled 2 μA/dB, generating 18.75 mV/dB at BFIN, hence 37.5 mV/dB at V_{LOG}. Now, a resistor (R4 in Figure 6) connected directly between BFIN and VLOG would form a controlled positive-feedback network with the internal 9.375 kΩ resistor which would raise the gain, and thus increase the slope voltage, while the same external resistor connected between BFIN and ground would form a shunt across the internal resistor and reduce the slope voltage. By connecting R4 to a potentiometer R2 across the output, the slope may be adjusted either way; the value for R4 shown in Figure 6 provides approximately ±10% range, with essentially no effect on the slope at the midposition.

The intercept may be adjusted by adding a small current into BFIN via R1 and R3. The AD606 is designed to have the nominal intercept value of –88 dBm when R1 is centered using this network, which provides a range of ±5 dB.

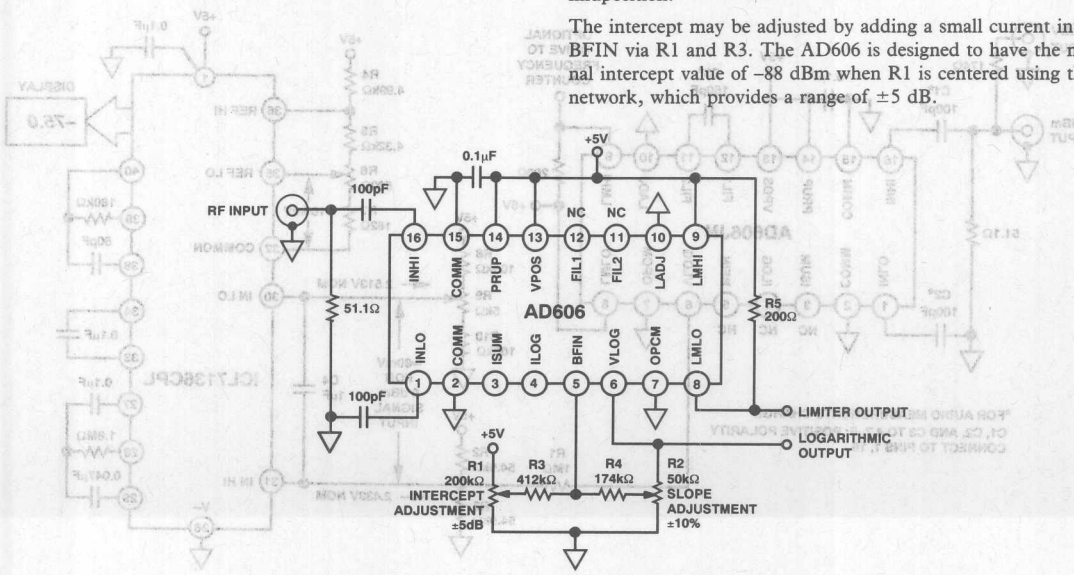

Figure 6. Basic Application Circuit Showing Optional Slope and Intercept Adjustments

minimize power drain. Calibration can be achieved in several ways: The simplest is to apply an RF input at the desired operating frequency which is amplitude modulated at a relatively low frequency (say 1 kHz to 10 kHz) to a known modulation index. Thus, one might choose a ratio of 2 between the maximum and minimum levels of the RF amplitude, corresponding to a 6 dB (strictly, 6.02 dB) change in input level. The average RF level should be set to about −35 dBm (the midpoint of the AD606's range). R2 is then adjusted so that the 6 dB input change results in the desired output voltage change, for example, 226 mV at 37.5 mV/dB.

A better choice would be a 4:1 ratio (12.04 dB), to spread the residual error out over a larger segment of the whole transfer function. If a pulsed RF generator is available, the decibel increment might be enlarged to 20 dB or more. Using just a fixed-level RF generator, the procedure is more time consuming, but is carried out in just the same way: manually change the level by a known number of decibels and adjust R2 until V_{LOG} varies by the corresponding voltage.

Having adjusted the slope, the intercept may now be simply adjusted using a known input level. A value of –35 dBm (397.6 mV rms, or 400 mV to within 0.05 dB) is recommended, and if the standard scaling is used (P_X = – 88.33 dBm, V_Y = 37.5 mV/dB), then V_{LOG} should be set to +2 V at this input level.

A Low Cost Audio Through RF Power Meter

Figure 7 shows a simple power meter that uses the AD606 and an ICL7136 3-1/2 digit DMM IC driving an LCD readout. The circuit operates from a single +5 V supply and provides direct readout in dBm, with a resolution of 0.1 dBm.

measure signals from below −80 dBm to over +10 dBm. An optional 50 Ω termination is included in the figure; this could form the lower arm of an external attenuator to accommodate larger signal levels. By the simple expedient of using a 13 dB attenuator, the LCD reading now becomes dBV (decibels above 1 V rms). This requires a series resistor of 174 Ω, presenting an input resistance of 224 Ω. Alternatively, the input resistance can be raised to 600 Ω using 464 Ω and 133 Ω. It is important to note that the AD606 inputs must be ac coupled. To extend the low frequency range, use larger coupling capacitors and an external loop filter, as outlined earlier.

The nominal 0.5 V to 3.5 V output of the AD606 (for a −75 dBm to +5 dBm input) must be scaled and level shifted to fit within the +1 V to +4.5 V common-mode range of the ICL7136 for the +5 V supply used. This is achieved by the passive resistor network of R1, R2, and R3 in conjunction with the bias networks of R4 through R7, which provide the ICL7136 with its reference voltage, and R9 through R11, which set the intercept. The ICL7136 measures the differential voltage between IN HI and IN LO, which ranges from −75 mV to +5 mV for a −75 dBm to +5 dBm input.

To calibrate the power meter, first adjust R6 for 100 mV between REF HI and REF LO. This sets the initial slope. Then adjust R10 to set IN LO 80 mV higher than IN HI. This sets the initial intercept. The slope and intercept may now be adjusted using a calibrated signal generator as outlined in the previous section.

To extend the low frequency limit of the system to audio frequencies, simply change C1, C2, and C3 to 4.7 μF.

The limiter output of the AD606 may be used to drive the high-impedance input of a frequency counter.

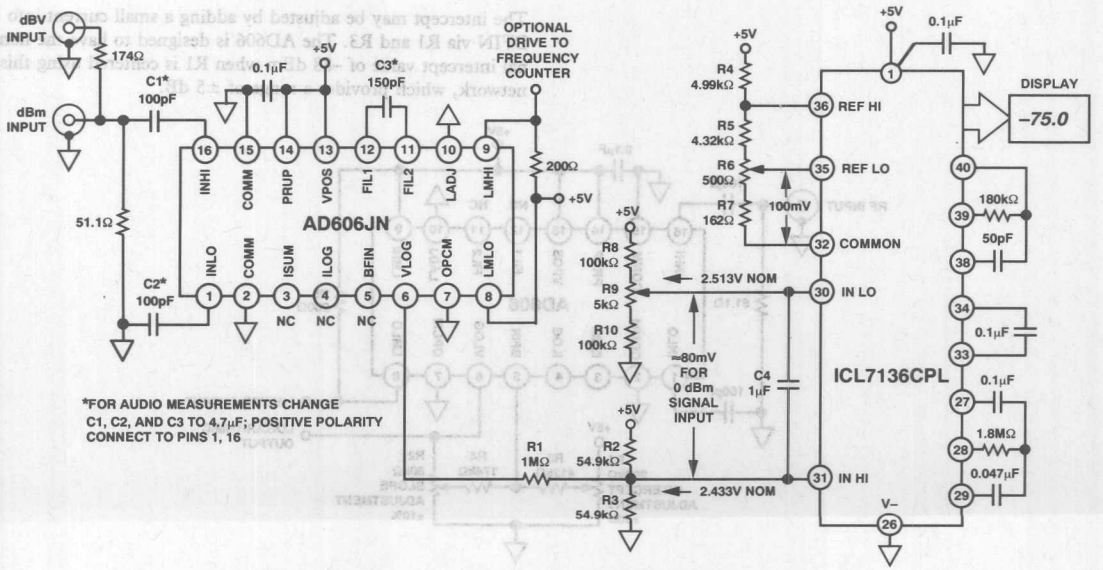

Figure 7. A Low Cost RF Power Meter

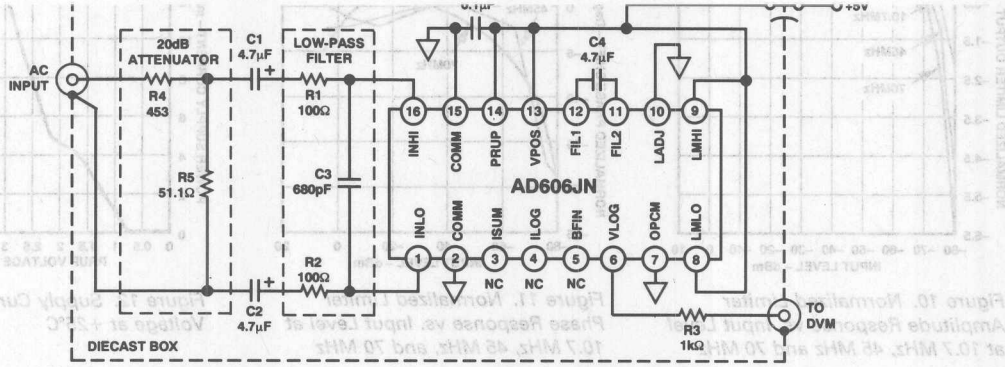

Figure 8. Circuit for Low Frequency Measurements

Low Frequency Applications

With reasonably sized input coupling capacitors and an optional input low-pass filter, the AD606 can operate to frequencies as low as 200 Hz with good log conformance. Figure 8 shows the schematic, with the low-pass filter included in the dashed box. This circuit should be built inside a die cast box and the signal brought in through a coaxial connector. The circuit must also have a low-pass filter to reject the attenuated RF signals that would otherwise be rectified along with the desired signal and be added to the log output. The shielded and filtered circuit has a 90 dB dynamic range, as shown in Figure 9.

In this circuit, R4 and R5 form a 20 dB attenuator that extends the input range to 10 V rms. R3 isolates loads from VLOG. Capacitors C1 and C2 (4.7 µF each), R1, R2, and the AD606's input resistance of 2.5 kΩ form a 100 Hz high-pass filter that is before the AD606; the corner frequency of this filter must be well below the lowest frequency of interest. In addition, the offset-correction loop introduces another pole at low signal levels that is transformed into another high-pass filter because it is in a feedback path. This indicates that there has to be a gradual transition from a 40 dB roll off at low signal levels to a 20 dB roll off at high signal levels, at which point the feedback low pass filter is effectively disabled since the incoming signal swamps the feedback signal.

This low-pass filter introduces some attenuation due to R1 and R2 in conjunction with the 2.5 kΩ input resistance of the AD606. To minimize this effect, the value of R1 and R2 should be kept as small as possible–100 Ω is a good value since it balances the need to reduce the attenuation as mentioned above with the requirement for R1 and R2 to be much larger then the impedance of C1 and C2 at the low-pass corner frequency, in our case about 1 MHz.

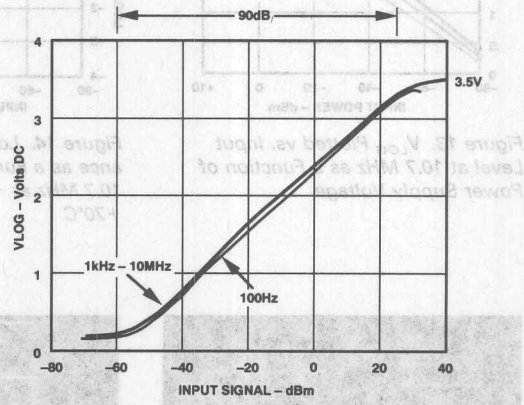

Figure 9. Performance of Low Frequency Circuit at 100 Hz and 1 kHz to 10 MHz (Note Attenuation)

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AD606—Typical Characteristics

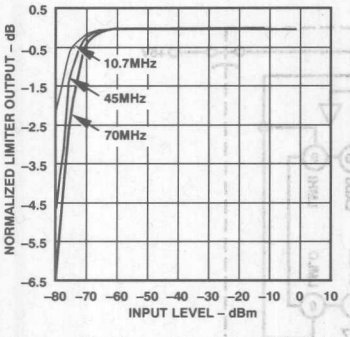

Figure 10. Normalized Limiter Amplitude Response vs. Input Level at 10.7 MHz, 45 MHz and 70 MHz

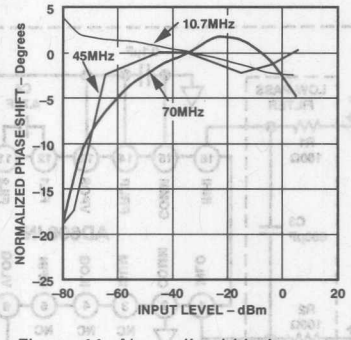

Figure 11. Normalized Limiter Phase Response vs. Input Level at 10.7 MHz, 45 MHz, and 70 MHz

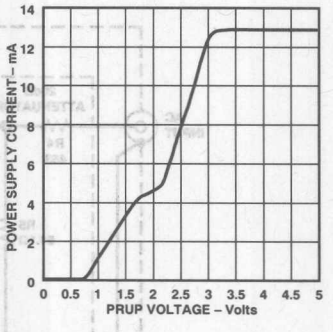

Figure 12. Supply Current vs. PRUP Voltage at +25°C

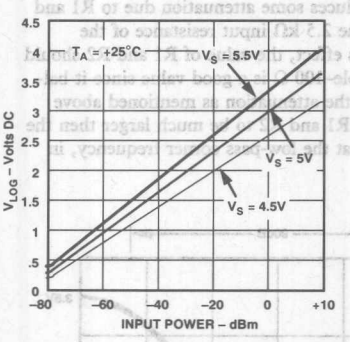

Figure 13. V_{LOG} Plotted vs. Input Level at 10.7 MHz as a Function of Power Supply Voltage

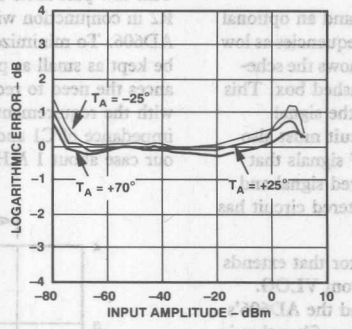

Figure 14. Logarithmic Conformance as a Function of Input Level at 10.7 MHz at −25°C, +25°C, and +70°C

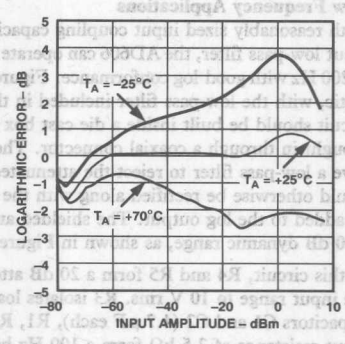

Figure 15. Logarithmic Conformance as a Function of Input Level at 45 MHz at −25°C, +25°C, and +70°C

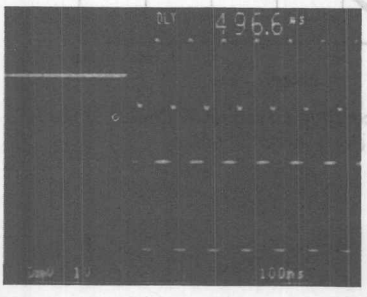

Figure 16. Limiter Response at Onset of 10.7 MHz Modulated Pulse at −75 dBm Using 200 pF Input Coupling Capacitors.

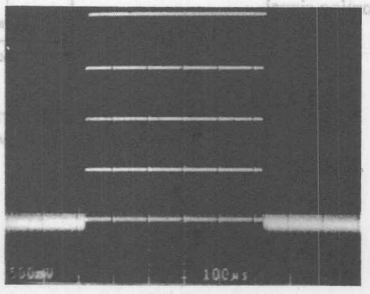

Figure 17. V_{LOG} Response to a 10.7 MHz CW Signal Modulated by a 25 μs Wide Pulse with a 25 kHz Repetition Rate Using 200 pF Input Coupling Capacitors. The Input Signal Goes from +5 dBm to −75 dBm in 20 dB Steps.

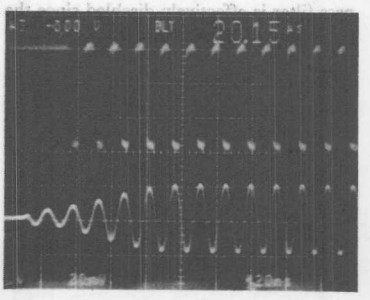

Figure 18. Limiter Response at Onset of 70 MHz Modulated Pulse at −55 dBm Using 200 pF Input Coupling Capacitors.

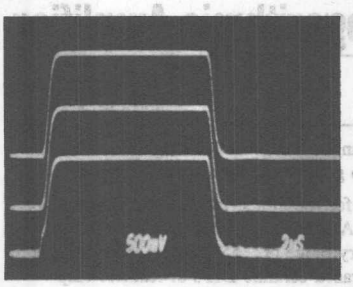

Figure 19. V_{LOG} Output for a Pulsed 10.7 MHz Input; Top Trace: −35 dBm to +5 dBm; Middle Trace: −15 dBm to −55 dBm; Bottom Trace: −35 dBm to −75 dBm

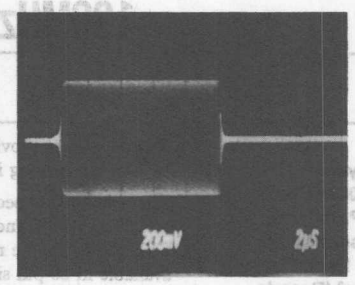

Figure 20. Example of Test Signal Used for Figure 19

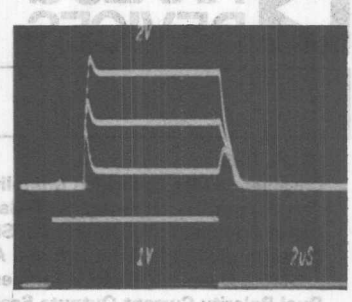

Figure 21. V_{LOG} Output for 10.7 MHz CW Input with PRUP Toggled ON and OFF; Top Trace: +5 dBm Input; Middle Trace: −35 dBm Input; Bottom Trace: −75 dBm; PRUP Input from HP8112A: 0 to 4 V, 10 µs Pulse Width with 10 kHz Repetition Rate

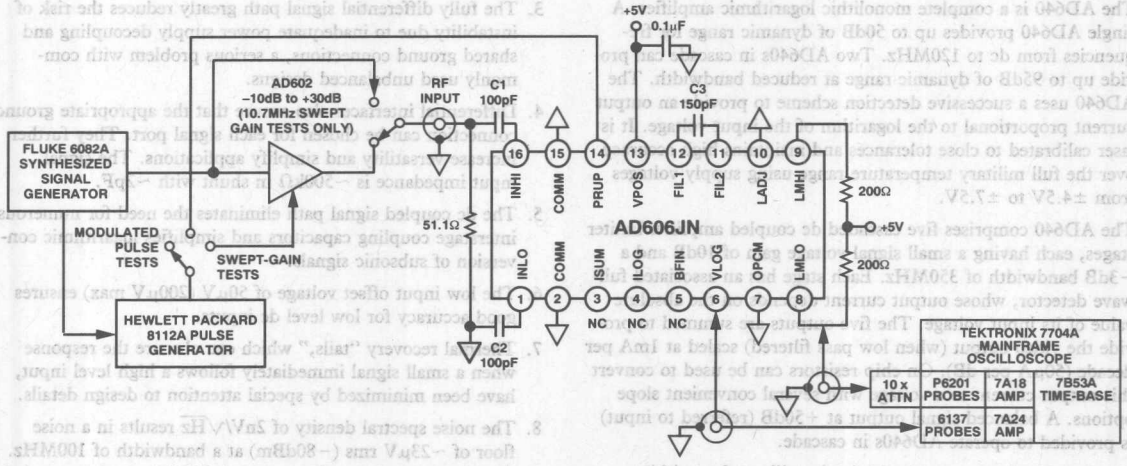

Figure 22. Test Setup for Characterization Data

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DC Coupled Demodulating 120MHz Logarithmic Amplifier

AD640

FEATURES

Complete, Fully Calibrated Monolithic System
Five Stages, Each Having 10dB Gain, 350MHz BW
Direct Coupled Fully Differential Signal Path
Logarithmic Slope, Intercept and AC Response are Stable Over Full Military Temperature Range
Dual Polarity Current Outputs Scaled 1mA/Decade
Voltage Slope Options (1V/Decade, 100mV/dB, etc.)
Low Power Operation (Typically 220mW at ±5V)
Low Cost Plastic Packages Also Available

APPLICATIONS

Radar, Sonar, Ultrasonic and Audio Systems
Precision Instrumentation from DC to 120MHz
Power Measurement with Absolute Calibration
Wide Range High Accuracy Signal Compression
Alternative to Discrete and Hybrid IF Strips
Replaces Several Discrete Log Amp ICs

PRODUCT DESCRIPTION

The AD640 is a complete monolithic logarithmic amplifier. A single AD640 provides up to 50dB of dynamic range for frequencies from dc to 120MHz. Two AD640s in cascade can provide up to 95dB of dynamic range at reduced bandwidth. The AD640 uses a successive detection scheme to provide an output current proportional to the logarithm of the input voltage. It is laser calibrated to close tolerances and maintains high accuracy over the full military temperature range using supply voltages from ±4.5V to ±7.5V.

The AD640 comprises five cascaded dc coupled amplifier/limiter stages, each having a small signal voltage gain of 10dB and a −3dB bandwidth of 350MHz. Each stage has an associated full-wave detector, whose output current depends on the absolute value of its input voltage. The five outputs are summed to provide the video output (when low pass filtered) scaled at 1mA per decade (50μA per dB). On chip resistors can be used to convert this output current to a voltage with several convenient slope options. A balanced signal output at +50dB (referred to input) is provided to operate AD640s in cascade.

The logarithmic response is absolutely calibrated to within ±1dB for dc or square wave inputs from ±0.75mV to ±200mV, with an intercept (logarithmic offset) at 1mV dc. An integral X10 attenuator provides an alternative input range of ±7.5mV to ±2V dc. Scaling is also guaranteed for sinusoidal inputs.

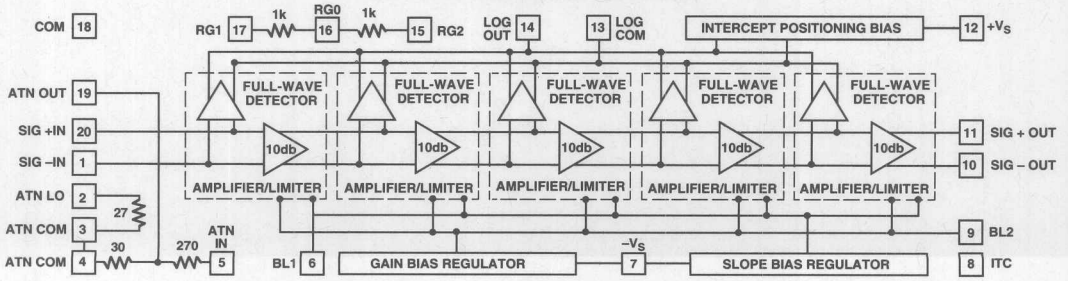
The AD640B is specified for the industrial temperature range of −40°C to +85°C and the AD640T, available processed to MIL-STD-883B, for the military range of −55°C to +125°C. Both are available in 20-pin side brazed ceramic DIPs or leadless chip carriers (LCC). The AD640J is specified for the commercial temperature range of 0 to +70°C, and is available in both 20-pin plastic DIP (N) and PLCC (P) packages.

This device is now available to Standard Military Drawing (DESC) number 5962-9095501MRA and 5962-9095501M2A.

PRODUCT HIGHLIGHTS

1. Absolute calibration of a wideband logarithmic amplifier is unique. The AD640 is a high accuracy measurement device, not simply a logarithmic building block.
2. Advanced design results in unprecedented stability over the full military temperature range.
3. The fully differential signal path greatly reduces the risk of instability due to inadequate power supply decoupling and shared ground connections, a serious problem with commonly used unbalanced designs.
4. Differential interfaces also ensure that the appropriate ground connection can be chosen for each signal port. They further increase versatility and simplify applications. The signal input impedance is ~500kΩ in shunt with ~2pF.
5. The dc coupled signal path eliminates the need for numerous interstage coupling capacitors and simplifies logarithmic conversion of subsonic signals.
6. The low input offset voltage of 50μV (200μV max) ensures good accuracy for low level dc inputs.
7. Thermal recovery "tails," which can obscure the response when a small signal immediately follows a high level input, have been minimized by special attention to design details.
8. The noise spectral density of 2nV/$\sqrt{\text{Hz}}$ results in a noise floor of ~23μV rms (−80dBm) at a bandwidth of 100MHz. The dynamic range using cascaded AD640s can be extended to 95dB by the inclusion of a simple filter between the two devices.

FUNCTIONAL BLOCK DIAGRAM



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

DC SPECIFICATIONS (V_S = ±5V, T_A = +25°C, unless otherwise noted)

Model		AD640J			AD640B			AD640T			
Transfer Function[1]		$I_{OUT}=I_Y$ LOG $\lvert V_{IN}/V_X\rvert$ for V_{IN}=±0.75mV to ±200mV dc									
Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
SIGNAL INPUTS (Pins 1, 20)											
Input Resistance	Differential		500			500			500		kΩ
Input Offset Voltage	Differential		50	500		50	200		50	200	μV
vs. Temperature			0.8			0.8			0.8		μV/°C
Over Temperature	T_{min} to T_{max}									300	μV
vs. Supply			2			2			2		μV/V
Input Bias Current			7	25		7	25		7	25	μA
Input Bias Offset			1			1			1		μA
Common Mode Range		−2		+0.3	−2		+0.3	−2		+0.3	V
INPUT ATTENUATOR (Pins 2, 3, 4, 5 & 19)											
Attenuation[2]	Pin 5 to Pin 19		20			20			20		dB
Input Resistance	Pins 5 to 3/4		300			300			300		Ω
SIGNAL OUTPUT (Pins 10, 11)											
Small Signal Gain[4]			50			50			50		dB
Peak Differential Output[5]			±180			±180			±180		mV
Output Resistance	Either Pin to COM		75			75			75		Ω
Quiescent Output Voltage	Either Pin to COM		−90			−90			−90		mV
LOGARITHMIC OUTPUT[6] (Pin 14)											
Voltage Compliance Range		−0.3		$+V_S$ −1	−0.3		$+V_S$ −1	−0.3		$+V_S$ −1	V
Slope Current, I_Y		0.95	1.00	1.05	0.98	1.00	1.02	0.98	1.00	1.02	mA
Accuracy vs. Temperature			0.002			0.002			0.002		%/°C
	T_{min} to T_{max}							0.98		1.02	mA
Accuracy vs. Supply	±V_S=4.5V to 7.5V		0.08	1.0		0.08	0.4		0.08	0.4	%/V
Intercept Voltage[7], V_X		0.85	1.00	1.15	0.95	1.00	1.05	0.95	1.00	1.05	mV
vs. Temperature			0.5			0.5			0.5		μV/°C
Over Temperature	T_{min} to T_{max}							0.90		1.10	mV
vs. Supply	±V_S=4.5V to 7.5V		2			2			2		μV/V
Logarithmic Offset											
(Alt. Definition of V_X)		−61.5	−60.0	−58.7	−60.5	−60.0	−59.5	−60.5	−60.0	−59.5	dBV
vs. Temperature			0.004			0.004			0.004		dB/°C
Over Temperature	T_{min} to T_{max}							−60.9		−59.1	dB
vs. Supply	±V_S=4.5V to 7.5V		0.017			0.017			0.017		dB/V
Intercept Voltage Using Attenuator		8.25	10.0	11.75	9.0	10.0	11.0	9.0	10.0	11.0	mV
Zero Signal Output Current[3]			−0.2			−0.2			−0.2		mA
ITC Disabled	Pin 8 to COM		−0.27			−0.27			−0.27		mA
Maximum Output Current			2.3			2.3			2.3		mA
APPLICATIONS RESISTORS (Pins 15, 16, 17)			1.000		0.995	1.000	1.005	0.995	1.000	1.005	kΩ
DC LINEARITY											
V_{IN}=±1mV to ±100mV			0.35	1.2		0.35	0.6		0.35	0.6	dB
TOTAL ABSOLUTE DC ACCURACY											
V_{IN}=±1mV to ±100mV[8]			0.55	2		0.55	0.9		0.55	0.9	dB
Over Temperature	T_{min} to T_{max}			3			1.7			1.8	dB
Over Supply Range	±V_S=4.5V to 7.5V			2			1.0			1.0	dB
V_{IN}=±0.75mV to ±200mV			1.0	3		1.0	2.0		1.0	2.0	dB
Using Attenuator											
V_{IN}=±10mV to ±1V			0.4	2.5		0.4	1.5		0.4	1.5	dB
Over Temperature	T_{min} to T_{max}		0.6	3		0.6	2.0		0.6	2.0	dB
V_{IN}=±7.5mV to 2V			1.2	3.5		1.2	2.5		1.2	2.5	dB
POWER REQUIREMENTS											
Voltage Supply Range		±4.5		±7.5	±4.5		±7.5	±4.5		±7.5	V
Quiescent Current[9]											
$+V_S$ (Pin 12)	T_{min} to T_{max}		9	15		9	15		9	15	mA
$-V_S$ (Pin 7)	T_{min} to T_{max}		35	60		35	60		35	60	mA

20

Model / Parameter	Conditions	AD640J Min	AD640J Typ	AD640J Max	AD640B Min	AD640B Typ	AD640B Max	AD640T Min	AD640T Typ	AD640T Max	Units
SIGNAL INPUT (Pins 1, 20)											
Input Capacitance	Either Pin to COM		2			2			2		pF
Noise Spectral Density	1kHz to 10MHz		2			2			2		nV/√Hz
Tangential Sensitivity	BW=100MHz		−72			−72			−72		dBm
3dB BANDWIDTH											
Each Stage			350			350			350		MHz
All Five Stages	Pins 1 & 20 to 10 & 11		145			145			145		MHz
LOGARITHMIC OUTPUTS[6]											
Slope Current, I_Y											
f<=1MHz		0.96	1.0	1.04	0.98	1.0	1.02	0.98	1.0	1.02	mA
f=30MHz		0.88	0.94	1.00	0.91	0.94	0.97	0.91	0.94	0.97	mA
f=60MHz		0.82	0.90	0.98	0.86	0.90	0.94	0.86	0.90	0.94	mA
f=90MHz			0.88			0.88			0.88		mA
f=120MHz			0.85			0.85			0.85		mA
Intercept, Dual AD640s[10, 11]											
f<=1MHz		−90.6	−88.6	−86.6	−89.6	−88.6	−87.6	−89.6	−88.6	−87.6	dBm
f=30MHz			−87.6			−87.6			−87.6		dBm
f=60MHz			−86.3			−86.3			−86.3		dBm
f=90MHz			−83.9			−83.9			−83.9		dBm
f=120MHz			−80.3			−80.3			−80.3		dBm
AC LINEARITY											
−40dBm to −2dBm[12]	f=1MHz		0.5	2.0		0.5	1.0		0.5	1.0	dB
−35dBm to −10dBm[12]	f=1MHz		0.25	1.0		0.25	0.5		0.25	0.5	dB
−75dBm to 0dBm[10]	f=1MHz		0.75	3.0		0.75	1.5		0.75	1.5	dB
−70dBm to −10dBm[10]	f=1MHz		0.5	2.0		0.5	1.0		0.5	1.0	dB
−75dBm to +15dBm[13]	f=10kHz		0.5	3.0		0.5	1.5		0.5	1.5	dB
PACKAGE OPTION[14]											
20-Pin Ceramic DIP Package (D)						AD640BD			AD640TD		
20-Pin Leadless Ceramic Chip Carrier (E)						AD640BE			AD640TE		
20-Pin Plastic DIP Package (N)			AD640JN								
20-Pin Plastic Leadless Chip Carrier (P)			AD640JP			AD640BP					
NUMBER OF TRANSISTORS			155			155			155		

NOTES

[1]Logarithms to base 10 are used throughout. The response is independent of the sign of V_{IN}.

[2]Attenuation ratio trimmed to calibrate intercept to 10mV when in use. It has a temperature coefficient of +0.3%/°C.

[3]The zero-signal current is a function of temperature unless internal temperature compensation (ITC) pin is grounded.

[4]Overall gain is trimmed using a ±200μV square wave at 2kHz, corrected for the onset of compression.

[5]The fully limited signal output will appear to be a square wave; its amplitude is proportional to absolute temperature.

[6]Currents defined as flowing *into* Pin 14. See FUNDAMENTALS OF LOGARITHMIC CONVERSION for full explanation of scaling concepts. Slope is measured by linear regression over central region of transfer function.

[7]The logarithmic intercept in dBV (decibels relative to 1V) is defined as 20 LOG_{10} (V_X/1V).

[8]Operating in circuit of Figure 24 using ±0.1% accurate values for R_{LA} and R_{LB}. Includes slope and nonlinearity errors. Input offset errors also included for V_{IN} >3mV dc, and over the full input range in ac applications.

[9]Essentially independent of supply voltages.

[10]Using the circuit of Figure 27, using cascaded AD640s and offset nulling. Input is sinusoidal, 0dBm in 50Ω=223mV rms.

[11]For a sinusoidal signal (see EFFECT OF WAVEFORM ON INTERCEPT). Pin 8 on second AD640 must be grounded to ensure temperature stability of intercept for dual AD640 system.

[12]Using the circuit of Figure 24, using single AD640 and offset nulling. Input is sinusoidal, 0dBm in 50Ω=223mV rms.

[13]Using the circuit of Figure 32, using cascaded AD640s and attenuator. Square wave input.

[14]For outline information see Package Information section.

All min and max specifications are guaranteed, but only those in **boldface** are 100% tested on all production units. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

THERMAL CHARACTERISTICS

	θ_{JC} (°C/W)	θ_{JA} (°C/W)
20-Pin Ceramic DIP Package (D-20)	25	85
20-Pin Leadless Ceramic Chip Carrier (E-20A)	25	85
20-Pin Plastic DIP Package (N-20)	24	61
20-Pin Plastic Leadless Chip Carrier (P-20A)	28	75

ABSOLUTE MAXIMUM RATINGS*

Supply Voltages . . . . . ±7.5V
Input Voltage (Pin 1 or Pin 20 to COM) . . . . −3V to +300mV
Attenuator Input Voltage (Pin 5 to Pin 3/4) . . . . . ±4V
Storage Temperature Range D, E . . . . . −65°C to +150°C
Storage Temperature Range N, P . . . . . −65°C to +125°C
Ambient Temperature Range, Rated Performance
Industrial, AD640B . . . . . −40°C to +85°C
Military, AD640T . . . . . −55°C to +125°C
Commercial, AD640J . . . . . 0 to +70°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.

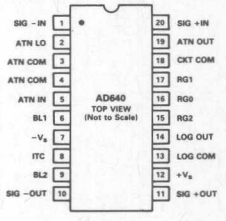
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD640JN	0°C to +70°C	Plastic DIP	N-20
AD640JP	0°C to +70°C	Plastic Leaded Chip Carrier	P-20A
AD640BD	−40°C to +85°C	Side Brazed Ceramic DIP	D-20
AD640BE	−40°C to +85°C	Ceramic Leadless Chip Carrier	E-20A
AD640BP	−40°C to +85°C	Plastic Leaded Chip Carrier	P-20A
AD640TD/883B 5962-9095501MRA	−55°C to +125°C	Side Brazed Ceramic DIP	D-20
AD640TE/883B 5962-9095501M2A	−55°C to +125°C	Ceramic Leadless Chip Carrier	E-20A
AD640TCHIP	−55°C to +125°C	Chip	

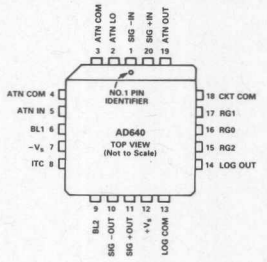
*For outline information see Package Information section.

CONNECTION DIAGRAMS

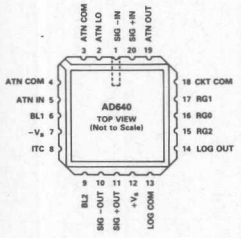
20-Pin Ceramic DIP (D) Package
20-Pin Plastic DIP (N) Package



20-Pin PLCC (P) Package



20-Pin LCC (E) Package



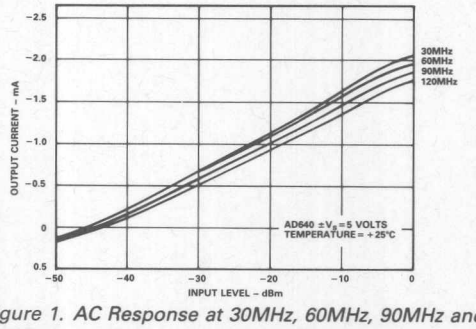


Figure 1. AC Response at 30MHz, 60MHz, 90MHz and 120MHz, vs. dBm Input (Sinusoidal Input)

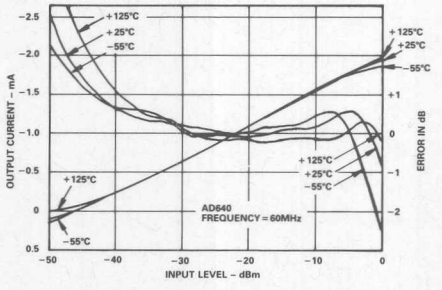


Figure 2. Logarithmic Response and Linearity at 60MHz, T_A for T_A = −55°C, +25°C, +125°C

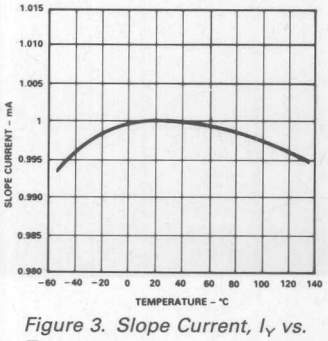


Figure 3. Slope Current, I_Y vs. Temperature

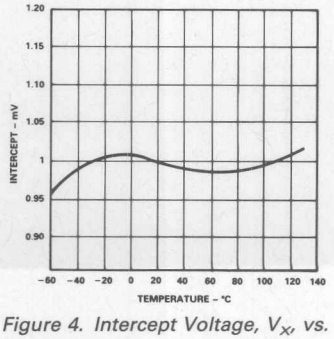


Figure 4. Intercept Voltage, V_X, vs. Temperature

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD640JN	0°C to +70°C	Plastic DIP	N-20
AD640JP	0°C to +70°C	Plastic Leaded Chip Carrier	P-20A
AD640BD	–40°C to +85°C	Side Brazed Ceramic DIP	D-20
AD640BE	–40°C to +85°C	Ceramic Leadless Chip Carrier	E-20A
AD640BP	–40°C to +85°C	Plastic Leaded Chip Carrier	P-20A
AD640TD/883B 5962-9095501MRA	–55°C to +125°C	Side Brazed Ceramic DIP	D-20
AD640TE/883B 5962-9095501MZA	–55°C to +125°C	Ceramic Leadless Chip Carrier	E-20A
ADK-40TCHIP	–55°C to +125°C	Chip	

*For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltages . . . . . ±7.5V
Input Voltage (Pin 1 or Pin 20 to COM) . . . . –3V to +300mV
Attenuator Input Voltage (Pin 5 to Pin 3/4) . . . . . ±4V
Storage Temperature Range D, E . . . . . –65°C to +150°C
Storage Temperature Range N, P . . . . . –65°C to +125°C
Ambient Temperature Range, Rated Performance
Industrial, AD640B . . . . . –40°C to +85°C
Military, AD640T . . . . . –55°C to +125°C
Commercial, AD640J . . . . . 0 to +70°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

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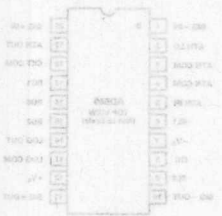
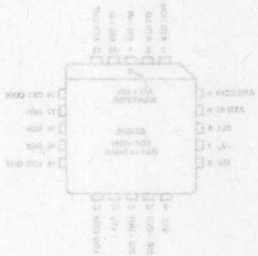
CONNECTION DIAGRAMS

20-Pin Ceramic DIP (D) Package

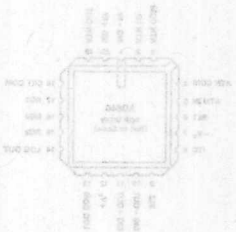


20-Pin Plastic DIP (N) Package

20-Pin PLCC (P) Package



20-Pin LCC (E) Package



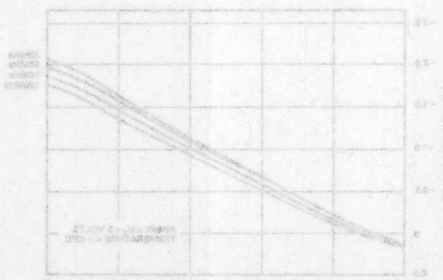


Figure 1. AC Response at 30MHz, 60MHz, 90MHz and 120MHz vs. dBm Input (Sinusoidal Input)

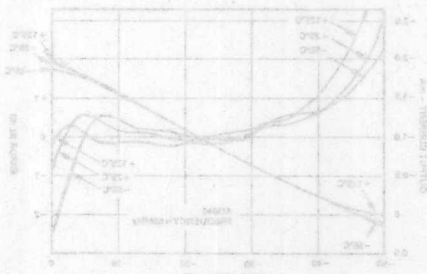


Figure 2. Logarithmic Response and Linearity at 60MHz, T_A for T_A = –55°C, +25°C, +125°C

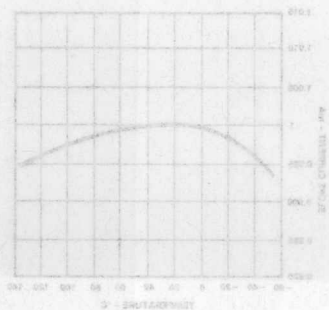


Figure 3. Slope Current, I_S vs. Temperature

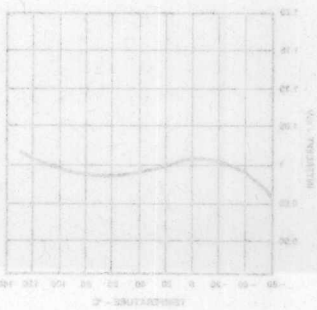


Figure 4. Intercept Voltage, V_X vs. Temperature

Special Function Components

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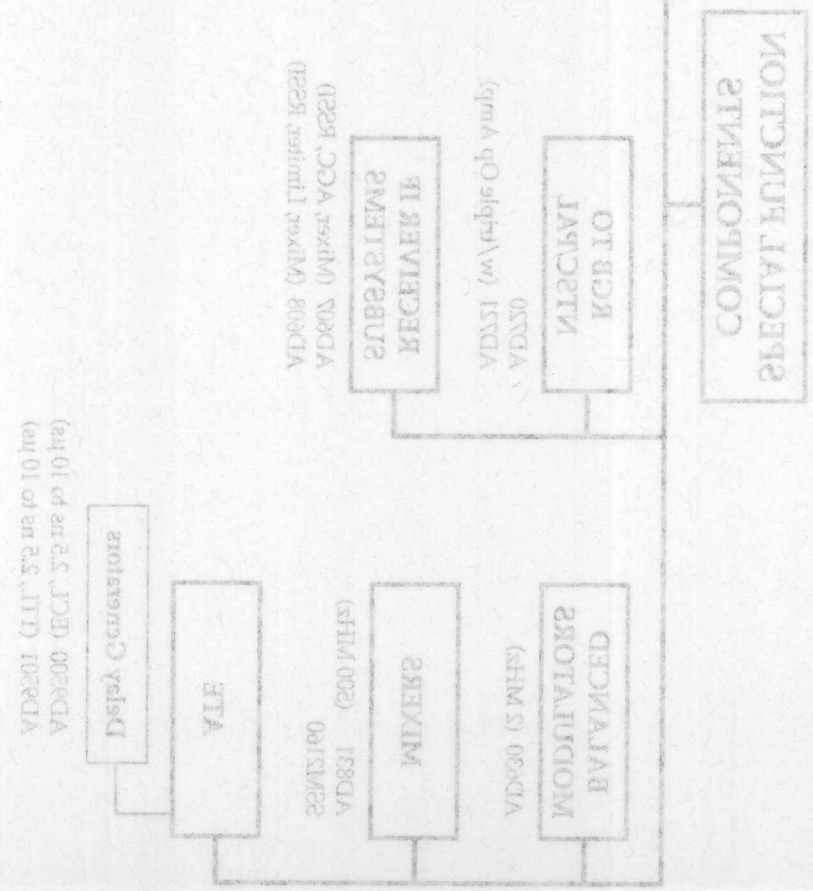
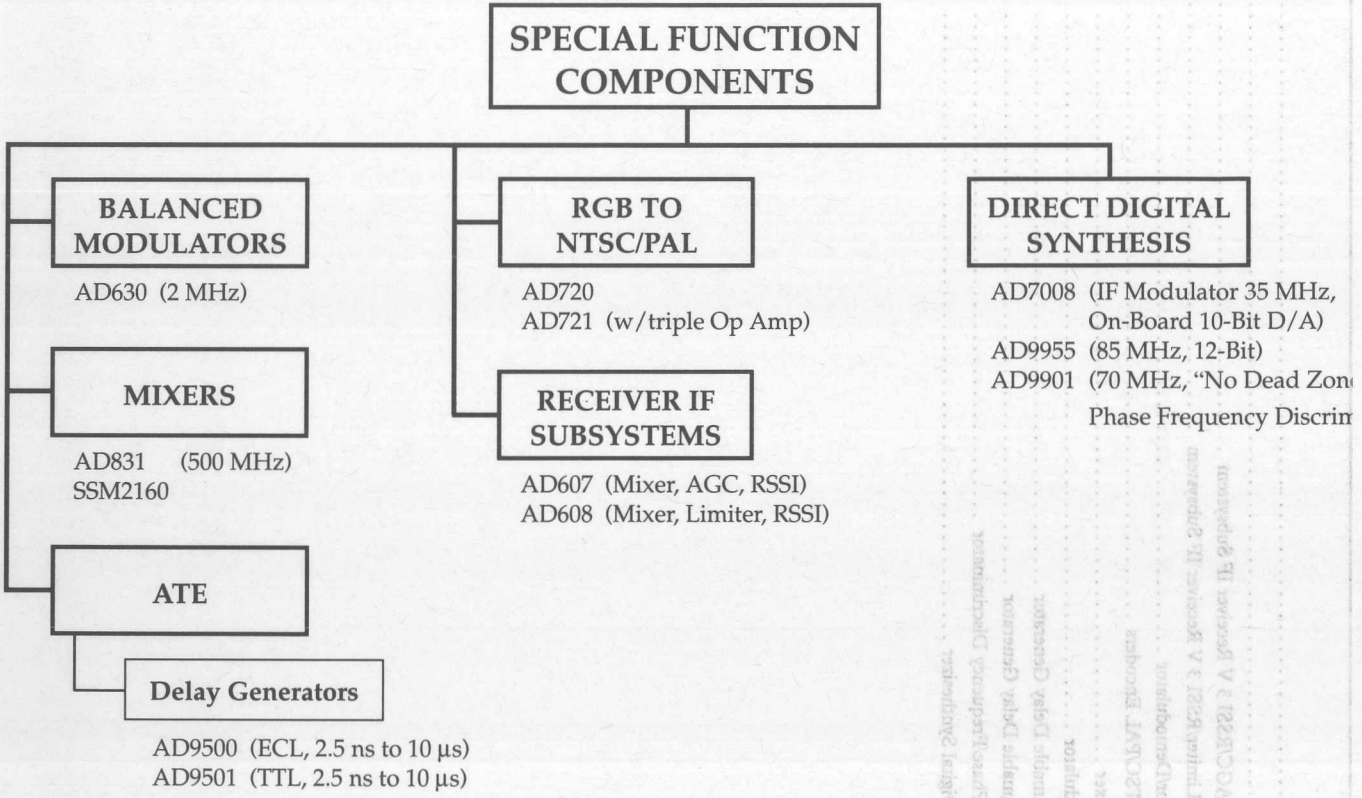


Selection Tree — Special Function Components



Selection Guides—Special Function Components

Frequency Synthesis

Model	Bus Interface Bits	Package Options[1]	Temp Ranges[2]	Page[3]	Comments
AD7008	8/16, µP	S	C[4]	21–35	DDS IF Modulator with 32-Bit Phase Accumulator and 10-Bit DAC, 20 MHz Output Capability, Single 5 V Supply, Low Power
AD9901		E, P, Q	C, M/	21–53	Ultrahigh Speed Digital Phase/Frequency Discriminator, No "Dead Zone," Linear Transfer Function up to 200 MHz, for PLLs
AD9955	32, µP	S	C	21–56	85 MHz Direct Digital Synthesizer; 32-Bit Phase Accumulator 12-Bit Sine Output
AD9955/PCB		Board	C	D	Evaluation Board which contains AD9955 and AD9713B or AD9721 DAC

RF/IF Products

Model	Function	Max Gain dB	Frequency Range	Package Options[1]	Temp Ranges[2]	Page[3]	Comments
AD607	IF Subsystem Mixer/AGC/RSSI	109	25–450 MHz	RS	I	21–5	Monoceiver™—Complete Receiver on a Chip
AD608	IF Subsystem Mixer/RSSI	110	5–450 MHz	R	I	21–9	+3 V Supply, 90 dB RSSI Range
AD831	Low Distortion Mixer	0	5–500 MHz	P	I	21–23	±5 V Supply, 24 dBm 3rd-Order Intercept

Special Function Components

Model	Function	Performance	Package Options[1]	Temp Ranges[2]	Page[3]	Comments
AD630	Balanced Modulator/Demodulator	2 MHz Bandwidth, Signal Recovery to −100 dB	D, E, N	C, I, M	21–13	Precision Gain ±1 or ±2
AD720	RGB to NTSC/PAL Converter	Complete Function with Internal Delay Line	P	C	21–16	RGB, Clock In, Luminance, Chrominance, Composite Out
AD9500	ECL Digitally Programmable Delay Generator	10 ps Resolution, 2.5 ns to 10 µs Full Scale	E, P, Q	I, M	21–45	Pulse Deskewing, Phase Control
AD9501	TTL/CMOS Digitally Programmable Delay Generator	10 ps Resolution, 2.5 ns to 10 µs Full Scale	N, P, Q	C, M	21–49	+5 V Supply, 50 MHz Pulse Rate

[1]Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = J-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline "SOIC" Package; RS = SSOP—Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-92; U = TSOP—Thin Small Outline Package; W = Nonhermetic Ceramic/Glass DIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C. If a device has military grade offerings, the M temperature designator will be followed by: / to indicate 883B, $_J$ for JAN, $_D$ for SMD, and $_S$ for space level.
[3]D = Data Sheet. All other entries refer to this volume.
[4]Operates to +25°C.
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Boldface Type: Data sheet information in this volume.

Selection Guides — Special Function Components

Frequency Synthesis

Model	Bus Interface	Package Options[1]	Temp Ranges[2]	Page[3]	Comments
ADV008	SPI, μP	S	C, I	21-35	DDS RF Modulator with 32-Bit Phase Accumulator and 10-Bit DAC, 20 MHz Output
ADV201	P, μP	Q	C, MV	21-53	Quadrature Digital Upconverter, Low Power, Dual 12-Bit, 65 MSPS DACs, Single 5 V Supply, Low Spurious, Wideband Digital Phase-Locked Loop, Digital Frequency Discriminator, No "Dead Zone"
ADS52	μP	S	C	21-36	52 MHz Digital Synthesizer, 32-Bit Linear Tuning Word, Programmable Functions up to 200 MHz, for PTLs
ADS9CRCB	Board	D	C	21-38	Evaluation Board which contains ADS005 and ADS021 DACs

RF/IF Products

Model	Function	Max Gain dB	Performance	Package Options[1]	Page[3]	Comments
ADM27	LF Subsystem	100	25–450 MHz	BS	21-5	Complete Receiver on a Chip
ADS08	IF Subsystem	110	5–50 MHz	R	21-9	90 dB ASIS Range
ADS21	Low Distortion	0	5–500 MHz	F	21-23	+13 V Supply, 24 dBm 3rd-Order Intercept
ADS27	IF Subsystem	100	25–450 MHz	BS	21-5	+5 V Supply, 90 dB ASIS Range
ADS08	IF Subsystem	110	5–50 MHz	R	21-9	+13 V Supply, 24 dBm 3rd-Order Intercept
ADS21	Low Distortion	0	5–500 MHz	F	21-23	+5 V Supply, 24 dBm 3rd-Order Intercept

Special Function Components

Model	Function	Performance	Package Options[1]	Temp Ranges[2]	Page[3]	Comments
ADJ30	Balanced Modulator/Demodulator	2 MHz Bandwidth, Signal Recovery to –100 dB	D, H, N	C, I, M	21-13	Precision Gain +1 or +2
ADV30	RGB to NTSC/PAL Converter	Complete Transition with Internal Delay Lines	F	C	21-15	RGB, Clock In, Luminance, Chrominance, Composite Out
ADV490	ECL Digitally Programmable Delay Generator	10 ps Resolution, 2.5 ns to 10 ns Full Scale	E, P, Q	I, M	21-45	Pulse Delaying, Pulse Control
ADV491	TTL/CMOS Digitally Programmable Delay Generator	10 ps Resolution, 2.5 ns to 10 ns Full Scale	N, P, Q	C, M	21-49	+5 V Supply, 50 MHz Pulse Rate

Delay Generator

Package Options: D = Hermetic DIP, Ceramic or Metal; E = Ceramic Leadless Chip Carrier; F = Ceramic Flatpack; G = Ceramic Pin Grid Array; H = Hermetic Metal Can; J = 1-Leaded Ceramic Package; M = Hermetic Metal Can DIP; N = Plastic or Epoxy Sealed DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; S = Small Outline "SOIC" Package; RS = SSOP; Shrink Small Outline Package; S = Plastic Quad Flatpack; ST = Thin Quad Flatpack; T = TO-52; U = TSOP – Thin Small Outline Package; W = Narrow Ceramic SBDIP; Y = Single-In-Line "SIP" Package; Z = Ceramic Leaded Chip Carrier.

Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, –40°C to +85°C (Some older products –25°C to +85°C); M = Military, –55°C to +125°C. If a device has military grade, the M suffix is omitted.

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Low Power Mixer/AGC/RSSI 3 V Receiver IF Subsystem

AD607

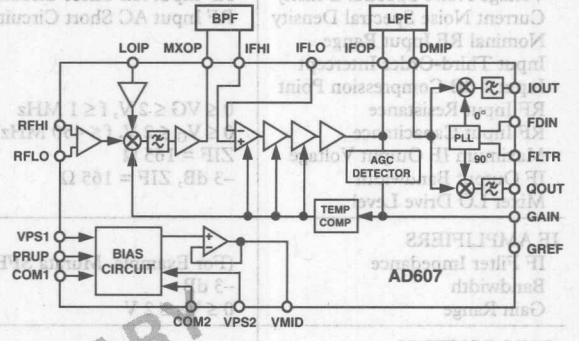
FEATURES

Complete Receiver on a Chip: Monoceiver™
Interfaces to AD7015 GSM Baseband Converter
Mixer
–15 dBm 1 dB Compression Point
>450 MHz Input Bandwidth
–16 dBm LO Input
Linear IF Amplifier
100 dB of Linear-in-dB Gain Control
Internal AGC with RSSI Output or External MGC
Any IF Below 25 MHz
Quadrature Demodulator
On-Board Phase-Locked Quadrature Oscillator
90 ± 1.5° Phase Quadrature at 10.7 MHz
Can Also Demodulate AM, FM, CW, SSB
Low Power
25 mW at 3 V
CMOS-Compatible Power-Down to 300 µW

APPLICATIONS

GSM, CDMA, PHP, TDMA Receivers
Infrared Data Receivers
Battery-Powered Communications Receivers

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD607 is a 3 V low power receiver RF/IF subsystem for operation at IF or RF input frequencies as high as 450 MHz and IFs to 25 MHz. It consists of a mixer, IF amplifiers, an I/Q demodulator, a phase-locked quadrature oscillator, AGC detector, and a biasing system with external power-down. In a typical DMR application, the AD607 accepts a 240 MHz IF input and downconverts it to a 10.7 MHz IF where it is filtered, amplified with internal AGC (or external MGC), and demodulated into I and Q baseband outputs.

The AD607's low noise, high intercept mixer is a doubly balanced "Gilbert-Cell" type and operates linearly for RF inputs spanning –95 dBm to –15 dBm. It has a nominal –5 dBm third-order intercept. The mixer section of the AD607 also includes a local oscillator (LO) preamplifier, which lowers the required LO drive to –16 dBm (50 mV sine wave amplitude).

Fully differential access to the RF input increases the versatility of this front end for such applications as interfacing to differential output SAW filters. The mixer's single-sided IF current output can directly drive a bandpass filter with an impedance of 200 Ω or greater. An optional second IF filter can be included to limit wideband noise and provide additional selectivity. The output for the second IF filter can optionally be used to drive an A/D converter or the AD607's PLL, as will be described below.

The gain control input (Pin 12) can serve as either an MGC input or an RSSI (AGC voltage) output. In MGC operation, the AD607 accepts a DSP-based MGC input of 0 V to 2 V at pin 12. This voltage can be generated by a DAC in the compatible AD70xx family of baseband converters. In AGC operation, an on-board detector and an external averaging capacitor connected to Pin 12 form an AGC loop that holds the I and Q output levels at about ±300 mV. The voltage across this capacitor then provides an RSSI output.

An I/Q demodulator provides in-phase and quadrature baseband outputs to interface with such baseband converters as the Analog Devices' AD7002, AD7005, AD7013, or AD7015. A unique quadrature VCO that is phase-locked to a low level or CMOS-compatible input at the intermediate frequency drives the I and Q demodulator.

The I/Q demodulator can also demodulate AM or FM when its oscillator is phase locked to the received signal; in this mode, the In-Phase and Quadrature demodulators become detectors for AM and FM, respectively. The oscillator can also be phase-locked to an external oscillator and the demodulator will act as a product detector for CW or SSB reception.

The AD607 uses supply voltages from 2.7 V to 6 V over the temperature range of –25°C to +85°C. Operation is enabled by a CMOS logical level; response time is typically <3 µs. When disabled the standby power is reduced to 300 µW. The AD607 comes in a 20-pin Small-Shrink Outline (SSOP) surface-mount package.

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This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

DYNAMIC PERFORMANCE				
MIXER				
RF and LO Frequency Range		450		MHz
Conversion Gain Range	$0 \le V_G \le 2$ V, Z_L =165 Ω, f_{RF} = 240 MHz		1.5 to 26.5	dB
Voltage Noise Spectral Density	RF Input AC Short Circuited, LO to VP		2	$nV\sqrt{Hz}$
Current Noise Spectral Density	RF Input AC Short Circuited, LO to VP		TBD	$pA/\sqrt{Hz}$
Nominal RF Input Range			–95 to –15	dBm
Input Third-Order Intercept			–5	dBm
Input 1 dB Compression Point			–15	dBm
RF Input Resistance	$0 \le VG \le 2$ V, f ≤ 1 MHz		2.7 to 5.5	kΩ
RF Input Capacitance	$0 \le V_G \le 2$ V, f ≤ 450 MHz		2.4 to 2.75	pF
Maximum IF Output Voltage	ZIF = 165 Ω		2	V p-p
IF Output Bandwidth	–3 dB, ZIF = 165 Ω		100	MHz
Mixer LO Drive Level			–16	dBm
IF AMPLIFIERS				
IF Filter Impedance	(For Example, Murata SFE10.7)	200	330	Ω
Bandwidth	–3 dB		50	MHz
Gain Range	$0 \le V_G \le 2$ V		7.5 to 82.5	dB
GAIN CONTROL				
Overall Gain Range	Mixer + IF Section, $0 \le V_G \le 2$ V, GREF Connected to 1.5 V		9 to 109	dB
Gain Scaling	GREF Connected to 1.5 V		50	dB/V
	GREF Connected to General Reference Voltage V_R		$75/V_R$	dB/V
Gain Error	$0 \le V_G \le 2$ V, GREF Connected to 1.5 V		<0.25	dB
Bias Current at GAIN (Pin 12)			–5	µA
Bias Current at GREF (Pin 7)			1	µA
Resistance at GAIN, GREF			>1	MΩ
I AND Q DEMODULATORS				
Input Resistance	From DMIP to VMID		>50	kΩ
Input Bias Current			1	µA
Demodulation Gain	Sine Wave Input, Baseband Output		18	dB
Maximum Output Voltage	$R_L \ge 10$ kΩ		2.5	V p-p
Demodulation Nonlinearity	Full Output Voltage		0.1	%
Output Bandwidth	Sine Wave Input, Baseband Output		3	MHz
CARRIER-RECOVERY PLL				
Frequency Range			0.4 to 25	MHz
Required Input Drive Level	Sine Wave Input at Pin 1		200	mV p-p
Quadrature Error	IF = 10.7 MHz		±1.5	Degree
Acquisition Time to ±3°	IF = 10.7 MHz		<10	µs
POWER-DOWN INTERFACE				
Logical Threshold			1.5	V dc
Input Current for Logical High			75	µA
Turn-On Response Time			500	ns
Turn-Off Response Time	To 200 µA Supply Current		1	µs
Standby Current			100	µA
POWER SUPPLY				
Supply Range		2.7	3 to 6	V
Supply Current	Mid-Gain, IF = 10.7 MHz		8	mA
OPERATING TEMPERATURE				
T_{MIN} to T_{MAX}		–25	+85	°C

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage VPOS . . . . . +6 V
Internal Power Dissipation[2] . . . . . 600 mW
Operating Temperature Range . . . . . –25°C to +85°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature, Soldering (60 sec) . . . . . +300°C

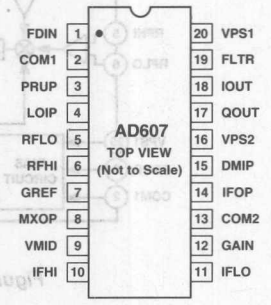
NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics: 20-pin SSOP package; θ_{JA} = TBD.

PIN CONNECTION

20-Lead SSOP



PIN DESCRIPTION

Pin	Mnemonic	Reads	Function
1	FDIN	Frequency Demodulator Input	PLL input for I/Q demodulator quadrature oscillator.
2	COM1	Common #1	Supply common for RF front end and main bias.
3	PRUP	Power-Up	3 V/5 V CMOS-compatible power-up control.
4	LOIP	Local Oscillator Input	LO external input.
5	RFLO	RF "Low" Input	Usually connected to ac ground.
6	RFHI	RF "High" Input	Accepts RF input of –95 dBm to –15 dBm.
7	GREF	Gain Reference	High impedance input, typically 1.5 V, sets gain scaling.
8	MXOP	Mixer Output	Low impedance, single-sided voltage output, +5 dBm max.
9	VMID	Mid-Supply Bias Voltage Output	Output of the mid-supply bias generator (VPOS/2).
10	IFHI	IF "High" Input	IF input, +5 dBm (±56 mV) max.
11	IFLO	IF "Low" Voltage	Reference node for IF input; auto-offset null.
12	GAIN	Gain Control Input	High impedance input, 0 V–2 V, max gain at V = 0.
13	COM2	Common #2	Supply common for IF stages and demodulator.
14	IFOP	IF Output	Low impedance, single-sided voltage output, +5 dBm max.
15	DMIP	Demodulator Input	Signal input to I and Q demodulators.
16	VPS2	VPOS Supply #2	Supply to high level IF, PLL, and demodulators.
17	QOUT	Quadrature Output	Low impedance Q baseband output, ±1.23 V full scale.
18	IOUT	In-Phase Output	Low impedance I baseband output, ±1.23 V full scale.
19	FLTR	PLL Loop Filter	Series RC PLL Loop filter connected to ground.
20	VPS1	VPOS Supply #1	Supply to mixer, low level IF, PLL, and gain control.

PRELIMINARY TECHNICAL DATA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD607 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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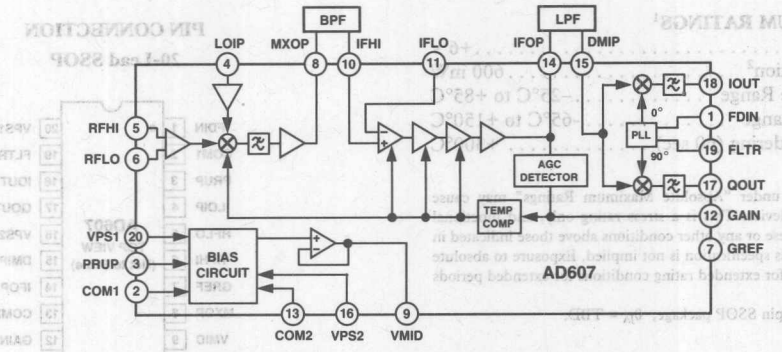

Figure 1. AD607 Functional Block Diagram

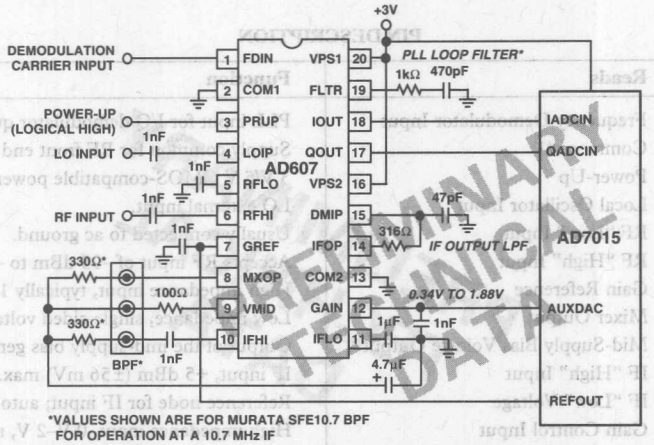

Figure 2. AD607 Connections to AD7015 Baseband Converter. The AUX DAC Output from the AD7015 Controls the Gain in the AD607

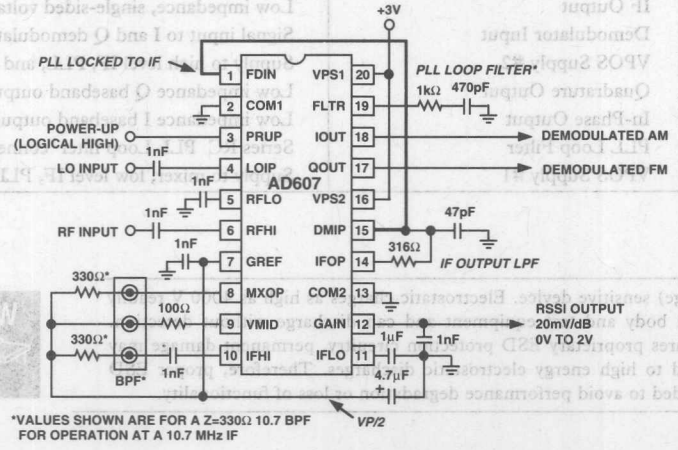

Figure 3. AD607 Connections for AM or FM Demodulation. The PLL Recovers the Received Carrier via the Connection (Darker Line) Between Pins 1 and 15. The AD607's Internal AGC Circuit Controls the Gain and Provides an RSSI Output at Pin 12

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Low Power Mixer/Limiter/RSSI 3 V Receiver IF Subsystem

AD608

FEATURES

Mixer
- **–15 dBm, 1 dB Compression Point**
- **–5 dBm IP3**
- **26 dB Conversion Gain**
- **>450 MHz Input Bandwidth**

Logarithmic/Limiting Amplifier
- **90 dB RSSI Range**
- **±3° Phase Stability over 80 dB Range**

Low Power
- **21 mW at 3 V Power Consumption**
- **CMOS-Compatible Power-Down to 200 µW typ**
- **150 ns Enable/Disable Time**

APPLICATIONS
- **Low Power PHP, GSM, TDMA, FM, or PM Receivers**
- **Battery-Powered Instrumentation**

GENERAL DESCRIPTION

The AD608 provides both a low power, low distortion, low noise mixer and a complete, monolithic logarithmic/limiting amplifier using a "successive-detection" technique. It provides both a high speed RSSI (Received Signal Strength Indicator) output with 90 dB dynamic range and a hard-limited output. The RSSI output is from a two-pole post demodulation low-pass filter and provides a loadable output voltage of +0.2 V to +2 V. The AD608 operates from a single 2.7 V to 6 V supply at a typical power level of 21 mW at 3 V.

The RF and LO bandwidths both exceed 450 MHz. In a typical IF application, the AD608 will accept the output of a 240 MHz SAW filter and downconvert it to a nominal 10.7 MHz IF with a conversion gain of 26 dB (Z_{IF} = 165 Ω). The AD608's logarithmic/limiting amplifier section handles any IF from LF to as high as 50 MHz.

The mixer is a doubly balanced "Gilbert-Cell" type and operates linearly for RF inputs spanning –95 dBm to –15 dBm. It has a nominal –5 dBm third-order intercept. An on-board LO preamplifier requires only –6 dBm of LO drive. The mixer's current output drives a reverse-terminated, industry-standard 10.7 MHz, 330 Ω filter and can drive reverse-terminated filter impedances as low as 220 Ω.

The nominal logarithmic scaling is such that the output is +0.2 V for a sinusoidal input of –75 dBm and +2.0 V at an input of +15 dBm; over this range the logarithmic conformance is typically ±1 dB. The logarithmic slope is proportional to the supply voltage. A feedback loop automatically nulls the input offset of the first stage down to the submicrovolt level.

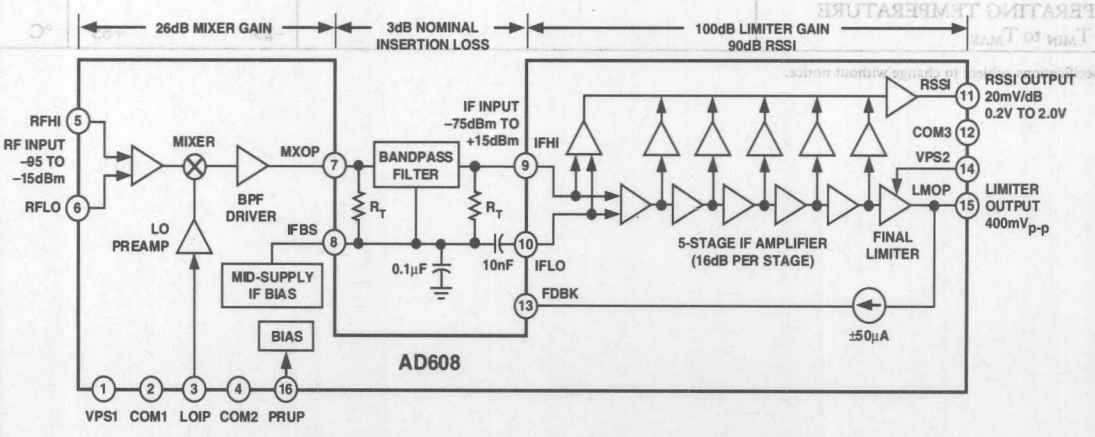
The AD608's limiter output provides a hard-limited signal output at 400 mV p-p. The voltage gain of the limiting amplifier to this output is more than 100 dB. Transition times are 7 ns, and the phase is stable to within ±3° at 10.7 MHz for signals from –75 dBm to +15 dBm.

It is enabled by a CMOS logic-level voltage input, with a response time of 150 ns. When disabled, the standby power is reduced to 200 µW within 400 ns.

The AD608 is specified for the industrial temperature range of –25°C to +85°C and is available in 16-pin plastic SOICs.

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



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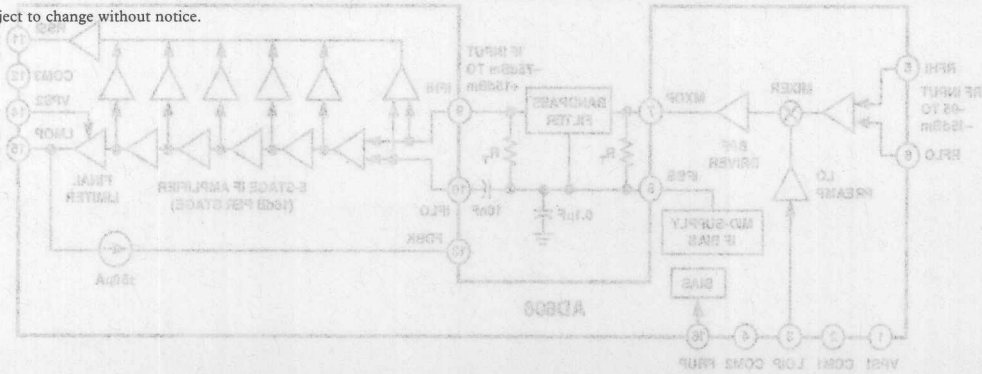
MIXER PERFORMANCE	f_{RF} = 240 MHz, f_{LO} = 229.3 MHz				
Conversion Gain	Doubly Terminated 330 Ω IF Filter			26	dB
Input Referred Noise	AC Short-Circuited Input		2.5		nV/√Hz
Equivalent Noise Resistance			375		Ω
Third-Order Intercept			–5		dBm
Input Resistance			4		kΩ
Input Capacitance			3		pF
LIMITER PERFORMANCE					
Gain	Full Temperature and Supply Range	100	110		
Input Referred Noise	AC Short-Circuited Input		1.75		nV/√Hz
Input Resistance			10		kΩ
Input Capacitance			2		pF
Phase Variation	–75 dBm to +15 dBm Input Signal at 10.7 MHz		±3		Degree
DC Level	Center of Output Swing (VPOS-1)		2		V
Output Level			400		mV p-p
Rise and Fall Times	Driving a 5 pF Load		7		ns
RSSI PERFORMANCE	At 10.7 MHz				
Nominal Slope	Proportional to VPOS		20		mV/dB
Nominal Intercept			–85		dBm
Minimum RSSI Voltage	–75 dBm Input Signal		0.2		V
Maximum RSSI Voltage	+15 dBm Input Signal		2.0		V
Logarithmic Linearity Error	–75 dBm to +15 dBm Input Signal		±1		dB
RSSI Response Time	10% to 90%		200		ns
Output Impedance	At Midscale		250		Ω
POWER-DOWN INTERFACE					
Logical Threshold	System Active on Logical High		1.5		V
Input Current	For Logical High		75		µA
Power-Up Response Time	Active Limiter Output		150		ns
Power-Down Response Time	To 200 µA Supply Current		400		ns
Power-Down Current			100		µA
POWER SUPPLY					
Operating Range		2.7		6	V
Powered Up Current	VPOS = 3 V		7.3		mA
OPERATING TEMPERATURE					
T_{MIN} to T_{MAX}		–25		+85	°C

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA



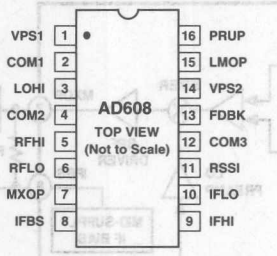
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Internal Power Dissipation[2] ..... 600 mW
Operating Temperature Range ..... –25°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature, Soldering (60 sec) ..... +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics: 16-pin SOIC package; θ_{JA} = TBD.



ORDERING GUIDE

Model	Temperature Range	Package Option*
AD608AR	–25°C to +85°C	16-Pin Narrow-Body SOIC (R-16A)

*For outline information see Package Information section.

PIN DESCRIPTION

Pin	Mnemonic	Description
1	VPS1	Positive Supply Input
2	COM1	Common
3	LOHI	Local Oscillator Input Connection
4	COM2	Common
5	RFHI	RF Input, Noninverting
6	RFLO	RF Input, Inverting
7	MXOP	Mixer Output
8	IFBS	Midpoint Supply Bias Output
9	IFHI	IF Input, Noninverting
10	IFLO	IF Input, Inverting
11	RSSI	Received Signal Strength Indicator Output
12	COM3	Output Common
13	FDBK	Feedback Loop Output
14	VPS2	Limiter Positive Supply Input
15	LMOP	Limiter Output
16	PRUP	Power-Up

PRELIMINARY TECHNICAL DATA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD608 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

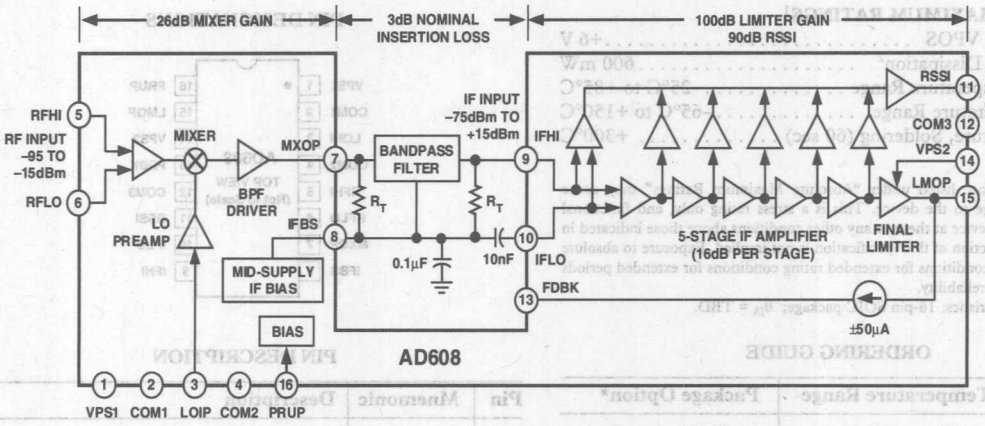


Figure 1. AD608 Functional Block Diagram

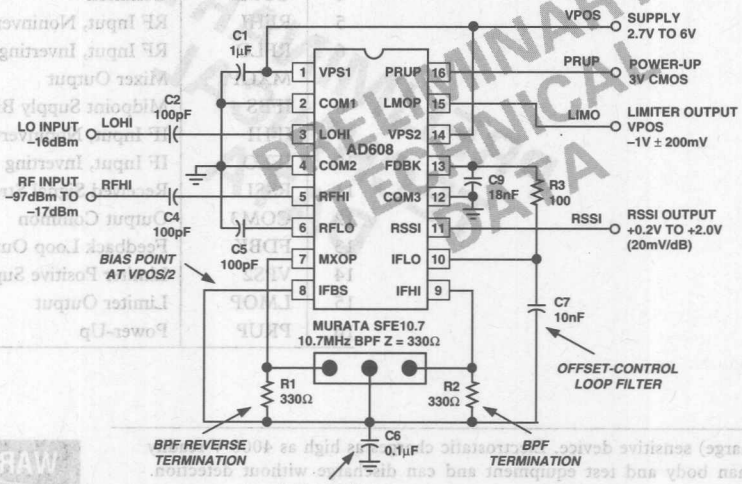


Figure 2. AD608 Application Circuit

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

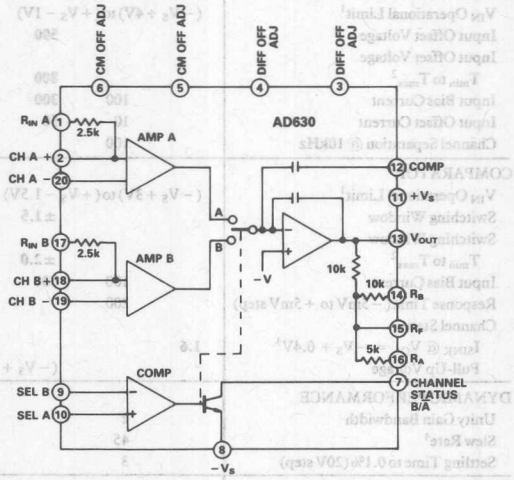
Balanced Modulator/Demodulator

AD630

FEATURES

Recovers Signal from +100dB Noise
2MHz Channel Bandwidth
45V/μs Slew Rate
−120dB Crosstalk @ 1kHz
Pin Programmable Closed Loop Gains of ±1 and ±2
0.05% Closed Loop Gain Accuracy and Match
100μV Channel Offset Voltage (AD630BD)
350kHz Full Power Bandwidth
Chips Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD630 is a high precision balanced modulator which combines a flexible commutating architecture with the accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase sensitive detection, lock-in amplification and square wave multiplication. A network of on-board applications resistors provides precision closed loop gains of ±1 and ±2 with 0.05% accuracy (AD630B). These resistors may also be used to accurately configure multiplexer gains of +1, +2, +3 or +4. Alternatively, external feedback may be employed allowing the designer to implement his own high gain or complex switched feedback topologies.

The AD630 may be thought of as a precision op amp with two independent differential input stages and a precision comparator which is used to select the active front end. The rapid response time of this comparator coupled with the high slew rate and fast settling of the linear amplifiers minimize switching distortion. In addition, the AD630 has extremely low crosstalk between channels of −100dB @ 10kHz.

The AD630 is intended for use in precision signal processing and instrumentation applications requiring wide dynamic range. When used as a synchronous demodulator in a lock-in amplifier configuration, it can recover a small signal from 100dB of interfering noise (see lock-in amplifier application). Although optimized for operation up to 1kHz, the circuit is useful at frequencies up to several hundred kilohertz.

Other features of the AD630 include pin programmable frequency compensation, optional input bias current compensation resistors, common mode and differential offset voltage adjustment, and a channel status output which indicates which of the two differential inputs is active. This device is now available to Standard Military Drawing (DESC) numbers 5962–8980701RA and 5962–89807012A.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. The configuration of the AD630 makes it ideal for signal processing applications such as: balanced modulation and demodulation, lock-in amplification, phase detection, and square wave multiplication.
2. The application flexibility of the AD630 makes it the best choice for many applications requiring precisely fixed gain, switched gain, multiplexing, integrating-switching functions, and high-speed precision amplification.
3. The 100dB dynamic range of the AD630 exceeds that of any hybrid or IC balanced modulator/demodulator and is comparable to that of costly signal processing instruments.
4. The op-amp format of the AD630 ensures easy implementation of high gain or complex switched feedback functions. The application resistors facilitate the implementation of most common applications with no additional parts.
5. The AD630 can be used as a two channel multiplexer with gains of +1, +2, +3 or +4. The channel separation of 100dB @ 10kHz approaches the limit which is achievable with an empty IC package.
6. The AD630 has pin-strappable frequency compensation (no external capacitor required) for stable operation at unity gain without sacrificing dynamic performance at higher gains.
7. Laser trimming of comparator and amplifying channel offsets eliminates the need for external nulling in most cases.

AD630–SPECIFICATIONS (@ +25°C and $\pm V_S = \pm 15V$ unless otherwise noted)

Model	AD630J/A			AD630K/B			AD630S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN										
Open Loop Gain	90	110		100	120		90	110		dB
±1, ±2 Closed Loop Gain Error		0.1				0.05		0.1		%
Closed Loop Gain Match		0.1				0.05		0.1		%
Closed Loop Gain Drift		2			2			2		ppm°C
CHANNEL INPUTS										
V_{IN} Operational Limit[1]	$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			Volts
Input Offset Voltage			500			100			500	µV
Input Offset Voltage										
T_{min} to T_{max}[2]			800			160			1000	µV
Input Bias Current		100	300		100	300		100	300	nA
Input Offset Current		10	50		10	50		10	50	nA
Channel Separation @ 10kHz		100			100			100		dB
COMPARATOR										
V_{IN} Operational Limit[1]	$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.3V)$			Volts
Switching Window			±1.5			±1.5			±1.5	mV
Switching Window										
T_{min} to T_{max}[2]			±2.0			±2.0			±2.5	mV
Input Bias Current		100	300		100	300		100	300	nA
Response Time (−5mV to +5mV step)		200			200			200		ns
Channel Status										
I_{SINK} @ $V_{OL} = -V_S + 0.4V$[3]	1.6			1.6			1.6			mA
Pull-Up Voltage			$(-V_S+33V)$			$(-V_S+33V)$			$(-V_S+33V)$	Volts
DYNAMIC PERFORMANCE										
Unity Gain Bandwidth		2			2			2		MHz
Slew Rate[4]		45			45			45		V/µs
Settling Time to 0.1% (20V step)		3			3			3		µs
OPERATING CHARACTERISTICS										
Common-Mode Rejection	85	105		90	110		90	110		dB
Power Supply Rejection	90	110		90	110		90	110		dB
Supply Voltage Range	±5		±16.5	±5		±16.5	±5		±16.5	Volts
Supply Current		4	5		4	5		4	5	mA
OUTPUT VOLTAGE, @ $R_L = 2k\Omega$										
T_{min} to T_{max}[2]	±10			±10			±10			Volts
Output Short Circuit Current		25			25			25		mA
TEMPERATURE RANGES										
Rated Performance – N Package	0		+70	0		+70		N/A		°C
D Package	−25		+85	−25		+85	−55		+125	°C

NOTES

[1]If one terminal of each differential channel or comparator input is kept within these limits the other terminal may be taken to the positive supply.

[2]These parameters are guaranteed but not tested for J and K grades. For A, B and S grades they are tested.

[3]I_{SINK} @ $V_{OL} = (-V_S + 1)$ volt is typically 4mA.

[4]Pin 12 Open. Slew rate with Pins 12 & 13 shorted is typically 35V/µs.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

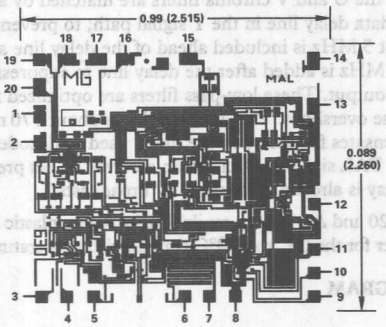
Supply Voltage	±18V
Internal Power Dissipation	600mW
Output Short Circuit to Ground	Indefinite
Storage Temperature, Ceramic Package	−65°C to +150°C
Storage Temperature, Plastic Package	−55°C to +125°C
Lead Temperature, 10 sec. Soldering	+300°C
Max Junction Temperature	+150°C

THERMAL CHARACTERISTICS

	θ_{JC}	θ_{JA}
20-Pin Plastic DIP (N)	24°C/W	61°C/W
20-Pin Ceramic DIP (D)	35°C/W	120°C/W
20-Pin Leadless Chip Carrier (E)	35°C/W	120°C/W

CHIP METALIZATION AND PINOUT

Dimensions shown in inches and (mm).
Contact factory for latest dimensions

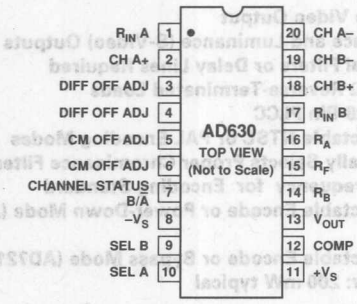


CHIP AVAILABILITY

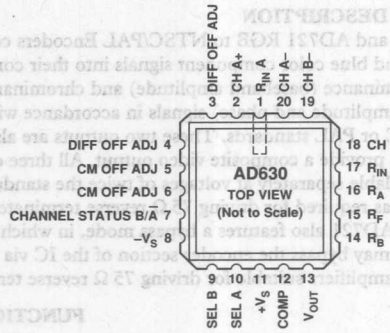
The AD630 is available in laser trimmed, passivated chip form. The figure shows the AD630 metalization pattern, bonding pads and dimensions. AD630 chips are available; consult factory for details.

PIN CONFIGURATIONS

20-Pin Plastic DIP (N-20)
20-Pin Side Brazed DIP (D-20)



20-Contact LCC (E-20A)



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD630JN	0°C to +70°C	Plastic DIP	N-20
AD630KN	0°C to +70°C	Plastic DIP	N-20
AD630AD	−25°C to +85°C	Side Brazed DIP	D-20
AD630BD	−25°C to +85°C	Side Brazed DIP	D-20
AD630SD	−55°C to +125°C	Side Brazed DIP	D-20
AD630SD/883B	−55°C to +125°C	Side Brazed DIP	D-20
5962-8980701RA	−55°C to +125°C	Side Brazed DIP	D-20
AD630SE/883B	−55°C to +125°C	LCC	E-20A
5962-89807012A	−55°C to +125°C	LCC	E-20A
AD630J Chip	0°C to +70°C	Chip	
AD630S Chip	−55°C to +125°C	Chip	

*For outline information see Package Information section.

21

FEATURES

Composite Video Output
Chrominance and Luminance (S-Video) Outputs
No External Filters or Delay Lines Required
Drives 75 Ω Reverse-Terminated Loads
Compact 28-Pin PLCC
Logic Selectable NTSC or PAL Encoding Modes
Automatically Selects Proper Chrominance Filter Cutoff Frequency for Encoding Standard
Logic Selectable Encode or Power-Down Mode (AD720 Only)
Logic Selectable Encode or Bypass Mode (AD721 Only)
Low Power: 200 mW typical

APPLICATIONS

RGB to NTSC or PAL Encoding
Drive RGB Signals into 75 Ω Load (AD721 Only)

PRODUCT DESCRIPTION

The AD720 and AD721 RGB to NTSC/PAL Encoders convert red, green and blue color component signals into their corresponding luminance (baseband amplitude) and chrominance (subcarrier amplitude and phase) signals in accordance with either NTSC or PAL standards. These two outputs are also combined to provide a composite video output. All three outputs are available separately at voltages of twice the standard signal levels as required for driving 75 Ω reverse terminated cables. The AD721 also features a bypass mode, in which the RGB inputs may bypass the encoder section of the IC via three gain-of-two amplifiers suitable for driving 75 Ω reverse terminated cables.

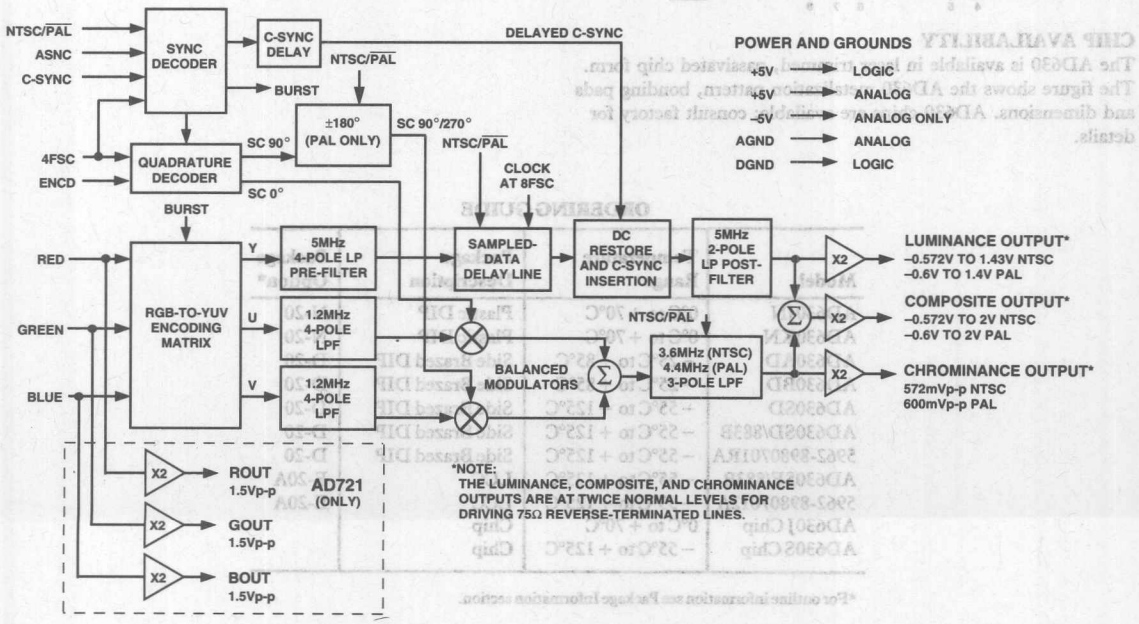
The AD720 and AD721 provide a complete, fully calibrated function, requiring only termination resistors, bypass capacitors, a clock input at four times the subcarrier frequency, and a composite sync pulse. There are two control inputs: one input selects the TV standard (NTSC/PAL) and the other (ENCD) powers down most sections of the chip when the encoding function is not in use (AD720) or activates the triple bypass buffer to drive the RGB signals when RGB encoding is not required (AD721). All logical inputs are CMOS compatible. The chip operates from ±5 V supplies.

All required low-pass filters are on chip. After the input signals pass through a precision RGB to YUV encoding matrix, two on-chip low-pass filters limit the bandwidth of the U and V color difference signals to 1.2 MHz prior to quadrature modulation of the color subcarrier; a third low-pass filter at 3.6 MHz (NTSC) or 4.4 MHz (PAL) follows the modulators to limit the harmonic content of the output.

Delays in the U and V chroma filters are matched by an on-chip sampled data delay line in the Y signal path; to prevent aliasing, prefilter at 5 MHz is included ahead of the delay line and a post filter at 5 MHz is added after the delay line to suppress harmonics in the output. These low-pass filters are optimized for minimum pulse overshoot. The overall delay is about 170 ns, which precompensates for delays in the filters used to decode the NTSC or PAL signal in a television receiver. (This precompensation delay is already present in TV broadcasts.)

The AD720 and AD721 are available in a 28-pin plastic leaded chip carrier for the 0°C to +70°C commercial temperature range.

FUNCTIONAL BLOCK DIAGRAM



SPECIFICATIONS (T_A = +25°C and supplies = ±5 V unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUTS (RDIN, GRIN, BLIN)					
Input Amplitude	NTSC		714		mV
	PAL		700		mV
Input Resistances[1]					
RDIN with Respect to AGND			2.3		kΩ
GRIN with Respect to AGND			4.2		kΩ
BLIN with Respect to AGND			4.2		kΩ
Input Capacitance			5		pF
LOGIC INPUTS (C-SYNC, 4FSC, ENCD, NTSC)					
Logic LO Input Voltage				**1**	V
Logic HI Input Voltage		**4**			V
Logic LO Input Current (DC)			**<1**		µA
Logic HI Input Current (DC)			**<1**		µA
BYPASS AMPLIFIERS (AD721 Only)					
Gain Error	Nominal Gain of ×2[2]	**–5**		**+5**	%
Small Signal –3 dB Bandwidth		100			MHz
Output Offset Voltage (Active State)		**–50**		**+50**	mV
Output Voltage (Inactive State)		**–50**		**+50**	mV
VIDEO OUTPUTS[3] (LUMA, CRMA, CMPS)					
Luminance (LUMA) Output					
Bandwidth			5		MHz
Gain Error		**–5**	±1	**+5**	%
Linearity			±0.1		%
Sync Level	NTSC	**252**	286	**320**	mV
	PAL		300		mV
Chrominance (CRMA) Output					
Bandwidth	NTSC		3.6		MHz
	PAL		4.4		MHz
Color Burst Amplitude	NTSC	**257**	286	**315**	mV p-p
	PAL		300		mV p-p
Absolute Gain Error		**–15**	±5	**+15**	%
Absolute Phase Error			±3		Degrees
Chroma/Luma Time Alignment[4]	NTSC		–170		ns
Composite Output					
Absolute Gain Error		**–5**	±1	**+5**	%
Differential Gain	With Respect to Chroma Channel		0.1		%
Differential Phase	With Respect to Chroma Channel		0.1		Degrees
Output Offset Voltage	Chroma, Luma, or Composite Outputs		50	**100**	mV
Chroma Feedthrough	Monochrome Input		20	**55**	mV p-p
POWER SUPPLIES (APOS, DPOS, VNEG)					
Recommended Supply Range	Dual Supply	±4.75		±5.25	V
Full Output Current[5]	–5 V Supply		35		mA
	+5 V Supply		67		mA
Zero Signal Quiescent Current	–5 V Supply	**10**	20	**35**	mA
	+5 V Supply	**10**	20	**35**	mA
Bypass Mode Quiescent Current	–5 V Supply		14	**20**	mA
(AD721 Only)	+5 V Supply		14	**20**	mA

NOTES

[1]Input scaling resistors provide best scaling accuracy when source resistance is 37.5 Ω (75 Ω reverse-terminated input).

[2]Required for driving a 75 Ω double reverse terminated load.

[3]All outputs are measured at a reverse-terminated load; voltages at IC pins are twice those specified here.

[4]This is a predistortion (per FCC specifications) that compensates for the chroma/luma delay in the low-pass filter that separates the luminance and chrominance signals in a television receiver.

[5]CRMA, LUMA, and CMPS outputs are all connected to 75 Ω reverse-terminated loads; full-white signal for entire field.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage $\pm V_S$ ..... ±6 V
Internal Power Dissipation ..... 600 mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature, Soldering 60 sec ..... +300°C

NOTE

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

Thermal characteristics: 28-pin plastic package: θ_{JA} = 100°C.

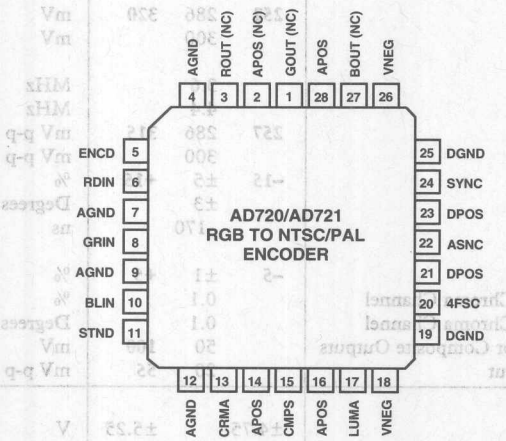
ORDERING GUIDE

Model	Temperature Range	Package	Package Option*
AD720JP	0°C to +70°C	28-Pin PLCC	P-28A
AD721JP	0°C to +70°C	28-Pin PLCC	P-28A

*For outline information see Package Information section.

PIN CONNECTIONS

28-Lead Plastic Leaded Chip Carrier (PLCC) Package
P-28A



NOTE:
CONNECTIONS IN ( ) PERTAIN ONLY TO AD720

PIN DESCRIPTIONS

Pin	Mnemonic*	Description*
1	(NC) GOUT	(No Connection) Green Bypass Buffer
2	(NC) APOS	(No Connection) Analog Positive Supply; +5 V ± 5%
3	(NC) ROUT	(No Connection) Red Bypass Buffer
4	AGND	Analog Ground Connection
5	ENCD	A Logical High Enables the NTSC/PAL Encode Mode (A Logical Low Powers Down the Chip)
6	RDIN	A Logical Low Enables the RGB Bypass Mode Red Component Video Input 0 mV to 714 mV for NTSC 0 mV to 700 mV for PAL
7	AGND	Analog Ground Connection
8	GRIN	Green Component Video Input 0 mV to 714 mV for NTSC 0 mV to 700 mV for PAL
9	AGND	Analog Ground Connection
10	BLIN	Blue Component Video Input 0 mV to 714 mV for NTSC 0 mV to 700 mV for PAL
11	STND	A Logical High Input Selects NTSC Encoding A Logical Low Input Selects PAL Encoding CMOS Logic Levels
12	AGND	Analog Ground Connection
13	CRMA	Chrominance Output; Subcarrier Only** 572 mV Peak-to-Peak for NTSC 600 mV Peak-to-Peak for PAL
14	APOS	Analog Positive Supply; +5 V ± 5%
15	CMPS	Composite Video Output** –572 mV to 2 V for NTSC –600 mV to 2 V for PAL
16	APOS	Analog Positive Supply; +5 V ± 5%
17	LUMA	Luminance Plus SYNC Output** –572 mV to 1.43 V for NTSC –600 mV to 1.4 V for PAL
18	VNEG	System Negative Supply; –5 V ± 5%
19	DGND	Digital Ground Connection
20	4FSC	Clock Input at Four Times the Subcarrier Frequency 14.318 180 MHz for NTSC 17.734 480 MHz for PAL CMOS Logic Levels
21	DPOS	Digital Positive Supply; +5 V ± 5%
22	ASNC	A Logical High Input Resets the Subcarrier Phase Every Frame A Logical Low Input Resets the Subcarrier Phase Every Fourth Frame CMOS Logic Levels
23	DPOS	Digital Positive Supply; +5 V ± 5%
24	SYNC	Input for Composite Television Synchronization Pulses Negative Sync Pulses CMOS Logic Levels
25	DGND	Digital Ground Connections (One of Two)
26	VNEG	System Negative Supply; –5 V ± 5%
27	(NC) BOUT	(No Connection) Blue Bypass Buffer
28	APOS	Analog Positive Supply; +5 V ± 5%

*( ) pertain only to AD720.
**The luminance, chrominance, and composite outputs are at twice normal levels for driving 75 Ω reverse-terminated lines.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD720/AD721 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

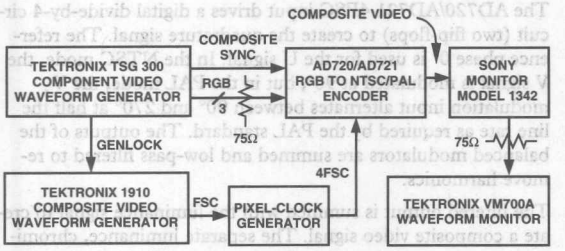


Figure 1. AD720/AD721 Evaluation Setup

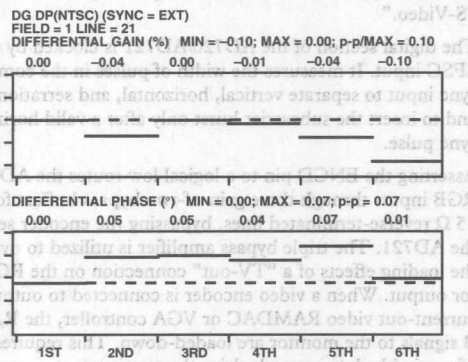


Figure 2. Composite Output Differential Phase and Gain, NTSC (Nulled to Chroma Output)

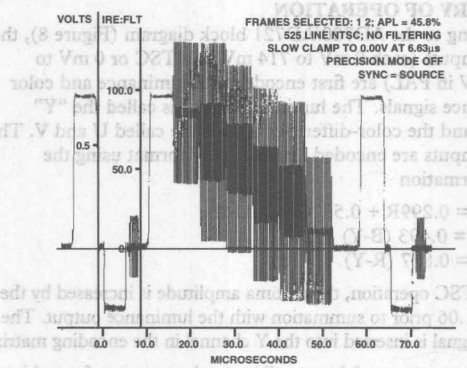


Figure 4. 100% Color Bars, NTSC

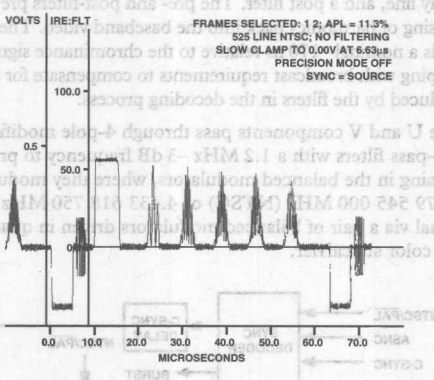


Figure 5. Multipulse, NTSC

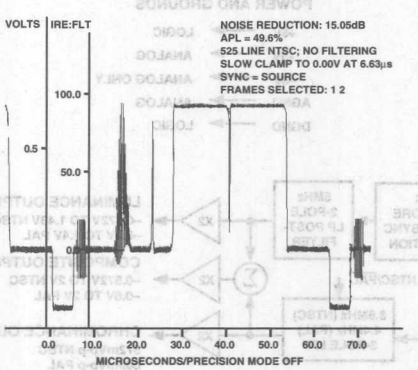


Figure 3. Modulated Pulse and Bar, NTSC

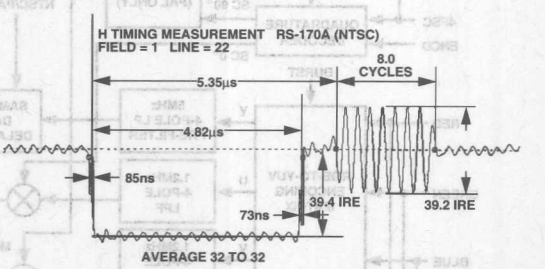


Figure 6. Horizontal Timing, NTSC

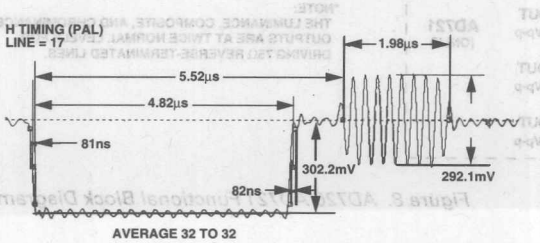


Figure 7. Horizontal Timing, PAL

RGB inputs (each 0 mV to 714 mV in NTSC or 0 mV to 700 mV in PAL) are first encoded into luminance and color difference signals. The luminance signal is called the "Y" signal and the color-difference signals are called U and V. The RGB inputs are encoded into the YUV format using the transformation

$$Y = 0.299R + 0.587G + 0.114B$$
$$U = 0.493\ (B-Y)$$
$$V = 0.877\ (R-Y)$$

For NTSC operation, the chroma amplitude is increased by the factor 1.06 prior to summation with the luminance output. The burst signal is inserted into the Y channel in the encoding matrix.

The three outputs of the encoding matrix, now transformed into Y, U, and V components, take two paths. The Y (luminance) signal is passed through a delay line consisting of a prefilter, a sampled-data delay line, and a post filter. The pre- and post-filters prevent aliasing of harmonics back into the baseband video. The overall delay is a nominal –170 ns relative to the chrominance signal, in keeping with broadcast requirements to compensate for delays introduced by the filters in the decoding process.

The U and V components pass through 4-pole modified Bessel low-pass filters with a 1.2 MHz –3 dB frequency to prevent aliasing in the balanced modulators, where they modulate a 3.579 545 000 MHz (NTSC) or 4.433 618 750 MHz (PAL) signal via a pair of balanced modulators driven in quadrature by the color subcarrier.

ence phase 0° is used for the U signal. In the NTSC mode, the V signal is modulated at 90°, but in the PAL mode, the V modulation input alternates between 90° and 270° at half the line rate as required by the PAL standard. The outputs of the balanced modulators are summed and low-pass filtered to remove harmonics.

The filtered output is summed with the luminance signal to create a composite video signal. The separate luminance, chrominance, and composite video signals are amplified by gain-of-two amplifiers for driving 75 Ω reverse-terminated lines. The separate luminance and chrominance outputs together are known as "S-Video."

The digital section of the AD720/AD721 is clocked by the 4FSC input. It measures the width of pulses in the composite sync input to separate vertical, horizontal, and serration pulses and to insert the subcarrier burst only after a valid horizontal sync pulse.

Asserting the ENCD pin to a logical low routes the AD721's RGB inputs through three gain-of-two bypass buffers for driving 75 Ω reverse-terminated lines, bypassing the encoder section of the AD721. The triple bypass amplifier is utilized to overcome the loading effects of a "TV-out" connection on the RGB monitor output. When a video encoder is connected to outputs of a current-out video RAMDAC or VGA controller, the R, G, and B signals to the monitor are loaded-down. This requires the use of a gain block to properly drive the monitor.

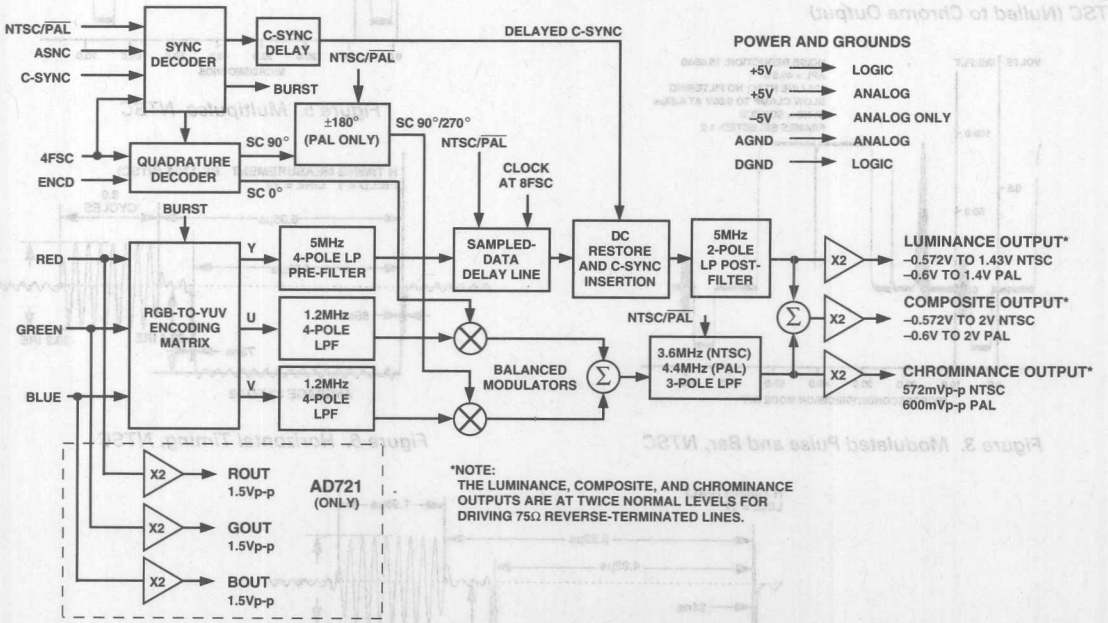


Figure 8. AD720/AD721 Functional Block Diagram

APPLYING THE AD720/AD721

Figure 9 shows the application of the AD720 and Figure 10 shows the application of the AD721. Note that the AD720 and AD721 differ from other analog encoders because they are dc coupled. This means that, for example, the expected RGB inputs are 0 mV to 714 mV in NTSC and 0 mV to 700 mV in PAL. The luminance, chrominance, and composite outputs are also dc coupled. These outputs can drive a 75 Ω reverse-terminated load. Unused outputs should be terminated with 150 Ω resistors.

The RGB data must be supplied to the AD720/AD721 at NTSC or PAL rates, interlaced format. Various VGA chip set vendors support this mode of operation. Most computers supply RGB outputs in noninterlaced format at higher data rates than NTSC and PAL, which means that "outboard" encoders must supply some form of timing conversion before the RGB data reaches the AD720/AD721.

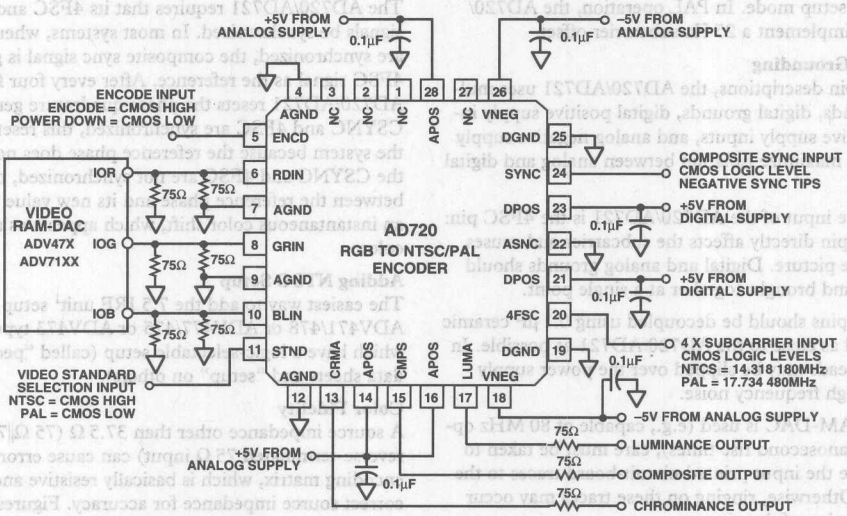


Figure 9. AD720 Application

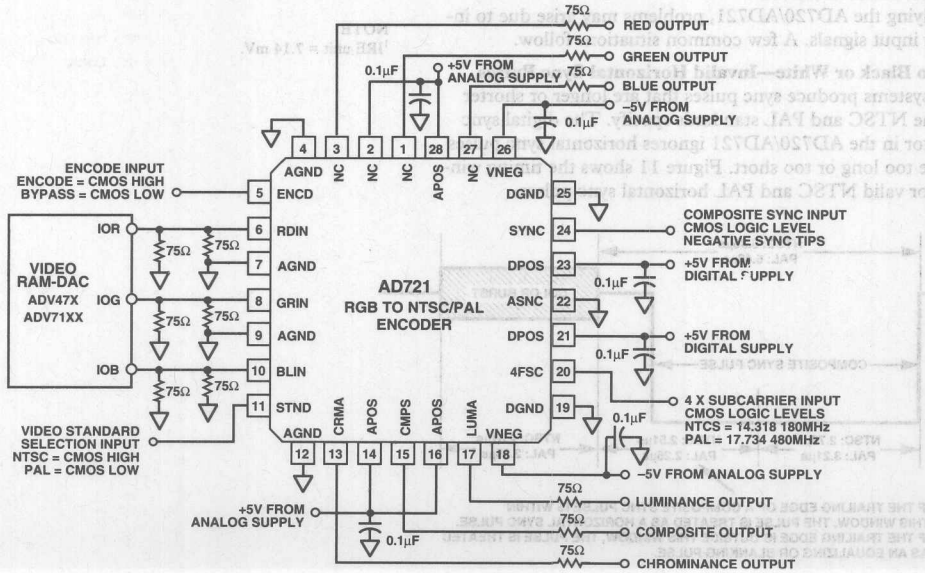


Figure 10. AD721 Application

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Note also that the AD720/AD721 does not have internal dc restoration and does not accept sync on green. The composite sync input is a separate, CMOS logical-level input and must be synchronized with the 4FSC input, which serves as the master clock for the AD720/AD721.

The AD720/AD721 does not implement two elements of the PAL and NTSC standards. In NTSC operation, it does not support the 7.5 IRE unit setup (1 IRE unit = 7.14 mV)—this must be added via software using the RGB inputs. Many RAM-DACs, such as the Analog Devices ADV471 and ADV478, offer a logic-selectable setup mode. In PAL operation, the AD720/AD721 does not implement a 25 Hz subcarrier offset.

Decoupling and Grounding

Referring to the pin descriptions, the AD720/AD721 uses multiple analog grounds, digital grounds, digital positive supply inputs, analog positive supply inputs, and analog negative supply inputs in order to maximize isolation between analog and digital signal paths.

The most sensitive input of the AD720/AD721 is the 4FSC pin: any noise on this pin directly affects the subcarrier and causes degradation of the picture. Digital and analog grounds should be kept separate and brought together at a single point.

All power supply pins should be decoupled using 0.1 µF ceramic capacitors located as close to the AD720/AD721 as possible. In addition, ferrite beads may be slipped over the power supply leads to reduce high frequency noise.

If a high speed RAM-DAC is used (e.g., capable of 80 MHz operation with subnanosecond rise times), care must be taken to properly terminate the input printed-circuit-board traces to the AD720/AD721. Otherwise, ringing on these traces may occur and cause degradation of the picture.

APPLICATIONS HINTS

In applying the AD720/AD721, problems may arise due to incorrect input signals. A few common situations follow.

Fade to Black or White—Invalid Horizontal Sync Pulses

Some systems produce sync pulses that are longer or shorter than the NTSC and PAL standards specify. The digital sync separator in the AD720/AD721 ignores horizontal sync pulses that are too long or too short. Figure 11 shows the timing windows for valid NTSC and PAL horizontal sync pulses.

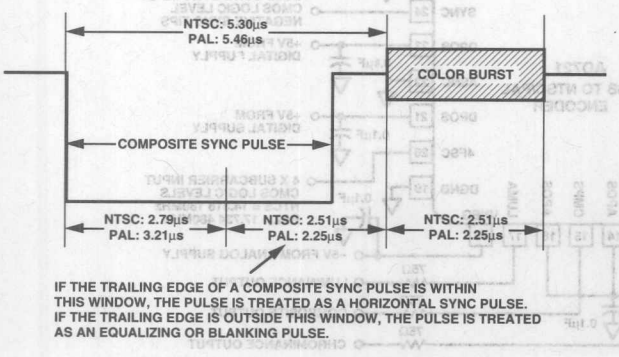


Figure 11. NTSC and PAL Timing for Valid Horizontal Sync Pulses

When the horizontal sync pulses are too long or too short, a dc offset voltage (due to charge storage) increases on the output of the sampled data delay line's auto-zero amplifier. Normally, this offset voltage is removed at the beginning of every line, as signified by the horizontal sync pulse. Without the horizontal sync pulse, the dc offset on the auto-zero amplifier increases over time (usually about three to five minutes) until it overrides the luminance information. The end result is a slow fade to black or white.

Color Flickering—Asynchronous Operation

The AD720/AD721 requires that its 4FSC and composite sync signals be synchronized. In most systems, when the two signals are synchronized, the composite sync signal is generated using a 4FSC signal as the reference. After every four frames, the AD720/AD721 resets the phase quadrature generator. When the CSYNC and 4FSC are synchronized, this reset is transparent to the system because the reference phase does not change. When the CSYNC and 4FSC are not synchronized, the difference between the reference phase and its new value upon reset causes an instantaneous color shift, which appears as a flickering in the color.

Adding NTSC Setup

The easiest way to add the 7.5 IRE unit[1] setup is to use a ADV471/478 or ADV477/475 or ADV473 type RAM-DAC, which have a logic-selectable setup (called "pedestal" on some data sheets and "setup" on others).

Color Fidelity

A source impedance other than 37.5 Ω (75 Ω‖75 Ω—a reverse-terminated 75 Ω input) can cause errors in the YUV encoding matrix, which is basically resistive and depends on the correct source impedance for accuracy. Figures 9 and 10 show the correct interface between a RAM-DAC and the AD720 and AD721 respectively, using 75 Ω reverse-terminated connections.

NOTE
[1]IRE unit = 7.14 mV.

ANALOG DEVICES

Low Distortion Mixer

AD831

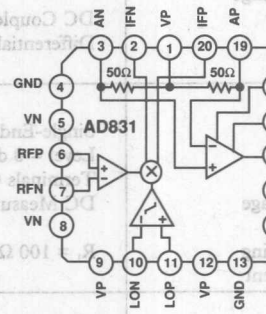
FEATURES

Doubly-Balanced Mixer
Low Distortion
+24 dBm Third Order Intercept (IP3)
+10 dBm 1 dB Compression Point
Low LO Drive Required: –10 dBm
Bandwidth
500 MHz RF and LO Input Bandwidths
250 MHz Differential Current IF Output
DC to >200 MHz Single-Ended Voltage IF Output
Single or Dual Supply Operation
DC Coupled Using Dual Supplies
All Ports May Be DC Coupled
No Lower Frequency Limit—Operation to DC
User-Programmable Power Consumption

APPLICATIONS

High Performance RF/IF Mixer
Direct to Baseband Conversion
Image-Reject Mixers
I/Q Modulators and Demodulators

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD831 is a low distortion, wide dynamic range, monolithic mixer for use in such applications as RF to IF down conversion in HF and VHF receivers, the second mixer in DMR base stations, direct-to-baseband conversion, quadrature modulation and demodulation, and doppler-shift detection in ultrasound imaging applications. The mixer includes an LO driver and a low-noise output amplifier and provides both user-programmable power consumption and 3rd-order intercept point.

The AD831 provides a +24 dBm third-order intercept point for –10 dBm LO power, thus improving system performance and reducing system cost compared to passive mixers, by eliminating the need for a high power LO driver and its attendant shielding and isolation problems.

The RF, IF, and LO ports may be dc or ac coupled when the mixer is operating from ±5 V supplies or ac coupled when operating from a single supply of 9 V minimum. The mixer operates with RF and LO inputs as high as 500 MHz.

The mixer's IF output is available as either a differential current output or a single-ended voltage output. The differential output is from a pair of open collectors and may be ac coupled via a transformer or capacitor to provide a 250 MHz output bandwidth. In down-conversion applications, a single capacitor connected across these outputs implements a low-pass filter to reduce harmonics directly at the mixer core, simplifying output filtering. When building a quadrature-amplitude modulator or image reject mixer, the differential current outputs of two AD831s may be summed by connecting them together.

An integral low noise amplifier provides a single-ended voltage output and can drive such low impedance loads as filters, 50 Ω amplifier inputs, and A/D converters. Its small signal bandwidth exceeds 200 MHz. A single resistor connected between pins OUT and FB sets its gain. The amplifier's low dc offset allows its use in such direct-coupled applications as direct-to-baseband conversion and quadrature-amplitude demodulation.

The mixer's SSB noise figure is 12 dB using its output amplifier and optimum source impedance. Unlike passive mixers, the AD831 has no insertion loss and does not require an external diplexer or passive termination.

A programmable-bias feature allows the user to reduce power consumption, with a reduction in the 1 dB compression point and third-order intercept. This permits a tradeoff between dynamic range and power consumption. For example, the AD831 may be used as a second mixer in cellular and two-way radio base stations at reduced power while still providing a substantial performance improvement over passive solutions.

PRODUCT HIGHLIGHTS

1. –10 dBm LO Drive for a +24 dBm Output Referred Third Order Intercept Point
2. Single-Ended Voltage Output
3. High Port-to-Port Isolation
4. No Insertion Loss
5. Single or Dual Supply Operation

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RF INPUT					
Bandwidth	–10 dBm Signal Level, IP3 ≥ +20 dBm 10.7 MHz IF and High Side Injection See Figure 1		400		MHz
Maximum Input Level			10		dBm
Common-Mode Range				±1	V
Bias Current	DC Coupled		160	500	µA
Resistance	Differential or Common Mode		1.3		kΩ
Capacitance			2		pF
IF OUTPUT					
Bandwidth	Single-Ended Voltage Output, –3 dB Level = 0 dBm, R_L = 100 Ω		200		MHz
Conversion Gain	Terminals OUT and VFB Connected		0		dB
Output Offset Voltage	DC Measurement; LO Input Switched ±1	–40	15	+40	mV
Slew Rate			300		V/µs
Output Voltage Swing	R_L = 100 Ω, Unity Gain		±1.4		V
Short Circuit Current			75		mA
LO INPUT					
Bandwidth	–10 dBm Input Signal Level 10.7 MHz IF and High Side Injection		400		MHz
Maximum Input Level		–1		+1	V
Common Mode Range		–1		+1	V
Minimum Switching Level	Differential Input Signal		200		mV p-p
Bias Current	DC Coupled		17	50	µA
Resistance	Differential or Common Mode		500		Ω
Capacitance			2		pF
ISOLATION BETWEEN PORTS					
LO to RF	LO = 100 MHz, R_S = 50 Ω, 10.7 MHz IF		70		dB
LO to IF	LO = 100 MHz, R_S = 50 Ω, 10.7 MHz IF		30		dB
RF to IF	RF = 100 MHz, R_S = 50 Ω, 10.7 MHz IF		45		dB
DISTORTION AND NOISE	LO = –10 dBm, f = 100 MHz				
3rd Order Intercept	Output Referred, ±100 mV LO Input		24		dBm
2rd Order Intercept	Output Referred, ±100 mV LO Input		62		dBm
1 dB Compression Point	R_L = 100 Ω, R_{BIAS} = ∞		10		dBm
Noise Figure, SSB	For Optimum Source Impedance		12		dB
POWER SUPPLIES					
Recommended Supply Range	Dual Supply	±4.5		±5.5	V
	Single Supply	9		11	V
Quiescent Current[1]	For Best 3rd Order Intercept Point Performance BIAS Pin Open Circuited		100	125	mA

NOTES

[1]Quiescent current is programmable.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage $\pm V_S$ . . . . . ±5.5 V
Input Voltages
RFHI, RFLO . . . . . ±3 V
LOHI, LOLO . . . . . ±1 V
Internal Power Dissipation[2] . . . . . 1200 mW
Operating Temperature Range
AD831A . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics:
20-Pin PLCC Package: θ_{JA} = 110°C/Watt; θ_{JC} = 20°C/Watt.
Note that the θ_{JA} = 110°C/W value is for the package measured while suspended in still air; mounted on a PC board, the typical value is θ_{JA} = 90°C/W due to the conduction provided by the AD831's package being in contact with the board, which serves as a heat sink.

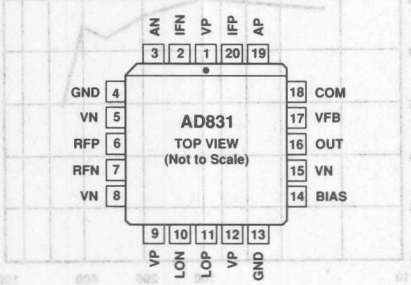
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD831AP	–40°C to +85°C	20-Lead PLCC	P-20A

*For outline information see Package Information section.

PIN CONFIGURATION

20-Lead PLCC



PIN DESCRIPTION

Pin	Mnemonic	Description
1	VP	Positive Supply Input
2	IFN	Mixer Current Output
3	AN	Amplifier Negative Input
4	GND	Ground
5	VN	Negative Supply Input
6	RFP	RF Input
7	RFN	RF Input
8	VN	Negative Supply Input
9	VP	Positive Supply Input
10	LON	Local Oscillator Input
11	LOP	Local Oscillator Input
12	VP	Positive Supply Input
13	GND	Ground
14	BIAS	Bias Input
15	VN	Negative Supply Input
16	OUT	Amplifier Output
17	VFB	Amplifier Feedback Input
18	COM	Amplifier Output Common
19	AP	Amplifier Positive Input
20	IFP	Mixer Current Output

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD831 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD831–Typical Characteristics

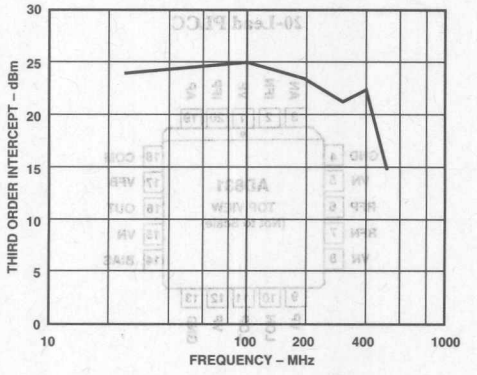


Figure 1. Third-Order Intercept vs. Frequency

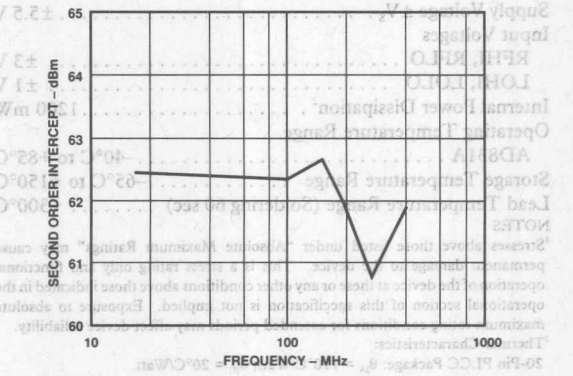


Figure 4. Second-Order Intercept vs. Frequency

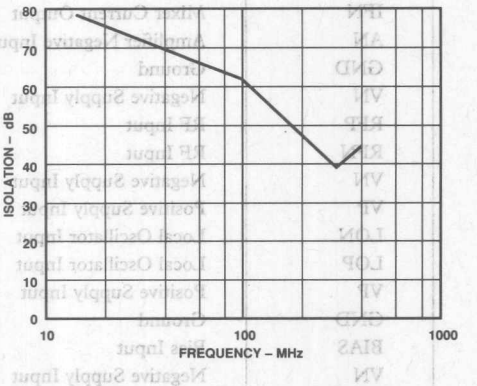


Figure 2. IF-to-RF Isolation vs. Frequency

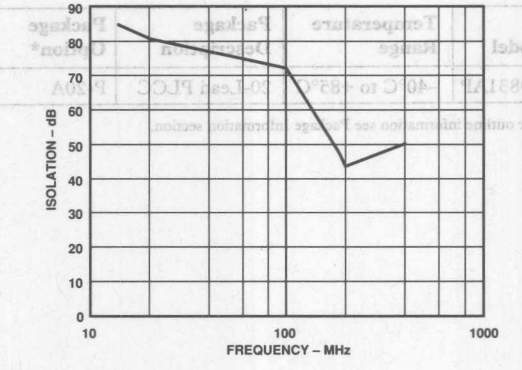


Figure 5. LO-to-RF Isolation vs. Frequency

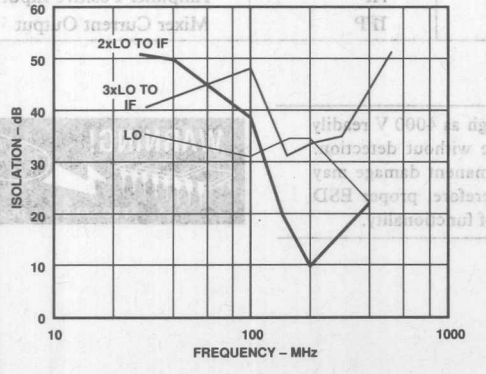


Figure 3. LO-to-IF Isolation vs. Frequency

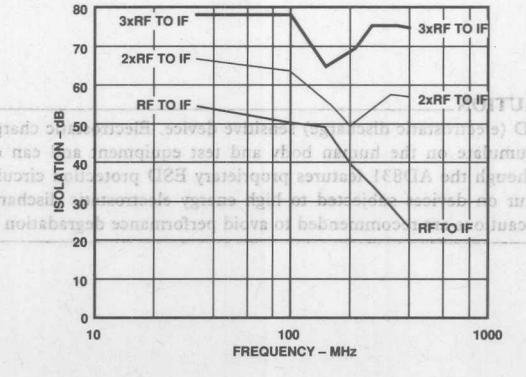


Figure 6. RF-to-IF Isolation vs. Frequency

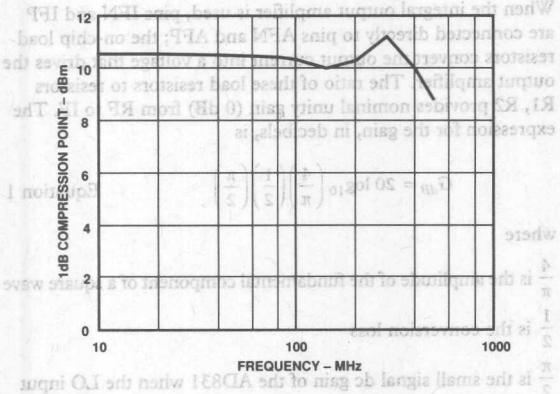


Figure 7. 1 dB Compression Point vs. Frequency, Gain = 1

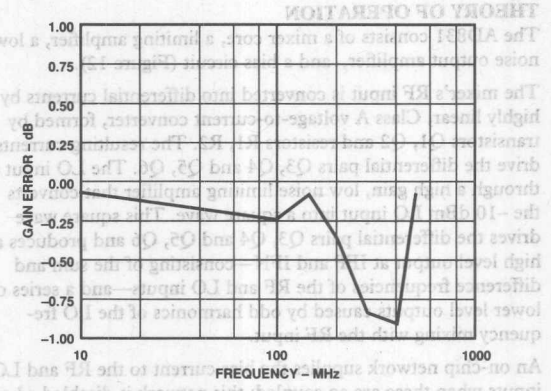


Figure 9. Gain Error vs. Frequency for Figure 7, Gain = 1

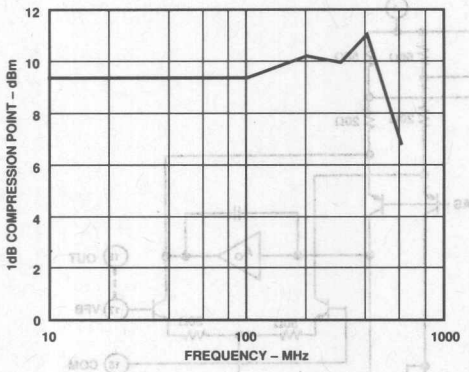


Figure 8. 1 dB Compression Point vs. Frequency, Gain = 2

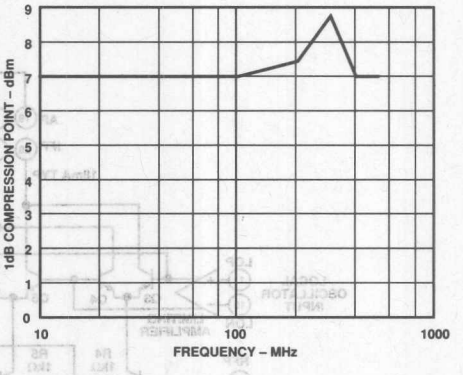


Figure 10. 1 dB Compression Point vs. Frequency, Gain = 4

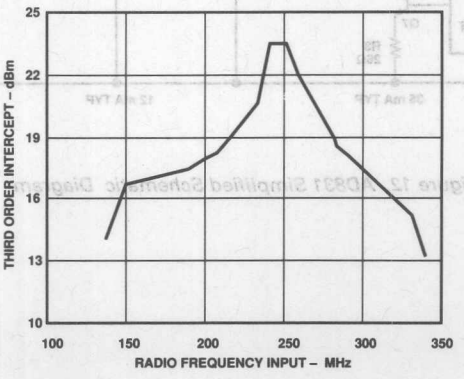


Figure 11. Third-Order Intercept vs. Frequency, LO Held Constant at 241 MHz

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The AD831 consists of a mixer core, a limiting amplifier, a low noise output amplifier, and a bias circuit (Figure 12).

The mixer's RF input is converted into differential currents by a highly linear, Class A voltage-to-current converter, formed by transistors Q1, Q2 and resistors R1, R2. The resulting currents drive the differential pairs Q3, Q4 and Q5, Q6. The LO input is through a high gain, low noise limiting amplifier that converts the –10 dBm LO input into a square wave. This square wave drives the differential pairs Q3, Q4 and Q5, Q6 and produces a high level output at IFP and IFN—consisting of the sum and difference frequencies of the RF and LO inputs—and a series of lower level outputs caused by odd harmonics of the LO frequency mixing with the RF input.

An on-chip network supplies the bias current to the RF and LO inputs when these are ac coupled; this network is disabled when the AD831 is dc coupled.

are connected directly to pins AFN and AFP; the on-chip load resistors convert the output current into a voltage that drives the output amplifier. The ratio of these load resistors to resistors R1, R2 provides nominal unity gain (0 dB) from RF to IF. The expression for the gain, in decibels, is

$$G_{dB} = 20 \log_{10}\left(\frac{4}{\pi}\right)\left(\frac{1}{2}\right)\left(\frac{\pi}{2}\right) \qquad \text{Equation 1}$$

where

$\frac{4}{\pi}$ is the amplitude of the fundamental component of a square wave

$\frac{1}{2}$ is the conversion loss

$\frac{\pi}{2}$ is the small signal dc gain of the AD831 when the LO input is driven fully positive or negative.

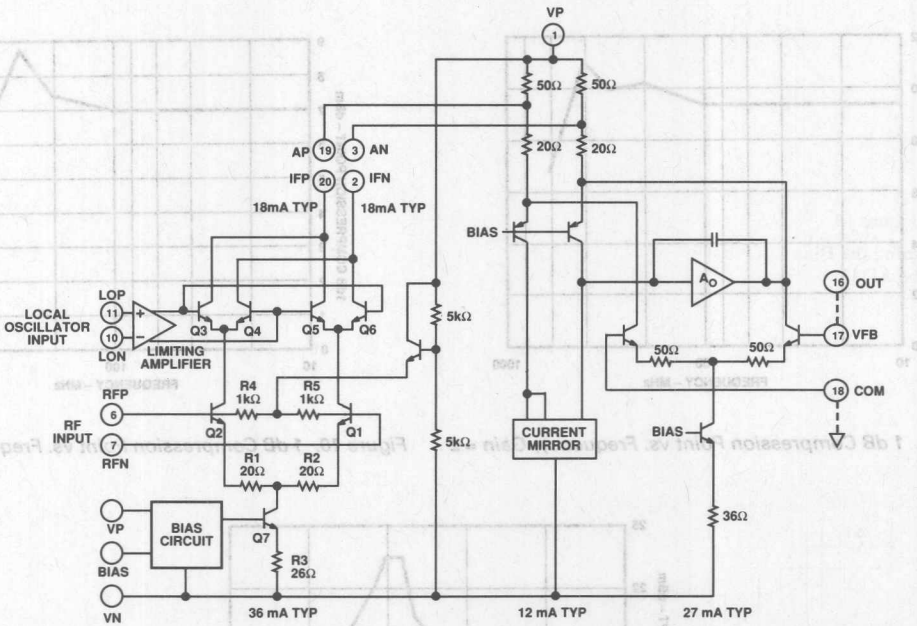


Figure 12. AD831 Simplified Schematic Diagram

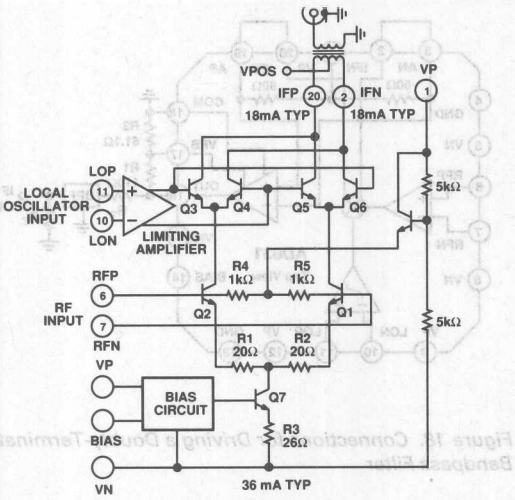


Figure 13. Connections for Transformer Coupling to the IF Output

The mixer has two open-collector outputs (differential currents) at pins IFN and IFP. These currents may be used to provide nominal unity RF-to-IF gain by connecting a center-tapped transformer (1:1 turns ratio) to pins IFN and IFP as shown in Figure 13.

Programming the Bias Current

Because the AD831's RF port is a Class-A circuit, the maximum RF input is proportional to the bias current. This bias current may be reduced by connecting a resistor from the BIAS pin to the positive supply (Figure 14). For normal operation, the BIAS pin is left unconnected. For lowest power consumption, the BIAS pin is connected directly to the positive supply The range of adjustment is 100 mA for normal operation to 45 mA total current at minimum power consumption.

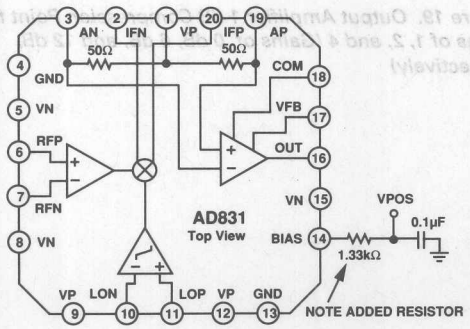


Figure 14. Programming the Quiescent Current

Low-Pass Filtering

A simple low-pass filter may be added between the mixer and the output amplifier by shunting the internal resistive loads (an with external capacitors; these attenuate the sum component in a down-conversion application (Figure 15). The corner frequency of this one-pole low-pass filter ($f = (2\pi RC_F)^{-1}$) should be placed about an octave above the difference frequency IF. Thus, for a 70 MHz IF, a –3 dB frequency of 140 MHz might be chosen, using $C_F = (2 \times \pi \times 14\ \Omega \times 140\ \text{MHz})^{-1} \approx 82\ \text{pF}$, the nearest standard value.

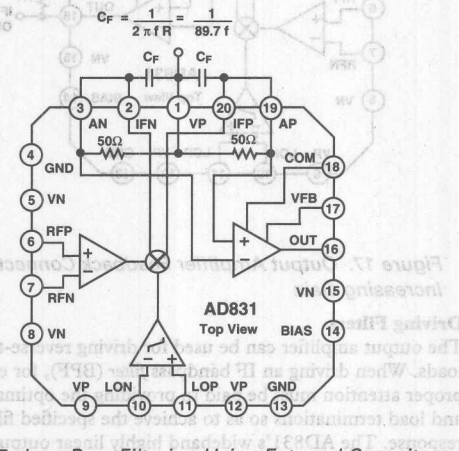


Figure 15. Low-Pass Filtering Using External Capacitors

Using the Output Amplifier

The AD831's output amplifier converts the mixer core's differential current output into a single-ended voltage and provides an output as high as ±1 V peak into a 50 Ω load (+10 dBm). For unity gain operation (Figure 16), the inputs AN and AP connect to the open-collector outputs of the mixer's core and OUT connects to VFB.

For gains other than unity, the amplifier's output at OUT is connected via an attenuator network to VFB; this determines the overall gain. Using resistors R1 and R2 (Figure 17), the gain setting expression is

$$G_{dB} = 20 \log_{10}\left(\frac{R1+R2}{R2}\right) \qquad \text{Equation 2}$$

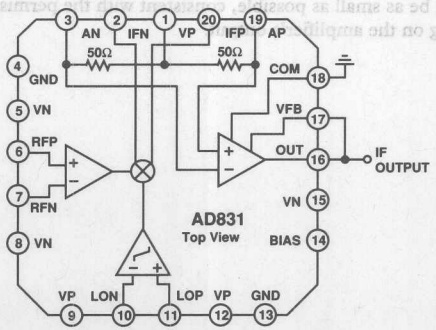


Figure 16. Output Amplifier Connected for Unity Gain Operation

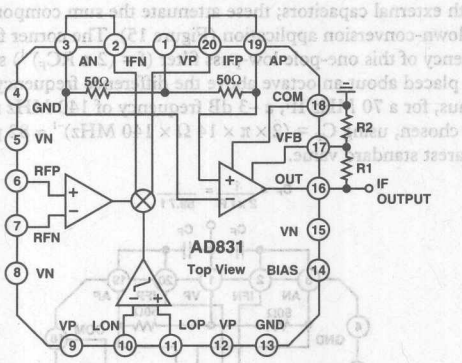


Figure 17. Output Amplifier Feedback Connections for Increasing Gain

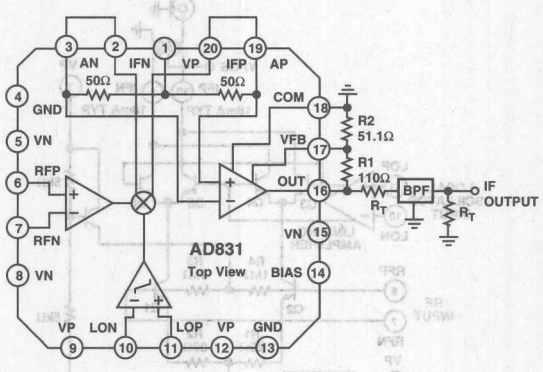


Figure 18. Connections for Driving a Doubly-Terminated Bandpass Filter

Driving Filters

The output amplifier can be used for driving reverse-terminated loads. When driving an IF bandpass *filter* (BPF), for example, proper attention must be paid to providing the optimal source and load terminations so as to achieve the specified filter response. The AD831's wideband highly linear output amplifier affords an opportunity to increase the RF-to-IF gain to compensate for a filter's insertion and termination losses.

Figure 18 indicates how the output amplifier's low impedance (voltage source) output can drive a doubly-terminated bandpass filter. The typical 10 dB of loss (4 dB of insertion loss and 6 dB due to the reverse-termination) be made up by the inclusion of a feedback network that increases the gain of the amplifier by 10 dB (×3.162). When constructing a feedback circuit, the signal path between OUT and VFB should be as short as possible.

Higher gains can be achieved, using different resistor ratios, but with concomitant reduction in the bandwidth of this amplifier (Figure 19). Note also that the Johnson noise of these gain-setting resistors, as well as that of the BPF terminating resistors, is ultimately reflected back to the mixer's input; thus they should be as small as possible, consistent with the permissible loading on the amplifier's output.

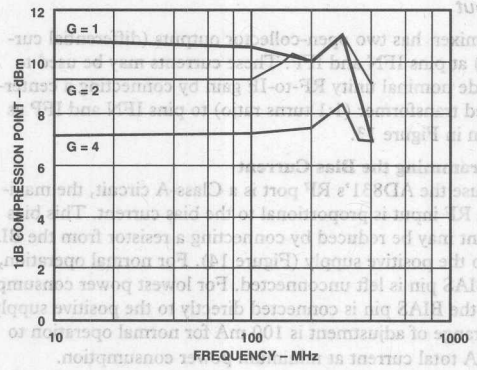


Figure 19. Output Amplifier 1 dB Compression Point for Gains of 1, 2, and 4 (Gains of 0 dB, 6 dB, and 12 dB, respectively)

APPLICATIONS

Careful component selection, circuit layout, power supply decoupling, and shielding are needed to minimize the AD831's susceptibility to interference from radio and TV stations, etc. In bench evaluation, we recommend placing all of the components in a shielded box and using feedthrough decoupling networks for the supply voltage.

Circuit layout and construction are also critical, since stray capacitances and lead inductances can form resonant circuits and are a potential source of circuit peaking, oscillation, or both.

Dual-Supply Operation

Figure 20 shows the connections for dual supply operation. Supplies may be as low as ±4.5 V but should be no higher than ±5.5 V due to power dissipation.

The RF input to the AD831 is shown connected single-ended to pin RFP with 51.1 Ω input termination resistor with an assumed source impedance of 50 Ω. The 82 pF capacitors (C_F) connected from IFN and IFP to VP provide a low-pass filter with a cutoff frequency of approximately 140 MHz in down-conversion applications (see the Theory of Operation section of this data sheet for more details). The LO input is connected single-ended because the limiting amplifier provides a symmetric drive to the mixer. To minimize intermodulation distortion, connect pins OUT and VFB by the shortest possible path. The connections shown are for unity-gain operation.

At LO frequencies less than 100 MHz, the AD831's LO power may be as low as –20 dBm for satisfactory operation. Above 100 MHz, the specified LO power of –10 dBm must be used.

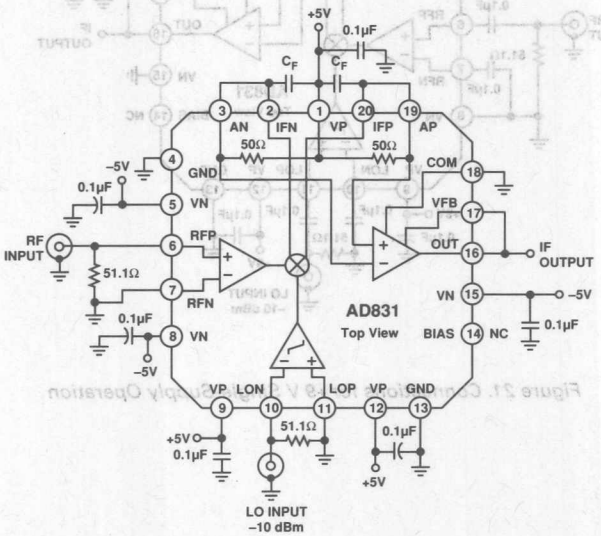


Figure 20. Connections for ±5 V Dual-Supply Operation

Single Supply Operation

Figure 21 is similar to the dual supply circuit in Figure 19. Supplies may be as low as 9 V but should not be higher than 11 V due to power dissipation. As in Figure 19, both the RF and LO ports are driven single-ended and terminated.

In single supply operation, the COM terminal is the "ground" reference for the output amplifier and must be biased to 1/2 the supply voltage, which is done by resistors R1 and R2. The OUT pin must be ac-coupled to the load.

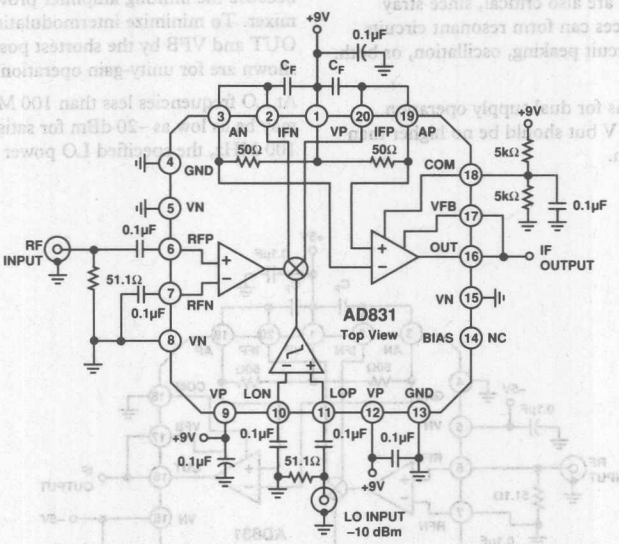


Figure 21. Connections for +9 V Single-Supply Operation

Connections Quadrature Demodulation

Two AD831 mixers may have their RF inputs connected in parallel and have their LO inputs driven in phase quadrature (Figure 22) to provide demodulated in-phase (I) and quadrature (Q) outputs. The mixers' inputs may be connected in parallel and a single termination resistor used if the mixers are located in close proximity on the PC board.

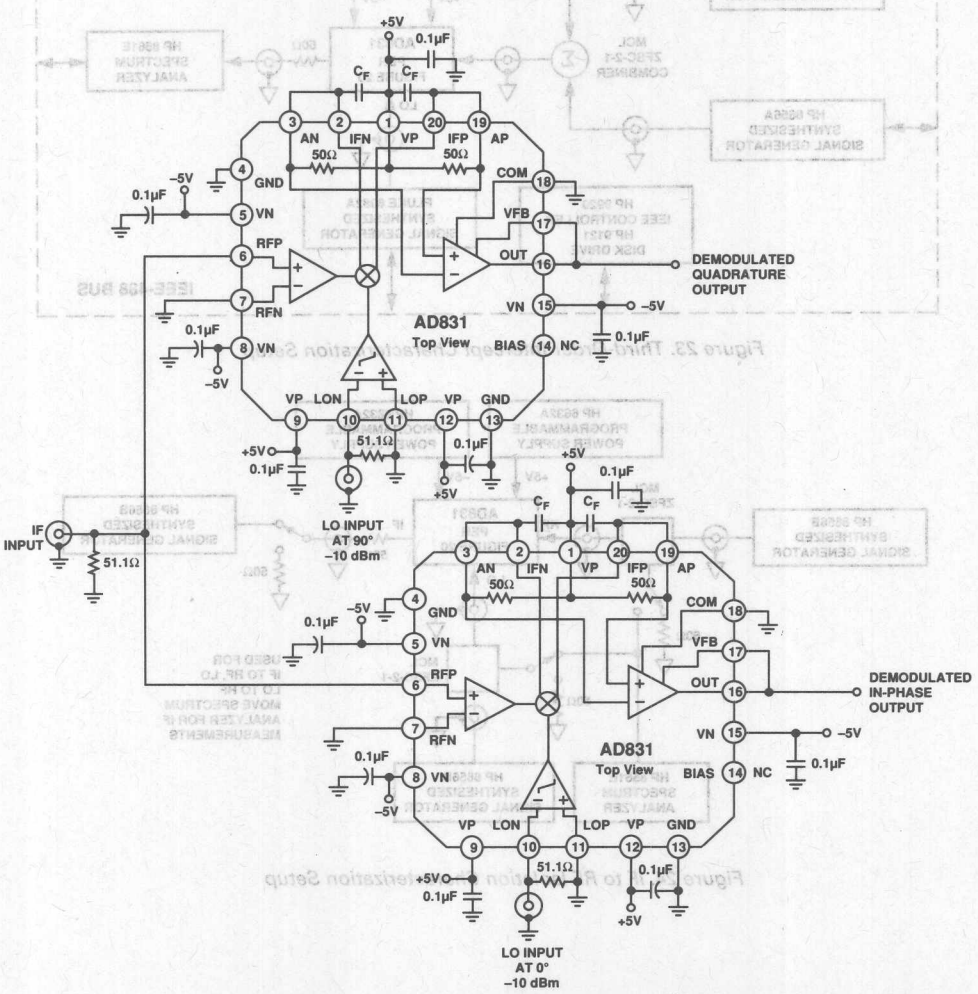


Figure 22. Connections for Quadrature Demodulation

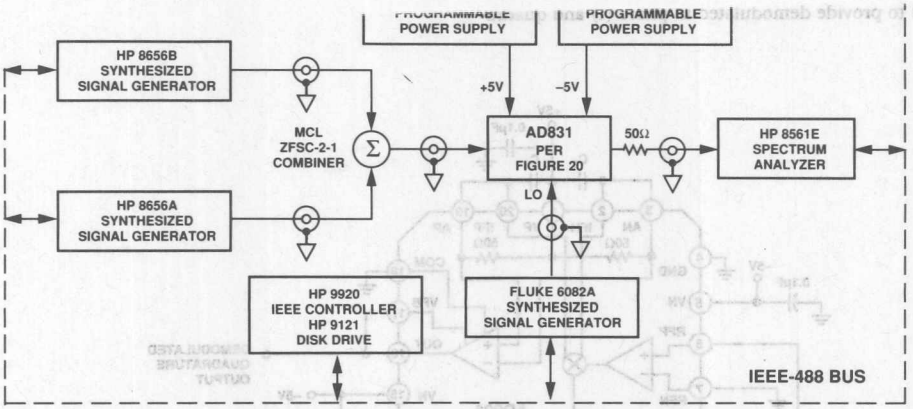


Figure 23. Third-Order Intercept Characterization Setup

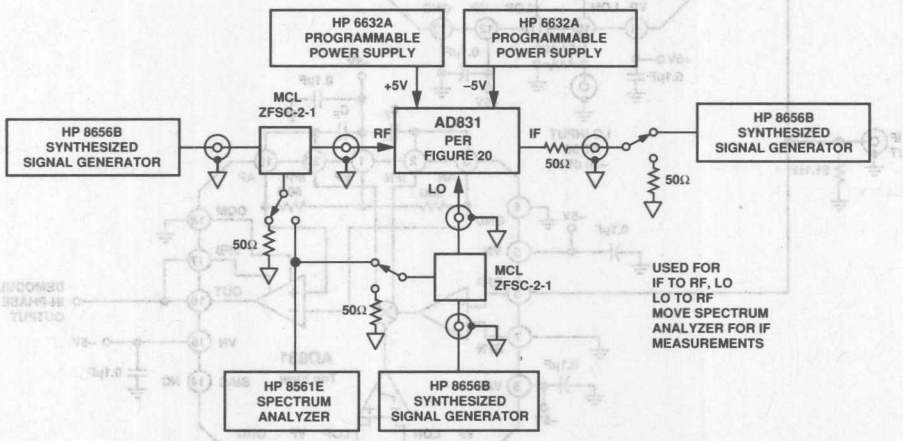


Figure 24. IF to RF Isolation Characterization Setup

ANALOG DEVICES

CMOS DDS Modulator

AD7008

FEATURES
Single +5 V Supply
32-Bit Phase Accumulator
On-Chip COSINE and SINE Look-Up Tables
On-Chip 10-Bit DAC
Frequency, Phase and Amplitude Modulation
Parallel and Serial Loading
Software and Hardware Power Down Options
20 MHz and 50 MHz Speed Grades
44-Pin PLCC

APPLICATIONS
Frequency Synthesizers
Frequency, Phase or Amplitude Modulators
DDS Tuning
Digital Demodulation

GENERAL DESCRIPTION

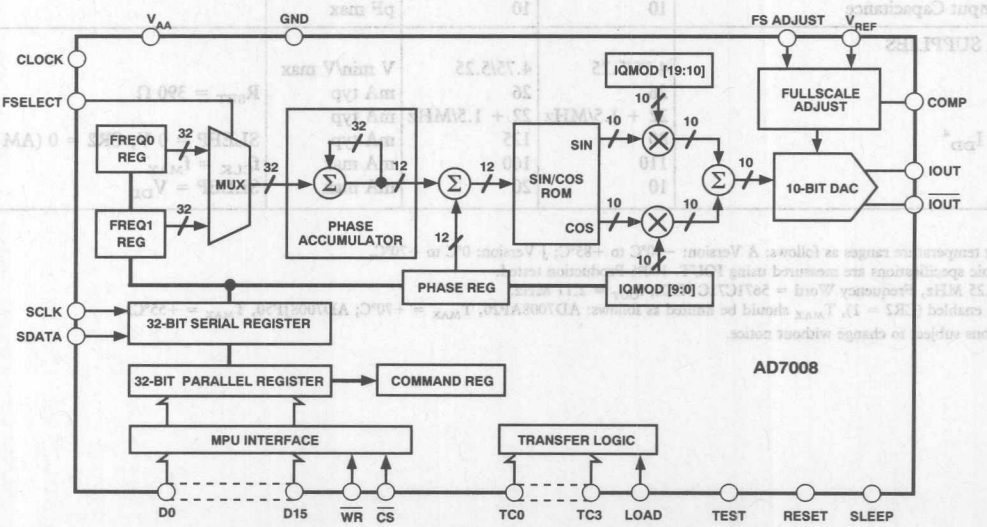
The AD7008 direct digital synthesis chip is a numerically controlled oscillator employing a 32-bit phase accumulator, sine and cosine look-up tables and a 10-bit D/A converter integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation, frequency modulation, and both in-phase and quadrature amplitude modulation suitable for SSB generation.

Clock rates up to 20 MHz and 50 MHz are supported. Frequency accuracy can be controlled to one part in 4 billion. Modulation may be effected by loading registers either through the parallel microprocessor interface or the serial interface. A frequency-select pin permits selection between two frequencies on a per cycle basis.

The serial and parallel interfaces may be operated independently and asynchronously from the DDS clock; the transfer control signals are internally synchronized to prevent metastability problems. The synchronizer can be bypassed to reduce the transfer latency in the event that the microprocessor clock is synchronous with the DDS clock.

A power-down pin allows external control of a power-down mode (also accessible through the microprocessor interface). The AD7008 is available in 44-pin PLCC.

FUNCTIONAL BLOCK DIAGRAM



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AD7008—SPECIFICATIONS[1] (V_{AA} = V_{DD} = +5 V ± 5%; T_A = T_{MIN} to T_{MAX}, R_{SET} = 390 Ω, R_{LOAD} = 51 Ω for IOUT and $\overline{IOUT}$, unless otherwise noted)

Parameter	AD7008AP20	AD7008JP50	Units	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS				
Resolution	10	10	Bits	
No. of Channels	1	1		
Update Rate (f_{MAX})	20	50	Msps max	
IOUT Full Scale	20	20	mA max	
Output Compliance	1	1	Volts max	
DC Accuracy				
Integral Nonlinearity	±1	±1	LSB typ	
Differential Nonlinearity	±1	±1	LSB typ	
DDS SPECIFICATIONS[2]				
Dynamic Specifications				
Signal-to-Noise Ratio	50	50	dB min	f_{CLK} = f_{MAX}, f_{OUT} = 2 MHz
Total Harmonic Distortion	−55	−53	dB min	f_{CLK} = f_{MAX}, f_{OUT} = 2 MHz
Spurious Free Dynamic Range (SFDR)[3]				
Narrow Band (±50 kHz)	−70	−70	dB min	f_{CLK} = 6.25 MHz, f_{OUT} = 2.11 MHz
Wide Band (±2 MHz)	−55	−55	dB min	
Power-Down Option	Yes	Yes		
VOLTAGE REFERENCE				
Internal Reference @ +25°C	1.27	1.27	Volts typ	
T_{MIN} to T_{MAX}	1.2/1.35	1.2/1.35	Volts min/max	
Reference TC	300	300	ppm/°C typ	
LOGIC INPUTS				
V_{INH}, Input High Voltage	V_{DD}–0.9	V_{DD}–0.9	V min	
V_{INL}, Input Low Voltage	0.9	0.9	V max	
I_{INH}, Input Current	10	10	μA max	
C_{IN}, Input Capacitance	10	10	pF max	
POWER SUPPLIES				
V_{DD}	4.75/5.25	4.75/5.25	V min/V max	
I_{AA}	26	26	mA typ	R_{SET} = 390 Ω
I_{DD}	22 + 1.5/MHz	22 + 1.5/MHz	mA typ	
I_{AA} + I_{DD}[4]	80	125	mA typ	SLEEP = 0 V; CR2 = 0 (AM Disabled)
	110	160	mA max	f_{CLK} = f_{MAX}
	10	20	mA max	SLEEP = V_{DD}

NOTES
[1]Operating temperature ranges as follows: A Version: −40°C to +85°C; J Version: 0°C to +70°C.
[2]All dynamic specifications are measured using IOUT. 100% Production tested.
[3]f_{CLK} = 6.25 MHz, Frequency Word = 5671C71C HEX, f_{OUT} = 2.11 MHz.
[4]With AM enabled (CR2 = 1), T_{MAX} should be limited as follows: AD7008AP20, T_{MAX} = +70°C; AD7008JP50, T_{MAX} = +55°C.
Specifications subject to change without notice.

TIMING CHARACTERISTICS ($V_{AA} = V_{DD} +5\ V \pm 5\%$; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	AD7008AP20	AD7008JP50	Units	Test Conditions/Comments
t_1	50	20	ns min	CLOCK Period
t_2	20	8	ns min	CLOCK High Duration
t_3	20	8	ns min	CLOCK Low Duration
t_4	5	5	ns min	CLOCK to Control Setup Time
t_5	3	3	ns min	CLOCK to Control Hold Time
t_6	$4t_1$	$4t_1$	ns min	LOAD Period
t_7	$2t_1$	$2t_1$	ns min	LOAD High Duration
t_8	5	5	ns min	LOAD High to TC0–TC3 Setup Time
t_9	5	5	ns min	LOAD High to TC0–TC3 Hold Time
t_{10}	10	10	ns min	$\overline{WR}$ Rising to $\overline{CS}$ Low Setup Time
t_{11}	10	10	ns min	$\overline{WR}$ Rising to $\overline{CS}$ Low Hold Time
t_{12}	20	20	ns min	Minimum $\overline{WR}$ Low Duration
t_{13}	10	10	ns min	Minimum $\overline{WR}$ High Duration
t_{14}	3	3	ns min	$\overline{WR}$ to D0–D15 Setup Time
t_{15}	3	3	ns min	$\overline{WR}$ to D0–D15 Hold Time
t_{16}	20	20	ns min	SCLK Period
t_{17}	8	8	ns min	SCLK High Duration
t_{18}	8	8	ns min	SCLK Low Duration
t_{19}	10	10	ns min	SCLK Rising to SDATA Setup Time
t_{20}	10	10	ns min	SCLK Rising to SDATA Hold Time

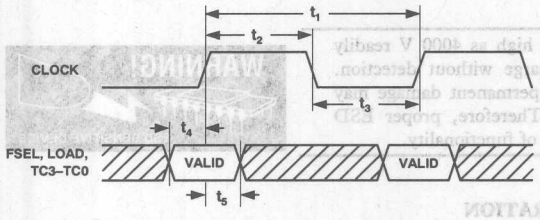


Figure 1. Clock Synchronization Timing

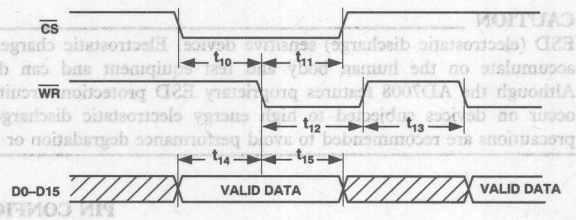


Figure 3. Parallel Port Timing

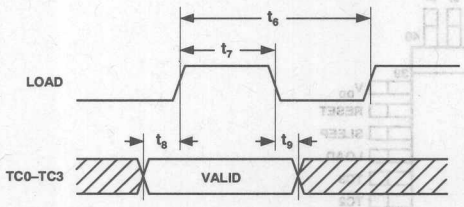


Figure 2. Register Transfer Timing

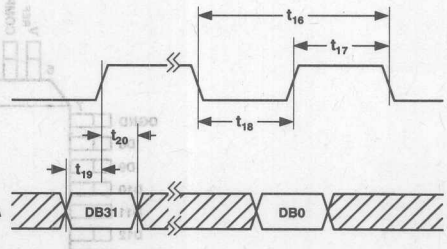


Figure 4. Serial Port Timing

AGND to DGND . . . . . −0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to AGND . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . −40°C to +85°C
Commercial (J Version) . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Junction Temperature . . . . . +115°C
PLCC θ_{JA} Thermal Impedance . . . . . +55°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD7008AP20	−40°C to +85°C	44-Pin PLCC	P-44A
AD7008JP50	0°C to +70°C	44-Pin PLCC	P-44A

*For outline information see Package Information section.

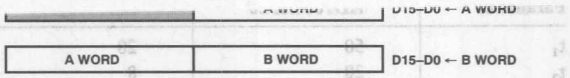


Figure 5. 16-Bit Parallel Port Loading Sequence

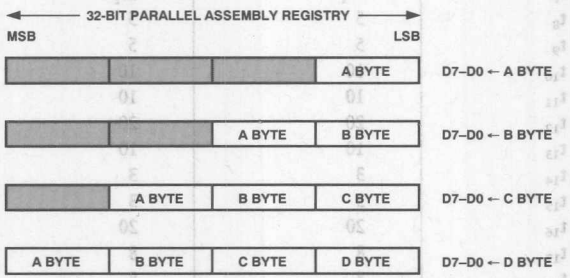
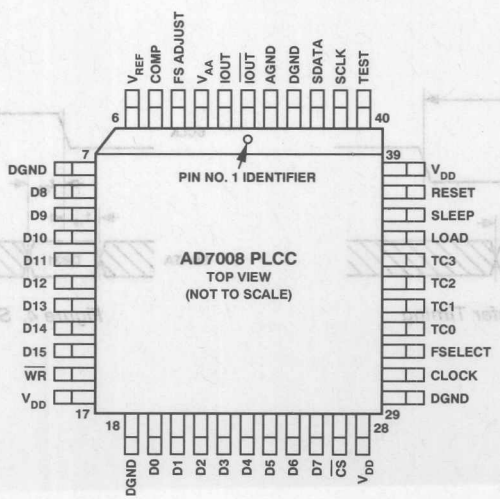


Figure 6. 8-Bit Parallel Port Loading Sequence

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7008 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
PLCC



PIN DESCRIPTION

Mnemonic	Function
POWER SUPPLY	
V_{AA}	Positive power supply for the analog section. A 0.1 μF decoupling capacitor should be connected between V_{AA} and AGND. This is +5 V ± 5 %.
AGND	Analog Ground.
V_{DD}	Positive power supply for the digital section. A 0.1 μF decoupling capacitor should be connected between V_{DD} and DGND. This is +5 V ± 5%. Both V_{AA} and V_{DD} should be externally tied together.
DGND	Digital Ground; both grounds should be externally tied together.
ANALOG SIGNAL AND REFERENCE	
IOUT, $\overline{IOUT}$	Current Output. This is a high impedance current source. A load resistor should be connected between IOUT and AGND. $\overline{IOUT}$ should be either tied directly to AGND or through an external load resistor to AGND.
FS ADJUST	Full-Scale Adjust Control. A resistor (R_{SET}) is connected between this pin and AGND. This determines the magnitude of the full-scale DAC current. The relationship between R_{SET} and the full-scale current is as follows: $$IOUT_{FULL\text{-}SCALE}\ (mA) = 6233 \times V_{REF}\ (V)/R_{SET}\ (\Omega)$$
V_{REF}	Voltage Reference Input. A 0.1 μF decoupling ceramic capacitor should be connected V_{REF} and V_{AA}. There is an internal 1.27 voltage reference which can over driven by an external reference if required.
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 μF decoupling ceramic capacitor should be connected between COMP and V_{AA}.
DIGITAL INTERFACE AND CONTROL	
CLOCK	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of this clock. Hence, the output frequency accuracy and phase noise is determined by this clock.
FSELECT	Frequency Select Input. FSELECT controls which frequency register, FREQ0 or FREQ1, is used in the phase accumulator. Frequency selection can be done on a cycle-per-cycle basis.
LOAD	Register load, active high digital Input. This pin, in conjunction with TC3–TC0, control loading of internal registers from either the parallel or serial assembly registers.
TC3–TC0	Transfer Control address bus, digital inputs. This address determines the source and destination registers that are used during a transfer. The source register can either be the parallel assembly register or the serial assembly register. The destination register can be any of the following: COMMAND REG, FREQ0 REG, FREQ1 REG, PHASE REG or IQMOD REG. TC3-TC0 should be valid prior to LOAD rising and should not change until LOAD falls.
$\overline{CS}$	Chip Select, active low digital input. This input in conjunction with $\overline{WR}$ is used when writing to the parallel assembly register.
$\overline{WR}$	Write, active low digital input. This input in conjunction with $\overline{CS}$ is used when writing to the parallel assembly register.
D7–D0	Data bus, digital inputs. This represent the low byte of the 16-bit data input port used to write to the 32-bit parallel assembly register. The databus can configured for either a 8-bit or 16-bit MPU/DSP ports.
D15–D8	Data Bus, Digital Inputs. This represent the high byte of the 16-bit data input port used to write to the 32-bit parallel assembly register. The databus can configured for either a 8-bit or 16-bit MPU/DSP ports. When the databus is configured for 8-bit operation, D8–D15 should be tied to DGND.
SCLK	Serial Clock, digital input. SCLK is used, in conjunction with SDATA, to clock data into the 32-bit serial assembly register.
SDATA	Serial Data, digital input. Serial data is clocked on the rising edge of SCLK, Most Significant Bit (MSB) first.
SLEEP	Low power sleep control, active high digital input. SLEEP puts the AD7008 into a low power sleep mode. Internal clocks are disable while also turning off the DAC current sources. A SLEEP bit is also provided in the COMMAND REG to put the AD7008 into a low power sleep mode.
RESET	Register Reset, active high digital input. RESET clears the COMMAND REG and all the modulation registers to zero.
TEST	Test Mode. This used for factory test only and should be left as a No Connect.

CIRCUIT DESCRIPTION

In contrast to previous direct digital synthesizer devices, the AD7008 provides an exciting new level of integration for the RF/Communications system designer. The AD7008 combines the numerical controlled oscillator (NCO), SIN/COSINE look-up tables, frequency, phase and IQ modulators, and a digital-to-analog converter on a single integrated circuit.

The internal circuitry of the AD7008 consists of four main sections. These are

Numerical Controlled Oscillator (NCO) + Phase Modulator
SIN and COSINE look up tables
In Phase and Quadrature Modulators
Digital-to-Analog Converter

Numerical Controlled Oscillator + Phase Modulator

This consists of two frequency select registers, a phase accumulator and a phase offset register. The main component of the NCO is a 32-bit phase accumulator which accumulates a phase step on every clock cycle. The value of the phase step determines how many clocks cycles are required for the phase accumulator to count 2π radians (i.e., one cycle of the output frequency). The output frequency, f_{OUT}, is given by:

$$f_{OUT} = \frac{Phase\ Step}{2\pi} f_{CLOCK} = \frac{\Delta\ Phase}{2^{32}} f_{CLOCK}$$

$$0 \le \Delta\ Phase \le 2^{32} - 1$$

The input to the phase accumulator (i.e., the phase step) can be selected either from the FREQ0 Register or FREQ1 Register and this is controlled by the FSELECT pin. This allows binary frequency shift keying to be easily implemented. The two FSK frequencies can be loaded into FREQ0 and FREQ1 and selected using the FSELECT pin. NCOs inherently generate continuous phase signals, thus avoiding any output discontinuity when switching between frequencies. More complex frequency modulation schemes, such as GMSK, can be implemented by updating the contents of these registers.

Following the NCO, a phase offset can be added to perform phase modulation using the 12-bit PHASE Register. The contents of this register are added to the most significant bits of the NCO.

Sin and Cosine Look-Up Tables (LUT)

The output of the phase accumulator is converted to an amplitude signal by means of an Sine/Cosine ROM LUT. Although the NCO contains a 32-bit phase accumulator, the output of the NCO is truncated to 12-bits. Using the full resolution of the phase accumulator is both impractical and unnecessary as this would require a look-up table of 2^{32} entries.

It is necessary only to have sufficient phase resolution in the LUTs such that the dc error of the output waveform is dominated by the quantization error in the DAC. This requires the look-up tables to have two more bits of phase resolution than the 10-bit DAC.

In Phase and Quadrature Modulators

Two 10-bit amplitude multipliers are provided allowing the easy implementation of either Quadrature Amplitude Modulation (QAM) or Amplitude Modulation (AM). The 20-bit IQMOD Register is used to control the amplitude of the I (cosine) and Q (sine) signals. IQMOD[9–0] controls the I amplitude and IQMOD[19–10] controls the Q amplitude.

The user should ensure that when summing the I and Q signals the result should not exceed 10-bits, as there is no internal clipping logic to prevent overflow.

When amplitude modulation is not required, the IQ multipliers can be bypassed (CR2 = 0). The sine output is directly sent to the 10-bit DAC.

Digital-to-Analog Converter

The AD7008 include a high impedance current source 10-bit DAC, capable of driving wide range of loads at different speeds. Full-scale output current can be adjusted, for optimum power and external load requirements, through the use of a single external resistor (R_{SET}).

The DAC can be configured for single or differential ended operation. $\overline{I_{OUT}}$ can be either tied directly to AGND for single ended operation or through external load resistor.

MPU Interface

The chip contains two 32-bit assembly registers, one for parallel bus data, and one for serial input data. Each of the modulation registers can be loaded from either assembly register under control of the LOAD pin and the Transfer-Control (TC) pins (See Table I). The Command register can only be loaded from the parallel assembly register.

Table I. Source and Destination Registers

TC3	TC2	TC1	TC0	LOAD	Source Register	Destination Register
X	X	X	X	0	N/A	N/A
0	0	X	X	1	Parallel	COMMAND
1	0	0	0	1	Parallel	FREQ0
1	0	0	1	1	Parallel	FREQ1
1	0	1	0	1	Parallel	PHASE
1	0	1	1	1	Parallel	IQMOD
1	1	0	0	1	Serial	FREQ0
1	1	0	1	1	Serial	FREQ1
1	1	1	0	1	Serial	PHASE
1	1	1	1	1	Serial	IQMOD

Table II. AD7008 Control Registers

Register	Size	Reset State	Description
COMMAND REG	4 Bits CR3–CR0	All Zeros	Command Register. This is written to using the parallel assembly register.
FREQ0 REG	32 Bits DB31–DB0	All Zeros	Frequency Select Register 0. This defines the output frequency, when FSELECT = 0, as a fraction of the CLOCK frequency.
FREQ1 REG	32 Bits DB31–DB0	All Zeros	Frequency Select Register 1. This defines the output frequency, when FSELECT = 1, as a fraction of the CLOCK frequency.
PHASE REG	12 Bits DB11–DB0	All Zeros	Phase Offset Register. The contents of this register is added to the output of the phase accumulator.
IQMOD REG	20 Bits DB19–DB0	All Zeros	I and Q Amplitude Modulation Register. This defines the amplitude of the I and Q signals as 10-bit two complement binary fractions. DB[19:10] is multiplied by the Quadrature (sine component and DB[9:0] is multiplied by the In-Phase (cosine) component.

Table III. Command Register Bits

CR0	= 0	Eight-Bit Databus. Pins D15–D8 are ignored and the parallel assembly register shifts eight places left on each write. Hence four successive writes are required to load the 32-bit parallel assembly register, Figure 6.
	= 1	Sixteen-Bit Databus. The parallel assembly register shifts 16 places left on each write. Hence two successive writes are required to load the 32-bit parallel assembly register, Figure 5.
CR1	= 0	Normal Operation.
	= 1	Low Power Sleep Mode. Internal Clocks and the DAC current sources are turn off.
CR2	= 0	Amplitude Modulation Bypass. The output of the sine LUT is directly sent to the DAC.
	= 1	Amplitude Modulation Enable. IQ modulation is enabled allowing AM or QAM to be performed.
CR3	= 0	Synchronizer Logic Enabled. The FSELECT, LOAD and TC3–TC0 signals are passed through a 4-stage pipeline to synchronize them with the CLOCK frequency, avoiding metastability problems.
	= 1	Synchronizer Logic Disabled. The FSELECT, LOAD and TC3–TC0 signals bypass the synchronization logic. This allows for faster response to the control signals.

TC3–TC0 should be set up and stable before LOAD rises, and should not change until after LOAD falls.

The microprocessor asserts both $\overline{WR}$ and $\overline{CS}$ to load the parallel assembly register. At the end of each write, the parallel assembly register is shifted left by 8 or 16 bits (depending on CR0), and the new data is loaded into the low bits. Hence, two 16-bit writes or four 8-bit writes are used to load the parallel assembly register. When loading parallel data destined for the phase or IQ registers, it is only necessary to write as much data as will be used by that register. For instance, the Command Register requires only one write to the parallel assembly register.

Serial data is input to the chip on the rising edge of SCLK, most significant bit first. The data in the assembly registers can be transferred to the modulation registers by means of the transfer control pins.

APPLICATIONS

The AD7008 can be used in a wide range of communication applications ranging from digital mobile radio, to frequency agile Wireless Local Area Networks (WANs), to SSB telephony.

For digital mobile radio applications the chip provides direct synthesis and phase modulation capabilities to 20 MHz in a single low power, low cost part.

For WANs a wide range of modulation capabilities allow a system developer to optimize modulation bandwidth and noise immunity.

In the area of SSB telephony (military, commercial and amateur), the chip provides the first single chip implementation of a phasing type SSB generator. Combined with a single chip DSP (ADSP-2101) implementing the speech input and Hilbert transform, the AD7008 forms a two-chip direct SSB generation capability to over 20 MHz.

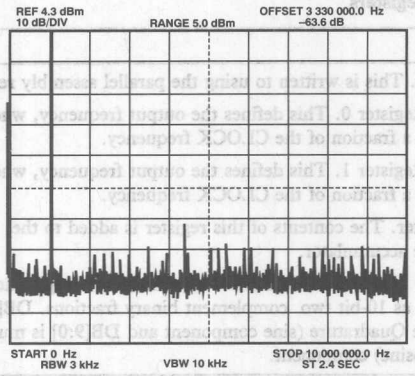


Figure 7. f_{CLK} = 20 MHz, f_{OUT} = 1.1 MHz

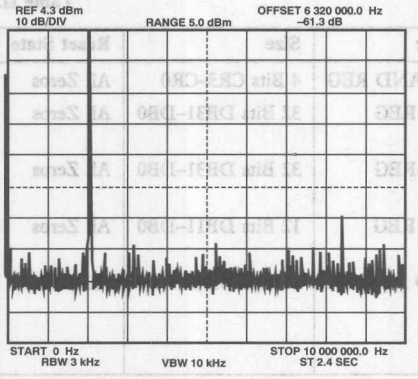


Figure 10. f_{CLK} = 20 MHz, f_{OUT} = 2.1 MHz

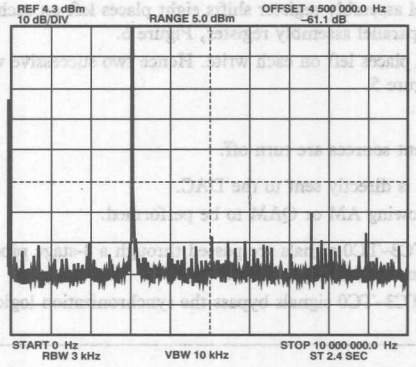


Figure 8. f_{CLK} = 20 MHz, f_{OUT} = 3.1 MHz

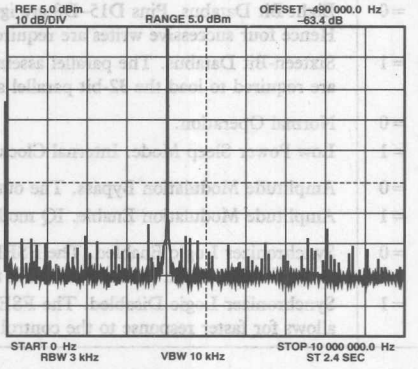


Figure 11. f_{CLK} = 20 MHz, f_{OUT} = 4.1 MHz

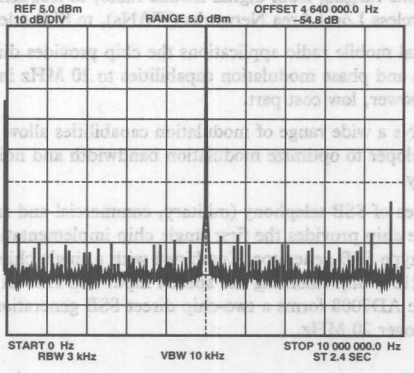


Figure 9. f_{CLK} = 20 MHz, f_{OUT} = 5.1 MHz

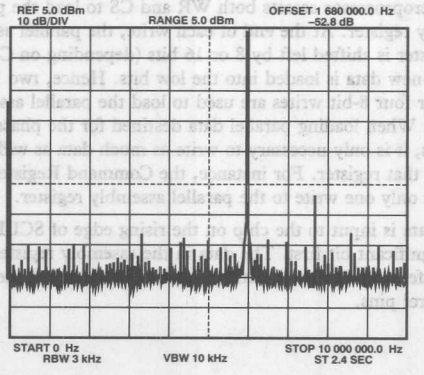


Figure 12. f_{CLK} = 20 MHz, f_{OUT} = 6.1 MHz

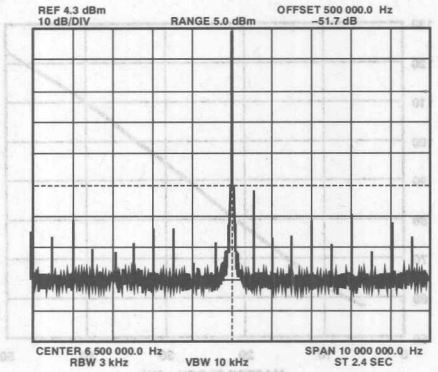


Figure 13. f_{CLK} = 20 MHz, f_{OUT} = 6.5 MHz

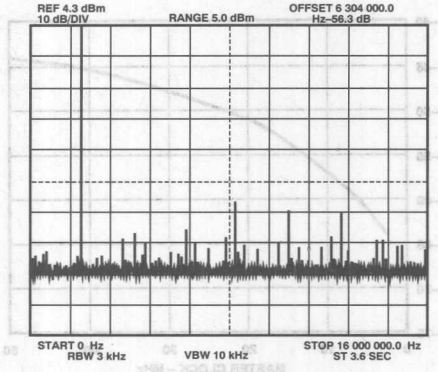


Figure 14. f_{CLK} = 50 MHz, f_{OUT} = 2.1 MHz

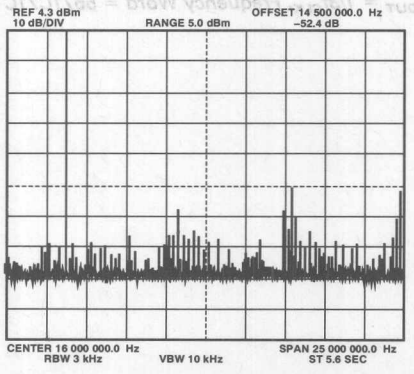


Figure 15. f_{CLK} = 50 MHz, f_{OUT} = 7.1 MHz

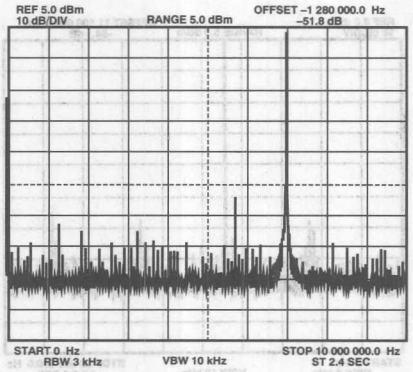


Figure 16. f_{CLK} = 20 MHz, f_{OUT} = 7.1 MHz

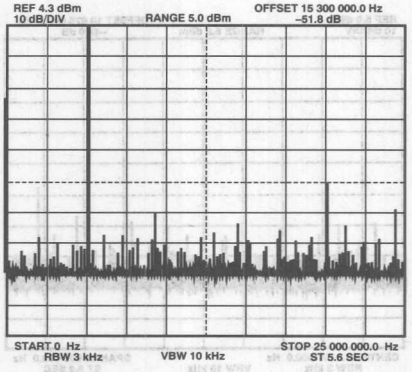


Figure 17. f_{CLK} = 50 MHz, f_{OUT} = 5.1 MHz

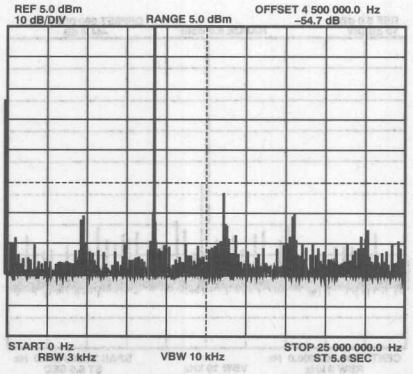


Figure 18. f_{CLK} = 50 MHz, f_{OUT} = 9.1 MHz

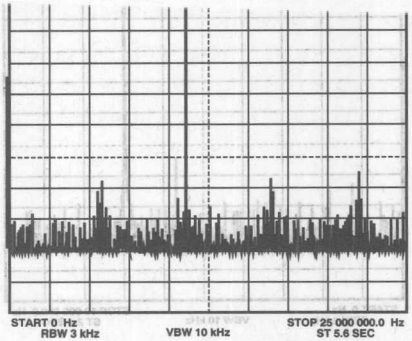


Figure 19. f_{CLK} = 50 MHz, f_{OUT} = 11.1 MHz

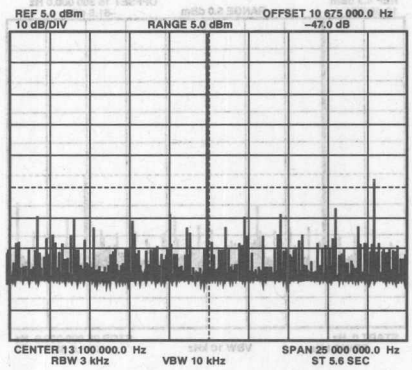


Figure 20. f_{CLK} = 50 MHz, f_{OUT} = 13.1 MHz

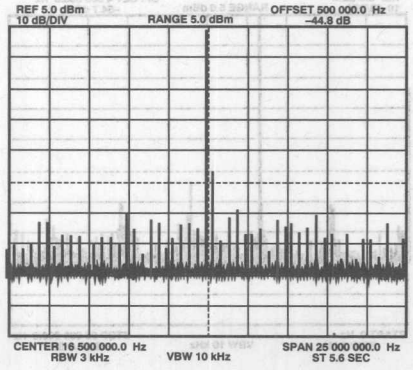


Figure 21. f_{CLK} = 50 MHz, f_{OUT} = 16.5 MHz

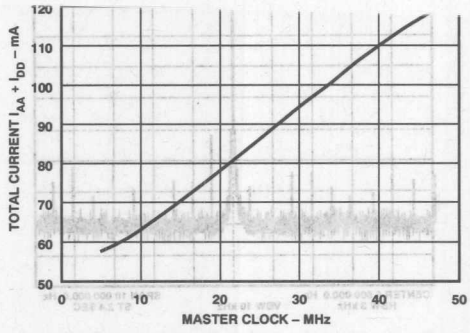


Figure 22. Typical Current Consumption vs. Frequency

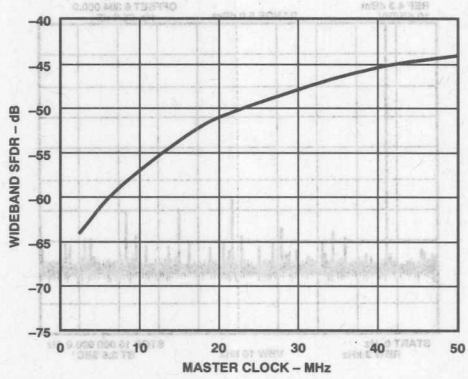


Figure 23. Typical Plot of SFDR vs. Master Clock Frequency When f_{OUT} = 1/3f_{CLK}, Frequency Word = 5671C71C HEX

Digitally Programmable Delay Generator

AD9500

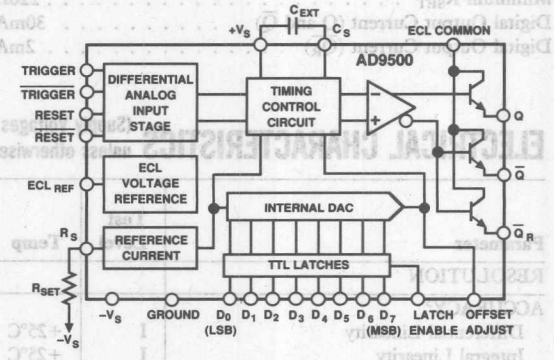
FEATURES

- 10ps Delay Resolution
- 2.5ns to 10μs Full-Scale Range
- Fully Differential Inputs
- Separate Trigger and Reset Inputs
- Low Power Dissipation – 310mW
- MIL-STD-883 Compliant Versions Available

APPLICATIONS

- ATE
- Pulse Deskewing
- Arbitrary Waveform Generators
- High-Stability Timing Source
- Multiple Phase Clock Generators

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

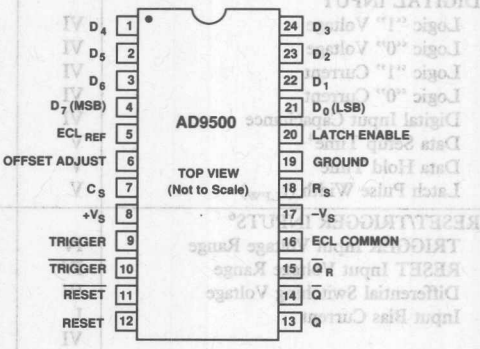
The AD9500 is a digitally programmable delay generator, which provides programmed delays, selected through an 8-bit digital code, in resolutions as small as 10ps. The AD9500 is constructed in a high-performance bipolar process, designed to provide high-speed operation for both digital and analog circuits.

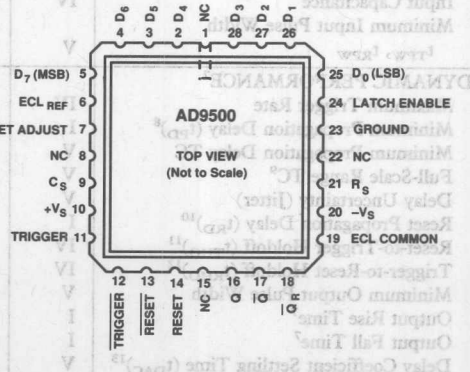
The AD9500 employs differential TRIGGER and RESET inputs which are designed primarily for ECL signal levels but function with analog and TTL input levels. An on-board ECL reference midpoint allows both of the inputs to be driven by either single ended or differential ECL circuits. The AD9500 output is a complementary ECL stage, which also provides a parallel $\overline{Q_R}$ output circuit to facilitate reset timing implementations.

The digital control data is passed to the AD9500 through a transparent latch controlled by the LATCH ENABLE signal. In the transparent mode, the internal DAC of the AD9500 will attempt to follow changes at the inputs. The LATCH ENABLE is otherwise used to strobe the digital data into the AD9500 latches.

The AD9500 is available as an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both grades are packaged in a 24-pin ceramic "Skinny" DIP (0.3" package width), as well as 28-pin surface mount packages. The AD9500 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD9500/883B data sheet for detailed specifications.

PIN CONFIGURATIONS





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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9500—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +7V
Negative Supply Voltage ($-V_S$) . . . . . −7V
ECL COMMON to Ground Differential . . −2.0V to +5.0V
Digital Input Voltage Range . . . . . −3.5V to +5.0V
Trigger/Reset Input Voltage Range . . . . . ±5.0V
Trigger/Reset Differential Voltage 5.0V
Minimum R_{SET} 220Ω
Digital Output Current (Q and $\overline{Q}$) 30mA
Digital Output Current ($\overline{Q_R}$) 2mA
Offset Adjust Current (Sinking) 4mA
Operating Temperature Range
AD9500BP/BQ . . . . . −25°C to +85°C
AD9500TE/TQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages $+V_S = +5.0V$, $-V_S = -5.2V$; $C_{EXT} = 0pF$; $R_{SET} = 500\Omega$, unless otherwise noted)

Parameter	Test Level	Temp	−25°C to +85°C AD9500BP/BQ Min	Typ	Max	−55°C to +125°C AD9500TE/TQ Min	Typ	Max	Units
RESOLUTION			8			8			Bits
ACCURACY[3]									
Differential Linearity	I	+25°C			0.5			0.5	LSB
Integral Linearity	I	+25°C			1.0			1.0	LSB
Monotonicity	I	+25°C		Guaranteed			Guaranteed		
DIGITAL INPUT									
Logic "1" Voltage	VI	Full	2.0			2.0			V
Logic "0" Voltage	VI	Full			0.8			0.8	V
Logic "1" Current	VI	Full			5			5	µA
Logic "0" Current	VI	Full			5			5	µA
Digital Input Capacitance	VI	+25°C			5.5			5.5	pF
Data Setup Time[4]	V	+25°C		0.4	0.75		0.4	0.75	ns
Data Hold Time[5]	V	+25°C		0.4	0.75		0.4	0.75	ns
Latch Pulse Width (t_{LPW})	V	+25°C	3.0			3.0			ns
RESET/TRIGGER INPUTS[6]									
TRIGGER Input Voltage Range	IV	Full		−2.5; 4.5			−2.5; 4.5		V
RESET Input Voltage Range	IV	Full		−2.5; 2.0			−2.5; 2.0		V
Differential Switching Voltage	IV	Full		40	300		40	300	mV
Input Bias Current	I	+25°C		40	50		40	50	µA
	VI	Full			75			75	µA
Input Resistance	IV	+25°C		4			4		kΩ
Input Capacitance	IV	+25°C		6.5	7.25		6.5	7.25	pF
Minimum Input Pulse Width t_{TPW}, t_{RPW}	V	+25°C		2.0			2.0		ns
DYNAMIC PERFORMANCE[7]									
Maximum Trigger Rate	IV	+25°C		60			60		MHz
Minimum Propagation Delay (t_{PD})[8]	I	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Minimum Propagation Delay TC	V	Full		7.5			7.5		ps/°C
Full-Scale Range TC[9]	V	Full		0.5			0.5		ps/°C
Delay Uncertainty (Jitter)	V	+25°C		10			10		ps
Reset Propagation Delay (t_{RD})[10]	I	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Reset-to-Trigger Holdoff (t_{THO})[11]	IV	+25°C	0.2	0		0.2	0		ns
Trigger-to-Reset Holdoff (t_{RHO})[12]	IV	+25°C	2.0	1.5		2.0	1.5		ns
Minimum Output Pulse Width	V	+25°C		3.3			3.3		ns
Output Rise Time[7]	I	+25°C			2.0			2.0	ns
Output Fall Time[7]	I	+25°C			2.0			2.0	ns
Delay Coefficient Settling Time (t_{DAC})[13]	V	+25°C		29			29		ns
Linear Ramp Settling Time (t_{LRS})	V	+25°C		22			22		ns

Parameter	Test Level	Temp	−25°C to +85°C AD9500BP/BQ Min	Typ	Max	−55°C to +125°C AD9500TE/TQ Min	Typ	Max	Units
SUPPORT FUNCTIONS									
ECL_{REF}	IV	+25°C	−1.4	−1.3	−1.2	−1.4	−1.3	−1.2	V
ECL_{REF} Voltage Drift[14]	V	Full		1.1			1.1		mV/°C
Offset Adjust Range	V	Full		−2			−2		mA
DIGITAL OUTPUTS[7]									
Logic "1" Voltage	VI	Full	−1.1			−1.1			V
Logic "0" Voltage	VI	Full			−1.5			−1.5	V
POWER SUPPLY[15]									
Positive Supply Current (+5.0V)	I	+25°C		24	28		24	28	mA
	VI	Full			30			30	mA
Negative Supply Current (−5.2V)	I	+25°C		37	42		37	42	mA
	VI	Full			44			44	mA
Nominal Power Dissipation	V	+25°C		312			312		mW
Power Supply Rejection Ratio[16]									
Full-Scale Range Sensitivity	I	+25°C		70	300		70	300	ps/V
Minimum Propagation Delay Sensitivity	I	+25°C		150	500		150	500	ps/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Typical thermal impedance

24-Pin Ceramic $\theta_{JA} = 56°C/W; \theta_{JC} = 16°C/W$

28-Pin PLCC (Plastic) $\theta_{JA} = 60°C/W; \theta_{JC} = 22°C/W$

28-Pin Ceramic LCC $\theta_{JA} = 69°C/W; \theta_{JC} = 25°C/W$

[3]$R_{SET} = 10k\Omega$ (Full-scale delay = 100ns).

[4]The digital data inputs must remain stable for the specified time prior to the LATCH ENABLE signal.

[5]The digital data inputs must remain stable for the specified time after the LATCH ENABLE signal.

[6]The TRIGGER and RESET inputs are differential and must be driven relative to one another. Both of these inputs are ECL compatible, but can also be used with TTL logic families in a limited fashion.

[7]Outputs terminated through 50Ω resistors to −2.0V.

[8]Program Delay = 0.0ps (Digital Data = 00_H). In Operation, any programmed delays are in addition to the Minimum Propagation Delay.

[9]Change in total delay through AD9500, exclusive of changes in minimum-propagation delay t_{PD}.

[10]Measured from the 50% transition point of the reset signal input, to the 50% transition point of the resetting output.

[11]Minimum time from falling edge of RESET to triggering input, to insure a valid output event.

[12]Minimum time from triggering event to rising edge of RESET, to insure a valid output event.

[13]Measured from the LATCH ENABLE input to the point when the AD9500 becomes 8-bit accurate again, after a full-scale change in the programmed delay.

[14]Standard 10K and 10KH ECL families operate with a 1.1mV/°C drift by design.

[15]Supply voltages should remain stable within ±5% for normal operation.

[16]Measured at ±5% of $-V_S$ and $+V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Periodically sample tested.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

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Model	Temperature Range	Description	Options*
AD9500BP	−25°C to +85°C	28-Pin PLCC (Plastic), Industrial Temperature	P-28A
AD9500BQ	−25°C to +85°C	24-Pin "Skinny" DIP, Industrial Temperature	Q-24
AD9500TE	−55°C to +125°C	28-Pin LCC, Extended Temperature	E-28A
AD9500TQ	−55°C to +125°C	24-Pin "Skinny" DIP, Extended Temperature	Q-24

*E = Leadless Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
D_4–D_6	– One of eight digital inputs used to set the programmed delay.
D_7 (MSB)	– One of eight digital inputs used to set the programmed delay. D_7 (MSB) is the most significant bit of the digital input word.
ECL_{REF}	– ECL midpoint reference, nominally −1.3V. Use of the ECL_{REF}, allows either of the TRIGGER or the RESET inputs to be configured for single-ended ECL inputs.
OFFSET ADJUST	– The OFFSET ADJUST is used to adjust the minimum propagation delay (t_{PD}), by pulling or pushing a small current out of or into the pin.
C_S	– C_S allows the full-scale range to be extended by using an external timing capacitor. The value of C_{EXT}, connected between C_S and $+V_S$, may range from no external capacitance to 0.1μF+. See R_S ($C_{INTERNAL}$ = 10pF).
$+V_S$	– Positive supply terminal, nominally +5.0V.
TRIGGER	– Noninverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The TRIGGER input must be driven in conjunction with the $\overline{\text{TRIGGER}}$ input.
$\overline{\text{TRIGGER}}$	– Inverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The $\overline{\text{TRIGGER}}$ input must be driven in conjunction with the TRIGGER input.
$\overline{\text{RESET}}$	– Inverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The RESET input must be driven in conjunction with the $\overline{\text{RESET}}$ input.
RESET	– Noninverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The $\overline{\text{RESET}}$ input must be driven in conjunction with the RESET input.
Q	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic HIGH on the Q output. A "resetting" event at the inputs will produce a logic LOW on the Q output
$\overline{Q}$	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q}$ output.
$\overline{Q_R}$	– $\overline{Q_R}$ output is parallel to the $\overline{Q}$ output. The $\overline{Q_R}$ output is typically used to drive delaying circuits for extending output pulse widths. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q_R}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q_R}$ output.
ECL COMMON	– The collector common for the ECL output stage. The collector common may be tied to +5.0V, but normally it is tied to the circuit ground for standard ECL outputs.
$-V_S$	– Negative supply terminal, nominally −5.2V.
R_S	– R_S is the reference current setting terminal. An external setting resistor, R_{SET}, connected between R_S and $-V_S$ determines the internal reference current. See C_S ($250\Omega \le R_{SET} \le 50k\Omega$).
GROUND	– The ground return for the TTL and analog inputs.
LATCH ENABLE	– Transparent TTL latch control line. A logic HIGH on the LATCH ENABLE freezes the digital code at the logic inputs. A logic LOW on the LATCH ENABLE allows the internal current levels to be continuously updated through the logic inputs D_0 thru D_7.
D_0 (LSB)	– One of eight digital inputs used to set the programmed delay. D_0 (LSB) is the least significant bit of the digital input word.
D_3–D_1	– One of eight digital inputs used to set the programmed delay.

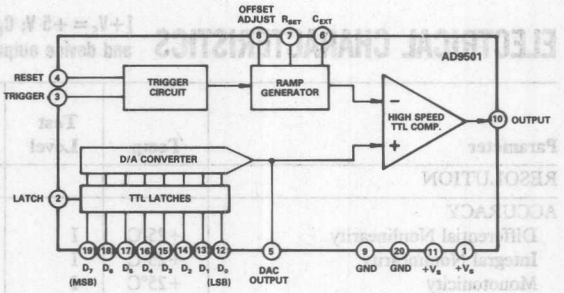
Digitally Programmable Delay Generator

AD9501

FEATURES
Single +5 V Supply
TTL and CMOS Compatible
10 ps Delay Resolution
2.5 ns to 10 μs Full-Scale Range
Maximum Trigger Rate 50 MHz
MIL-STD-883-Compliant Versions Available

APPLICATIONS
Disk Drive Deskewing
Data Communications
Test Equipment
Radar I & Q Matching

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9501 is a digitally programmable delay generator which provides programmed time delays of an input pulse. Operating from a single +5 V supply, the AD9501 is TTL- or CMOS-compatible, and is capable of providing accurate timing adjustments with resolutions as low as 10 ps. Its accuracy and programmability make it ideal for use in data deskewing and pulse delay applications, as well as clock timing adjustments.

Full-scale delay range is set by the combination of an external resistor and capacitor, and can range from 2.5 ns to 10 μs for a single AD9501. An eight-bit digital word selects a time delay within the full-scale range. When triggered by the rising edge of an input pulse, the output of the AD9501 will be delayed by an amount equal to the selected time delay (t_D) plus an inherent propagation delay (t_{PD}).

The AD9501 is available for a commercial temperature range of 0°C to +70°C in a 20-pin plastic DIP, 20-pin ceramic DIP, and a 20-lead plastic leaded chip carrier (PLCC). Devices fully compliant to MIL-STD-883 are available in ceramic DIPs. Refer to the *Analog Devices Military Products Databook* or current AD9501/883B data sheet for detailed specifications.

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This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9501—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage	+7 V
Digital Input Voltage Range	−0.5 V to $+V_S$
Trigger/Reset Input Volt. Range	−0.5 V to $+V_S$
Minimum R_{SET}	30 Ω
Digital Output Current (Sourcing)	10 mA
Digital Output Current (Sinking)	50 mA
Operating Temperature Range	
AD9501JN/JP/JQ	0°C to +70°C
AD9501SQ	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature[2]	+175°C
Lead Soldering Temperature (10 sec)	+300°C

ELECTRICAL CHARACTERISTICS

[$+V_S = +5$ V; C_{EXT} = Open; $R_{SET} = 3090$ Ω (Full-scale range = 100 ns); Pin 8 grounded; and device output connected to Pin 4 RESET input unless otherwise noted]

Parameter	Temp	Test Level	0°C to +70°C AD9501JN/JP/JQ Min	Typ	Max	−55°C to +125°C AD9501SQ Min	Typ	Max	Units
RESOLUTION			8			8			Bits
ACCURACY									
Differential Nonlinearity	+25°C	I			0.5			0.5	LSB
Integral Nonlinearity	+25°C	I			1			1	LSB
Monotonicity	+25°C	I		Guaranteed			Guaranteed		
DIGITAL INPUTS									
Latch Input "1" Voltage	Full	VI	2.0			2.3			V
Latch Input "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Voltage	Full	VI	2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			60			60	μA
Logic "0" Current	Full	VI			3			3	μA
Digital Input Capacitance	+25°C	IV			5.5			5.5	pF
Data Setup Time (t_S)[3]	+25°C	V		2.5			2.5		ns
Data Hold Time (t_H)[4]	+25°C	V		2.5			2.5		ns
Latch Pulse Width (t_L)	+25°C	V		3.5			3.5		ns
Reset/Trigger Pulse Width (t_R, t_T)	+25°C	V		2			2		ns
DYNAMIC PERFORMANCE									
Maximum Trigger Rate[5]	+25°C	IV	18	22		18	22		MHz
Minimum Propagation Delay (t_{PD})[6]	+25°C	I		25	30		25	30	ns
Propagation Delay Tempco[7]	Full	V		25			25		ps/°C
Full-Scale Range Tempco	Full	V		36			36		ps/°C
Delay Uncertainty	+25°C	V		53			53		ps
Reset Propagation Delay (t_{RD})[8]	+25°C	I		14.5	17.5		14.5	17.5	ns
Reset-to-Trigger Holdoff (t_{THO})[9]	+25°C	V		4.5			4.5		ns
Trigger-to-Reset Holdoff (t_{RHO})[10]	+25°C	V		19			19		ns
Minimum Output Pulse Width[11]	+25°C	V		7.5			7.5		ns
Output Rise Time[12]	+25°C	I		2.3	3.5		2.3	3.5	ns
Output Fall Time[12]	+25°C	I		1.0	2.0		1.0	2.0	ns
DAC Settling Time (t_{LD})[13]	+25°C	V		30			30		ns
Linear Ramp Settling Time (t_{LRS})[14]	+25°C	V		20			20		ns
DIGITAL OUTPUT									
Logic "1" Voltage (Source 1 mA)	Full	VI	2.4			2.4			V
Logic "0" Voltage (Sink 4 mA)	Full	VI		0.24	0.4		0.24	0.5	V
POWER SUPPLY[15]									
Positive Supply Current (+5.0 V)	Full	VI		69.5	83		69.5	83	mA
Power Dissipation	Full	VI			415			415	mW
Power Supply Rejection Ratio[16]									
Full-Scale Range Sensitivity	+25°C	I		0.7	2.0		0.7	2.0	ns/V
Minimum Prop Delay Sensitivity	+25°C	I		0.45	1.7		0.45	1.7	ns/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances: 20-lead plastic leaded chip carrier θ_{JA}=73°C/W; θ_{JC}=29°C/W. 20-pin ceramic DIP θ_{JA}=65°C/W; θ_{JC}=20°C/W. 20-pin plastic DIP θ_{JA}=65°C/W; θ_{JC}=26°C/W.

[3]Digital data inputs must remain stable for the specified time prior to the positive transition of the LATCH signal.

[4]Digital data inputs must remain stable for the specified time after the positive transition of the LATCH signal.

[5]Programmed delay (t_D)=0 ns. Maximum self-resetting trigger rate is limited to 6.9 MHz with 100 ns programmed delay. If t_D=0 ns and external RESET signal is used, maximum trigger rate is 23 MHz.

[6]Programmed delay (t_D)=0 ns. In operation, any programmed delays are in addition to the minimum propagation delay (t_{PD}).

[7]Programmed delay (t_D)=0 ns. [Minimum propagation delay (t_{PD})]

[8]Measured from 50% transition point of the RESET signal input to the 50% transition point of the falling edge of the output.

[9]Minimum time from the falling edge of RESET to the triggering input to insure valid output pulse, using external RESET pulse.

[10]Minimum time from triggering event to rising edge of RESET to insure valid output event, using external RESET pulse. Extends to 125 ns when programmed delay is 100 ns.

[11]When self-resetting with a full-scale programmed delay.

[12]Measured from +0.4 V to +2.4 V; source = 1 mA; sink = 4 mA.

[13]Measured from the data input to the time when the AD9501 becomes 8-bit accurate, after a full-scale change in the program delay data word.

[14]Measured from the RESET input to the time when the AD9501 becomes 8-bit accurate, after a full-scale programmed delay.

[15]Supply voltage should remain stable within ±5% for normal operation.

[16]Measured at $+V_S$ = +5.0 V ±5%; specification shown is for worst case.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

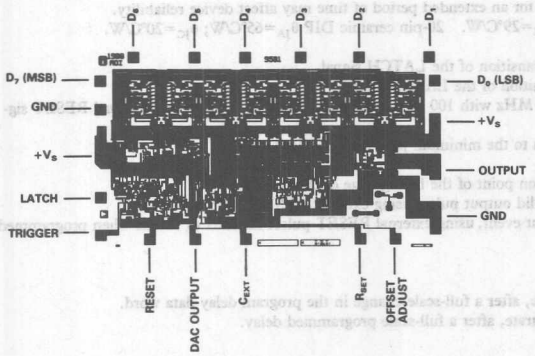
V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Device	Temperature	Description	Package Option*
AD9501JN	0°C to +70°C	20-Pin Plastic DIP	N-20
AD9501JP	0°C to +70°C	20-Lead PLCC	P-20A
AD9501JQ	0°C to +70°C	20-Pin Ceramic DIP	Q-20
AD9501SQ	−55°C to +125°C	20-Pin Ceramic DIP	Q-20

*N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

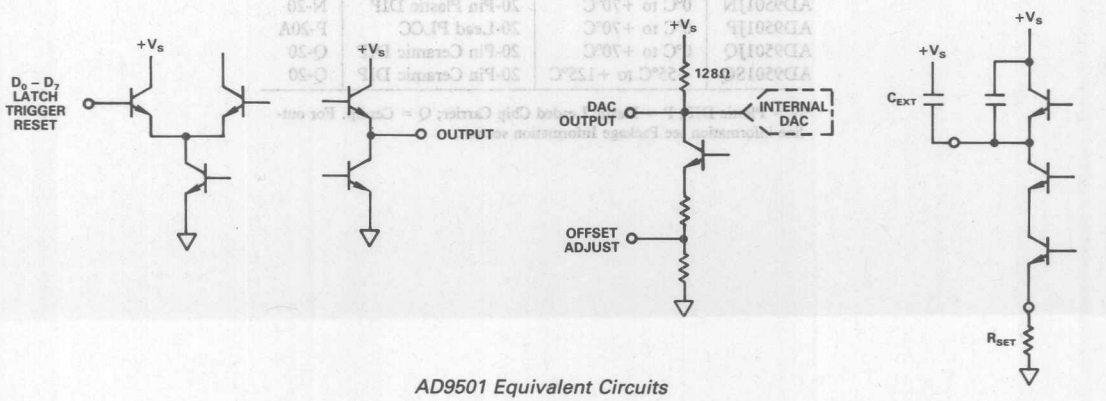


MECHANICAL INFORMATION

Die Dimensions	.89 × 153 × 15 (±2) mils
Pad Dimensions	.4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	Ground
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1 mil, Gold; Gold Ball Bonding

AD9501 PIN DESCRIPTIONS

Pin No.	Name	Function
1	$+V_S$	Positive voltage supply; nominally +5 V.
2	LATCH	TTL/CMOS register control line. Logic HIGH latches input data D_0–D_7. Register is transparent for logic LOW.
3	TRIGGER	TTL/CMOS-compatible input. Rising edge triggers the internal ramp generator, and begins the delay cycle.
4	RESET	TTL/CMOS-compatible input. Logic HIGH resets the ramp voltage and OUTPUT.
5	DAC OUTPUT	Output voltage of the internal digital-to-analog converter.
6	C_{EXT}	Optional external capacitor connected to $+V_S$; used with R_{SET} and 8.5 pF internal capacitor to determine full-scale delay range (t_{DFS}).
7	R_{SET}	External resistor to ground, used to determine full-scale delay range (t_{DFS}).
8	OFFSET ADJUST	Normally connected to GROUND. Can be used to adjust minimum propagation delay (t_{PD}); see Theory of Operation text.
9	GROUND	Circuit ground return.
10	OUTPUT	TTL-compatible delayed output pulse.
11	$+V_S$	Positive voltage supply; nominally +5 V.
12–19	D_0–D_7	TTL/CMOS-compatible inputs, used to set the programmed delay of the AD9501 delayed output. D_0 is LSB and D_7 is MSB.
20	GROUND	Circuit ground return.



AD9501 Equivalent Circuits

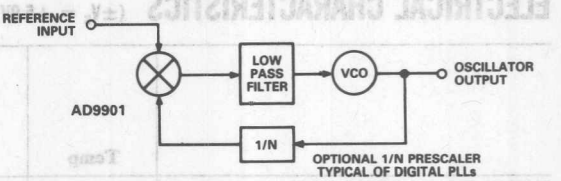
Ultrahigh Speed Phase/Frequency Discriminator

AD9901

FEATURES
Phase and Frequency Detection
ECL/TTL/CMOS Compatible
Linear Transfer Function
No "Dead Zone"
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Low Phase Noise Reference Loops
Fast-Tuning "Agile" IF Loops
Secure "Hopping" Communications
Coherent Radar Transmitter/Receiver Chains

PHASE-LOCKED LOOP



GENERAL DESCRIPTION

The AD9901 is a digital phase/frequency discriminator capable of directly comparing phase/frequency inputs up to 200MHz. Processing in a high speed trench-oxide isolated process, combined with an innovative design, gives the AD9901 a linear detection range, free of indeterminate phase detection zones common to other digital designs.

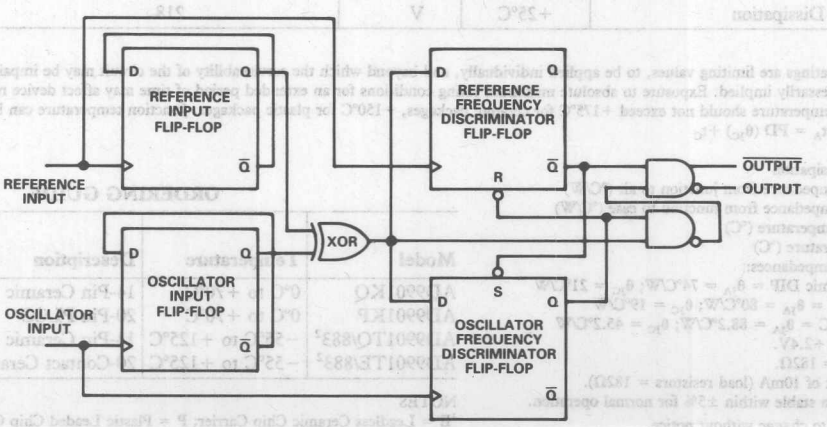
With a single +5V supply, the AD9901 can be configured to operate with TTL or CMOS logic levels; it can also operate with ECL inputs when operated with a −5.2V supply. The open-collector outputs allow the output swing to be matched to post-filtering input requirements. A simple current setting resistor controls the output stage current range, permitting a reduction in power when operated at lower frequencies.

A major feature of the AD9901 is its ability to compare phase-/frequency inputs at standard IF frequencies without prescalers. Excessive phase uncertainty which is common with standard PLL configurations is also eliminated. The AD9901 provides the locking speed of traditional phase/frequency discriminators, with the phase stability of analog mixers.

The AD9901 is available as a commercial temperature range device, 0°C to +70°C, and as a military temperature device, −55°C to +125°C. The commercial versions are packaged in a 14-pin ceramic DIP and a 20-pin PLCC.

The AD9901 Phase/Frequency Discriminator is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9901/883B data sheet for specifications.

FUNCTIONAL BLOCK DIAGRAM



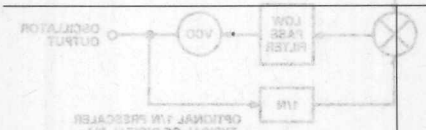
This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9901—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$ for TTL Operation)	+7V
Negative Supply Voltage ($-V_S$ for ECL Operation)	−7V
Input Voltage Range (TTL Operation)	0V to +5.5V
Differential Input Voltage (ECL Operation)	4.0V
I_{SET} Current	12mA
Output Current	30mA
Operating Temperature Range	
AD9901KQ/KP	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature[2]	
Plastic	+150°C
Ceramic	+175°C
Lead Soldering Temperature (10sec)	+300°C

ELECTRICAL CHARACTERISTICS ($\pm V_S$ = +5.0V [for TTL] or −5.2V [for ECL], unless otherwise noted)



	Temp	Test Level	Commercial Temperature 0°C to +70°C AD9901KQ/KP Min	Typ	Max	Units
INPUT CHARACTERISTICS						
TTL Input Logic "1" Voltage	Full	VI	2.0			V
TTL Input Logic "0" Voltage	Full	VI			0.8	V
TTL Input Logic "1" Current[3]	Full	VI			0.6	mA
TTL Input Logic "0" Current[3]	Full	VI			1.6	mA
ECL Differential Switching Volt.	Full	VI	300			mV
ECL Input Current	Full	VI			20	μA
OUTPUT CHARACTERISTICS						
Peak-to-Peak Output Voltage Swing[4]	Full	VI	1.6	1.8	2.0	V
TTL Output Compliance Range	Full	V		3–7		V
ECL Output Compliance Range	Full	V		±2		V
I_{OUT} Range	Full	V		0.9–11		mA
Internal Reference Voltage	Full	VI	0.42	0.47	0.52	V
AC CHARACTERISTICS						
Linear Phase Detection Range[4]						
40kHz	+25°C	V		360		Degrees
30MHz	+25°C	V		320		Degrees
70MHz	+25°C	V		270		Degrees
Functionality @ 70MHz	+25°C	I		Pass/Fail		
POWER SUPPLY CHARACTERISTICS						
TTL Supply Current (+5.0V)[5, 6]	+25°C	I		43.5	54.0	mA
	Full	I		43.5	54.0	mA
ECL Supply Current (−5.2V)[5, 6]	+25°C	I		42.5	52.5	mA
	Full	I		42.5	52.5	mA
Nominal Power Dissipation	+25°C	V		218		mW

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Maximum junction temperature should not exceed +175°C for ceramic packages, +150°C for plastic packages. Junction temperature can be calculated by:

$t_J = PD\ (\theta_{JA}) + t_A = PD\ (\theta_{JC}) + t_C$

where:

PD = power dissipation

θ_{JA} = thermal impedance from junction to air (°C/W)

θ_{JC} = thermal impedance from junction to case (°C/W)

t_A = ambient temperature (°C)

t_C = case temperature (°C)

typical thermal impedances:

AD9901 Ceramic DIP = θ_{JA} = 74°C/W; θ_{JC} = 21°C/W

AD9901 LCC = θ_{JA} = 80°C/W; θ_{JC} = 19°C/W

AD9901 PLCC = θ_{JA} = 88.2°C/W; θ_{JC} = 45.2°C/W

[3]V_L = +0.4V; V_H = +2.4V.

[4]R_{SET} = 47.5Ω; R_L = 182Ω.

[5]Includes load current of 10mA (load resistors = 182Ω).

[6]Supply should remain stable within ±5% for normal operation.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature	Description	Package Option[1]
AD9901KQ	0°C to +70°C	14-Pin Ceramic DIP	Q-14
AD9901KP	0°C to +70°C	20-Pin PLCC	P-20A
AD9901TQ/883[2]	−55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD9901TE/883[2]	−55°C to +125°C	20-Contact Ceramic LCC	E-20A

NOTES

[1]E = Leadless Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

[2]For specifications, refer to Analog Devices *Military Products Databook*.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

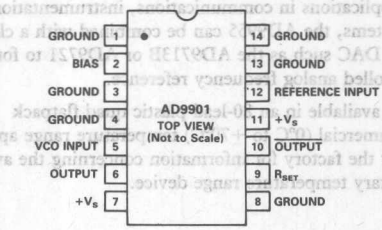
IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

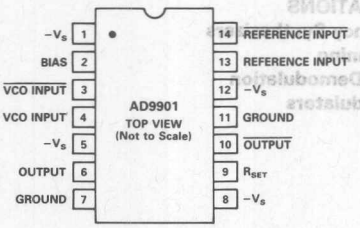
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

PIN CONFIGURATIONS

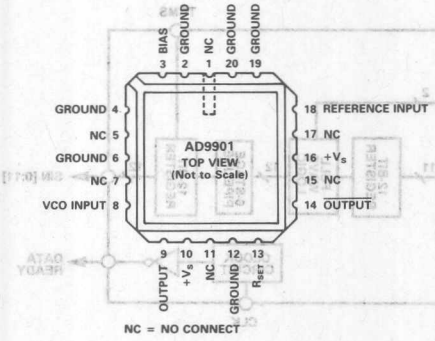
TTL DIP Pinouts



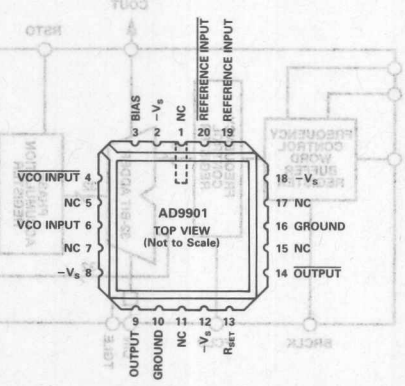
ECL DIP Pinouts



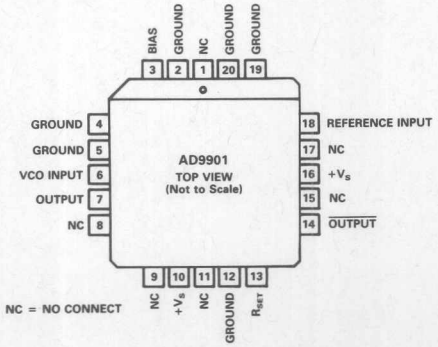
TTL LCC Pinouts



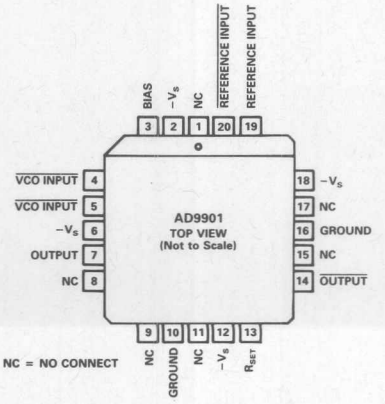
ECL LCC Pinouts



TTL PLCC Pinouts



ECL PLCC Pinouts



21

FEATURES
85 MHz Minimum Clock Rate
32-Bit Phase Accumulator
12-Bit Sine Output
>90 dB Spurious Free Dynamic Range
Continuous Frequency Update
On-Board Data Ready Signal

APPLICATIONS
Frequency Synthesizers
DDS Tuning
Digital Demodulation
FM Modulators

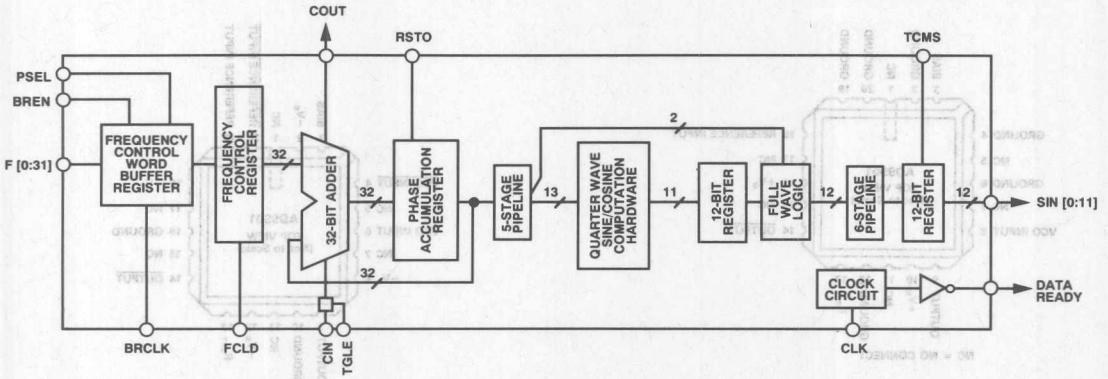
GENERAL DESCRIPTION

The AD9955 is a 85 MHz direct digital synthesizer for frequency synthesis applications. It comprises a 32-bit phase accumulator and a 15-bit phase-to-12-bit sine amplitude converter. The control logic is CMOS compatible, and the clock input is TTL. CMOS outputs are latched on board, and a data ready signal is provided.

Designed for applications in communications, instrumentation, and military systems, the AD9955 can be combined with a clock reference and a DAC such as the AD9713B or AD9721 to form a digitally-controlled analog frequency reference.

The AD9955 is available in an 80-lead plastic quad flatpack (PQFP) for commercial (0°C to +70°C) temperature range applications. Contact the factory for information concerning the availability of a military temperature range device.

FUNCTIONAL BLOCK DIAGRAM



SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; f_{CLK} = 40 MHz; C_L = 20 pF, unless otherwise noted)

Parameter (Conditions)	Temperature	Test Level	AD9955 Min	AD9955 Typ	AD9955 Max	Units
CMOS INPUTS[1]						
Logic "1" Voltage	Full	II	3.5			V
Logic "0" Voltage	Full	II			1.5	V
Logic "1" Current	Full	II			1.0	μA
Logic "0" Current	Full	II			−1.0	μA
Input Capacitance	+25°C	V		10		pF
CMOS OUTPUTS						
Logic "1" Voltage (V_{IH})	Full	II	4.5			V
Logic "0" Voltage (V_{IL})	Full	II			0.4	V
Logic "1" Current	Full	II			12	mA
Logic "0" Current	Full	II			12	mA
Output Capacitance	+25°C	V		3		pF
TTL INPUTS[2]						
Logic "1" Voltage	Full	IV	2.0			V
Logic "0" Voltage	Full	II			0.8	V
Logic "1" Current	Full	II			1.0	μA
Logic "0" Current	Full	II			−1.0	μA
Input Capacitance	+25°C	V		4		pF
POWER SUPPLIES						
$+V_S$ Current[3]						
CLK = 50 MHz	Full	IV		120	160	mA
CLK = 100 MHz	+25°C	V		240		mA
Nominal Power Dissipation						
CLK = 50 MHz	+25°C	V		600		mW
CLK = 100 MHz	+25°C	V		1.2		W
Relative to Frequency	+25°C	V		11.5		mW/MHz
AC SPECIFICATIONS[4]						
Clock Update Rate (CLK)[5]	Full	IV	85	100		MHz
Frequency Update Rate (BRCLK)[6]	Full	II	40			MHz
Clock Pulse Width						
CLK Digital "1"	Full	IV	7.9	5.7		ns
CLK Digital "0"	Full	IV	3.8	2.2		ns
Frequency Update Pulse Width						
BRCLK Digital "1"	Full	II	10			ns
BRCLK Digital "0"	Full	II	10			ns
Input Rise/Fall Times						
CLK Rise Time	Full	IV			2	ns
CLK Fall Time	Full	IV			2	ns
BRCLK Rise Time	Full	IV			5	ns
BRCLK Fall Time	Full	IV			5	ns
BRCLK Input Timing						
Setup Time (t_{CS}, t_{ES})[7]	Full	II	5	2		ns
Hold Time (t_{CH}, t_{EH})[7]	Full	IV	5	1.8		ns
CLK Input Timing						
Setup Time (t_{LS})[8]	Full	IV	2.0	0.7		ns
Hold Time (t_{LH})[8]	Full	IV	2.0	0.7		ns
RESET 0 Timing						
Setup Time (t_{RS})[9]	Full	IV	6			ns
Hold Time (t_{RH})[9]	Full	IV	6			ns
Output Timing Characteristics						
Data Output Delay (t_{OD})[10]	Full	IV	3.4	6.1	8.7	ns
DRDY Output Delay (t_{DR})[10]	Full	IV	4.7	7.5	10	ns
Output Data Setup Time (t_{OS})[11]	Full	IV	0.8	1.9		ns
Carry Output Delay[12]	+25°C	V		7.7		ns
Spurious-Free Dynamic Range (SFDR)						
Worst Case Spur[13]	+25°C	V		>90		dBc
Latency of Initial Data[14]	+25°C	V		14		Clock Cycles

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NOTES
[1]Includes F[0:31], PSEL, BREN, FCLD, CIN, TGLE, BRCLK, TCMS, and RST0.
[2]Only the clock (CLK) is TTL compatible.
[3]f_{OUT} = 1/2 f_{CLK}. See performance curves.
[4]Nominal conditions (V_{IH} = 3.4 V; V_{IL} = 0.4 V).
[5]Based on minimum clock pulse width duty cycle (68% HIGH @ 85 MHz).
[6]This specification defines the maximum rate at which the output frequency tuning word (F[0:31]) can be updated.
[7]Referenced to 2.5 V point of rising edge of BRCLK, specified for F[0:31], BREN.
[8]Referred to rising edge of CLK, specified for FCLD. CIN setup time is typically 1.2 ns, specified for FCLD, CIN.
[9]Referred to 1.6 V point of the rising edge of CLK. See Timing Diagram.
[10]Referenced to 1.6 V point of the rising edge of CLK for 1.6 V point of the rising/falling edge of SIN [0:11]; or the falling edge of DRDY. Load is shown below.
[11]Referenced from 1.6 V point of the rising/falling edge of SIN[0:11] to 1.6 V point of the falling edge of DATA READY. Specified driving AD9713B; no additional capacitive load.
[12]Referenced from 1.6 V point of rising edge of CLK to 1.6 V point of the rising/falling edge of COUT.
[13]Based on proprietary phase-to-sine algorithm, TGLE HIGH.
[14]Referred to CLK for FCLD high. See Timing Diagram.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C; parameter is guaranteed by design and characterization at temperature extremes.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.

Parameters based on characterization testing have limits based on 6 sigma of a normal distribution; typical values are the mean of the distribution.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S$) . . . . . −0.5 V to +7 V
Input Voltage . . . . . −0.5 V to $+V_S$ +0.5 V
Output Voltage Swing . . . . . −0.5 V to $+V_S$ +0.5 V
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Maximum Junction Temperature[2] . . . . . +150°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +250°C

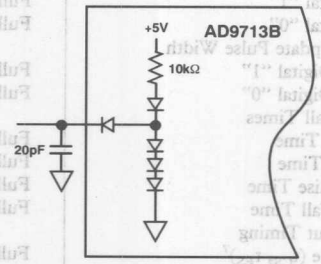
NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedance; part soldered in place:
θ_{JA} = 62°C/W
θ_{JC} = 7°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD9955KS-66[2]	0°C to +70°C	80-Terminal Plastic Quad Flatpack	S-80
AD9955KS-6[3]	0°C to +70°C	80-Terminal Plastic Quad Flatpack	S-80
AD9955/PCB	N/A	DDS Evaluation Board	

NOTES
[1]For outline information see Package Information section.
[2]Model AD9955KS-66 units are shipped in a standard JEDEC tray; minimum order quantity is 66 units (1 full tray).
[3]AD9955KS-6 units are shipped in a nonstandard tray; minimum order quantity is 6 units (1 full tray). Three nonstandard trays will fit in a standard JEDEC tray outline, allowing use with standard assembly equipment. Contact factory for details.

NOTE: All units are dry packed to inhibit moisture absorption. Units which are exposed to air for more than 48 hours should be baked for 24 hours at +125°C prior to assembly.

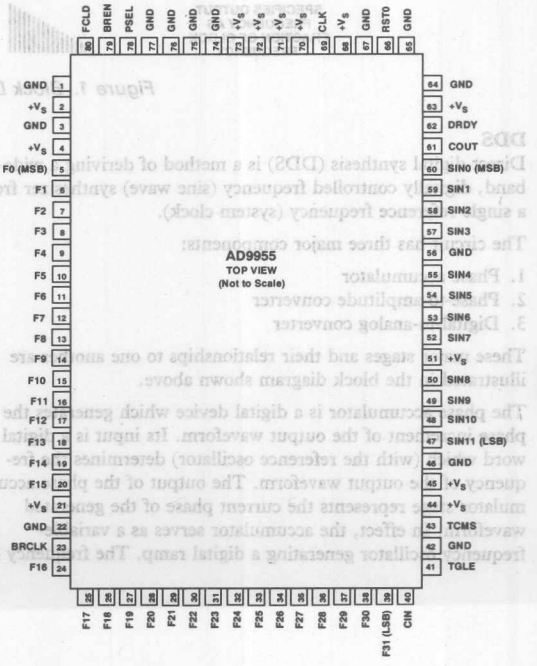


AD9955 Load Circuit

AD9955 PIN DESCRIPTIONS

Name	Description
GND	Ground Reference Voltage Connection.
$+V_S$	Positive voltage power connection, nominally +5 V.
BRCLK	Buffer Register Clock. Data inputs are loaded into the Frequency Control Word Buffer Register on the rising edge of BRCLK when register is enabled (BREN input at Logic "1").
CLK	System Clock. Continuous TTL signal for synchronizing all internal operations, except loading of Frequency Control Word Buffer Register; rising edge initiates synchronization.
F[0:31]	32 parallel data inputs for loading frequency tuning word.
BREN	Buffer Load Enable Signal. Enables loading of data into the Frequency Control Word Buffer Register. If BREN is logic "0," register retains its contents. If BREN is Logic "1," theFrequency Control Word Buffer Register either (1) parallel loads the data present at F[0:31] inputs (PSEL = HIGH) or (2) serially shifts data present at F[31] input (PSEL = LOW).
FCLD	Frequency Control Load Enable Signal. FCLD = HIGH enables loading of data from Frequency Control Word Buffer Register into Frequency Control Register. Loading takes place on next rising edge of CLK signal. FCLD = LOW disables loading of data.
DRDY	Data Ready Signal. Output data (SIN [0:11]) is valid on the rising edge of DRDY, which tracks propagation delay variations of the output data vs. temperature. The duty cycle of DRDY is dependent on the duty cycle of the CLK input. The DRDY signal should be used only for applications which have a very high clock rate (85 Msps) and require operation over a wide temperature range. Normally allowed to float.
CIN	Carry-In signal is provided as the carry input to the least significant bit (LSB) of the 32-bit adder in the phase accumulator. This signal is used as the carry input only if the TGLE signal is a logic zero; carry has 1 LSB weight, and is used for stacking units for 64-bit DDS. Normally tied to ground.
TGLE	Carry Toggle Enable. When HIGH, the CIN signal is disabled, and the Carry-In toggles internally between HIGH and LOW on each clock (CLK) cycle to reduce the worst case spurious response of the digital output signal by 3.92 dB. Normally tied to ground.
TCMS	Twos Complement/Magnitude Mode Select. Selects binary output format of data on SIN[0:11] outputs. If TCMS is a Logic "1," format of output data at SIN[0:11] is in twos complement format. If TCMS is a Logic "0," data is binary unsigned magnitude format. Normally tied to ground.
SIN[0:11]	12 parallel data bits comprising the sine data output. Frequency of the sine data outputs is defined by the Frequency Control Register (Δ phase) as $f_{OUT} = f_{CLK}\left(\frac{\Delta\ phase}{2^{32}}\right)$ Binary data format of 12-bit samples is either twos complement or unsigned magnitude, determined by TCMS signal.
RST0	Reset Phase to Zero Signal. Activates synchronous reset of the Phase Accumulation Register to a binary value of "0," or zero radians. Reset is enabled when RST0 is a Logic "1" and takes place on rising edge of system clock (CLK). Normally low.
COUT	Carry-Out signal output of the 32-bit adder in the phase accumulator; used for stacking two AD9955 units for 64-bit DDS. Normally allowed to float.
PSEL	Parallel/Serial Frequency Control Word Buffer Input Selector. Selects mode for loading the Buffer Register. If a load is enabled (BREN = "1"), and PSEL is a Logic "1," data is parallel loaded into the Frequency Control Word Buffer Register from the F0:31] inputs on the next rising edge of BRCLK. If a load is enabled and PSEL is a Logic "0," data is serially shifted into the Frequency Control Word Buffer Register from the F[31] input on rising edge of BRCLK.

PIN DESIGNATIONS



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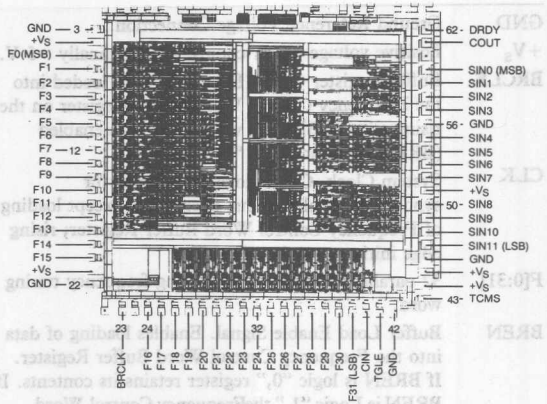
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	Ground
Passivation	Oxynitride
Die Attach	Epoxy
Bond Wire	Gold



AD9955 Chip Layout

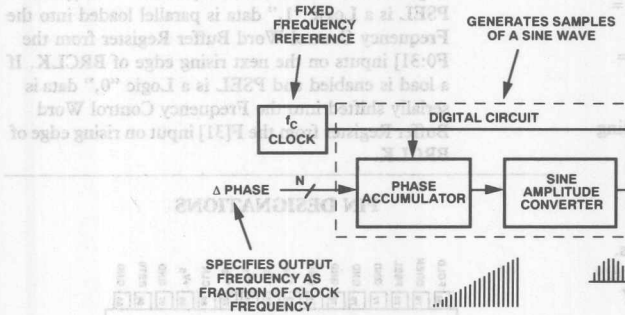


Figure 1. Block Diagram of DDS Generator

DDS

Direct digital synthesis (DDS) is a method of deriving a wide-band, digitally controlled frequency (sine wave) synthesizer from a single reference frequency (system clock).

The circuit has three major components:

1. Phase accumulator
2. Phase-to-amplitude converter
3. Digital-to-analog converter

These major stages and their relationships to one another are illustrated in the block diagram shown above.

The phase accumulator is a digital device which generates the phase increment of the output waveform. Its input is a digital word which (with the reference oscillator) determines the frequency of the output waveform. The output of the phase accumulator stage represents the current phase of the generated waveform. In effect, the accumulator serves as a variable-frequency oscillator generating a digital ramp. The frequency of the signal is defined by Δphase as

$$f_{OUT} = \frac{\Delta phase}{\Delta phase_{MAX}} f_{CLOCK} = \frac{\Delta phase}{2^N} f_{CLOCK}$$

Translating phase information from the phase accumulator into amplitude data takes place in the phase-to-amplitude converter. This is most commonly accomplished by means of a look-up table (LUT) stored in memory, but may be calculated instead using a digital algorithm to minimize circuit complexity and/or increase the update rate.

In the final step of frequency synthesis, amplitude data is converted into an analog signal. This is done by a digital-to-analog (D/A) converter which must have good linearity; low glitch impulse; and fast, symmetrical rise and fall times. When it does, the frequency synthesizer is able to produce a spectrally pure waveform.

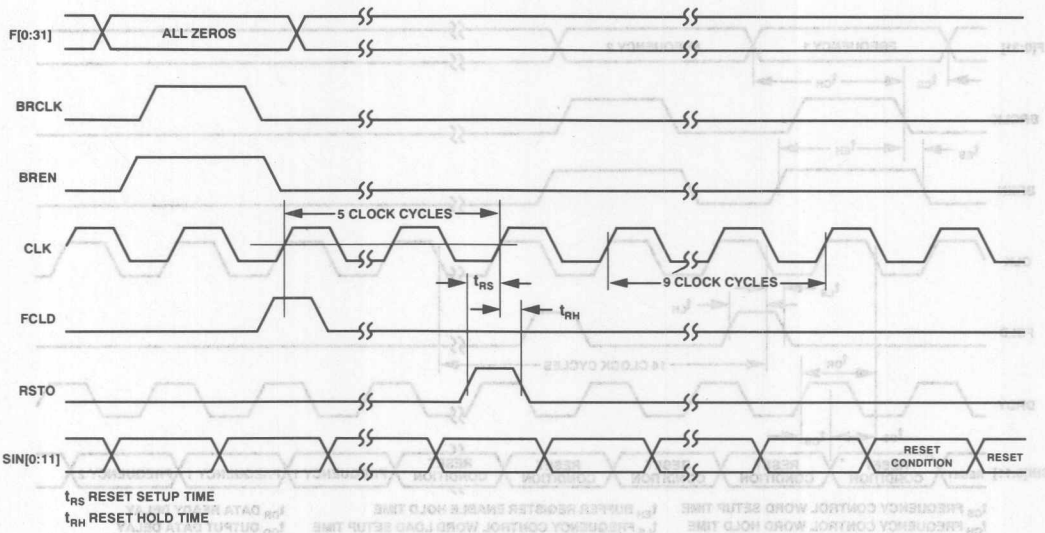


Figure 2. Reset Timing

AD9955 DIRECT DIGITAL SYNTHESIZER

The AD9955 is a digital device which integrates a 32-bit phase accumulator and 15-bit phase to 12-bit sine amplitude converter (see block diagram). The circuit is fabricated in a CMOS process technology, and designed to minimize the number of external devices necessary to implement a high speed DDS system.

Phase Accumulator Architecture

The phase accumulator is comprised of 8 pipelined, 4-bit adder cells to achieve the typical 100 MHz operation. The pipelined accumulator requires the use of input data alignment registers between the frequency control register and the accumulator to maintain the phase-coherent switching characteristics of the DDS. The alignment registers on the 16 least significant bits of the accumulator were eliminated to save power and reduce the number of pipeline delays; this results in a maximum phase discontinuity of 0.005°.

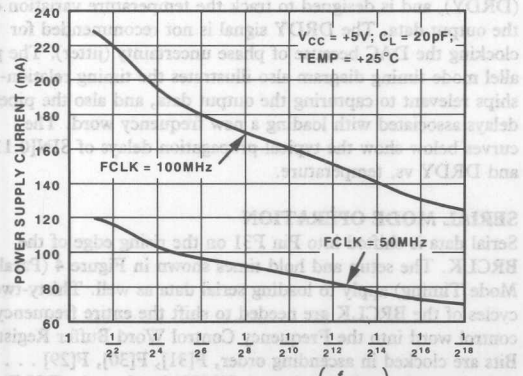


Figure 3. Power Supply Current vs. Output Frequency

The accumulator incorporates carry input and output pins (CIN and COUT) to enable stacking of devices to achieve greater than 32-bit resolution. In normal operation, CIN will be connected to ground, and COUT allowed to float.

An additional feature of the AD9955 accumulator is controlled by the TGLE pin. With this pin tied HIGH, the CIN pin is disabled and the carry input is internally toggled on successive clock cycles. The toggling of the carry input has two major benefits. The theoretical worst case spur is reduced by 3.92 dB, making the worst case spurious free dynamic range of the SIN[0:11] outputs 90.3 dBc. In addition, the DDS spur performance is made more consistent versus frequency due to the randomizing of the errors introduced by possible DAC nonlinearities.

Resetting the AD9955

The synchronous reset function (RST0) resets the output of the phase accumulator to zero radians, allowing the user to initialize the AD9955 from a known state. A reminder: the RSTO signal does not affect the contents of the alignment registers on either side of the adders. To properly reset the AD9955 to zero radians (SIN[0:11] = 1000 0000 0000), perform the following steps in the order listed:

1. Frequency input should be preloaded to zero (F[0:31] = 0; see loading the AD9955).
2. Four clock cycles must pass to clear the prealignment registers.
3. The RSTO signal should go HIGH for at least 12 ns, and meet required setup (t_{RS}) and hold (t_{RH}) times.
4. Nine additional clock cycles must pass to clear the post-alignment registers and allow the new tuning word (0 radians) to propagate through the phase to sine amplitude conversion circuitry.

Critical timing and pipeline delays required for resetting the AD9955 are illustrated in the reset timing diagram. After the RSTO signal is returned to LOW, a new frequency can be

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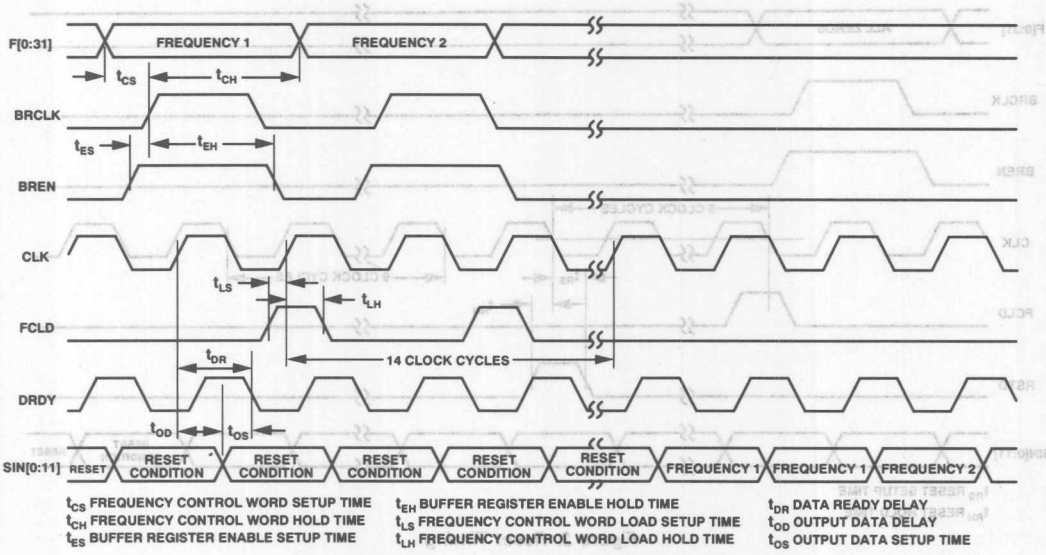

Figure 4. Parallel Mode Timing

loaded into the frequency control register; the SIN[0:11] outputs will remain at the midscale value for 14 clock cycles while the new tuning word propagates through the AD9955.

Loading the Frequency Control Word

For convenience, the frequency control register is double buffered at the inputs to allow asynchronous loading of a new frequency control word. The frequency control word buffer register can be loaded in either parallel (PSEL = HIGH) or serial (PSEL = LOW) mode. The data is clocked on the rising edge of the BRCLK signal when the BREN pin is held HIGH. In serial mode, the data is fed through the LSB (F[31]) and requires multiple clock edges to shift in data.

Once new frequency data is loaded into the frequency control word buffer, it is passed into the frequency control register on the next rising edge of the CLK signal following a HIGH signal on the FCLD pin. The new frequency control word is then used as the input to the phase accumulator and it begins to accumulate at the new rate. The Parallel Mode Timing diagram illustrates the critical timing relationships for loading new frequency data into the AD9955 from the reset condition; these relationships remain the same for any arbitrary condition.

Phase to Sine Architecture

The phase to sine amplitude converter calculates the sine amplitude using a proprietary algorithm for the first 90° of the sine cycle, and takes advantage of the symmetry of the waveform to calculate the remaining quadrants. Only the 15 most significant bits of the phase accumulator output are needed to achieve the 12-bit accuracy of the SIN[0:11] outputs.

In normal operation (TGLE = LOW), the frequency tuning word may take on both odd and even values. Odd frequency input words will result in a spurious free dynamic range (SFDR) of 90.3 dBc, while even frequency words may have spurious frequency content as high as 86.4 dBc. The carry toggle feature discussed above guarantees a worst case SFDR of the frequency tuning words of 90.3 dBc.

The architecture and implementation of the phase to sine algorithm uses several compression techniques to reduce the amount of internal memory required, and to guarantee a minimum throughput rate of 85 MHz, a new benchmark for CMOS DDS circuits. Accordingly, the CLK input is TTL logic compatible, and buffered internally to minimize input capacitance. Although most devices will operate with a 50% duty cycle on CLK input, guaranteed operation at 85 MHz will require adjustment of clock duty cycle (see specification table). All other inputs and outputs are CMOS logic compatible.

SIN Outputs

The SIN[0:11] outputs of the phase to sine conversion circuitry are latched at the output to minimize data skew. The TCMS control signal specifies the format of the output data as either binary unsigned magnitude or two's complement format. The output data is valid on the rising edge of the data ready signal (DRDY), and is designed to track the temperature variation of the output data. The DRDY signal is not recommended for clocking the DAC because of phase uncertainty (jitter). The parallel mode timing diagram also illustrates the timing relationships relevant to capturing the output data, and also the pipeline delays associated with loading a new frequency word. The curves below show the typical propagation delays of SIN[0:11] and DRDY vs. temperature.

SERIAL MODE OPERATION

Serial data is shifted into Pin F31 on the rising edge of the BRCLK. The setup and hold times shown in Figure 4 (Parallel Mode Timing) apply to loading serial data as well. Thirty-two cycles of the BRCLK are needed to shift the entire frequency control word into the Frequency Control Word Buffer Register. Bits are clocked in ascending order, F[31], F[30], F[29] . . . with the MSB clocked in last. A HIGH signal on the FCLD pin allows all 32 bits to pass to the Frequency Control Register on the next rising edge of the CLK.

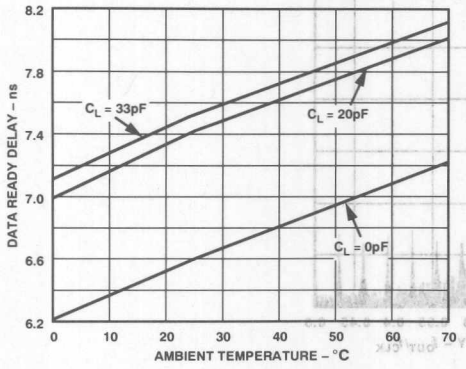

Figure 5. Data Ready Delay vs. Ambient Temperature

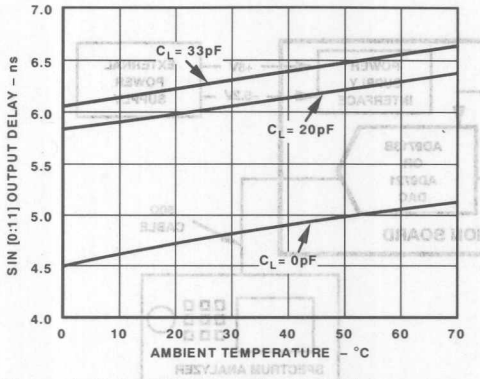

Figure 6. Output Delay vs. Ambient Temperature

Applications Information

The AD9955 can be used in digital demodulation applications to provide a digital frequency reference, or combined with a DAC to provide an analog frequency reference. In the latter application, a DAC with exceptional ac performance is required. The diagram below gives a recommended hookup for a complete direct digital synthesizer employing the AD9955 and the AD9721, a 10-bit 100 Msps DAC.

As in all high speed applications, proper layout is critical; it is particularly important when both analog and digital signals are involved. Analog signal paths should be kept as short as possible, and properly terminated to avoid reflections.

Digital signal paths should also be kept short, and run lengths matched to avoid propagation delay mismatch. In the diagram, series resistors (130 ohms) are inserted in the connections between the SIN[0:9] outputs of the AD9955 and the data inputs of the AD9721 (D_1–D_{10}) to reduce data feedthrough effects and to insure that the setup and hold times of the AD9721's input register are met over the commercial temperature range (0°C to +70°C).

Layout of the ground circuit is a critical factor. A single, low impedance ground plane will reduce noise on the circuit ground. Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane, and provide low impedance power planes.

Evaluation Board

An evaluation board is available which combines the AD9955 and either the AD9713B, an 80 Msps 12-bit DAC, or the AD9721, a 10- bit 100 Msps DAC, both of which are supplied with the board. This simplifies the task of evaluating and characterizing the DDS synthesizer. The block diagram shown in Figure 9 illustrates its operation. For more information, please consult the AD9955/PCB data sheet.

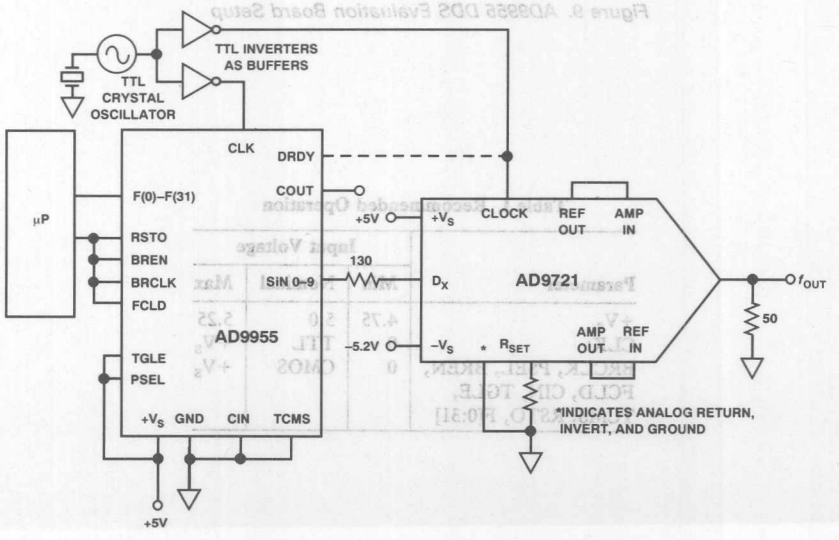

Figure 7. AD9955/AD9721 DDS Synthesizer

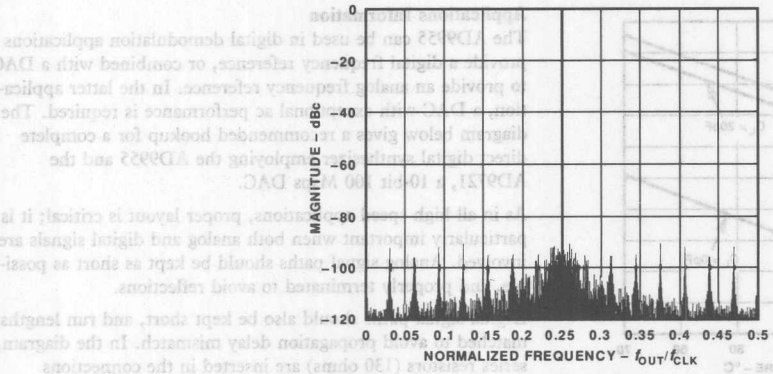

Figure 8. AD9955 Output Spectrum

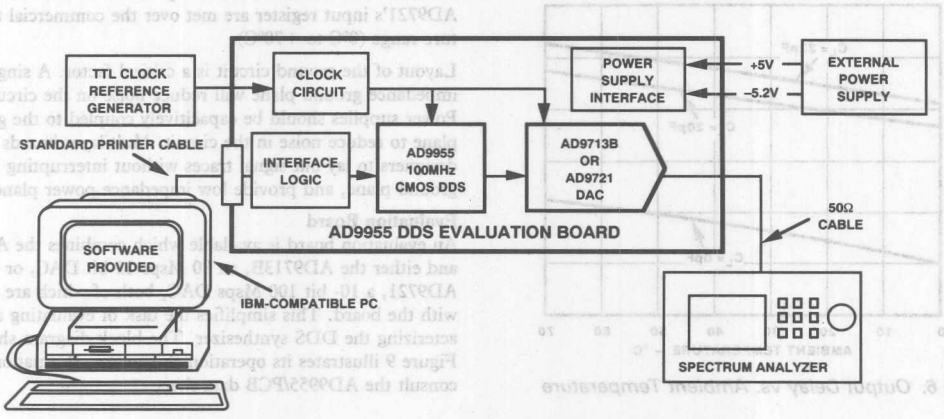

Figure 9. AD9955 DDS Evaluation Board Setup

Table I. Recommended Operation

Parameter	Input Voltage		
	Min	Nominal	Max
$+V_S$	4.75	5.0	5.25
CLK	0	TTL	$+V_S$
BRCLK, PSEL, BREN, FCLD, CIN, TGLE, TCMS, RSTO, F[0:31]	0	CMOS	$+V_S$

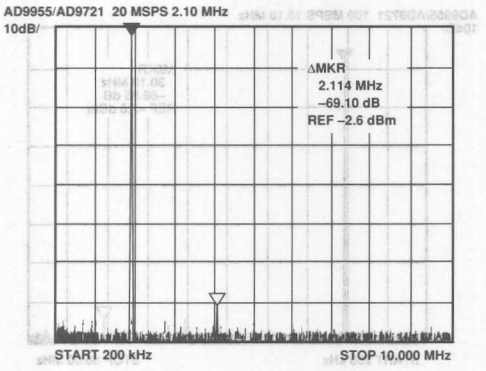

Figure 10. AD9955/AD9721 Output Spectrum

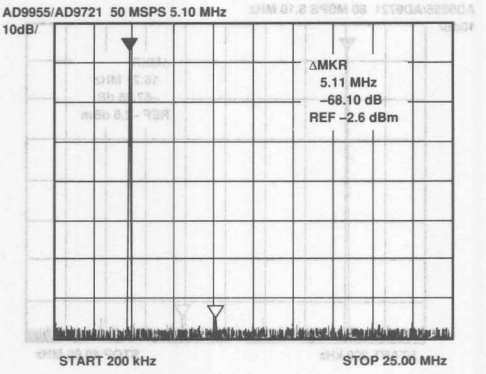

Figure 13. AD9955/AD9721 Output Spectrum

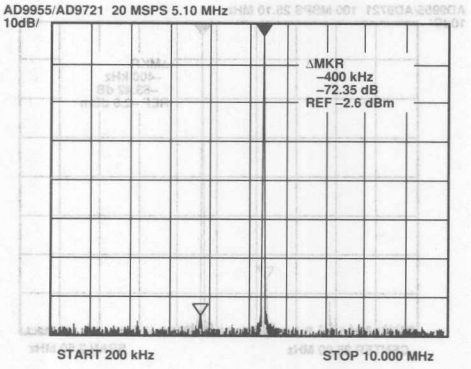

Figure 11. AD9955/AD9721 Output Spectrum

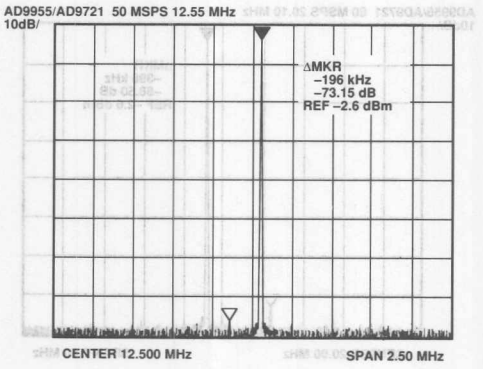

Figure 14. AD9955/AD9721 Output Spectrum

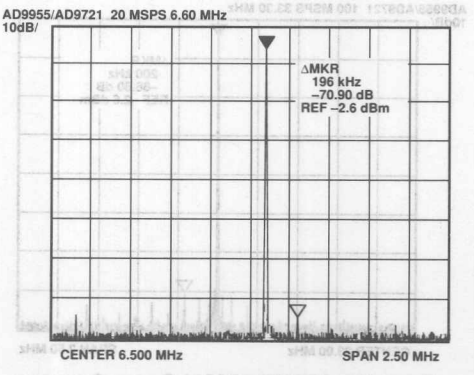

Figure 12. AD9955/AD9721 Output Spectrum

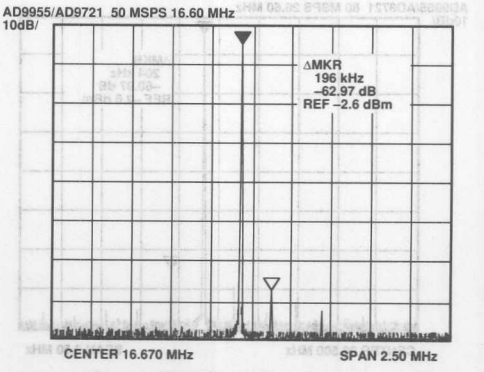

Figure 15. AD9955/AD9721 Output Spectrum

21

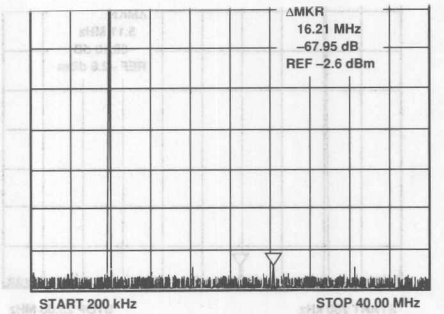

Figure 16. AD9955/AD9721 Output Spectrum

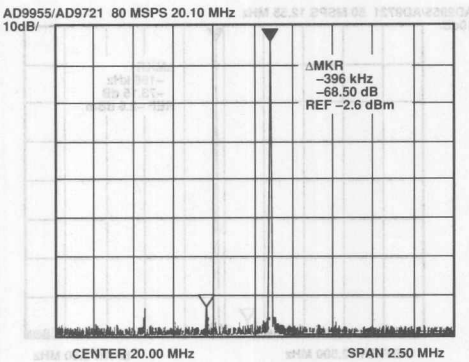

Figure 17. AD9955/AD9721 Output Spectrum

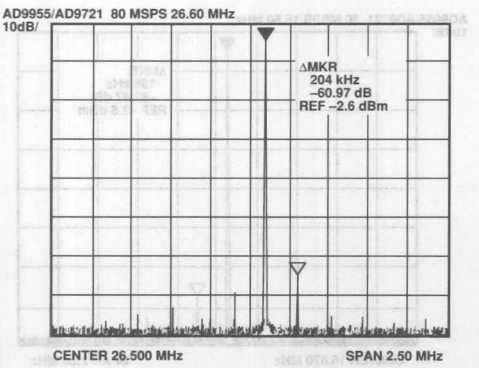

Figure 18. AD9955/AD9721 Output Spectrum

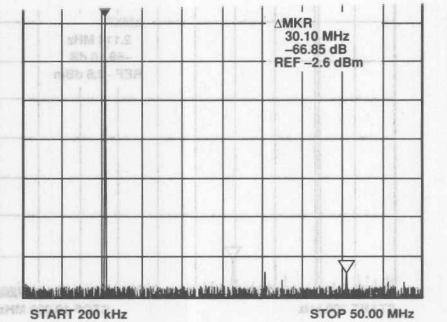

Figure 19. AD9955/AD9721 Output Spectrum

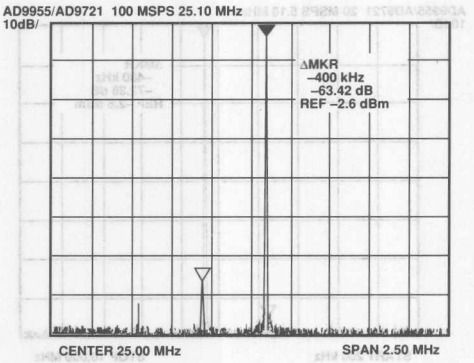

Figure 20. AD9955/AD9721 Output Spectrum

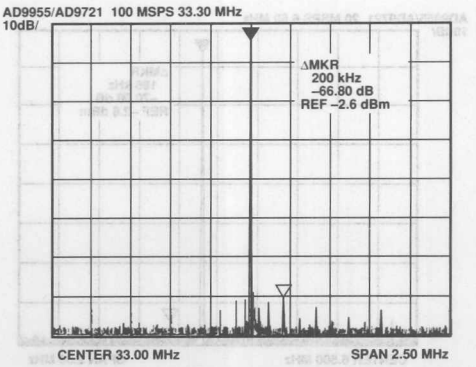

Figure 21. AD9955/AD9721 Output Spectrum

Power Supplies
Modular AC/DC Power Supplies

GENERAL DESCRIPTION

Analog Devices offers a broad line of modular ac/dc power supplies that provide both OEMs and designers a reliable, easy to use, low-cost solution to their power requirements. Models are available in PC mountable and chassis mountable designs with 5 volt to 15 volt (single, dual, triple) outputs and current ratings from 100 mA to 5 amps. Since these modular supplies are fully encapsulated, no trimming or external component selection is necessary; simply mount the unit, connect power and output leads, and you're on the air! Most Analog Devices' power supplies are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

AC/DC POWER SUPPLY FEATURES

- Current Limit Short Circuit Protection
- PC Mounted and Chassis Mounted Versions
- Single (+5 V), Dual (±15 V), and Triple (±15 V/+5 V) Output Supplies
- Current Outputs:
  100 mA to 500 mA for Dual and Triple Output Supplies
  1000 mA to 5000 mA for Single Output Supplies
- Wide Input Voltage Range
- Low Output Ripple and Noise
- Excellent Line & Load Regulation Characteristics
- High Temperature Stability
- Free-Air Convection Cooling; No External Heat Sink Required

GENERAL SPECIFICATIONS

Power Requirements
- Input Voltage Range: 105 V ac to 125 V ac
- Frequency: 50 Hz to 250 Hz

Electrical Specifications
- Temperature Coefficient: 0.02%/°C
- Output Voltage Accuracy: ±2%, max
  See Specifications Table
- Breakdown Voltage: 500 V rms, min
- Isolation Resistance: 50 MΩ
- Short Circuit Protection: All ac/dc power supplies employ current limiting. They can withstand substantial overload including direct short. Prolonged operation should be avoided since excessive temperature rises will occur.

Environmental Requirements
- Operating Temperature Range: −25°C to +71°C
- Storage Temperature Range: −25°C to +85°C

SPECIFICATIONS – Typical @ +25°C and 115 V ac 60 Hz unless otherwise noted*

	Type	Model	Output Voltage Volts	Output Current mA	Line Reg. max %	Load Reg. max %	Output Voltage Error max	Ripple & Noise mV rms max	Dimensions Inches
PC Board Mounted	Dual Output	902	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		902-2	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×0.875
		920	±15	±200	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5×2.5×1.62
	Single Output	905	5	1000	0.02	0.05	±1%	1	3.5×2.5×1.25
		922	5	2000	0.02	0.05	±1%	1	3.5×2.5×1.62
	Triple Output	923	±15	±100	0.02	0.02	±1%	0.5	3.5×2.5×1.25
			+5	500	0.02	0.05	±1%	0.5	
Chassis Mounted	Dual Output	970	±15	±200	0.05	0.05	±2%	1	4.4×2.7×1.45
		975	±15	±500	0.05	0.05	±2%	1	4.4×2.7×2.00
	Single Output	955	5	1000	0.05	0.15	±2%	2	4.4×2.7×1.45
		976	5	3000	0.05	0.10	±2%	100 (p-p typ)	4.75×2.7×1.45
		977	5	5000	0.05	0.10	±2%	100 (p-p typ)	4.75×2.7×1.45

*Consult Analog Devices Power Supplies Catalog for additional information.
Specifications subject to change without notice.

Power Supplies
Modular DC/DC Converters

GENERAL DESCRIPTION

Analog Devices' line of compact dc/dc converters offers system designers a means of supplying a reliable, easy to use, low cost solution to a variety of floating (analog and digital) power applications. These devices provide high accuracy, short circuit protected, regulated outputs with very low output noise and ripple characteristics.

Nine models are offered in four power levels of 1 watt, 1.8 watts, 4.5 watts and 6 watts. Input voltage versions include 5 volt, 12 volt and 28 volt with output ranges as follows: +5 volt, ±12 volts and ±15 volts at ±40 mA to 1000 mA output current capability.

Most models are high efficiency (typically over 60% at full load) and feature complete 6-sided continuous shielding for EMI/RFI protection. A π-type input filter is contained, in some models, which virtually eliminates the effects of reflected input ripple current. Most Analog Devices' dc/dc converters are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

DC/DC POWER SUPPLY FEATURES

- Inaudible (>20 kHz) Converter Switching Frequency
- Continuous, Six-Sided EMI/RFI Shielding Except on 1 Watt and 1.8 Watt Models
- Output Short Circuit Protection (Either Output to Common)
- Automatic Restart After Short Condition Removed
- Automatic Starting with Reverse Current Injected into Outputs
- Low Output Ripple and Noise
- High Temperature Stability
- Free Air Convection Cooling
  No external heat sink or specification derating is required over the operating temperature range.

GENERAL SPECIFICATIONS FOR 1 W AND 1.8 W MODELS

Line Regulation – Full Range: ±0.3% (±1% max, 949)
Load Regulation – No Load to Full Load: ±0.4% (±0.5% max, 949)
Output Noise and Ripple: 20 mV p-p, with 15 µF tantalum capacitor across each output (2 mV rms max, 949)
Breakdown Voltage: 300 V dc min (500 V dc min, 949)
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C (+100°C, 949)
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

GENERAL SPECIFICATIONS FOR 4.5 W AND 6 W MODELS

Line Regulation – Full Range: ±0.07% max (±0.02% max, 960 Series) (±0.1% max, 943)
Load Regulation – No Load to Full Load: ±0.07% max (±0.02% max, 960 Series) (±0.1% max, 943)
Output Noise and Ripple: 1 mV rms max
Breakdown Voltage: 500 V dc min
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

SPECIFICATIONS – Typical @ +25°C at nominal input voltage unless otherwise noted*

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input[1] Voltage Range Volts	Input Current Full Load	Output Voltage Error max	Temperature Coefficient /°C max	Efficiency Full Load min	Dimensions Inches
943	5	1000	5	4.75/5.25	1.52 A	±1%	±0.02%	62%	2.0×2.0×0.38
958	5	100	5	4.5/5.5	200 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
941	±12	±150	5	4.75/5.25	1.17 A	±1%	±0.01%	58%	2.0×2.0×0.38
960	±12	±40	5	4.5/5.5	384 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
962	±15	±33	5	4.5/5.5	396 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
966	±15	±190	12	11.2/13.2	710 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
949	±15	±60**	5	4.65/5.5	0.6 A	±2%	±0.03%	58%	2.0×1.0×0.375
940	±15	±150	5	4.75/5.25	1.35 A	±1%	±0.01%	62%	2.0×2.0×0.38
945	±15	±150	28	23/31	250 mA	±0.5%	±0.01%	61%	2.0×2.0×0.38

NOTES
[1]Models 940 and 941 will deliver up to 120 mA output current (and Model 943 will deliver up to 600 mA) over an input voltage range of 4.65 V dc and 5.5 V dc.
*Consult Analog Devices Power Supplies Catalog for additional information.
**Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120 mA.
Specifications subject to change without notice.

Package Information
Contents

ADI Letter Designator	PMI Letter Designator	Package Description	MIL-M38510 Applicable Configuration	Page
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D-14	YB*	14-Lead	D1-3	23–5
D-16	QB*	16-Lead	D2-3	23–5
D-18	XB*	18-Lead	D6-3	23–5
D-20		20-Lead	D8-3	23–5
D-22	RB*	22-Lead		23–5
D-24	VB*	24-Lead		23–5
D-24A		24-Lead (Single Width)		23–5
D-28	TB*	28-Lead	D10-3	23–5
D-28A		28-Lead (Single Width)		23–5
D-40		40-Lead		23–5
D-48		48-Lead		23–5
Side Brazed DIP for Hybrids (Ceramic)				
DH-24A		24-Lead		23–5
DH-28		28-Lead		23–5
Bottom Brazed DIP (Ceramic)				
DH-40A		40-Lead		23–6
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Leadless Chip Carrier (Ceramic)				
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E-44A		44-Terminal		23–6
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G-223		223-Lead		23–7
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H-03A		3-Lead (TO-52)		23–8
H-03B		3-Lead (TO-5 Style)		23–8
	H	6-Lead (TO-78)		23–8
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H-12A		12-Lead (TO-8 Style)		23–8

*Special order only.

ADI Letter Designator	PMI Letter Designator	Package Description	MIL-M38510 Applicable Configuration	Page
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J-44		44-Lead		23–9
J-68		68-Lead		23–9
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M-40		40-Lead		23–9
M-46		46-Lead		23–9
Plastic DIP				
N-8	P	8-Lead		23–10
N-14	P	14-Lead		23–10
N-16	P	16-Lead		23–10
N-18	P	18-Lead		23–10
N-20	P	20-Lead		23–10
N-22	P	22-Lead		23–10
N-24	P	24-Lead		23–10
N-24A	P	24-Lead (Double Width)		23–10
N-24B		24-Lead		23–10
N-28	P	28-Lead		23–10
N-28A	P	28-Lead		23–10
N-40A	P	40-Lead		23–10
N-48	P	48-Lead		23–10
Plastic Leaded Chip Carrier (PLCC)				
P-20A	PC	20-Lead		23–10
P-28A	PC	28-Lead		23–10
P-44A		44-Lead		23–10
P-68A		68-Lead		23–10
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Cerdip				
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Q-16	Q	16-Lead	D2-1	23–11
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Q-20	R	20-Lead	D8-1	23–11
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ADI Letter Designator	PMI Letter Designator	Package Description	MIL-M38510 Applicable Configuration	Page
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RS-28		28-Lead		23–12
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S-52		52-Terminal		23–13
S-64		64-Terminal		23–13
S-80		80-Terminal		23–13
S-160		160-Terminal		23–13
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ST-64		64-Lead		23–13
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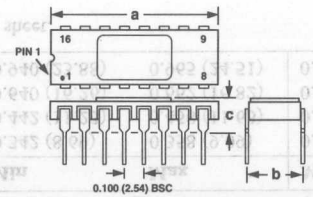
Z-16A		16-Lead		23–14
Z-16B		16-Lead		23–14
Z-16C		16-Lead		23–14
Z-28		28-Lead		23–14
Z-40		40-Lead		23–14
Z-68		68-Lead		23–14

ADI Letter Designator	PMI Letter Designator	Package Description	MIL-M38510 Applicable Configuration	Page
Small Outline (SO)				
R-8		8-Lead		23-12
	SO-8	8-Lead		23-12
R-14	SO-14	14-Lead		23-12
R-16A	SO-16	16-Lead		23-12
R-16	SOL-16	16-Lead (Wide Body)		23-12
R-18	SOL-18	18-Lead		23-12
R-20	SOL-20	20-Lead		23-12
R-24	SOL-24	24-Lead		23-12
R-24A		24-Lead		23-12
R-28	SOL-28	28-Lead		23-12
Shrink Small Outline Package (SSOP)				
RS-20		20-Lead		23-12
RS-24		24-Lead		23-12
RS-28		28-Lead		23-12
Plastic Quad Flatpack (PQFP)				
S-44		44-Terminal		23-13
S-52		52-Terminal		23-13
S-64		64-Terminal		23-13
S-80		80-Terminal		23-13
S-160		160-Terminal		23-13
Thin Quad Flatpack (TQFP)				
ST-48		48-Lead		23-13
ST-64		64-Lead		23-13
Thin Small Outline Package (TSOP)				
U-32		32-Lead		23-14
Leaded Chip Carrier (Ceramic)				
Z-8A		8-Lead		23-14
Z-16A		16-Lead		23-14
Z-16B		16-Lead		23-14
Z-16C		16-Lead		23-14
Z-28		28-Lead		23-14
Z-40		40-Lead		23-14
Z-68		68-Lead		23-14

Package Information—Outline Dimensions

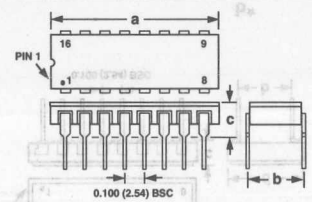
Side Brazed DIP (Ceramic)



ADI Letter Designator	PMI Letter Designator	Product Description	a* Min	a* Max	b* Min	b* Max	c* Min	c* Max
D-8		8-Lead	0.512 (13.005)	0.528 (14.41)	0.280 (7.11)	0.320 (8.13)		0.210 (5.33)
D-14	YB**	14-Lead		0.785 (19.94)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-16	QB**	16-Lead		0.840 (21.34)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-18	XB**	18-Lead		0.960 (23.38)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-20		22-Lead		1.060 (26.92)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-22	RB**	20-Lead		1.111 (28.22)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-24	VB**	24-Lead		1.290 (32.77)	0.590 (14.99)	0.620 (15.75)		0.225 (5.72)
D-24A		24-Lead (Single Width)		1.280 (32.51)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-28	TB**	28-Lead		1.490 (37.85)	0.590 (14.99)	0.620 (15.75)		0.225 (5.72)
D-28A		28-Lead (Single Width)		1.480 (37.59)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-40		40-Lead		2.096 (53.24)	0.521 (13.23)	0.630 (16.00)		0.225 (5.72)
D-48		48-Lead	2.376 (60.35)	2.424 (63.57)	0.520 (13.21)	0.630 (16.00)		0.225 (5.72)

*For complete package dimensions see reference manual or data sheet.
**Special order only

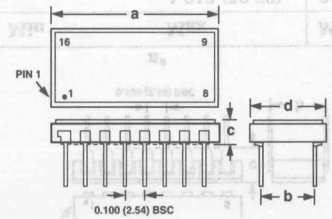
Side Brazed DIP for Hybrids (Ceramic)



ADI Letter Designator	PMI Letter Designator	Product Description	a* Min	a* Max	b* Min	b* Max	c* Min	c* Max
DH-24A		24-Lead		1.212 (30.79)	0.590 (14.99)	0.620 (15.75)		0.225 (5.72)
DH-28		28-Lead		1.414 (35.92)	0.590 (14.99)	0.610 (15.49)		0.225 (5.72)

*For complete package dimensions see reference manual or data sheet.

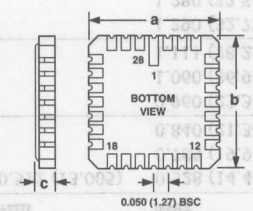
Package Information—Outline Dimensions



Bottom Brazed DIP (Ceramic)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*		d*	
			Min	Max	Min	Max	Min	Max	Min	M
DH-40A		40-Lead	2.074 (52.68)	2.116 (53.75)	0.89 (22.61)	0.91 (23.11)		0.225 (5.72)	1.08 (27.41)	1.
DH-48A		48-Lead	2.450 (62.23)	2.500 (63.50)	0.990 (25.15)	1.010 (25.65)	0.177 (4.50)	0.233 (5.92)	1.287 (32.69)	1.

*For complete package dimensions see reference manual or data sheet.

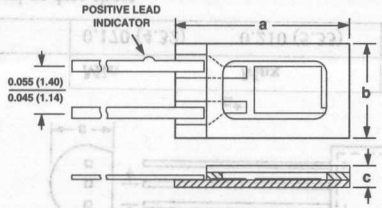


Leadless Chip Carrier (Ceramic)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
E-20A	RC	20-Terminal	0.342 (8.69)	0.358 (9.09)	0.342 (8.69)	0.358 (9.09)	0.064 (1.63)	0.10(
E-28A	TC	28-Terminal	0.442 (11.23)	0.458 (11.63)	0.442 (11.23)	0.458 (11.63)	0.064 (1.63)	0.10(
E-44A		44-Terminal	0.640 (16.26)	0.662 (16.82)	0.640 (16.26)	0.662 (16.82)	0.064 (1.63)	0.10(
E-68A		68-Terminal	0.940 (23.88)	0.965 (24.51)	0.940 (23.88)	0.965 (24.51)	0.065 (1.65)	0.103

*For complete package dimensions see reference manual or data sheet.

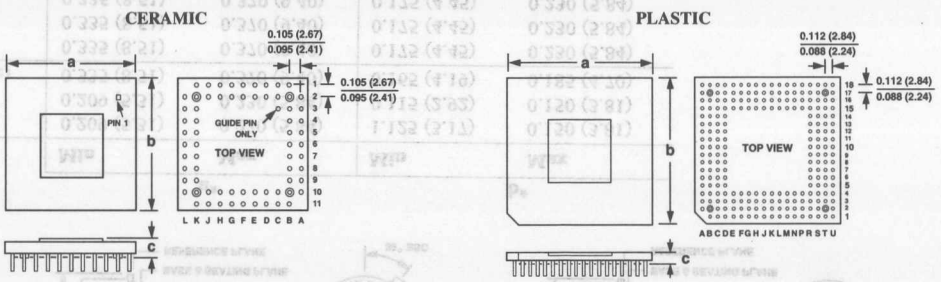
Flatpack (Ceramic)



ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
F-2A		2-Lead		0.250 (6.35)	0.081 (2.06)	0.093 (2.36)	0.044 (1.12)	0.066 (1.68)

*For complete package dimensions see reference manual or data sheet.

Pin Grid Array (Ceramic)



ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
G-68A		68-Lead	1.080 (27.43)	1.110 (28.19)	1.080 (27.43)	1.110 (28.19)	0.123 (3.12)	0.164 (4.17)
G-100A		100-Lead	1.308 (33.22)	1.332 (33.83)	1.308 (33.22)	1.332 (33.83)		0.169 (4.29)
G-223		223-Lead	1.844 (46.84)	1.876 (47.65)	1.844 (46.84)	1.876 (47.65)	0.138 (3.51)	0.164 (4.17)

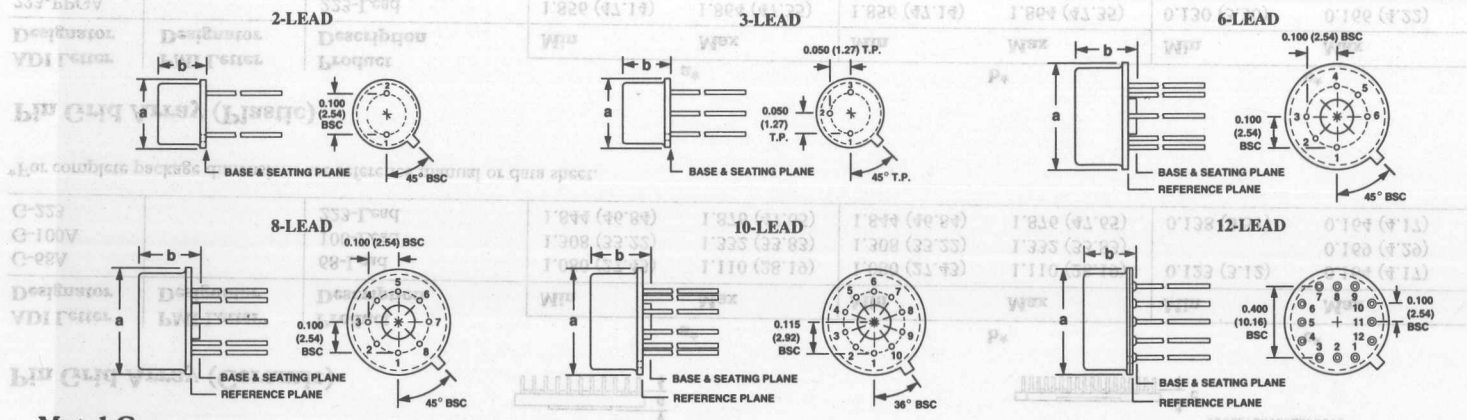
*For complete package dimensions see reference manual or data sheet.

Pin Grid Array (Plastic)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
223-PPGA		223-Lead	1.856 (47.14)	1.864 (47.35)	1.856 (47.14)	1.864 (47.35)	0.130 (3.30)	0.166 (4.22)

*For complete package dimensions see reference manual or data sheet.

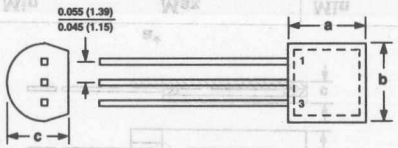
Package Information—Outline Dimensions



Metal Can

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*	
			Min	Max	Min	Max
H-02A		2-Lead	0.209 (5.31)	0.230 (5.84)	1.125 (3.17)	0.150 (3.81)
H-03A		3-Lead (TO-52)	0.209 (5.31)	0.230 (5.84)	0.115 (2.92)	0.150 (3.81)
H-03B		3-Lead (TO-5 Style)	0.335 (8.51)	0.370 (9.40)	0.165 (4.19)	0.185 (4.70)
	H	6-Lead (TO-78)	0.335 (8.51)	0.370 (9.40)	0.175 (4.45)	0.230 (5.84)
H-08A	J	8-Lead (TO-99)	0.335 (8.51)	0.370 (9.40)	0.175 (4.45)	0.230 (5.84)
H-10A	K	10-Lead (TO-100)	0.335 (8.51)	0.370 (9.40)	0.175 (4.45)	0.230 (5.84)
H-12A		12-Lead (TO-8 Style)	0.592 (15.04)	0.615 (15.62)	0.148 (3.76)	0.226 (5.74)

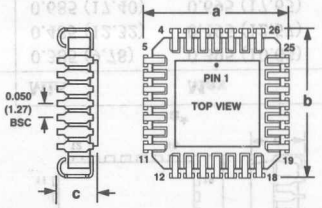
*For complete package dimensions see reference manual or data sheet.



Plastic

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
TO-92		3-Lead	0.170 (4.32)	0.210 (5.33)	0.175 (4.45)	0.205 (5.21)	0.125 (3.18)	0.165 (4.19)

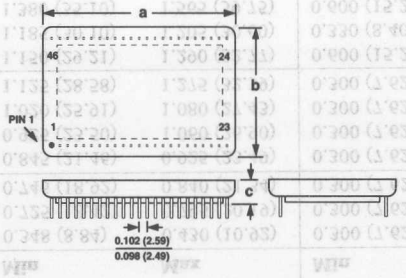
*For complete package dimensions see reference manual or data sheet.



J-Leaded Chip Carrier

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
J-28		28-Lead	0.498 (12.65)	0.491 (12.47)	0.489 (12.42)	0.491 (12.47)		0.125 (3.18)
J-44		44-Lead	0.680 (17.27)	0.700 (17.78)	0.680 (17.27)	0.700 (17.78)	0.100 (2.54)	0.135 (3.43)
J-68		68-Lead	0.980 (24.89)	1.000 (25.4)	0.980 (24.89)	1.000 (25.4)	0.100 (2.54)	0.135 (3.43)

*For complete package dimensions see reference manual or data sheet.



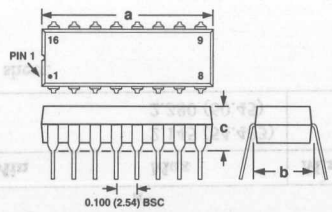
Metal Platform (DIP)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
M-40		40-Lead		2.145 (54.483)		1.145 (29.083)		0.19 (4.83)
M-46		46-Lead		2.380 (60.45)		1.580 (40.13)		0.231 (5.87)

*For complete package dimensions see reference manual or data sheet.

Package Information—Outline Dimensions

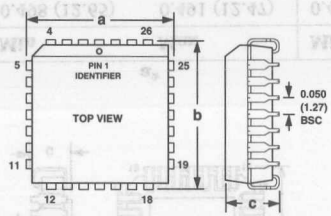
Plastic DIP



ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
N-8	P	8-Lead	0.348 (8.84)	0.430 (10.92)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-14	P	14-Lead	0.725 (18.42)	0.795 (20.19)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-16	P	16-Lead	0.745 (18.92)	0.840 (21.34)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-18	P	18-Lead	0.845 (21.46)	0.925 (23.49)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-20	P	20-Lead	0.925 (23.50)	1.060 (26.90)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-22	P	22-Lead	1.020 (25.91)	1.080 (27.43)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-24	P	24-Lead	1.125 (28.58)	1.275 (32.39)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-24A	P	24-Lead (Double Width)	1.150 (29.21)	1.290 (32.77)	0.600 (15.24)	0.625 (15.88)		0.250 (6.35)
N-24B		24-Lead	1.185 (30.10)	1.205 (30.60)	0.330 (8.40)	0.346 (8.80)	0.142 (3.60)	0.162 (4.10)
N-28	P	28-Lead	1.380 (35.10)	1.565 (39.75)	0.600 (15.24)	0.625 (15.88)		0.250 (6.35)
N-28A	P	28-Lead	1.440 (36.58)	1.450 (36.83)	0.594 (15.09)	0.606 (15.39)		0.200 (5.08)
N-40A	P	40-Lead		2.080 (52.83)	0.580 (14.73)	0.620 (15.75)		0.200 (5.08)
N-48	P	48-Lead	2.385(60.58)	2.480 (62.99)	0.590 (14.99)	0.630 (16.0)		0.250 (6.35)

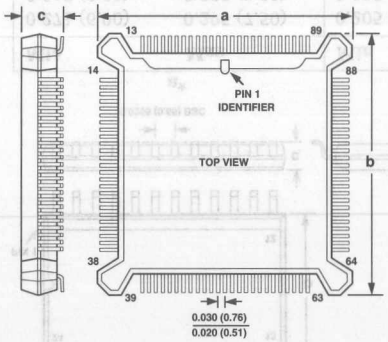
*For complete package dimensions see reference manual or data sheet.

Plastic Leaded Chip Carrier (PLCC)



ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
P-20A	PC	20-Lead	0.385 (9.78)	0.395 (10.03)	0.385 (9.78)	0.395 (10.03)	0.165 (4.19)	0.180 (4.57)
P-28A	PC	28-Lead	0.485 (12.32)	0.495 (12.57)	0.485 (12.32)	0.495 (12.57)	0.165 (4.19)	0.180 (4.57)
P-44A		44-Lead	0.685 (17.40)	0.695 (17.65)	0.685 (17.40)	0.695 (17.65)	0.165 (4.19)	0.180 (4.57)
P-68A		68-Lead	0.885 (22.48)	0.995 (25.27)	0.885 (22.48)	0.995 (25.27)	0.169 (4.29)	0.175 (4.45)

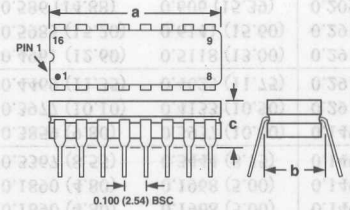
*For complete package dimensions see reference manual or data sheet.



Plastic Quad Flatpack

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
P-100		100-Lead	0.897 (22.78)	0.903 (22.94)	0.897 (22.78)	0.903 (22.94)	0.160 (4.06)	0.180 (4.57)

*For complete package dimensions see reference manual or data sheet.



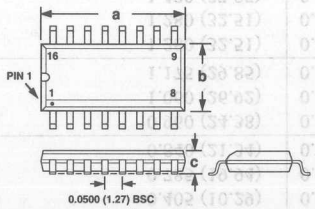
Cerdip

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
Q-8	Z	8-Lead		0.405 (10.29)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-14	Y	14-Lead		0.785 (19.94)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-16	Q	16-Lead		0.840 (21.34)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-18	X	18-Lead		0.960 (24.38)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-20	R	20-Lead		1.060 (26.92)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-22		22-Lead		1.175 (29.85)	0.390 (9.09)	0.420 (10.67)		0.200 (5.08)
Q-24	W	24-Lead		1.280 (32.51)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-24A		24-Lead (Wide Body)		1.280 (32.51)	0.590 (15.00)	0.620 (15.75)		0.200 (5.08)
Q-28	T	28-Lead		1.490 (37.85)	0.590 (14.99)	0.620 (15.75)		0.225 (5.72)

*For complete package dimensions see reference manual or data sheet.

Package Information—Outline Dimensions

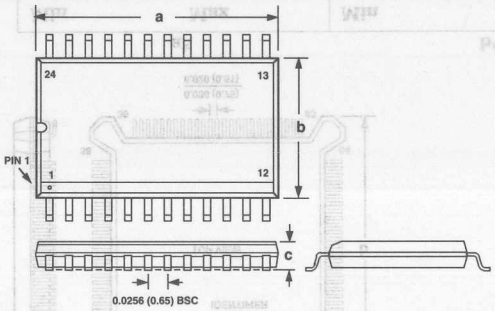
Small Outline (SO)



ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
R-8		8-Lead	0.1890 (4.80)	0.1968 (5.00)	0.1497 (3.80)	0.1574 (4.00)	0.094 (2.39)	0.102 (2.59)
	SO-8	8-Lead	0.1890 (4.80)	0.1968 (5.00)	0.1497 (3.80)	0.1574 (4.00)	0.0532 (1.35)	0.0688 (1.75)
R-14	SO-14	14-Lead	0.3367 (8.55)	0.3444 (8.75)	0.1497 (3.80)	0.1574 (4.00)	0.0532 (1.35)	0.0688 (1.75)
R-16A	SO-16	16-Lead	0.3859 (9.80)	0.3937 (10.00)	0.1497 (3.80)	0.1574 (4.00)	0.0532 (1.35)	0.0688 (1.75)
R-16	SOL-16	16-Lead (Wide Body)	0.3977 (10.10)	0.4133 (10.50)	0.2914 (7.40)	0.2992 (7.60)	0.0926 (2.35)	0.1043 (2.65)
R-18	SOL-18	18-Lead	0.4469 (11.35)	0.4625 (11.75)	0.2914 (7.40)	0.2992 (7.60)	0.0926 (2.35)	0.1043 (2.65)
R-20	SOL-20	20-Lead	0.4961 (12.60)	0.5118 (13.00)	0.2914 (7.40)	0.2992 (7.60)	0.0926 (2.35)	0.1043 (2.65)
R-24	SOL-24	24-Lead	0.5985 (15.20)	0.6141 (15.60)	0.2914 (7.40)	0.2992 (7.60)	0.0926 (2.35)	0.1043 (2.65)
R-24A		24-Lead	0.586 (14.88)	0.606 (15.39)	0.205 (5.21)	0.221 (5.61)	0.067 (1.70)	0.089 (2.25)
R-28	SOL-28	28-Lead	0.6969 (17.70)	0.7125 (18.10)	0.2914 (7.40)	0.2992 (7.60)	0.0926 (2.35)	0.1043 (2.65)

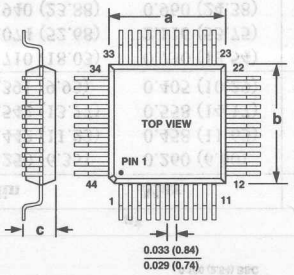
*For complete package dimensions see reference manual or data sheet.

Shrink Small Outline Package (SSOP)



ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
RS-20		20-Lead	0.271 (6.90)	0.295 (7.50)	0.205 (5.21)	0.212 (5.38)	0.068 (1.73)	0.078 (1.98)
RS-24		24-Lead	0.318 (8.08)	0.328 (8.33)	0.205 (5.21)	0.212 (5.38)	0.068 (1.73)	0.078 (1.98)
RS-28		28-Lead	0.397 (10.08)	0.407 (10.34)	0.205 (5.21)	0.212 (5.38)	0.068 (1.73)	0.078 (1.98)

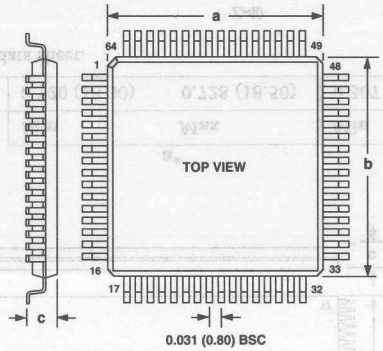
*For complete package dimensions see reference manual or data sheet.



Plastic Quad Flatpack (PQFP)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
S-44		44-Terminal	0.390 (9.91)	0.398 (10.11)	0.390 (9.91)	0.398 (10.11)		0.096 (2.44)
S-52		52-Terminal	0.390 (9.91)	0.398 (10.11)	0.390 (9.91)	0.398 (10.11)	0.084 (2.13)	0.094 (2.39)
S-64		64-Terminal		0.787 (20.0)		0.551 (14.0)		0.122 (3.10)
S-80		80-Terminal	0.7834 (19.90)	0.7913 (20.10)	0.6948 (17.65)	0.7145 (18.15)		0.1338 (3.40)
S-160		160-Terminal	1.098 (27.89)	1.106 (28.09)	1.096 (27.84)	1.106 (28.09)		0.160 (4.06)

*For complete package dimensions see reference manual or data sheet.

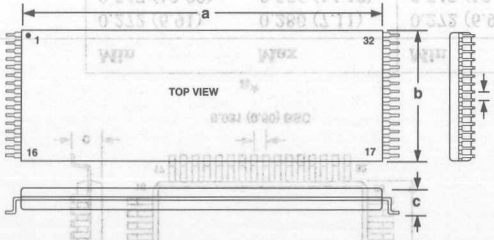


Thin Quad Flatpack (TQFP)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
ST-48		48-Lead	0.272 (6.91)	0.280 (7.11)	0.272 (6.91)	0.280 (7.11)		0.067 (1.70)
ST-64		64-Lead	0.547 (13.89)	0.556 (14.12)	0.547 (13.89)	0.556 (14.12)		0.063 (1.60)

*For complete package dimensions see reference manual or data sheet.

Package Information—Outline Dimensions

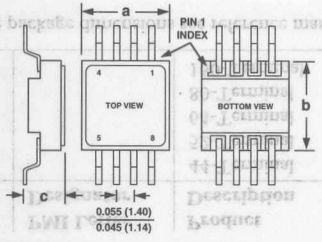


Thin Small Outline Package (TSOP)

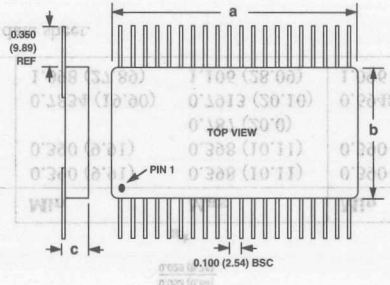
ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
U-32		32-Lead	0.720 (18.30)	0.728 (18.50)	0.307 (7.80)	0.323 (8.20)	0.037 (0.94)	0.0410 (1.04)

*For complete package dimensions see reference manual or data sheet.

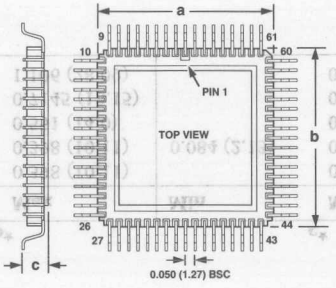
Z-08, Z-16A,BC, Z-28



Z-40



Z-68



Leaded Chip Carrier (Ceramic)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
Z-8A		8-Lead	0.250 (6.35)	0.260 (6.60)	0.250 (6.35)	0.260 (6.60)	0.018 (0.46)	0.098 (2.49)
Z-16A		16-Lead	0.442 (11.23)	0.458 (11.63)	0.442 (11.23)	0.458 (11.63)	0.103 (2.62)	0.133 (3.38)
Z-16B		16-Lead	0.542 (13.77)	0.558 (14.17)	0.542 (13.77)	0.558 (14.17)	0.113 (2.87)	0.143 (3.63)
Z-16C		16-Lead	0.391 (9.93)	0.405 (10.29)	0.2 (6.3)	0.260 (6.60)	0.018 (0.46)	0.098 (2.49)
Z-28		28-Lead	0.710 (18.03)	0.730 (18.54)	0.490 (12.45)	0.510 (12.95)		
Z-40		40-Lead	2.074 (52.68)	2.116 (53.75)	1.079 (27.41)	1.101 (27.97)		0.217 (5.51)
Z-68		68-Lead	0.940 (23.88)	0.960 (24.38)	0.940 (23.88)	0.960 (24.38)	0.092 (2.34)	0.118 (2.997)

*For complete package dimensions see reference manual or data sheet.

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INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us, or one of our authorized distributors.
3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed on pages 24–16 and 24–17) or our main office in Norwood, Massachusetts U.S.A. (617-329-4700).

MODEL NUMBERING

In this reference manual many of the data sheets for products having a number of standard options contain an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. Two model numbering schemes are used by Analog Devices. The first model numbering scheme is used for designating standard Analog Devices monolithic and hybrid products. The second scheme is used by our Precision Monolithics Division (formerly PMI) as designators for its product line.

Figure 1 shows the form of model number used for our proprietary standard monolithic ICs and many of our hybrids. It consists of an "AD" (Analog Devices) prefix, a 3-to-5-digit number,* an alphabetic performance/temperature-range designator and a package designator. One or two additional letters may immediately follow the digits ("A" for second-generation redesigned ICs, "DI" for dielectrically isolated CMOS switches, e.g., AD536AJH, AD7512DIKD).

Figure 2 shows a different numbering scheme used by our Precision Monolithics Division. This numbering scheme starts with a prefix which designates the device type and model number. It is then followed by a suffix consisting of alphabetic designators (as applicable) to indicate additional functional designations or options and packaging options.

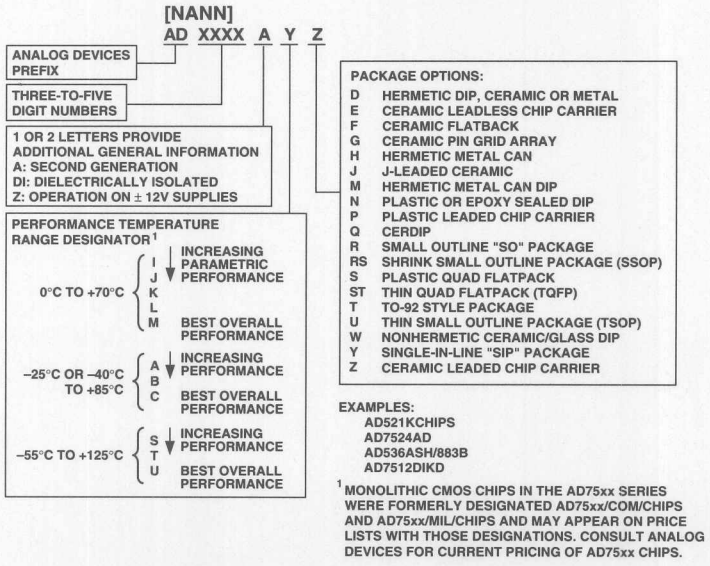

Figure 1. Model-Number Designations for Standard Analog Devices Monolithic and Hybrid IC Products. S, T and U Grades Have the Added Suffix /883B for Devices that Qualify to the Latest Revision of MIL-STD-883, Level B.

*For some models, the combination [digit][letter] [two or three digits] is used instead of ADXXXX, e.g., 2S80.

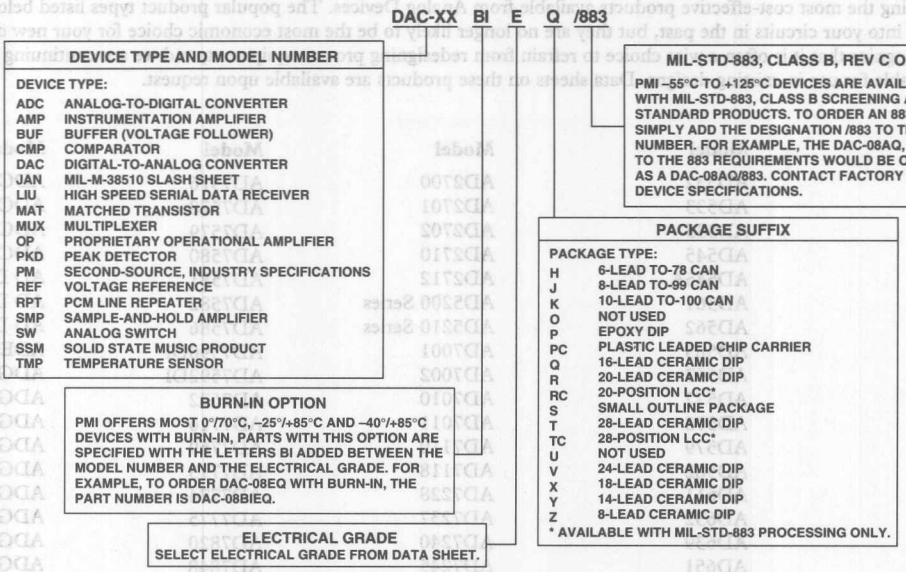

Figure 2. Precision Monolithics Division's Product Designations

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory.

Eligible customers may place their orders through our regional customer service centers by dialing 1-800-262-5645 (U.S.A. only) or through our representatives or authorized distributors. (The telephone numbers for our representatives or authorized distributors are listed on pages 24–16 and 24–17.) Analog Devices' minimum order value is $500.00.

WARRANTY AND REPAIR CHARGE POLICIES

All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Product Families Still Available

The information published in this Reference Manual is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs. Data sheets on these products are available upon request.

Model	Model	Model	Model	Model
AC1226	AD532	AD2700	AD7576	ADC1130
AC2626	AD533	AD2701	AD7578	ADC1131
AD2S44	AD535	AD2702	AD7579	ADC1140
AD2S47	AD545	AD2710	AD7580	ADC1143
AD2S65	AD545A	AD2712	AD7581	AD DAC08
AD2S66	AD561	AD5200 Series	AD7582	AD DAC71
AD2S75	AD562	AD5210 Series	AD7586	AD DAC72
AD2S110	AD563	AD7001	AD7590DI	ADEB770
AD203	AD567	AD7002	AD7592DI	ADG221
AD230	AD572	AD7010	AD7672	ADG222
AD231	AD578	AD7011	AD7716	ADG445
AD231A	AD579	AD7110	AD7769	ADG506A
AD232	AD582	AD7118	AD7773	ADG507A
AD232A	AD611	AD7228	AD7774	ADG526A
AD233	AD632	AD7237	AD7775	ADG527A
AD233A	AD639	AD7240	AD7820	ADG528A
AD234	AD651	AD7245	AD7848	ADG529A
AD235	AD675	AD7247	AD7850	AD OP07
AD236	AD730	AD7248	AD9003	AD OP27
AD237	AD741	AD7341	AD9003A	AD OP37
AD238	AD773	AD7371	AD9005A	ADSP-1008A
AD239	AD774	AD7501	AD9007	ADSP-1009A
AD241	AD796	AD7502	AD9014	ADSP-1010A
AD246	AD803	AD7503	AD9034	ADSP-1010B
AD346	AD805	AD7506	AD9502	ADSP-1012A
AD363	AD880	AD7507	AD9505	ADSP-1016A
AD363R	AD890	AD7510DI	AD9560	ADSP-1024A
AD364	AD891	AD7511DI	AD9610	ADSP-1080A
AD364R	AD891A	AD7512DI	AD9611	ADSP-1081A
AD365	AD892T/E	AD7520	AD9686	ADSP-1101
AD380	AD896	AD7522	AD9703	ADSP-1110A
AD386	AD897	AD7523	AD22001	ADSP-1401
AD389	AD899	AD7525	AD22050	ADSP-1402
AD390	AD1139	AD7533	AD22150	ADSP-1410
AD394	AD1154	AD7534	AD75019	ADSP-3128A
AD395	AD1170	AD7535	AD75069	ADSP-3201
AD396	AD1315	AD7536	AD75089	ADSP-3202
AD503	AD1317	AD7541	AD75090	ADSP-3210
AD504	AD1320	AD7541A	AD79024	ADSP-3211
AD506	AD1324	AD7542	AD ADC71	ADSP-3212
AD507	AD1334	AD7543	AD ADC72	ADSP-3220
AD507SH/883B	AD1341	AD7545	AD ADC80	ADSP-3221
AD510	AD1362	AD7545A	AD ADC84	ADSP-3222
AD515	AD1376	AD7546	AD ADC85	ADV101
AD515A	AD1377	AD7548	ADC170	ADV453
AD517	AD1378	AD7549	ADC908	ADV471
AD518	AD1380	AD7572	ADC910	ADV473
AD521	AD1403	AD7572A	ADC912	ADV475
AD522	AD2026	AD7574	ADC912A	ADV476

Model	Model	Model	Model	Model
ADV477	DRC1745	OP227	PM7628	1B41
ADV478	DRC1746	OP260	PM7645	1B51
ADV7120	HDS1240E	OP421	REF03	1S74
ADV7121	HDS1250A	OSC1758	REF05	2B20
ADV7122	HOS050/050A/050C	PKD01	REF08	2B22
ADV7128	HOS060/060A	PM108/208/308	REF10	2B23
ADV7141	HTC0300A	PM111/211	RPT82	2B24
ADV7146	HTS0010	PM119	RPT83	2B31
ADV7148	HTS0025	PM139	RPT85	2B34
ADV7150	IPA1764	PM148/248	RPT86	2B50
ADV7151	JM38510/11301/11302	PM155	RPT87	2B52
ADV7152	LIU01	PM155A	SDC1740/RDC1740	2B53
ADVFC32	MUX88	PM156	SDC1741/RDC1741	2B54
AMP03	OP01	PM156A	SDC1742/RDC1742	2B55
AMP05	OP02	PM157	SMP10	2B56
BUF03	OP04	PM157A	SMP11	2B57
CAV1210	OP05	PM219	SMP81	2B58
CMP01	OP06	PM239	SSM2013	2B59
CMP02	OP08	PM248	SSM2014	2S50
CMP05	OP09	PM308	SSM2015	2S80A
CMP08	OP10	PM355	SSM2016	2S81A
CMP404	OP11	PM356	SSM2018	2S82A
DAC01	OP12	PM562	SSM2044	3B Series
DAC02/03	OP14	PM725	SSM2045	4B Series
DAC05/06	OP15	PM741	SSM2047	5B Series
DAC10	OP16	PM747	SSM2100	6B Series
DAC20	OP17	PM0820	SSM2110	7B Series
DAC86	OP20	PM0828	SSM2120	277
DAC88	OP21	PM1008	SSM2122	281
DAC89	OP22	PM1012	SSM2125	284J
DAC100	OP32	PM2108	SSM2126	286J
DAC210	OP41	PM4136	SSM2131	289
DAC888	OP43	PM6012	SSM2132	290
DAC1136	OP44	PM7224	SSM2134	290A
DAC1138	OP50	PM7226	SSM2139	292
DAC1146	OP61	PM7226A	SSM2210	292A
DAC1408A	OP64	PM7524	SSM2220	310
DAC1508A	OP65	PM7528	SSM2300	365
DAC8012	OP80	PM7533	SW01/02	429
DAC8143	OP111	PM7541	SW201	451
DAC8212	OP147	PM7541A	SW202	453
DAC8841	OP150	PM7542	SW7510/7511	460
DAS1152	OP160	PM7543	1B21	741A
DAS1153	OP166	PM7545	1B22	755
DAS1158	OP207	PM7548	1B31	757
DAS1159	OP215	PM7574	1B32	759
				950

Analog Devices offers a wide variety of high performance DSP products. These products are not included in this manual because our new *Digital Signal Processing Reference Manual* is scheduled for publication in late 1994. That reference manual will provide complete data sheets for the design-in products listed below.

Model
AD28msp01
AD28msp02
AD1848
AD1849
AD1851
AD1856
AD1860
AD1864
AD1865
AD1866
AD1868
AD1878
AD1879
ADDS-2100A-ICE
ADDS-2101-EZ
ADDS-2101-ICE
ADDS-2111-EZ
ADDS-2111-ICE
ADDS-21msp50-EZ
ADDS-21msp50-ICE
ADDS-21xx-Software
ADDS-21020-EZ
ADDS-210xx-Software
ADSP-2100
ADSP-2100A
ADSP-2101
ADSP-2102
ADSP-2103
ADSP-2105
ADSP-2106
ADSP-2111
ADSP-2112
ADSP-2115
ADSP-21msp50A
ADSP-21msp51
ADSP-21msp55A
ADSP-21msp56A
ADSP-21010
ADSP-21020

Substitution Guide

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but—as a rule—they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, contact your local sales office.

Model	Closest Recommended Equivalent
AD2S34	None
AD2S46	None
AD101A	PM1008
AD108/208/308	AD705
AD108A/208A/308A	AD705
AD111/211/311	AD790
AD201A	PM2008
AD206	None
AD293	AD210
AD294	AD210
AD295	AD210
AD301A	PM3008
AD345	AD1324
AD351	AD790
AD362	AD1362
AD367	None
AD368	None
AD369	None
AD370/371	AD767
AD376	AD1376
AD381	AD744
AD382	AD744/AD845
AD392	AD664
AD395/883B	AD394/883B
AD501	AD711
AD502	AD711
AD505	AD843
AD506SH/883B	AD42626
AD508	AD517
AD509	AD843
AD511	AD711
AD512	AD711
AD513	AD711
AD514	AD711
AD516	AD711
AD520	AD524
AD523	AD549
AD528	AD711/744
AD530	AD533
AD531	AD532
AD540	AD544
AD559	AD557/AD558
AD565	AD565A
AD566	AD566A
AD575	AD573
AD583	AD585
AD612	AD524
AD614	AD524
AD674A	AD674B
AD682	AD781
AD689	AD587
AD770	Consult ADI
AD801	AD711
AD1145	AD7846
AD1147/48	AD669
AD1175	RTI870
AD1321	AD1324
AD1322	AD1324
AD1332	None
AD1408	AD558
AD1508	AD558
AD1678	AD678
AD1679	AD679
AD1779	AD779
AD1885	None
AD2002	None
AD2003	None
AD2004	None
AD2006	None
AD2008	None
AD2009	None
AD2010	None
AD2016	None
AD2020	None
AD2021	None
AD2022	None
AD2023	None
AD2024	None
AD2025	None
AD2027	None
AD2028	None
AD2033	None
AD2036	None
AD2037	None
AD2038	None
AD2040	None
AD2050	None
AD2051	None
AD2060	None
AD2061	None
AD2070	None
AD2071	None
AD3554	None
AD3860	AD567
AD5010/6020	AD9000
AD5201	AD578
AD5202	AD5212
AD5204	AD5214
AD5205	AD5215
AD5211	AD578
AD5240	AD ADC85
AD6012	AD565A
AD7005	AD7011/AD7013
AD7115	AD7111
AD7513	ADG201A
AD7516	AD7510DI
AD7519	None
AD7521	AD7541A
AD7527	AD7548
AD7530	AD7533
AD7531	AD7541A
AD7544	AD7548
AD7550	Consult ADI
AD7552	Consult ADI
AD7555	Consult ADI
AD7560	None
AD7570	AD7579/AD7580
AD7571	AD7579/AD7580
AD7583	AD7880+MUX
AD7772	Consult ADI
AD9005	AD9005B
AD9006	None
AD9011	AD9002
AD9016	None
AD9020SE/883B	AD9020SZ/883B
AD9020TE/883B	AD9020TZ/883B
AD9028	None
AD9038	None
AD9040	AD9040A
AD9060SE/883B	AD9060SZ/883B
AD9060TE/883B	AD9060TZ/883B
AD9300TE/883B	AD9300TQ/883B
AD9521	AD640
AD9615	AD9611/AD9617
AD9630AQ	AD9630AN
AD9630SQ/883B	AD9630AN
AD9685	AD96685
AD9687	AD96687
AD9688	AD9002
AD9712	AD9712B
AD9713	AD9713B
AD9768JQ	AD9768JD
AD9768SQ	AD9768SD
AD9768SE	AD9768SD
AD9950	AD9955
AD75062	None
AD75068	None
AD ADC816	AD7820/AD7821
ADC8S	AD673
ADC10Z	AD574A
ADC12QL	AD7578
ADC12QM	None
ADC12QZ	AD574A
ADC14I/17I	AD1170
ADC16Q	None
ADC1100	AD1170
ADC1102	AD7870
ADC1103	AD7572A
ADC1105	Consult ADI
ADC1109	AD7572A
ADC1111	AD574A
ADC1121	AD7880

Model	Closest Recommended Equivalent
ADC1123	AD7880
ADC1133	AD574A
ADCQM	None
ADCQU	AD574A
AD DAC100	AD561
ADG200	None
ADG201	ADG201A
ADLH0032	None
ADLH0033	None
ADLH0032G/CG	AD843
ADLH0033G/CG	AD9620/AD9630
ADM501	None
ADP501	None
ADREF01	REF01
ADREF02	REF02
ADSHC85	AD585
ADSHM5	HTC0300A
AMP01BX	AMP01AX
AMP01BX/883C	AMP01AX/883C
AMP05BX	AMP05AX
AMP05BX/883C	AMP05Z/883C
API1620/1718	Consult ADI
BDM1615/16/17	None
BUF03BJ/883C	BUF03AJ/883C
CAV0920/1020	AD9020/9060
CAV1202	AD9007
CAV1205	AD9007
CMP01Z	CMP01J
CMP05BJ	CMP05CJ
CMP05BZ	CMP05CZ
CMP05GJ	CMP05CJ
CMP404BY	CMP404AY
CMP404BY/883C	CMP404AY/883C
DAC02ACX1	DAC02CCX1
DAC05AX1	DAC02CCX1
DAC05EX1	DAC02CCX1
DAC10BX	DAC10FX
DAC10CX	DAC10GX
DAC10DF	AD568
DAC10H	None
DAC10Z	None
DAC12QS	AD667
DAC12QZ	AD667
DAC12M	AD7845
DAC14QM	AD1139
DAC16QM	AD1139
DAC100AAQ7	DAC100ACQ7
DAC100AAQ8	DAC100ACQ8
DAC100ABQ7	DAC100ACQ7
DAC100ABQ8	DAC100ACQ8
DAC100BBQ5/883C	DAC100ACQ5/883C
DAC100BCQ7	DAC100BBQ7
DAC100DDQ7	DAC100CCQ7
DAC312BR	DAC312ER
DAC888AX	DAC888EX
DAC888BX	DAC888EX
DAC1009	AD767
DAC1106	AD568
DAC1108	AD568
DAC1112	AD667
DAC1117	None
DAC1118	AD767
DAC1122	AD7541A
DAC1125	AD7533
DAC1132	AD667
DAC1137	None
DAC1408-6P	DAC1408-8P
DAC1408-7P	DAC1408-8P
DAC1408-7Q	DAC1408-8Q
DAC1408-GQ	DAC1408-8Q
DAC1420	None
DAC1422	None
DAC1423	None
DAC1508A-8Q	DAC1408-8Q
DAS09	AD8401
DAS1128	AD1341
DAS1150	None
DAS1151	None
DAS1155	None
DAS1156	None
DAS1157	DAS1158
DRC1605/06/07	Consult ADI
DRC1705/1706	Consult ADI
DRC1765/66	AD2S65/66
DSC1605/06/07	Consult ADI
DSC1705/1706	Consult ADI
DSC1765/66	None
DTM1716/17	None
HAS0802	HAS1202A
HAS1002	HAS1202A
HAS1202	HAS1202A
HDD1015	AD9712B
HDD1409	None
HDG Series	AD9701
HDG0805	AD9701
HDH0802	AD9713B
HDH1003	AD9713B
HDH1205	AD9713B
HDL3805	ADV453/ADV478
HDL3806	ADV453/ADV478
HDM1210	AD668/AD9713B
HDS0810E	AD9712B
HDS0820	AD9713B
HDS1015E	AD9712B
HDS1025	AD9713B
HDS1250	HDS1250A
HOS100AH/SH	None
HOS200	AD9620/30
HTC0300	HTC0300A
HTC0500	HTC0300A
IPA1751	IPA1764
IRDC1730/31/33	AD2S80A/82A
IVS100	None
MAH0801	AD9005B
MAH1001	AD9005B
MAS0801	AD9005B
MAS1001	AD9005B
MAS1202	AD9005B
MAT01/883C	MAT01AH/883C
MAT02BH	MAT02AH
MAT02BH/883C	MAT02AH/883C
MATV0811	AD9012/48
MATV0816	AD9012/48
MATV0820	AD9012/48
MCI1794	AD2S80A/82A
MDA Family	AD9712B/13B
MDD Series	AD9713B
MDH Family	AD9712B/13B
MDMS Family	AD9712B/13B
MDS Family	AD9712B/13B
MDSL Family	AD9712B/13B
MOD1005/20	AD9020/60
MOD1205	AD9005B
MUX08AQ	MUX08BQ
MUX24AQ	MUX24EQ
MUX24BQ	MUX24FQ
MUX16AT	MUX16ET
MUX16BT	MUX16FT
MUX200	None
OP01HJ	OP01J
OP01HZ	OP01HP
OP02BJ	OP02AJ
OP02BJ/883C	OP02AJ/883C
OP02EJ	OP07DJ
OP02EP	OP177GP
OP02EZ	OP177GZ
OP02J	OP02AJ
OP02/883C	OP02AZ/883C
OP04DY	OP04CY
OP04GBC	OP04NBC
OP04Y/883C	OP04AY/883C
OP05Z	OP05AZ
OP05/883C	OP05AZ/883C
OP06BJ/883C	OP06AJ/883C
OP06EZ	OP06GZ
OP06FZ	OP06GZ
OP08AJ	PM1008AJ
OP08AJ/883C	PM1008AJ/883C
OP08AZ/883C	PM1008AZ/883C
OP08CZ/883C	PM1008AZ/883C
OP08EJ	PM1008EJ
OP08EZ	PM1008EZ
OP09ARC/883C	OP11ARC/883C
OP09FY	OP09EY
OP12BZ	OP12AZ
OP12CZ	OP12AZ
OP12GZ	OP12FZ
OP14DZ	OP14CZ
OP14GRBC	OP14GBC
OP14J/883C	OP14AJ/883C
OP15BJ	OP15AJ
OP15BZ	OP15AZ
OP16BJ	OP16AJ
OP17BZ/883C	OP17AZ/883C
OP17CJ	OP17AJ
OP17FJ	OP17EJ

Model	Closest Recommended Equivalent
OP17FZ	OP17EZ
OP20CJ	OP20BJ
OP21GRBC	OP21GBC
OP215BJ	OP215AJ
OP215BJ/883C	OP215AJ/883C
OP215BZ	OP215AZ
OP215CZ/883C	OP215BZ/883
OP21BJ	OP21AJ
OP21BZ	OP21AZ
OP21EJ	OP21AJ
OP220BJ	OP220AJ
OP22AJ	OP22AJ/883C
OP22EJ	OP22AJ/883C
OP32BZ	OP32AZ
QMX01	None
RDC1725	Consult ADI
RDC1726	Consult ADI
RDC1728	Consult ADI
RDC1767	Consult ADI
RDC1768	Consult ADI
RSCT1621	AD2S80A/82A
RTI870	None
RTI980	None
RTI1200	RTI711 Series
RTI1201	RTI711 Series
RTI1202	RTI711 Series
RTI1230	None
RTI1231	None
RTI1232	None
RTI1240	None
RTI1241	None
RTI1242	None
RTI1243	None
RTI1250	None
RTI1251	None
RTI1252	None
RTI1270	None
RTM Series	Consult ADI
SAC1763	None
SBCD1752/53/56/57	None
SCDX1623	None
SCM1677	None
SDC1602/3/4	Consult ADI
SDC1700	Consult ADI
SDC1702	Consult ADI
SDC1703	Consult ADI
SDC1704	Consult ADI
SDC1711	None
SDC1721	None
SDC1725	Consult ADI
SDC1726	Consult ADI
SDC1728	Consult ADI
SDC1767	Consult ADI
SDC1768	Consult ADI
SERDEX	None
SHA1A	AD585
SHA2A	AD781
SHA3	AD585
SHA4	AD585
SHA5	None
SHA6	None
SHA1114	AD585
SHA1134	None
SHA1144	None
SHC85	AD585
SHM5/SHM5K	None
SMP10BY	SMP10AY
SMP10BY/883C	SMP10AY/883C
SPA1695	None
SSCT1621	AD2S80A/82A
SSCT1622/23	None
STB03	None
STM Series	Consult ADI
SW01BQ	SW01FQ
SW7510AQ	SW7510EQ
SW7510BQ	SW7510FQ
SW7511AQ	SW1577BQ
THC Family	HTC0300A
THS Family	HTC0300A
TSL1612	Consult ADI
1S10/20	AD2S80A/82A
1S14/24/44/64/74	AD2S83
1S60/61	AD2S80A/82A
2B30	2B31
2B35	None
2S20	AD2S80A/82A
2S54	Consult ADI
2S56	Consult ADI
2S58	Consult ADI
5S70/5S72	AD2S75
9S70/71/72	None
9S75/76/79	None
40	AD711
41	AD515A
42	AD549
43	AD549
44	AD845
45	AD744
46	AD844
47	AD845
48	AD845
50	AD844
51	AD844
52	AD707
102	AD845
106	AD711
107	AD711
108	AD845
110	AD845
118	AD711
120	AD844
141	AD711
142	AD845
143	AD845
146	AD382
148	AD549
149	AD844
153	AD517
161	None
163	None
165	None
170	None
171	None
180	AD OP07
183	AD707
184	AD707
220	None
230	None
231	None
232	None
233	None
234	None
235	None
260	AD707
261	OP177
272	None
273	None
274J	284J
275	AD210
276	None
279	286J
280	281
282J	292A
283J	292A
285	Consult ADI
287	None
288	AD210
293	AD210
294	AD210
301	310 (Module)
302	310 (Module)
311	AD549
350	None
422	None
424	AD534
425	AD534
426	AD534
427	None
428	AD538
432	None
433	AD534
434	AD534
435	AD734
436	AD734
440	None
441	None
442	None
450	AD652
452	None
454	AD537
456	AD537

Model	Recommended Equivalent
458	460
602J10	AD524
602J100	AD524
602K100	AD524
603	AD524
605	AD524
606	AD625
610	AD625
751	None
752	759
756	None
901	9022
903	905
904	9022
906	905
907	None
908	None
909	None
915	9022
921	None
926	None
927	None
928	922
931	None
932	None
933	None
935	None
942	None
944	None
946	None
947	Consult ADI
948	Consult ADI
951	None
952	970
953	966
956	None
959	960
964	None
965	940
967	None
968	945
971	None
972	None
973	975
974	None
977E	977

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In addition to the free publications, a group of technical reference books containing a wealth of tutorial material are available at reasonable cost. Subsystem chip sets are supported with hardware, software, and user documentation, at prices related to content.

An overview of Analog Devices is available in a 20-page brochure entitled: *Analog.Digital.Solutions.* It discusses: a vision of the future and the key role of signal processing using analog, mixed-signal, and digital ICs; what we offer electronic OEMs in standard-function ICs and in devices for such specialized markets as computers, communications, transportation and industry; as well as our capabilities and resources, our commitment to customer support and satisfaction, the global scale of our business, and our commitment to the future.

Brief descriptions of typical technical publications appear below. For copies of any items, to subscribe to any of our free serials or to request any other publications, please get in touch with your nearest sales office or the Analog Devices literature center; phone (617) 461-3392; toll free in U.S., 800-262-5643; or fax (617) 821-4273.

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SPECIAL LINEAR REFERENCE MANUAL—1992. Data sheets and selection guides to Analog Multipliers/Dividers, Signal Compression Components, RMS-to-DC Converters, Mass Storage Components, ATE Components, Special Function Components, Matched Transistors, Temperature Sensors, Signal Conditioning Components, Automotive Components, Digital Signal Processing Products, Mixed-Signal ASICs, Power Supplies.

DATA CONVERTER REFERENCE MANUAL—1992: Volumes 1 and 2. Data sheets and selection guides on A/D and D/A Converters, V/F and F/V Converters, Synchro/Resolver-to-Digital Converters, Sample/Track-Hold Amplifiers, Switches and Multiplexers, Voltage References, Data-Acquisition Subsystems, Analog I/O Ports, Communications Products, Bus Interface and I/O Products, Application-Specific ICs, Digital Panel Meters, Power Supplies.

MILITARY/AEROSPACE REFERENCE MANUAL—1994. Information and data on products available with processing in accordance with MIL-STD-883. Data sheets and selection guides on Operational Amplifiers, A/D and D/A Converters, Digital Signal Processing, Instrumentation Amps, Multipliers/Dividers, V/F & F/V Converters, Switches & Multiplexers, Sample/Track-Hold Amplifiers, Voltage References and Special Function Components.

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High-Speed Op Amp Sliding Selection Guide. A slide rule for selecting op amps by bandwidth or viewing characteristics by model number. Lists dynamic specs such as slew rate, settling time, differential gain and phase, voltage and current noise, supply voltage and current, and many more.

Instrumentation Amplifier Application Guide, by Charles Kitchin and Lew Counts. Its 44-pages include basic instrumentation-amplifier ("in-amp") theory, design considerations, applications, specifications, and products—plus a brief bibliography and two indexes (by topic and by device model number).

Multiple Digital-to-Analog Converter Integrated Circuits Selection Guide. A 32-page guide for the designer who wants to save space and cost in applications calling for from two to eight or more DACs and resolutions from 6 to 18 bits. Devices include triple 6-, 8-, and 10-bit video DACs, dual 18-bit audio DACs, 8-bit octuples, and 12- and 14-bit quads.

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Personal Sound Architecture. An 8-page brochure describing a programmable architecture for integrating sound into personal computers using software-based technologies and IC chipsets (including Analog Devices DSPs, codecs, and other peripherals) for sound cards.

RMS-to-DC Conversion Application Guide 2nd Edition by C. Kitchin and L. Counts (1986—61 pages). RMS-DC Conversion: Theory, Basic Design Considerations; RMS Application

Circuits; Testing Critical Parameters; Input Buffer Amplifier Requirements; Programs for Computing Errors, Ripple and Settling Time.

Sampling Analog-to-Digital Converter Integrated Circuits—1992 Short Form Selection Guide. Its 28 pages cover 35 different models with resolutions from 8 to 16 bits, and 12-bit resolution up to 20 Msps. Besides block diagrams and key specs of each product, the booklet includes a detailed discussion of selection issues and a selection table sorted by resolution and speed.

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NEW—*SYSTEM APPLICATIONS GUIDE.* Norwood MA: Analog Devices, Inc. (1993), 800 pages, 8 1/2″ × 11″ softcover. Precision sensor signal conditioning and transmission; multiplexing; programmable-gain amplifiers; high-accuracy topics: sample-holds, references, conversion; audio; video; high-speed topics: signals & systems, amplification, ADC selection, interfacing, performance verification; sigma-delta conversion; wide dynamic range; direct digital synthesis, signal computing, motor control. $30.00

NEW—*ADSP-2100 FAMILY APPLICATIONS HANDBOOK, Volume I:* A companion to the ADSP-21000 family of floating-point processors. Introduction; Trigonometric, mathematical, and transcendental functions; Matrix functions; FIR and IIR filters; Multirate filters; Adaptive filters; Fourier transforms; Graphics; Image processing; JTAG downloader; Index. Includes 33 figures, 14 tables, and 61 program listings. $22.00

ADSP-2100 FAMILY USER'S MANUAL. Englewood Cliffs NJ: Prentice Hall (1993). A comprehensive reference for Analog Devices' ADSP-2100 Family, an architectural and code-compatible set of 16-bit fixed-point DSP microprocessors that offer varying levels of feature integration. Topics covered in this manual include: Base architecture—computation units, program sequencer, data-address generators; Integrated on-chip peripherals—serial ports, timer, host interface port, A/D and D/A converters; System hardware and memory interfacing; Programmer's model and instruction-set reference; System design and programming examples. $24.00

AMPLIFIER APPLICATIONS GUIDE, by the Applications Engineering Staff of Analog Devices and edited by Walt Kester, published by Analog Devices (1992). 648 pages of timely and practical information on amplifiers—including operational, audio, instrumentation, video, and log amps. Topics include: Introduction; Precision transducer interfaces; High impedance, low current; Single-supply, low-power; Audio; Filtering, Driving ADCs; Video and other high-speed applications; Nonlinear circuit applications; Unusual applications; Subtleties; Hardware techniques; Simulation; and a complete Index. $20.00

ANALOG-DIGITAL CONVERSION HANDBOOK: Third Edition, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Englewood Cliffs, NJ: Prentice Hall (1986). A comprehensive guide to A/D and D/A converters and their applications. This third edition of our classic is in hardcover and has more than 700 pages, an Index, a Bibliography, and much new material, including: video-speed, synchro-resolver, V/F, high-resolution, and logarithmic converters, ICs for DSP, and a "Guide for the Troubled." Seven of its 22 chapters are totally new. $32.95

DIGITAL SIGNAL-PROCESSING APPLICATIONS USING THE ADSP-2100 FAMILY, by the Applications Staff of Analog Devices, DSP Division; edited by Amy Mar (628 pages). Englewood Cliffs, NJ: Prentice Hall (1990). Bridge the gap between DSP algorithms and their real-world implementation on state-of-the-art signal processors. Each chapter tackles a specific application topic, briefly describing the algorithm and discussing its implementation on the ADSP-2100 family of DSP chips. Comprehensive source-code listings are complete with comments and accompanied by explanatory text. Programs are listed on a pair of supplementary diskettes—furnished with the book. Application areas include fixed- and floating-point arithmetic, function approximation, digital filters, one- and two-dimensional FFTs, image processing, graphics, LP speech coding, PCM, ADPCM, high-speed modem algorithms, DTMF coding, sonar beam-forming. Additional topics include memory interface, multiprocessing, and host interface. The book can serve as a companion to *Digital Signal Processing in VLSI*. **Now in paperback**; its price includes a diskette. $30.00

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DIGITAL SIGNAL PROCESSING IN VLSI, by Richard J. Higgins. Englewood Cliffs, NJ: Prentice Hall (1990). An introductory 614-page guide for the engineer and scientist who needs to understand and use DSP algorithms and special-purpose DSP hardware ICs—and the software tools developed to carry them out efficiently. Real-World Signal Processing; Sampled Signals and Systems; The DFT and the FFT Algorithm; Digital Filters; The Bridge to VLSI; Real DSP Hardware; Software Development for the DSP System; DSP Applications; plus Bibliography and Index. $38.00

DIGITAL SIGNAL PROCESSING LABORATORY: Using the ADSP-2101 Microcomputer, by Vinay K. Ingle and John G. Proakis (Northeastern University). Englewood Cliffs, NJ: Prentice Hall (1991). Contents: Introduction to the ADSP-2100/2101 family; ADSP-2101 instruction set overview; Overview of development tools; Getting started with the ADSP-2101; Laboratory experiments using the ADSP-2101; FIR filter implementation; IIR filter implementation; Fast Fourier transform implementation; Applications in communications; Adaptive filters and their applications; References; Index. $24.00

HIGH-SPEED DESIGN SEMINAR, published by Analog Devices (1990). A 496-page guide to the practical application of high-speed semiconductor devices in processing of analog signals. Topics include: data conversion, digital video applications, high-speed sample-holds and operational amplifiers, nonlinear signal processors (including log amps), comparators and pin electronics, time-delay generators, phase-locked loops, direct digital synthesis, computer graphics and RAMDACs, and high-speed techniques. $20.00

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NONLINEAR CIRCUITS HANDBOOK: Designing with Analog Function Modules and ICs, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Norwood, MA: Analog Devices, Inc. (1974). A 540-page guide to multiplying and dividing, squaring and rooting, rms-to-dc conversion, and multifunction devices. Principles, circuitry, performance, specifications, testing, and application of these devices—contains 325 illustrations. $5.95

TRANSDUCER INTERFACING HANDBOOK: A Guide to Analog Signal Conditioning, edited by Daniel H. Sheingold. Norwood, MA: Analog Devices, Inc. (1980). A book for the electronic engineer who must interface transducers for temperature, pressure, force, level, or flow to electronics, these 260 pages tell how transducers work—as circuit elements—and how to connect them to electronic circuits for effective processing of their signals. $14.50

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